# Zhiang Wang

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## Research interests

- Modeling and optimization in VLSI CAD
- Software/hardware co-design
- Gpu acceleration

## Education

**University of California, San Diego** Expected June 2024
*Ph.D in Electrical and Computer Engineering* *San Diego, CA*
- Advisor: Prof. Andrew B. Kahng

**University of Science and Technology of China (USTC)** Sep. 2015 - Jun. 2019
*Bachelor in Applied Physics, School of Physics (GPA: 3.98/4.30) (Rank top 1/77)* *Hefei, China*

## Experience

**Graduate Researcher** Sep. 2019 – Present
*University of California, San Diego* *San Diego, CA*
- Participated in an open-source research project (OpenROAD) supported by DARPA.
- Participated in an open-source project for automated machine learning hardware synthesis (VeriGOOD-ML) supported by DARPA.

**Intern-Software Engineer** Jun. 2022 – Sep. 2022
*Cadence Design Systems* *San Jose, CA*

## Projects

**Hier-RTLMP** **[c2, c5, j1]** (OpenROAD Integrated) | *C++14, SWIG, Tcl* Sep. 2019 – Present
- A macro placer which utilizes RTL information and tries to "mimic" the interaction between the frontend RTL designer and the backend physical design engineer to produce human-quality floorplans
- Implement the whole project based on OpenDB and OpenSTA infrastructure
- Available as "partition_design" and "rtl_macro_placer" Tcl commands in OpenROAD
- Able to handle machine learning accelerators with hundreds or thousands of macros

**TritonPart** (OpenROAD Integrated) | *C++14, SWIG, Tcl* Sep. 2019 – Present
- Multidimensional real-value weights on vertices and hyperedges
- Timing-driven partitioning framework
- Embedding-aware partitioning

**SpecPart** **[c4, j2]** | *Julia* Sep. 2021 – Present
- A supervised spectral framework for hypergraph partitioning solution improvement
- Hypergraph Partitioning for VLSI: Benchmarks, Code and Leaderboard

**VeriGOOD-ML** **[c1, c3]** Sep. 2019 – Present
- Implement the backend flow for all the benchmarks
- Build machine learning models for power-performance-area (PPA) prediction
- Build machine learning models for design space exploration (software/hardware co-design)

**RL-based Macro Placement** **[c6]** Sep. 2019 – Present
- Provide testcase along with open enablements and open-source / commercial EDA tool flows
- Enable anyone to perform RL-based macro placement for their own designs using **Google's Circuit Training**
- Implement missing or binarized elements of **Google's Circuit Training**

## Papers

**All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order.**

### Conferences

[c1] H. Esmaeilzadeh, S. Ghodrati, J. Gu, S. Guo, A. B. Kahng, J. K. Kim, S. Kinzer, R. Mahapatra, S. D. Manasi, E. Mascarenhas, S. S. Sapatnekar, R. Varadarajan, **Z. Wang**, H. Xu, B. R. Yatham and Z. Zeng, "VeriGOOD-ML: An Open-Source Flow for Automated ML Hardware Synthesis", *Proc. ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, 2021, pp. 1-7.

[c2] A. B. Kahng, R. Varadarajan and **Z. Wang**, "RTL-MP: Toward Practical, Human-Quality Chip Planning and Macro Placement", *Proc. ACM/IEEE International Symposium on Physical Design (ISPD)*, 2022.

[c3] H. Esmaeilzadeh, S. Ghodrati, A. B. Kahng, J. K. Kim, S. Kinzer, S. Kundu, R. Mahapatra, S. D. Manasi, S. S. Sapatnekar, **Z. Wang** and Z. Zeng, "Physically Accurate Learning-based Performance Prediction of Hardware-accelerated ML Algorithms", *Proc. ACM/IEEE Workshop on Machine Learning for CAD*, 2022.

[c4] I. Bustany, A. B. Kahng, Y. Koutis, B. Pramanik and **Z. Wang**, "SpecPart: A Supervised Spectral Framework for Hypergraph Partitioning Solution Improvement" *Proc. ACM/IEEE International Conference on Computer-Aided Design*, 2022. **(Best Paper Award)**

[c5] J. Jung, A. B. Kahng, R. Varadarajan and **Z. Wang**, "IEEE CEDA DATC: Expanding Research Foundations for IC Physical Design and ML-Enabled EDA", *Proc. ACM/IEEE International Conference on Computer-Aided Design*, 2022. **(Invited Paper)**

[c6] C.-K. Cheng, A. B. Kahng, S. Kundu, Y. Wang and Z. Wang, "Assessment of Reinforcement Learning for Macro Placement", *Proc. ACM/IEEE International Symposium on Physical Design*, 2023.

### Journals

[j1] A. B. Kahng, R. Varadarajan and **Z. Wang**, "Hier-RTLMP: A Hierarchical Automatic Macro Placer for Large-scale Complex IP Blocks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. (under review)

[j2] I. Bustany, A. B. Kahng, I. Koutis, B. Pramanik and **Z. Wang**, "K-SpecPart: A Supervised Spectral Framework for Multi-Way Hypergraph Partitioning Solution Improvement", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. (under review)

### Book Chapters

[b1] A. B. Kahng, and **Z. Wang**, "ML for Design QoR Prediction", *Machine Learning Applications in Electronic Design Automation*, Springer. (Invited Book Chapter)

## Technical Skills

**Languages**: Python, C/C++, Tcl, Verilog, MATLAB, CUDA
**EDA Tools**: Cadence Innovus, Synopsys Design Compiler