

Automated Implementation of the Digital Configuration Interface for Application Specific Integrated Circuits

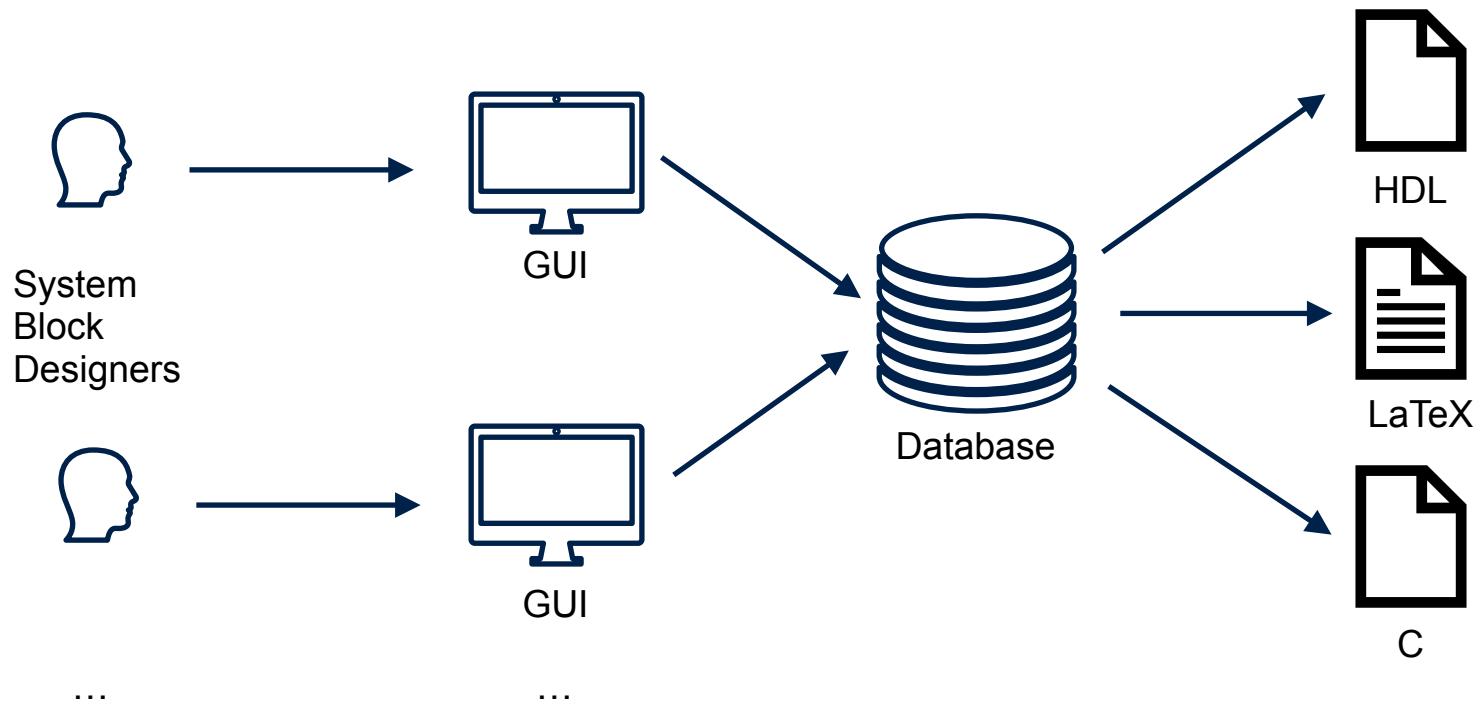
Zhihong Lei

Mid-Term Master Thesis Presentation

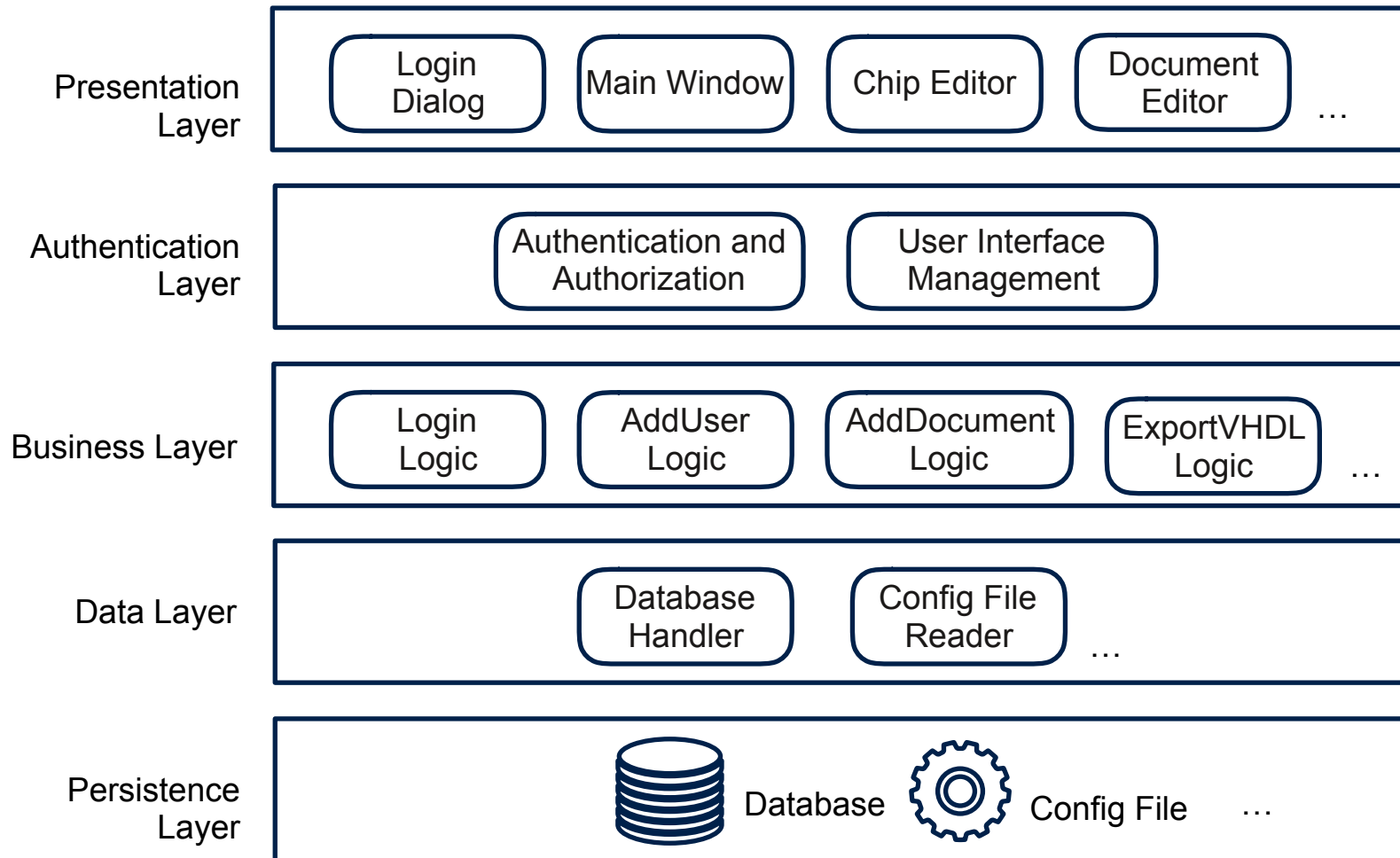
Supervisor: Johannes Bastl, M.Sc

Univ.-Prof. Dr.-Ing. Stefan Heinen
Integrated Analog Circuits and RF Systems Laboratory

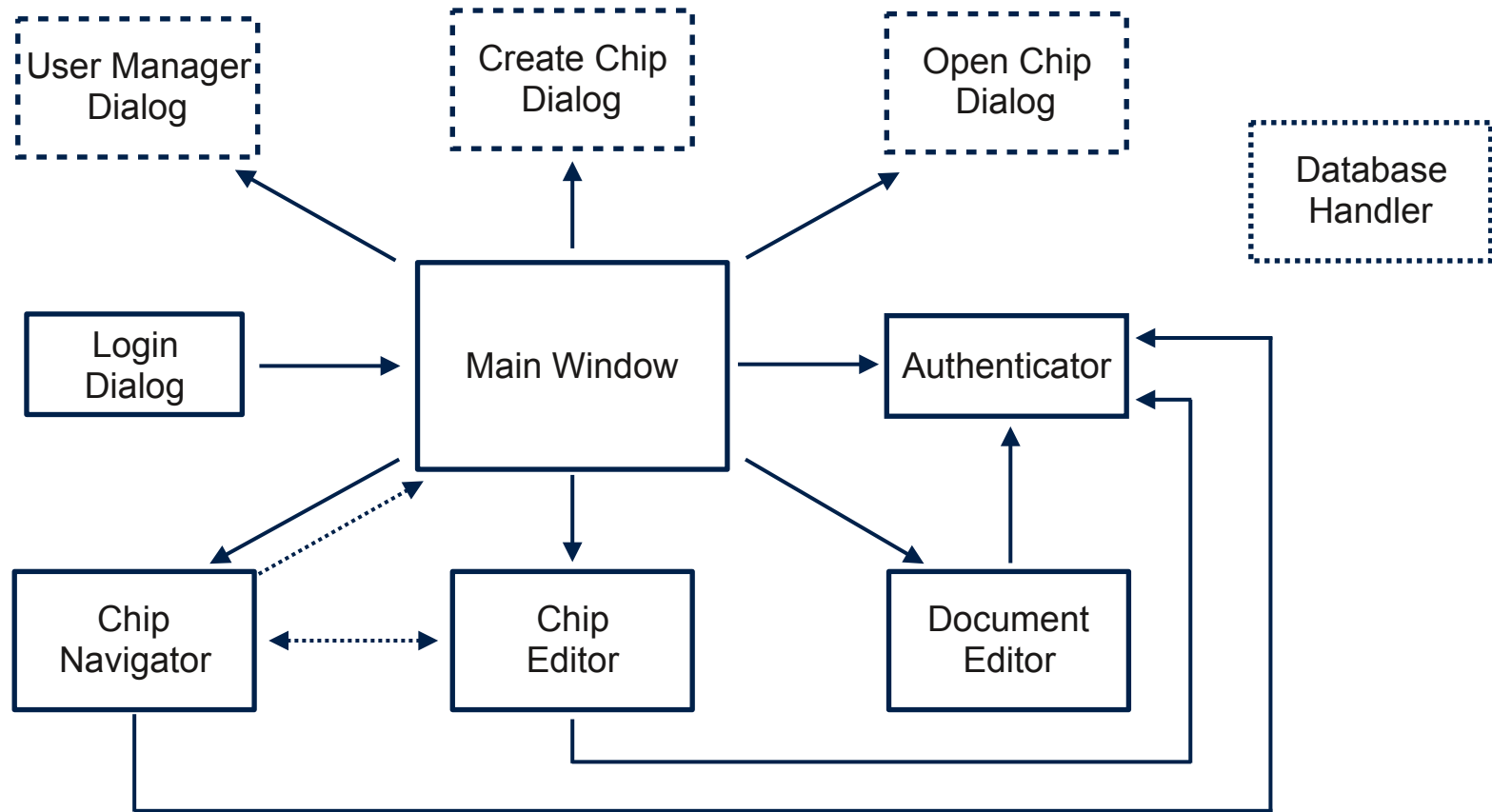
- A database centered software that aids in implementation of digital configuration interface for ASICs



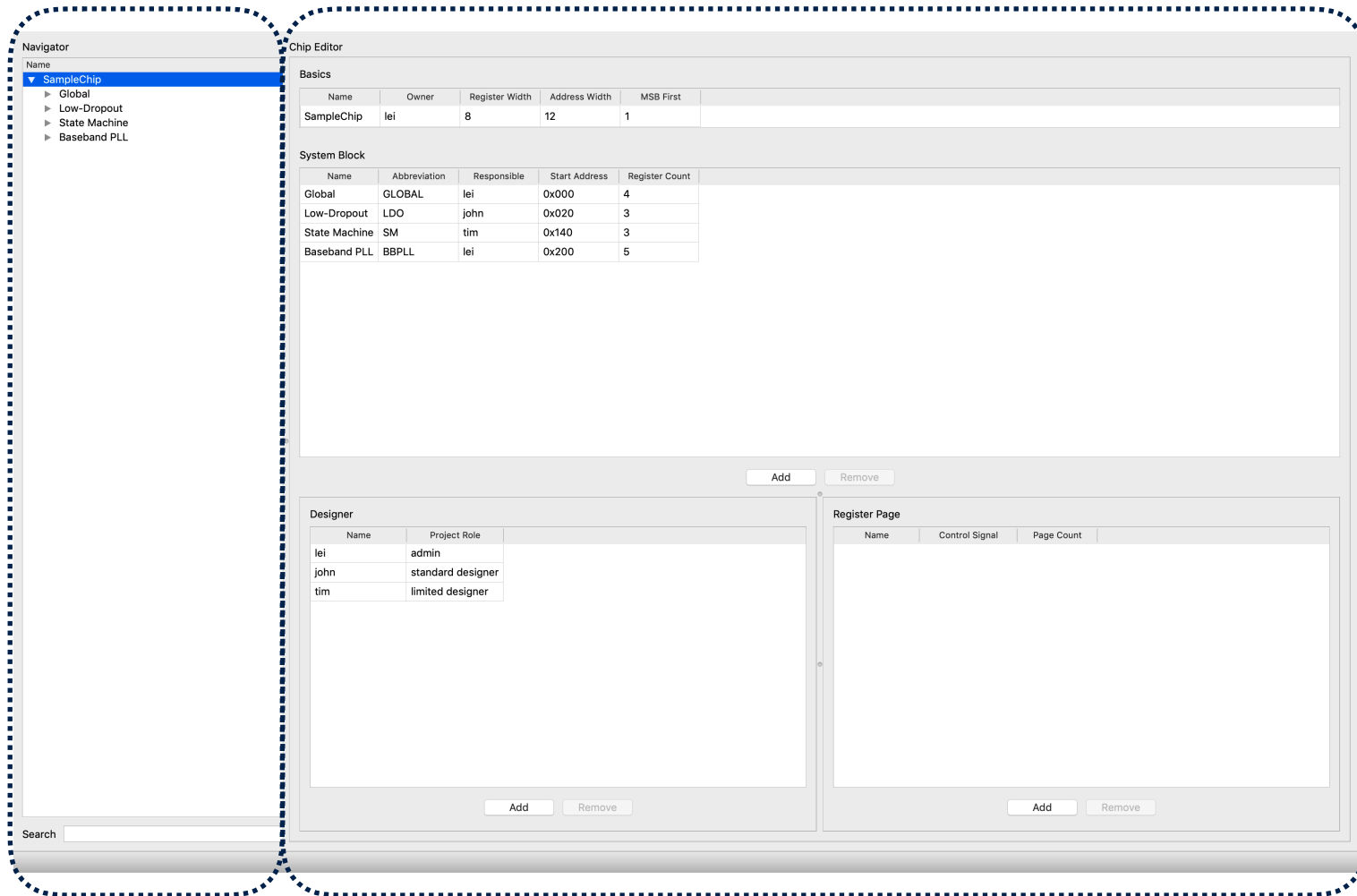
Designed Architecture



Object-Oriented Programming in Practice



Main Window



Chip Navigator

Work Area

Main Window

The screenshot displays the Main Window interface, which is divided into three main sections: the Chip Navigator, the Chip Editor, and the Document Editor.

Chip Navigator: Located on the left, it shows a tree view of the project structure. The 'SampleChip' is selected, and its sub-components are listed: Global, Low-Dropout, State Machine, and Baseband PLL.

Chip Editor: The central area, divided into two panes. The top pane, titled 'System Block', contains a table with the following data:

Name	Abbreviation	Responsible	Start Address	Register Count
Global	GLOBAL	lei	0x000	4
Low-Dropout	LDO	john	0x020	3
State Machine	SM	tim	0x140	3
Baseband PLL	BBPLL	lei	0x200	5

The bottom pane, titled 'Designer', contains a table with the following data:

Name	Project Role
lei	admin
john	standard designer
tim	limited designer

Document Editor: The rightmost section, titled 'Table of Content', lists the following sections:

- Global
 - GLOBAL_RESETB1_REG
 - GLOBAL_RESETB2_REG
 - GLOBAL_initALL_REG
 - GLOBAL_MAIN_REG
- Low-Dropout
 - LDO_D_VOUT_REG
 - LDO_CLK_VOUT_REG
 - LDO_BOOST_REG
- State Machine
 - SM_MAIN_REG
 - SM_COMMAND_REG
 - SM_TX_SET_REG
- Baseband PLL
 - BBPLL_CTRL_REG
 - BBPLL_FREQ_H_REG
 - BBPLL_FREQ_M_REG
 - BBPLL_FREQ_L_REG
 - BBPLL_POSTDIV_OSCICTRL_REG

Below the Table of Content, the 'Global' section is expanded, showing the 'GLOBAL_RESETB1_REG - 0x000' register. It includes a table with the following data:

7	6	5	4	3	2	1	0
...	WUR_RESETB	OSCI_CTRL_RESETB	ULP_RESET	SM_RESETB	TX_RESETB	DEM_RESETB	PLL_RESETB
.	0	0	0	0	0	0	0

Below the table, the following list of register assignments is provided:

- WUR_RESETB is written to WAKEUP<3>
- OSCI_CTRL_RESETB is written to OSCI_CTRL<0>
- ULP_RESET is written to ULP_MAIN<1> and inverted to ULP_MAIN<4>
- SM_RESETB is written to SM_MAIN<1>
- TX_RESETB is written to TX_MAIN<5>
- DEM_RESETB is written to DEM_MAIN<7>
- PLL_RESETB is written to PLL_MAIN<3>

The 'GLOBAL_RESETB2_REG - 0x001' register is also shown, with a table and a list of register assignments:

7	6	5	4	3	2	1	0
...	RXADC_RESETB	BBPLL_RESETB	OTP_RESETB	RSSI_CTRL_RESETB	SLEEP_VREF_RESETB		
.	.	.	0	0	0	0	0

Below the table, the following list of register assignments is provided:

- RXADC_RESETB is written to RXADC_SET_REG<7>
- BBPLL_RESETB is written to BBPLL_CTRL_REG<7>
- OTP_RESETB is written to OTP_CONFIG_REG<0>
- RSSI_CTRL_RESETB is written to RSSI_CTRL_REG<3>
- SLEEP_VREF_RESETB is written to SLEEP_VREF_REG<2>

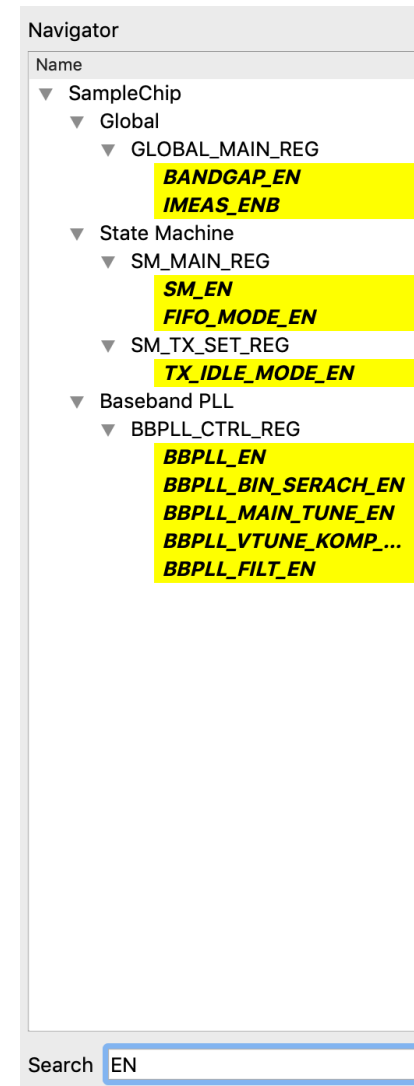
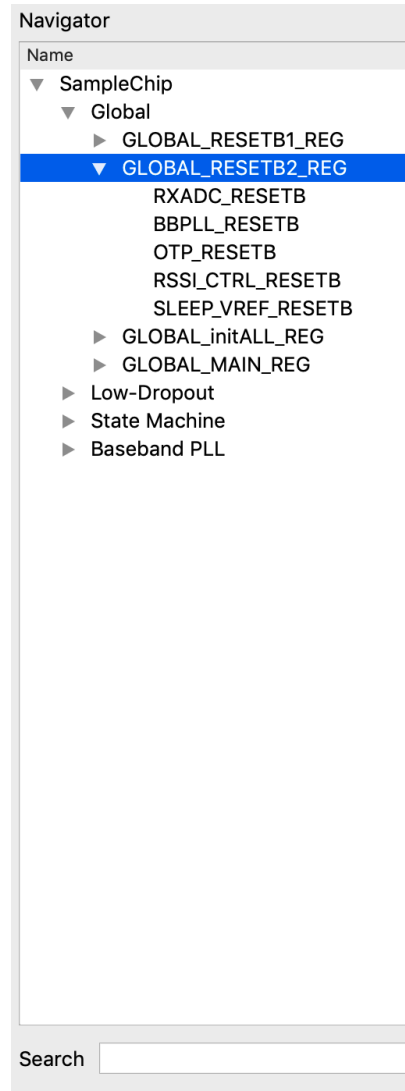
Chip Navigator

Work Area

Chip Navigator

4-level tree widget
chip, block, register, signal

Search area



■ Chip-level view

Chip Editor

Basics

Name	Owner	Register Width	Address Width	MSB First
SampleChip	lei	8	12	1

System Block

Name	Abbreviation	Responsible	Start Address	Register Count
Global	GLOBAL	lei	0x000	4
Low-Dropout	LDO	john	0x020	3
State Machine	SM	tim	0x140	3
Baseband PLL	BBPLL	lei	0x200	5

Add Remove

Designer

Name	Project Role
lei	admin
john	standard designer
tim	limited designer

Add Remove

Register Page

Name	Control Signal	Page Count
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Add Remove

Basic Information about the chip

List of system blocks

Edit System Block

Block Name

Abbreviation

Responsible +

Start Address

Cancel OK

Designers

List of register pages

■ Block-level View - Signals

Chip Editor

Signal Register

Name	Width	Signal Type	Register Type	Value	Port
WUR_RESETB	1	Control Signal	R/W	0x0	0
OSCI_CTRL_RESETB	1	Control Signal	R/W	0x0	0
ULP_RESET	1	Control Signal	R/W	0x0	0
SM_RESETB	1	Control Signal	R/W	0x0	0
TX_RESETB	1	Control Signal	R/W	0x0	0
DEM_RESETB	1	Control Signal	R/W	0x0	0
PLL_RESETB	1	Control Signal	R/W	0x0	0
RXADC_RESETB	1	Control Signal	R/W	0x0	0
BBPLL_RESETB	1	Control Signal	R/W	0x0	0
OTP_RESETB	1	Control Signal	R/W	0x0	0
RSSI_CTRL_RESETB	1	Control Signal	R/W	0x0	0
SLEEP_VREF_RESETB	1	Control Signal	R/W	0x0	0
GLOBAL_INIT	8	Control Signal	R/W	0x00	1
IMPROVE_SPI_COMMS	1	Control Signal	R/W	0x0	0

Add Remove

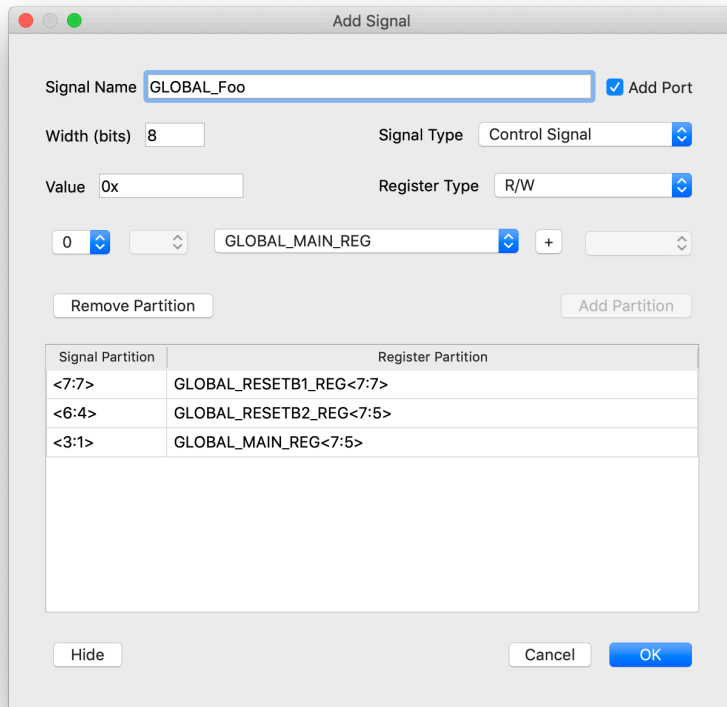
Signal Partition	Register Partition
<0:0>	GLOBAL_RESETB1_REG<6:6>

Add Remove

All signals in current block

Signal-Register mappings

■ Add/Edit signals



Signal Name: GLOBAL_Foo ☒ Add Port

Width (bits): 8 Signal Type: Control Signal

Value: 0x Register Type: R/W

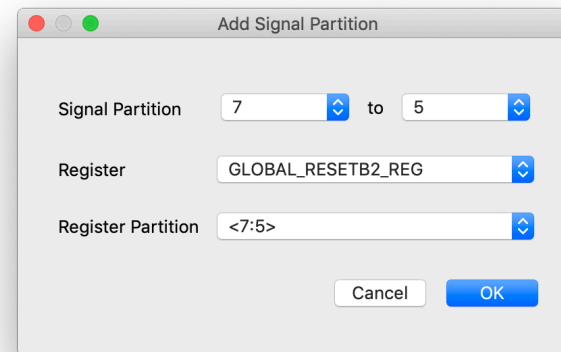
0 GLOBAL_MAIN_REG +

Remove Partition Add Partition

Signal Partition	Register Partition
<7:7>	GLOBAL_RESETB1_REG<7:7>
<6:4>	GLOBAL_RESETB2_REG<7:5>
<3:1>	GLOBAL_MAIN_REG<7:5>

Hide Cancel OK

Add/Edit Multi-bit Signal dialog



Signal Partition: 7 to 5

Register: GLOBAL_RESETB2_REG

Register Partition: <7:5>

Cancel OK

Add Signal-Register Mapping dialog

■ Block-level View - Registers

Chip Editor

Signal Register

Name	Register Type	Presumed Address
GLOBAL_RESETB1_REG	R/W	0x000
GLOBAL_RESETB2_REG	R/W	0x001
GLOBAL_initALL_REG	R/W	0x002
GLOBAL_MAIN_REG	R/W	0x003

Add Remove

Register Partition	Signal Partition
<6:6>	WUR_RESETB<0:0>
<5:5>	OSCI_CTRL_RESETB<0:0>
<4:4>	ULP_RESETB<0:0>
<3:3>	SM_RESETB<0:0>
<2:2>	TX_RESETB<0:0>
<1:1>	DEM_RESETB<0:0>
<0:0>	PLL_RESETB<0:0>

All registers in current block

Add Register

Register Name GLOBAL_Foo_REG

Register Type R/W

Cancel OK

Register-Signal mappings

Add Register dialog

Document Editor

Text	Change the output voltage of the CLK LDO.
Text	$V_{CLK} = V_{ref, 500mV} \cdot \frac{174k\Omega - 2k\Omega}{65k\Omega - 2k\Omega} \cdot LDO_D_VOUT<4:0>$. The init value corresponds to 1.3V. 1 LSB corresponds to about 20mV around the init value. Digital tuning range is 1.0V...2.0V but the output is about 200mV lower than VDD for maximum output current (80 mA).

Type

Text

Content

$V_{CLK} = V_{ref, 500mV} \cdot \frac{174k\Omega - 2k\Omega}{65k\Omega - 2k\Omega} \cdot LDO_D_VOUT<4:0>$. The init value corresponds to 1.3V. 1 LSB corresponds to about 20mV around the init value. Digital tuning range is 1.0V...2.0V but the output is about 200mV lower than VDD for maximum output current (80 mA).

Preview

$$V_{CLK} = V_{ref, 500mV} \cdot \frac{174k\Omega - 2k\Omega \cdot LDO_D_VOUT<4:0>}{65k\Omega - 2k\Omega \cdot LDO_D_VOUT<4:0>}$$

The init value corresponds to 1.3V. 1 LSB corresponds to about 20mV around the init value. Digital tuning range is 1.0V...2.0V but the output is about 200mV lower than VDD for maximum output current (80 mA).

Hide Preview

Cancel

OK

Add

Remove

List of documents of currently selected block/register/signal

Document editing area

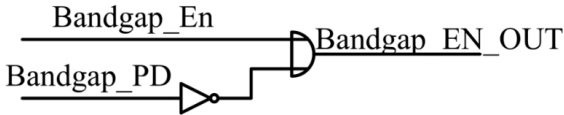
Preview: HTML web viewer supporting LaTeX

Type

Caption

Path

Preview



Bandgap power down mechanism

Image

Type

Row Column

Caption

Table

TX_MODE	Band Operation
00	2.4 GHz
01	800 MHz
10	433 MHz
11	433 MHz

Preview

TX_MODE	Band Operation
00	2.4 GHz
01	800 MHz
10	433 MHz
11	433 MHz

Table

Navigator

Name

- ▼ SampleChip
 - ▶ Global
 - ▶ Low-Dropout
 - ▶ State Machine
 - ▶ Baseband PLL

Search

Document Editor

Table of Content

1. [Global](#)
 - [GLOBAL_RESETB1_REG](#)
 - [GLOBAL_RESETB2_REG](#)
 - [GLOBAL_initALL_REG](#)
 - [GLOBAL_MAIN_REG](#)
2. [Low-Dropout](#)
 - [LDO_D_VOUT_REG](#)
 - [LDO_CLK_VOUT_REG](#)
 - [LDO_BOOST_REG](#)
3. [State Machine](#)
 - [SM_MAIN_REG](#)
 - [SM_COMMAND_REG](#)
 - [SM_TX_SET_REG](#)
4. [Baseband PLL](#)
 - [BBPLL_CTRL_REG](#)
 - [BBPLL_FREQ_H_REG](#)
 - [BBPLL_FREQ_M_REG](#)
 - [BBPLL_FREQ_L_REG](#)
 - [BBPLL_POSTDIV_OSCICTRL_REG](#)

Global

GLOBAL_RESETB1_REG - 0x000

7	6	5	4	3	2	1	0
...	WUR_RESETB	OSCI_CTRL_RESETB	ULP_RESET	SM_RESETB	TX_RESETB	DEM_RESETB	PLL_RESETB
.	0	0	0	0	0	0	0

- WUR_RESETB is written to WAKEUP<3>
- OSCI_CTRL_RESETB is written to OSCI_CTRL<0>
- ULP_RESET is written to ULP_MAIN<1> and inverted to ULP_MAIN<4>
- SM_RESETB is written to SM_MAIN<1>
- TX_RESETB is written to TX_MAIN<5>
- DEM_RESETB is written to DEM_MAIN<7>
- PLL_RESETB is written to PLL_MAIN<3>

GLOBAL_RESETB2_REG - 0x001

7	6	5	4	3	2	1	0
...	RXADC_RESETB	BBPLL_RESETB	OTP_RESETB	RSSI_CTRL_RESETB	SLEEP_VREF_RESETB
.	.	.	0	0	0	0	0

- RXADC_RESETB is written to RXADC_SET_REG<7>
- BBPLL_RESETB is written to BBPLL_CTRL_REG<7>
- OTP_RESETB is written to OTP_CONFIG_REG<0>
- RSSI_CTRL_RESETB is written to RSSI_CTRL_REG<3>
- SLEEP_VREF_RESETB is written to SLEEP_VREF_REG<2>

Live Demo ...

Time Table

Timeline	Work
15.07	Implementation of export function of LaTeX document and VHDL source code
31.07	Implementation of database exception handling; refining the software
31.08	Deployment; trial run; thesis writing
30.09	Finalization

Thank you