Automated Implementation of the Digital Configuration Interface for Application Specific Integrated Circuits

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Mid-Term Master Thesis Presentation

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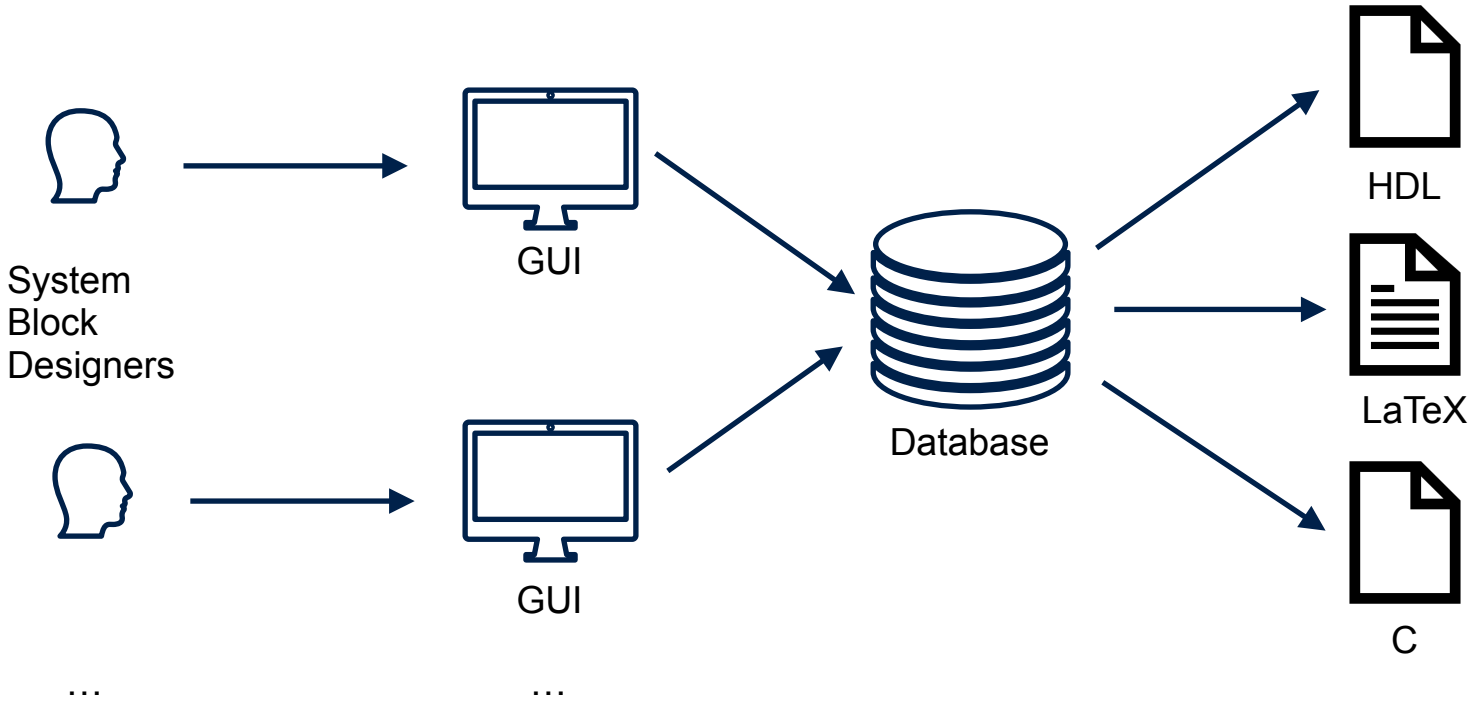
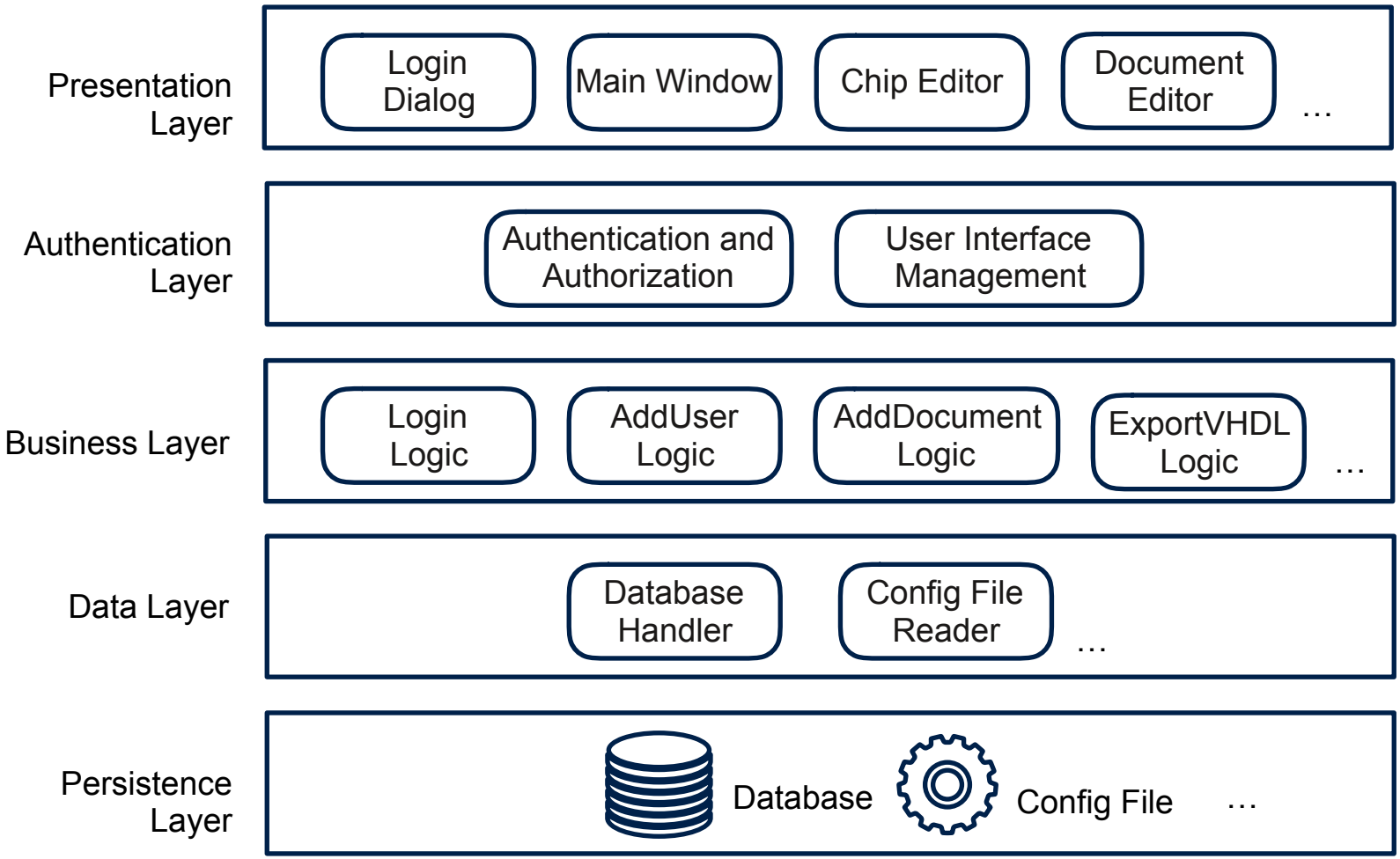
Proposal

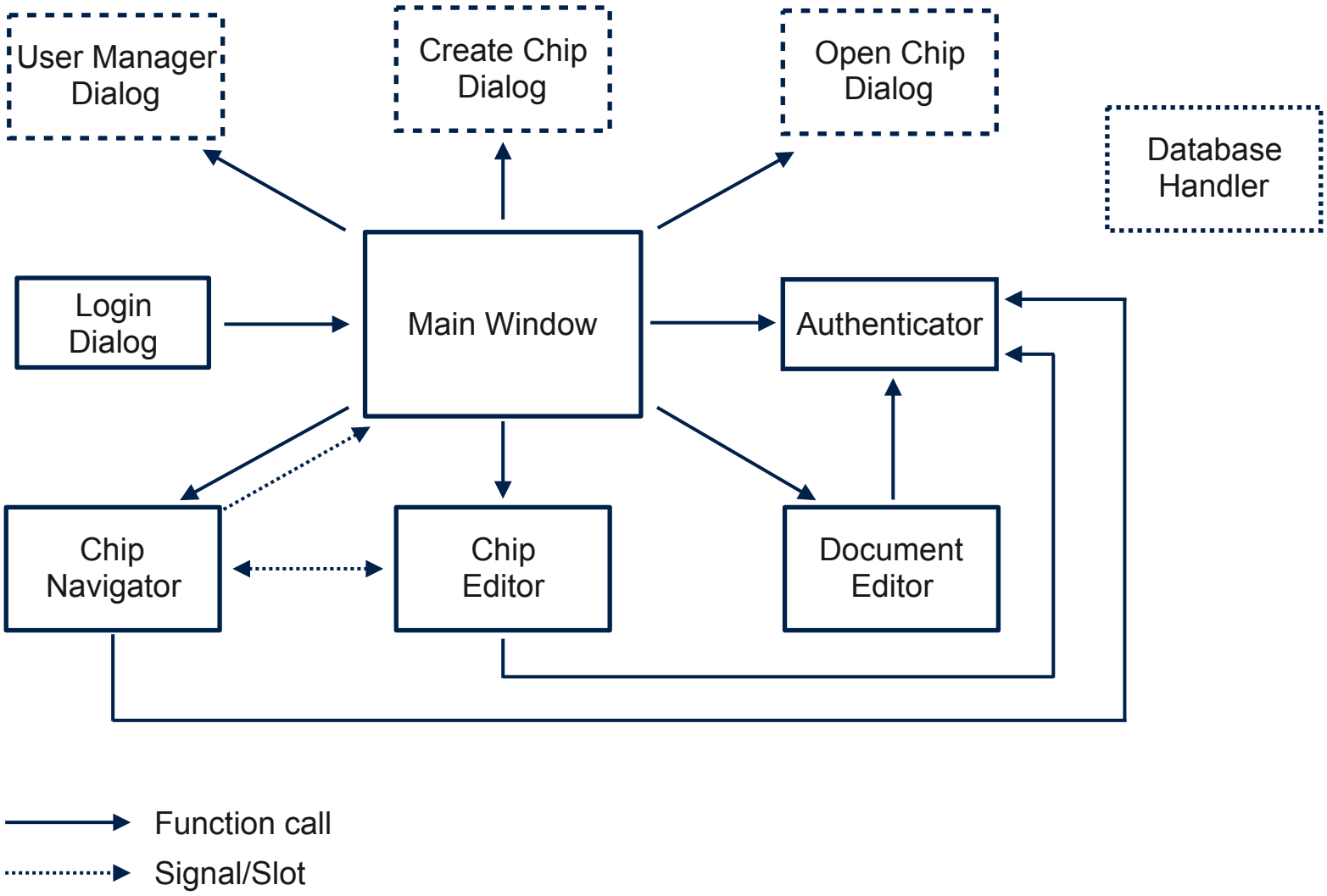
- A database centered software that aids in implementation of digital configuration interface for ASICs



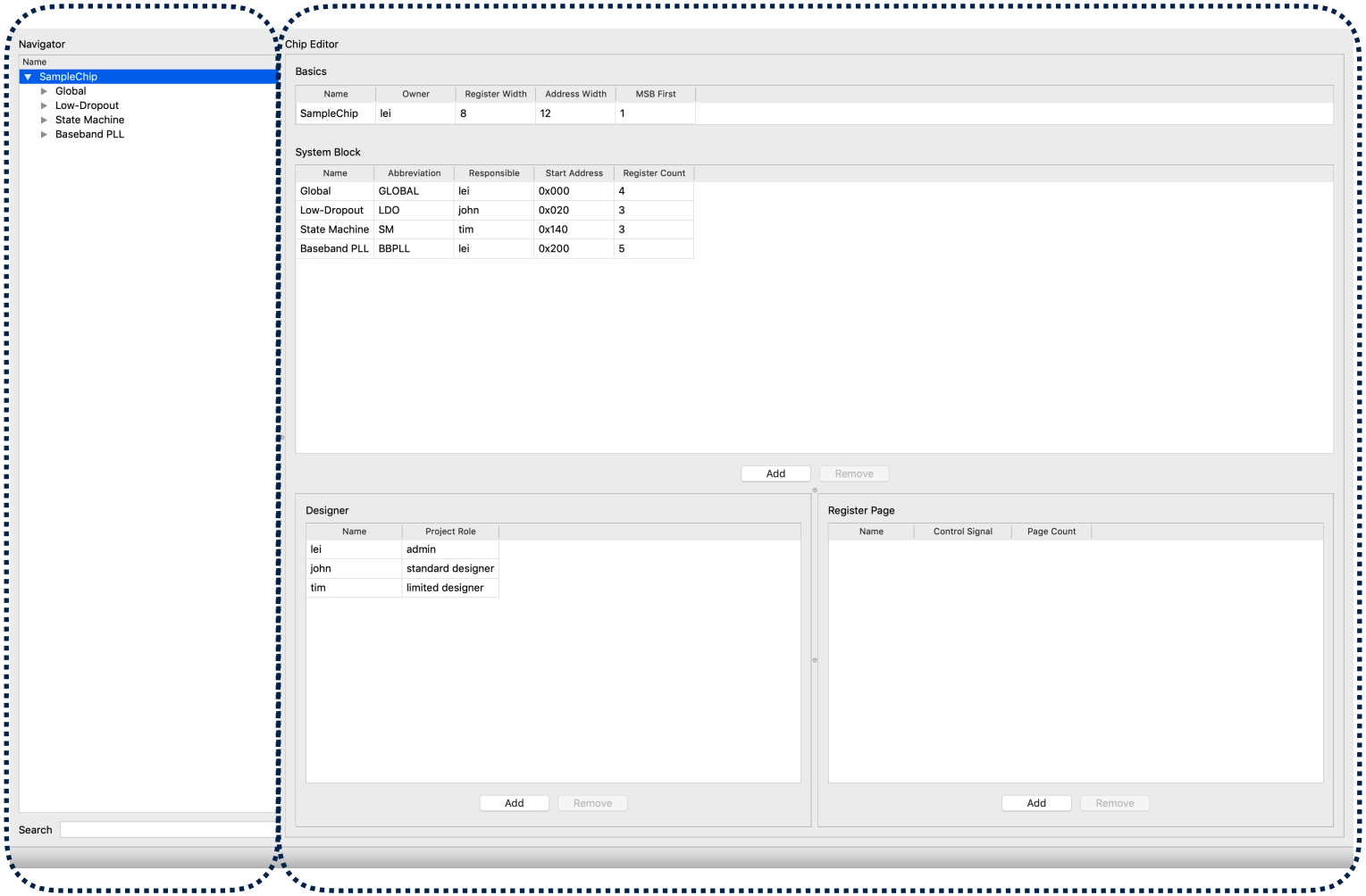
Designed Architecture



Object-Oriented Programming in Practice



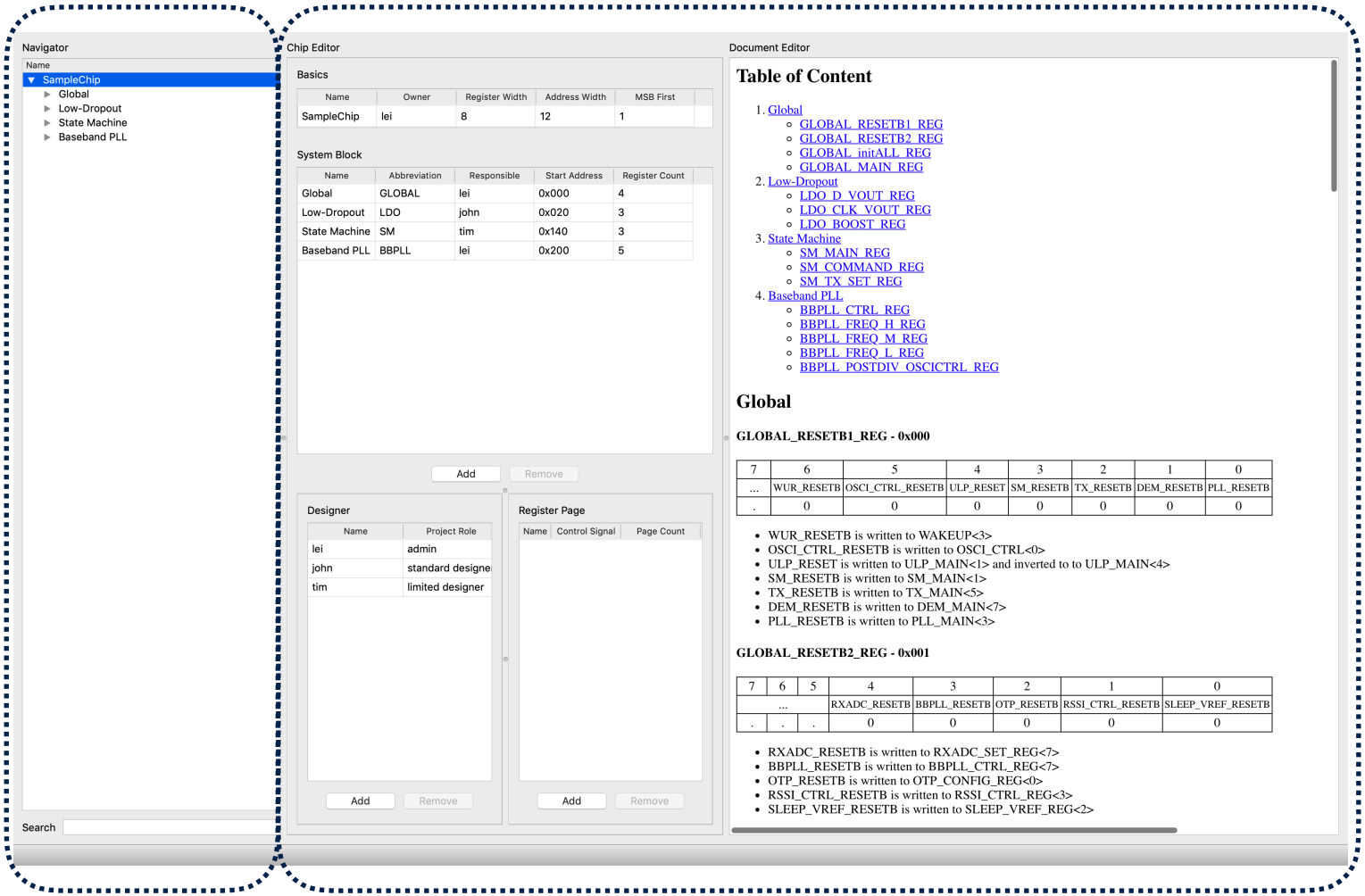
Main Window



Chip Navigator

Work Area

Main Window



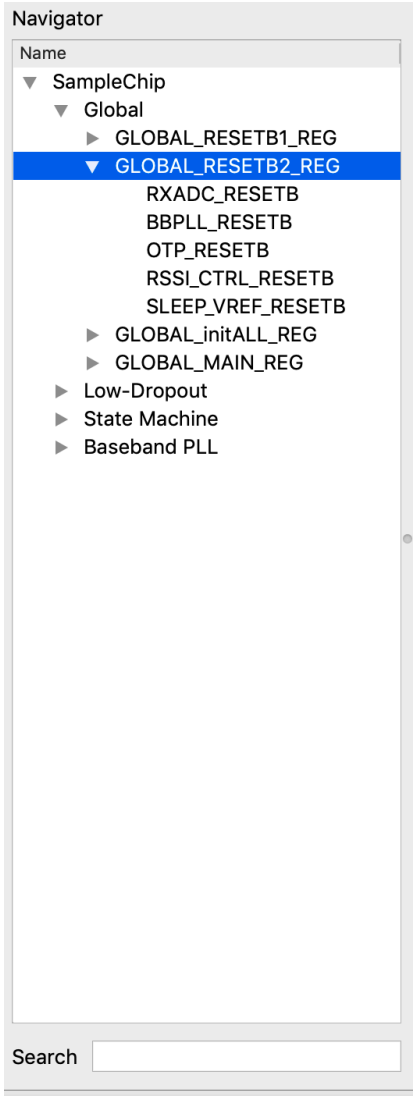
Chip Navigator

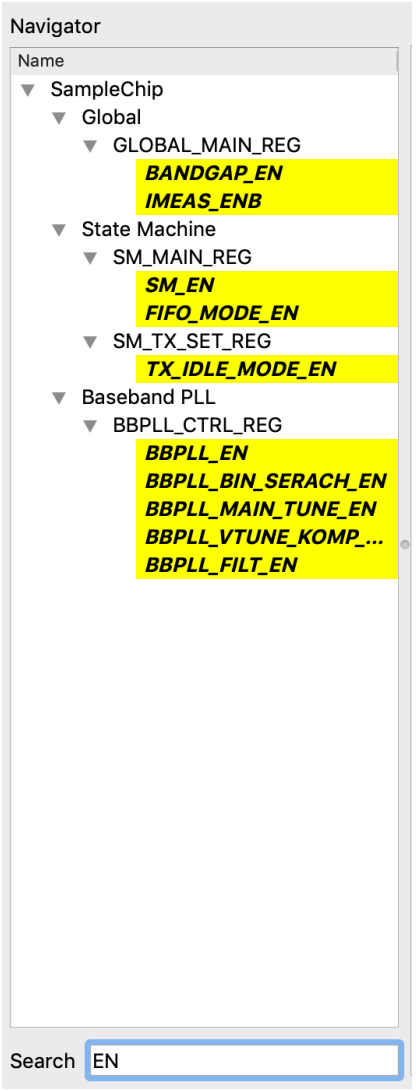
Work Area

Chip Navigator

4-level tree widget
chip, block, register, signal

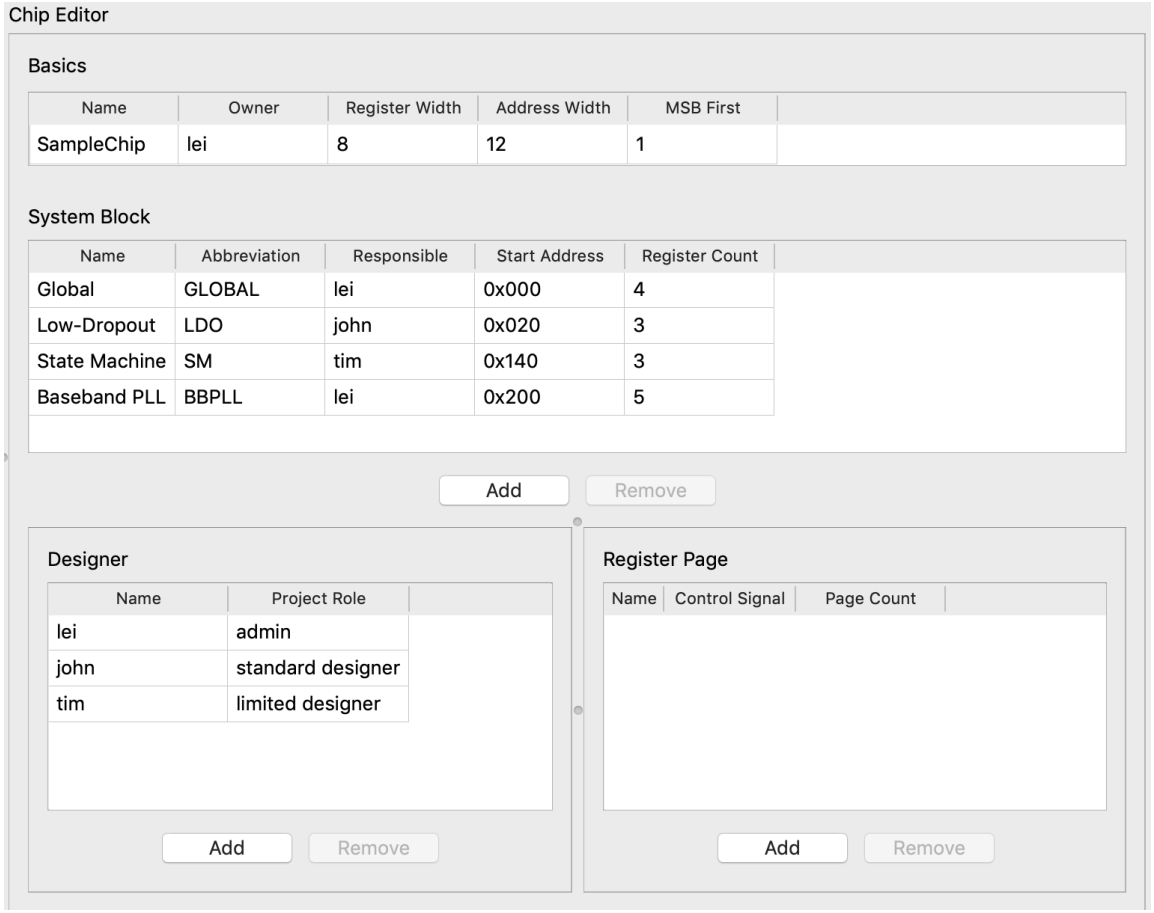
Search area





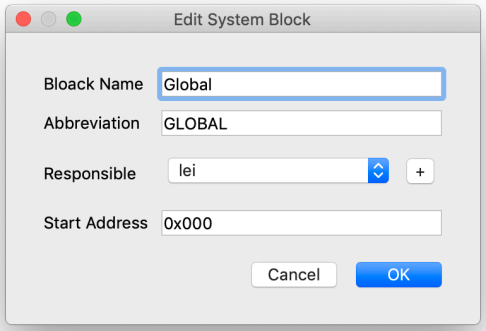
Chip Editor

- Chip-level view



Basic Information about the chip

List of system blocks

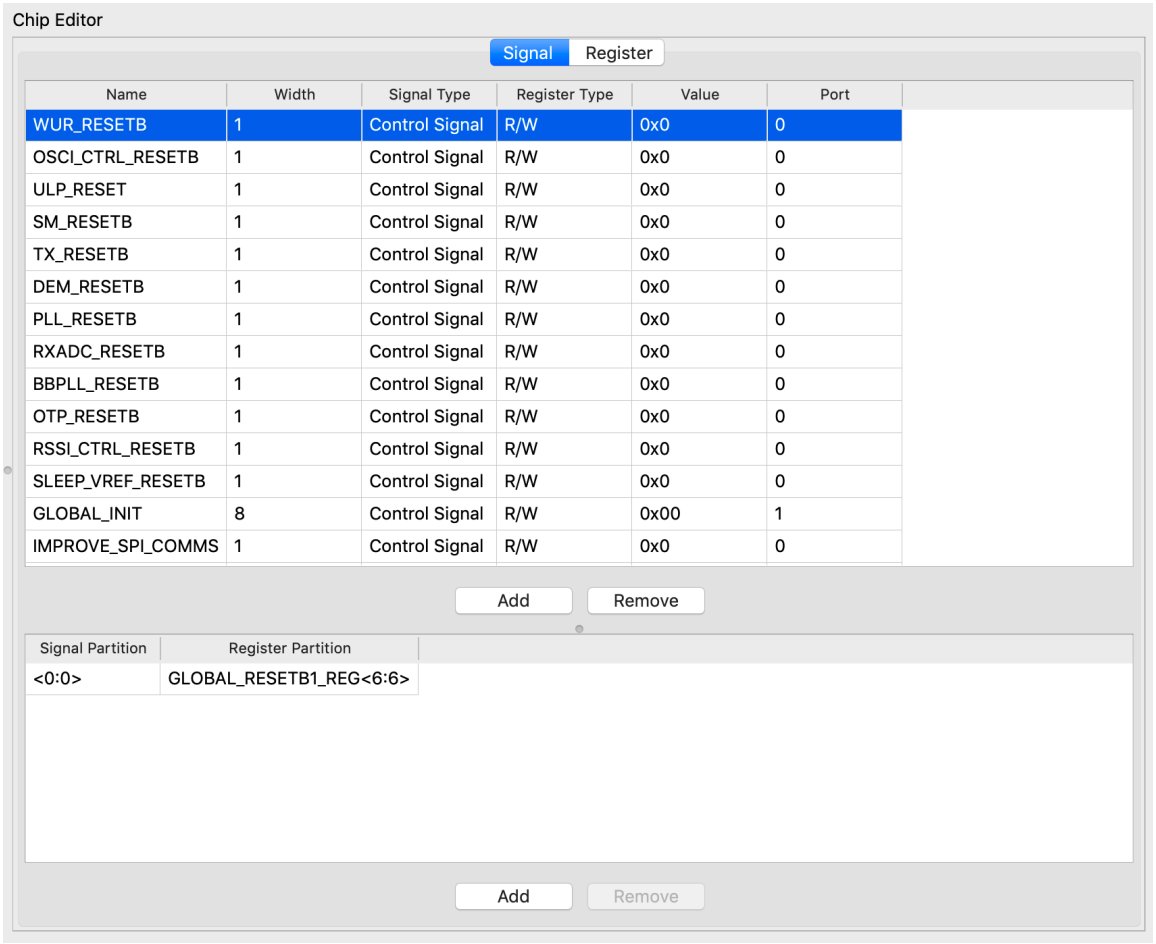


Designers

List of register pages

Chip Editor

- Block-level View - Signals

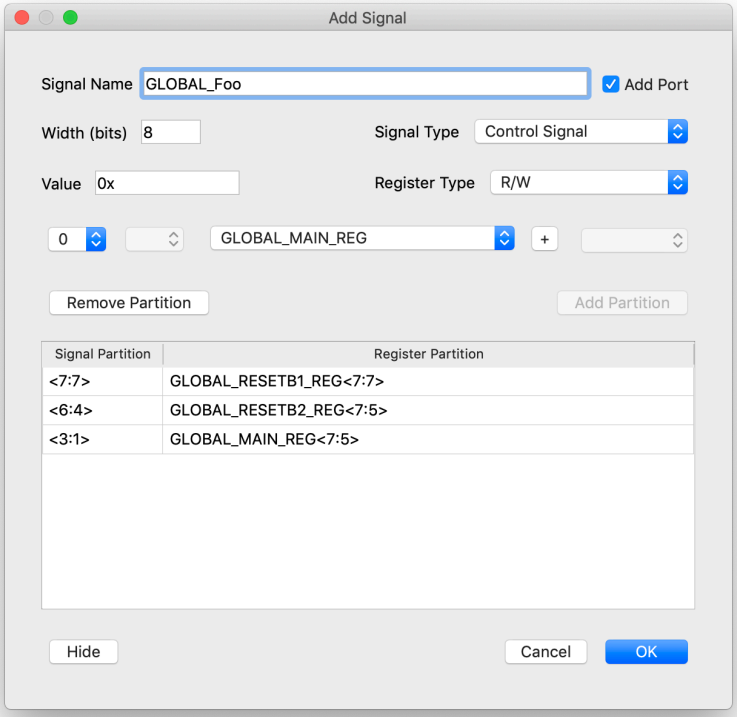


All signals in current block

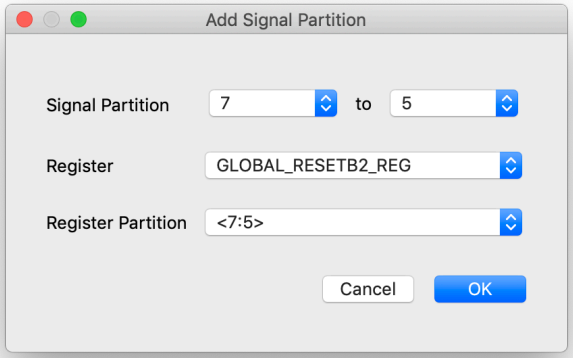
Signal-Register mappings

Chip Editor

- Add/Edit signals



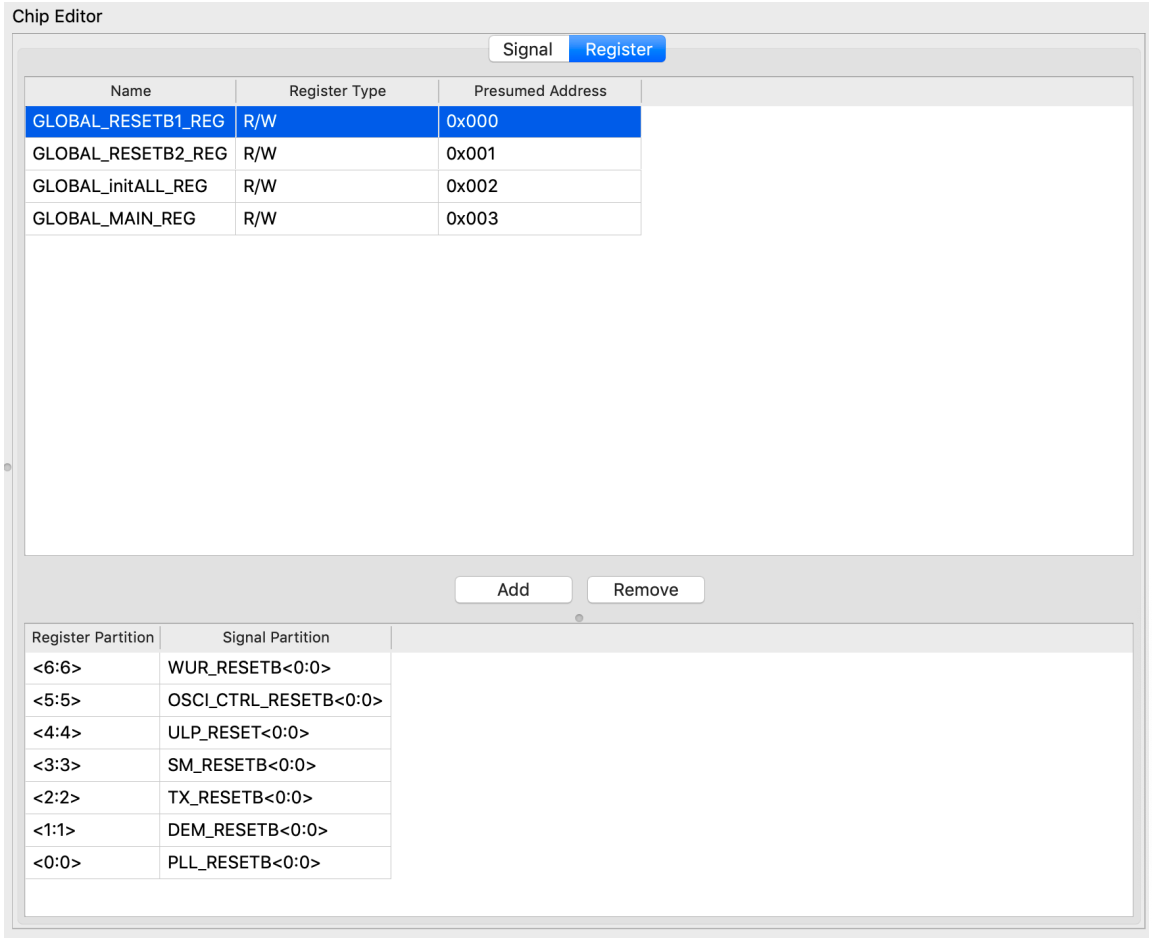
Add/Edit Multi-bit Signal dialog



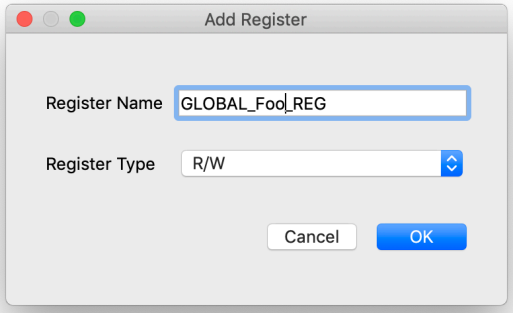
Add Signal-Register Mapping dialog

Chip Editor

- Block-level View - Registers



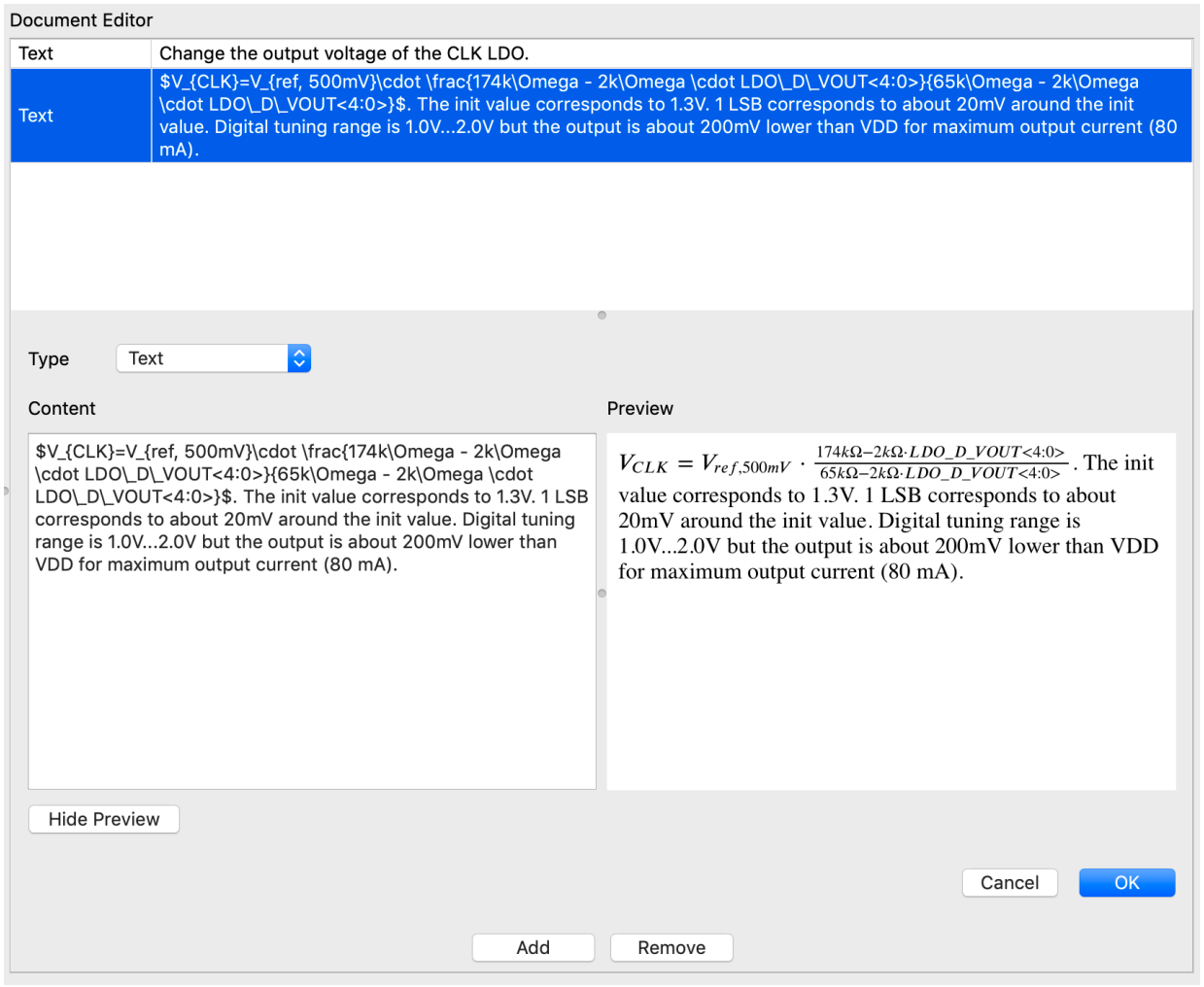
All registers in current block



Add Register dialog

Register-Signal mappings

Document Editor

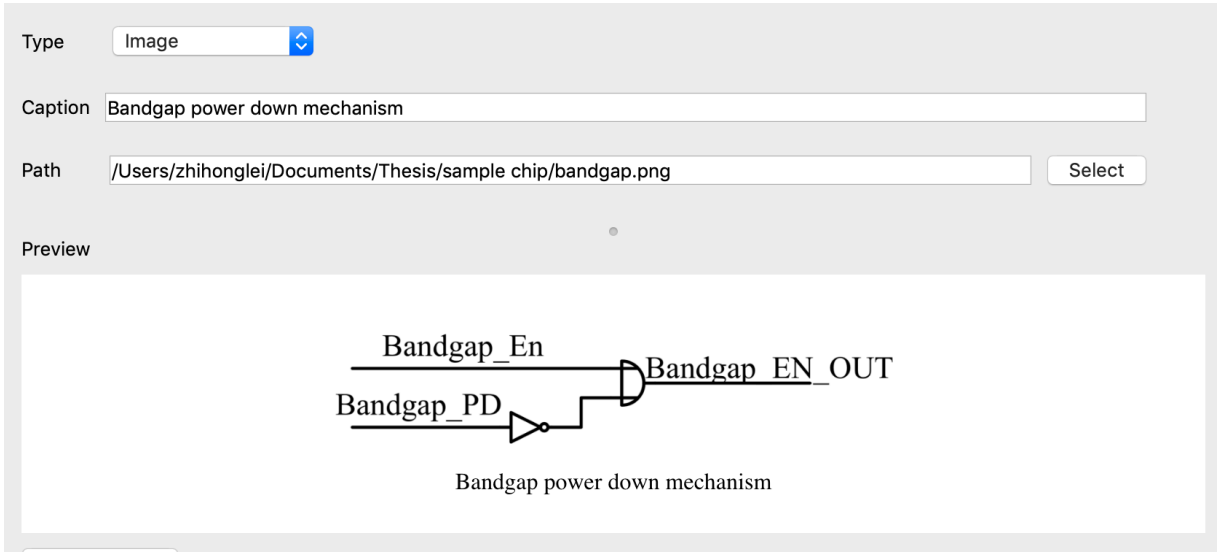


List of documents of currently selected block/register/signal

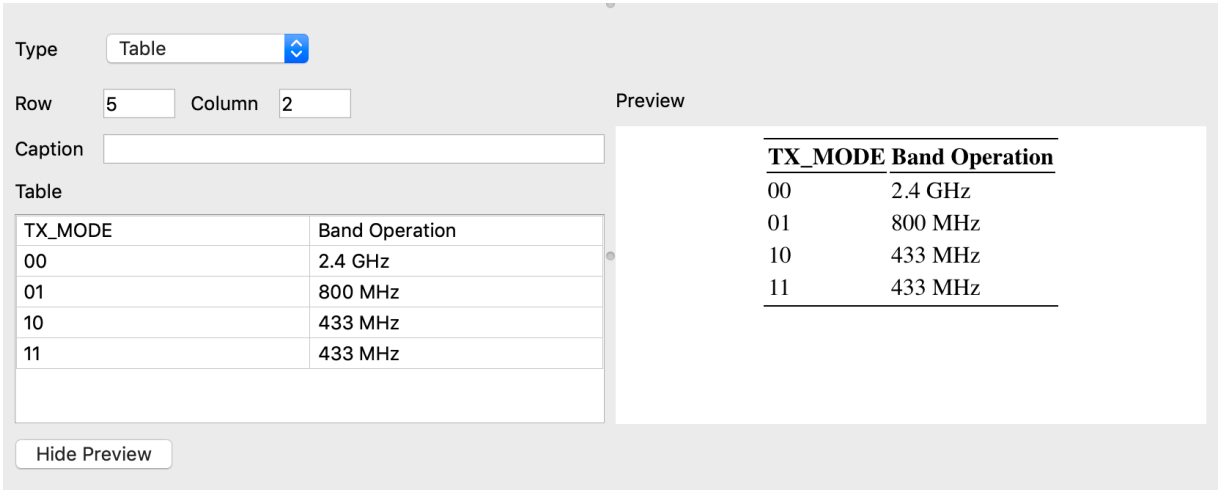
Document editing area

Preview: HTML web viewer supporting LaTeX

Document Editor



Image



Table

Document Overview

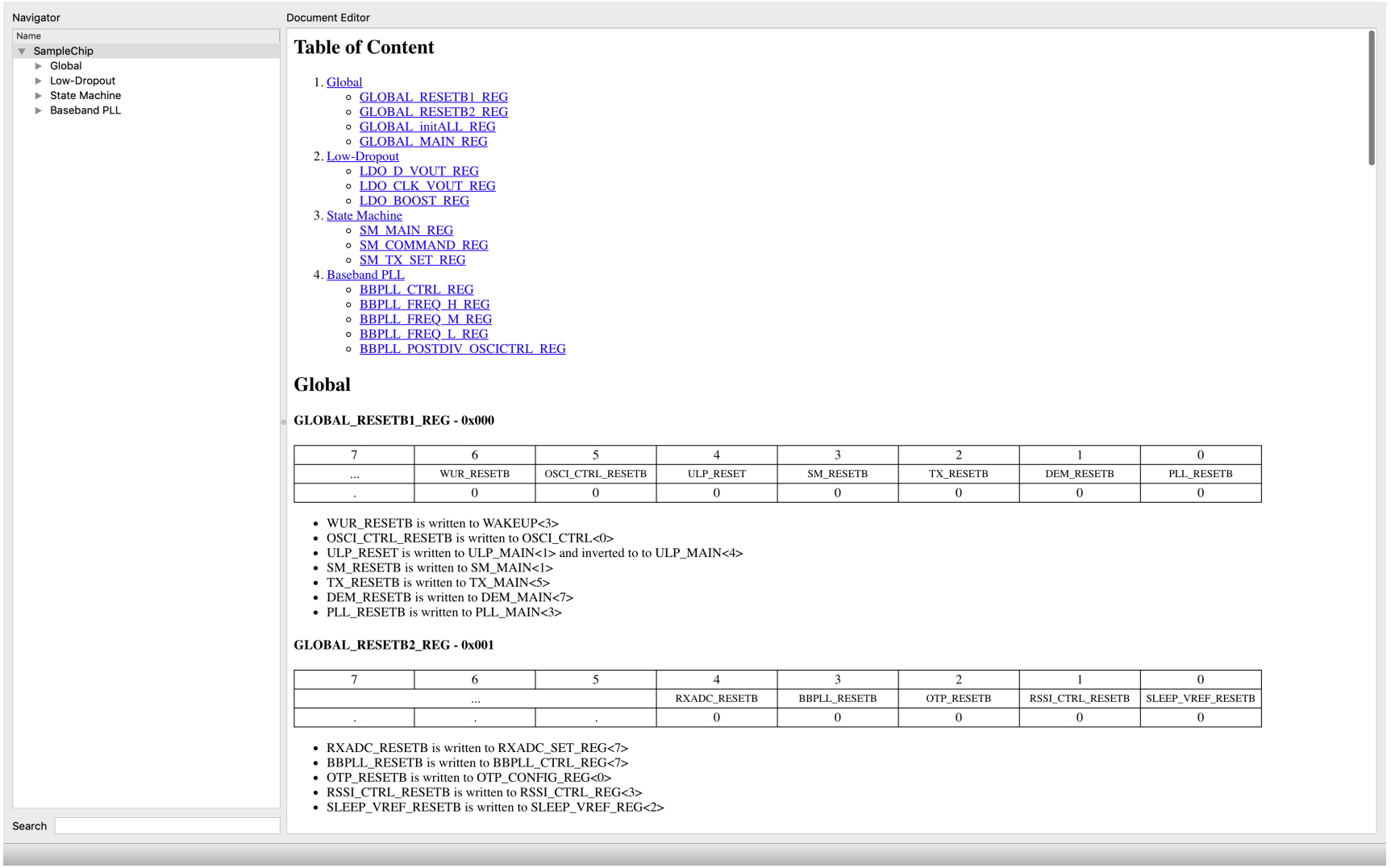


Table of Content

Global

GLOBAL_RESETB1_REG - 0x000

7	6	5	4	3	2	1	0
...	WUR_RESETB	OSCI_CTRL_RESETB	ULP_RESET	SM_RESETB	TX_RESETB	DEM_RESETB	PLL_RESETB
.	0	0	0	0	0	0	0

- WUR_RESETB is written to WAKEUP<3>
- OSCI_CTRL_RESETB is written to OSCI_CTRL<0>
- ULP_RESET is written to ULP_MAIN<1> and inverted to to ULP_MAIN<4>
- SM_RESETB is written to SM_MAIN<1>
- TX_RESETB is written to TX_MAIN<5>
- DEM_RESETB is written to DEM_MAIN<7>
- PLL_RESETB is written to PLL_MAIN<3>

GLOBAL_RESETB2_REG - 0x001

7	6	5	4	3	2	1	0
...			RXADC_RESETB	BBPLL_RESETB	OTP_RESETB	RSSI_CTRL_RESETB	SLEEP_VREF_RESETB
.	.	.	0	0	0	0	0

- RXADC_RESETB is written to RXADC_SET_REG<7>
- BBPLL_RESETB is written to BBPLL_CTRL_REG<7>
- OTP_RESETB is written to OTP_CONFIG_REG<0>
- RSSI_CTRL_RESETB is written to RSSI_CTRL_REG<3>
- SLEEP_VREF_RESETB is written to SLEEP_VREF_REG<2>

Live Demo …

Time Table

Timeline	Work
15.07	Implementation of export function of LaTeX document and VHDL source code
31.07	Implementation of database exception handling; refining the software
31.08	Deployment; trial run; thesis writing
30.09	Finalization

Thank you