**CIS5642 - Computer Architecture**

**Implementing a 3-Level Cache Using Simplescalar**

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**I. Cache Configuration & Basic Design**

Cache configuration 1: single core processor

L1 D-cache: 16KB, L1 I- Cache: 16KB, 2-way, block size: 64B

L2 cache: 512KB, 4-way, block size: 64B

L3 cache: 8MB, 8-way, block size: 64B

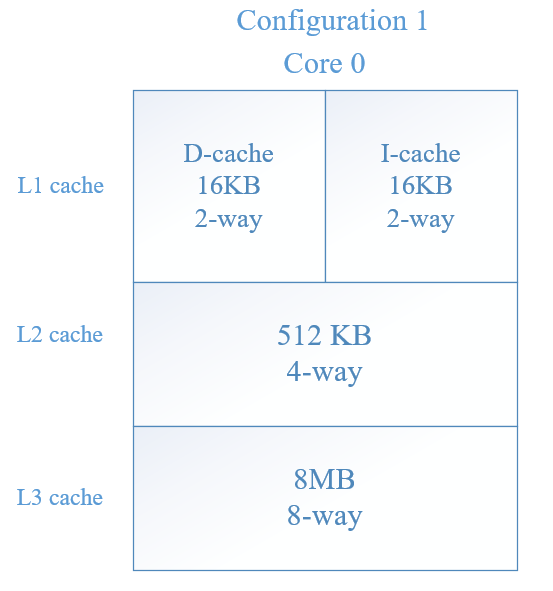


Figure 1: Configuration 1’s 3-level cache structure

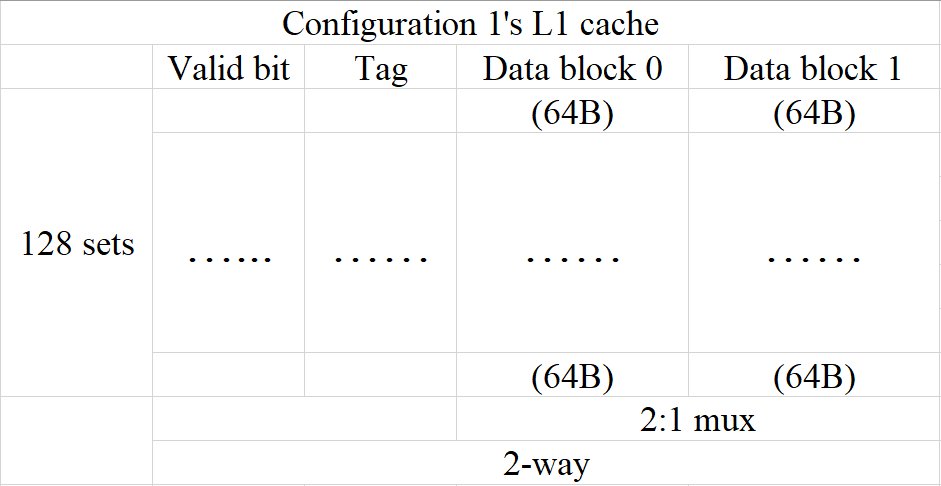


Figure 2: Configuration 1’s L1 cache design

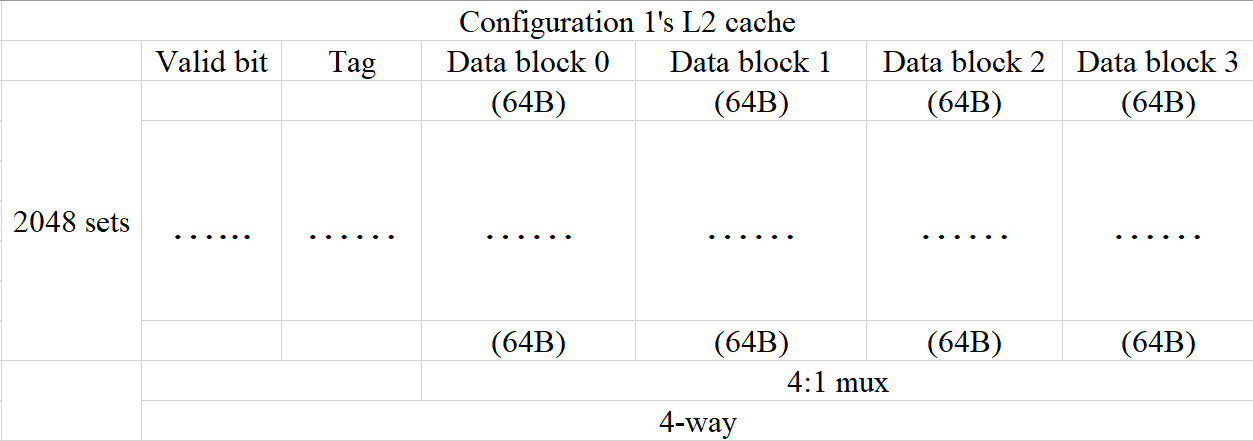


Figure 3: Configuration 1’s L2 cache design

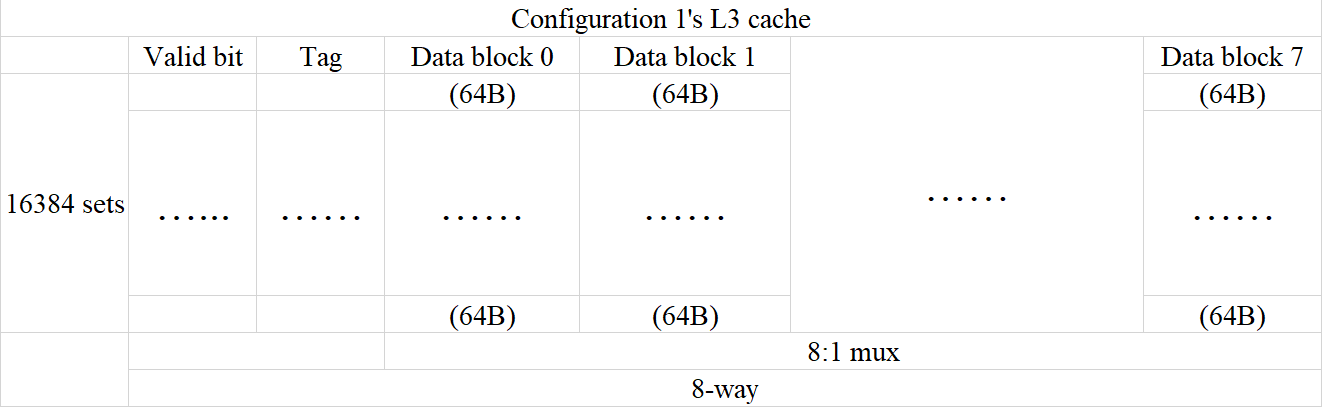


Figure 4: Configuration 1’s L3 cache design

Configuration 2: Dual core processor, each core has its own L1 and L2 cache and two cores share the L3 cache.

L1 D-cache: 8KB, L1 I- Cache: 8KB, direct mapped, block size: 64B

L2 cache: 128KB, 2-way, block size: 64B,

L3 cache: 16MB, 4-way, block size: 256B

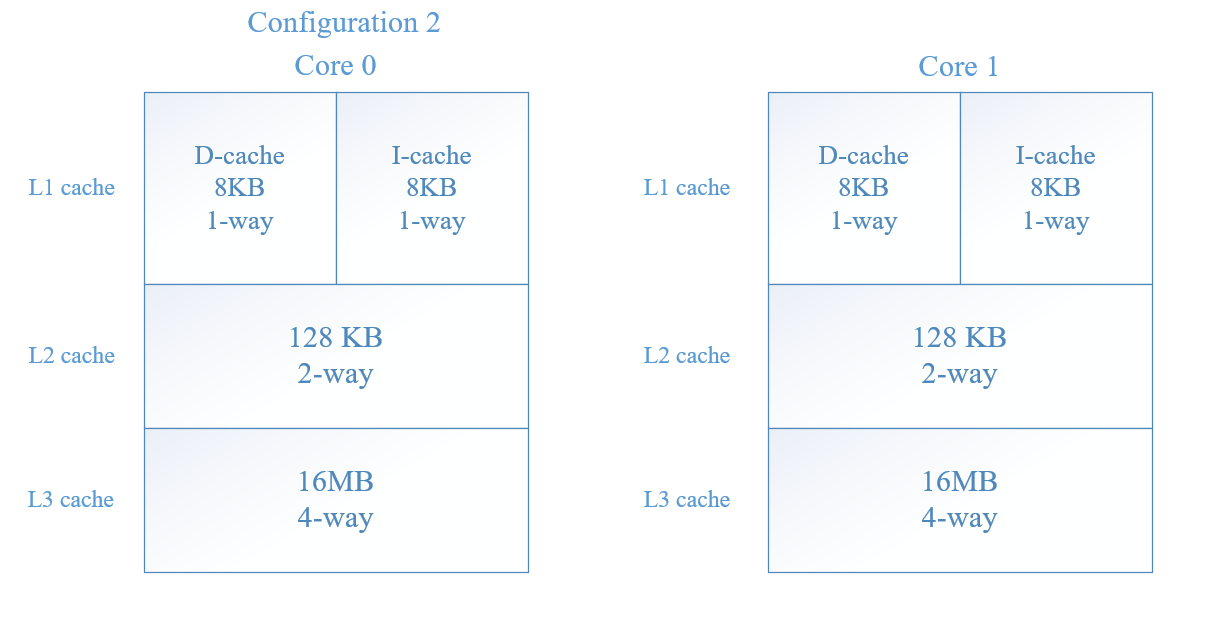


Figure 5: Configuration 2 cache structure

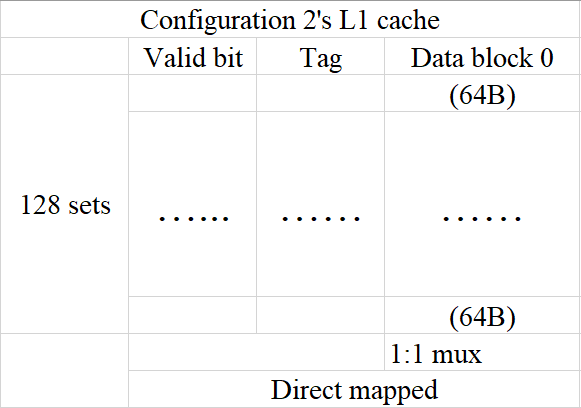


Figure 6: Configuration 2’s L1 cache design

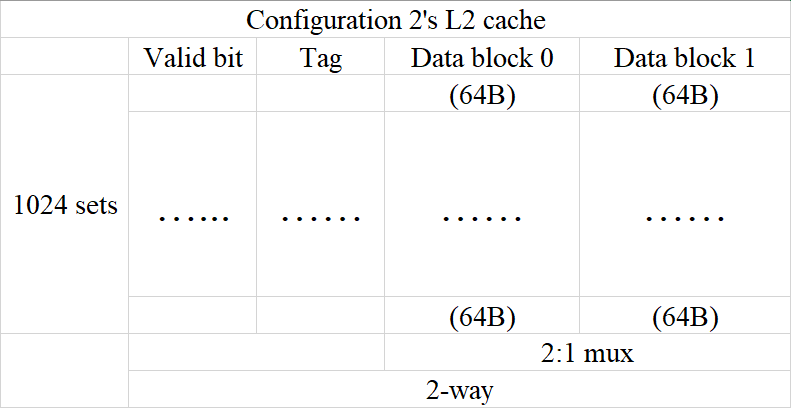


Figure 7: Configuration 2’s L2 cache design

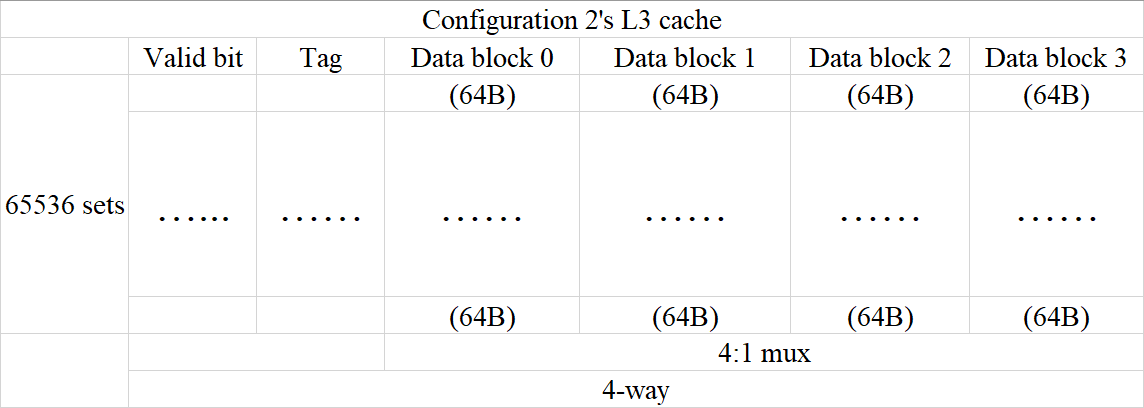


Figure 8: Configuration 2’s L3 cache design

**II. SimpleScalar**

**III. Testing Plan**

**IV. Each Member’s Responsibility**