**CIS5642 - Computer Architecture**

**Design Project Guidelines: Implementing a 3-Level Cache Using Simplescalar**

**Summary**

The goal of the class projects is to give students experience in computer architecture, and specifically, to familiarize students with the design and implementation of a 3-level cache.

**Project Descriptions**

In this project, you will implement a 3-level cache (L1, L2, L3) using simplescalar (or other similar tool approved by the instructor). L1 cache consists of separate I and D caches, both L2 and L3 are unified caches. They demonstrate inclusion property, i.e, all data in the L1 D-cache are present in L2, and all data in L2 are present in L3 cache.

Your tasks include:

1) Get familiar with Simplescalar. The simulator and its related documents can be downloaded at <http://www.simplescalar.com/>.

2) Modify the Simplescalar to support inclusion property and 3-level cache.

3) Modify the Simplescalar to support multicore.

4) Perform experiments to evaluate the cache design. You need use at least 2 benchmarks to collect the cache hit/miss information for the following configurations:

Configuration 1: single core processor

L1 D-cache: 16KB, L1 I- Cache: 16KB, 2-way, block size: 64B

L2 cache: 512KB, 4-way, block size: 64B

L3 cache: 8MB, 8-way, block size: 64B

Configuration 2: Dual core processor, each core has its own L1 and L2 cache and two cores share the L3 cache.

L1 D-cache: 8KB, L1 I- Cache: 8KB, direct mapped, block size: 64B

L2 cache: 128KB, 2-way, block size: 64B,

L3 cache: 16MB, 4-way, block size: 256B

**Schedule**

* 11/26: System Design Report Due
* 12/10: Project Demo/Presentation
* 12/14: Final report due.

**Requirements and Constraints**

* Work in groups of up to 2 students each
* Students select your group members
* Each member must design part of the project and must write his/her **OWN** part of the final report.
* Essential to help each other **WITHIN** teams!

**Phase 1 - System Design Report**

* This document reports the basic design including the design of each cache level, the design of the cache replacement algorithm (LRU or LFU), your understanding on SimpleScalar, and your plan to do the testing, etc. You should also indicate the responsibility of each team member in this report. It counts for 20% of your project grade.

**Phase 2 - Presentation and Demo**

* Each team will give a short presentation (approximately 15 minutes) about your project. Each member will orally talk about your design part.
* Demonstrate the simulation and testing results to the class.

**Phase 3 - Final Report**

* A final report contains two parts. The first part is a team-based report that includes the title of your project, a list of project team members and description of each member's contribution, a detailed description of your design, a discussion of how you test your design, and a discussion of what does not work correctly in your final design. You should also turn in the source code for your design and any relevant test benches in electronic format.
* The second part of the final report is an individual report. Each member will write a short individual report to state:

                1) What's your contribution on the team project?  
                2) What have you learned from this project?  
                3) Evaluate your team member's work.  
                4) Any comments on this project.

**Grade**

* Projects will be graded on how well the design works, the complexity of the design, optimizations made to the design, the thoroughness of the testing methodology, and the overall quality of the reports, presentation and demo.
  + Grade = System Design Report (20%) +Project functionality (25%) + Presentation (15%)+Final Report (40%)
  + Deduct 5 points per day late on each phase