HW5

Zhijiia Chen

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3.1 The base performance is $11 + 3 + 4 + 10 + 3 + 2 + 2 + 1 + 1 = 37$ cycles per loop iteration.

3.14 a. As shown in the following table, unscheduled instruction takes 19 clock cycles per loop iteration, while scheduled instruction takes 13 clock cycles. So the scheduled instruction is 31.58% faster, and the clock should be 31.58% faster for the unscheduled instruction to match the performance of scheduled instruction.

clock cycle	scheduled instruction	unscheduled instruction
1	addi x4,x1,#800	addi x4,x1,#800
2	fld F2,0(x1)	fld F2,0(x1)
3	stall	fld F6,0(x2)
4	fmul.d F4,F2,F0	fmul.d F4,F2,F0
5	fld F2,0(x1)	addi x1,x1,#8
6	stall	addi x2,x2,#8
7	stall	sltu x3,x1,x4
8	stall	stall
9	stall	stall
10	fadd.d F6,F4,F6	fadd.d F6,F4,F6
11	stall	bnez x3,foo
12	stall	stall
13	stall	stall
14	fsd F6,0(X2)	fsd F6,-8(X2)
15	addi x1,x1,#8	fld F2,0(x1)
16	addi x2,x2,#8	fld F6,0(x2)
17	sltu x3,x1,x4	fmul.d F4,F2,F0
18	stall x3,x1,x4	addi x1,x1,#8
19	bnez x3,foo	sltu x3,x1,x4
20	stall	stall
21	fld F2,0(x1)	stall
22	stall	fadd.d F6,F4,F6
23	fmul.d F4,F2,F0	bnez x3,foo
24	...	...

3.14 b. As shown in the following table, the loops need to be unrolled three times. The three loops take 19 clock cycles, so each iteration now takes 6.33 cycles.

clock cycle	scheduled instruction
1	add x4,x1,#800
2	fld F2,0(x1)
3	fld F6,0(x2)
4	fmul.d F4,F2,F0
5	fld F2,8(x1)
6	fld F8,8(x2)
7	fmul.d F10,F2,F0
8	fld F2,16(x1)
9	fld F12,16(x2)
10	fmul.d F14,F2,F0
11	fadd.d F6,F4,F6
12	addi x1,x1,#24
13	fadd.d F8,F10,F8
14	addi x2,x2,#24
15	sltu x3,x1,x4
16	fadd.d F12,F14,F12
17	fsd F6,-24(X2)
18	fsd F8,-16(X2)
19	bnez x3,foo
20	fsd F12,-8(X2)
21	...

3.15 a See the following table.

Iteration	Instruction	Issues	Executes	Memory access	Write CDB	Comment
1	fld F2,0(x1)	1	2	2	3	
1	fmul.d F4,F2,F0	2	4		19	wait for F2
1	fld F2,0(x1)	3	4	4	5	
1	fadd.d F6,F4,F6	4	20		30	wait for F4
1	fsd F6,0(X2)	5	31	31		wait for F6
1	addi x1,x1,#8	6	7		8	
1	addi x2,x2,#8	7	8		9	
1	sltu x3,x1,x4	8	9		10	
1	bnez x3,foo	9	11			wait for x3
2	fld F2,0(x1)	10	12	12	13	wait for bnez
2	fmul.d F4,F2,F0	11	19		34	wait for F2 and FP multiplier
2	fld F2,0(x1)	12	13		14	
2	fadd.d F6,F4,F6	13	35		45	wait for F4
2	fsd F6,0(X2)	14	46	46		wait for F6
2	addi x1,x1,#8	15	16		17	
2	addi x2,x2,#8	16	17		18	
2	sltu x3,x1,x4	17	18		19	
2	bnez x3,foo	18	20			wait for x3
3	fld F2,0(x1)	19	21	21	22	wait for bnez
3	fmul.d F4,F2,F0	20	34		49	wait for F2 and FP multiplier
3	fld F2,0(x1)	21	22	22	23	
3	fadd.d F6,F4,F6	22	50		60	wait for F4
3	fsd F6,0(X2)	23	61	61		wait for F6
3	addi x1,x1,#8	24	25		26	
3	addi x2,x2,#8	25	26		27	
3	sltu x3,x1,x4	26	27		28	
3	bnez x3,foo	27	29			wait for x3

3.17 For the correlating predictor, as shown in the following table, there are 3 misprediction, so the misprediction rate is 33.33%.

Branch PC mod 4	Entry	Prediction	Outcome	Update
2	4	T	T	None
3	6	NT	NT	change prediction to "NT"
1	2	NT	NT	None
3	7	NT	NT	None
1	3	T	NT	change prediction to "T with one misprediction"
2	4	T	T	None
1	3	T	NT	change prediction to "NT"
2	4	T	T	None
3	7	NT	T	change prediction to "NT with one misprediction"

For the local predictor, as shown in the following table, there are 4 misprediction, so the misprediction rate is 44.44%.

Branch PC mod 4	Entry	Prediction	Outcome	Update
0	0	T	T	change prediction to "T"
1	4	T	NT	change prediction to "T with one misprediction"
1	5	T	NT	change prediction to "NT"
1	7	NT	NT	None
1	7	NT	NT	None
0	0	T	T	None
1	7	NT	NT	None
0	0	T	T	None
1	7	NT	T	change prediction to "NT with one misprediction"