

ECE 385

Spring 2018
Experiment #1

Introductory Experiment

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ABM / Thursday (11:30 - 14:20)
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0.1 Introduction

This lab introduces us the basic equipment that we are going to use in this course. During this first lab, we are going to build a 2 to 1 multiplexer using all NAND gates. However, the minimized circuit represent may cause a static hazard (glitches). We will detect the glitches using function generator and oscilloscope. Then by adding a redundant part to the circuit, we eliminate the static hazard.

0.2 Pre-Lab

0.2.1 Description of operation of the circuits

Description of operation for Part A circuit

In part A, we are building a 2 to 1 MUX using the simplest form of representation. In this part, we used three SN7400 to accomplish this goal. The reason that we used 3 chips is that we built 7 inverters and connected them in series to mimic one inverter. This allow us to see the glitches on oscilloscope when later we test the circuit using function generator. The SN7400 chip includes four NAND gates, and each of them are used in this part. To use the chip, we need first power the chip by connecting pin 14 to Vcc and pin 7 to ground. Then we build our circuit using the chip. The k-map for this part is shown below. In this case, the output is given by $Y=ab+b'c$.

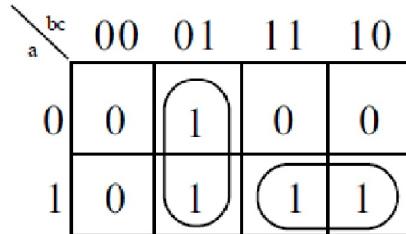


Figure 1: K-map (notice that there are only two circular loops)

Description of operation for part B circuit

In part B, we are building the same 2 to 1 mux, but with a redundant term ac . By adding this redundant term, we covered all adjacent min-terms in the K-map. Therefore, we eliminated the glitches. To accomplish this, we added one more 2-port NAND gate and a 3-port NAND gate (using SN7410) to the circuit in part A. The k-map for this part is shown below. In this case, the output is given by $Y=ab+b'c+ac$.

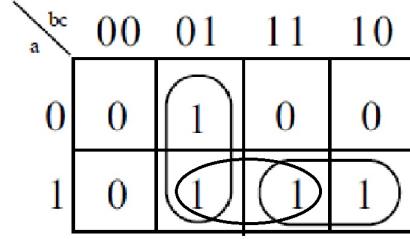


Figure 2: K-map (notice that there are only two circular loops)

0.2.2 Component Layout Sheet

Component Layout Sheet for Part A

The component layout sheet for part A is shown below. I have labeled the part numbers, all inputs, outputs and the intrinsic connections of my circuit in the sheet. Please zoom in to check the sheet!

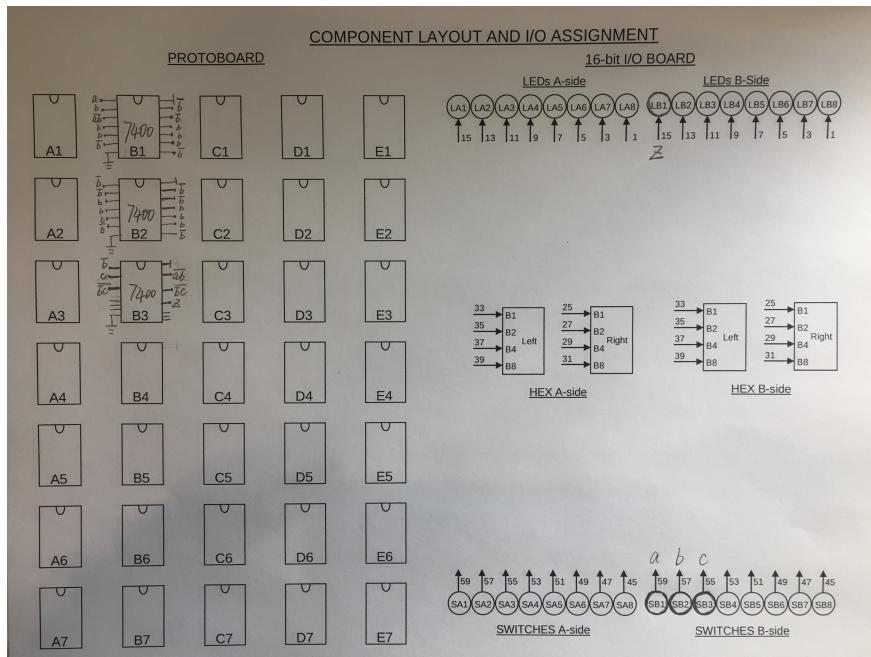


Figure 3: Component Layout Sheet for Part A

Component Layout Sheet for Part B

The component layout sheet for part B is shown below. I have labeled the part numbers, all inputs, outputs and the intrinsic connections of my circuit in the sheet. Please zoom in to check the sheet!

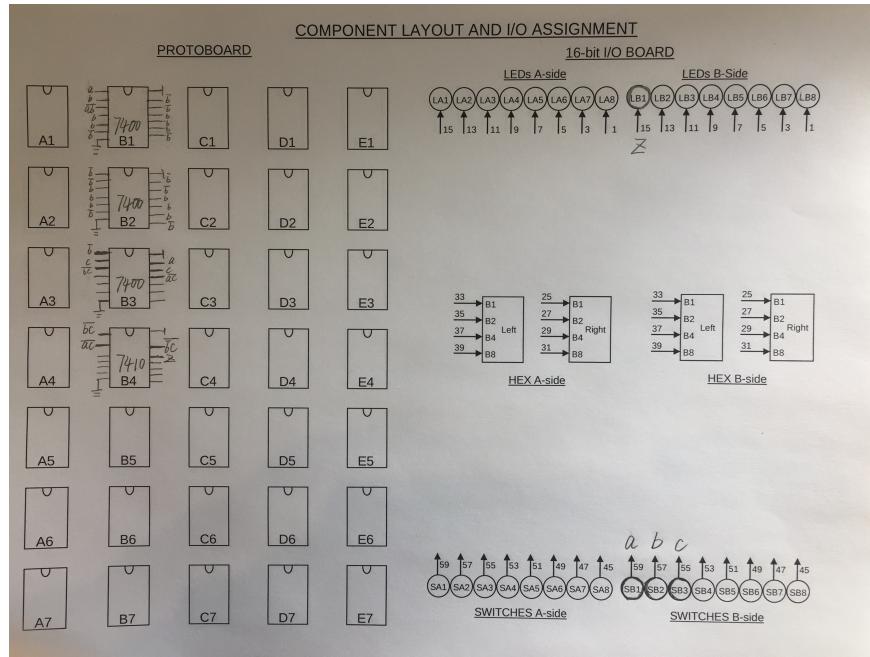


Figure 4: Component Layout Sheet for Part B

0.2.3 Circuit Diagrams

Circuit Diagrams for part A

In this part, seven inverters which are built from NAND gates are used to mimic one inverter. This is because any number of odd inverters in series is equivalent to one inverter. We connect 7 of them in series because we want the delay to show up more obviously. And the reason of using NAND gates as inverters is because they usually have longer delays than the actual inverters. The circuit diagram is shown below.

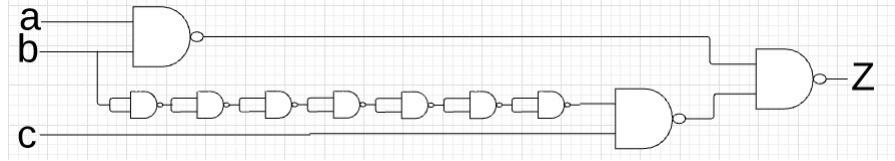


Figure 5: Circuit Diagram without redundant term

Circuit Diagrams for part B

In part B, we add ac , the redundant term and a 3-port NAND gate. This circuit should eliminate the glitches.

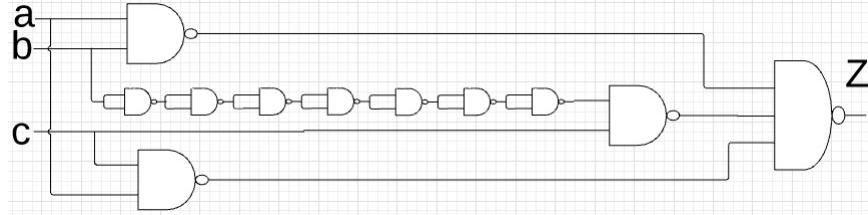


Figure 6: Truth Table

0.3 Lab

0.3.1 Part 1

Part 1 of the lab asks us to test all the chips in the lab kit. This is done by connecting LEDs on the output of gates in each chip. After testing, all chips function properly.

0.3.2 Part 2

In this part, we tested all possible input combinations using three switches representing a, b and c. The truth table is shown below. The circuit passes all the test cases.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 7: Truth Table

0.3.3 Part 3

In this part, we used function generator and oscilloscope to detect the glitches from the circuit. To do this, we set the function generator to 1 MHZ, 0 to 5 V square wave and 2.5 V offset. The function generator is also set to HIGH Z mode. The waveform for the input and output signals are shown below. Notice that there are glitches on the output signal. This is what we want to see. The glitches represents static hazard and can be eliminated in the next section when we add a redundant term ac.



Figure 8: Input signal of B

0.3.4 Part 4

In this part, we are testing how well the redundant circuit eliminate glitches. The truth table is the same as in part 2. It is shown below.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 9: Truth Table for redundant circuit

After we added the redundant term ac , the glitches are gone. However, there are still some noises, but those noises are allowed. The input and the output signals are shown below.



Figure 10: Input signal of B

When we make B connected to the function generator, we found that the glitches are gone. By comparing the timing of the glitches. They are more likely to occur at the falling edge of input B.

0.4 Post-Lab

0.4.1 Part 1

The timing table is shown below. The grey area represents uncertain signals.

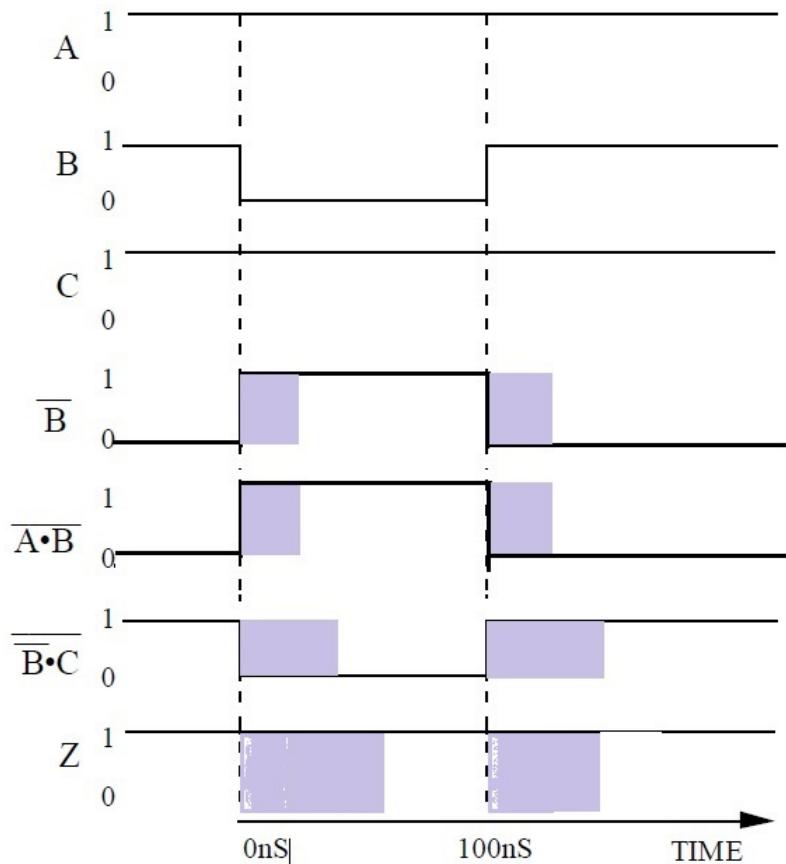


Figure 11: Timing Table

On the falling edge of B, the output Z takes 60ns to stabilize. On the Rising edge of B, the output Z takes 40ns to stabilize. There is potential glitches in the output Z. One possible glitch may occur between 0-60ns, and another possible glitch may occur between 100-140ns. Glitches occur when the output Z changes from HIGH to LOW due to the delay of the signals.

0.4.2 Part 2

The debouncer circuit is shown below. (1)When the SPDT switch is connected to A, it makes the input D to be 0. Therefore the output Q and input F become 1. This makes QN becomes 0. (2)When the SPDT switch is connected to B, it makes the input G becomes 1. Therefore, the output QN and the input E become 1. This makes Q becomes 0. This feature makes the circuit behave like a switch. With a single we get two outputs (0 and 1) simultaneously. Therefore, the glitches problem caused by inverter is solved because we can feed 0 and 1 to the circuit simultaneously now.

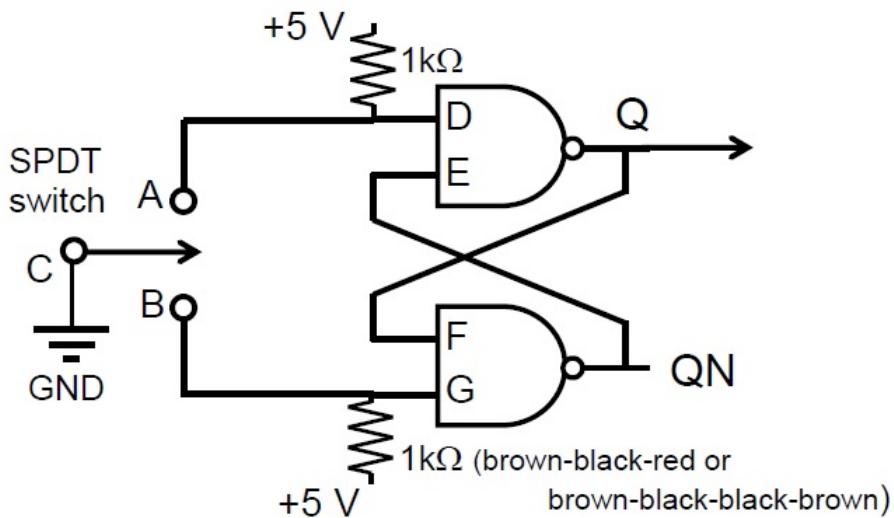


Figure 12: Timing Table

0.5 Conclusion

For this lab, we saw that delay and glitches are common hazard in logic circuit. We also explored that glitches are more likely to occur at the falling edge of the input signal (when input goes from HIGH to LOW). However, this static hazard can be eliminated. By covering all adjacent min-terms in the K-map which represents the circuits, we can eliminating the glitches. We also see that a better way of reducing glitches is by using a debouncer circuit.