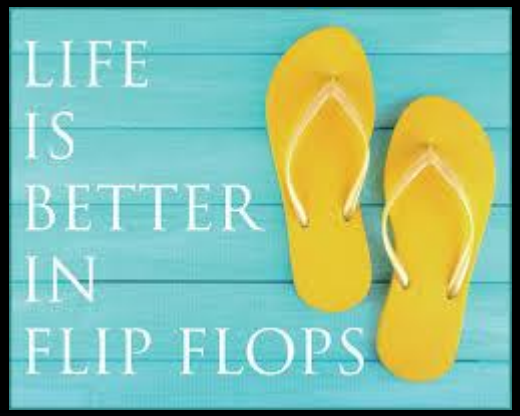
Week 4, Part E: Flip flops



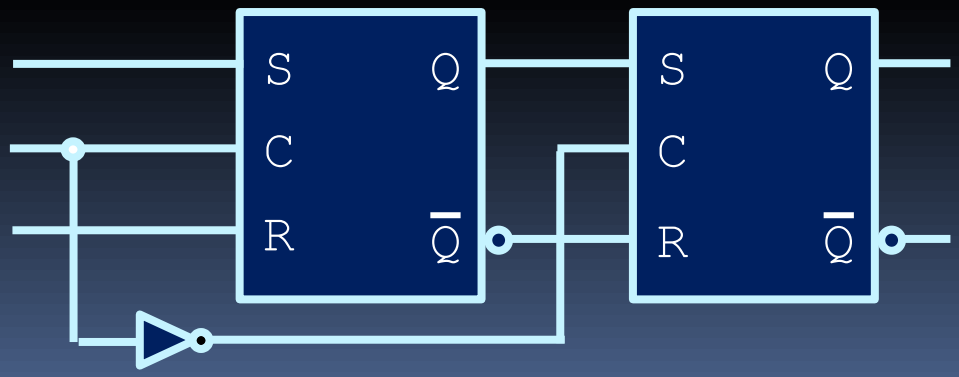
Reminder

- We are trying to a circuit that can store a bit.

- NAND / NOR feedback – oscillation.
- SR latches – no clock.
- Clocked SR latches – forbidden state.
- D latches – have clocks, no forbidden state.
  - But timing issues.

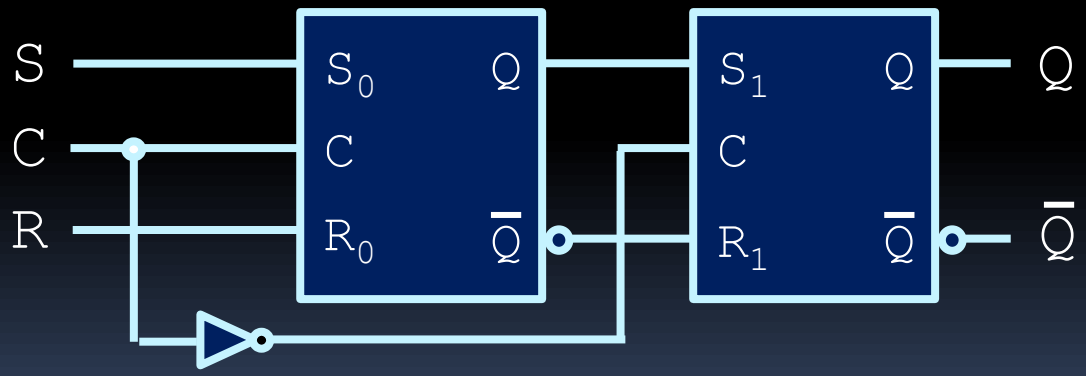
Fixing latch timing issues

- Preferable behaviour:
  - Have output change only once when the clock changes.
- Solution: create disconnect between circuit output and circuit input, to prevent unwanted feedback and changes to output.

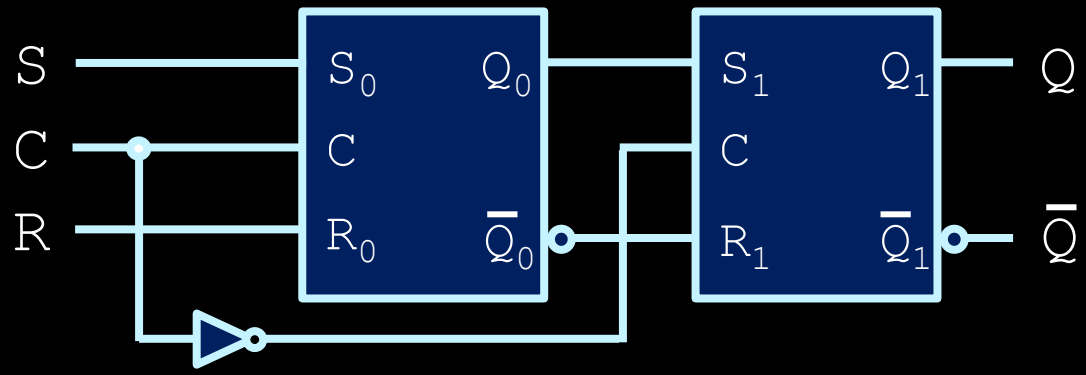


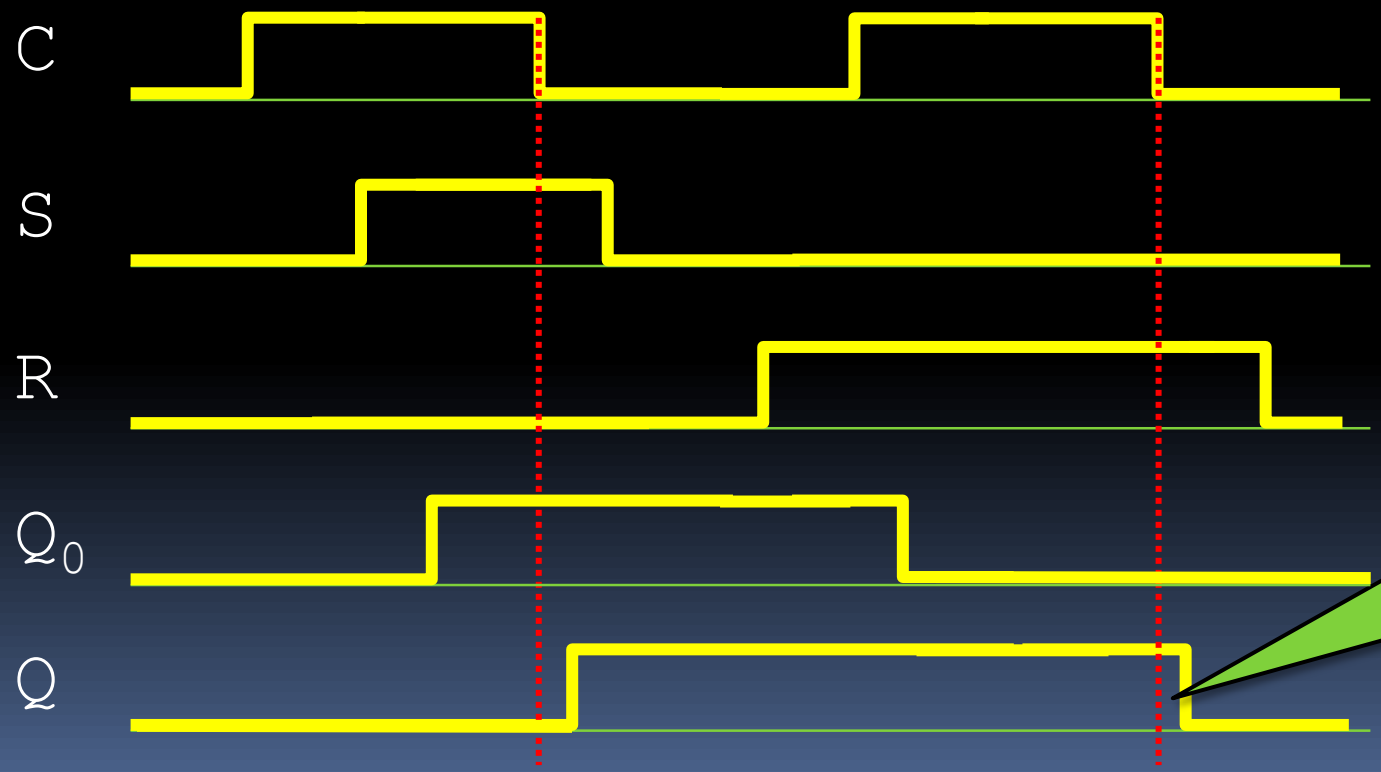
SR master-slave flip-flop

- A flip-flop is a latched circuit whose output is triggered with the rising edge or falling edge of a clock pulse.
- Example: the SR master-slave flip-flop



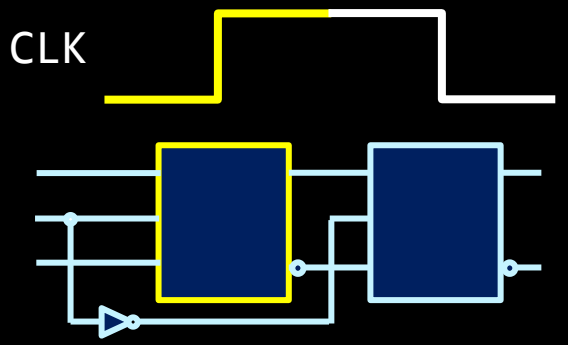
SR master-slave flip-flop

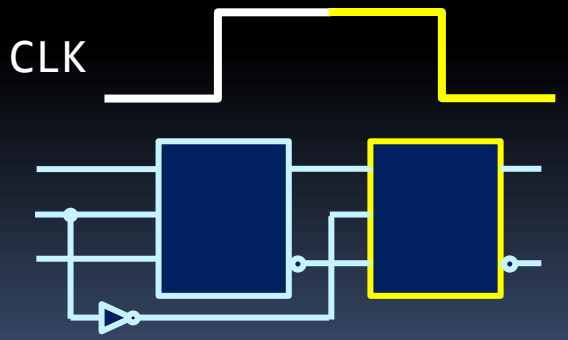




Flip flop Behaviour Sumary

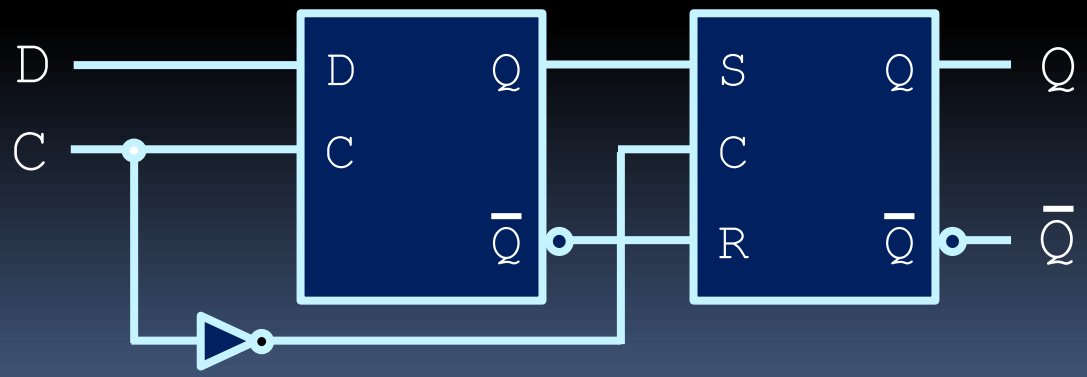
- For input to propagate to output, it takes each of the latches to be active once.
- First latch changes on "flip".
- Output can only change upon "flop", which is basically the falling edge of the clock signal
- At most one change per clock cycle





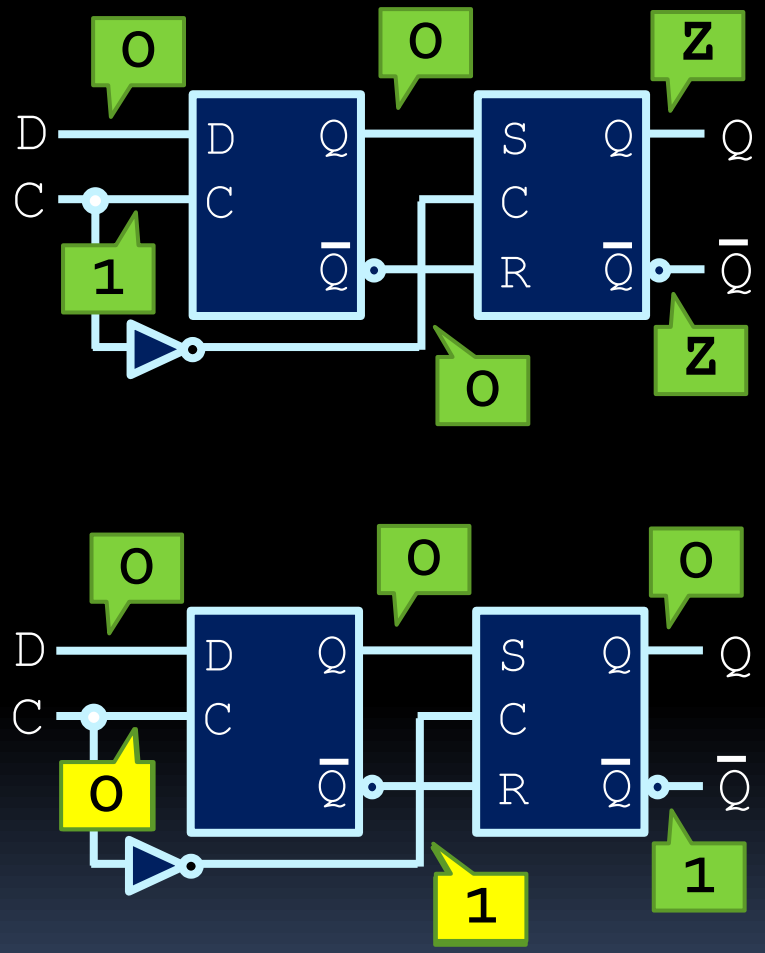
Edge-triggered D flip-flop

- SR flip-flops still have issues of unstable behaviour (race condition) when S=1 R=1
- Solution: D flip-flop
  - Connect D latch to the input of a SR latch.
  - Negative-edge triggered flip-flop (like the SR)



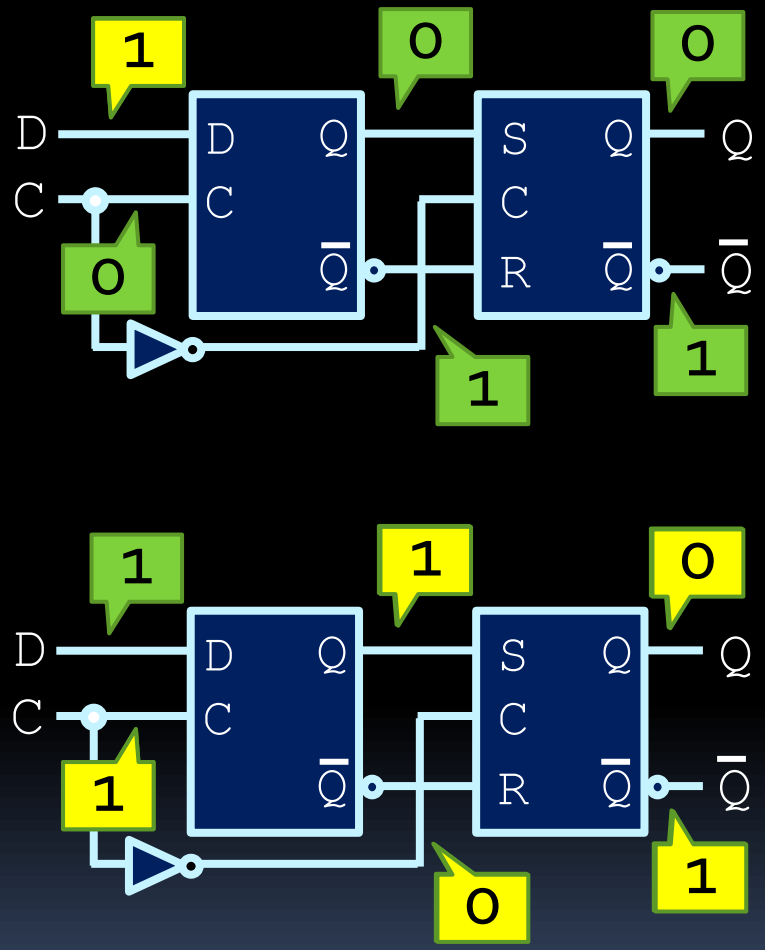
Flip-flop behaviour

- Observe the behaviour:
  - If the clock signal is high, the input to the first latch is sent out to the second.
  - The second latch doesn't do anything until the clock signal goes down again.
  - When it clock goes from high to low, the first latch stops transmitting a signal, and the second one starts.



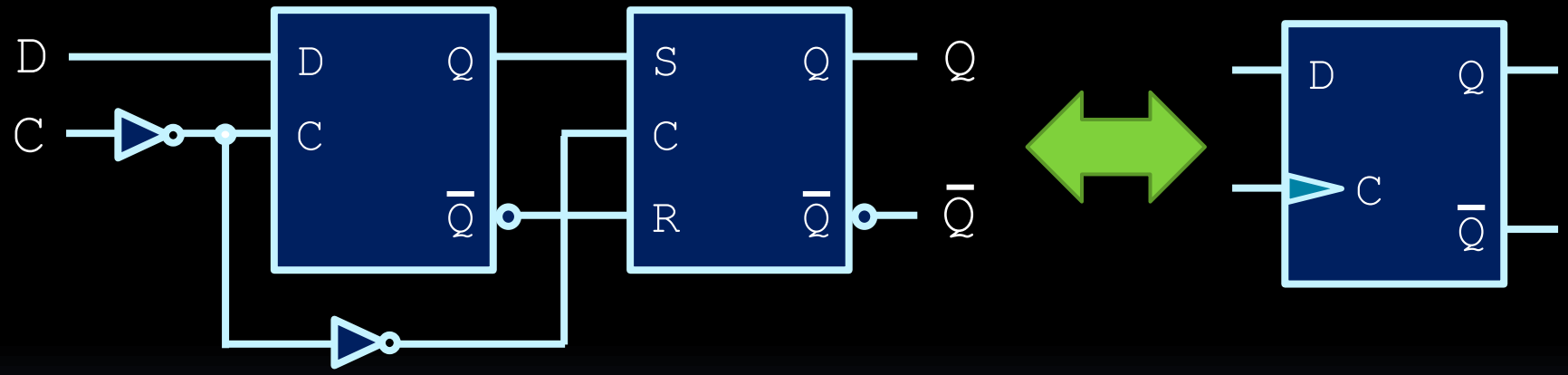
Flip-flop behaviour

- Continued from previous:
  - If the input to D changes, the change isn't transmitted to the second latch until the clock goes high again.
  - Once the clock goes high, the first latch starts transmitting at the same time as the second latch stops.



Edge-triggered flip-flop

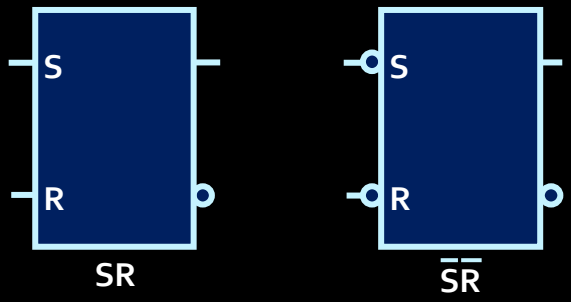
- Alternative: positive-edge triggered flip-flops



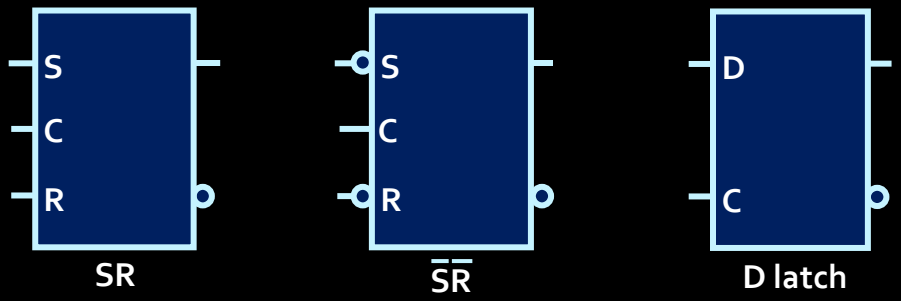
- These are the most commonly-used flip-flop circuits (and our choice for the course).
  - When we say just "flip-flop", we usually mean this.

Notation

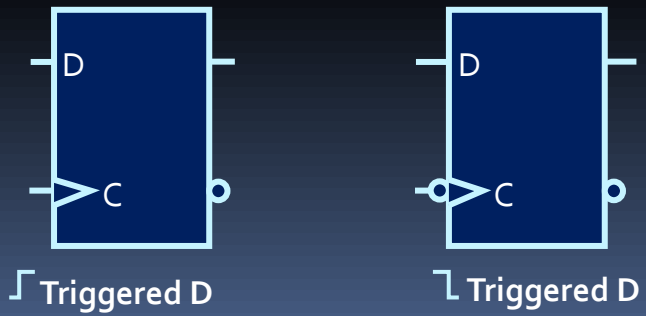
- Latches



- Clocked latches

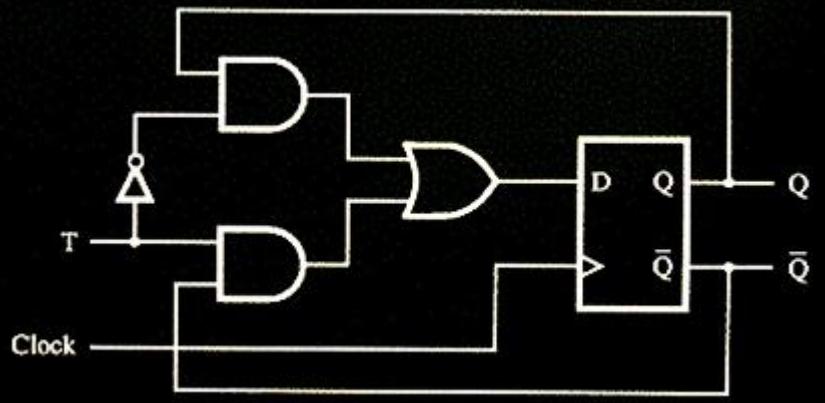


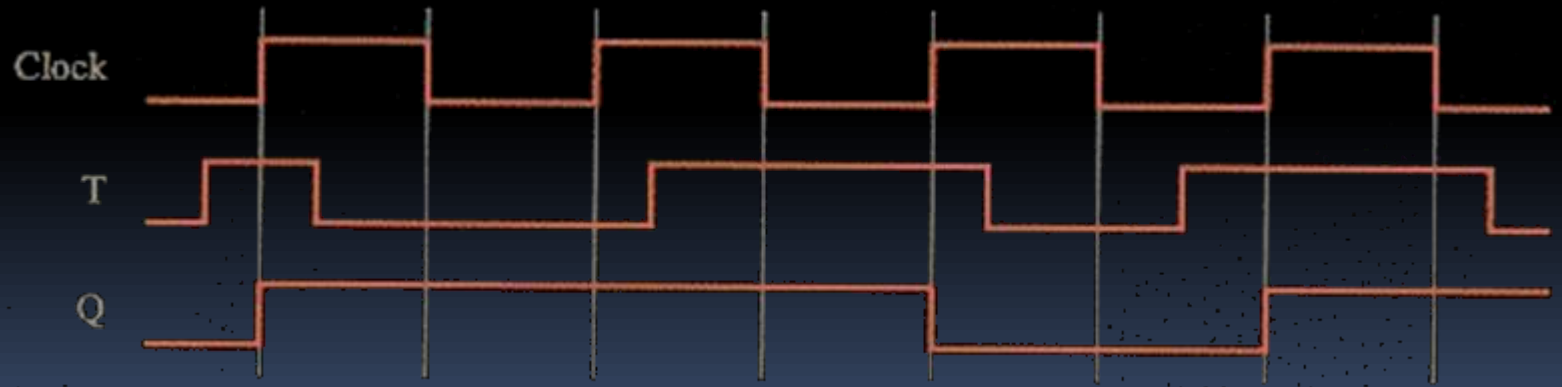
- Edge-triggered flip-flops



Other Flip-Flops

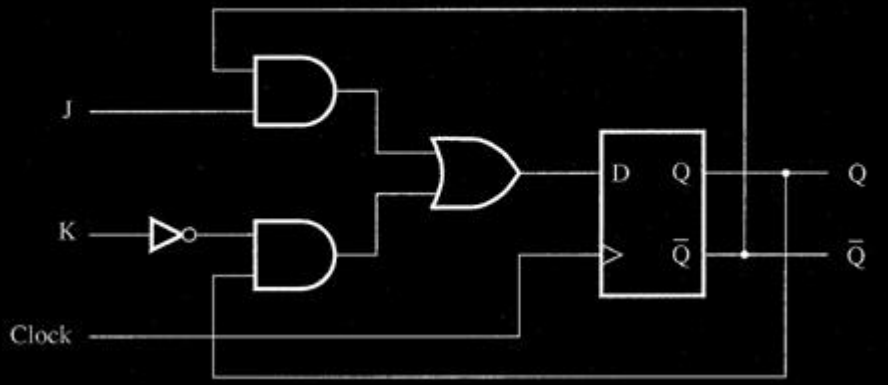
- The T flip-flop:
  - Like the D flip-flop, except that it toggles its value whenever the input to T is high.

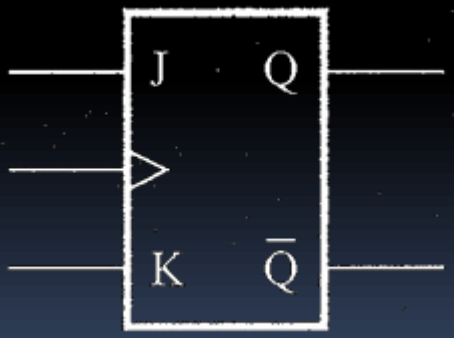




Other Flip-Flops

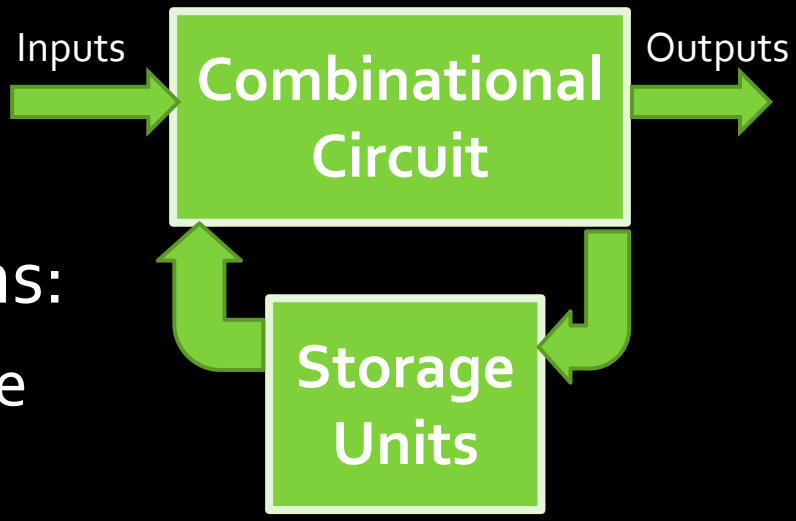
- The JK Flip-Flop:
  - Takes advantage of all combinations of two inputs (J & K) to produce four different behaviours:
    - if J and K are 0, maintain output.
    - if J is 0 and K is 1, set output to 0.
    - if J is 1 and K is 0, set output to 1.
    - if J and K are 1, toggle output value.





Sequential circuit design

- Similar to creating combinational circuits, with extra considerations:
  - The flip-flops now provide extra inputs to the circuit
  - Extra circuitry needs to be designed for the flip-flop inputs.
  - …which is next week's lecture ☺



Today we learned

- Sequential circuits – circuits with memory
- Latch
- Flip-flop

Next week

- Registers, Counters
- Finite State Machines
- Sequential circuit design