|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Address | Offset | Name | Value | Notes |
| BASE | 0x50200000  0x50300000 | Null | PIO0  PIO1 | Null | Null |
| CTRL | 0x50200000 | 0x000 | PIO control register | 0000 0000 0000  ---- ---- ---- ---- ---- | Since the SM\_ENABLE, SM\_RESTART, and CLKDIV\_RESTART is rest to 0x0. Additionally, ‘-’ means reserved so, we cannot find the detail values. |
| FSTAT | 0x50200004 | 0x004 | FIFO status register | 0000 ---- 1111 ----0000 ---- 1111 ---- | Since the first 4 bits of RXFULL and TXFULL are 0 after reset and the rest 4 bits are reserved. Additionally, the first 4 bits of RXEMPTY and TXEMPTY are 1 and the rest of them are reserved. |
| FDEBUG | 0x50200008 | 0x008 | FIFO debug register | 0000 ---- 0000 ---- 0000 ---- 0000 ---- | Since the first 4 bits of RXSTALL, RXUNDER, TXOVER, and TXSTALL are 0 after resetting. Additionally, the rest of 4 bits of them are reserved. |
| FLEVEL | 0x5020000c | 0x00c | FIFO levels | 0x0000 | All of bits of this register is rested to 0 after offsetting, and no reserved bits in this register. |
| TXF0  TXF1  TFX2  TFX3 | 0x50200010  0x50200014  0x50200018  0x5020001c | 0x010  0x014  0x018  0x01c | TX FIFO | 0x0000 | All of bits of this register is rested to 0 after offsetting, and no reserved bits in this register. Additionally, there are on messages printed out. |
| RXF0  RXF1  RXF2  RXF3 | 0x50200020  0x50200024  0x50200028  0x5020002c | 0x020  0x024  0x028  0x02c | RX FIFO | 0x0000 | All of bits of this register is rested to 0 after offsetting, and no reserved bits in this register. Additionally, there are no messages received. |
| INSTR\_MEM0 | 0x50200048 | 0x048 | Instruction memory 0 | 0000 0000 0000 0000  ---- ---- ---- ---- | Since, the first half of this register is rested to 0 and the last parts are reserved. |
| … | … | … | … | … | … |
| INSTR\_MEM31 | 0x502000c4 | 0x0c4 | Instruction memory 31 | 0000 0000 0000 0000  ---- ---- ---- ---- | Similarly, as INSTR\_MEM0 |
| SM0\_CLKDIV | 0x502000c8 | 0x0c8 | Clock divisors register for state machine 0 | ---- ---- 0000 1111 0011 1111 0000 0000 | The first 8 bits are reserved, and FRAC is rested to 0. Additionally, the system clock is 125 Mhz, and the cycles\_per\_bit is 10. |
| SM0\_EXECCTRL | 0x502000cc | 0x0cc | Execution/behavioral settings for state machine 0 | 0000 0--0 0000 0001 1111 0000 0000 0000 | Since the 5 to 6 bits are reserved and 12 to 16 bits are offset to 0x1f, and the rest of them are rested to 0. |
| SM0\_SHIFTCTRL | 0x502000d0 | 0x0d8 | Shift registers for state machine 0 | ---- ---- ---- ---- 0011 0000 0000 0000 | Since the first half register’s bits are reserved and 18 ,19 bits are rest to 1. |
| SM0\_ADDR | 0x502000d4 | 0x0d4 | Current instruction addresses of state machine 0 | 0000 ---- ---- ----  ---- ---- ---- ---- | Because the first 4 bits are rested to 0 and the rest bits of it are reserved. |
| SM0\_INSTR | 0x502000d8 | 0x0d8 | Instruction registers for state machine 0 | 0x---- |  |
| SM0\_PINCTRL | 0x502000dc | 0x0dc | State machine pin control 0 | 0000 0000 0000 0000 0000 0000 0010 1000 | Since only the 26 to 28 bits are offset to 0x5(101). |
| SM1\_CLKDIV | 0x502000e0 | 0x0e0 | Clock divisors register for state machine 1 | ---- ---- 0000 1111 0011 1111 0000 0000 | Similar to SM0\_CLKDIV |
| SM1\_EXECCTRL | 0x502000e4 | 0x0e4 | Execution/behavioral settings for state machine 1 | 0000 0--0 0000 0001 1111 0000 0000 0000 | Similar to SM0\_ EXECCTRL |
| SM1\_SHIFTCTRL | 0x502000e8 | 0x0e8 | Control behavior of the input/output shift registers for state machine 1 | ---- ---- ---- ---- 0011 0000 0000 0000 | Similar to SM0\_ SHIFTCTRL |
| SM1\_ADDR | 0x502000ec | 0x0ec | Current instruction addresses of state machine 1 | 0000 ---- ---- ----  ---- ---- ---- ---- | Similar to SM0\_ ADDR |
| SM1\_INSTR | 0x502000f0 | 0x0f0 | Instruction registers for state machine 1 | x---- | Similar to SM0\_ INSTR |
| SM1\_PINCTRL | 0x502000f4 | 0x0f4 | State machine pin control 1 | 0000 0000 0000 0000 0000 0000 0010 1000 | Similar to SM0\_ PINCTRL |
| SM2\_CLKDIV | 0x502000f8 | 0x0f8 | Clock divisors register for state machine 2 | ---- ---- 0000 1111 0011 1111 0000 0000 | Similar to SM0\_CLKDIV |
| SM2\_EXECCTRL | 0x502000fc | 0x0fc | Execution/behavioral settings for state machine 2 | 0000 0--0 0000 0001 1111 0000 0000 0000 | Similar to SM0\_ EXECCTRL |
| SM2\_SHIFTCTRL | 0x50200100 | 0x100 | Shift registers for state machine 2 | ---- ---- ---- ---- 0011 0000 0000 0000 | Similar to SM0\_ SHIFTCTRL |
| SM2\_ADDR | 0x50200104 | 0x104 | Current instruction addresses of state machine 2 | 0000 ---- ---- ----  ---- ---- ---- ---- | Similar to SM0\_ ADDR |
| SM2\_INSTR | 0x50200108 | 0x108 | Instruction registers for state machine 2 | 0x---- | Similar to SM0\_ INSTR |
| SM2\_PINCTRL | 0x5020010c | 0x10c | State machine pin control 2 | 0000 0000 0000 0000 0000 0000 0010 1000 | Similar to SM0\_ PINCTRL |
| SM3\_CLKDIV | 0x50200110 | 0x110 | Clock divisors register for state machine 3 | ---- ---- 0000 1111 0011 1111 0000 0000 | Similar to SM0\_CLKDIV |
| SM3\_EXECCTRL | 0x50200114 | 0x114 | Execution/behavioral settings for state machine 3 | 0000 0--0 0000 0001 1111 0000 0000 0000 | Similar to SM0\_ EXECCTRL |
| SM3\_SHIFTCTRL | 0x50200118 | 0x118 | Shift registers for state machine 3 | ---- ---- ---- ---- 0011 0000 0000 0000 | Similar to SM0\_ SHIFTCTRL |
| SM3\_ADDR | 0x5020011c | 0x11c | Current instruction addresses of state machine 3 | 0000 ---- ---- ----  ---- ---- ---- ---- | Similar to SM0\_ ADDR |
| SM3\_INSTR | 0x50200120 | 0x120 | Instruction registers for state machine 3 | 0x---- | Similar to SM0\_ INSTR |
| SM3\_PINCTRL | 0x50200124 | 0x124 | State machine pin control 3 | 0000 0000 0000 0000 0000 0000 0010 1000 | Similar to SM0\_ PINCTRL |