A 2.5 GS/s 7-Bit 5-Way Time-Interleaved SAR ADC With On-Chip Background Offset and Timing-Skew Calibration

Kiho Seong, *Graduate Student Member, IEEE*, Jae-Soub Han, *Graduate Student Member, IEEE*, Yong Shim, *Member, IEEE*, and Kwang-Hyun Baek, *Senior Member, IEEE*

***Abstract*—This brief presents the on-chip background offset and timing-skew calibration of the 1-then-2b/cycle time-interleaved successive-approximation-register analog-to-digital converter (TI SAR ADC). For timing-skew between sub-ADC's sampling clocks, a comparator offset-based window detector (WD) is used to adjust the clock edge misalignment. In addition, comparator offset calibration is considered both in terms of 1) global offset (between the offset-free reference comparator and the local reference comparator in each sub-ADC) and 2) local offset (between the local reference comparator and the rest of the comparators in the same sub-ADC). The proposed calibration sufficiently suppresses noise floor and spurs, and all calibrations are performed in the background without interfering with normal ADC operation. The prototype 5-way TI SAR ADC is fabricated in a 28 nm CMOS process and occupies a 0.03 mm^2 area including on-chip calibration. With the proposed calibration, the prototype achieves SNDR of 40 dB at Nyquist input and consumes 7.57 mW, leading to the Walden figure of merit (FoM$_W$) of 37.2 fJ/conversion-step.**

***Index Terms*—SAR ADC, time-interleaved, background calibration, multi-bit/cycle.**

I. Introduction

Wireless communication systems and serial link transceivers require high-speed and medium-resolution analog-to-digital converter (ADC) [1]–[3]. Time-interleaved successive-approximation-register ADC (TI SAR ADC) is the most promising candidate for these applications based on 1) compatibility with CMOS scaling due to mostly digital-based structure and 2) power-efficient architecture using multiple ADCs at low-speed operating frequency. However, due to the nature of multi-ADC, TI SAR ADC suffers from the mismatches such as timing-skew and offset between sub-ADCs [4], [5]. To overcome these mismatches, various calibration techniques have been proposed [6]–[13].

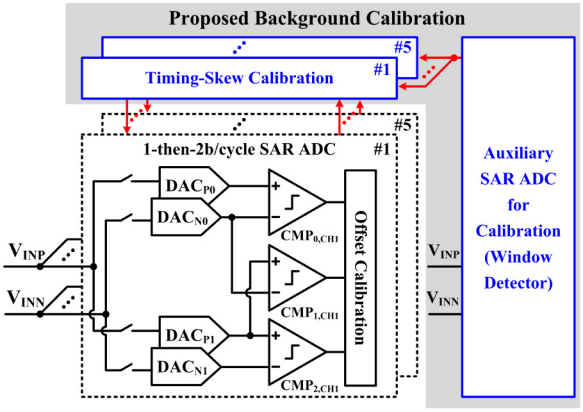

Fig. 1. Block diagram of the proposed 5-way TI SAR ADC with background calibration.

Recently, a 1-then-2b/cycle architecture using the background offset calibration method was proposed in [7] as shown in Fig. 1 (inside the lower-left dotted box). This calibration method effectively eliminates local offset mismatches among comparators within sub-ADCs, but offset mismatches still exist between comparators within different sub-ADCs. This global offset degrades the performance of TI ADC. Moreover, [7] adopts a common clock bootstrap method that takes great effort to route clock signals to reduce timing-skew mismatches. However, this approach will face difficulties as the number of sub-ADCs increases.

There have been many studies to overcome the timing-skew mismatch, one of which is timing-skew calibration using a window detector (WD) [6]. WD is assumed to be a good timing-skew estimator, but the structure introduced in [6] shows a vulnerability to environmental changes that require an additional calibration scheme resulting in high design complexity. To solve the design problem, [12] proposed a WD based on the offset applied to the comparator. By introducing an offset voltage to the comparator and creating a window, the WD design becomes concise. However, setting the proper window width still requires foreground calibration, which interrupts normal operation and reduces overall throughput.

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The authors are with the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea (e-mail: yongshim@cau.ac.kr; kbaek@cau.ac.kr).

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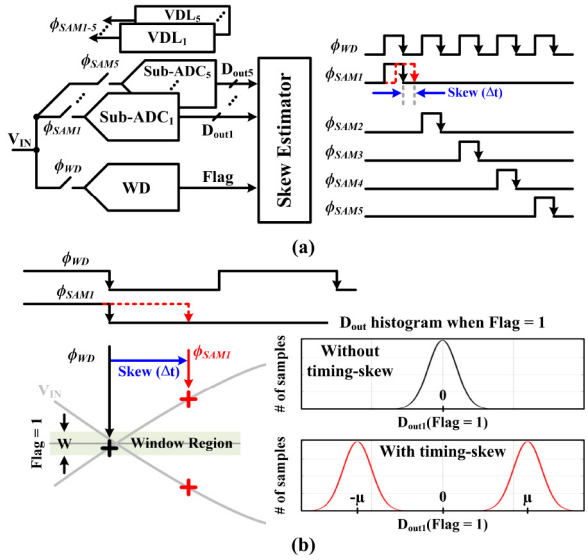

Fig. 2. (a) Architecture of the TI ADC with window detector and its timing diagram, (b) D_{out} histogram of corresponding ADC with and without skew.

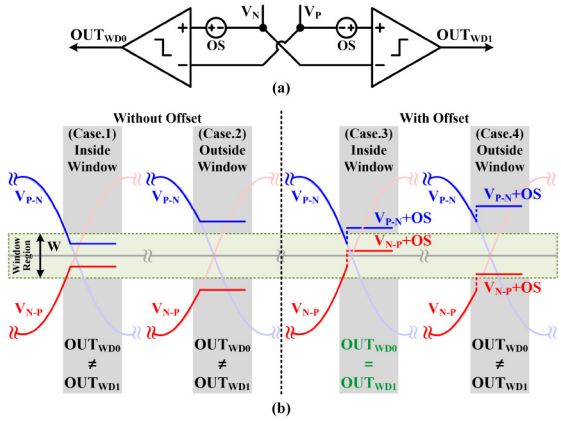

Fig. 3. Comparator offset-based window detector.

Based on the above issues, this brief proposes background offset and timing-skew calibration using the WD. A simple block diagram of the proposed TI SAR ADC is shown in Fig. 1. Apart from the five sub-ADCs, there is an auxiliary SAR ADC for background calibration and the timing-skew calibration logics for correcting skew between the sub-ADCs.

Here, the core idea of this brief can be summarized as follows: 1) The background timing-skew and offset calibration based on WD, and it allows the proposed ADC to operate seamlessly without additional calibration phases. 2) The global offset (between comparators within different sub-ADCs) and local offset (between comparators within the same sub-ADC) are simultaneously calibrated, thereby improving the overall performance of the ADC.

The rest of this brief is organized as follows. Section II describes the concept of WD to detect skew between ADCs. The proposed architecture and calibration procedure are introduced in Section III. The comparison of measurement results with state-of-the-art TI SAR ADC is shown in Section IV. Finally, the conclusion is presented in Section V.

II. Window Detector

A. Timing-Skew Detection Through Voltage Window

Fig. 2(a) shows the overall architecture and timing diagram of the WD-based TI ADC [6], [8], [9], [12]. It consists of five sub-ADCs (Sub-ADC$_{1-5}$), a WD, and a skew estimator. The sub-ADCs and WD sample the input at the falling edge of the sampling clock ($\phi_{SAM1-5,WD}$). WD has a full-rate sampling clock (ϕ_{WD}), while each sub-ADC has an interleaved clock (ϕ_{SAM1-5}). That is, only one sub-ADC sample the input (V_{IN}) simultaneously with the WD. The main idea of skew estimation using WD is shown in Fig. 2(b). The skew estimation event occurs when the WD samples (ϕ_{WD}) the V_{IN}'s zero-crossing point. The WD then generates a flag to activate the skew estimator, which collects digital output (D_{out}) from the sub-ADC. If there is no skew between the sampling clocks, the D_{out} is expected to have a zero mean and some distribution. Meanwhile, when the skew is Δt, the sampled D_{out} distribution has a non-zero mean (for instance, $\pm\mu$ in Fig. 2(b)).

B. Mean Absolute Deviation

The timing-skew between sampling clocks of different sub-ADCs is now expressed as the mean value of the digital output captured by the skew estimator. Since the mean value of D_{out} can have both positive and negative values, taking the absolute mean value of the received D_{out}, ($E(|D_{out}|) = \mu$ in Fig. 2(b)) becomes a good indicator of skew. This is the main idea of skew estimation based on mean absolute deviation (MAD) [9]. Therefore, the calibration process should minimize this mean value (μ) by adjusting the delay from the variable delay line (VDL) in Fig. 2(a) which controls the sampling timing of each sub-ADC.

C. Comparator Offset-Based Window Detector

The input cross-coupled comparators having an offset can be used as a simple and robust WD [12] as shown in Fig. 3(a). In Fig. 3(b), assume that $V_{P,N}$ are differential input, and the gray background represents the sampled signal.

First of all, if there is no offset, the outputs of comparators, regardless of the V_{P-N}, always have different polarities. On the other hand, if the comparators have an offset (V_{OS}), the outputs possibly then have the same polarity if the input difference is sufficiently small, especially if the sampled input difference is less than the offset (Case 3). If the magnitude of the offset is expressed as half of the voltage window width, the comparator outputs have the same polarity when the sampled input difference is within the window width (V_{P-N}<W).

However, [12] adopts foreground offset calibration to make comparators as a WD, which requires an additional phase interfering with normal operation and needs an additional input signal for calibration. In this brief, the background window width control method (offset control) resolves these disadvantages.

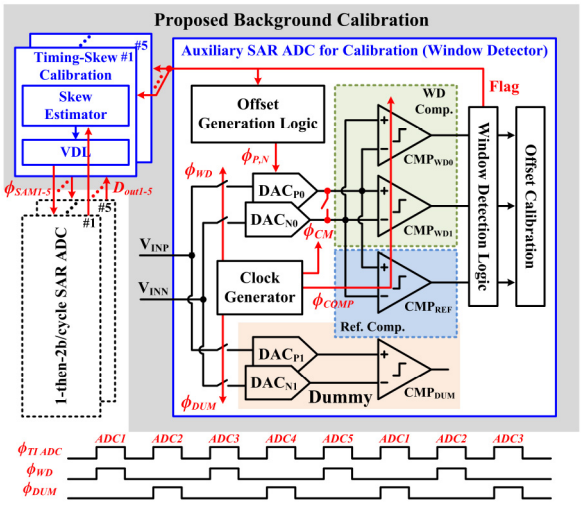

Fig. 4. Overall architecture of the proposed 5-way TI SAR ADC.

III. Overall Architecture and Background Calibration

Fig. 4 shows the overall architecture of the proposed TI SAR ADC. It is divided into three main parts: five sub-ADCs, timing-skew calibration blocks, and an auxiliary SAR ADC with WD for calibration. The timing-skew calibration block reduces the skew by adjusting the sampling clocks (ϕ_{SAM1-5}) based on the information obtained from the calibration. The remaining auxiliary SAR ADC is a crucial part of the WD for skew estimation and offset calibration. Basically, this unit is a simple replica of a sub-ADC with input cross-coupling comparators ($CMP_{WD0,WD1}$), a reference comparator (CMP_{REF}), CDACs ($DAC_{P0,N0}$), and an offset calibration unit. Apart from these basic components, there are additional units, including a clock generator, an offset generation logic, a window detection logic, and a dummy ADC having CMP_{DUM} and $DAC_{P1,N1}$. Note that, WD samples the input at half the ADC sampling rate (ϕ_{WD}) to ensure sufficient detection and calibration time. Since this causes input impedance variation, dummy ADC is used to sample inputs for the remaining half-cycle of the clock (ϕ_{DUM}), ensuring that the auxiliary ADC operates at a full ADC sampling rate without impedance issues [6], [8], [9], [12].

A. Background Window Control Using Offset Calibration

Fig. 5 shows a block diagram and waveforms of the proposed background window control scheme using offset calibration. In addition, from a calibration point of view, $CMP_{WD0,WD1}$ operate mostly the same. Therefore, the window control procedure for CMP_{WD1} is explained only for simplicity. In the sampling phase (ϕ_{WD}), the comparator input difference (V_{P-N}) tracks the input signal difference ($V_{INP-INN}$). At the end of the sampling period, when the sampled input difference is sufficiently small and is within the window region, the flag signal is generated. When the flag signal is activated, the ϕ_{CM} signal briefly shorts the comparator differential input and induces $V_{P-N} = 0$ right after the next sampling phase. Thereafter, the switch ϕ_P for the LSB capacitor in the DAC_{P0} is closed, and accordingly, $V_{P-N} = 1$ LSB. Then, the OUT_{WD1}, becomes high, which increases the offset control voltage (CAL_{WD1}) inside the offset calibration unit. This operation is repeated for 15 cycles after the flag signal is activated, and the CAL_{WD1} level rises until the OUT_{WD1} is low even at the $V_{P-N} = 1$ LSB. The waveform in which the CAL_{WD1} decreases when this event occurs is shown in cycle 14 in Fig. 5, which means that offset calibration converges so that the CMP_{WD1} has an internal 1 LSB offset.

The calibration process for the CMP_{WD0} is almost the same except for ϕ_N switching, not ϕ_P. This makes $V_{P-N} = -1$ LSB, and the corresponding offset of CMP_{WD0} is 1 LSB. This entire process is used to incorporate the 1 LSB offset into each comparator. Since the voltage step for offset calibration ($\Delta CAL_{WD0,1}$) is small, the window width is gradually adjusted to be proportional to ± 1 LSB. Lastly, because the CMP_{REF} must be offset-free for global offset calibration, the above offset calibration procedure can be used in the same way except for introducing 1 LSB voltage into the input terminal.

B. Individual Loop Local-Global Offset Calibration

The proposed ADC provides simultaneous local-global offset calibration. Fig. 6(a) shows the simplified architecture of the proposed TI SAR ADC to illustrate the local-global offset calibration loops (only the components participating in this calibration are displayed in black). As discussed before, each sub-ADC has three comparators (CMP_{0-2}) to resolve 2b/cycle, and the auxiliary ADC has three comparators inside ($CMP_{WD0,WD1}$, and CMP_{REF}). During global offset calibration, the CMP_{REF} is used as the zero-offset reference for the comparator (CMP_1) in each sub-ADC. In other words, the CMP_1 of the sub-ADC corrects its own offset characteristics to the CMP_{REF} through the offset calibration (OS CAL) unit. Meanwhile, the CMP_1 of each sub-ADC functions as a local reference and is used to correct the offsets of the remaining comparators, $CMP_{0,2}$, of the same sub-ADC.

A detailed of the OS CAL unit is shown in Fig. 6(c). It consists of a decision logic, a 6-bit counter, a 6-bit R-2R DAC, and control switches. Here, the decision logic gets two comparator outputs, one from the reference comparator and the other from the comparator to be calibrated. And it controls the up/down counter and switches to change the analog voltages ($V_{BP,BN}$) generated by R-2R DAC which is applied to the additional transistors ($M_{CP,CN}$). Then $M_{CP,CN}$ acts as a static load with varying strength depending on the voltage applied to the gate, mimicking the offset to the comparator. The offset calibration range is ± 35 mV which can cover the estimated offset ($3\sigma = 30$ mV) with a calibration step of 1 mV. It should be noted here that the proposed offset calibration simultaneously calibrates the global and local offset, unlike similar architecture that only correct the local offset in [7], and it has low complexity than traditional LMS-based digital background calibration. In addition, since the two loops operate independently, the system stabilizes during the dual loop operation. Fig. 6(b) conceptually shows individual loops for local ($Loop_L$) and global offset calibration ($Loop_G$).

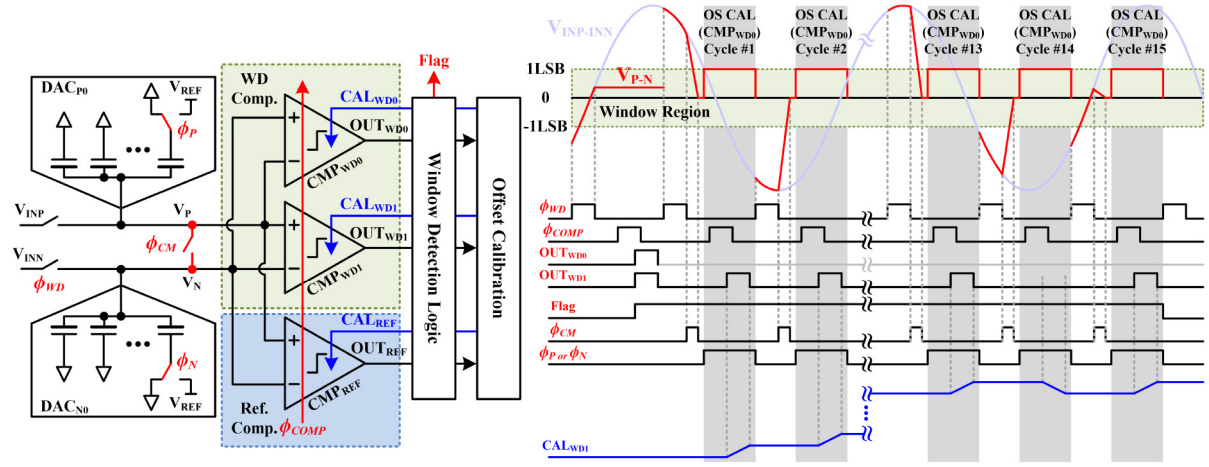

Fig. 5. Background window width control for window detector.

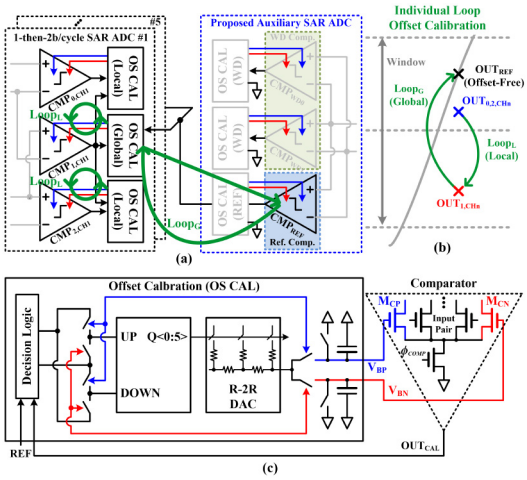

Fig. 6. (a) Architecture of the local-global offset calibration, (b) calibration procedure, and (c) block diagram of the offset calibration.

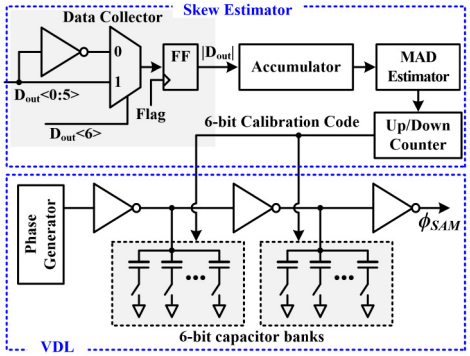

Fig. 7. Block diagram of the skew estimator and variable delay line (VDL).

C. Timing-Skew Calibration

The timing-skew calibration block controls the sampling timing to eliminate the skew between sub-ADCs. Fig. 7 shows its implementation, where the unit consists of 1) a skew estimator that collects digital output from sub-ADC and 2) a VDL that adjusts the sampling clock for skew calibration. The skew estimator consists of a data collector, an accumulator, a MAD estimator, and an up/down counter. If flag is enabled, the data collector takes the absolute value of the D_{out}. Thereafter, the data $|D_{out}|$ is accumulated and averaged through the accumulator. The current mean value $E_n(|D_{out}|)$ is then compared with the previous $E_{n-1}(|D_{out}|)$ in the MAD estimator, and it is used to update the up/down counter. Accordingly, the output of the up/down counter is controlled to minimize the skew between the sampling clocks by adjusting the VDL and the 6-bit capacitor bank. The calibration range of VDL is ±15 ps and the step length is 0.5 ps. It can cover the estimated timing-skew mismatch (3σ = 10 ps) and achieve the SNDR of 40 dB. Note that the global offset calibration step of 63 cycles is performed within the timing-skew calibration of one cycle and it converges before skew calibration. Therefore the global offset calibration does not affect skew calibration.

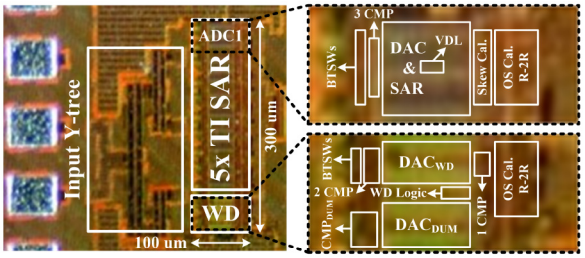

Fig. 8. Die photo.

IV. Measurement Results

The proposed TI SAR ADC was fabricated in a 28 nm CMOS process. Fig. 8 shows a prototype chip microphotograph, which occupies 0.03 mm^2 including five sub-ADCs and WD for on-chip calibration. The proposed ADC adopts symmetrical input Y-tree [14] to minimize bandwidth mismatch, and the full-custom unit MOM capacitor (1 fF) is designed to reduce CDAC mismatch and gain error. The ADC has an input range of 1.72 $V_{pp,diff}$. Fig. 9(a, b) shows dynamic performance measured at different input frequencies with and without calibration. The careful layout of CDAC mitigates the effect of gain mismatch, and as a result, the gain mismatch spurs

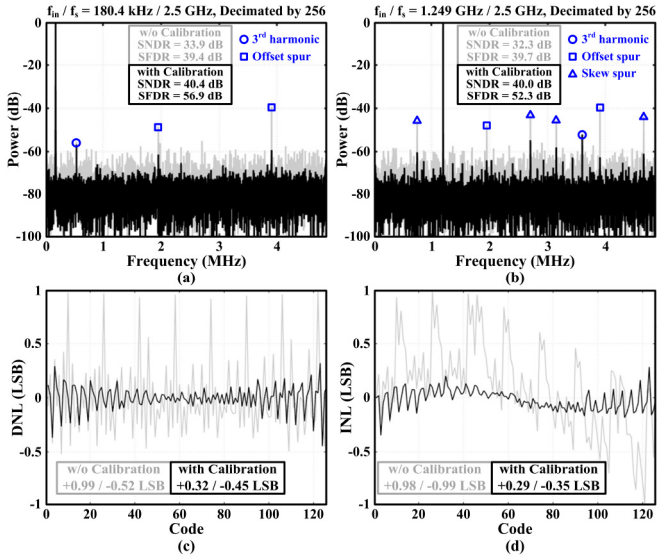

Fig. 9. Measured (a, b) dynamic and (c, d) static performance.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART TI SAR ADC

	JSSC'17 [2]	JSSC'18 [7]	TCAS-I'21 [13]	**This Work**
Architecture	16x TI SAR	1-2b 2x TI SAR	2x TI SAR	**1-2b 5x TI SAR**
Technology (nm)	40	28	28	**28**
Supply (V)	1.1	0.9	1.2/0.9	**0.9**
Resolution (bit)	8	7	7	**7**
fs (GS/s)	2	2.4	2	**2.5**
SNDR (dB)	39.4	40.1	36.4	**40.0**
SFDR (dB)	55.1	54.3	47.8	**52.3**
DNL (LSB)	-0.6/0.6	0.49	-0.98/0.86	**-0.45/0.32**
INL (LSB)	-0.6/0.6	0.57	-1.4/1.5	**-0.35/0.29**
Power (mW)	54.2	5	7.62	**7.57**
FoM$_W$ (fJ/c.-s)	355	25.3	70.8	**37.2**
Area (mm^2)	0.54	0.0043	0.0082	**0.03**

are not shown in Fig. 9(a). The proposed calibration effectively suppresses noise floor and spurs, resulting in significant improvements in dynamic performance. Note that, noise floor becomes an issue due to offset mismatch between comparators in sub-ADC, and spurs are mainly due to offset and timing-skew mismatch of each sub-ADC. As can be seen in Fig. 9(b), SNDR and SFDR at Nyquist-frequency inputs are improved to 40 dB and 52.3 dB from 32.3 dB and 39.7 dB, respectively. As shown in Fig. 9(c, d), the static performance, DNL and INL using the proposed calibration technique were found to be $-0.45/0.32$ LSB and $-0.35/0.29$ LSB, respectively. Table I summarizes the overall performance of the prototype and compares it with the state-of-the-art TI SAR ADC with similar specifications. Compared to a similar architecture in [7], the proposed work exhibits similar dynamic performance and better static performance even with more sub-ADCs. Note that, the TI ADC proposed in [7] targets small CDACs, which reduce silicon footprint and power consumption at the expense of static performance. Finally, the proposed ADC achieves the Walden figure of merit (FoM$_W$) of 37.2 fJ/conversion-step.

V. CONCLUSION

In this brief, an on-chip background offset and timing-skew calibration techniques are presented to compensate the mismatch of 1-then-2b/cycle TI SAR ADC. The proposed local-global offset calibration not only compensates offset errors between comparators of each sub-ADC, but also calibrates offset mismatch between sub-ADCs operating in a time-interleaved manner. In addition, timing-skew calibration using WD compensates for sampling clock timing-skew between sub-ADCs. With all calibration techniques applied, the prototype chip fabricated in a 28 nm CMOS process shows sufficiently low noise floor and spurs. The measured dynamic performance is 40 dB SNDR and 52.3 dB SFDR at Nyquist rates, with the power consumption of 7.57 mW. This leads to the FoM$_W$ as 37.2 fJ/conversion-step.

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