Explicit Formula for Channel Mismatch Effects in Time-Interleaved ADC Systems

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Abstract – A time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits. In the system, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. However, mismatches such as offset, gain mismatches among channel ADCs as well as timing skew of the clocks distributed to them degrade S/N of the ADC system as a whole. This paper analyzes the channel mismatch effects in the time-interleaved ADC system. Previous analysis showed the effect for each mismatch *individually*, however in this paper we derive *explicit* formula for the mismatch effects when *all* of offset, gain and timing mismatches exist together. We have clarified that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent from them, and this can be seen clearly in frequency domain. We also discuss the bandwidth mismatch effect. The derived formula can be used for calibration algorithms to compensate for the channel mismatch effects.

Keywords : ADC, Interleave, Channel Mismatch, Calibration, Error Correction

1. Introduction

Electronic devices are continuously getting faster and accordingly the need for instruments such as digitizing oscilloscopes and LSI testers to measure their performance is growing. A/D converters (ADCs) incorporated in such instruments have to operate at very high sampling rate. This paper studies theoretical issues of a time-interleaved ADC system where several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate [1, 2, 3, 4, 5]. Fig.1 shows such an ADC system where each M channel ADCs $(ADC_1, ADC_2, ..., ADC_M)$ operates with one of M phase clocks $(CK_1, CK_2, ..., CK_M)$. The sampling rate of the ADC as a whole is M times the channel sampling rate. This time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits, and is widely used. Ideally characteristics of channel ADCs should be identical, and clock skew should be zero. However, in reality there are mismatches such as offset, gain mismatches among channel ADCs as well as timing skew of the clocks distributed to them, which cause so-called *pattern noise* and significantly degrade S/N (effective bits) of the ADC system as a whole. Hence calibration often has to be performed to ensure uniformity among the characteristics of the channels. It is important to clarify the issues of the interleaved ADC architecture when designing the system.

This paper first reviews interleaving issues: the effects of offset, gain and timing mismatches *individually* [3, 4, 5, 6, 7, 8, 9]. Then we will derive *explicit* formula for the mismatch effects when all of offset, gain and timing mismatches exist together, and show that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent from them. We also analyze the bandwidth mismatch effect. The derived formula can be used for calibration algorithms to compensate for the channel mismatch effects. In this paper we concentrate on 2-channel and 4-channel interleaved systems because most practical applications use them; 8-channel or other types are rarely used in practical situation. However note that extension of these results to interleaved systems with a different number of channels is also possible.

Hereafter, we will use following notations:
M: number of channel ADCs in the ADC system,
f_{noise}: pattern noise frequency of the ADC output,
f_{in}: input frequency applied to the ADC system,
f_s: sampling frequency of the ADC system,
f_s/M: sampling frequency of each channel ADC.

2. Individual Channel Mismatch Effects

This section reviews the effects of offset, gain and timing mismatches *individually* in interleaved ADC systems.

A. Offset Mismatch Effects: Suppose that the offsets of each channel are different and the other characteristics are identical (Fig.2). This mismatch causes *fixed pattern noise* in the ADC system; for a DC input, each channel may produce a different output code and the period of this error signal is M/f_s. The pattern noise is almost independent of the input signal in time and frequency domains, and it is additive noise in time domain while in frequency domain it causes noise peaks at $f_{noise} = k \times f_s/M$ $(k = 1, 2, 3, ...)$. The S/N degradation of the ADC system (total pattern-noise power) due to the offset mismatch is constant regardless of the input frequency f_{in}.

B. Gain Mismatch Effects: Suppose that the gains of each channel are different and the other characteristics are identical (Fig.3). If a sinusoidal input signal is applied to the system, the largest difference in channel outputs occurs at the peaks of the sine wave. As with the offset mismatch case, the basic error occurs with a period of M/f_s but the magnitude of the error is modulated by the input frequency f_{in}. Thus the pattern noise due to gain mismatch is multiplicative in time domain while noise spectrum peaks are at $f_{noise} = -f_{in} + k \times f_s/M$ $(k = 1, 2, 3, ...)$. f_{noise} depends on f_{in} while the S/N degradation of the ADC system due to the gain mismatch is independent of f_{in}. Also note that in the offset mismatch case the S/N degradation (noise power) is independent of the amplitude of the input but in the gain mismatch case it depends on the amplitude.

C. Clock Timing Error Effects: There are two kinds of timing errors in an interleaved ADC system: clock skew (systematic error) and clock jitter (random error). Clock jitter effects are unavoidable in any ADC system but the interleaved architecture also suffers from clock skew effects. Suppose that the clocks $CK_1, CK_2, ..., CK_M$ have skews $dt_1, dt_2, ..., dt_M$ (Fig.4). This skew causes noise in the ADC system, and in the time domain the largest error occurs when the input signal has the largest slew rate, or crosses zero. The envelop of the error signal is the largest at the zero-crossings with a period of M/f_s; it is shifted by 90 degrees compared to the gain mismatch case. In the frequency domain, as with the gain mismatch case, the basic error occurs with a period of M/f_s and the magnitude of the error is modulated by the input frequency f_{in}; the noise spectrum peaks are at $f_{noise} = -f_{in} + k \times f_s/M$ $(k = 1, 2, 3, ...)$. Note that S/N degrades as f_{in} increases.

3. Combined Channel Mismatch Effects

In this section we will derive *explicit* formula for the mismatch effects when all of offset, gain and timing mismatches exist together, and show that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent of them.

A. 2-channel Interleaved ADC $(M = 2)$: First we consider a two-channel interleaved ADC system. Fig.5 shows its configuration where each of two channel ADCs (ADC_1, ADC_2) operates with one of two-phase clocks (Φ_1, Φ_2 with a period of $2T_s$) respectively. The sampling rate of the ADC as a whole is twice the channel sampling rate (f_s where $f_s := 1/T_s$). However, as mentioned before, this interleaved ADC system suffers from channel mismatch effects [6, 7, 9]: gain mismatch, offset mismatch and timing mismatch [7, 9]. Ideally ADC_1 and ADC_2 should be identical, however in reality their gains and offsets may be different each other, and also the sampling timings may deviate from Φ_1 and Φ_2. Let the gains of ADC_1, ADC_2 be G_1, G_2 respectively, and their offsets be os_1, os_2 respectively. Also let the sampling timing deviations from Φ_1 for ADC_1 and Φ_2 for ADC_2 be δt_1, δt_2 respectively. Suppose that the input to the ADC is a sinusoidal signal $V_{in}(t) = A\cos(2\pi f_{in} t)$. Then the output of the two-channel interleaved system is given as follows:

$$V_{out}(n) = \begin{cases} G_1 A\cos(2\pi f_{in}(nT_s + \delta t_1)) + os_1 & (n\text{: odd}) \\ G_2 A\cos(2\pi f_{in}(nT_s + \delta t_2)) + os_2 & (n\text{: even}) \end{cases} \quad (1)$$

Let $G := (G_1 + G_2)/2$, $\alpha := (G_2 - G_1)/(2G)$, $\delta_{cm} := (\delta t_1 + \delta t_2)/2$, $\delta t := \delta t_2 - \delta t_1$, $os_{cm} := (os_1 + os_2)/2$ and $os_{diff} := (os_2 - os_1)/2$. Without loss of generality, we assume that $\delta_{cm} = 0$. Then we obtain the following:

$$V_{out}(nT_s) = A_s\cos(2\pi f_{in} nT_s + \theta_s) + A_n\cos(2\pi(-f_{in} + \frac{1}{2}f_s)nT_s + \theta_n) + os_{cm} + \cos(\pi n) os_{diff} \quad (2)$$

where

$$A_s := AG\sqrt{\cos^2(\pi f_{in}\delta t) + \alpha^2\sin^2(\pi f_{in}\delta t)},$$
$$A_n := AG\sqrt{\alpha^2\cos^2(\pi f_{in}\delta t) + \sin^2(\pi f_{in}\delta t)},$$
$$\theta_s := \arctan(\alpha\tan(\pi f_{in}\delta t)),$$
$$\theta_n := \arctan(\tan(\pi f_{in}\delta t)/\alpha).$$

Remark (i) Let consider in frequency domain, and the frequency of the first term in eq.(2) is f_{in}, that of the second term is $-f_{in} + \frac{1}{2}f_s$, the third one is 0 (DC) and the fourth one is $\frac{1}{2}f_s$. In other words, the first term corresponds to signal while the second term is due to gain and timing mismatches and the fourth term is caused by offset mismatch (the third term is caused by the average offset of ADC_1 and ADC_2).

(ii) Eq.(2) that we have newly derived consider the gain, offset and timing mismatches together and hence this is a very general result. However in previous references [4, 5, 6, 7, 8, 9] each channel mismatch effect in interleaved ADC systems is discussed only individually.
(iii) From eq.(2) we see that the effects of gain and timing mismatch interact each other while the offset mismatch effect is independent.
(iv) Numerical simulation shows that eqs. (1) and (2) match exactly as shown in Fig.6. Also Fig.7 shows numerical simulation result for the SNR due to the gain mismatch and timing skew.

B. 4-channel Interleaved ADC ($M = 4$): Next we consider a four-channel interleaved ADC system, and Fig.8 shows its configuration. Similarly let the gains of ADC_1, ADC_2, ADC_3, ADC_4 be G_1, G_2, G_3, G_4 respectively, and their offsets be os_1, os_2, os_3, os_4 respectively. Also let the sampling timing deviations be δt_1, δt_2 δt_3, δt_4 respectively. Suppose that the input to the ADC is a sinusoidal signal $V_{in}(t) = A\cos(2\pi f_{in}t)$. Then the output of the 4-channel interleaved system is given as follows:

$$V_{out}(n) = \begin{cases} G_1 A\cos(2\pi f_{in}(nT_s + \delta t_1)) + os_1 & (n = 4m) \\ G_2 A\cos(2\pi f_{in}(nT_s + \delta t_2)) + os_2 & (n = 4m+1) \\ G_3 A\cos(2\pi f_{in}(nT_s + \delta t_3)) + os_3 & (n = 4m+2) \\ G_4 A\cos(2\pi f_{in}(nT_s + \delta t_4)) + os_4 & (n = 4m+3) \end{cases} \tag{3}$$

where $m = 0, \pm 1, \pm 2, \pm 3, ...$, and let $G_1 := G(1+\alpha_1)$, $G_2 := G(1+\alpha_2)$, $G_3 := G(1+\alpha_3)$, and $G_4 := G(1+\alpha_4)$. Without loss of generality, we assume that $\delta t_1 + \delta t_2 + \delta t_3 + \delta t_4 = 0$. Then we obtain the following:

$$\begin{aligned} V_{out}(nT_s) &= \sqrt{A_{sc}^2 + A_{ss}^2}\cos(2\pi f_{in}nT_s - \arctan\frac{A_{ss}}{A_{sc}}) \\ &+\sqrt{A_{n1c}^2 + A_{n1s}^2}\cos(2\pi nT_s(f_{in} + \frac{1}{4}f_s) - \arctan\frac{A_{n1s}}{A_{n1c}}) \\ &+\sqrt{A_{n2c}^2 + A_{n2s}^2}\cos(2\pi nT_s(f_{in} + \frac{1}{2}f_s) - \arctan\frac{A_{n2s}}{A_{n2c}}) \\ &+\sqrt{A_{n3c}^2 + A_{n3s}^2}\cos(2\pi nT_s(f_{in} + \frac{3}{4}f_s) - \arctan\frac{A_{n3s}}{A_{n3c}}) \\ &+\frac{1}{4}(os_1 - os_2 + os_3 - os_4)\cos(2\pi nT_s(\frac{1}{2}f_s)) \\ &+\frac{1}{2}\sqrt{(os_1 - os_3)^2 + (os_2 - os_4)^2}\times \\ &\cos(2\pi nT_s(\frac{1}{4}f_s) - \arctan\frac{os_2 - os_4}{os_1 - os_3}) \\ &+(os_1 + os_2 + os_3 + os_4)/4. \end{aligned} \tag{4}$$

where A_{sc}, A_{ss}, A_{n1c}, A_{n1s}, A_{n2c}, A_{n2s}, A_{n3c}, A_{n3s} are appropriately defined (which are omitted here due to space limitation).

Remark Similar arguments described in 2-channel case are valid for 4-channel case. Also numerical simulation shows that eqs. (3) and (4) match exactly as shown in Fig.9.

4. Bandwidth Mismatch Effect

In this section, we will introduce a rather new problem, *bandwidth mismatch*, in an interleaved ADC or an interleaved sampling system, and then we will derive the explicit formula for its effects. Many electrical circuits can be approximated by a first order system (Fig.10); a typical example is an open-loop track/hold circuit in track mode, where the ON-resistance of the sampling switch and the hold capacitor constitute a first order RC circuit. Here we assume that k-th channel ADC is approximated by a first order system and its bandwidth is given by f_k^c, which can be mismatched among channels while there are no mismatches of offset, DC gain and timing discussed in the previous sections. (The reader may argue that the approximation of an ADC to a first order system might be too inaccurate, however, for a track/hold circuit in track mode this approximation is very reasonable and hence the discussion in this section is applicable at least to interleaved sampling systems which consist of an array of track/hold circuits.) Setting the DC gain of each channel to one, without loss of generality, and then the frequency transfer function $H_k(j2\pi f)$ of k-th channel is given by

$$H_k(j2\pi f) = 1/(1 + jf/f_k^c)$$

and for the input of $V_{in}(t) = \cos(2\pi f_{in}t)$, the output $V_{outk}(nT_s)$ is given by

$$V_{outk}(nT_s) = G_k\cos(2\pi f_{in}nT_s + \theta_k)$$

where

$$G_k = 1/\sqrt{1 + (f_{in}/f_k^c)^2}, \qquad \theta_k = -\arctan(f_{in}/f_k^c).$$

We see that the mismatch of the bandwidth f_k^c among channels ($k = 1, 2, .., n$) causes G_k and θ_k mismatches. Note that G_k and θ_k are functions of the input frequency f_{in} as well as the bandwidth f_k^c, and also note that when $f_{in} = 0$, $G_k = 1$ and $\theta_k = 0$. Then we will call the mismatch of G_k as *AC gain mismatch* and also the mismatch of θ_k as *phase mismatch*. Remark that the AC gain mismatch is different from the gain mismatch discussed before in that AC gain mismatch depends on f_{in} but the gain mismatch discussed before does not. Also note that the phase mismatch is somewhat similar but somewhat different from the timing skew mismatch effects.

A. 2-channel Interleaved ADC ($M = 2$): We consider a two-channel interleaved ADC system, where the bandwidth of each channel is given by f_1^c and f_2^c respectively. Then when an input of $V_{in}(t) =$

$\cos(2\pi f_{in}t)$ is applied, the output of the interleaved system is given by

$$V_{out}(n) = \begin{cases} G_1\cos(2\pi f_{in}nT_s + \theta_1) & (n\text{: odd}) \\ G_2\cos(2\pi f_{in}nT_s + \theta_2) & (n\text{: even}). \end{cases}$$

Then we can obtain the following formula:

$$V_{out}(nT_s) = A_s\cos(2\pi f_{in}nT_s + \theta_s)$$

$$+A_n\cos(2\pi(-f_{in} + f_s/2)nT_s + \theta_n),$$

where

$$A_s = \frac{1}{2}\sqrt{G_c^2\cos^2(\theta_d) + G_d^2\sin^2(\theta_d)},$$

$$A_n = \frac{1}{2}\sqrt{G_c^2\sin^2(\theta_d) + G_d^2\cos^2(\theta_d)},$$

$$\theta_s = \arctan\{\frac{G_c\sin(\theta_c)\cos(\theta_d) + G_d\cos(\theta_c)\sin(\theta_d)}{G_c\cos(\theta_c)\cos(\theta_d) - G_d\sin(\theta_c)\sin(\theta_d)}\},$$

$$\theta_n = -\arctan\{\frac{G_c\cos(\theta_c)\sin(\theta_d) + G_d\sin(\theta_c)\cos(\theta_d)}{G_c\sin(\theta_c)\sin(\theta_d) - G_d\cos(\theta_c)\cos(\theta_d)}\},$$

$$G_d = G_1 - G2, \qquad G_c = G_1 + G_2,$$

$$\theta_d = (\theta_1 - \theta_2)/2, \qquad \theta_c = (\theta_1 + \theta_2)/2.$$

Also SNR due to the bandwith mismatch is given by

$$SNR = 10\log_{10}(A_s^2/A_n^2).$$

B. 4-channel Interleaved ADC ($M = 4$): Next we consider a four-channel interleaved ADC system, where the bandwidth of each channel is given by f_1^c, f_2^c f_3^c and f_4^c respectively. Then when the input of of $V_{in}(t) = \cos(2\pi f_{in}t)$ is applied, the output of the interleaved system is given by

$$V_{out}(nT_s) = \begin{cases} G_1\cos(2\pi f_{in}nT_s + \theta_1) & (n = 4m) \\ G_2\cos(2\pi f_{in}nT_s + \theta_2) & (n = 4m+1) \\ G_3\cos(2\pi f_{in}nT_s + \theta_3) & (n = 4m+2) \\ G_4\cos(2\pi f_{in}nT_s + \theta_4) & (n = 4m+3). \end{cases} \quad (5)$$

Then we can obtain the following formula:

$$V_{out}(nT_s) = \sqrt{A_{sc}^2 + A_{ss}^2}\cos\left\{2\pi f_{in}nT_s - \arctan\left(\frac{A_{ss}}{A_{sc}}\right)\right\}$$

$$+\sqrt{A_{n1c}^2 + A_{n1s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n1s}}{A_{n1c}}\right)\right\}$$

$$+\sqrt{A_{n2c}^2 + A_{n2s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{2}f_s\right)nT_s - \arctan\left(\frac{A_{n2s}}{A_{n2c}}\right)\right\}$$

$$+\sqrt{A_{n3c}^2 + A_{n3s}^2}\cos\left\{2\pi\left(f_{in} + \frac{3}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n3s}}{A_{n3c}}\right)\right\}$$

where $A_{sc}, A_{ss}, A_{n1c}, A_{n1s}, A_{n2c}, A_{n2s}, A_{n3c}$ and A_{n3s} are defined appropriately (which are omitted here due to space limitation). The SNR is given by

$$SNR = 10\log_{10}\frac{A_{sc}^2 + A_{ss}^2}{A_{n1c}^2 + A_{n1s}^2 + A_{n2c}^2 + A_{n2s}^2 + A_{n3c}^2 + A_{n3s}^2}.$$

5. Conclusion

We have analyzed the channel mismatch effects in the time-interleaved ADC system, and derived *explicit* formula for the mismatch effects when *all* of offset, gain and timing mismatches exist together. We have clarified that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent from them. Also we discussed the bandwidth mismatch effect. These formula are useful to know how much mismatch is tolerable for a specified SNR. Also based on our derived formula we are investigating algorithms to measure the values of offset, gain and timing mismatches and to compensate for them.

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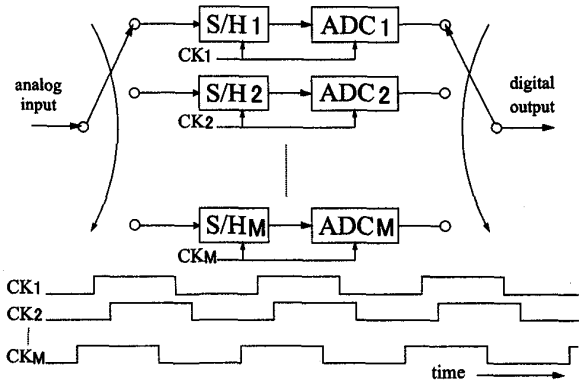
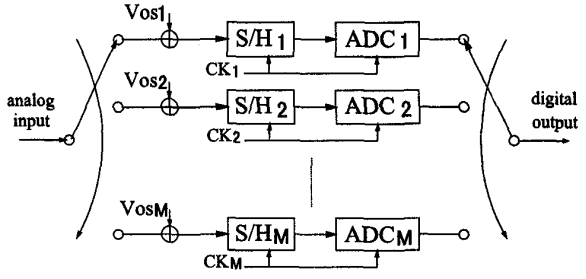
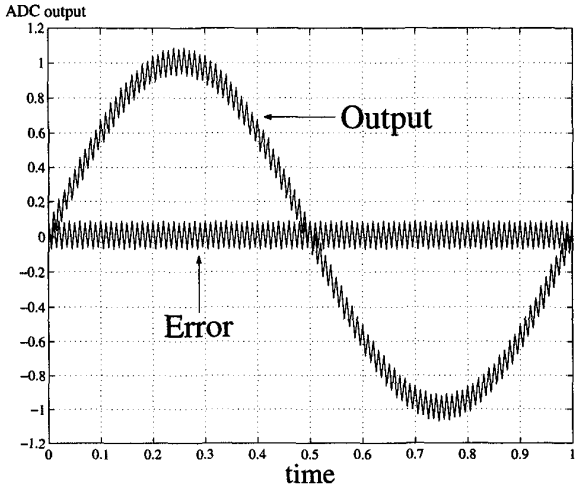


Fig.1: Time-interleaved ADC system.

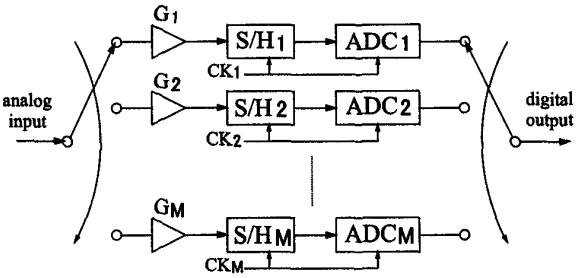


(a): Offset mismatch model. Vos_k represents the offset of k-th channel ($k = 1, 2, ..., M$).

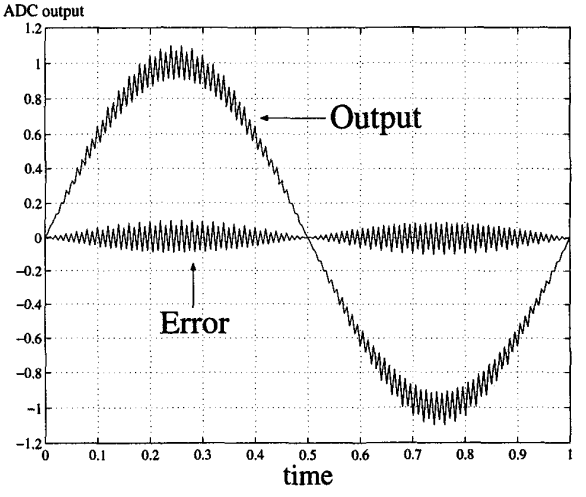


(b): ADC output and error signals for a sinusoidal input.

Fig.2: Offset mismatch effect.



(a): Gain mismatch model. G_k represents the gain of k-th channel ($k = 1, 2, ..., M$).



(b): ADC output and error signals for a sinusoidal input.

Fig.3: Gain mismatch effect.

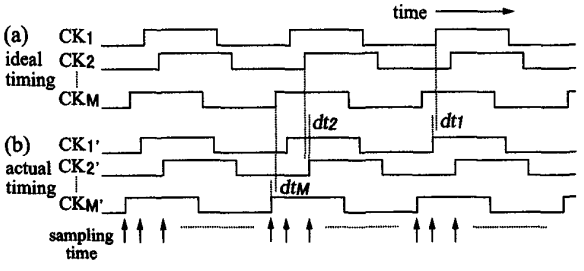


Fig.4: Clock skew. (a) Ideal clock timing. (b) Clock timing with skews of $dt_1, dt_2, ..., dt_M$.

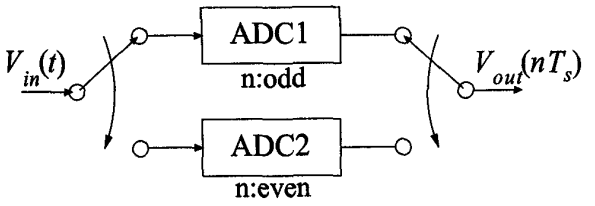


Fig.5: Two-channel time-interleaved ADC system.

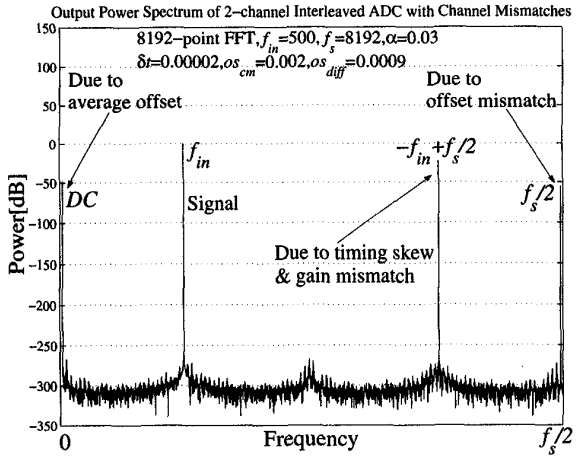


Fig.6: Simulation result of a two-channel time-interleaved ADC system with channel mismatches which verifies the correctness of our derived eq.(2).

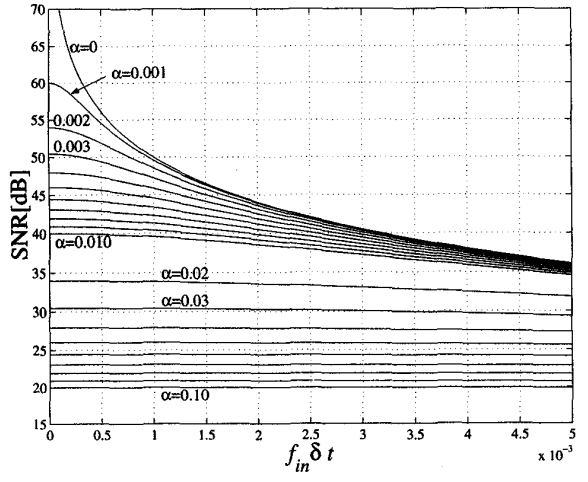


Fig.7: Simulation result of SNR of a two-channel interleaved ADC system with gain mismatch (α) and timing skew (δt) based on eq.(2).

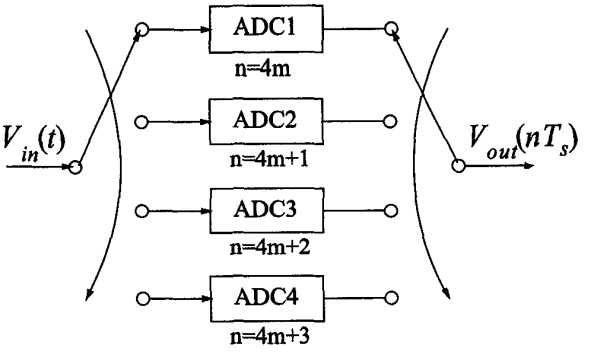


Fig.8: Four-channel time-interleaved ADC system.

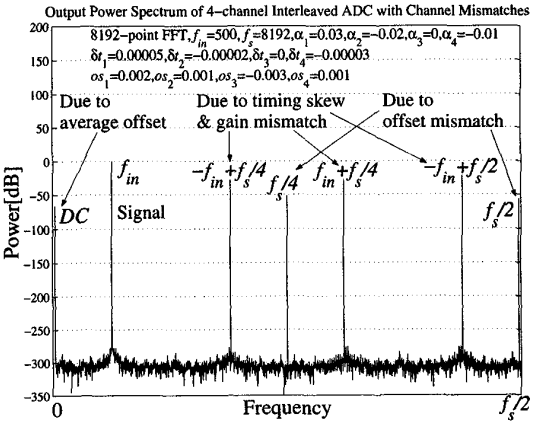


Fig.9: Simulation result of a four-channel time-interleaved ADC system with channel mismatches which verifies the correctness of our derived eq.(4).

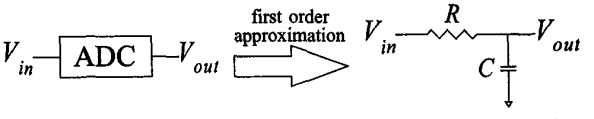


Fig.10: Approximation of an ADC to the first order system.