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A 6-bit 1.3-GS/s Ping-Pong Domino-SAR ADC in 55nm CMOS

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***Abstract*—This study presents a 6-bit domino successive approximation register (SAR) analog-to-digital converter (ADC). The proposed domino-SAR ADC architecture provides high-speed domino operation and the offset immunity of SAR ADCs. The ping-pong operation enacts a master clock sampling scheme to achieve a sampling rate of 1.3 GHz. A prototype ADC chip was fabricated using a 55-nm CMOS technology. The chip consumes a total power of 3.5 mW from a 1.2-V power supply. The measured peak SNDR and SFDR are 33 dB and 48 dB, respectively. The peak effective number of bits is 5.2 bits, equivalent to the figure of merit of 73 fJ/conversion step.**

***Index Terms*—Analog-to-digital converter (ADC), digital-to-analog converter (DAC), domino, ping-pong, successive-approximation register (SAR).**

I. Introduction

LOW-resolution and high-speed analog-to-digital converters (ADCs) are widely used in wireless communication systems, serial link transceivers, and digital oscilloscopes [1]–[7]. The flash ADC has the highest sampling rate of all ADC architectures [1], [2]. The circuit complexity and power consumption of a flash ADC grow exponentially as the number of bits increase. For example, there are $2^N - 1$ activated comparators for an N-bit flash ADC. To save more power, successive approximation register (SAR) ADCs contain superior energy efficiency and smaller footprints but suffer from slower operating speeds [3], [4].

To break the power-speed tradeoff, a 6-bit comparator asynchronous binary search (CABS) ADC was fabricated using a large comparator array (63 comparators); only six comparators were activated to cut down on the power consumption [5]. However, the input bandwidth of the CABS ADC was still limited because all comparators were connected to the analog input. The circuitry complexity of the CABS ADC increases rapidly with its resolution. In this study, the term "domino" is used for denoting a similar ADC architecture. To achieve sampling rates on the order of a few gigahertz, two 6-bit domino ADCs were fabricated using a 40-nm CMOS technology [6], [7]. Moreover, the domino ADC architecture was applied to implement coarse and fine ADCs in an 11-bit 250-MS/s two-step ADC [8]. These domino ADCs use their foreground calibration schemes to alleviate the performance degradation caused by the offset mismatch [6]–[8]. However, these offset calibration schemes require additional equipments and testing time. Furthermore, these foreground calibration schemes cannot track time-varying offset deviation.

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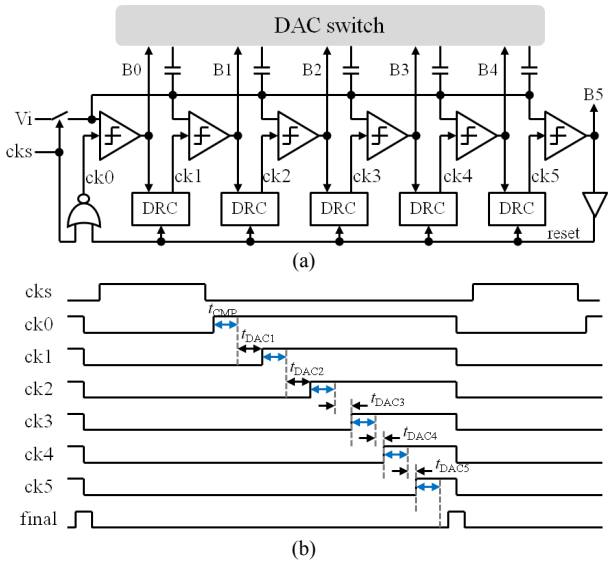

Fig. 1. (a) A prior domino ADC architecture and (b) its timing chart [6].

The study presents an alternative solution for decreasing the performance degradation caused by offset deviations among comparators in domino-based ADCs. In this study, the offset problem in domino ADCs and the speed limit in SAR ADCs were overcome by the proposed domino-SAR ADC architecture. The proposed ping-pong operation works in combination with the proposed adaptive sampler to provide a relatively long tracking time. This brief describes a conceptual 6-bit 1.3 GS/s ping-pong domino-SAR ADC in a 55 nm CMOS technology. Measurement results proved that the offset deviation can be tolerated by conducting a redundant SAR operation.

II. ADC Architecture

A. Domino ADC Architecture

Fig. 1a displays the 6-bit domino ADC presented in [6]. In contrast to a conventional single-comparator SAR ADC, six domino comparators perform individual bit conversions. During the input tracking period (*cks* is high), all comparator outputs are reset to low. When the input is sampled (*cks* goes

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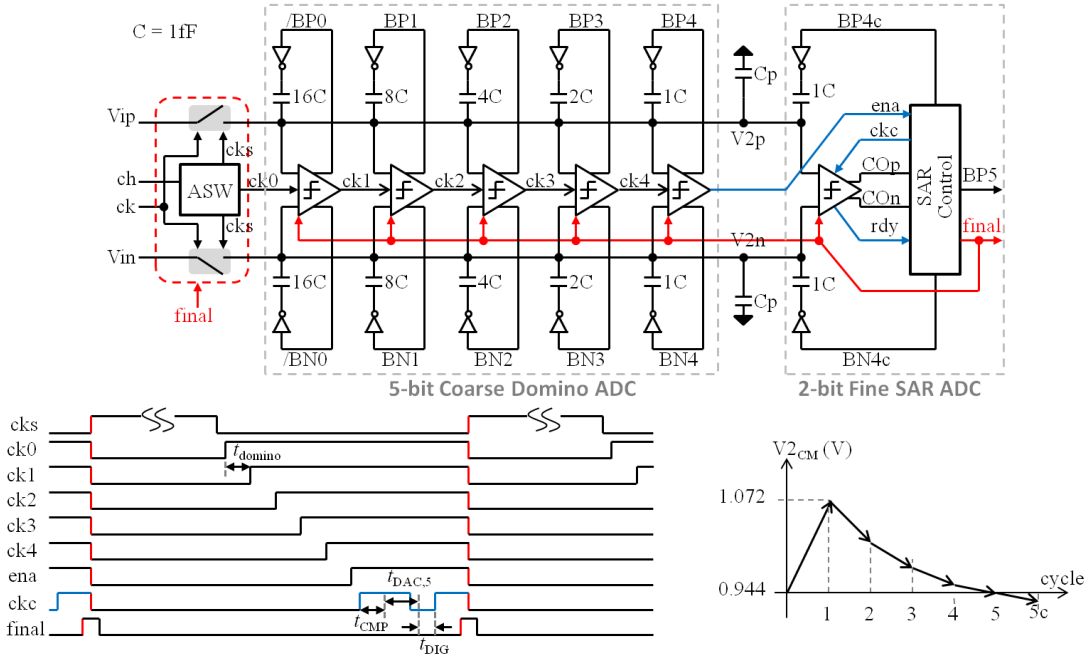

Fig. 2. Proposed domino SAR ADC architecture and its timing chart.

low), the most significant bit (MSB) comparison is firstly triggered (*ck0* goes high) to yield the output *B0*. The comparator output directly controls the MSB digital-to-analog (DAC) switch. Simultaneously, *B0* is passed to the first delay-and-reset circuit (DRC) to trigger the MSB comparison with a certain time delay. Like a falling line of dominos, the comparison is sequentially triggered from the MSB to the least significant bit (LSB) cycles. After *B5* has been obtained, the finish flag *final* goes high to reset all domino comparators. All comparator clock and output signals are reset to low.

As shown in Fig. 1a, the domino comparator acts as a 1-bit quantizer and data latch because it is not reused after the comparison has been completed. Therefore, the domino ADC is an optimal candidate for achieving higher sampling rates. The conversion time ($t_{CONV,SAR}$) of a 6-bit top-plate sampling SAR ADC [9] is represented as

$$t_{CONV,SAR} = 6 \cdot t_{CMP} + 5 \cdot \left(t_{DIG} + t_{DAC,1} \right) \quad (1)$$

where t_{CMP} is the average comparison delay; $t_{DAC,1}$ represents the MSB DAC settling time, which is the longest waiting time during the successive approximation (SA) process; t_{DIG} is the DAC control logic delay that is contributed by two dynamic flip-flops.

For domino ADCs, the delay between the present comparator output and the next comparator clock signal can be individually adjusted. Fig. 1b presents the timing chart of a 6-bit domino ADC. Each DRC has an individual delay for meeting the required DAC settling time during the SA process. The conversion time of the domino ADC ($t_{CONV,domino}$) is represented as

$$t_{CONV,domino} = 6 \cdot t_{CMP} + 5 \cdot t_{DAC,avg}, \quad (2)$$

where $t_{DAC,avg}$ is the average DAC settling time from MSB to LSB cycles. On the basis of (2) and without any logic delay on the DAC control path, the total conversion time of the domino ADC is shorter than that of the SAR ADC presented in [9].

The offset problem is observed in domino ADCs when more than one comparator is used. The comparator offset must be less than half LSB so that the resolution of the ADC is not affected. To meet this criterion, domino ADCs fabricated in [5]–[8] used foreground offset calibration schemes. In [5] and [8], two digital-tuning capacitor arrays were added to the output nodes of domino comparators. The additional loading capacitance slowed down the comparison or increased the power consumption of the ADCs. In [6], two current DACs were used to adjust the offset; however, this increased the power consumption. In [7], two variable MOS capacitors were controlled by two analog signals to compensate for the offset voltage. The analog MOS capacitance varied with changes in temperature.

B. Domino SAR ADC Architecture

To suppress the offset problem in domino ADCs, as shown in Fig. 2, the domino SAR ADC architecture is proposed without using any offset calibration scheme [10]. The proposed domino SAR ADC comprises an adaptive sampling switch (ASW), five domino comparators, a 5-bit C-DAC, and a 2-bit SAR ADC. After the first five domino comparisons, the domino-ready signal (*ena*) triggers the SAR operation to perform the final two comparisons. Finally, the SAR-ready signal (*final*) resets all comparators for the next conversion and triggers the ASW to perform the next input tracking. The detailed operation of the ASW is described in Section III-C. In generic configurations, an M-bit coarse domino ADC and an (N − M + 1)-bit fine SAR ADC can be used to implement an N-bit domino-SAR ADC to obtain various offset tolerance ranges. In this study, N is 6 and M is 5.

As shown in Fig. 2, the proposed domino SAR ADC can be viewed as a 6-bit subrange ADC comprising a 5-bit coarse domino ADC and a 2-bit fine SAR ADC. The comparator

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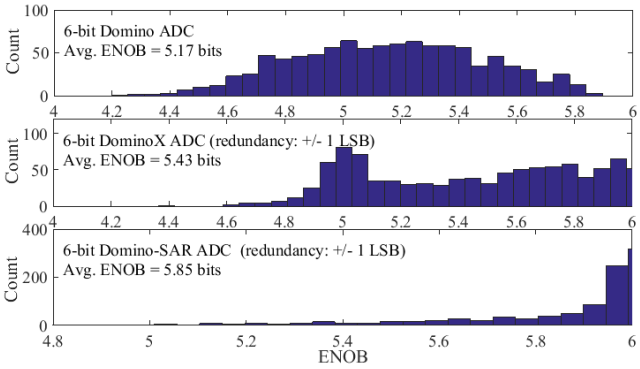

Fig. 3. ENOB degradation caused by the offset deviation among comparators for domino (top), dominoX (middle), and domino SAR (bottom) ADCs.

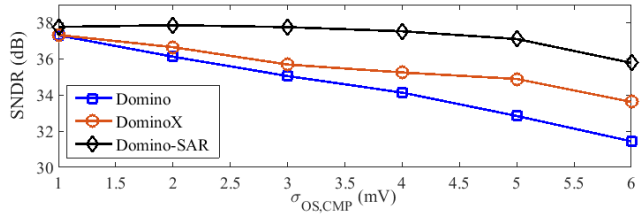

Fig. 4. Simulated average SNDR versus σ_{OS} for three ADCs.

offset in the domino ADC may contribute to errors if an offset mismatch exists between the domino and SAR ADCs. Because the final two comparisons are executed by the same comparator, the offset mismatch can be tolerated by using the over-range protection [3]. In this work, the redundancy provides ±1 LSB to tolerate the offset mismatch and possible DAC settling errors before the SAR conversion.

To maintain an effective number of bits (ENOB) greater than five, the standard deviation of the comparator offset ($\sigma_{OS,CMP}$) must be within 0.167 LSB. Here, the LSB voltage is 16 mV; therefore, $\sigma_{OS,CMP} < 2.67$ mV_{rms}. As described in Section III-A, after 1000 Monte Carlo simulation runs, the comparator offset was observed to be within ±15 mV ($\sigma_{OS,CMP}$ is 5 mV_{rms}). Fig. 3 displays the ENOB histograms of three 6-bit ADCs, a 6-bit domino ADC, a 6-bit domino ADC with 1-bit redundancy (dominoX), and the proposed domino SAR ADC, with σ_{OS} of 5 mV_{rms}. The average ENOBs of domino, dominoX, and domino SAR ADCs were 5.17, 5.43, and 5.85 bits, respectively. Considering the ENOB of five bits as the threshold level, the yields of domino, dominoX, and domino SAR ADCs were 72%, 90%, and 98.4%, respectively. The results shown in Fig. 3 reveal that the proposed domino SAR ADC can effectively improve the ENOB without using the offset calibration.

Fig. 4 shows the SNDR versus $\sigma_{OS,CMP}$ for three ADC architectures. The 6-bit domino ADC had the worst SNDR because the offset mismatch worsened the resolution. With a redundancy of ±1 LSB, the dominoX ADC can tolerate an offset mismatch before the redundant bit but cannot tolerate that after the redundant bit. The proposed domino SAR ADC had an optimal SNDR because only a small amount of offset mismatch was observed after the redundant bit comparison.

As shown in Fig. 2, the major drawback of the domino SAR ADC is the speed penalty since one redundant cycle is used. The total conversion time ($t_{CONV,domino-SAR}$) is represented as

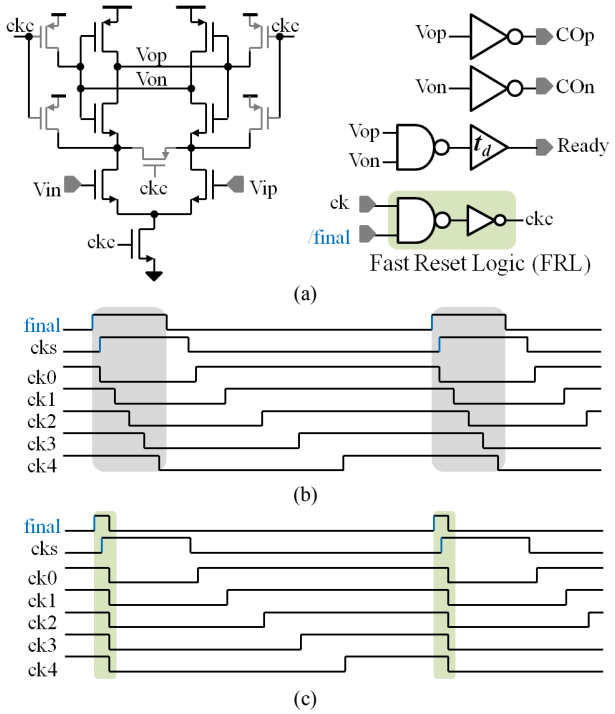

Fig. 5. (a) Proposed dynamic comparator with a variable delay (τ) and the fast reset logic (FRL) circuit, the reset profile, (b) without the FRL circuit, and (c) with the FRL circuit.

$$t_{CONV,domino-SAR} = t_{CONV,domino} + \left(t_{CMP} + t_{DAC,5} + t_{DIG}\right). \quad (3)$$

In comparison with the domino ADC, the additional time spent by the domino SAR ADC is $t_{CMP} + t_{DAC,5} + t_{DIG}$. An additional time of 0.2 ns is spent to tolerate the offset errors on the basis of the timing parameters in this work—t_{CMP} = 100 ps, t_{DIG} = 80 ps, and $t_{DAC,5}$ = 20 ps.

III. Circuit Implementation

A. Comparator Design

Fig. 5a depicts the core circuit of the domino and SAR comparators. All comparators have similar latch sense amplifier circuits [11]. Five transistors are used to reset the comparators and suppress the memory effect when *ckc* is low. The *Ready* signal is activated after the comparator outputs are generated. The domino ADC has an individual delay (t_d) between comparators. In this work, under typical conditions, the first three domino comparators had delays of 50, 40, and 30 ps, respectively. The delay of the other comparators was 20 ps.

For domino-based ADC architectures, the comparators are reset one by one. Fig. 5b shows the timing profile for a sequential comparator reset sequence. This individual reset reduces the available input tracking time because the bottom plates of capacitors are not reset appropriately. Therefore, this sequential reset profile limits the sampling accuracy for high-frequency input signals. To correct this drawback, a fast reset logic (FRL) circuit was employed to implement a concurrent reset profile. Fig. 5c displays the reset profile of the proposed FRL circuit. The circuit enables the allocation of a longer tracking time for maintaining a higher effective resolution bandwidth.

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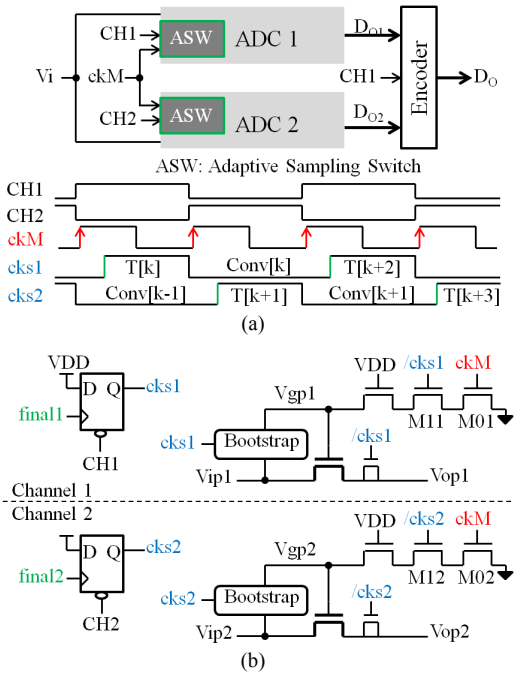

Fig. 6. (a) Proposed ping-pong ADC architecture and its operation and (b) the adaptive sampling switch with the master clock sampling scheme.

B. Reference Scaling C-DAC

Fig. 2 displays two binary-weighted (5 + 1)-bit C-DACs. The capacitor bank is {16*C*, 8*C*, 4*C*, 2*C*, *C*, *C*}, with one redundant capacitor. The unit capacitance of 1 fF was implemented using the fringe capacitor structure. The full-scale input range was from 0.688 (V_{RB}) to 1.2 V (V_{REF}), equivalent to one LSB of 16 mV. To avoid the use of two reference buffers for V_{REF} and V_{RB}, a reference scaling scheme is proposed that utilizes only one V_{REF} reference buffer with a well-designed parasitic capacitor C_P. The equivalent full-scale input voltage is represented as

$$V_{in,FS} = \frac{32C}{32C + C_P} \times V_{REF}, \quad (4)$$

where C_P is the lumped capacitance from *V2* to the ground. To obtain $V_{in,FS}$ of 512 mV, C_P can be set to have a capacitance of 43 fF for V_{REF} of 1.2 V. C_P comprises all the parasitic and dummy capacitances. The dummy capacitors are placed such that the target capacitance is obtained by using the post-layout simulation results. The inaccuracy of C_P only introduces a small gain error that can be corrected by post-processing. The total sampling capacitance of 75 fF contains a negligible thermal noise power of $(0.33\ mV_{rms})^2$. The capacitor mismatch of the capacitor arrays (the effective total capacitance is 32 fF) does not cause severe damage on the 6-bit linearity.

To maintain a short comparison delay, the input common-mode voltage of the comparators should be maintained at high voltage levels [11]. In this work, an up-then-down DAC switching scheme was used to maintain the common-mode voltage higher than 0.9 V [12]. As shown in Fig. 2, during the input tracking period, the bottom plates of the MSB capacitors were connected to the ground, and the bottom plates of other capacitors were connected to V_{REF}. Fig. 2 presents the common-mode voltage variation during the SA process. Here, the common-mode voltage variation of 128 mV contributed a negligible dynamic offset voltage to the proposed 6-bit ADC.

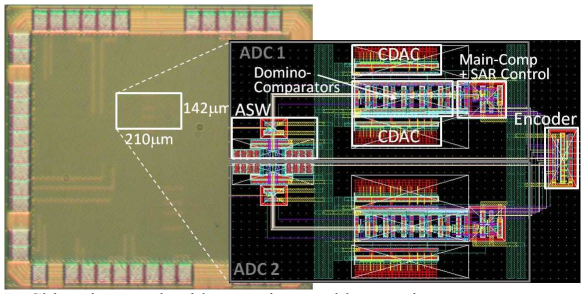

Fig. 7. Chip micrograph with super-imposed layout view.

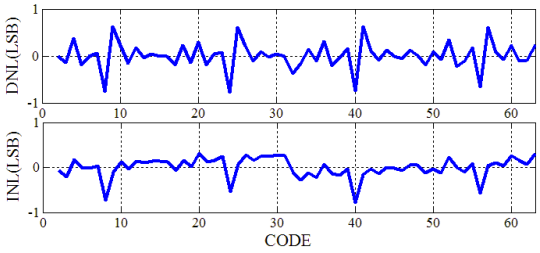

Fig. 8. Measured differential and integral nonlinearity plots.

C. Ping-Pong Operation and Adaptive Sampling

Fig. 6a presents the block diagram of the proposed 6-bit 1.3 GS/s ADC. The ADC was clocked by *ckM* with a 50% duty cycle. The ADC comprised two domino SAR channel ADCs (ADC1 and ADC2) and an encoder. These channel ADCs were interleaved by *CH1* and *CH2*. The ping-pong operation had two features—one was the double sampling rate and the other was the availability of a long conversion time. Offset, gain, and skew errors between channel ADCs must be suppressed. In general, offset and gain errors can be corrected by post-processing. Skew error can be mitigated by using a similar master sampling operation [13]. As shown in Fig. 6a, the rising edge of *ckM* determined the sampling instant for both channel ADCs. The circuit was well designed and laid out to maintain a small skew caused by the mismatch between M01 and M02.

Fig. 6b displays the proposed adaptive sampler with a dynamic flip-flop. During the channel ADC conversion, the *final* signal goes high to enable the tracking of the next input (*cks* goes high). Even if a metastable condition occurs, the channel ADC operates appropriately but requires a relatively long conversion time. Only a short tracking time is introduced for the next input. In addition, the conversion time varies with the process, voltage, and temperature (PVT) variations. Therefore, if the input frequencies are not high, both metastability and PVT variations can be conditionally tolerated without compromising the accuracy of the input tracking.

IV. Measurement Results

Fig. 7 shows the chip micrograph of the ping-pong domino SAR ADC fabricated using a 55-nm CMOS technology. This ADC prototype occupied an active area of 0.03 mm^2. At 1.3 GS/s, the ADC consumed a total power of 3.5 mW from a 1.2-V power supply. The analog, digital, and reference powers were 1.95, 1.16, and 0.39 mW, respectively. Fig. 8 depicts the

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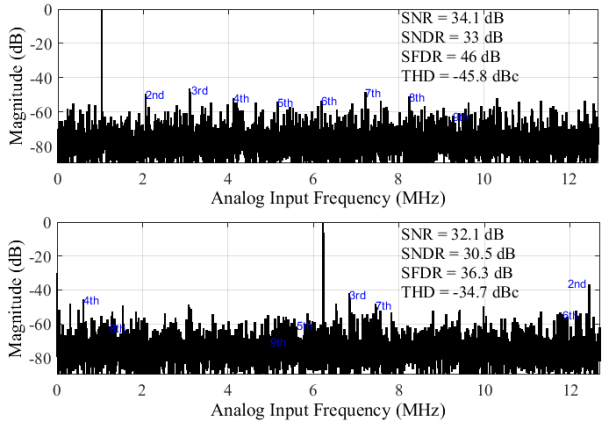

Fig. 9. Measured spectra for input frequencies of 1 MHz (top) and 631 MHz (bottom) at 1.3 GS/s (8192-pt, down-sampled by 51).

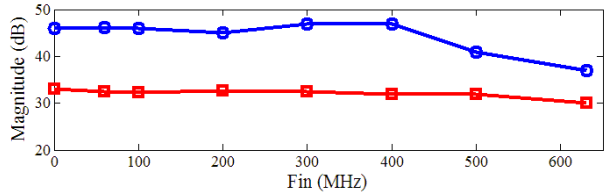

Fig. 10. Measured SNDR and SFDR versus input frequencies at 1.3 GS/s.

measured differential nonlinearity (DNL) and integral nonlinearity (INL) plots. The peak DNL and INL were −0.78/+0.62 LSB and −0.85/+0.32 LSB, respectively. The third comparator offset dominated the DNL errors.

Fig. 9 presents spectra for input frequencies of 1 and 631 MHz at 1.3 GS/s. With an input frequency of 1 MHz, the measured SNDR and SFDR were 33 and 48 dB, respectively. The total harmonic distortion (THD) was −45.8 dBc. With an input frequency of 631 MHz, the measured SNDR and SFDR were 30.5 and 36 dB, respectively; the THD was −34.7 dBc. Fig. 10 displays the measured SNDR and SFDR versus input frequencies. The SNDR was more than 30 dB for the first Nyquist band. The peak and Nyquist Walden figures of merit (FOMs) were 73 and 99 fJ/conversion-step, respectively.

Table I summarizes the performance of the proposed ADC and compares its performance with those of prior 6-bit ADCs. Compared with the ADCs in [3] and [6], the proposed ADC provided superior energy efficiency. Compared to the ADCs in [4] and [7], the proposed ADC provided a faster operating speed by using a slower process node; however, a worse FOM was obtained.

V. Conclusion

This study proposed a 6-bit 1.3 GS/s ping-pong domino SAR ADC fabricated with a 55-nm CMOS technology. The proposed domino SAR ADC architecture improved the performance degradation caused by the comparator offset. The ping-pong ADC operation further doubled the sampling rate by using a master clock sampling scheme. The prototype ADC achieved a Nyquist SNDR of 30.5 dB while consuming 3.5 mW power from a 1.2-V power supply. The conceptual domino SAR ADC was fabricated to achieve a sampling rate of 1.3 GHz without using any offset calibration scheme.

TABLE I
Performance Summary and Comparison with Prior 6-bit ADCs

Parameter	This work	[3]	[4]	[6]	[7]
Architecture	Domino-SAR	SAR	SAR	Domino	Domino
Process(nm)	55	40	40	40	40
Sample rate (GHz)	1.3	1.2	1	1.25	0.7
Power (mW)	3.5	5.3	1.26	6.08	0.95
Supply (V)	1.2	1.2	0.9	1	1.2
Peak SNDR (dB)	33	34.4	35.1	30.5	35.1
Nyq. SNDR (dB)	30.5	31.2	34.6	26.8	34.8
Peak SFDR (dB)	48	46	NA	42	49.5
Nyq. SFDR (dB)	36	40	50	39	47.8
FOM_{peak} (fJ/c.-s.)	73	124	27.1	178	30
FOM_{Nyq} (fJ/c.-s.)	99	180	28.7	272	30
Area (mm^2)	0.03	0.009	0.00058	0.014	0.004
Calibration	No	No	No	Yes	Yes

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