This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2017.2756036, IEEE Transactions on Circuits and Systems II: Express Briefs

A 1.4-mW 10-bit 150-MS/s SAR ADC With Nonbinary Split Capacitive DAC in 65 nm CMOS

Dengquan Li, Zhangming Zhu, Ruixue Ding and Yintang Yang

***Abstract*—This brief presents a high-speed successive approximation register (SAR) analog-to-digital converter (ADC) with nonbinary searching technique. By inserting redundancy in the first five decision steps, the digital-to-analog converter (DAC) settling errors can be tolerated and settling time can thus be reduced. In addition, split capacitor technology has also been adopted to further boost the conversion speed. With split switching method, no common mode voltage is needed in DAC reset phase and dynamic offset can be removed as well. Full adder based encoder is employed to convert the raw 11-bit to 10-bit binary codes, showing less power penalty. The prototype ADC fabricated in 65 nm CMOS achieves 51.1 dB SNDR and 62.3 dB SFDR at 150-MS/s sampling rate. It consumes 1.4 mW, resulting in a Walden figure of merit (FoM) of 31.8 fJ/conversion step.**

***Index Terms*—Analog-to-digital converter, successive approximation register, nonbinary, split capacitors.**

I. Introduction

Successive approximation register (SAR) ADCs are often used in low-speed applications due to their low-power and sequential operation feature. However, thanks to the advanced nanometer CMOS technology and innovative architectures, high-speed SAR ADC design becomes a reality. Asynchronous SAR conversion reduces the wasted time of each comparison cycle and avoids the use of external high frequency clock [1]. Multi-bit per cycle SAR ADC is also an effective way to increase the speed by resolving 2 or more bits in one conversion cycle, while at the cost of complicated offset calibration and increased power consumption and area [2]. A loop-unrolled architecture was proposed in [3], which employs 6 comparators for a 6-bit SAR ADC. Each comparison result can be directly stored and used for DAC settling, removing the comparator reset time. Nevertheless, nonlinearity due to offset mismatch makes this architecture not suitable for high resolution ADCs. Two-step SAR ADC in [4] utilizes the partial interleaving concept to resolve the residue voltage of the first stage. But the inter-stage gain could be nonideal due to undesired parasitics and charge sharing.

Recently, non-binary algorithm, which relaxes the DAC settling requirement and reduces the settling time without DAC area penalty, has been studied [5]-[7]. This method needs one or two more conversion steps to get N+1 or N+2 bits, where N is the ADC resolution, absorbing the DAC settling errors in the first few steps and allowing incomplete DAC settling. Thus, the DAC settling time can be significantly reduced. Although more steps are required, the general conversion speed is boosted especially for SAR ADC with higher resolution. In this work, split DAC array is employed to further increase the conversion speed. As a result, there is no common-mode voltage (V_{cm}) variation issue and only static offset appears in comparator. The static offset does not affect the ADC linearity and can be easily diminished in digital domain. In addition, the conversion speed and linearity characteristic of non-binary split and binary split switching have been analyzed and compared. Furthermore, other circuit implementation methods, including comparator, DAC floorplan, SAR logic and encoder, are proposed for high speed and better robustness. A prototype ADC is implemented in 65 nm CMOS. It achieves 51.1 dB SNDR and 62.3 dB SFDR at a sampling rate of 150 MS/s with Nyquist input, while consuming 1.4 mW power from 1.2 V supply and occupying an active area of 0.079 mm^2.

This brief is organized as follows. In Sec. II, the nonbinary split architecture is described. The circuit implementations are presented in Sec. III. The measurement results are shown in Sec. IV. And the conclusion is drawn in Sec. V.

II. Proposed SAR ADC Architecture

A. Nonbinary searching algorithm

In a conventional binary searching way, the settling error in one decision step should be less than LSB/2 to ensure accuracy. While in a nonbinary searching scheme, the settling condition can be relaxed to q(k)×LSB, where q(k) is the redundancy in k-th step [6]. As a result, the settling can be faster. The settling time is expressed as:

$$t_i \geq RC_i \ln \frac{p(k)}{q(k)} \tag{1}$$

where R is the wire resistance, C_i is the capacitor to be charged (or discharged), i=k+1, and p(k) is the difference between two adjacent bit decision threshold value. The value of q(k) should satisfy the following equation [5]

$$2^X - 2^N = \sum_{k=1}^{X-1} 2^k q(k) \tag{2}$$

where X is the total steps for SAR conversion and N is the ADC resolution. When we set proper value of q(k), the redundancy can be added into the specific step based on the following relation:

This work was supported by the National Natural Science Foundation of China (61625403, 61674118).

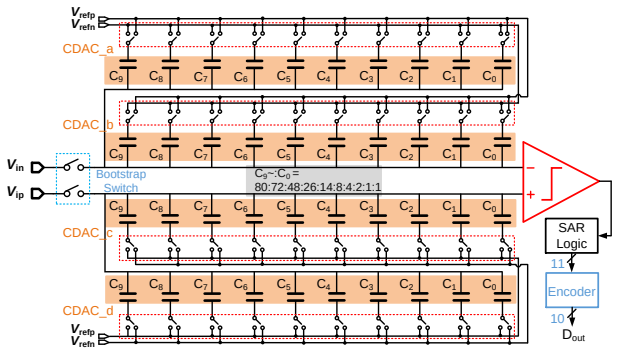
The authors are with the School of Microelectronics, Xidian University, Xi'an 710071, China (e-mail: zmyh@263.net; zhangmingzhu@xidian.edu.cn).

1549-7747 (c) 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

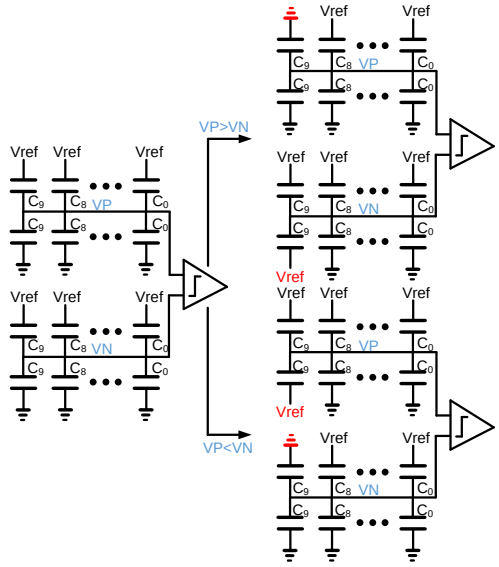
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2017.2756036, IEEE Transactions on Circuits and Systems II: Express Briefs

TABLE I
THE VALUES OF p(k) AND q(k)

k	1	2	3	4	5	6	7	8	9	10	11
p(k)	512	160	144	96	52	28	16	8	4	2	1
q(k)	192	64	16	8	4	0	0	0	0	0	0



(a)



(b)

Fig. 1. (a) Proposed nonbinary SAR ADC with split DAC array and (b) switching example for the first decision step.

$$q(\mathrm{k}) = 1 + \sum_{i=k+2}^{X} p(\mathrm{i}) - p(\mathrm{k}+1) \tag{3}$$

If an error occurs at k-th step, its next step will move to the wrong direction, so the sum of the follow-on step sizes should exceed the current step size. This is the basic idea of nonbinary searching and a simple explanation for (3).

More redundancy may offer larger error tolerance, while at the cost of complexity and hardware penalty. In this work, 11 steps are adopted and the redundancies for first two MSBs are 192 and 64 LSB respectively. The value of p(k) can then be calculated as:

$$p(\mathrm{k}+1) = 2^{X-k-1} - q(\mathrm{k}) - \sum_{i=k+1}^{X-1} 2^{i-k-1} q(\mathrm{i}) \tag{4}$$

The corresponding values of p(k) and q(k) in this work is listed in Table I.

B. *Proposed SAR ADC architecture*

The proposed SAR ADC architecture is shown in Fig. 1(a).

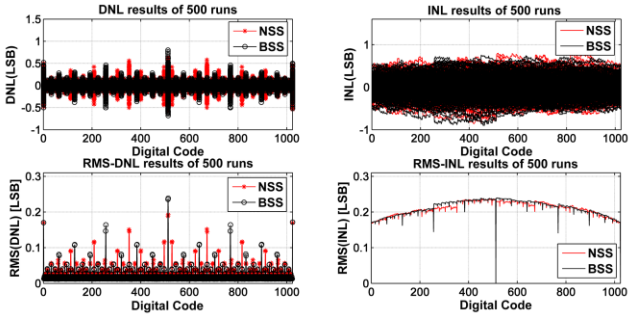


Fig. 2. Behavioral simulation comparing the linearity of BSS and NSS 10-b SAR ADC.

It consists of 4 capacitive DACs, a differential sampling network, a dynamic comparator, SAR logic, and an encoder. The asynchronous clock is generated internal to ensure the fast SAR conversion. Bootstrapped switches are adopted in the front end for high sampling linearity. The values of p(k) in Table I can be used to design the DAC array. In this work, capacitors are split to two capacitors with the same capacitance to further decrease the charging (or discharging) time according to (1). In addition, by doing this, no V_{cm} voltage is needed in DAC reset phase, avoiding the large switches to transmit V_{cm}. The nonbinary capacitors used in the sub DAC are [$80C_0$, $72C_0$, $48C_0$, $26C_0$, $14C_0$, $8C_0$, $4C_0$, $2C_0$, C_0, C_0].

To cope with the unstable common mode issue, [8] proposed a bidirectional single-side switching that reduce the largest V_{cm} by 50% compared to monotonic switching. In [9], the first two bits are involved in V_{cm}-based switching and then monotonic switching is performed for the following steps, resulting in a 75% reduction of V_{cm} variation. But the usage of external common mode voltage during DAC reset could be an issue to these methods, because the switches need to be large and thus leading to an increased area and driving power.

In this work, the split capacitor switching [10] allows V_{cm} stable. The switches change symmetrically from MSB to LSB+1, while for LSB conversion monotonic switching is adopted. So the variation of V_{cm} is negligible due to the small size of LSB capacitor. The benefit of having constant V_{cm} is reduced dynamic offset, which induces errors and causes nonlinearity. The transition for the first conversion step as an example is illustrated in Fig. 1 (b).

C. *Linearity and settling speed analysis*

In binary searching scheme, any settling error or comparison error has no way to calibrate, resulting in nonlinearity. While in the nonbinary searching scheme, redundancy allows overlapped conversion curves, i.e. one analog voltage may map to more than one digital code. If the mismatch caused error is within the redundancy range, the decision error in this bit can be corrected in the following steps. In order to compare the impact of capacitor mismatch on conventional binary split switching (BSS) and non-binary split switching (NSS), a Matlab model has been created. The capacitors are set to be the ideal value plus Gaussian random variables. Monte Carlo simulations with 500 runs are then performed. The results show that NSS has better linearity than BSS. Fig. 2 shows the results of standard deviation is set as 1%, the maximum DNL/INL of

1549-7747 (c) 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2017.2756036, IEEE Transactions on Circuits and Systems II: Express Briefs

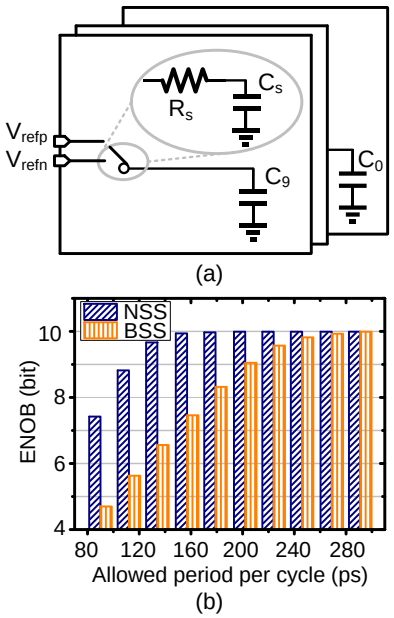


Fig. 3. (a) Behavioral model when charging (or discharging) the n-th capacitor in DAC and (b) the allowed period per cycle vs ENOB with BSS and NSS.

BSS and NSS are 0.81/-0.90 LSB and 0.64/-0.82 LSB, respectively. And the RMS-DNL/INL of BSS and NSS are 0.24/0.24 LSB and 0.19/0.23 LSB, respectively. The RMS non-linearity in Fig. 2 is defined as sqrt(mean($DNL_i/INL_i)^2$)). Note that with larger mismatch factor, the improvement is larger.

A behavioral model has been designed to verify the effectiveness of speed improvement of redundancy. The MOS switch is modeled as R_s and C_s, and the capacitor to be charged (or discharged) is C_n (n=0, 1,…, 9), shown in Fig. 3 (a). R_s is set as 100 Ohm, and C_0 in DAC is 2.8 fF. All C_s in parallel are modeled as a parasitic with 10 fF. Using the first-order RC circuit approximation, the DAC voltage at t_n can be calculated as:

$$V_n = V_{n-1} + V_{dn}\left(1 - e^{-\frac{t_n - t_0}{R_s(C_n + C_s)}}\right) \quad (5)$$

where V_{dn} is the voltage difference between n-th and (n-1)-th step, and t_0 is the time when n-th capacitor begins charging. Swiping the allowed period per cycle, i.e. (t_n-t_0), the ENOBs of the BSS method and proposed NSS method are shown in Fig. 3 (b). The allowed DAC settling time per cycle for BSS is 291 ps and for NSS is 179 ps, respectively. As BSS needs 9 DAC settling periods and NSS needs 10 DAC settling periods (with 1-b redundancy) for a 10-bit SAR ADC, the total settling time for BSS is 2619 ps (=$9\tau_{BSS}$) and for NSS is 1790 ps (=$10\tau_{NSS}$). This shows that NSS has a 31.6% DAC settling speed improvement over BSS.

III. Circuit Implementations

A. Dynamic comparator

A high speed comparator with low power and low noise is crucial for SAR ADC design. In this work, a two stage dynamic comparator composed of preamplifier and latch is adopted, as shown in Fig. 4 (a). When Clk is low, the comparator goes into

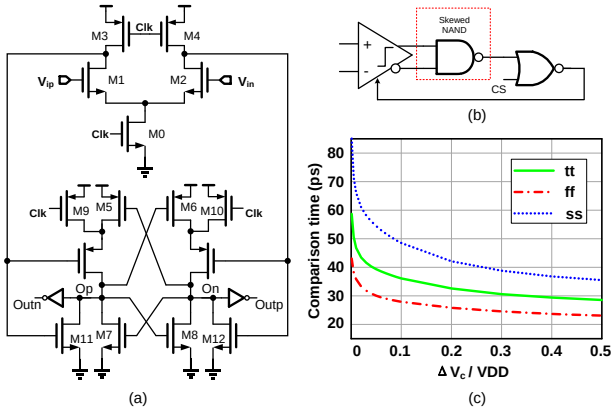


Fig. 4. (a) Schematic of the dynamic comparator. (b) Asynchronous clock generator. (c) The input voltage difference vs comparison time.

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	36	36	36	24	24	13	7	4	4	7	13	24	24	36	36	36	D	D	D	D	D	D
D	40	40	40	40	36	36	36	24	24	13	D	0.5	0.5	D	13	24	24	36	36	36	40	40	40	40	D	
D	40	40	40	40	36	36	36	24	24	13	7	1	D	7	13	24	24	36	36	36	40	40	40	40	D	
D	40	40	40	40	36	36	36	24	24	13	D	0.5	0.5	D	13	24	24	36	36	36	40	40	40	40	D	
D	40	40	40	40	36	36	36	24	24	13	7	4	4	7	13	24	24	36	36	36	40	40	40	40	D	
D	40	40	40	40	36	36	36	24	24	13	13	2	2	7	13	24	24	36	36	36	40	40	40	40	D	
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Fig. 5. Floorplan of the sub CDAC.

reset mode and the outputs (Outn and Outp) equal high. When Clk turns to high, the outputs of preamplifier are discharged to ground with different speed dependent on the input voltages V_{ip} and V_{in}, and then latched by M5-M8. Asynchronous SAR ADCs encounter metastability issue, which results in sparkle codes. By allocating a threshold skewed NAND gate [1] to achieve faster detection of Outp/Outn going low, shown in Fig. 4 (b), the sparkle code rate (defined as the code error larger than 4 LSB) in this work is reduced to 10^{-6}. Fig. 4 (c) illustrates the simulation results of the relationship between input voltage difference (ΔV_c) and comparison time under process corners.

B. Floorplan of DAC

Compared to metal-oxide-metal (MOM) capacitors, metal-insulator-metal (MIM) capacitors have less parasitic capacitance and better matching. The capacitive DAC is implemented with MIM capacitors in this work, where the unit size is 5.6 fF in the 65-nm CMOS technology. As this value is completely satisfied for a 10-bit SAR ADC considering the thermal noise and matching requirements, two unit capacitors are cascaded as C_0. So the unit capacitor used in this work is 2.8 fF and the total capacitance is 1.43 pF in one side of the DAC. The routing parasitic capacitors may become the bottleneck for the DAC accuracy. In this work, segmented common-centroid layout technique is employed to overcome this issue. Fig. 5 shows the floorplan of the CDAC_a, which has 208 unit capacitors in total. The digital in Fig. 5 indicates the corresponding capacitors and D represents the dummy cell. The 77 dummy cells in CDAC_a are placed for better matching and are connected to ground. Two types of guard rings are also placed around the CDAC to isolate noise.

1549-7747 (c) 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2017.2756036, IEEE Transactions on Circuits and Systems II: Express Briefs

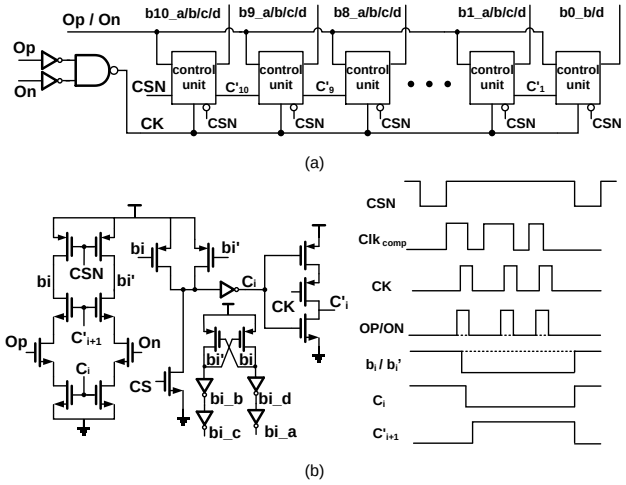


Fig. 6. (a) SAR logic controller and (b) schematic of the dynamic register.

Wight	512	256	128	64	32	16	8	4	2	1
					B6					
				B4	B5		B8			
		B2		B3	B4	B7	B5			
+		B1	B3	B1	B2	B5	B4	B9	B10	B11
Binary code	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10

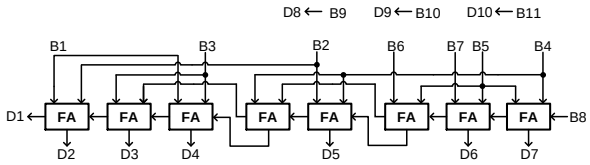


Fig. 7. The encoding function and the schematic of the encoder.

C. SAR logic controller

A series of registers are cascaded to implement the successive approximation operation, shown in Fig. 6 (a). The dynamic register is required to store the comparator outputs and control the capacitive DAC at the same time. For the conventional way, D-flip-flops are used to achieve this goal, resulting in the critical path delay as $2t_{dq}$, where t_{dq} is the delay from the rising clock edge to the valid output of a DFF. While in this work, dynamic registers are adopted, which can be directly triggered by the comparator output. The schematic and timing diagram of the dynamic register is shown in Fig. 6 (b). CSN is the reverse of the sampling signal, which is generated through on-chip dividers and NAND gates. This signal is used for all registers to reset the outputs to their initial states. During the sampling phase, both bi and bi' are charged to VDD. When comparison completes, the results are captured and stored at b_i/b_i'. Meanwhile, b_{i_a}/ b_{i_b}/ b_{i_c}/ b_{i_d} are generated to control the DAC switches. When b_i/b_i' is discharged to low, C_i is discharged to turn off the current bit register. After C_i and CK goes to low, C_i' is triggered to enable the next bit register. Note that low-threshold-voltage (LVT) devices are adopted to further increase their speed.

D. Encoder

The encoder should convert the 11-bit nonbinary codes to 10-bit binary codes. Fig. 7 shows the encoding function and the schematic of the corresponding encoder, which consists of 8 full adders. In [11], additional capacitors are added in the DAC to remove settling errors, leading to overflow of the digital output. As shown in Table I, there is no such issue in the proposed architecture due to the sum of p(k) is 2^{10}. Therefore, the complexity and the area of the encoder in this work could be reduced. Note that the standard cell of full adders are provided by the foundry and can be directly adopted in circuit design, making the layout and simulation more convenient.

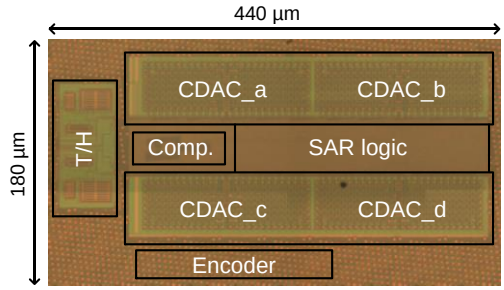


Fig. 8. Chip micrograph.

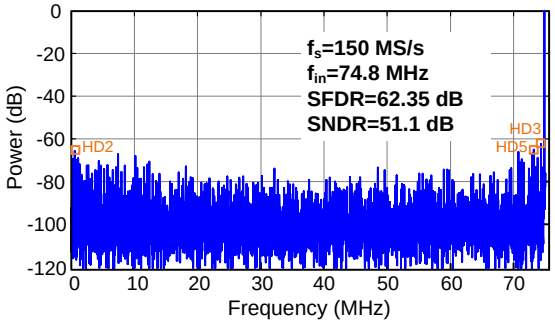


Fig. 9. Measured 16384-point FFT spectrum with 150 MS/s sampling rate at 74.8 MHz input frequency.

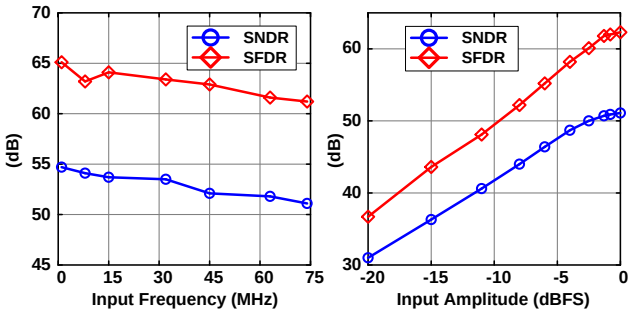


Fig. 10. SNDR and SFDR vs input frequency and amplitude.

IV. Measurement Results

The prototype ADC is fabricated in a 65 nm CMOS process and occupies an active area of 0.079mm^2, as shown in Fig. 8. There are 4 CDACs in total to implement nonbinary split searching scheme. By locating the SAR logics between the differential CDACs, the routing wires can be minimized and the paths for CDAC control signals are identical. The raw 11-bit digital codes travel downwards to encoder for converting 10-bit binary codes. No decimation is adopted in this work and the outputs are driven by LVDS transmitter.

1549-7747 (c) 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2017.2756036, IEEE Transactions on Circuits and Systems II: Express Briefs

TABLE II
PERFORMANCE COMPARISON

Reference	[13]	[14]	[15]	[16]	[12]	**This work**
Architecture	SAR	TI-SAR	SAR	SAR	Pipe-SAR	**SAR**
Technology (nm)	65	65	28	90	65	**65**
Resolution (bit)	10	10	10	10	12	**10**
Sampling rate (MS/s)	220	170	240	160	180	**150**
Supply voltage (V)	1.2	1	1	1	1.2	**1.2**
SNDR (dB) @ Nyquist	51.7	53.2	53	53	60.9	**51.1**
Power (mW)	4.3	2.3	0.68	1.97	6	**1.4**
Area (mm^2)	0.015	0.104	0.003	0.11	0.068	**0.079**
FoM @ Nyquist (fJ/Conv.-step)	63	36.4	7.8	33.5	36.7	**31.8**

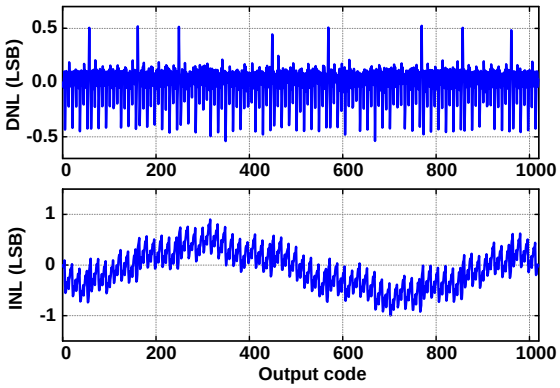


Fig. 11. Measured static performance.

Fig. 9 shows the measured FFT spectrum with 150-MS/s sampling rate, and a 2.1 V_{pp} 74.8 MHz sinusoidal input signal. The measured SNDR and SFDR are 51.1 dB and 62.3 dB, respectively. The third harmonic tone limits the SFDR, which is suspected due to the inadequate bandwidth of the sampling switches. Furthermore, the second harmonic is also considerable large, most likely introduced by the unbalanced routing wires of the differential input. Fig. 10 plots the measured SNDR and SFDR for various input frequencies and amplitude with 150-MS/s sampling frequency. All the measurements are performed under the supply voltage of 1.2 V. The total power consumption is 1.4 mW and the Walden figure-of-merit (FoM) is 31.8 fJ/conversion step. Forty-eight percent of the power is consumed by digital blocks including SAR logics and encoder, and fifty-two percent by the analog blocks including sampling switches, comparator and references. Fig. 11 shows the measured DNL and INL, which are within -0.54/0.52 LSB and -1/0.9 LSB, respectively. Table II compares this work to some previous designs with similar resolution and sampling rate, showing this prototype achieves a comparable FoM to the state-of-the-art.

One possible way to improve the FoM is to use smaller unit capacitor if the matching specification is relaxed. This reduces both the DAC switching energy and DAC settling time. Another way is to increase the sampling time, since bandwidth of sampling switches could become a limiting factor for a high speed SAR ADC.

V. CONCLUSION

In this brief, a high-speed SAR ADC with nonbinary split capacitive DAC array has been presented. With redundancy in first 5 MSB decision, the DAC settling errors can be tolerated and settling time can be reduced. By the use of a simple encoder which only consists of 8 full adders, the raw 11-bit codes can be easily converted to 10-bit binary codes. The prototype achieves 31.8 fJ/conversion step of FoM and occupies an active area of 0.079 mm^2. It is suitable to be time-interleaved for some higher speed applications.

REFERENCES

[1] S. Chen and R. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669-2680, Dec. 2006.

[2] C.-H. Chan *et al.*, "A 5.5mW 6b 5GS/s 4×interleaved 3b/cycle SAR ADC in 65nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 466-467, Feb. 2015.

[3] L. Chen *et al.*, "A 0.95-mW 6-b 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 3, pp. 244-248, Mar. 2017.

[4] H. Huang *et al.*, "A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer," in *IEEE Asian Solid-State Circuits Conf. (ASSCC)*, pp. 1-4, Nov. 2015.

[5] T. Ogawa *et al.*, "SAR ADC algorithm with redundancy," in *Proc. IEEE Asia Pacific Conf. Circuits and Syst. (APCCAS)*, pp. 268-271, 2008.

[6] Y. Kurisu *et al.*, "A successive approximation A/D converter using generalized non-binary algorithm," in *Proc. IEEE 43rd Int. Sym. Multiple-Valued Logic (ISMVL)*, pp. 152-157, 2013.

[7] D. Zhang and A. Alvandpour, "A 12.5-ENOB 10-kS/s redundant SAR ADC in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 3, pp. 244-248, Mar. 2016.

[8] L. Chen *et al.*, "A 24-µW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," *IEEE ESSCIRC*, pp. 219-222, Sep. 2014.

[9] D. Xing *et al.*, "Seven-bit 700-MS/s four-way time-interleaved SAR ADC with partial Vcm-based switching," *IEEE Trans. VLSI Syst.*, vol. 25, no. 3, pp. 1168-1172, Mar. 2017.

[10] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 739-747, Apr. 2007.

[11] C.C. Liu *et al.*, "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," *IEEE ISSCC Dig. Tech. Papers*, pp. 386-387, Feb. 2010.

[12] J. Zhong, *et al.*, "A 12b 180MS/s 0.068mm2 pipelined-SAR ADC with merged-residue DAC for noise reduction," *IEEE ESSCIRC*, pp. 169-172, Sep. 2016.

[13] R. Vitek *et al.*, "A 0.015 mm2 63 fJ/conversion-step 10-bit 220MS/s SAR ADC with 1.5b/step redundancy and digital metastability correction," in *Proc. IEEE CICC*, pp. 1-4, 2012.

[14] S. –S. Wong *et al.*, "A 2.3 mW 10-bit 170 MS/s two-step binary-search assisted time-interleaved SAR ADC," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1783-1794, Aug. 2013.

[15] J. -H. Tsai *et al.*, "A 0.003 mm2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1382-1398, Jun. 2015.

[16] C. H. Lee *et al.*, "A 2.5-bit/cycle 10-bit 160-MS/s SAR ADC in 90-nm CMOS process," in *Proc. IEEE Symp. On VLSI Design, Automation, and Test (VLSI-DAT)*, pp. 1-4, Apr. 2016.

1549-7747 (c) 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.