20.7 A 110dB Ternary PWM Current-Mode Audio DAC with Monolithic 2Vrms Driver

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Increased integration in entertainment systems is driven by continuous demand for lower total cost. This pushes more processing circuitry into digital SOCs. However, there persists a need in many systems for large voltage swing signals, conflicting with the trend toward lower digital voltage supplies. This design implements a stereo DAC for digital audio that incorporates a single-ended 2Vrms output drive. The IC is fabricated in a standard 0.35µm/3.3V/70Å gate process with a 3µm/18V/450Å gate module.

The chip block diagram is shown in Fig. 20.7.1. Input data is at 24-bit resolution, with 48/96/192kHz sample rates. The interpolation filter engine performs volume control, digital deemphasis, and up to three stages of 2x interpolation (for 48kHz input). Data is provided to a multibit delta-sigma modulator (DSM) at 6.144MHz (128Fs) after a 16x sample-and-hold. The DSM quantizer output is ternary PWM encoded and converted to analog by 4 parallel time-interleaved 2x8-tap semidigital FIR current source DACs operating at 12.288MHz. A class-AB amplifier with low-pass filter converts the final current signal to an output voltage.

The DSM is a fifth-order feedforward topology with two in-band resonator loops (Fig. 20.7.2). PWM encoding of the quantizer output minimizes the effects of intersymbol interference (ISI) in the continuous-time current source DAC. Predistortion is used in the DSM to compensate for nonlinearities introduced by PWM encoding [1].

For small output voltage step size and increased tolerance to jitter, a 64-element DAC was chosen. A brute-force implementation would use a 6-bit quantizer DSM, requiring large dynamic element matching hardware, and problems with ISI would persist. Alternately, the output data word may be PWM encoded at a high clock rate [2], but the required PWM clock for this case would be 48kHz*128*64 = 393MHz. In this design, a 4-bit quantizer is used in the DSM, and the quantizer outputs are interleaved in time 1:4. Each interleaved output is two-bit PWM encoded and passed through two 8-tap current-mode FIR filters [3]; the FIRs reduce output step size and suppress harmonics introduced by PWM encoding. Current summation of the four interleaved outputs reconstructs the input signal. Unit element mismatch within each 8-tap FIR does not cause distortion since all elements are used an equal number of times for any given input. However, mismatch error among the four interleaved FIR filters manifests as decimation-by-4, so out-of-band noise (OBN) at multiples of 128*Fs/4 can mix into the baseband. This effect is minimized with band rejection in the DSM at multiples of 128*Fs/4 (Fig. 20.7.2). However, since total quantization error energy is conserved, band rejection in the DSM redistributes OBN elsewhere, increasing the peak OBN gain.

A dual-bitstream ternary PWM scheme is used to increase the number of levels in the DSM quantizer by roughly a factor of 2 over a single-bitstream implementation, decreasing OBN and increasing the stable operating range of the DSM. The ternary PWM system generates 2 output bitstreams (D1, D2) for each quantizer output Q (Fig. 20.7.3). To maintain a constant data edge rate, 13 of the 4-bit quantizer output levels are available. Each bitstream in a pair of 8-clock waveforms must have a rising and falling edge. For odd codes, mismatch between the two FIR filters in each pair is shaped out of band by 2-element 2nd-order dynamic element matching (DEM) (Fig. 20.7.2).

The 64-element current source array is built from 4 interleaved pairs of 8-tap FIR filters. Each individual FIR (Fig. 20.7.4) is driven by a PWM bitstream passed through an 8-flipflop shift register. In the unit current cell, a cascoded PMOS current cell (M0, M1) is used to minimize substrate coupling. NMOS data switches (M2, M3) are used to save headroom. Balanced summing junction and data line parasitics are maintained with dummy devices M4-M6. To maintain constant digital edge activity on the local supply, ground, and substrate, a second 8-flipflop shift register with dummy loads M7-M12 is placed next to the first. This shift register is provided with data which transitions when the PWM bitstream does not (Fig. 20.7.3).

The NMOS data switches are driven rail-to-rail, minimizing transition time and total current drain over a buffered approach. While simplifying the data drivers, this approach can introduce demodulation of high frequency OBN on the opamp input nodes due to mismatched parasitics on node pairs N1/N3 and N2/N4. Dummy device M7 (M10) matches device M1 (M4) to minimize this effect. This structure also minimizes coupling on the cascode bias line, reducing adjacent element symbol crosstalk without buffering the cascode line [4].

Optimization of the current DAC placed the input common-mode (CM) of the amp at 1V, while the output CM voltage is set to 4V. Two NMOS current sources are used to level shift the opamp input down through the feedback resistors. This enables the use of faster, smaller 3.3V devices for the current DAC and at the differential input of the opamp (the digital core is also built from 3.3V devices). To reduce inband 1/f noise, chopper stabilization is used on the pulldown current sources.

The driver amplifier is a fully-differential class-AB topology with common-mode feedback; one side is used for the final output voltage. High voltage devices are used in and around the output driver stage. To handle a 4V output CM and to avoid the need for a level shift, the CM feedback amp uses high voltage input transistors. Polysilicon feedback resistors are sized appropriately to minimize nonlinearity due to grain boundaries, bottom-surface depletion, and self-heating. The output driver supply voltage is 12V, avoiding high gate field effects and providing compatibility with low-cost power supply systems. The unipolar driver supply reduces system cost by eliminating a negative voltage supply.

An output FFT is shown in Fig. 20.7.5; Figure 20.7.6 summarizes experimental results. The die size is 5.98 mm^2, and the die photo appears in Fig. 20.7.7.

References:

[1] J. Gaboriau, X. Fei, and E. Walburger, "Low THD+N, Power Audio DAC Using PWM Technology," AES 16th UK Conference, April 2001.
[2] D. Reefman, J. van den Homberg, E. van Tuijl, et al., "A New Digital-to-Analog Converter Design Technique for HiFi Applications," 114th AES Convention, March 2003.
[3] D. K. Su and B. A. Wooley, "A CMOS Oversampling D/A Converter with a Current-Mode Semi-Digital Reconstruction Filter," *ISSCC Dig. Tech. Papers*, pp. 230-231, Feb. 1993.
[4] N. Terada and S. Nakao, "A 126dB D-Range Current-Mode Advanced Segmented DAC," AES 16th UK Conference, April 2001.

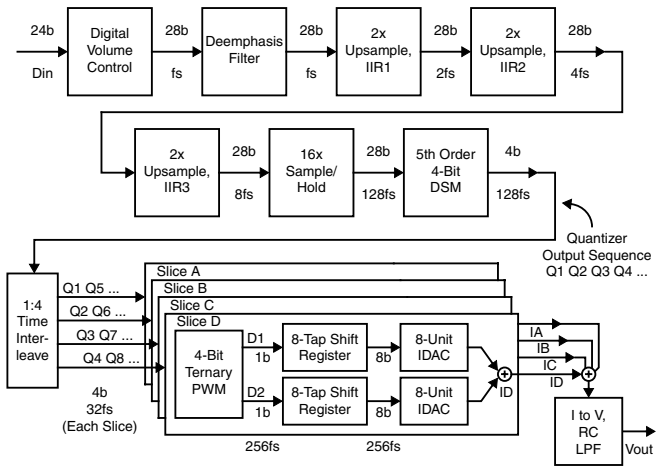


Figure 20.7.1: Audio DAC block diagram.

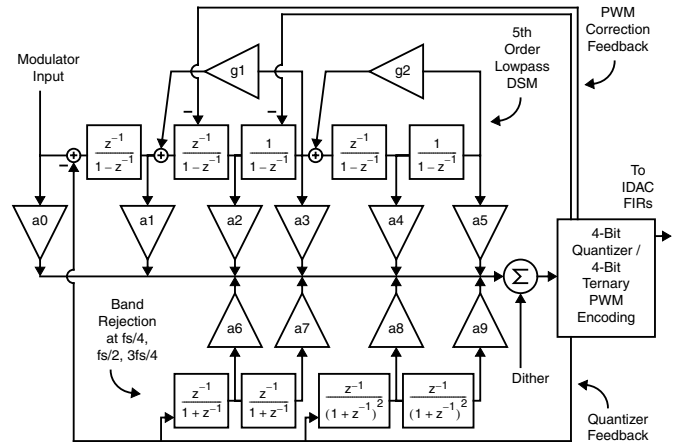


Figure 20.7.2: Delta-sigma modulator.

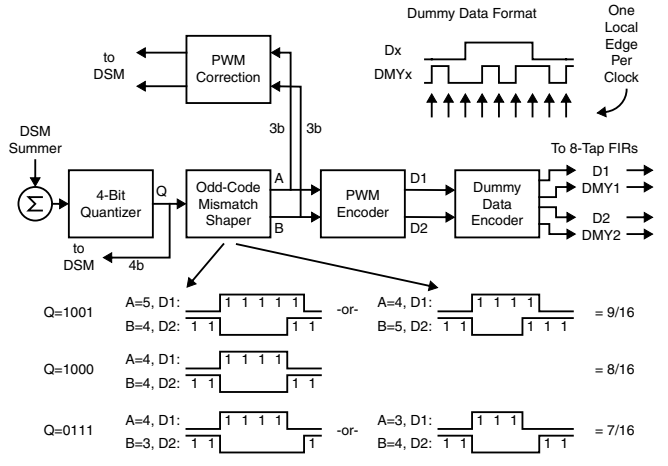


Figure 20.7.3: Ternary PWM encoding.

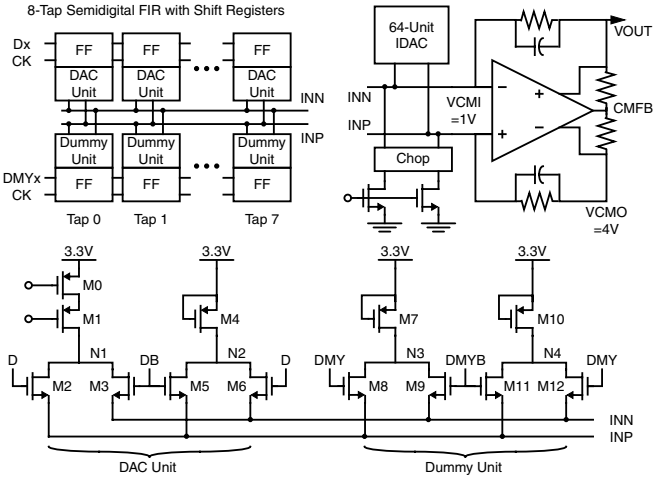


Figure 20.7.4: DAC FIR, output driver.

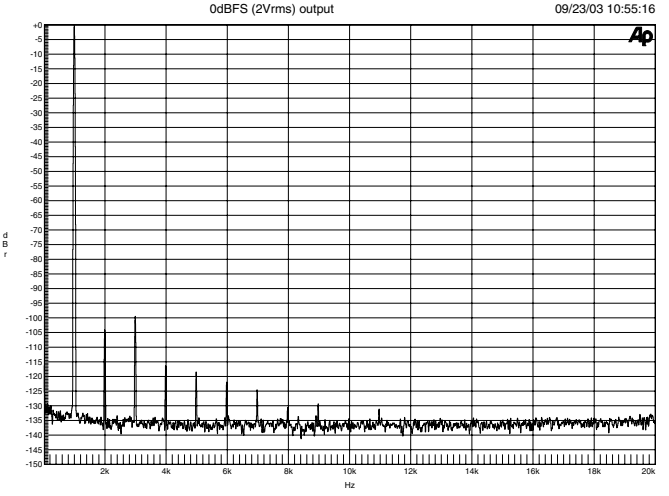


Figure 20.7.5: Output FFT (32,768 points) with 5kΩ load.

Specification	Performance	Comment
Output Swing	2Vrms (5.76Vpp)	
THD	-99dB	997Hz, 0dBFS (5kΩ load)
Dynamic Range	110dB	997Hz, -60dBFS, A-weighted
Power Dissipation	214mW	Total
	137mW	12V analog (5kΩ load)
	22mW	3.3V analog
	55mW	3.3V digital
Die area	2.02mm x 2.96mm	0.35µm/3.3V/70Å, 3µm/18V/450Å, 2P3M

Figure 20.7.6: Performance summary.

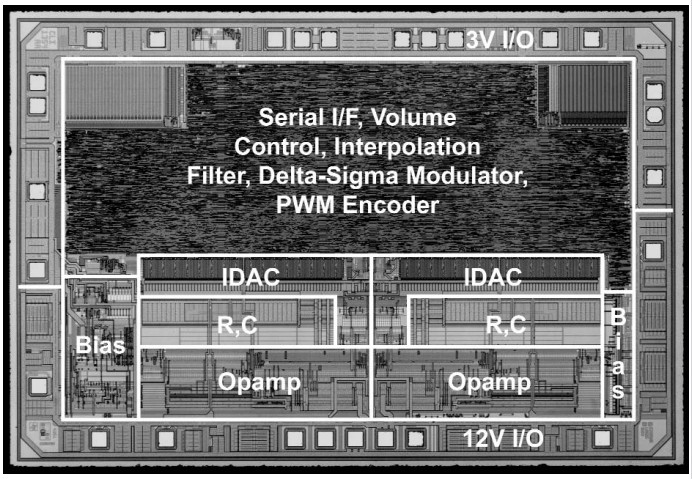
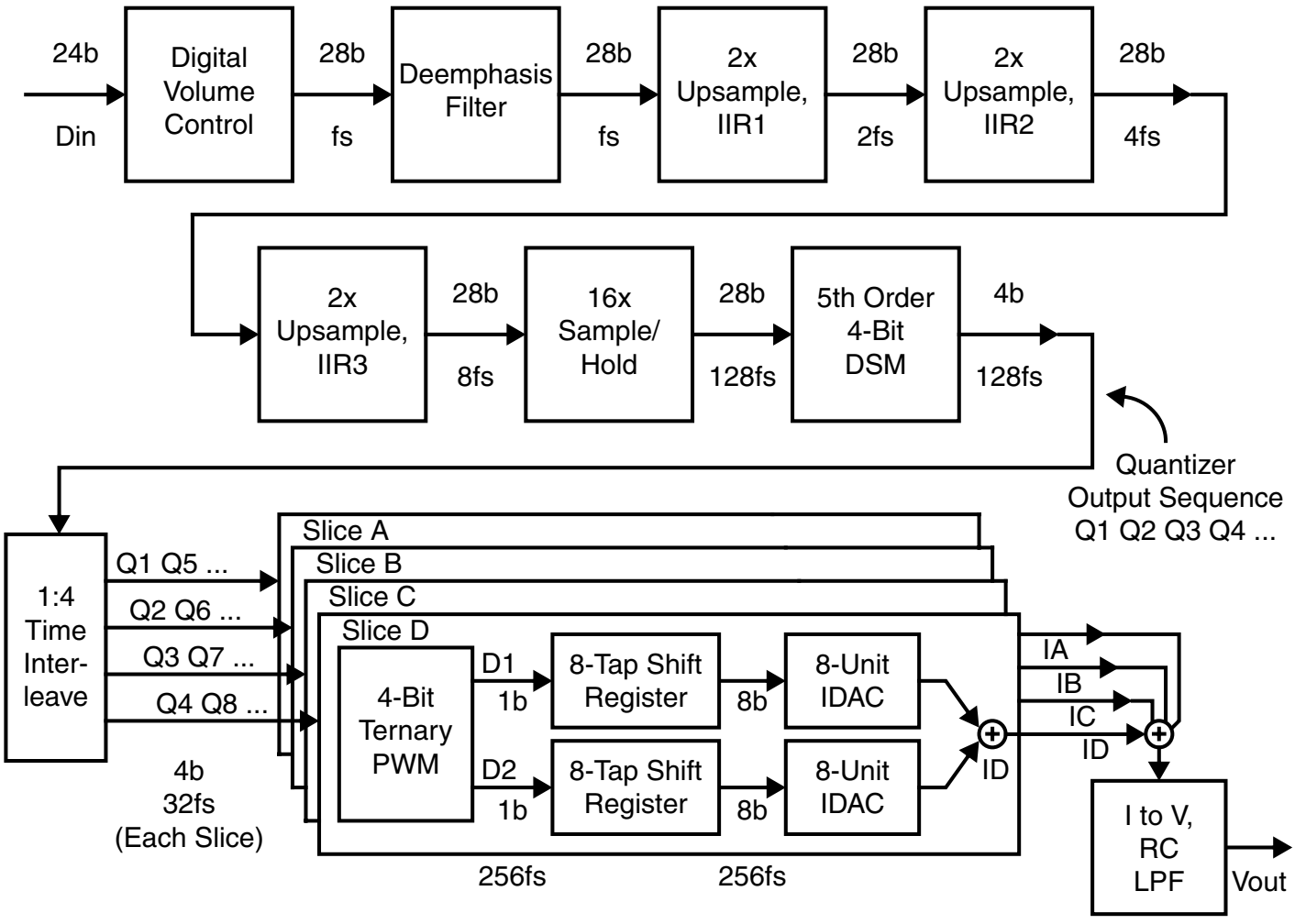


Figure 20.7.7: Die photo.



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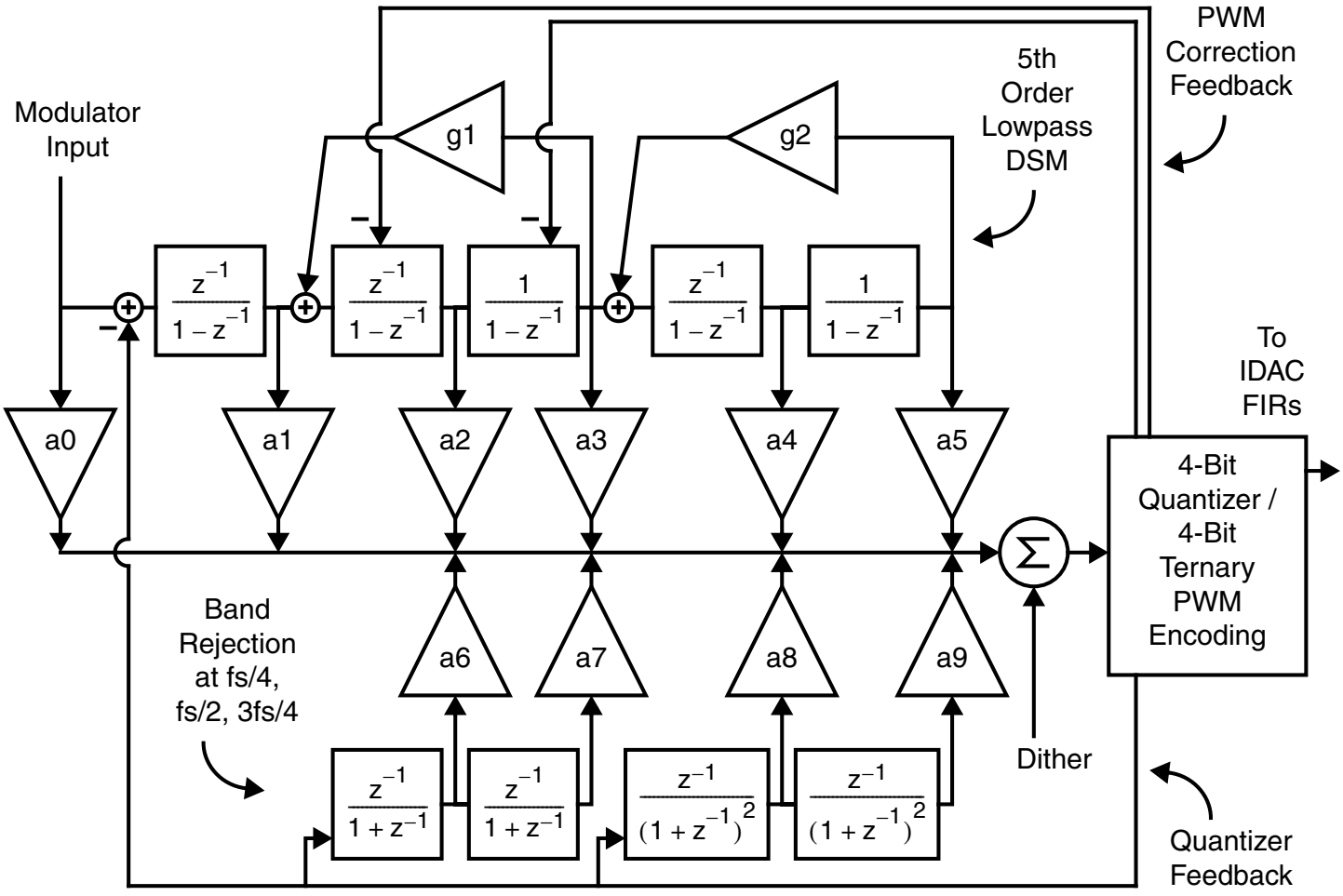
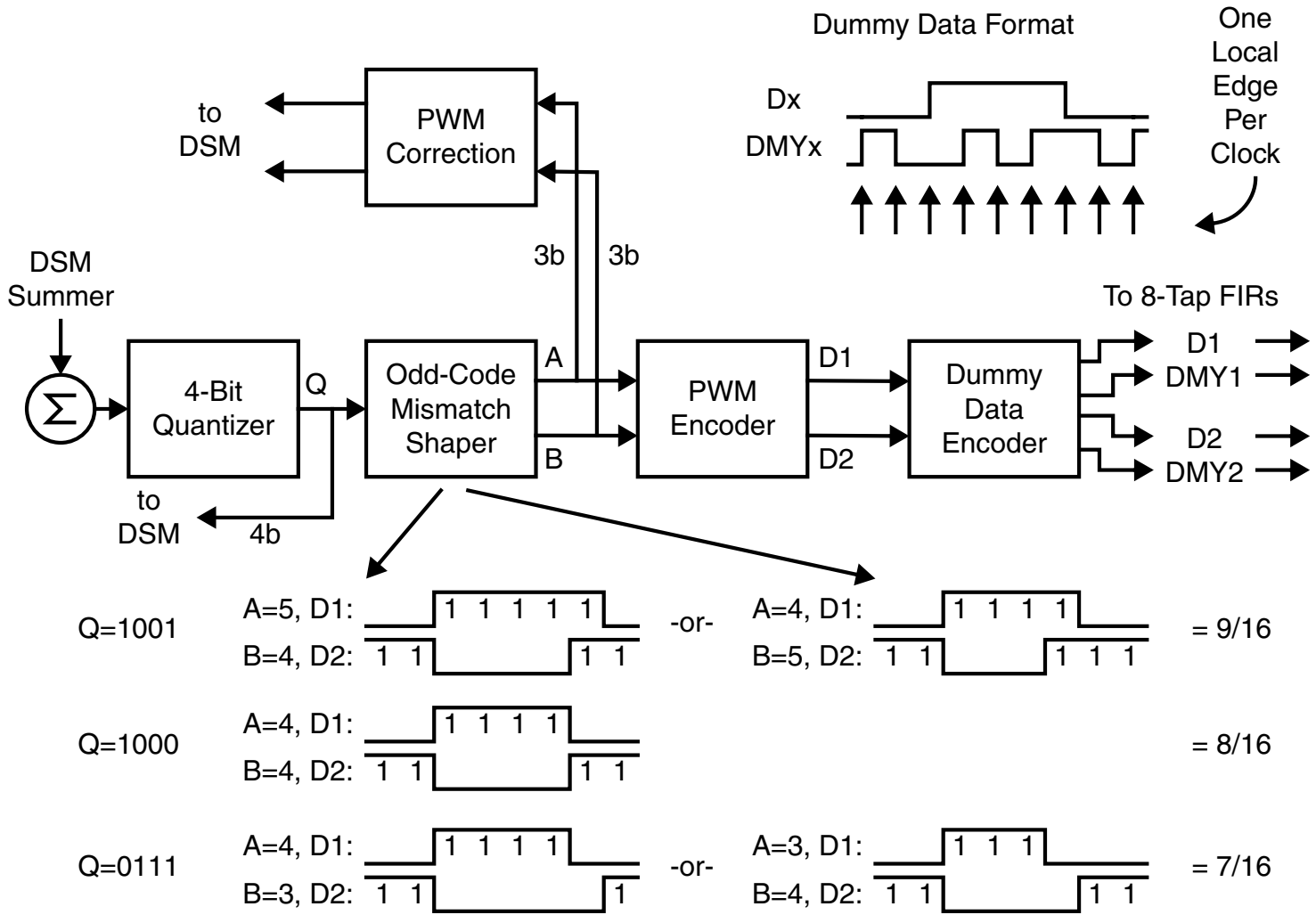


Figure 20.7.2: Delta-sigma modulator.



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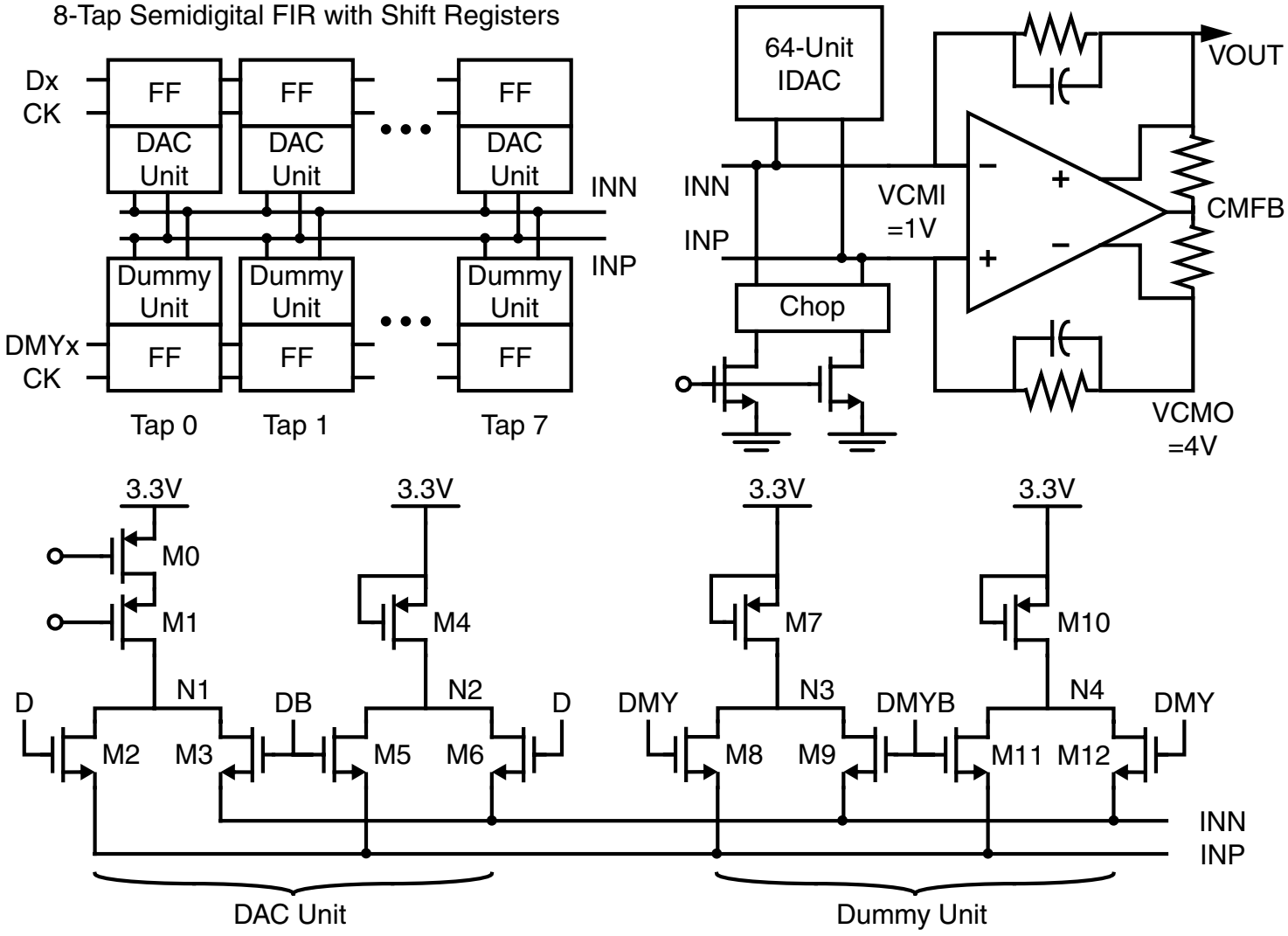
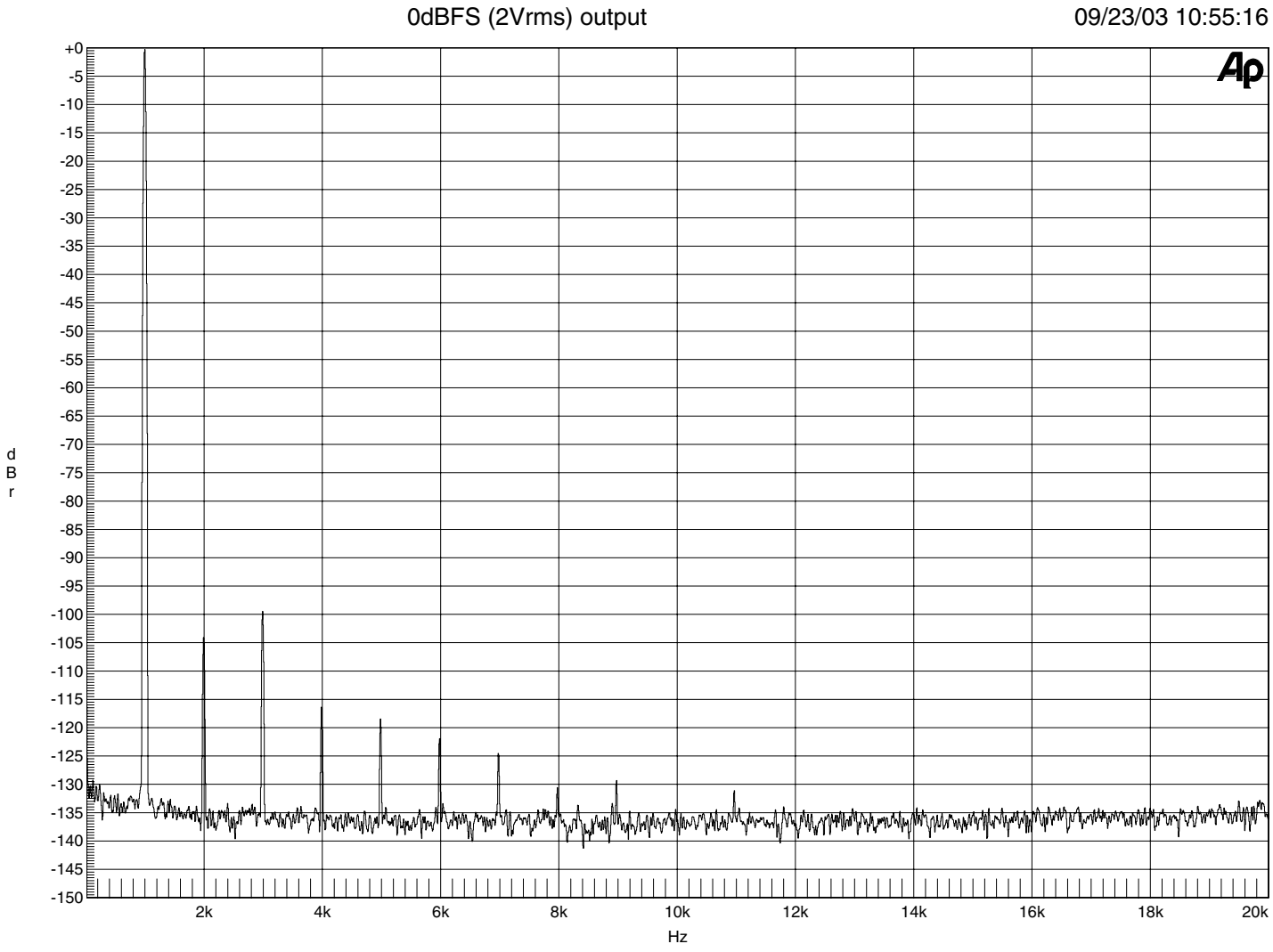


Figure 20.7.4: DAC FIR, output driver.



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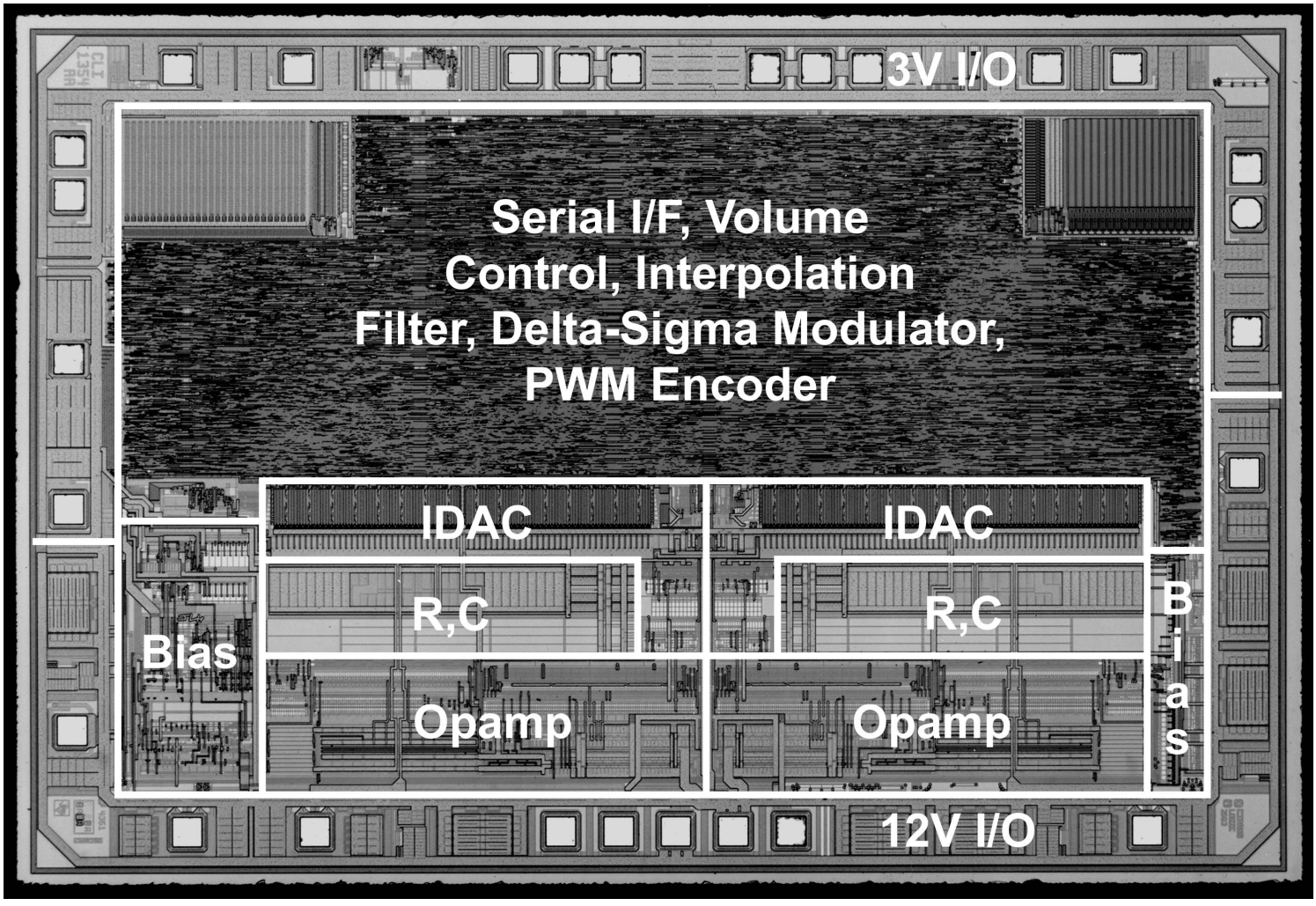

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