A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier

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***Abstract*— A temperature-stabilized 12-bit single-channel successive approximation register (SAR)-assisted pipelined analog-to-digital converter (ADC) running at 1 GS/s with Nyquist signal to noise and distortion ratio (SNDR) above 60 dB is presented. The ADC uses a three-stage (4 b-4 b-6 b) SAR-assisted pipeline hybrid architecture to achieve an attractive energy efficiency along with an extended sampling rate. A high-linearity open-loop Gm-R-based residue amplifier (RA) with both complete-settled and dynamic features improves the residue amplification efficiency and speed, while reducing the gain variation over a temperature drift. The inter-stage gain variation over the temperature is compensated through complementary temperature coefficients (TCs) from the inner devices of the RA. Furthermore, a cascade amplification topology in the backend RA alleviates the effect of the input parasitic capacitance to its front-end capacitor DAC (CDAC), thus leading to a small CDAC size to accelerate amplification and conversion. The prototype ADC was fabricated in a 28-nm CMOS process and consumes 7.6 mW from a 1-V power supply at 1 GS/s. The measured inter-stage gain variation is less than 2.3% with a temperature range from 0 °C to 80 °C. The SNDR and SFDR are 60 and 74.6 dB with a Nyquist input, respectively, achieving a Walden figure-of-merit (FoM) of 9.3 fJ/conversion-step and a Schreier FoM of 168.2 dB.**

***Index Terms*— Analog-to-digital converter (ADC), Gm-R amplifier, pipelined-successive approximation register (SAR) ADC, residue amplifier (RA), SAR-assisted pipelined ADC, SAR, temperature compensation.**

I. Introduction

HIGH-RESOLUTION analog-to-digital converters (ADCs) running in the gigahertz range [1]–[9] have attracted attention in both the wireless and wireline application spaces, enabled by continuous technology scaling. Pipelined ADCs [1]–[4] are often considered as the first candidates; however, conventionally, the amplifiers often become the power bottleneck, leading to a poor energy efficiency. This indicates a general need for high-efficiency residue amplification techniques for pipeline architectures, including both traditional pipelined ADCs [1]–[4] and pipelined-successive approximation register (SAR) ADCs [7], [9]. Time-interleaved (TI) ADCs [5]–[7] are an alternative for gigahertz high-resolution ADCs, but they face the challenges of increased area, inter-channel cross-talk, high complexity of calibration, and so on. Moreover, for the single-channel ADC, improving the sampling rate not only helps reduce the number of channels in a massive TI ADC but also contributes to lower their overall jitter and input capacitance, imposing a further push on the ADC performance boundary.

Conventional SAR ADCs [10]–[12] are not suitable for high sampling rate accompanied by high resolution, due to the speed limitation from its inherent serial conversion process. A two-step SAR-assisted pipelined ADC [8], [9], [13]–[17] breaks such limitation through the pipelined operation, while simultaneously achieving a good energy efficiency. As the sampling rate is increased, the two-step high-resolution ADC also encounters a speed bottleneck due to the large number of successive bit decisions required in each stage. Even though multi-bit/cycle SAR logic [17], loop-unrolling architecture [7], [9], and current-mode DAC [16] can improve the cycle speed of the sub-SAR ADC, they potentially induce more errors due to the additional mismatch sources. A three-stage SAR-assisted pipelined SAR ADC [7] further speeds up the conversion rate by distributing the bit decisions into more sub stages, which shows a single-channel 12-bit ADC with a conversion rate above 500 MS/s, while maintaining the attractive energy efficiency of the two-step architecture as shown in Fig. 1.

After the SAR cycle speed bottleneck has been addressed by the three-stage architecture, the residue amplifier (RA) constrains the overall speed, while it simultaneously has a major influence on the noise, linearity, and power consumption of the ADC. When compared with the closed-loop-based RA [13], [14], the open-loop-based RA [3], [7], [19]–[23] offers a higher amplification speed and a better power efficiency, but is with a higher PVT sensitivity and a worse linearity. Digital background calibration for the PVT stability

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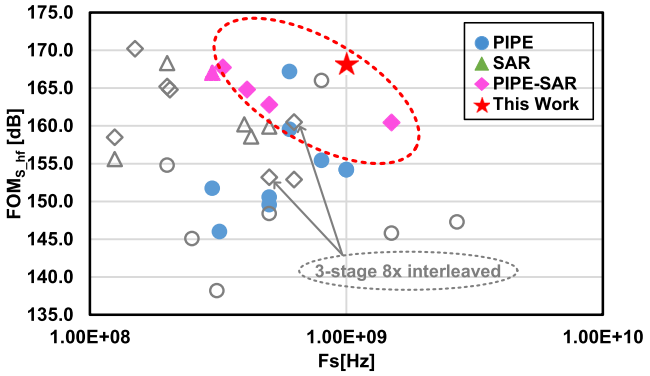

Fig. 1. Single-channel ADC survey with ≥50 dB SNDR and ≥300 MS/s presented at ISSCC and VLSI [18], where the colorized marking are the single-channel ADCs and the gray marking are the per-channel speed of TI-ADCs.

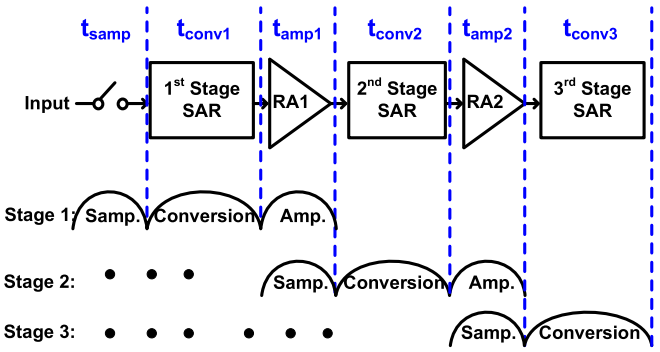

Fig. 2. Block diagram and operation timing of the three-stage SAR-assisted pipelined ADC.

and linearity [22], [23] increases the design complexity, while the analog methods [2], [3], [17], [21] have shown a simpler approach. A high-gain and high-linearity RA with fast amplification speed is essential for a high-speed and high-resolution three-stage SAR-assisted pipelined ADC [7].

In this article, both the amplification time of the RA and the conversion time of the sub-ADCs are reduced to achieve a single-channel 12-bit ADC at 1 GS/s. A high-linearity dynamic open-loop Gm-R-based RA is presented to achieve an amplification time around 200 ps with a voltage gain of 8. Moreover, a voltage bias circuit with an inverse temperature characteristic of the RA is designed to compensate the RA's gain variation under temperature change. Furthermore, a small capacitor DAC (CDAC) size in all stages is accomplished by alleviating the input parasitic capacitance of the second-stage RA with a split architecture, thereby reducing the time constant of the RA to further speed up the amplification. With the above techniques, the proposed ADC has over 60-dB signal to noise and distortion ratio (SNDR) with a Nyquist input and runs at 1 GS/s, reaching a Walden figure-of-merit (FoM) of 9.3 fJ/conversion-step and a Schreier FoM of 168.2 dB.

This article is organized as follows. Section II discusses the timing of the three-stage SAR-assisted pipelined ADC with high-speed operation. Section III reviews the past RAs and presents the referred amplifier. Section IV analyses the CDAC2 minimization. Section V introduces the overall ADC architecture and the critical design considerations. Section VI provides the measurement results, while Section VII summarizes the conclusions.

II. Timing of Three-Stage SAR-Assisted Pipelined ADC

To extend the speed of the SAR-assigned pipeline ADC, the three-stage architecture can be adopted which allows each stage to resolve less bits to speed up the overall pipeline operation. Fig. 2 shows the typical time allocation of the three-stage SAR-assisted pipeline ADC. The first and second stages need to accomplish the sampling (t_{samp}), SAR conversion ($t_{\text{conv1/2}}$), and residue amplification operation ($t_{\text{amp1//2}}$) within one period, while the third stage only needs to complete the sampling (t_{amp2}) and SAR conversion (t_{conv3}). Unlike the two-stage SAR-assisted pipelined architecture where the first stage is often the speed bottleneck of the ADC, both the first and second stages can be critical in the three-stage architecture. Therefore, the maximum achievable speed is limited by the slowest among those three stages as

$$t_{\text{3st,pipeSAR}} = \text{Max}\left\{\begin{matrix} t_{\text{samp}} + t_{\text{conv1}} + t_{\text{amp1}} \\ t_{\text{amp1}} + t_{\text{conv2}} + t_{\text{amp2}} \\ t_{\text{amp2}} + t_{\text{conv3}} \end{matrix}\right\}. \quad (1)$$

For a high-resolution and high-speed target, the sampling time of the first stage is fundamentally limited by the noise and sampling accuracy requirement. To further push the pipeline speed, one freedom is to allocate less resolving bits in the first and second stages. Nevertheless, this deteriorates the linearity of the first-stage amplifier and simultaneously asks for more quantization in the last stage, thus making the third stage become the speed bottleneck of the ADC. Another important option is shrinking the amplification time which can rise the speed of both first and second stages. Besides the amplifier circuit topology, which will be discussed later in Section III, its load capacitance is also a critical factor affecting the amplification time. Because it has a direct influence on the SAR conversion speed, minimizing the CDAC in each stage becomes a crucial target in this design.

III. Residue Amplifier

The RA is a critical block of the SAR-assisted pipelined ADC which transfers the residue to the successive pipeline stage. A high-speed and high-resolution pipelined ADC calls for an RA with a high gain in a short amplification time. RAs can be generally classified into closed- or open-loop topologies based on their working mechanism. Conventional closed-loop RA [14] ensures its gain accuracy through a high dc open-loop gain and a passive feedback configuration with complete setting, but resulting in a long setting time and high power consumption. It also suffers from low intrinsic gain under technology scaling. Recently, the ring amplifier [4], [15], [24], [25] cascading three-stage inverter provides a power-efficient and fast-settling closed-loop RA solution with a slew-based charging as shown in Fig. 3(a). Many improvements based on the ring amplifier have done for both good resilience to PVT

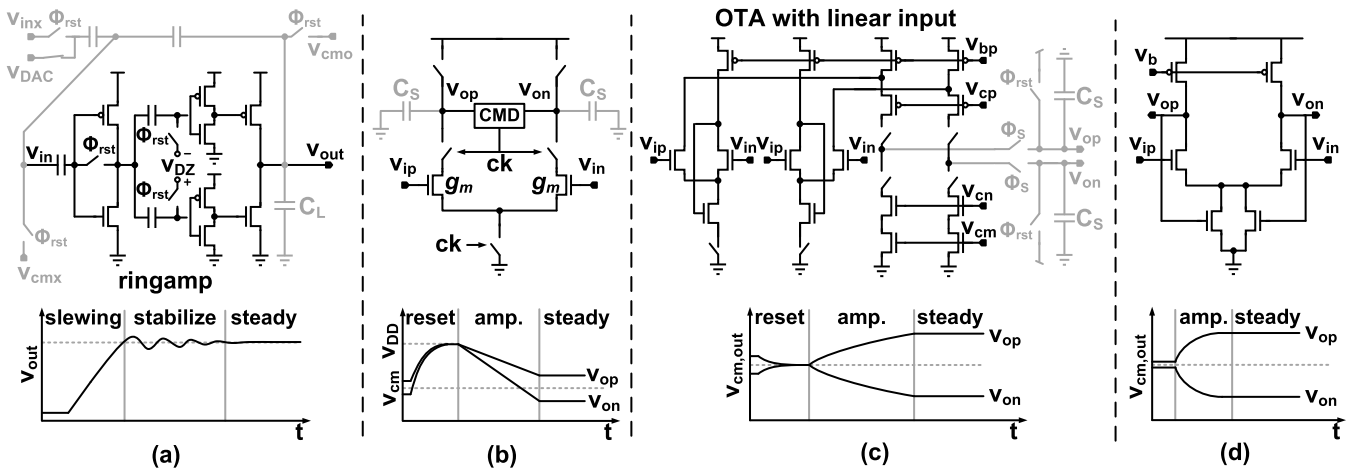

Fig. 3. Residue amplifiers with their conceptual transient responses. (a) Ring amplifier with closed-loop. (b) Dynamic amplifier with open-loop. (c) Integrator-type amplifier with open-loop. (d) Conventional complete settled amplifier with open-loop.

variation [15], [25] and fast-settling with high stability [4], while its dead-zone consideration induces design challenge under different scenarios [4], [24], especially for conventional analog designers. Recently, the open-loop architectures have been reported to overcome the weaknesses of the closed-loop architecture, achieving high power efficiency in high-speed scenario. In this section, we first review and discuss the state-of-the-art designs of two open-loop RA topologies: incomplete-settled and complete-settled amplification. Then, the adopted RA is introduced.

A. Incomplete-Settled RA

The dynamic amplifiers [19], [20] and integrator-type RA [7] working in the incomplete-settled scheme are shown in Fig. 3(b) and (c), respectively. They can achieve an excellent power efficiency and low noise integrating feature with long integration time. However, with a short amplification time in high-speed designs, its noise benefit weakens due to the increased jitter sensitivity [22], [26].

As the amplified output is not completely settled, the gain accuracy of the incomplete-settled RA is also sensitive to the clock jitter. The gain of the incomplete-settled RA is proportional to the integrating time as indicated in the following equations [22]:

$$A_V = \begin{cases} G_m \times R_o \times (1 - e^{-t_{\text{amp}}/\tau}) & \text{(2a)} \\ G_m \times t_{\text{amp}}/C_S, \quad t_{\text{amp}} \ll \tau & \text{(2b)} \end{cases}$$

where G_m and R_o are the transconductance and output impedance of the RA, respectively. τ is the time constant, which is the product of R_o and the sampling capacitance (C_S) of the backend stage. For a given A_v, a shorter t_{amp} requires a steeper slope of integration, which tends to suffer from larger jitter-induced error, and thus degrades the signal-to-noise ratio (SNR). Consequently, the jitter-induced noise becomes the primary restriction when the incomplete-settled RAs target higher SNR and speed specifications [17], [22].

Fig. 3(c) illustrates the amplification timing of the dynamic incomplete-settled RAs. Because it is necessary to integrate with the same initial output voltage (e.g., 0 V), the reset phase is required before charging the load capacitance. The phase of the "amp." comprises the startup time ($t_{\text{settling,RA}}$) of the RAs and the charging time ($t_{\text{settling,Cs}}$) of the load capacitance. Therefore, the total amplification time ($t_{\text{amp,tot}}$) of the dynamic incomplete-settled RAs is given by

$$t_{\text{amp,tot}} = t_{\text{settling,RA}} + t_{\text{settling},C_S} + t_{\text{rst}}. \tag{3}$$

$t_{\text{settling,RA}}$ relates to the load capacitance and the charging current of the RAs. For a low-noise and high-speed targets, $t_{\text{settling,Cs}}$ is limited by the jitter-induced noise requirement as interpreted above. t_{rst} depends on the overdrive of the reset switch and the load. The inevitable reset time of the incomplete-settled RA increases the critical timing path of the ADC, thus inducing a speed constraint in the pipelined ADC.

B. Complete-Settled RA

Fig. 3(d) shows a conventional open-loop RA with complete-settled amplification [8], which is immune to the above-mentioned clock jitter issue. Unlike the incomplete-settled RA, its gain is independent of time as long as the amplification process is settled, which can be expressed as

$$A_V = G_m \times R_{o,\text{eq}} \tag{4}$$

where G_m and $R_{o,\text{eq}}$ are the transconductance and the output impedance of the amplifier, respectively. Furthermore, due to its complete-settled characteristic, its voltage gain only suffers from transconductance G_m variations over voltage and temperature, allowing the adoption of a simple G_m bias circuit to perform a pure voltage-domain compensation. However, such solution consumes static power and has a poor V–I conversion linearity which requires either a higher than first-order background gain calibrations [23] with large power and

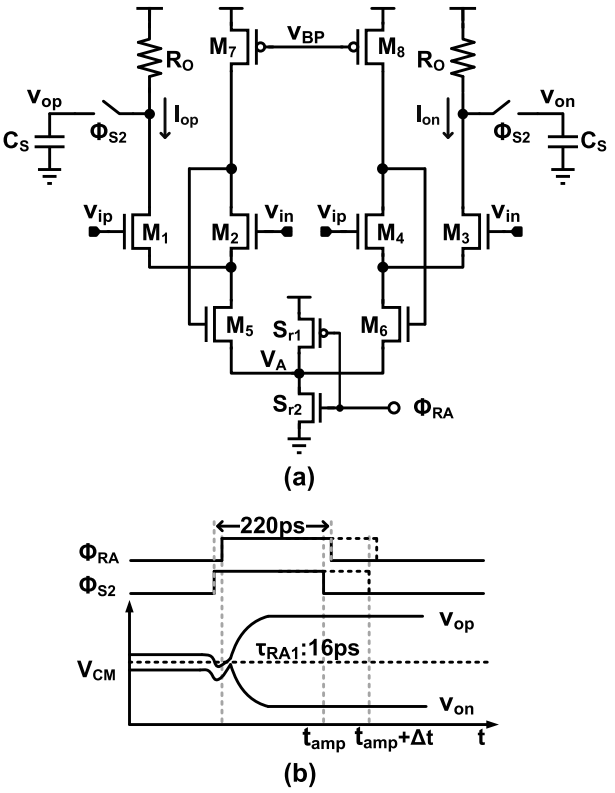

Fig. 4. (a) Gm-R-based residue amplifier. (b) Timing diagram.

area overhead or an analog linearization technique [2] but with limited ability for a high-resolution ADC. Thereby, a high-linearity and purely dynamic power Gm-R-based RA is introduced in this design.

C. Proposed RA

Fig. 4(a) illustrates the circuit schematic of the proposed residue amplifier, which is an open-loop architecture consisting of a differential Gm-cell with clock-controlled and resistive load (R_O). When compared with a conventional static open-loop amplifier [2], [8], [23], this RA is designed to have a dynamic operation with switches S_{r1} and S_{r2}. The Gm-cell is based on a differential flipped voltage follower (DFVF) [27], [28], and the shunt-shunt feedback branches (M_2, M_5, M_7/M_4, M_6, M_8) keep the gate-source voltages of M_2 and M_4 constant as the inputs vary. From this, the DFVF guarantees a high linearity under a large input swing with good power efficiency in a class-AB behavior. In contrast to the integrator-type RA [3], [7], [22], with a large time constant and an incomplete-settled mechanism, the proposed one is completely settled with a small time constant through R_O (200 Ω). The gain of the amplifier at the steady-state can be described by [27]

$$A_V = 2\sqrt{\mu_n \times C_{\text{ox}} \times (W/L)_{M_{1\&3}} \times \mu_p \times C_{\text{ox}} \times (W/L)_{M_{7\&8}}} \times R_{\text{out}} \times V_{\text{OV},M_{7\&8}} \quad (5)$$

where μ_n and μ_p are the mobility of NMOS and PMOS devices, respectively. W/L is the transistor size, and V_{OV} is the overdrive voltage. R_{out} is the equivalent output impedance. Profiting from the complete-settled characteristic, the gain

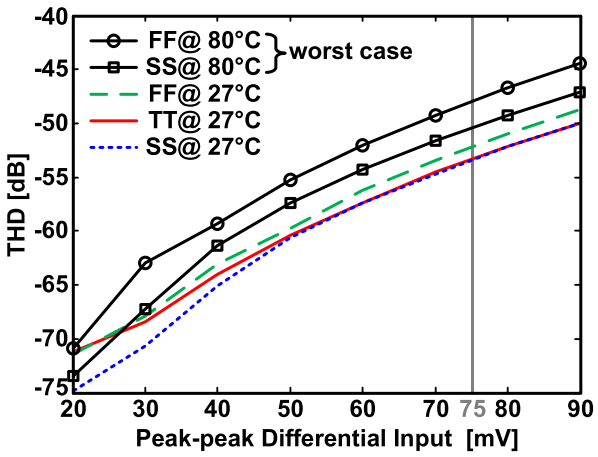

Fig. 5. Simulated linearity of the presented RA with different residue input ranges.

variation versus temperature variation of the presented RA can be easily compensated in the voltage-domain as shown in Section V. Fig. 4(b) shows the signal behavior of the proposed RA with an input residue voltage and a load of 40 fF. During the amplification phase (both Φ_{S2} and Φ_{RA} are high), the residue voltage is amplified to the next stage in a pipelined manner. With an ADC full swing (V_{FS}) of 1.2 V_{pp}, the residue voltage is within 75 mV_{pp}. The open-loop DFVF RA with 8× gain ensures a near 9-b linearity under the worst case working scenario as plotted in Fig. 5. Besides, the proposed complete-settled RA eliminates the reset time and its gain is independent of the time as long as the amplification is well-settled. Its amplification time can be expressed as

$$t_{\text{amp,tot,gmR}} = t_{\text{settling,RA}} + t_{\text{settling},C_S} \quad (6a)$$

$$t_{\text{settling},C_S} = \ln 2 \times (N_{\text{bit}} + 1) \times \tau_{\text{RA}} \quad (6b)$$

where N_{bit} is the target bit resolution and τ_{RA} is the time constant of the amplifier which is equal to $R_{\text{out}} \times C_{\text{load}}$. Compared with the incomplete-settled RA, the reset time t_{rst} in (3) is eliminated to speed up the amplification. In the first stage, 250 ps is allocated for the sampling time t_{samp} to ensure the sampling accuracy under Nyquist input. The first 4-b decisions finish within 500 ps with a small DAC-assisted SAR conversion (detailed in Section V). Then, only ∼200 ps is left for RA1 to amplify the residue signal under a 1 GS/s goal. Therefore, a small load capacitance of RA1, which is CDAC2, is a key for a short t_{amp1}. Likewise, CDAC2 also affects the conversion time of the second-stage SAR t_{conv2}, and in consequence potentially leading the second stage to be the speed bottleneck of the overall ADC.

The presented dynamic Gm-R-based amplifier provides a high-speed and energy-efficient residue amplification with a dynamic feature. First, compared with the incomplete-settled RA, the proposed RA not only removes the reset time but also frees from the jitter-induced error, while both of them limit the amplification speed of the incomplete-settled RA at high resolution. Second, the load capacitance (CDAC2) of RA1 is reduced with a two-stage RA2 structure (detailed in Section IV) to further shorten the amplification time. In consequence, the presented Gm-R-based amplifier achieves

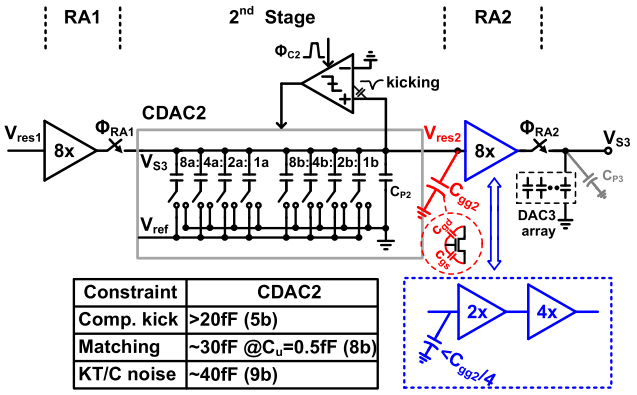

Fig. 6. Second-stage and split RA2 (single-side for simplification).

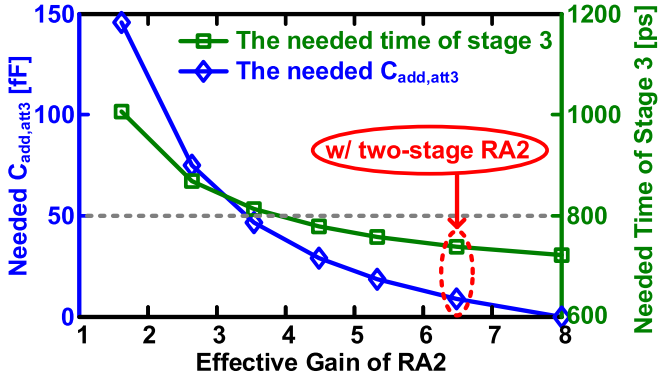

Fig. 7. Needed $C_{\text{add,att3}}$ and loop time of the third stage with different effective gains of RA2.

an 8× gain with ∼200-ps amplification time, which is one of the fastest to date. Furthermore, the proposed Gm-R-based RA suffers from fewer temperature-related variables benefiting from its complete-settled characteristic, and then a low-power voltage-domain temperature compensation instead of the complex time-domain solutions [17], [21] can be adopted (detailed in Section V-B).

IV. CDAC2 Minimization

The size of the CDAC in the SAR ADC is limited by the fundamental requirements, such as noise, mismatch, and the kickback noise from the comparator. For a three-stage SAR-assisted pipelined ADC as shown in Fig. 2, the value of the CDAC1 in the first stage is set by the noise and mismatch requirements which indeed is a relative large value of 540 fF in this design. While with a gain of 8 from RA1, only a small CDAC2 can meet the noise, mismatch, and comparator kickback noise requirements. For the kickback noise of the comparator, it only needs to be suppressed within 5-b accuracy as the error correction in the third stage can cover the decision error from the second stage, thereby a small value (30 fF) of CDAC2 can fulfill the comparator kickback noise requirement. In terms of matching, a CDAC with 0.5-fF MOM unit capacitor in the adopted technology is enough to achieve an 8-b matching requirement [30]; then, it does not impose a limitation on the total capacitance of CDAC2. Finally, a 9-bit noise requirement in the second-stage DAC calls for a minimum CDAC2 of 40 fF. Fig. 6 depicts the above-mentioned constraints and their set minimum boundary on CDAC2.

The listed constraints in Fig. 6 are further relaxed by RA2 in the third stage; therefore, a small unit capacitor (0.5 fF) is adopted in CDAC3. In contrast to the first and second stages, the timing allocation of the third stage only consists of sampling (t_{amp2}) and 6-b conversion (t_{conv3}). With t_{amp2} set to a ∼200-ps target, the maximum available time for t_{conv3} is only 800 ps. To maintain a large full scale in the third stage and reuse the same reference from previous stages for high-speed and design simplicity, the gain of RA2 is also designed to be 8. With a gain of 8- and 7-b accuracy in 200-ps amplification time, the resistive load is 200 Ω requiring at least a 40-mS transconductance. Such a large transconductance results in a large input parasitic capacitance in RA2 (C_{in2} =∼30 fF), which increases the total capacitance on the top-plate of CDAC2, thereby in turn increases the amplification time of RA1 and settling time of CDAC2. Eventually, the small CDAC2 (40 fF) will suffer from a large gain loss as introduced next.

A. Effective Gain Loss

When RA2 is enabled for amplification, its input capacitance C_{in2} consists of two parts. One is from the constant gate capacitance C_{gg2} and the other is the varying gate capacitance ΔC_{gg} that is originated by the dynamic operation of RA2. The nonlinearity caused by such ΔC_{gg} is mitigated by the lower internal swing and RA1 when referred to the input; therefore, mainly C_{gg} is considered in the below discussion. If RA1 is reused for RA2, a large parasitic capacitance C_{gg2} originating from C_{gs} and C_{gd} of the input pair causes a significant signal attenuation on V_{res2}, equivalently leading to an effective gain loss on RA2. For a 6-b SAR ADC in the last stage, the settling time of CDAC3 ($t_{\text{settling,CDAC3}}$) needs more than $5\tau_{\text{CDAC3}}$ to avoid the settling error, where τ_{CDAC3} depends on the ON-resistance of switches and the total capacitance (C_{tot3}) in the third stage. The above-mentioned gain loss degrades the power efficiency of RA2 and reduces the full scale of the third stage, consequently requiring more attenuation capacitance (C_{P3}) and additional settling time in CDAC3. Such extra time multiplied by 5 through the SAR bit cycling potentially makes the third stage become the speed bottleneck. Likewise, if the gain of RA2 is designed as 4 or smaller to reduce C_{gg2}, a similar consequence of a larger attenuation capacitor also slows down the third-stage conversion. Considering the gain loss with different gains of RA2 ($A_{V,\text{RA2}}$), the additional attenuation capacitance ($C_{\text{add,att3}}$), based on the condition with effective gain = 8, in the third stage can be given by

$$C_{\text{add,att3}} = \text{CDAC3}\left(\frac{8}{A_{V,\text{RA2}}(1-\alpha_{\text{att,RA2}})} - 1\right) \tag{7}$$

where $\alpha_{\text{att,RA2}}$ is the attenuation factor of V_{res2}, which depends on the transconductance of RA2. The simulated result from Fig. 7 shows the amount of needed $C_{\text{add,att3}}$ in the third stage with different effective gain of RA2. In this design, after taking the 200-ps amplification time into account, only

600 ps is available for the third-stage SAR conversion, and the maximum available $t_{\text{settling,CDAC3}}$ needs to be within 25% of the SAR conversion time to guarantee the last 6-b SAR logics are well-completed. Assuming the same switch size, the necessary time of the third stage with the corresponding $C_{\text{add,att3}}$ under different transconductance and a fixed 40-fF CDAC2 is shown in Fig. 7. A larger effective gain of RA2 will reduce the $C_{\text{add,att3}}$ and thereby the settling time of CDAC3. When the intrinsic gain of RA2 is designed as 8 with large transconductance as RA1, the consequent large C_{gg} of RA2 leads to almost 50% V_{res2} attenuation with 40-fF CDAC2, and thus the small effective gain (4.5×) makes RA2 less efficient. Although RA2 of 4.5× effective gain keeps the time expenditure of the third stage within the loop time boundary, it leaves no margin for the metastable condition.

B. Two-Stage Amplifier

One solution is to enlarge the size of CDAC2, tolerating the parasitic-induced error of RA2. While large CDAC2 tends to need a longer amplification time of RA1 and slow down the speed of stage 1. Another solution is to scale down the size of RA2, reducing the parasitic-induced gain loss from RA2. However, the gain of RA2 will be scaled down simultaneously, equivalently leading to the effective gain reduction. The consequent longer amplification time of RA2 and the conversion time of the third stage slow down the loop speed of stage 2 or stage 3 where either scenario will prevent our design to reach the GS/s target.

To keep a large gain of RA2 with a small input parasitic and avoid a large CDAC in the last two pipelined-SAR stages, RA2 is split into two stages, in which the first stage is with small parasitic and small gain, whereas the second stage is with large parasitic and large gain. In this design, RA2 with 8× gain is cascaded by a 2× gain with 4× gain as shown in Fig. 6. The effective gain loss is reduced to 19%, and the settling time of CDAC3 is reduced >50% than the single-stage RA2 with 8× intrinsic gain as shown in Fig. 7. Thanks to the complete-settled feature, both stages in RA2 can amplify the signal at the same time. Such configuration is not feasible in the integrator-type amplifiers, because the integrating process is incomplete-settled in the intermediate time and the large second-stage input variable parasitic capacitance will affect the first-stage amplifier's linearity. Those two constraints make the amplifier become more sensitive to PVT variations and more nonlinear that cannot fit the RA2's design requirements and inevitable demands for a two-step operation at lower speed.

The proposed complete-settled amplifier together with two-stage setup ensures a high-speed operation, which is not only on the three-stage conversion but also on the RA2's amplification. In this design, the pole of the first stage is designed to be more than double the location of the second stage's pole. While to maintain the same bandwidth as RA1, an additional 25% power is budgeted in RA2. The additional noise contribution from the two-stage configuration is not critical for RA2 as it will be relaxed by the gain of RA1. Another consideration is the linearity, as the input of the second stage of RA2 is amplified two times by the first stage of RA2. In this design, both the stages of RA2 are configured with the FVF input pair same as RA1 to meet the 7-b linearity requirement.

V. Proposed ADC Implementation

A. Three-Stage SAR-Assisted Pipelined Architecture

Fig. 8 presents the overall architecture and timing diagram of the prototype ADC, composed of three sub-SAR ADCs, two RAs, a clock generator, a digital logic, and a calibration block. To guarantee a >70 dB sampling linearity, 250 ps is assigned for the sampling ($\Phi_S = 1$). The ADC is designed with a fully asynchronous loop timing and 14 conversion cycles, while 1 redundant bit is allocated between each stage for error correction. Both the first and second stages only resolve 4-bit, ensuring an adequate sampling and amplification time for high linearity. In the first stage, a large CDAC (L-DAC = 540 fF) is required to alleviate the thermal noise and mismatch, which usually becomes the speed bottleneck of the SAR-assisted pipelined ADC. In this article, a small CDAC (S-DAC = 60 fF) is used for the high-speed first-stage SAR conversion where its decisions are transferred to the L-DAC in a bit-by-bit manner to generate the residue voltage (V_{res1}) on the L-DAC. Both the L-CDAC and S-DAC sample the input signal (1.2 $V_{\text{pp-diff}}$) together during Φ_S, and the sampling mismatch can be mitigated by a symmetric clock tree and a careful layout and corrected by the bit overlapping in the second stage. V_{res1} is amplified by RA1 with a gain of 8 to the second stage that resolves another 4 bits and its residue voltage (V_{res2}) is delivered to the third stage through RA2 with a gain of 8, as well. Due to the above-mentioned residue voltage attenuation during the amplification, the full-scale range of the second and third stages is ∼500 and ∼400 $mV_{\text{pp-diff}}$, respectively. Finally, the remaining 6 bits are determined in the last-stage SAR ADC. The splitting monotonic switching scheme [10], used in each stage, maintains a constant common mode voltage for both RAs and comparators. To reduce the inductive effect from the bonding wire, an input buffer [1] is embedded on chip.

B. Temperature Compensation With Current Biasing

Due to the large gain of RA1, the impact of the gain variation in RA2 is significantly relaxed. The SNDR degradation due to the gain variation in RA1 and RA2 of the proposed ADC is illustrated in Fig. 9. For a target above 9-b ENOB, the gain variation in RA1 and RA2 should be within ±3% (RA1 and RA2 have the same compensation scheme in this article). While the gain variation over the process can be calibrated in the foreground and the supply voltage variation can be mitigated by the power management unit, the temperature variation becomes the major issue.

The gain over temperature (T) of the proposed RA can be expressed as

$$A_V(T) \propto \sqrt{\mu_n(T) \times \mu_p(T)} \times V_{\text{OV}_{M7,8}}(T) \times R_O \qquad (8)$$

where $V_{\text{OV},M7,8}$ is the overdrive voltage of M_7 and M_8 in Fig. 4(a). As the adopted $P+$ poly resistor only varies

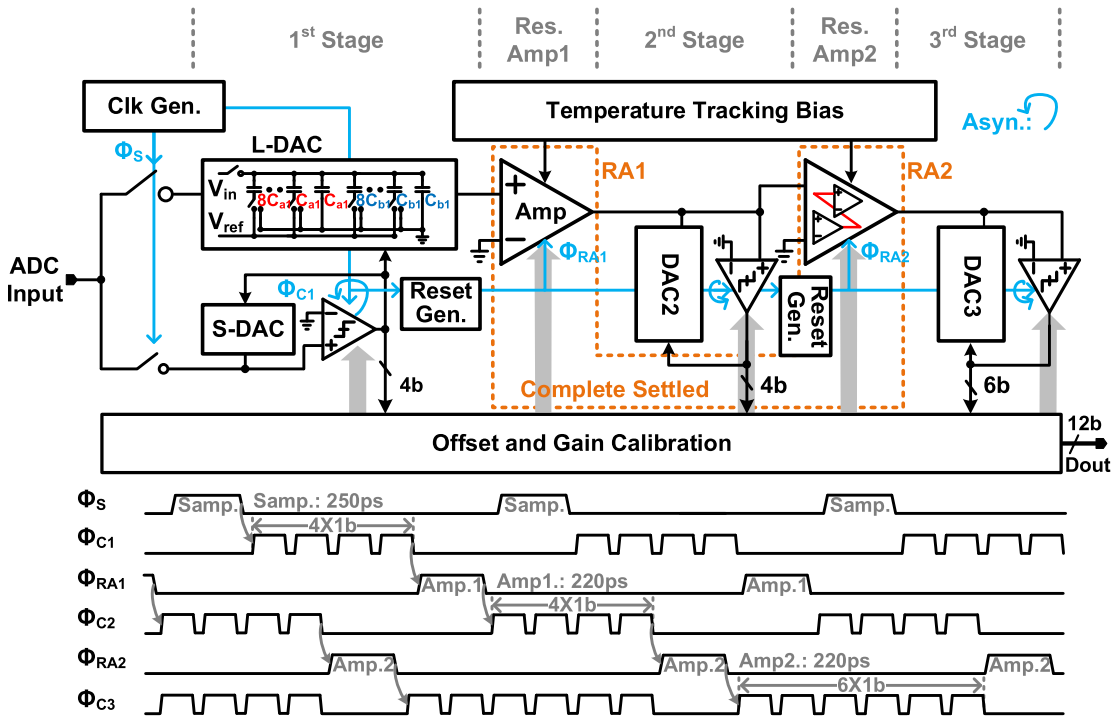

Fig. 8. Block diagram and timing diagram of the proposed three-stage ADC.

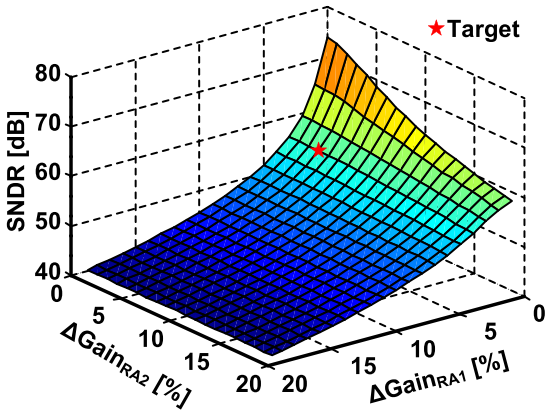

Fig. 9. Impact of gain variation in RA1 and RA2 on the ADC performance.

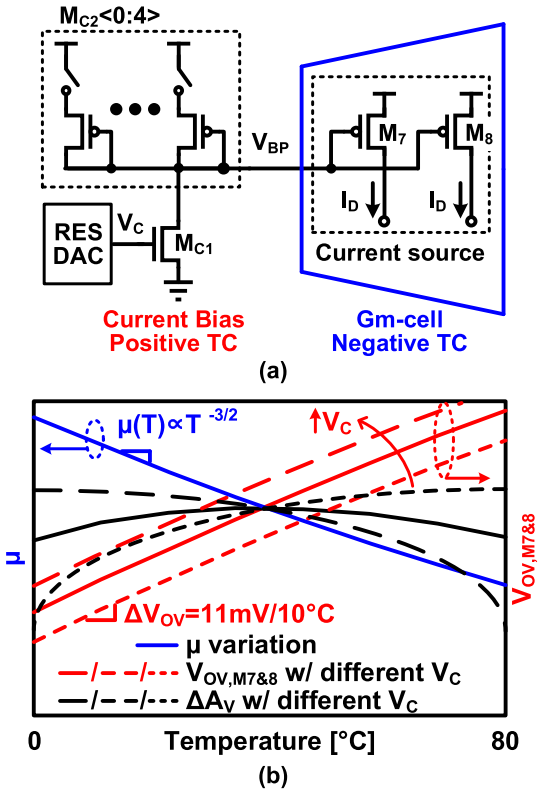

Fig. 10. Temperature compensation concept in the proposed RA. (a) Compensation scheme. (b) Temperature characteristic of mobility, overdrive voltage, and gain.

0.22 Ω/decade °C according to the data from the foundry, the gain variation is dominated by the temperature-related mobility and overdrive voltage.

It is well-known that the mobility has a negative temperature coefficient (TC) characteristic [blue line in Fig. 10(b)] [29]. Consequently, it leads to a complementary gain compensation scheme like [21], where $V_{\mathrm{OV},M7,8}$ is expected to produce a positive TC to compensate the mobility variation. Benefitting from the complete-settled feature of the presented Gm-R-based RA, the compensation can be simply achieved through the biasing scheme of Fig. 10(a) rather than the complex time-domain approach [21]. $V_{\mathrm{OV},M7,8}$ under temperature variations is given by

$$V_{\mathrm{OV},M_{7\&8}}(T) \propto \sqrt{\frac{(W/L)_{\mathrm{MC1}}}{(W/L)_{\mathrm{MC2}}}} \times [V_{\mathrm{C}} - V_{\mathrm{thn,MC1}}(T)] \qquad (9)$$

where $(W/L)_{\mathrm{MC1}}$ and $(W/L)_{\mathrm{MC2}}$ are the dimensions of the transistors M_{C1} and M_{C2}, respectively. V_{C} and $V_{\mathrm{tnn,MC1}}$ are the bias and threshold voltage of the transistor M_{C1}, respectively. It can be recognized from (9) that $V_{\mathrm{OV},M7,8}$

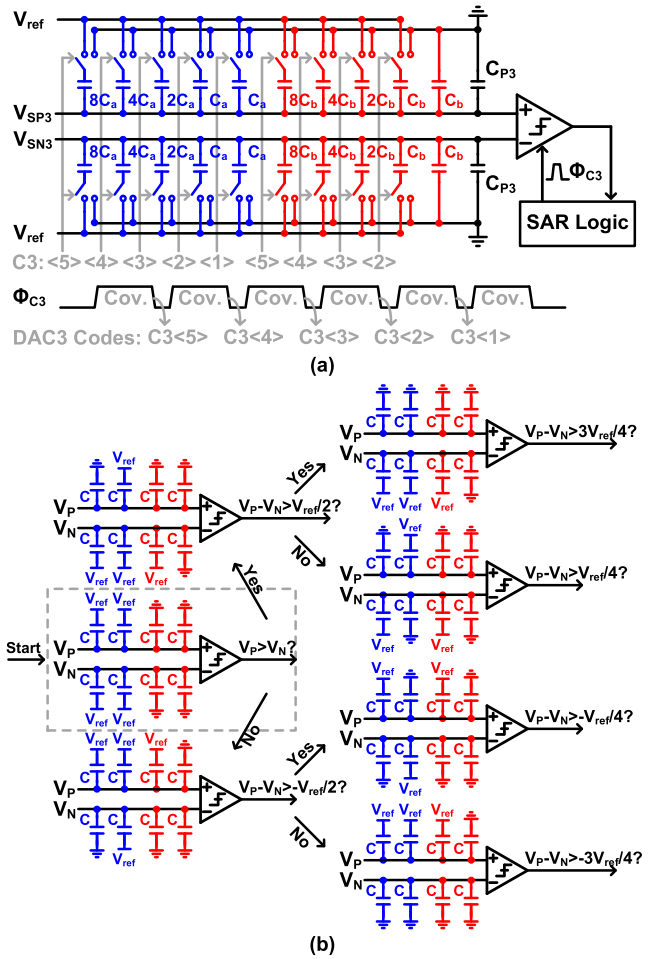

Fig. 11. (a) Third stage. (b) Switching example with 3 b.

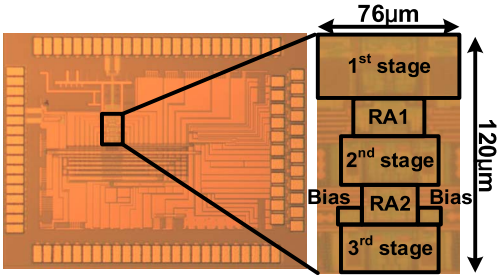

Fig. 12. Die photograph.

produces a positive TC [red line in Fig. 10(b)] as $V_{\text{th,MC1}}$ experiences a negative TC characteristic [29]. As illustrated by (9), V_C works as a dc offset of $V_{\text{thn,MC1}}$, and the dimension ratio of M_{C1} to M_{C2} is used to change the slope of $V_{\text{thn,MC1}}$ variation versus temperature change. The size of M_{C2} in Fig. 10(a) is programmable with a 5-b digital control to compensate the process corners with the measurement of two temperature points (e.g., 0 °C and 80 °C). After that, V_C is configured to guarantee the accurate inter-stage gain [31]. In addition to the variation in the Gm-cell itself, the charge share from the sampling switches also causes a small gain variation through the impact on the input common mode of the RA. Ultimately, the gain variation in the Gm-cell itself is multiplied by the gain variation in the charge share, which

TABLE I
ADC NOISE CONTRIBUTION

Input buffer noise	28.5 nV^2	45.6%
KT/C noise	15.98 nV^2	25.5%
RA1 noise	8.8 nV^2	14.1%
QTZ noise	7.16 nV^2	11.4%
RA2 noise	1.12 nV^2	1.8%
Comparator noise	1.02 nV^2	1.6%
Total noise	62.58 nV^2	100%
SNR	64.6 dB	

enlarges the total gain variation. Thus, a larger compensation range of $V_{\text{OV},M7\&8}$ is needed to well-compensate the total gain variation. Like the other pipelined ADCs with open-loop RA, the accuracy effective gain detection is still necessary to match two pipelined stages. In this design, the effective gain is extracted based on the code histogram [32] in the digital domain (off-chip) and the correction is realized by trimming the bias of the RAs in the analog domain (on-chip). In practice, some well-known methods [1], [7], [23] can be implemented on-chip to achieve the first-order gain calibration.

C. Third-Stage Design and Overall Noise Contribution

In the third stage, CDAC3 adopts a single-end operation as illustrated with a 3-b switching example in Fig. 11, which reduces CDAC3 size by half. Because the third stage only resolves 6 b and experiences a 64× gain from the input, its thermal noise requirement is relaxed. Therefore, only a 50-fF capacitance in CDAC3 is used, limited by the minimum unit capacitance (0.5 fF) for matching. The noise of the two-stage amplifier, dominated by the first stage in RA2, is significantly relaxed by the gain from RA1 [22]. Table I shows the simulated noise contribution of the total ADC. The total input referred noise is 62.58 nV^2, resulting in a 64.6-dB SNR.

VI. MEASUREMENT RESULTS

The prototype ADC was fabricated in a 28-nm CMOS process. The die photograph is shown in Fig. 12 occupying a core area of 0.0091 mm^2. The ADC powered by a 1-V supply exhibits a 1.2 $V_{\text{pp-diff}}$ full-scale range. Due to the unskilled layout, the L-DAC suffers from some mismatch and a bit weight calibration is adopted in the measurement. The first 4-b codes are corrected with integer bit weight one-time, and the bit weight array is fixed to different samples. Besides the one-time calibration to the comparator offset (histogram-based detection in the measurement), RAs' gain is done in the foreground. As illustrated in Fig. 13, the measured DNL and INL are +0.47/−0.39 LSB and +1.87/−2.21 LSB, respectively.

Fig. 14 shows the measured output spectrum after a decimation of 225-fold at a low input frequency and near the Nyquist input frequency, respectively. For a low input frequency of 140.63 MHz, the measured SNDR and SFDR are 61.4 and 74.6 dB, respectively, and the noise performance (SNR) is

TABLE II
ADC PERFORMANCE SUMMARY AND COMPARISON

	This work	VLSI 2017[16] K.-J. Moon	JSSC 2018[3] R. Sehgal	ISSCC 2017[9] L. Kull	ISSCC 2017[17] H. Huang	ISSCC 2019[25] B. Hershberg	JSSC 2019[4] J. Lagos
Architecture	Pipelined SAR	Pipelined SAR	Pipeline	Pipelined SAR	Pipelined SAR	Pipeline	Pipeline
Residue Amplifier	Open-loop Gm-R	gm-cell	Open-loop Integrator	CML Amplifier	Dynamic Amplifier	Ring Amplifier	Ring Amplifier
Technology	28nm	28nm	28nm	14nm	65nm	16nm	28nm
Resolution [bits]	12	10	12	10	12	11	12
Sample Rate [MS/s]	1000	500	280	1500	330	600	1000
Supply Voltage [V]	1	1	1	0.95	1.3	0.85	0.9
SFDR @Nyq. [dB]	74.56	69.2	77	58.39	75.8	78.3	73.1
SNDR @Nyq. [dB]	60.02	56.6	64	50.1	63.5	60.2	56.6
Power [mW]	7.6	6	13	6.92*	6.2	6.0	24.8
FoM_{Walden} @Nyq. [fJ/conv-step]	9.28	21.7	35.8	17.7*	15.4	12	45
$FoM_{Schreier}$ @Nyq. [dB]	168.2	162.8	164.3	160.5*	167.8	167.2	159.6
Area [mm^2]	0.0091	0.015	0.22	0.0016	0.08	0.037	0.54

* including the reference buffer

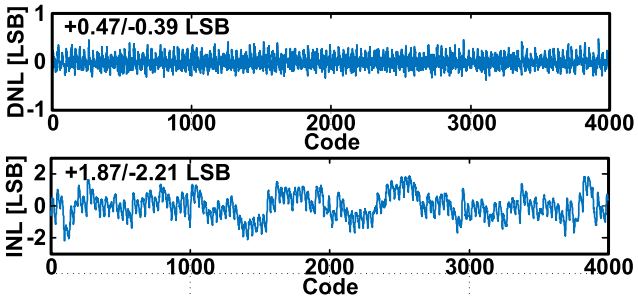

Fig. 13. Measured DNL and INL.

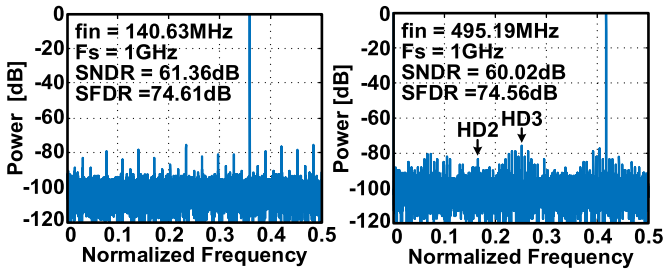

Fig. 14. Measured output spectrum at 1 GS/s with 140.63-MHz input and 495.19-MHz input (16384 points and ADC output decimated by 225×).

limited by the input buffer. For the near Nyquist input frequency of 495.19 MHz, the measured SNDR keeps 60 dB and the SFDR keeps 74.6 dB. Fig. 15 shows the measured dynamic performance at 1 GS/s versus the input frequency. The ADC achieves above 9-b ENOB even with the input frequency raised up to 1.2 GHz, and the estimated clock jitter (∼200 fs) degrades the dynamic performance when the input signal exceeds 1 GHz. Fig. 16 depicts the measured dynamic performance at 140.63-MHz input and sweeping from 600 MS/s to 1.3 GS/s. It can be seen that the ADC keeps around 59-dB SNDR under 1.1 GS/s.

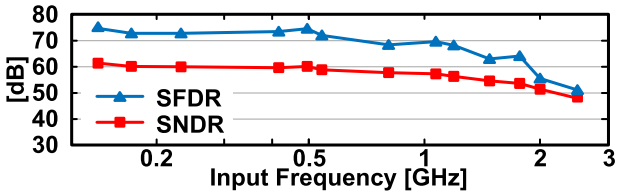

Fig. 15. Measured SFDR/SNDR versus input frequency.

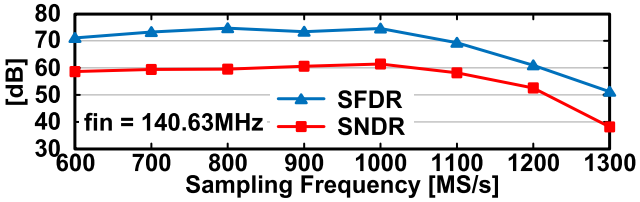

Fig. 16. Measured SFDR/SNDR versus sampling rate at low input frequency.

As shown from the analysis of the temperature compensation scheme in Section V-B, the bias voltage V_C is identified through one-time foreground calibration and a two-point temperature test is used to compensate the process variation. The measured dynamic performance versus temperature is shown in Fig. 17. According to the simulation results and analysis of Section V-B, the gain error of RA1 limits the overall accuracy of the three-stage ADC, and the estimated gain error of RA1 is in the range of +3.5% to −10% over a temperature between 0 °C and 80 °C. With compensation, the measured SNDR and SFDR from 0 °C to 80 °C are maintained above 56.2 and 68 dB, respectively, which reflect that the gain error of RA1 is reduced to less than ±2.3%.

The ADC consumes 7.6-mW power (excluding the input buffer) running at 1 GS/s with a 1-V supply, resulting in a 9.28 fJ/conversion-step Walden FoM and 168.2-dB Schreier FoM. The power breakdown is presented in Fig. 18, where

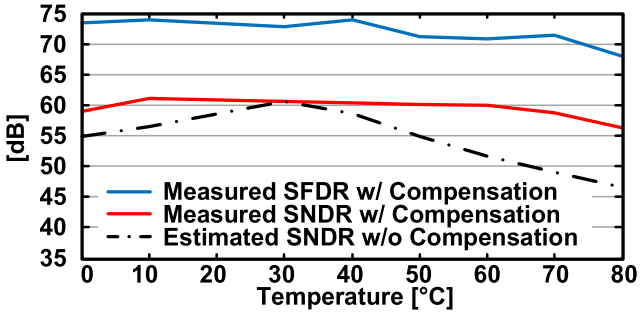

Fig. 17. Measured SFDR/SNDR versus temperature.

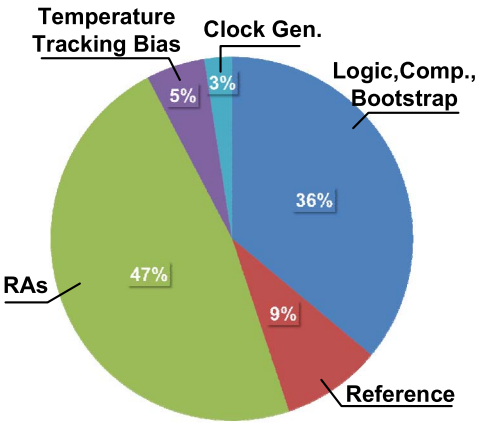

Fig. 18. Measured power breakdown.

the RAs consume almost half of the power due to their short amplification time and low-noise requirements. Table II summarizes the ADC performance and compares this article against the state-of-the-art single-channel designs with similar speed and SNDR. This article achieves an excellent energy efficiency and FoM with a good temperature stability.

VII. Conclusion

This article presented a single-channel 12-b 1 GS/s SAR-assisted pipelined ADC with a three-stage architecture. The open-loop RAs, designed with dynamic and complete-settling behavior, are power-efficient and immune to jitter. The cascade amplification topology is used to avoid large CDAC in the backend stage, leading to fast residue amplification and SAR conversion. A low-cost inter-stage gain compensation is realized by a complementary temperature feature with only a current bias circuit. The ADC demonstrates above 9-b ENOB over the temperature range from 0 °C to 80 °C. It achieves 60-dB SNDR for a Nyquist input at 1 GS/s and only consumes 7.6-mW power. The Walden FoM and Schreier FoM are 9.3 fJ/conversion-step and 168.2 dB, respectively.

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He has been with DECE/IST, University of Lisbon since October 1980. Since 1992, has been on leave from the University of Lisbon and with DECE, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair Professor since August 2013. He was the Dean of the Faculty from 1994 to 1997 and has been a Vice Rector of UM since 1997. From September 2008 to August 2018, he was the Vice Rector of research), and from September 2018 to August 2023, he is the Vice Rector of global affairs. He created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in January 2011 to State Key Laboratory (SKLAB) of China (the 1st in Engineering in Macao), being its Founding Director. He was the Founding Chair of UMTEC (UM company) from January 2009 to March 2019, supporting the incubation and creation in 2018 of Digifluidic, the first UM Spin-Off, whose CEO is a SKLAB Ph.D. graduate. He was also a Co-Founder of Chipidea Microelectronics, Macao (now Synopsys) in 2001/2002. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and, in UM, has supervised (or co-supervised) 46 theses, Ph.D. (25) and masters (21). He has coauthored seven books, 11 book chapters, 497 papers, in scientific journals (184) and in conference proceedings (313), and other 64 academic works, in a total of 612 publications. He holds 33 patents, USA (30) and Taiwan (3).

Dr. Martins was the Founding Chair of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair of the IEEE Asia-Pacific Conference on CAS—APCCAS'2008, the Vice President (VP) of Region 10 (Asia, Australia and Pacific) from 2009 to 2011 and the VP of the World Regional Activities and Membership of IEEE CASS from 2012 to 2013, an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, and a nominated Best Associate Editor from 2012 to 2013. He was also a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, 2018—Chair, and 2019; the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014; and the IEEE CASS Nominations Committee from 2016 to 2017. Plus, he was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016, receiving the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He was also the VP from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities (AULP), and received two Macao Government decorations: the Medal of Professional Merit (Portuguese, 1999) and the Honorary Title of Value (Chinese, 2001). In July 2010, he was elected, unanimously, as the Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia.