A 7.2 mW 75.3 dB SNDR 10 MHz BW CT Delta-Sigma Modulator Using Gm-C-Based Noise-Shaped Quantizer and Digital Integrator

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Abstract

A 3rd order continuous-time delta-sigma modulator using a Gm-C based noise-shaped integrating quantizer (NSIQ) with a digital back-end integrator is presented in this paper. By incorporating the back-end digital integrator, the conventional tradeoff between resolution and speed in time-based quantization is alleviated. Therefore by using only three clock edges and a low-power Gm-C, effective 4-bit quantization is achieved which also provides first order noise-shaping. The zero-crossing comparator is replaced by a preamplifier and three latches. The proposed modulator was fabricated in a 0.13µm CMOS process with an active area of 0.08mm^2. It operates at 640 MHz and achieves a peak SNDR of 75.3 dB and a peak SFDR of 94.1 dB in a 10 MHz bandwidth while consuming 7.2 mW from a 1.2V power supply.

Introduction

Employing quantizers with noise shaping property in delta-sigma modulators (DSMs) such as the VCO-based quantizer and the noise-shaped integrating quantizer (NSIQ) [1] is an attractive solution to reduce the power consumption compared to traditional quantizers (such as flash) and to provide an extra order of noise-shaping. However, time based quantizers suffer from speed/resolution tradeoff. For instance, in a conventional NSIQ, a counting clock speed of $2^N f_s$ is needed to achieve N-bit quantization. Therefore, the maximum speed will be limited by the NSIQ's counting clock.

In this paper, we propose a continuous-time (CT) delta-sigma analog-to-digital converter (ADC) using Gm-C based NSIQ followed by a digital integrator. The dual-slope nature of the proposed Gm-C NSIQ drastically reduces the linearity requirements of the Gm-C circuitry, which also serves as an active-adder. In addition, utilizing the digital integrator at the backend of the loop relieves the speed requirement of the quantizer. With the aid of bi-directional discharging scheme and the digital integration, the proposed Gm-C based NSIQ provides effective 4-bit of quantization and provides an extra order of noise-shaping only by using three counting clock edges and three corresponding latches.

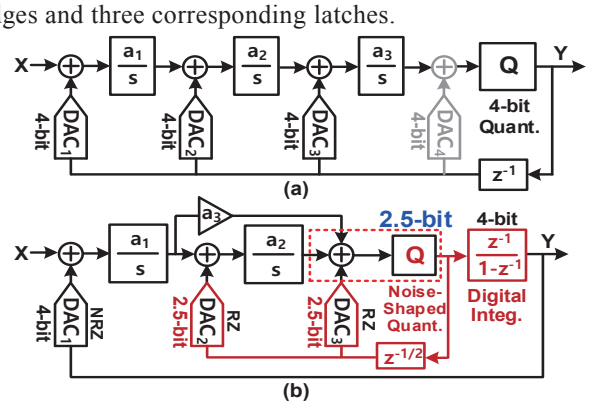

Fig. 1 Block diagrams of (a) a conventional DSM and (b) the proposed DSM using back-end digital integrator [2].

Proposed Architecture

In a traditional DSM shown in Fig. 1(a), the quantizer has to process both the signal and filtered quantization noise. To overcome the tradeoff between speed and resolution in NSIQ, a delayed digital integrator is placed at the back-end of the loop, as shown in Fig. 1(b). This structure comes with several advantages over that of the conventional DSM. First, the input of the quantizer is effectively the differentiated version of that of the traditional DSM. Therefore, the signal amplitude is suppressed, allowing to remove the several quantizer levels [2]. This concept is illustrated in Fig. 2 (a) and (b). In the proposed design, the digital integrator increases the 2.5-bit output of the quantizer to 4-bit final output of the DSMs. Thus, the quantizer effectively acts as a 4-bit quantizer and enhances the signal-to-noise ratio (SNR) and stability. The second benefit is the reduced hardware and number of levels for the internal DACs of the modulator. In this structure, the internal DACs are operated by the output of the quantizer instead of the integrated one, therefore, internal DACs (DAC_2 and DAC_3 in Fig. 1(b)) use only 6 unit elements (2.5-bit). Third, the linearity requirement of the quantizer is alleviated because the quantizer only deals with differentiated signals.

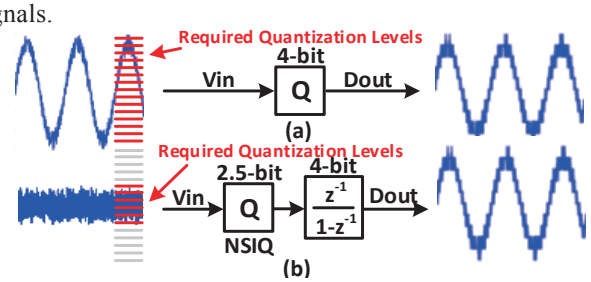

Fig. 2 Required quantization levels of (a) a conventional DSM and (b) the proposed DSM.

Gm-C-Based NSIQ

The quantizer consists of a Gm-C integrator and a pre-amplifier followed by only 3 dynamic latches with control logic for 7 quantization levels using the bidirectional discharging [1] as shown in Fig. 3(a). In the sampling phase, the input signals of the loop filter and the DAC_3 for excess loop delay compensation are summed through G_{m1} and G_{m2} onto C_{gm}. In the discharging phase, both G_{m1} and G_{m2} will be combined to create one equivalent G_m. A combination of a current source and a resistor (R_{dis}) is used to set the discharging slope according to the desired discharging direction. A simple differential pair with resistive degeneration is used for the Gm cells as shown in Fig. 3(b) to prove the efficiency and relaxed linearity requirements of the proposed Gm-C based NSIQ.

The operation principle of the quantizer is shown in Fig. 3(c). In this architecture, the continuous-time comparator (for zero-crossing detection) is replaced by a low-power pre-amplifier and three dynamic latches. The direction of discharge is read at the beginning of the discharge phase. Three delayed version of clock edges will trigger each dynamic

latch consecutively. If the zero crossing has occurred (i.e. the output of the latch has different polarity compared to the discharge direction polarity), the discharging will be terminated and the residue voltage will be kept at the output capacitance of the Gm-C integrator. The discharging stops if the output of one of the three latches changes polarity.

Unlike the opamp-based NSIQ, the charging and discharging on the output capacitance (node Vq on C_{gm} in Fig. 3(a)) is performed using the same Gm and the same slope. This results in a true dual-slope behavior of the NSIQ. With the relaxed linearity requirement and reduced number of quantization levels offered by the digital integrator, the Gm-C based NSIQ operates at a higher speed with lower power compared to the active-RC one. In addition, this quantizer not only provides a first order quantization noise shaping, but it also serves as an active adder.

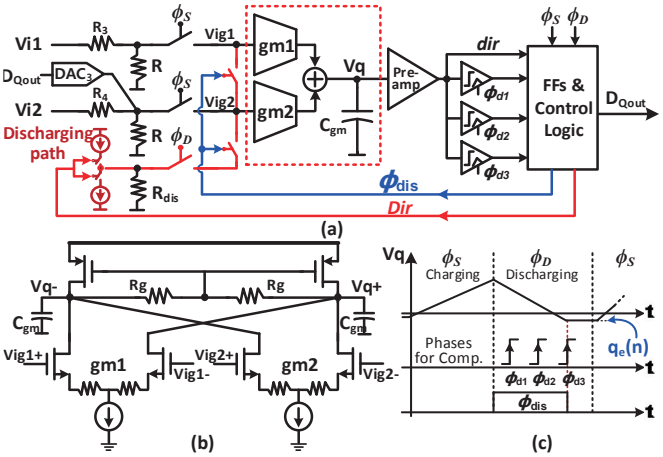

Fig. 3 (a) The proposed Gm-c-based NSIQ structure (b) the schematic of the Gm-C (c) a timing example of the quantizer.

The simplified schematic of the proposed 3rd order CT DSM is shown in Fig. 4. The single-ended implementation is illustrated for simplicity. In this modulator, each opamp consists of three amplifying stages with two feedforward stages. The digital integrator is implemented using an up/down accumulator based on a barrel shift register. DAC_1 employs cascoded current-source elements and is optimized for 15-bit linearity.

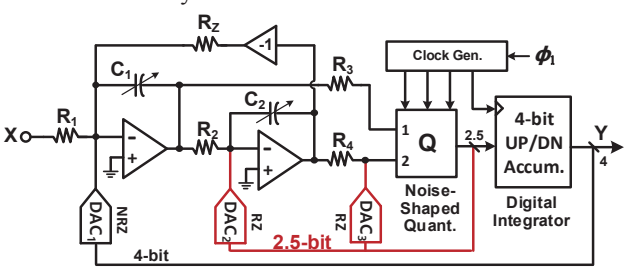

Fig. 4 Schematic of the proposed 3rd order CT DSM.

Measurement Results

The proposed CT DSM was fabricated in a 0.13 µm CMOS process with an active area of 0.08 mm^2. The small active area is a direct result of the reduced sizes of the DAC_2 and DAC_3, and the only two analog integrators. Clocked at 640 MHz, the modulator consumes 7.19 mW from a 1.2 V supply, of which 4.69 mW is drawn by the analog part, 1.01 mW by the digital circuitry, and 1.49 mW by the clock generation. The achieved minimal power consumption shows the effectiveness of the proposed architecture with the Gm-C-based NSIQ and the digital integrator.

Fig. 4 plots the 65k windowed FFT spectrum of the output with a -0.75 dBFS 1.9 MHz input sinewave. In a 10 MHz BW, the proposed DSM achieves peak SNDR, SNR, and SFDR of 75.3 dB, 75.5 dB, and 94.1 dB, respectively. The measured SNR and SNDR as a function of the input amplitude are shown in Fig. 5(left), and the die photograph is shown in Fig. 5(right). The measured dynamic range is 78.5 dB. Table I summarizes the measured performance and compares with the state-of-the-art DSMs with similar BW and resolution. The proposed DSM achieves a Walden FOM_{Wa} of 75.9 fJ/conv-step and a Schreier FOM_{Sch} of 169.9 dB.

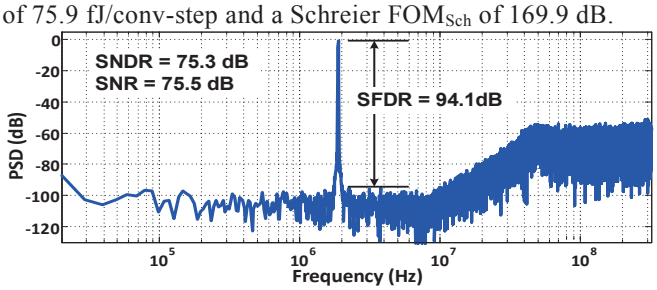

Fig. 4 Measured output spectrum with 1.9MHz input.

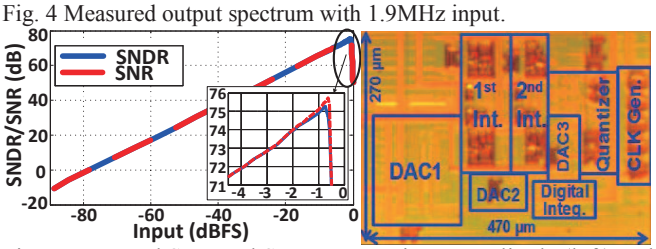

Fig. 5 Measured SNR and SNDR versus input amplitude (left) and die photo (right).

Table I. Performance Summary and comparison

	This Work	[3]	[4]	[5]	[6]
Technology (nm)	**130**	90	40	28	90
Supply (V)	**1.2**	1.4/1.0	1.1	1.2/1.5	1.2/1.4
Fs (MHz)	**640**	600	300	640	300
Bandwidth (MHz)	**10**	10	10	18	8.5
DR (dB)	**78.5**	83.5	70.6	78.1	69.3
Peak SNDR (dB)	**75.3**	78.3	70.0	73.6	67.2
Peak SNR (dB)	**75.5**	83	70.6	75.4	69.3
Peak SFDR (dB)	**94.1**	85	81.3	80.5	71
Power (mW)	**7.19**	16	2.57	3.9	4.3
Active Area (mm^2)	**0.08**	0.36	0.05	0.08	0.12
FOMWa (fJ/conv)	**75.9**	120	50	27.7	135
FOMSch (dB)	**169.93**	171.5	166.5	174.7	162.3

$FOM_{Wa}=P/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$, $FOM_{Sch}=DR+10Log_{10}(BW/P)$

References

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