# A Cryo-CMOS PLL for Quantum Computing Applications

Jiang Gong, *Student Member, IEEE*, Edoardo Charbon, *Fellow, IEEE*, Fabio Sebastiano, *Senior Member, IEEE*, and Masoud Babaie, *Senior Member, IEEE*

***Abstract*— This article presents the first cryogenic phase-locked loop (PLL) operating at 4.2 K. The PLL is designed for the control system of scalable quantum computers. The specifications of PLL are derived from the required control fidelity for a single-qubit operation. By considering the benefits and challenges of cryogenic operation, a dedicated analog PLL structure is used so as to maintain high performance from 300 to 4.2 K. The PLL incorporates a dynamic-amplifier-based charge-domain sub-sampling phase detector (PD), which simultaneously achieves low phase noise (PN) and low reference spur, thanks to its high phase-detection gain and minimized periodic disturbances on the voltage-controlled oscillator (VCO) control. Fabricated in a 40-nm CMOS process, the PLL achieves −78.4-dBc reference spur, 75-fs rms jitter, and 4-mW power consumption at 300 K when generating a 10-GHz carrier, leading to a −256.5-dB jitter-power FOM. At 4.2 K, the PLL synthesizes 9.4- to 11.6-GHz tones with an rms jitter of 37 fs and a reference spur of −69 dBc while consuming 2.7 mW at 10 GHz.**

***Index Terms*— Charge-sampling, cryo-CMOS, cryo-CMOS PLL, dynamic amplifier, dynamic-amplifier-based phase detector (PD), in-band phase noise (PN), low jitter, phase-locked loop (PLL), quantum computing, reference spur.**

## I. Introduction

PRACTICAL quantum computing (QC) applications require the manipulation and readout of thousands or even millions of quantum bits (qubits) to execute quantum algorithms [1], [2]. However, qubit state manipulation and readout typically require the generation and acquisition of high-accuracy and low-noise signals (e.g., microwave bursts). A major contemporary obstacle to realizing a large-scale and practical quantum computer is the sheer interconnect complexity between the milli-kelvin qubits placed in a dilution refrigerator and the room temperature (RT) controller. To address this challenge, [3] proposes to place a fully integrated cryogenic CMOS (cryo-CMOS) control system operating in close vicinity to the qubits. Eventually, the cryo-CMOS controller could be co-integrated with advanced "hot" qubits operating at ∼1 K [4] on the same die or package, thus eliminating the wiring issue and offering a compact solution toward the realization of large-scale quantum computers. Toward this goal, developing building blocks for QC applications at cryogenic temperatures (CTs) (i.e., 1–4.2 K) has been an active field of research over the past few years [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25].

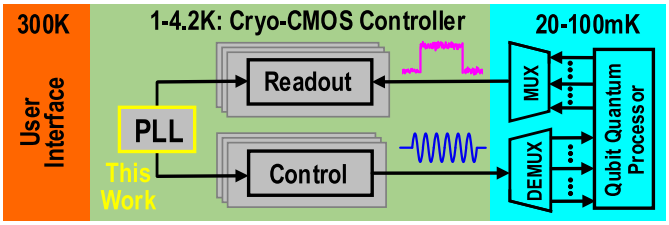



Fig. 1. Simplified block diagram of a cryogenic controller interfacing a quantum processor [3].

Although a cryo-CMOS receiver for the gate-based RF readout of spin qubits [22] and cryo-CMOS burst generators for the control of superconducting and spin qubits [23], [24], [25] have been presented, they rely ON an OFF-chip local oscillator (LO) operating at RT to down/up-convert the desired signals. This requires a complex and high-frequency OFF-chip LO distribution network and a power-hungry ON-chip LO driver (∼7 mW in [25]). Moreover, in a large-scale quantum computer, many separate LOs would be required, which necessitates the use of numerous cables, thus limiting the system form factor and increasing the risk of crosstalk among various signals. Consequently, as shown in Fig. 1, it is beneficial to generate the LO at CT as well. However, the minimum operating temperature of prior-art phase-locked loops (PLLs) is limited to 77 K [26], and only the performance of stand-alone voltage-controlled oscillators (VCOs) at 4.2 K has been reported [10], [11], [12], [13]. Hence, there is a lack of PLLs operating at 4.2 K and meeting the performance requirements for the qubit control. Nevertheless, designing a cryo-CMOS PLL for QC applications presents several challenges. First, low phase noise (PN) and low reference spur ($S_{REF}$) are simultaneously required to ensure that the PLL does not limit the overall control fidelity of the qubits. Second, the PLL must operate at CT. Yet, from RT to CT, the parameters of transistors vary significantly and no mature device models are available at CT. For example, compared with RT, the

Manuscript received 15 February 2022; revised 11 August 2022; accepted 7 November 2022. Date of publication 29 November 2022; date of current version 25 April 2023. This work was supported in part by Intel Corporation and in part by the Netherlands Organization for Scientific Research under Project 17303. This article was approved by Associate Editor Jaeha Kim. *(Corresponding author: Jiang Gong.)*

Jiang Gong and Fabio Sebastiano are with the Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CJ Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands (e-mail: gongjiangjlu@gmail.com).

Edoardo Charbon is with the Kavli Institute of Nanoscience, 2628 CJ Delft, The Netherlands, and also with the École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland.

Masoud Babaie is with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with QuTech, 2628 CD Delft, The Netherlands.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3223629.

Digital Object Identifier 10.1109/JSSC.2022.3223629

0018-9200 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

threshold voltage of transistors is expected to increase by ~150 mV, and the carrier mobility can increase up to 2× at CT [27]. Although the ON-resistance of a transmission gate at CT reduces when the input voltage is close to the supply or ground level, it can increase by more than two orders of magnitude when the input voltage is near the middle of the supply voltage. This could lead to severe problems in a sampling circuit [19]. In addition, transistors exhibit much worse matching properties at CT [25], degrading the linearity of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) and matching of current sources. Finally, as the cryogenic refrigerator cooling power is limited, a low power consumption ($P_{\rm dc}$) is necessary to control more qubits.

This work advances the prior art by introducing the first cryo-CMOS PLL operating at 4.2 K. A new charge-domain sub-sampling phase detector (PD) based on the operation of a dynamic amplifier is leveraged to meet the required specifications. At 10 GHz, the cryo-CMOS PLL achieves 37-fs rms jitter and −69-dBc $S_{\rm REF}$ while consuming 2.7 mW, corresponding to a PLL FOM of −264 dB.

This article is an expanded version of [17] and is organized as follows. The PLL specifications are derived in Section II. Section III discusses the device modeling for circuit design at 4.2 K and the most appropriate PLL structure for QC applications. In Section IV, the theoretical analysis and design considerations of the proposed PD are presented. Section V describes the PLL architecture, its phase-domain model, and cryogenic circuit design considerations. Finally, we present the measurement results in Section VI and conclude this article in Section VII.

## II. PLL Specifications

### A. PN Requirements

A quantum computer operates by processing the information stored in qubits. Any single-qubit state can be pictorially represented by a 3-D unit vector on the Bloch sphere. The qubit state manipulation corresponds to a vector rotation on the Bloch sphere, which is typically realized by applying microwave bursts to the superconducting and spin qubits [2], [23], [24], [25]. The rotation speed and rotation angle can be controlled by the amplitude and duration of the microwave bursts, respectively. Unfortunately, due to the mismatch between the instantaneous PLL frequency and the qubit resonant frequency, the qubit state would be subject to unwanted rotations, creating control error and thus degrading qubit fidelity ($F$).

For a single-qubit operation, the infidelity ($1-F$) due to the PLL's frequency noise [$\mathcal{L}_\phi(f)\cdot f^2$] can be expressed as

$$1-F=\int_0^{+\infty} 2\cdot\frac{\mathcal{L}_\phi(f)\cdot f^2}{f_R^2}\cdot|H_{\rm LO}(f)|^2{\rm df} \tag{1}$$

where $\mathcal{L}_\phi(f)$ is the PLL's PN, $f_R$ is the qubit rotation speed, and $H_{\rm LO}(f)$ is the intrinsic qubit filter function [28]. By considering a rotation angle ($\theta$) of $\pi$, the worst case squared magnitude of $H_{\rm LO}(f)$ can be found as [28]

$$|H_{\rm LO}(f)|^2=\frac{\left(1+\cos\left(\frac{f}{f_R}\pi\right)\right)\cdot\left(1+\left(\frac{f}{f_R}\right)^2\right)}{2\left(1-\left(\frac{f}{f_R}\right)^2\right)^2} \tag{2}$$

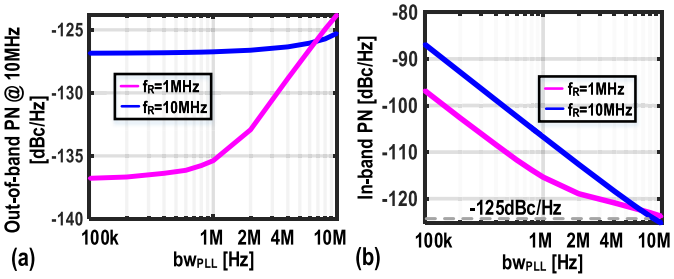



Fig. 2. Theoretically required (a) out-of-band PN at a 10-MHz offset and (b) in-band PN versus $\rm bw_{PLL}$ by considering a control fidelity of 99.999% and qubit rotation speed of 1 and 10 MHz.

which shows a first-order low-pass response with a dc gain of 1- and 3-dB bandwidth of ~1.9 $f_R$ and exhibits high-frequency notches. This indicates that a qubit has a different sensitivity to PLL's PN at different frequency offsets, and the choice of $f_R$ has a substantial impact on the control fidelity.

For the sake of simplicity, a type-I PLL is considered here. Suppose that PLL's PN has the following form:

$$\mathcal{L}_\phi(f)=\begin{cases}\beta/{\rm bw}_{\rm PLL}^2, & f\le {\rm bw}_{\rm PLL}\\ \beta/f^2, & f\ge {\rm bw}_{\rm PLL}\end{cases} \tag{3}$$

where $\beta$ is a constant coefficient in $\rm Hz^2/Hz^1$ and $\rm bw_{PLL}$ is the PLL bandwidth. Equation (3) neglects the flicker noise of the entire PLL[2] and assumes that the in-band PN of the PLL ($\beta/{\rm bw}_{\rm PLL}^2$) is flat and the out-of-band PN ($\beta/f^2$) is dominated by the VCO. By substituting (2) and (3) into (1), the infidelity for a typical qubit rotation speed higher than 0.1 MHz could be solved numerically and may be estimated by

$$1-F\approx\frac{1.6\pi\beta}{f_R}\cdot\frac{1}{1+0.5({\rm bw}_{\rm PLL}/f_R)^{1.6}}. \tag{4}$$

For fault-tolerant operations, a qubit infidelity well below 0.1% is typically required [29]. Therefore, the PLL targets an infidelity of 0.001% to avoid limiting the inherent fidelity of a qubit. The qubit rotation speed is currently ~1 MHz and will be extended to 10 MHz in the future [29]. Based on those considerations, Fig. 2(a) and (b), respectively, depicts the theoretically required out-of-band PN at a 10-MHz offset and in-band PN as a function of $\rm bw_{PLL}$ for a 99.999% fidelity. Since $P_{\rm dc}$ of a high-performance PLL is typically dominated by the VCO, it is thus beneficial to reduce the VCO's $P_{\rm dc}$ by increasing the out-of-band PN, which could be realized using a larger $\rm bw_{PLL}$ [see Fig. 2(a)]. However, as depicted in Fig. 2(b), a larger $\rm bw_{PLL}$ would require a more stringent in-band PN, demanding lower PN contributed by the PLL reference clock buffer and loop components. By considering an $f_R$ of 1 MHz[3] and a reference frequency ($F_{\rm REF}$) of 100 MHz, a $\rm bw_{PLL}$ of 4 MHz is selected to relax the VCO PN requirement. Further increasing $\rm bw_{PLL}$ would degrade the PLL stability and spurious performance and require a tougher in-band PN. The resulting in-band PN, PN at a 10-MHz offset, and rms jitter

[1] $\beta$ has the same unit as the psd of frequency noise.

[2] When the flicker noise is included, the accurate infidelity could be obtained by simulation based on (1).

[3] An $f_R$ of 1 MHz is targeted as the required $\beta$ and $\beta/{\rm bw}_{\rm PLL}^2$ are more stringent given a realistic $\rm bw_{PLL}$.

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

should be below −121 dBc/Hz, −129 dBc/Hz, and 60 fs when synthesizing a 10-GHz carrier.

### B. Frequency Inaccuracy Requirement

Apart from the frequency noise, the deterministic frequency inaccuracy ($f_{\text{err}}$) between the applied microwave burst and qubit resonant frequency also degrades the fidelity. For a $\theta$ of $\pi$, the infidelity incurred due to $f_{\text{err}}$ is [28]

$$1-F = \frac{f_{\text{err}}^2}{f_R^2}. \tag{5}$$

Considering an infidelity of 0.001% and a qubit rotation speed of 1 MHz, the required frequency inaccuracy $f_{\text{err}}$ should be below 3 kHz. At first glance, a fractional-$N$ PLL might be required to achieve the required $f_{\text{err}}$. However, it is challenging to design a low-jitter fractional-$N$ PLL with low power consumption. Instead, a power-efficient approach would be to use an individual numerically controlled oscillator (NCO) to synthesize the required *fractional* frequency of each qubit [2]. Consequently, a single power-efficient integer-$N$ PLL can be used to upconvert the qubits' baseband signals and address multiple qubits simultaneously.

### C. $S_{REF}$ Requirement

To facilitate scalability and manipulate more qubits, frequency-division multiplexing (FDM) could be used, where multiple qubits share a single microwave control line. However, a PLL typically generates spurious tones, which could be at the resonant frequencies of the unaddressed qubits. Due to those spurious tones, the states of the unaddressed qubits would also experience undesired rotations, degrading the fidelity. The infidelity due to $S_{\text{REF}}$ is [29]

$$1 - F = \frac{\pi^2}{4} \cdot 10^{S_{\text{REF}}/10}. \tag{6}$$

This translates to a −54-dBc $S_{\text{REF}}$ requirement when a 99.999% fidelity is targeted.

## III. Device Modeling for Circuit Design at 4.2 K and Appropriate PLL Architecture for QC Applications

### A. Device Modeling for Circuit Design at 4.2 K

Since standard foundry process development kits (PDKs) do not offer device models for CT, the PLL design was based on the measured characteristics of devices from the target 40-nm CMOS process.

Transistors exhibit large deviations in their parameters, such as higher threshold voltage, higher subthreshold slope, higher mobility, worse mismatch, and lower output impedance in saturation region [27], [30], [31]. Based on the measured drain current versus gate–source and drain–source voltage, a lookup table-based Verilog-A model was built to capture the dc behavior of transistors at 4.2 K. This model helps predict $K_{\text{PD}}$ and other PLL loop parameters at 4.2 K through transient and dc simulations.

Compared with RT, the measured quality factor of a spiral inductor and an MOM capacitor shows a ∼2.5× increase due to higher metal conductivity and lower loss in the substrate [32] at 4.2 K. Nevertheless, the inductance and capacitance change marginally (∼5%) from RT to 4.2 K [32]. Those variations were accounted for by increasing the conductivity of metals (5×) and the substrate resistivity (800×) in both the EM and parasitic extraction tools, which were used to predict the VCO performance at 4.2 K. While the sheet resistance of the unsilicided polysilicon resistor is fairly constant over temperature, the silicided counterpart exhibits ∼2.5× resistance reduction from RT to 4.2 K. Hence, the loop filter can be designed to be relatively immune to temperature variations by adopting MOM capacitors and unsilicided polysilicon resistors.

The thermal noise of a long-channel MOS transistor is typically modeled by

$$S_{n,\text{th}}(f) = 4\text{KT}_{\text{ch}}\gamma\, g_{\text{ds0}} \tag{7}$$

where $T_{\text{ch}}$ is the channel temperature, $\gamma$ is the noise coefficient, and $g_{\text{ds0}}$ is the channel conductance under 0-V drain–source voltage. Compared with RT, one would expect an 18.5-dB noise reduction at 4.2 K. Unfortunately, based on the study presented in [33], even by dissipating a moderate 0.8-mW $P_{\text{dc}}$, a transistor measuring 17 $\mu$m/40 nm is expected to exhibit a $T_{\text{ch}}$ of ∼30 K due to the self-heating at 4.2 K, limiting the noise improvement to ∼10 dB. On the other hand, if a short-channel device (e.g., L < 100 nm) is required to optimize speed and to minimize parasitic capacitance, the total channel noise contains a large portion of a temperature-independent shot noise, which can be empirically modeled by

$$\overline{i_{n,\text{ch}}^2} = 4\text{KT}_{\text{ch}} g_{\text{ds0}} \cdot \xi \cdot (1-\nu)^2 + 2\text{qI}_D \cdot \nu^2 \tag{8}$$

where $\xi$ is the noise coefficient, and $\nu^2$ is the Fano factor and a function of the channel length [34], [35], [36]. At RT, ∼25% of the total channel noise is estimated to be shot noise in a 40-nm device [34]. Hence, we assume that $\xi \cdot (1-\nu)^2 = 1$ and $\nu^2 = 0.5$ for a 40-nm channel length transistor in this article. Taking both the thermal and shot noise into account, the channel white noise is also modeled in the lookup table-based Verilog-A model at 4.2 K. By considering $T_{\text{ch}} = 30$ K, the channel noise reduction is limited to 4.8 dB at 4.2 K, where the shot noise contributes up to 77% of the noise. Unlike thermal noise, there is no indication of a temperature-dependent mechanism for flicker noise [37], [38].

### B. Appropriate PLL Architecture for QC Applications

As mentioned in Section II-B, an integer-$N$ PLL is required to convert the desired signals. This section will investigate the most appropriate integer-$N$ PLL architecture for QC applications by considering the benefits and challenges of cryogenic operation.

A digital PLL [39] is less attractive at CT as the quantization noise (QN) of a time-to-digital converter (TDC), and a digitally controlled oscillator (DCO) does not significantly scale with temperature. First, the resolution of a simple TDC typically equals a gate delay, which is estimated to reduce by ∼30% from 300 to 4.2 K [40]. The resulting in-band PN improvement is limited to 3 dB. Second, compared with RT,

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

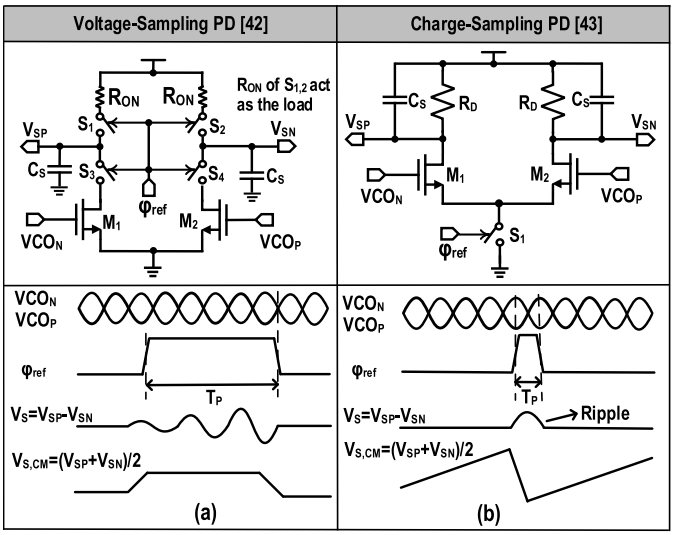



Fig. 3. Schematics and conceptual waveforms of (a) voltage-sampling PD [42] and (b) charge-sampling PD [43].

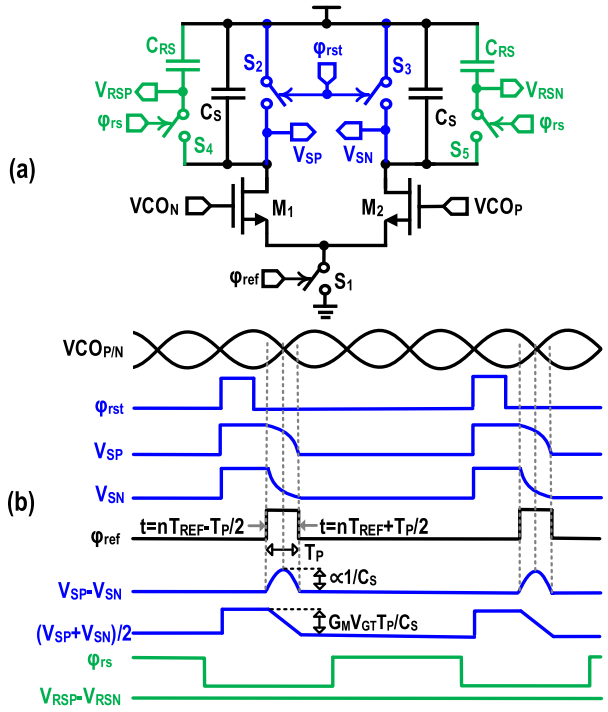



Fig. 4. (a) Simplified schematic and (b) conceptual waveforms of a DAPD.

the measured inherent PN of an oscillator improves substantially (∼10 dB) at 4.2 K [10]. Yet, the measured frequency resolution of a DCO is weakly temperature-dependent. Thus, the PN introduced by the finite resolution of the DCO does not appreciably improve over temperature. Hence, the total PN of a DCO could be entirely dominated by its QN, limiting the PLL's out-of-band PN. While a bang-bang PLL relaxes the PD's resolution requirement [41], its locking behavior and bandwidth are strongly noise-dependent and difficult to predict at CT due to the lack of mature noise models.

An analog charge-pump PLL (CPPLL) [44] could be used at CT due to thermal noise reduction and the absence of QN introduced by the PD and oscillator. However, the CPPLL loop components (i.e., charge pump and divider) consume high $P_{\rm dc}$ and introduce high in-band PN. Furthermore, the mismatch of active devices becomes much worse at CT [31], which degrades the matching between the charge pump's "up" and "down" current branches, resulting in a higher $S_{\rm REF}$. An injection-locked clock multiplier (ILCM) could generate a low-noise clock efficiently by eliminating the loop components. Yet, its PN and $S_{\rm REF}$ performance are severely degraded if the free-running frequency of the oscillator is not tuned precisely to the desired frequency over voltage and temperature variations. Hence, an ILCM must incorporate complex digital calibration [45], [46], [47], [48], resulting in high design complexity.

Analog PLLs based on the voltage-sampling [42], [49], [50], [51], [52], [53], [54] or charge-sampling [43], [55] concepts are more promising candidates at CT [see Fig. 3(a) and (b)], as they can achieve low in-band PN due to their high phase-detection gain ($K_{\rm PD}$). Nevertheless, a voltage-sampling PD (VSPD) requires an RF output bandwidth to properly track the oscillator voltage and a large sampling capacitance ($C_S$) to achieve a low in-band PN, thus demanding a relatively large $P_{\rm dc}$. Besides, compared with RT, the on-resistance of the sampling switches ($S_{3,4}$) dramatically increases at CT as the dc voltage at the sampler output is typically designed to be near the middle of the supply voltage.

Hence, the sampler output voltage swing could be severely compromised, thus degrading $K_{\rm PD}$ and in-band PN. Moreover, in order not to degrade $K_{\rm PD}$, the reference pulsewidth ($T_P$) should be at least a few oscillator cycles ($T_{\rm VCO}$) to ensure that the VSPD output reaches its steady-state before the sampling instants. This limits the minimum achievable $S_{\rm REF}$ due to the oscillator's disturbance during $T_P$.

The output bandwidth and $T_P$ can be much lower in a charge-sampling PD (CSPD) introduced in [43] and [55]. Nevertheless, as depicted in Fig. 3(b), even in the locked condition, the differential-mode (DM) output voltage of the CSPD experiences a ripple during $T_P$, thus degrading the minimum achievable $S_{\rm REF}$. Besides, the load resistor ($R_D$) and $C_S$ should be very large to simultaneously improve $K_{\rm PD}$ and $S_{\rm REF}$, thus compromising the PLL phase margin, especially when a wide bandwidth is used due to a considerable $R_D C_S$ delay. Moreover, the CSPD output common-mode (CM) voltage varies significantly over one reference period ($T_{\rm REF}$) [see Fig. 3(b)], thus demanding a stringent requirement on the CM rejection of the next stages. To improve on those limitations, we introduce a charge-mode sub-sampling PLL that incorporates a new PD based on the operation of a dynamic amplifier.

## IV. Dynamic-Amplifier-Based PD

### A. Operation

Fig. 4(a) and (b) illustrates the schematic and conceptual waveforms of the dynamic-amplifier-based PD (DAPD). The circuit begins in the reset mode, with the output nodes $V_{\rm SP}$ and $V_{\rm SN}$ precharged to $V_{\rm DD}$ when the reset clock ($\varphi_{\rm rst}$) is high. This

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

aims to clear the memory of the previous operation and set a high CM voltage for the next mode. When the reference clock ($\varphi_{\text{ref}}$) goes high, the circuit enters the phase-detection mode. The transconductance devices ($M_{1,2}$) are instantly turned ON, drawing a DM current of $G_M A_{\text{VCO}} \sin(\omega_{\text{VCO}} t + \phi_e)$ from $C_S$, where $G_M$ is the large-signal transconductance of $M_{1,2}$ and $\phi_e$ is the instantaneous phase error between the zero-crossing of the VCO and the middle of $\varphi_{\text{ref}}$. Note that the on-resistance of the sampling switch $S_1$ and reset switches $S_{2,3}$ reduces at CT due to the large overdrive voltage. Hence, compared with a VSPD, a DAPD benefits more from the cryogenic operation. The operation of a DAPD is similar to that of a dynamic amplifier [56], [57], [58] or a charge-steering amplifier [59], [60], which has demonstrated excellent power efficiency and noise performance when used in data converters and wire line transceivers [56], [57], [58], [59], [60]. As will be demonstrated, the proposed DAPD can achieve low PN and high $K_{\text{PD}}$ with low $P_{\text{dc}}$ when incorporated into a PLL.

### B. Phase-Detection Gain

During the $n$th reference clock period ($nT_{\text{REF}}$), the DM current of $M_{1,2}$ can be modeled by

$$I_n(t) = G_M A_{\text{VCO}} \sin(\omega_{\text{VCO}} t + \phi_e) \cdot p_0\left(nT_{\text{REF}} + \frac{T_P}{2} - t\right) \tag{9}$$

where $p_0(t)$ is a deterministic sampling function and can be expressed by a unit step function $u$(t)

$$p_0(t) = u(-t + T_P) - u(-t). \tag{10}$$

The sampled DM voltage at the time instant $nT_{\text{REF}} + T_P/2$ is

$$\begin{aligned} V_S(n) &= V_{\text{SP}}(n) - V_{\text{SN}}(n) = \frac{2}{C_S} \int_{-\infty}^{+\infty} I_n(t) \text{dt} \\ &= V_C \int_{-\infty}^{+\infty} \sin(\omega_{\text{VCO}} t + \phi_e) p_0\left(nT_{\text{REF}} + \frac{T_P}{2} - t\right) \text{dt} \end{aligned} \tag{11}$$

where $V_C$ is defined as $2G_M A_{\text{VCO}}/C_S$.[4] If $\phi_e$ is small, by solving the integral of (11), $K_{\text{PD}}$ can be estimated by

$$K_{\text{PD}} = \frac{\overline{V_s}}{\phi_e} \approx \frac{4G_M A_{\text{VCO}} \sin(0.5\omega_{\text{VCO}} T_P)}{\omega_{\text{VCO}} C_S} \tag{12}$$

$K_{\text{PD}}$ is a periodic function of $T_P$ and reaches the maximum at $T_P = 0.5T_{\text{VCO}}$. Due to the sinusoidal dependence of $K_{\text{PD}}$ to $T_P$, $K_{\text{PD}}$ varies less than 30% even if $T_P$ varies from 0.25 to 0.75 $T_{\text{VCO}}$. Besides, based on the measured frequency of a ring oscillator, $T_P$ is expected to vary less than 40% from 300 to 4.2 K [27]. Therefore, $T_P$ may not need calibration over process, voltage, and temperature (PVT) variations. This property is similar to a CSPD in [43] due to the windowed-current integration. However, as listed in Table I, $K_{\text{PD}}$ of a DAPD is inversely proportional to $C_S$, which is in stark contrast to that of a CSPD in [43].

Fig. 5(a) and (b), respectively, shows the simulated and calculated $K_{\text{PD}}$ versus $F_{\text{VCO}}$ and $C_S$ by considering $(W/L)_{1,2} =$ $1.2\mu/40$ nm, $A_{\text{VCO}} = 0.45$ V, and $T_P = 30$ ps. The simulations closely match the presented theory if a reasonable $C_S$ value is used. Interestingly, even with a constant $T_P$ of 30 ps, $K_{\text{PD}}$ varies by less than 10% when $F_{\text{VCO}}$ changes between 5 and 10 GHz. In addition, compared with 300 K, the simulated $K_{\text{PD}}$ reduces ~20% at 4.2 K due to the increase in threshold voltage. A small $C_S$ is desired to achieve a high $K_{\text{PD}}$. However, as depicted in Fig. 4(b), the CM voltage of the DAPD drops during $T_P$. If $M_{1,2}$ enter the triode region due to this CM drop, $G_M$ and hence $K_{\text{PD}}$ would be potentially compromised. As a result, the simulated $K_{\text{PD}}$ deviates from the calculated value if a smaller $C_S$ is used [see Fig. 5(b)].

[4]For simplicity, the transconductance of $M_{1,2}$ is assumed to be constant.

TABLE I
COMPARISON BETWEEN A CSPD AND A DAPD

| | CSPD [43] | DAPD |
|---|---|---|
| $K_{\text{PD}}$ | $2A_{\text{VCO}} \cdot \frac{G_M R_D}{N\pi} \cdot \sin(0.5\omega_{\text{VCO}} T_P)$ | $\frac{4G_M A_{\text{VCO}}}{\omega_{\text{VCO}} C_S} \cdot \sin(0.5\omega_{\text{VCO}} T_P)$ |
| Intrinsic Delay | ~$2.5T_{\text{REF}}$ | $0.5T_P \approx 0.25T_{\text{VCO}}$ |
| PN | *Not* a function of $C_S$ | A function of $C_S$ |
| $S_{\text{REF}}$ | 1, Degraded by $C_S$ mismatch<br>2, High CMR of next stages required | 1, *Not* degraded by $C_S$ mismatch<br>2, High CMR of next stages *not* required |

Note that the last integral term in (11) results from the convolution of the sampling function and the transconductors' DM current. Hence, the complete spectrum of $V_S$ without considering the zero-order hold could be expressed as

$$V_S(f) = V_C \sum_{k=-\infty}^{+\infty} S(f - kF_{\text{REF}}) \cdot P_0(f - kF_{\text{REF}}) \tag{13}$$

where $S(f)$ is the spectrum of $\sin(\omega_{\text{VCO}} t + \phi_e)$, and $P_n(f)$ is the spectrum of $p_0(t)$ [61]. Since $\phi_e$ is typically very small when a PLL is locked, $S(f)$ can be estimated by

$$S(f) \approx \frac{1}{2}(\Phi(f - F_{\text{VCO}}) + \Phi(f + F_{\text{VCO}})) \tag{14}$$

where $\Phi(f)$ is the spectrum of $\phi_e$, and $F_{\text{VCO}}$ is the VCO frequency. As $P_0(f)$ is $T_P \cdot \text{sinc}(\pi f T_P) e^{-i\pi f T_P}$,

the spectrum of $V_S$ is

$$\begin{aligned} V_S(f) = V_C T_P \cdot \sum_{k=-\infty}^{+\infty} ((&\Phi(f - kF_{\text{REF}} - F_{\text{VCO}}) + \Phi(f - kF_{\text{REF}} \\ &+ F_{\text{VCO}})) \cdot \text{sinc}(\pi(f - kF_{\text{REF}})T_P) \cdot e^{-i\pi f T_P}). \end{aligned} \tag{15}$$

By ignoring the high-frequency aliasing components of $\Phi(f)$, (15) can be estimated by

$$V_S(f) \approx V_C \Phi(f) \sum_{p=\pm 1} \frac{\sin(\pi(f + p \cdot F_{\text{VCO}})T_P)}{\pi(f + p \cdot F_{\text{VCO}})} \cdot e^{-i\pi f T_P}. \tag{16}$$

Consequently, the intrinsic delay of a DAPD is $T_P/2$, which is very small compared with $T_{\text{REF}}$ and hence can be safely ignored. On the other hand, the narrowband nature of a CSPD

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

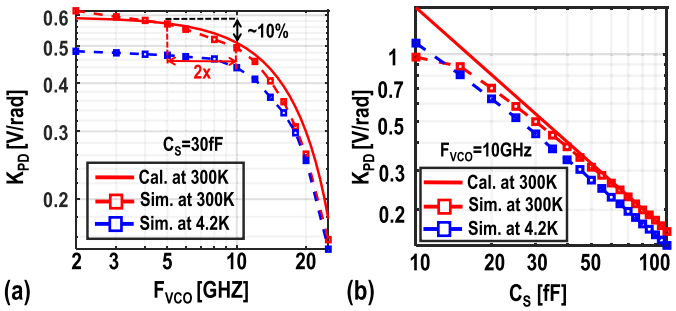



Fig. 5. Simulated and calculated $K_{PD}$ versus (a) $F_{VCO}$ and (b) $C_S$ with a $T_P$ of 30 ps at 300 and 4.2 K.

adds a significant loop latency due to the large $R_D C_S$ delay ($\sim 2.5 T_{REF}$ in [43]), degrading the PLL phase margin.

As depicted in Fig. 4(b), the DM voltage of the DAPD ($V_{SP} - V_{SN}$) experiences a voltage ripple due to the windowed-current integration, degrading $S_{REF}$. While a large $C_S$ could be used to reduce this ripple, the resulting $K_{PD}$ would be degraded. To this end, as shown in Fig. 4(a), an extra stage composed of capacitors $C_{RS}$ and switches $S_{4,5}$ is added to resample $V_{SP}$ and $V_{SN}$ after the phase comparison without compromising $K_{PD}$. The resampling also ideally eliminates the CM ripple at the DAPD output. As a result, a highly constant output voltage ($V_{RSP}$ and $V_{RSN}$) can be used to control the VCO without degrading $S_{REF}$. While the on-resistance of switches $S_{4,5}$ does not affect $K_{PD}$, it could introduce a delay at CT and degrade the phase margin. This issue will be addressed in Section V.

### C. Transient Response of the DAPD

Fig. 6 shows the simulated DAPD's steady-state waveforms and transient response when a 5° input phase step is applied to the VCO at 130 ns. As expected, due to the phase error, the DM voltage at the DAPD output becomes non-zero (~50 mV), while the CM voltage is nearly unchanged. Thanks to the resampling, both the DM and CM ripples at the DAPD output are dramatically suppressed. The small residual DM ripple at $F_{VCO}$ is mainly due to the gate's parasitic capacitance ($C_{gd}$) of $M_{1,2}$, which can be sufficiently attenuated by the PLL loop filter and should not limit $S_{REF}$ performance. Compared with a CSPD, the simulated CM ripple of a DAPD is $>10\times$ smaller and is only limited by the leakage of $M_{1,2}$. This significantly relaxes the CM rejection of the following stages for a given $S_{REF}$ requirement.

### D. Phase-Noise Analysis

*1) Noise of Reset Switches:* When the reset switches $S_{2,3}$ are turned on, the voltage noise on $C_S$ from the previous operation is cleared. However, the on-resistance of $S_{2,3}$ ($R_{ON}$) generates noise, which is held on $C_S$ until the next reset occurs. By ignoring the pole formed by $C_{RS}$ and $S_{4,5}$, the reset noise at the sampler output is

$$\frac{\overline{v_{n,\mathrm{rst}}^2}}{\Delta f}(f) = \frac{2(1-\alpha)\cdot 4\mathrm{KT}R_{ON}}{1+(2\pi f R_{ON} C_S)^2} + \frac{2\alpha^2 \cdot 2\mathrm{KT}}{C_S F_{REF}} \mathrm{sinc}\left(\frac{\alpha \pi f}{F_{REF}}\right)^2 \quad (17)$$

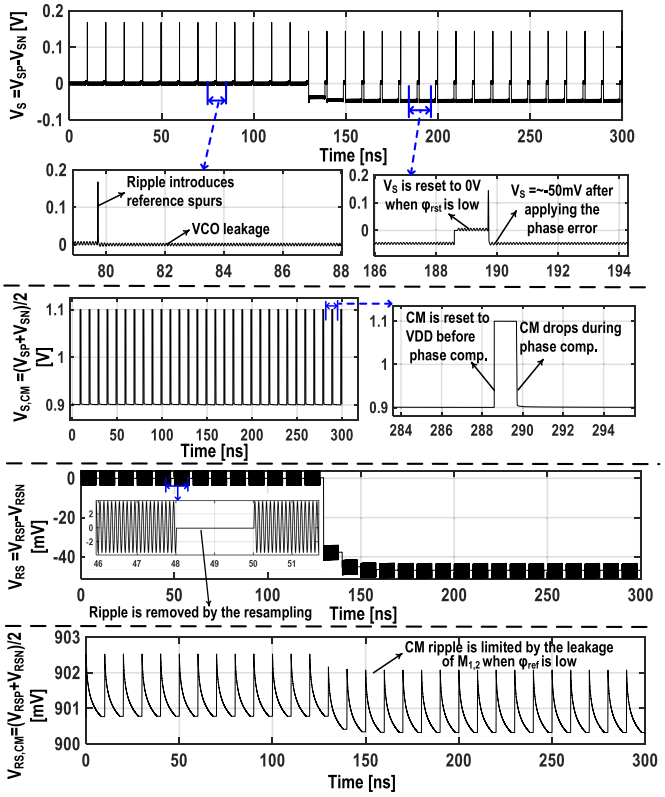



Fig. 6. Simulated DAPD's transient response to a 5° input phase step and its steady-state waveforms at 300 K.

where $\alpha$ is the duty cycle of $\varphi_{rst}$ [62]. In a DAPD, $\alpha$ is ~1, and the low-frequency noise can be estimated by

$$\frac{\overline{v_{n,\mathrm{rst}}^2}}{\Delta f}(f) \approx \frac{4\mathrm{KT}}{C_S F_{REF}}. \quad (18)$$

Note that (18) slightly overestimates the reset noise held on $C_S$, as part of it is discharged during the phase-detection mode due to the finite output impedance of $M_{1,2}$.

*2) Noise of Transconductors:* During the phase-detection mode, $M_{1,2}$ inject noise current pulses into $C_S$, creating a voltage noise held there until the next reset occurs. The sampled voltage noise due to $M_{1,2}$ can be expressed as

$$\frac{\overline{v_n^2}}{\Delta f}(f) = \sum_{k=-\infty}^{+\infty} |H_w(f - k\cdot F_{REF})|^2 \cdot S_i(f - k\cdot F_{REF}) \quad (19)$$

where $H_w(f)$ is the transfer function (TF) of the windowed-current integration process, and $S_i(f)$ is the power spectral density (psd) of the devices' current noise [63]. $H_w(f)$ can be found as

$$H_w(f) = \frac{1}{C_S} \cdot T_P \cdot \mathrm{sinc}(\pi f T_P). \quad (20)$$

Suppose that $M_{1,2}$ only generate white noise (e.g., thermal noise and shot noise). The low-frequency noise can be found by calculating the running sum of (19), and it can be estimated by

$$\frac{\overline{v_{n,\mathrm{white}}^2}}{\Delta f}(f) \approx 2 \cdot \frac{\overline{i_{n,\mathrm{white}}^2}}{\Delta f} \cdot \frac{1}{C_S^2} \cdot \frac{T_P}{F_{REF}} \quad (21)$$

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

$\overline{i^2_{n,\text{white}}}/\Delta f$ is the psd of $M_{1,2}$'s white noise and can be found from (8).

If $M_{1,2}$ contain only flicker noise with a psd of $\overline{i^2_{n,\text{fl}}}/\Delta f$, the running sum of (19) gives

$$\frac{\overline{v^2_{n,\text{fl}}}}{\Delta f}(f) \approx 2 \cdot \frac{\overline{i^2_{n,\text{fl}}}}{\Delta f} \cdot \frac{1}{C_S^2} \cdot \frac{T_P}{F_{\text{REF}}} \cdot \frac{T_P}{T_{\text{REF}}} = 2 \cdot \frac{\overline{i^2_{n,\text{fl}}}}{\Delta f} \cdot \frac{T_P^2}{C_S^2}. \tag{22}$$

*3) Noise of Other Components:* Compared with $M_{1,2}$ noise, the noise of the tail switch $S_1$ can be safely ignored since the ON-resistance of $S_1$ is designed to be $\ll 1/G_M$ to ensure a fast turn on of $M_{1,2}$. The resampling switches $S_{4,5}$ also generate noise, and the resulting voltage noise at the DAPD output can be estimated as $4\text{KT}/(C_{\text{RS}} F_{\text{REF}})$. A large $C_{\text{RS}}$ can be used to reduce the resampling noise without affecting $K_{\text{PD}}$. However, $C_S$ and $C_{\text{RS}}$ form a discrete-time low-pass filter, degrading the phase margin if $C_{\text{RS}}$ is too large. This issue will be resolved in Section V.

*4) In-Band PN Due to DAPD:* The in-band PN due to DAPD ($\mathcal{L}_{\text{DAPD}}$) is obtained by referring the sampled voltage noise to the input of the DAPD

$$\mathcal{L}_{\text{DAPD}} \approx \frac{\left(4\text{KTC}_S + \frac{\overline{i^2_{n,\text{white}}}}{\Delta f} \cdot 2T_P + \frac{\overline{i^2_{n,\text{fl}}}}{\Delta f} \cdot 2F_{\text{REF}} T_P^2\right)}{F_{\text{REF}} C_S^2 K_{\text{PD}}^2}. \tag{23}$$

Since $K_{\text{PD}}$ is proportional to $1/C_S$, the reset noise contribution to $\mathcal{L}_{\text{DAPD}}$ is proportional to $C_S$, indicating that a small $C_S$ helps improve the in-band PN. In contrast, the in-band PN of a CSPD is not a function of $C_S$ [43]. Hence, a very large $C_S$ is typically used to reduce the DM ripple in a CSPD [43]. Fig. 7(a) and (b), respectively, depicts the simulated and calculated $\mathcal{L}_{\text{DAPD}}$ versus $C_S$ and $T_P$ at a 300-kHz offset from a 10-GHz carrier when $(W/L)_{1,2} = 1.2\mu/40$ nm. The simulations match very well with the presented theory. As expected, $\mathcal{L}_{\text{DAPD}}$ is dominated by the reset noise if a large $C_S$ is used since $\mathcal{L}_{\text{DAPD}}$ contributed by both the flicker and thermal noise of $M_{1,2}$ is not a function of $C_S$. In addition, by varying $T_P$, the individual contribution of each noise source to $\mathcal{L}_{\text{DAPD}}$ also varies. Nevertheless, $\mathcal{L}_{\text{DAPD}}$ is still below $-130$ dBc/Hz and varies less than 2 dB when $T_P$ is within 0.2–0.5 $T_{\text{VCO}}$.

Fig. 7(c) and (d) shows the simulated $\mathcal{L}_{\text{DAPD}}$ at 4.2 K due to DAPD's white noise[5] versus $C_S$ and $T_P$, respectively. Thanks to the temperature reduction, the PN contributed by the thermal noise of reset switches and $M_{1,2}$ is reduced dramatically. However, the temperature-independent shot noise limits the final PN improvement to ~10 dB.[6]

### E. Mismatch and $P_{dc}$ Analysis

The DAPD components are subject to a large mismatch due to the use of small device sizes. If the VCO zero-crossings still occur at the center of the $\varphi_{\text{ref}}$ pulse, then a non-zero $V_S$ will be created due to the mismatch of $C_S$ and $G_M$. This implies that the PLL is not locked. Hence, the PLL must develop a static phase offset to equalize $V_{\text{SP}}$ and $V_{\text{SN}}$ by shifting the locking point away from the ideal point. After resampling, $V_{\text{RSP}}$ and $V_{\text{RSN}}$ are still ideally constant. Hence, the mismatch of DAPD components does not degrade $S_{\text{REF}}$. On the contrary, $C_S$ mismatch in a CSPD [43] does not change the locking point but increases $S_{\text{REF}}$.

The DAPD mainly dissipates the dynamic current when charging $C_S$ during $\varphi_{\text{rst}}$. $P_{\text{dc}}$ of the DAPD core could be estimated by

$$P_{\text{dc,DAPD}} \approx 2 \cdot C_S \cdot F_{\text{REF}} \cdot \frac{G_M V_{\text{GT}} T_P}{C_S} \cdot V_{\text{DD}} \tag{24}$$

where $V_{\text{GT}}$ is the overdrive voltage of $M_{1,2}$. The resulting $P_{\text{dc}}$ is less than 2 $\mu$W by considering $F_{\text{REF}} =$ 100 MHz and $V_{\text{GT}} =$ 0.25 V.

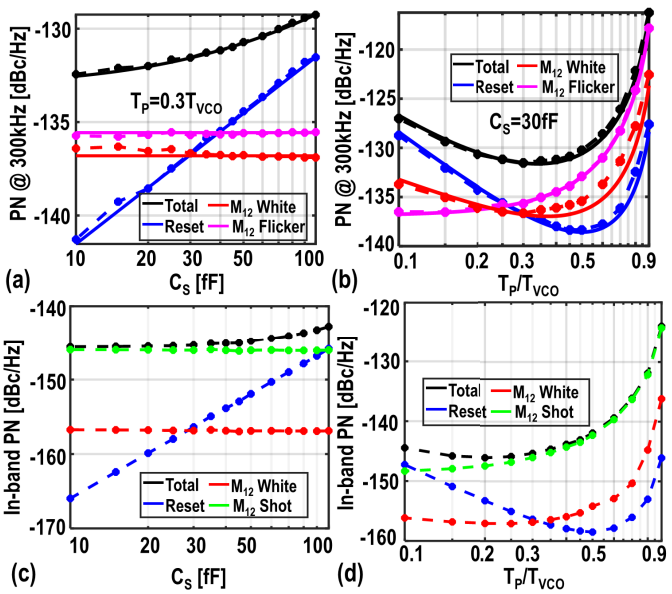



Fig. 7. Simulated and calculated PN at a 300-kHz offset from a 10-GHz carrier versus (a) $C_S$ and (b) $T_P$ at 300 K; simulated in-band PN due to DAPD's white noise versus (c) $C_S$ and (d) $T_P$ at 4.2 K.

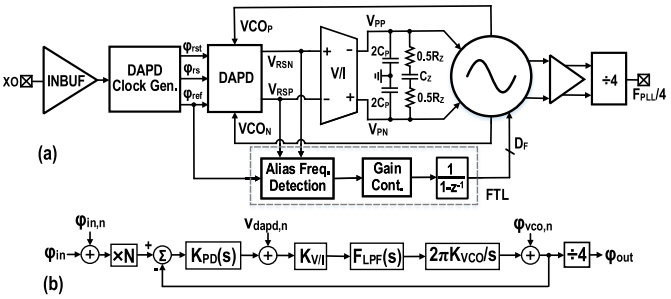



Fig. 8. (a) Block diagram and (b) phase-domain model of the cryo-CMOS analog DAPLL with noise sources of interest.

## V. Cryo-CMOS Analog DAPLL

### A. System Overview

The block diagram of the proposed cryo-CMOS dynamic-amplifier-based sub-sampling PLL (DAPLL) is shown in Fig. 8(a). An input buffer (INBUF) is used to reshape the external 100-MHz sinusoidal reference clock into a steep square

[5]The flicker noise is not included in those simulations due to the lack of device model.

[6]If the flicker noise is considered to be temperature-independent in the process we used, the final PN improvement is estimated to be within 6 dB.

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

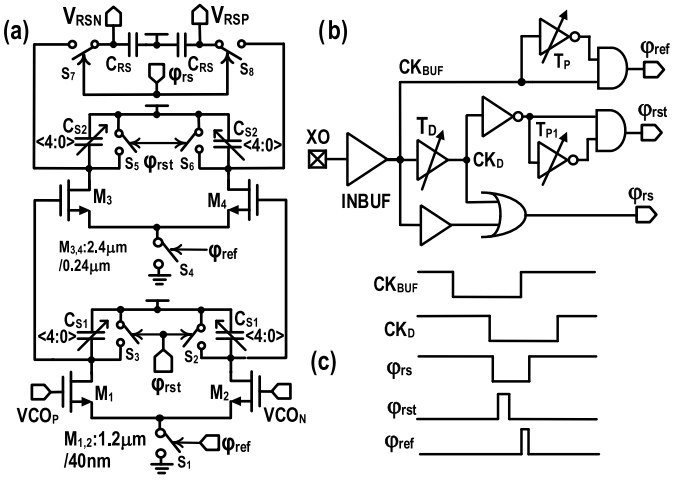



Fig. 9. Schematics of (a) DAPD and (b) its clock generation; (c) timing diagram of DAPD.

wave. The required clock pulses ($\varphi_{\rm rst}$, $\varphi_{\rm rs}$, and $\varphi_{\rm ref}$) for a proper operation of the DAPD are derived from a clock generation circuit. The DAPD directly senses the phase error between the VCO and $\varphi_{\rm ref}$ without any isolation buffers and outputs a very stable voltage. A fully differential V/I stage (based on a folded-cascode operational transconductance amplifier) and a passive loop filter are then used to generate a tuning voltage for the fine frequency control. An ON-chip divide-by-4 circuit based on the static current-mode-logic (CML) latch is designed to ease the cryogenic measurements.

To avoid locking to a wrong harmonic, the VCO's frequency is manually tuned within $\pm 0.5 F_{\rm REF}$ of the desired frequency at power on. Afterward, the VCO's frequency is kept close to the lock-in range of the PLL by a frequency-tracking loop (FTL) similar to that in [55], which is running in background to correct the frequency error introduced by a sudden frequency disturbance on the VCO.

As shown in Fig. 8(b), a linear phase-domain model of the DAPLL is developed to predict the loop dynamics and PN performance at 4.2 K. Here, $F_{\rm LPF}(s)$ and $K_{\rm VCO}$, respectively, represent the TF of the loop filter and VCO tuning gain. A damping factor of $\sim$1.6 is selected in this design to guarantee PLL's stability at CT. By considering the zero-order hold effect and ignoring the sinc-type response introduced by the windowed-current integration, the s-domain $K_{\rm PD}$ can be estimated by

$$K_{\rm PD}(s) \approx K_{\rm PD} \cdot \frac{1 - e^{-sT_{\rm REF}}}{sT_{\rm REF}}. \tag{25}$$

### B. Dynamic-Amplifier-Based PD

The periodic switching of $C_{\rm RS}$ in Fig. 4 injects charge to the VCO through $C_{\rm gd}$ of $M_{1,2}$, degrading $S_{\rm REF}$. As depicted in Fig. 9(a), a two-stage cascaded DA is thus used before the resampling stage to achieve better isolation between the VCO and $C_{\rm RS}$. $S_{\rm REF}$ due to $\varphi_{\rm rst}$ switching can be minimized by narrowing down the duty cycle of $\varphi_{\rm rst}$. To accommodate the transconductance variation in $M_{1-4}$ at 4.2 K, $K_{\rm PD}$ can be digitally regulated by sampling capacitors $C_{S1}$ and $C_{S2}$. $M_{1,2}$ are sized with a minimum channel length and a small width to reduce the modulated capacitance seen by the VCO tank and optimize $S_{\rm REF}$. A high $K_{\rm PD}$ of the first-stage DA ($\sim$0.6 V/rad) ensures that the in-band PN contributed by $M_{1,2}$ is very low [see (23)]. However, such a high $K_{\rm PD}$ introduces a large loop gain for the PLL. Hence, the resulting loop is difficult to stabilize without using a large loop filter capacitor. To this end, the second stage is sized with a low gain by choosing a large $C_{S2}$ to optimize the overall $K_{\rm PD}$.A large $C_{S2}$ also helps preserve a high common-mode voltage at the second-stage DA output. Hence, the resampling switches $S_{7,8}$ can have enough voltage headroom, thus leading to low ON-resistance at CT. Due to the good isolation offered by $M_{1,2}$ between the VCO and second-stage DA, $M_{3,4}$ are up-sized with a channel length of 240 nm to reduce their shot noise and flicker noise at CT without penalizing $S_{\rm REF}$.

Note that the charge transfer between $C_{S2}$ and $C_{\rm RS}$ forms a discrete-time low-pass filter. Thus, $C_{\rm RS}$ should be minimized to preserve a high phase margin of the PLL. Fortunately, by choosing $C_{\rm RS} = C_{S2}/4$, the resulting phase margin degradation is within 14° for a 4-MHz PLL bandwidth. Thanks to the high gain of the first stage, the simulated noise contribution due to resampling switches $S_{7,8}$ at 300 K is less than 10% of the total noise. At 300 K, the simulated PN floor due to DAPD is $-128$ dBc/Hz when referred to a 10-GHz carrier, in which the first- and second-stage DA show a similar contribution. By considering $T_{\rm ch} = 4.2$ K due to the DAPD's low $P_{\rm dc}$ ($<10\,\mu$W), the estimated PN floor is expected to be $\sim -137$ dBc/Hz, dominated by the first-stage DA's shot noise.

### C. DAPD Clock Generation

Fig. 9(b) and (c) shows the schematic and timing diagram of DAPD clock generation, respectively. Note that in theory, the DAPD output is only determined by $\varphi_{\rm ref}$. The clock jitter of $\varphi_{\rm rst}$ and $\varphi_{\rm rs}$ thus has a minor impact on DAPD's PN. Therefore, the clock generation circuits of $\varphi_{\rm rst}$ and $\varphi_{\rm rs}$ can be designed with low power. $\varphi_{\rm ref}$ is generated by a pulse generator, which is derived from the rising edge of the buffered XO output. At RT, the simulated PN floor of the INBUF is $-161$ dBc/Hz. By considering $T_{\rm ch} = 4.2$ K, the PN floor is dominated by the shot noise and is limited to $-167$ dBc/Hz. Compared with RT, $T_P$ is expected to reduce by $\sim$30% at 4.2 K, degrading $K_{\rm PD}$ moderately by $<$10%. To generate $\varphi_{\rm rst}$ and $\varphi_{\rm rs}$, an intermediate clock ($\rm CK_D$) is generated by delaying $\rm CK_{BUF}$ through a digitally controlled delay line. Its delay ($T_D$) can be tuned from 0.6 to 3 ns to ensure that the required clock pulses can be reliably generated under PVT variations. $\varphi_{\rm rst}$, derived from the falling edge of $\rm CK_D$, is generated by a second pulse generator. Finally, the falling edge of $\rm CK_D$ and the rising edge of $\rm CK_{BUF}$ are leveraged to generate $\varphi_{\rm rs}$.

### D. VCO and its Buffer

The schematic of the $LC$-VCO is shown in Fig. 10(a). The negative resistance is provided by a CMOS differential pair ($M_{1-4}$), implemented with low-threshold thin-oxide devices. The excess gain ($G_X$) of the VCO is designed to be $\sim$3 to

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

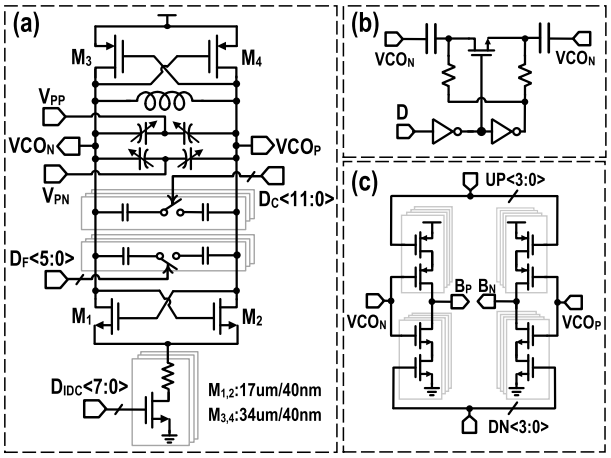



Fig. 10. Schematics of (a) VCO, (b) VCO capacitor bank unit, and (c) VCO buffer.

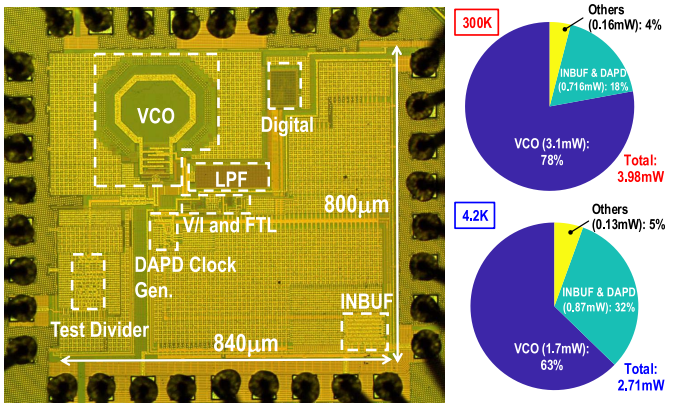



Fig. 11. Chip micrograph and measured power breakdown of the DAPLL.

ensure a robust startup at RT. However, due to the significant increase in the tank's quality factor and transconductance at 4.2 K, the conversion of $M_{1-4}$'s device flicker noise to PN can be severely degraded due to the increased $G_X$ [64]. An 8-bit digitally controlled tail-resistor bank is thus used to optimize $G_X$ and PN at 4.2 K. This resistor bank also helps adjust the VCO swing and thus optimize $K_{\mathrm{PD}}$ over the PLL tuning range. In a future design, an amplitude calibration technique [65] could be used to stabilize the VCO swing across the band of operation without incurring extra $P_{\mathrm{dc}}$. Due to the dramatic reduction in the PN in the thermal region and limited improvement of the PN in the flicker region, the VCO would exhibit a very high flicker corner (e.g., a few MHz) at 4.2 K. Yet, the flicker-corner issue could be partially mitigated by using a large DAPLL loop bandwidth. The VCO can be fine-tuned by two differential accumulation-mode varactors, and its coarse frequency tuning is realized by a switched capacitor bank, whose unit cell schematic is shown in Fig. 10(b). A dc-coupled VCO buffer is used to drive the test divider as shown in Fig. 10(c).

## VI. Measurement Results

The DAPLL has been fabricated in a standard 40-nm bulk CMOS process. Fig. 11 shows the chip micrograph and the

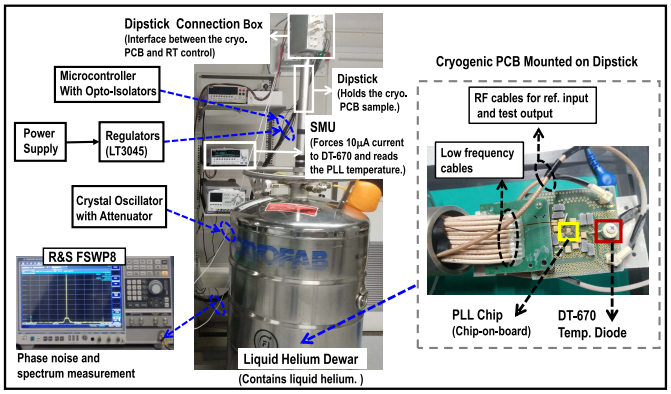



Fig. 12. Cryogenic measurement setup.

measured power breakdown. The core area of the chip is ∼0.14 mm $^2$. Since the divider consumes a high $P_{\mathrm{dc}}$ to minimize its PN and drive the long cables used in the cryogenic setup, the PLL core components could heat up beyond 100 K [33]. To mitigate this issue, the test divider is placed physically far away (∼200 $\mu$m) from the PLL in the layout. The DAPLL's performance has been characterized over a wide temperature range from 300 to 4.2 K. To measure the DAPLL's performance under cryogenic conditions, the setup shown in Fig. 12 was used, where a test board with a wire-bonded chip was mounted at one end of a dipstick. The DAPLL's ambient temperature ($T_{\mathrm{am}}$) can be changed by adjusting the vertical position of the dipstick placed inside a helium dewar and monitored by a temperature diode mounted on the surface of the board close to the chip. To facilitate the measurements, the 100-MHz sinusoidal reference, power supply, and biasing were placed at RT. Since the reference signal's frequency is low, the long cable used in the measurement setup has a minor impact on its swing.

As shown in Fig. 11, the DAPLL dissipates ∼4 mW (excluding the test divider but including the ON-chip INBUF) from a 1.1-V power supply at 300 K. When the chip is cooled down to 4.2 K, $P_{\mathrm{dc}}$ of the DAPLL is reduced to 2.7 mW under the same supply. This is mainly because the VCO requires less current to deliver the same swing due to the increased tank quality factor at 4.2 K. The DAPLL can cover an output frequency range of 8.9–11.1 GHz and 9.4–11.6 GHz at 300 and 4.2 K, respectively. The slightly increased output frequency at 4.2 K is mainly due to the reduction in the VCO $LC$ tank's inductance and parasitic capacitance to the substrate.

Fig. 13(a) shows the measured PN plot at 300 K from an R&S FSWP8 PN analyzer, where the PLL is running at 10 GHz. An in-band PN floor of −130 dBc/Hz has been achieved at the 2.5-GHz divided output, limited by the ON-chip INBUF. The measured rms jitter and integrated PN (from 10 kHz to 30 MHz) excluding reference spurs are ∼75 fs and −49.5 dBc, respectively, corresponding to a PLL jitter-power FOM of −256.5 dB. Fig. 13(b) shows the measured PN plot at 4.2 K after re-optimizing the loop parameters to improve the fidelity. The measured rms jitter and integrated PN are dramatically reduced to 37 fs and −55.8 dBc, respectively.

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

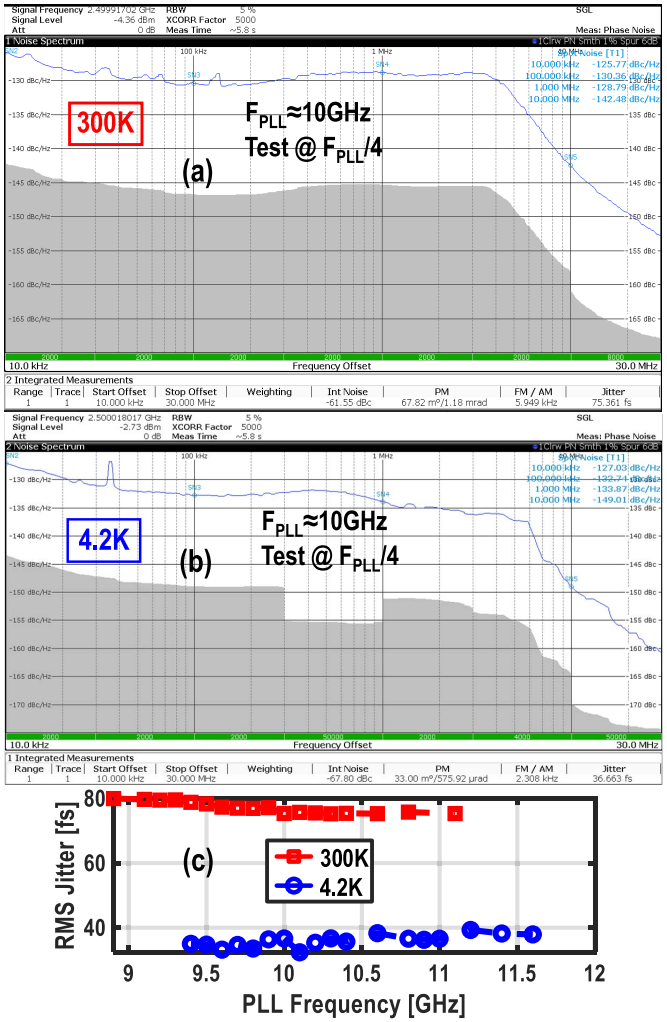



Fig. 13. Measured PN plots at (a) 300 and (b) 4.2 K after an ON-chip divide-by-4 when the PLL is running at 10 GHz; (c) rms jitter at 300 and 4.2 K over the PLL tuning range.

The estimated control fidelity is 99.9994% (99.9998%) for a 1-MHz (10-MHz) $f_R$, thus satisfying the requirements of LO generation for QC applications. Fig. 13(c) shows the measured rms jitter over the tuning range at 4.2 and 300 K. In each measurement point, the VCO's frequency was initially calibrated within the PLL's locking range by adjusting the VCO's switched capacitor at power on. Then, the PLL locks the phase of the VCO to the reference. Compared with 300 K, the measured rms jitter improves nearly by 2× due to the noise reduction at 4.2 K.

Fig. 14(a) depicts three measured PN plots based on different $C_{S2}$ settings while keeping other loop parameters fixed at 4.2 K, where the PLL is running at 10.8 GHz. As expected, $K_{\mathrm{PD}}$ and hence the PLL loop gain become too large when a very small $C_{S2}$ is used, resulting in a wide loop bandwidth and jitter peaking. However, when a very large $C_{S2}$ is used, $K_{\mathrm{PD}}$ and the PLL loop gain are reduced, leading to less filtering of the VCO's PN due to a narrow bandwidth. Based on the phase-domain model and the estimated PN of the DAPD and INBUF discussed in Section V, the model-predicted PN is compared with a measured PN profile at 4.2 K [see Fig. 14(b)].

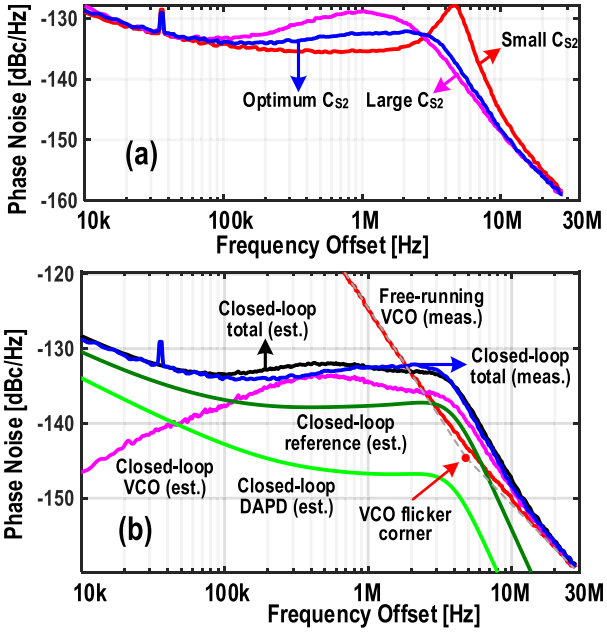



Fig. 14. (a) Measured PN profiles by varying $C_{S2}$ at 4.2 K and (b) estimated PN profiles in comparison to the measurement at 4.2 K, where the test frequency is 2.7 GHz.

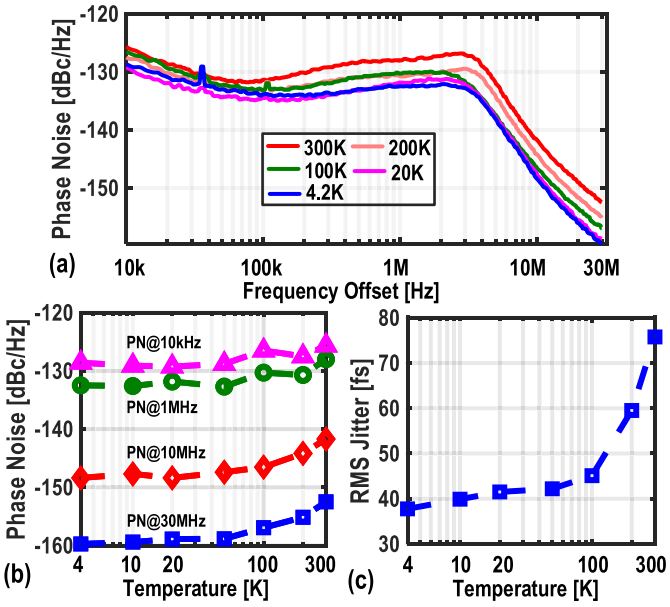



Fig. 15. (a) Measured PN profiles, (b) spot noise, and (c) rms jitter over the temperature.

The measured output PN in blue matches well with the estimated noise profile in black. Below 100 kHz, the in-band PN is dominated by the flicker noise of the INBUF. From 100 kHz to 4 MHz, the in-band PN is limited by the filtered flicker PN of the VCO and shot PN of the INBUF. The flicker PN of the VCO could be better suppressed by the PLL if a lower damping factor was selected, at the cost of worse loop stability.

Fig. 15(a) and (b), respectively, shows the measured PN profiles and spot noise over $T_{\mathrm{am}}$ after re-optimizing the jitter performance. The PN at the 10- and 30-MHz offsets improves

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART

| | This Work | | T. Liu [26] TCAS-I'17 | J.-H. Seol [54] JSSC'21 | J. Gong [43] JSSC'21 | Z. Zhang [50] JSSC'20 | Z. Yang [42] ISSCC'19 | D.-G. Lee [51] JSSC'20 | M. Mercandelli [53] ISSCC'20 | A. Santiccioli [41] JSSC'20 | H. Zhang [45] VLSI'19 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PLL Architecture | Integer-N DAPLL | | Integer-N Charge-Pump PLL | Integer-N Reference Oversampling PLL | Integer-N Charge-Sampling PLL | Integer-N Sub-Sampling PLL | Integer-N Sub-Sampling PLL | Integer-N Sub-Sampling PLL | Fractional-N Sampling PLL | Fractional-N Bang-Bang PLL | Integer-N Injection-Locked PLL |
| Power Supply [V] | 1.1 | | 1.2 | NA | 1.1/0.6 | 0.65 | 1/0.55 | 1 | 0.9 | 0.9 | **0.14 |
| Temperature [K] | 4.2 | 300 | 77 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 |
| $F_{REF}$ [MHz] | 100 | | NA | 200 | 100 | 200 | 103 | 100 | 500 | 500 | 100 |
| $F_{PLL}$ [GHz]<br>FTR [GHz] | 10<br>9.4-11.6 | 10<br>8.9-11.1 | 2.5<br>2.22-3.6 | 4<br>(NA) | 11.2<br>9.8-12.2 | 14<br>12-16 | 26.4<br>25.4-29.5 | 2.4<br>NA | 12.5<br>11.9-14.1 | 13.5<br>12.8-15.2 | 2.4<br>2.2-2.6 |
| REF. Spur [dBc] | -69.1 | -78.4 | NA | -78.1 | -77.3 | -64.6 | -63 | -67 | -73.5 | -80.1 | -66.5 |
| RMS Jitter, $\sigma_j$ [fs]<br>[Int. Bandwidth] | 36.7<br>[10k-30MHz] | 75.3<br>[10k-30MHz] | 420<br>NA | 67.1<br>[10k-100M] | 48.6<br>[1k-100MHz] | 56.4<br>[1k-100MHz] | 71<br>[1k-100M] | 161<br>[10k-100M] | ***51.7<br>[1k-100MHz] | ***58.9<br>[1k-100MHz] | 298<br>[0.1k-100M] |
| Est. Total Jitter [fs]<br>[with REF. spur] | 37.5 | 75.4 | NA | 67.5 | 48.7 | 57.2 | 71.3 | 166.4 | 51.8 | 58.9 | 301.3 |
| Power, $P_{DC}$ [mW] | 2.7 | 4 | 8.5 | 5.2 | 5 | 7.2 | 15.3 | 0.9 | 18 | 19.8 | 0.17 |
| *FOM [dB] | -264.4 | -256.5 | -238.3 | -256.3 | -259.2 | -256.4 | -251.1 | -256.3 | -253.2 | -251.6 | -258.2 |
| Core Area [mm²] | 0.14 | | 0.08 | 0.17 | 0.13 | 0.234 | 0.24 | 0.42 | 0.16 | 0.17 | 0.23 |
| Process [nm] | 40 | | 65 | 28 | 40 | 40 | 65 | 65 | 28 | 28 | 65 |

*FOM = $20*\log_{10}(\sigma_j/1s) + 10*\log_{10}(P_{DC}/1mW)$ ** For the VCO only (supply of the rest circuit is not reported.) ***Jitter of a fractional-N PLL (measured in an integer-N channel)

substantially (∼5 dB) from 300 to 100 K. However, it reduces moderately (<3 dB) by further going from 100 to 4.2 K. This is because, above 100 K, self-heating of the VCO can be safely ignored as the increase in channel temperature ($\Delta T_{ch}$) is expected to be within $0.1 \times T_{am}$ (i.e., $T_{ch} \approx T_{am}$) [33]. Hence, the measured PN in the VCO's thermal region improves significantly due to reduced channel noise and increased quality factor. Below 100 K, the VCO suffers from severe self-heating, resulting in $T_{ch} \gg T_{am}$ [33]. In addition, as thermal noise reduces, the shot noise cannot be ignored. The combination of self-heating and shot noise results in a minor PN improvement below 100 K. Moreover, the measured PN at a 10-kHz offset improves merely ∼3 dB from 300 to 4.2 K. This is likely due to the fact that the PN in the flicker region of the INBUF is not a strong function of $T_{ch}$. Furthermore, the improvement of PN at a 1-MHz offset is ∼5 dB from 300 to 4.2 K, limited by both the shot and flicker noise of the VCO. Consequently, while the measured rms jitter improves significantly from 75 to 45 fs by going from 300 to 100 K, the jitter improvement is limited to merely 1.5 dB when $T_{am}$ is further reduced from 100 to 4.2 K [see Fig. 15(c)].

Fig. 16(a) and (b) shows the measured spectrum at 300 and 4.2 K, respectively. At 300 K, the measured $S_{REF}$ at the divide-by-4 output is −90.4 dBc, which increases to −78.4 dBc when referred to the 10-GHz PLL frequency. The measured $S_{REF}$ becomes −69 dBc at 4.2 K, probably due to cryogenic measurement constraints (e.g., coupling between dense cables). While the measured $S_{REF}$ is degraded at 4.2 K, the target specification of −54 dBc is satisfied with >10-dB margin over the PLL tuning range as shown in Fig. 16(c). The measured reference spur (<−67.5 dBc) is well below the integrated PN (∼−55.8 dBc), which degrades the rms jitter by <1.5 fs.

Table II shows comparison of the performance of the presented DAPLL with the state-of-the-art. At 300 K, the FOM and $S_{REF}$ achieved in this work are very competitive. By moving to 4.2 K, our FOM improves by ∼8 dB, outperforming the RT/CT prior art. Moreover, this work is the first cryo-CMOS PLL operating at 4.2 K and meets the specification requirements of LO generation for QC applications.

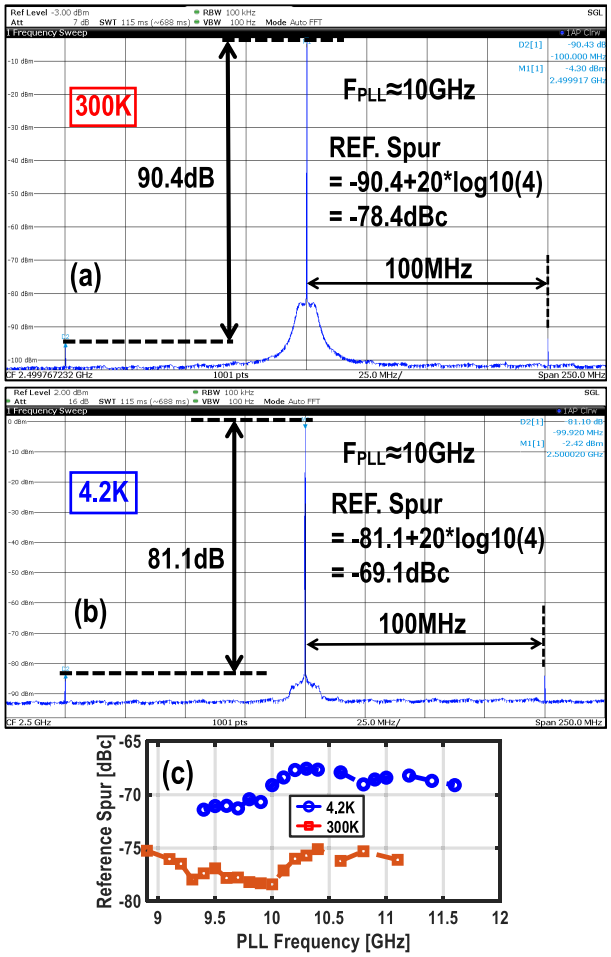



Fig. 16. Measured spectrum at (a) 300 and (b) 4.2 K after an ON-chip divide-by-4 when the PLL is running at 10 GHz; (c) $S_{REF}$ at 300 and 4.2 K over the PLL tuning range.

## VII. CONCLUSION

A cryo-CMOS PLL for qubit control is presented. The specifications of PLL are derived from the control fidelity for a single-qubit operation. An analog charge-domain

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

sub-sampling PLL structure is selected to benefit more from noise reduction from 300 to 4.2 K. A DAPD is proposed to simultaneously achieve low spur and low jitter. $K_{PD}$ and PN of the DAPD are analyzed in depth. Design considerations of the PLL for cryogenic operation are also analyzed. At 300 K, the PLL achieves 75-fs rms jitter and 4-mW $P_{dc}$ at 10 GHz, leading to a −256.5-dB PLL jitter-power FOM, while maintaining −78.4-dBc $S_{REF}$. At 4.2 K, the PLL achieves an rms jitter of 37 fs and an $S_{REF}$ of −69 dBc, while consuming 2.7 mW. The proposed cryo-CMOS PLL meets the performance requirements for the qubit control, which marks a major step toward a fully integrated qubit controller.

## ACKNOWLEDGMENT

The authors would like to acknowledge Ramon W. J. Overwater and Pascal T. Hart from TU Delft for device characterization and modeling, and Atef Akhnoukh and Zu-Yao Chang from TU Delft for tapeout and chip assembly support.

## REFERENCES

[1] F. Arute et al., "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, 2019.

[2] X. Xue et al., "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, vol. 593, no. 7858, pp. 205–210, 2021.

[3] E. Charbon et al., "15.5 cryo-CMOS circuits and systems for scalable quantum computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 264–265.

[4] C. H. Yang et al., "Operation of a silicon quantum processor unit cell above one Kelvin," *Nature*, vol. 580, no. 7803, pp. 350–354, 2020.

[5] J. van Staveren et al., "Voltage references for the ultra-wide temperature range from 4.2 K to 300K in 40-nm CMOS," in *Proc. IEEE 45th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2019, pp. 37–40.

[6] M. J. Gong et al., "Design considerations for spin readout amplifiers in monolithically integrated semiconductor quantum processors," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 111–114.

[7] I. Bashir et al., "A mixed-signal control core for a fully integrated semiconductor quantum computer system-on-chip," in *Proc. IEEE 45th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2019, pp. 125–128.

[8] M. Mehrpoo, F. Sebastiano, E. Charbon, and M. Babaie, "A cryogenic CMOS parametric amplifier," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 5–8, 2020.

[9] L. L. Guevel et al., "19.2 A 110 mK 295 $\mu$W 28 nm FDSOI CMOS quantum integrated circuit with a 2.8 GHz excitation and nA current sensing of an on-chip double quantum dot," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 306–308.

[10] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[11] A. V. Matheoud, N. Sahin Solmaz, and G. Boero, "A low-power microwave HEMT *LC* oscillator operating down to 1.4 K," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2782–2792, Jun. 2019.

[12] J. Gong, Y. Chen, F. Sebastiano, E. Charbon, and M. Babaie, "A 200 dB FoM 4-to-5 GHz cryogenic oscillator with an automatic common-mode resonance calibration for quantum computing applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 308–310.

[13] A. Ruffino, Y. Peng, T.-Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba, and E. Charbon, "13.2 A fully-integrated 40-nm 5–6.5 GHz cryo-CMOS system-on-chip with I/Q receiver and frequency synthesizer for scalable multiplexed readout of quantum dots," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 210–212.

[14] P. Vliex et al., "Bias voltage DAC operating at cryogenic temperatures for solid-state qubit applications," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 218–221, 2020.

[15] A. Esmailiyan et al., "A fully integrated DAC for CMOS position-based charge qubits with single-electron detector loopback testing," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 354–357, 2020.

[16] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A wideband low-power cryogenic CMOS circulator for quantum applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1224–1238, May 2020.

[17] J. Gong, E. Charbon, F. Sebastiano, and M. Babaie, "A 2.7 mW 45fs$_{rms}$-jitter cryogenic dynamic-amplifier-based PLL for quantum computing applications," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2021, pp. 1–2.

[18] Y. Peng, A. Ruffino, and E. Charbon, "A cryogenic broadband sub-1-dB NF CMOS low noise amplifier for quantum applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2040–2053, Jul. 2021.

[19] G. Kiene et al., "13.4 A 1 GS/s 6-to-8b 0.5 mW/qubit cryo-CMOS SAR ADC for quantum computing in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 214–216.

[20] S. Pauka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electron.*, vol. 4, no. 1, pp. 64–70, 2021.

[21] J.-S. Park et al., "13.1 A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22 nm FFL FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 208–210.

[22] B. Prabowo et al., "A 6-to-8 GHz 0.17 mW/qubit cryo-CMOS receiver for multiple spin qubit readout in 40 nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 212–214.

[23] K. Kang et al., "A 5.5 mW/channel 2-to-7 GHz frequency synthesizable qubit-controlling cryogenic pulse modulator for scalable quantum computers," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[24] J. C. Bardin et al., "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Oct. 2019.

[25] J. P. G. Van Dijk et al., "A scalable cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2930–2946, Sep. 2020.

[26] T. Liu, X. Wang, R. Wang, G. Wu, T. Zhang, and P. Gui, "A temperature compensated triple-path PLL with $K_{VCO}$ non-linearity desensitization capable of operating at 77 K," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 11, pp. 2835–2843, May 2017.

[27] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.

[28] J. van Dijk et al., "Impact of classical control electronics on qubit fidelity," *Phys. Rev. A, Gen. Phys.*, vol. 12, Oct. 2019, Art. no. 044054, doi: 10.1103/PhysRevApplied.12.044054.

[29] J. P. G. van Dijk, B. Patra, S. Pellerano, E. Charbon, F. Sebastiano, and M. Babaie, "Designing a DDS-based SoC for high-fidelity multi-qubit control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5380–5393, Dec. 2020.

[30] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018.

[31] P. A. T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of mismatch in cryo-CMOS," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 263–273, 2020.

[32] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 448–456, 2020.

[33] P. A. T Hart, M. Babaie, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of self-heating in nanometer bulk-CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 891–901, 2021.

[34] V. M. Mahajan et al., "A physical understanding of RF noise in bulk nMOSFETs with channel lengths in the nanometer regime," *IEEE Trans. Electron Devices*, vol. 59, no. 1, pp. 197–205, Dec. 2012.

[35] J. Jeon et al., "The first observation of shot noise characteristics in 10-nm scale MOSFETs," in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 48–49.

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.

[36] J. A. McNeill, "Noise in short channel MOSFETs," in *Proc. IEEE Custom Integr. Circuits Conf.*, Jun. 2009, pp. 567–572.
[37] J. Craninckx et al., "CMOS cryo-electronics for quantum computing," in *IEDM Tech. Dig.*, Dec. 2020, p. 25.
[38] B. C. Paz et al., "Performance and low-frequency noise of 22-nm FDSOI down to 4.2 K for cryogenic applications," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4563–4567, Sep. 2020.
[39] R. Staszewski et al., "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
[40] M. Mehrpoo et al., "Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Dec. 2019, pp. 1–5.
[41] A. Santiccioli et al., "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang-bang PLL with digital frequency-error recovery for fast locking," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3349–3361, Sep. 2020.
[42] Z. Yang, Y. Chen, S. Yang, P.-I. Mak, and R. P. Martins, "A 25.4-to-29.5 GHz 10.2 mW isolated sub-sampling PLL achieving −252.9 dB jitter-power FoM and −63 dBc reference spur," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 270–272.
[43] J. Gong, E. Charbon, F. Sebastiano, and M. Babaie, "A low-jitter and low-spur charge-sampling PLL," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 492–504, Feb. 2022.
[44] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, no. 11, pp. 1849–1858, Nov. 1980.
[45] H. Zhang et al., "0.2 mW 70 $fs_{rms}$-jitter injection-locked PLL using desensitized SSPD-based injecting-time self-alignment achieving −270 dB FoM and −66 dBc reference spur," in *Proc. Symp. VLSI Circuits*, Aug. 2019, pp. C38–C39.
[46] S. Yoo, S. Choi, Y. Lee, T. Seong, Y. Lim, and J. Choi, "A low-jitter and low-reference-spur ring-VCO-based injection-locked clock multiplier using a triple-point background calibrator," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 298–309, Jan. 2021.
[47] J. Gong et al., "A 1.33 mW, 1.6 $ps_{rms}$-integrated-jitter, 1.8–2.7 GHz ring-oscillator-based fractional-N injection-locked DPLL for Internet-of-Things applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 44–47.
[48] K. M. Megawer, A. Elkholy, D. Coombs, M. G. Ahmed, A. Elmallah, and K. P. Hanumolu, "A 5 GHz 370 $fs_{rms}$ 6.5 mW clock multiplier using a crystal-oscillator frequency quadrupler in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jun. 2018, pp. 392–394.
[49] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by $N^2$," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.
[50] Z. Zhang, G. Zhu, and C. P. Yue, "A 0.65-V 12–16-GHz sub-sampling PLL with 56.4-$fs_{rms}$ integrated jitter and −256.4-dB FoM," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1665–1683, Jan. 2020.
[51] D.-G. Lee and P. P. Mercier, "A sub-mW 2.4-GHz active-mixer-adopted sub-sampling PLL achieving an FoM of −256 dB," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1542–1552, Jun. 2020.
[52] Y. Lim et al., "A 170 MHz-lock-in-range and −253 dB-$FoM_{jitter}$ 12-to-14.5 GHz subsampling PLL with a 150 $\mu$W frequency-disturbance-correcting loop using a low-power unevenly spaced edge generator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 280–282.
[53] M. Mercandelli et al., "A 12.5-GHz fractional-N type-I sampling PLL achieving 58-fs integrated jitter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Nov. 2020, pp. 274–276.
[54] J.-H. Seol, K. Choo, D. Blaauw, D. Sylvester, and T. Jang, "Reference oversampling PLL achieving −256-dB FoM and −78-dBc reference spur," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2993–3007, Oct. 2021.
[55] J. Gong, F. Sebastiano, E. Charbon, and M. Babaie, "A 10-to-12 GHz 5 mW charge-sampling PLL achieving 50 fsec RMS jitter,−258.9 dB FOM and −65 dBc reference spur," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 15–18.
[56] M. S. Akter, K. A. A. Makinwa, and K. Bult, "A capacitively degenerated 100-dB linear 20–150 MS/s dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1115–1126, Apr. 2018.
[57] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2-times interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," *IEEE J Solid-State Circuits*, vol. 47, no. 12, pp. 2880–2887, Dec. 2012.
[58] J. Lin, M. Miyahara, and A. Matsuzawa, "A 15.5 dB, wide signal swing, dynamic amplifier using a common-mode voltage detection technique," in *2011 IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 21–24.
[59] B. Razavi, "Charge steering: A low-power design paradigm," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2013, pp. 1–8.
[60] J. W. Jung and B. Razavi, "A 25-Gb/s 5-mW CMOS CDR/deserializer," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 684–697, Mar. 2013.
[61] G. Xu and J. Yuan, "Performance analysis of general charge sampling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 2, pp. 107–111, Feb. 2005.
[62] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York, NY, USA: Wiley, 1986.
[63] T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Noise analysis for comparator-based circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 3, pp. 541–553, Mar. 2009.
[64] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Analysis and minimization of flicker noise up-conversion in voltage-biased oscillators," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2382–2394, Jun. 2013.
[65] A. D. Berny, A. M. Niknejad, and R. G. Meyer, "A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 909–917, Apr. 2005.

**Jiang Gong** (Student Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from Jilin University, Changchun, China, in 2015, and the M.Sc. degree *(cum laude)* in microelectronics from the Delft University of Technology, Delft, The Netherlands, in November 2017, where he is currently pursuing the Ph.D. degree.

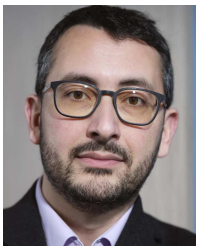
His research focuses on high spectral purity and wide tuning range frequency synthesizers for wireless, wireline, and quantum computing applications.

Mr. Gong was a recipient of the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award from 2021 to 2022. He serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and the IEEE SOLID-STATE CIRCUITS LETTERS (SSCL).

**Edoardo Charbon** (Fellow, IEEE) received the Diploma degree from ETH Zurich, Zürich, Switzerland, in 1988, the M.S. degree from the University of California at San Diego, San Diego, CA, USA, in 1991, and the Ph.D. degree from the University of California at Berkeley, Berkeley, CA, in 1995, all in electrical engineering and EECS.

He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the company's initiative on information hiding for intellectual property (IP) protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002, he has been a Member of the Faculty of the École Polytechnique Fédérale de Lausanne, where he has been a Full Professor since 2015. From 2008 to 2016, he was with the Delft University of Technology as the Chair of VLSI design. He is a Distinguished Visiting Scholar with the W. M. Keck Institute for Space, Caltech and a fellow of the Kavli Institute of Nanoscience Delft, Delft, The Netherlands. He has been the driving force behind the creation of deep-submicrometer CMOS single-photon avalanche diode (SPAD) technology, which is mass-produced since 2015 and is present in telemeters, proximity sensors, and medical diagnostics tools. He has authored or coauthored over 400 articles and two books, and he holds 23 patents. His research interests include 3-D vision, Fluorescence Lifetime Imaging (FLIM), Fluorescence Correlation Spectroscopy (FCS), Near-Infrared Optical Tomography (NIROT) to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing.

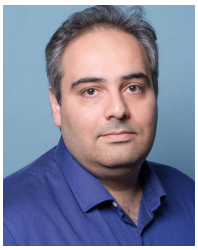
Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.



**Fabio Sebastiano** (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees *(cum laude)* in electrical engineering from the University of Pisa, Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree *(cum laude)* from the Sant'Anna School of Advanced Studies, Pisa, in 2006, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Associate Professor and the Research Lead of the Quantum Computing Division, QuTech, Delft. He has authored or coauthored one book, 11 patents, and over 100 technical publications. His research interests include cryogenic electronics, quantum computing, sensor read-outs, and fully integrated frequency references.

Dr. Sebastiano is on the Technical Program Committee Member of the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Symposium, and has been on the Program Committee of International Microwave Symposium (IMS). He has served as a Distinguished Lecturer of the IEEE Solid-State Circuit Society. He was a co-recipient of the International Symposium on Circuits and Systems (ISCAS) Best Student Paper Award in 2008, the Design, Automation and Test in Europe (DATE) Best Intellectual Property (IP) Award in 2017, the ISSCC Jan van Vessem Award for Outstanding European Paper in 2020, and the IEEE Custom Integrated Circuits Conference (CICC) Best Paper Award in 2022. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and has also served as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.



**Masoud Babaie** (Senior Member, IEEE) received the B.Sc. (Hons.) degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. degree *(cum laude)* in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016.

From 2006 to 2011, he was with the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently an Associate Professor. He has authored or coauthored one book, three book chapters, 11 patents, and more than 80 technical articles. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie was a co-recipient of the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award from 2015 to 2016, the IEEE International Solid-State Circuits Conference (ISSCC) Demonstration Session Certificate of Recognition in 2019, the IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper in 2020, and the IEEE Custom Integrated Circuits Conference (CICC) Best Paper Award in 2022. He was a recipient of the Veni Award from the Netherlands Organization for Scientific Research (NWO) in 2019. He also serves as the Technical Program Committee for the IEEE ISSCC and the Co-Chair for the Emerging Computing Devices and Circuits Subcommittee of the IEEE European Solid-State Circuits Conference (ESSCIRC).

Authorized licensed use limited to: Fuzhou University. Downloaded on January 07,2025 at 13:12:10 UTC from IEEE Xplore. Restrictions apply.