A 2-GS/s 8-bit Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC

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***Abstract*— This paper presents a 2-GS/s 8-bit 16× time-interleaved (TI) analog-to-digital converter (ADC) for a millimeter-wave pulsed radar baseband system-on-chip (SoC). To suppress sampling timing errors among sub-ADCs, a foreground timing-skew calibration technique with small additional circuits is proposed. Measured spurious-free dynamic range and signal-to-noise distortion ratio at 1-GHz full Nyquist is, therefore, enhanced by 16 and 11 dB, respectively. Unlike conventional calibration techniques based on redundant ADCs or complicated digital calculations, additional circuit components are only several small resistors and a capacitor, resulting in only 0.4% area penalty. This area saving enables the compact integration of the radar baseband SoC with digital beamforming, where eight-channel TI-ADCs occupy the dominant chip area otherwise. Even though this is foreground, no system performance is sacrificed because the calibration sequence is closed loop and fast enough to be executed during an existing calibration interval in a periodic beam transmission sequence. The TI-ADCs are embedded on industrial SoC in a 40-nm CMOS process. The power consumption including the input buffer and the reference buffer is 54.2 mW from a 1.1-V supply, and figure of merit is 355 fJ/conversion step.**

***Index Terms*— Calibration, millimeter-wave radar, time-interleaved (TI) ADC, timing skew.**

I. Introduction

MILLIMETER-WAVE radar system is one of the key components for today's advanced driving assistant systems and future automated driving. The main advantage of this system is environmental robustness such as rain, fog, and snow. Thus, it can be applied to a vehicle surrounding sensor or a traffic monitor to avoid car crash accidents under variable weather conditions. A pulsed wave radar is one of the millimeter-wave radar systems. It can detect objects with higher range resolution compared with other continuous wave radar systems [1], [2]. In this pulsed radar system, a high-speed analog-to-digital converter (ADC) is required in a baseband receiver, because a wideband pulse signal is transmitted for obtaining high-range resolution. A time-interleaving technique with SAR ADC is the most feasible solution to realize both over GHz operation and middle resolution around 8 bit [3]–[17], however, it induces some mismatch issues among ADC elements (sub-ADCs) including offset, gain error, and timing skew [4]. Since the offset and gain mismatches are static errors, they can be easily estimated by DC input reference and corrected in digital domain. On the other hand, the timing-skew error cannot be solved by DC input because the errors due to timing skew appear differently depending on the input frequency. The timing skew is caused by misalignment of sampling edges in each sub-ADC, which generates spurs and degrades signal-to-noise distortion ratio (SNDR) of time-interleaved (TI)-ADC especially in higher frequency operation such as for radar applications.

To suppress the timing-skew errors, several calibration techniques are reported. In [5], two extra redundant sub-ADCs are employed to estimate the timing skews and align the sampling edges, however, additional sub-ADCs cause an area overhead. In addition, an increased load at a simultaneous sample and hold operations becomes a burden to an input buffer. The full digital calibration reported in [6] does not need extra analog circuits, however, a heavy digital calculation circuit is required, which occupies more than 40% of total area. Though these conventional calibration techniques can reduce the timing-skew errors in background, the additional circuit area is not negligible. In the pulsed radar baseband system-on-chip (SoC), just a small increase in ADC area makes a large impact on the total SoC area saving, because multiple ADCs are needed to implement a function of digital beamforming. In this pulsed radar system, eight-channel TI-ADCs are implemented, which occupies a large area of total baseband SoC. Hence, reducing an area overhead of calibration circuits is indispensable in such ADC-rich systems.

In this paper, a foreground timing-skew calibration with a low area overhead is described [18]. The technique estimates timing skew only by using a clock inverter, a few resistors, and a capacitor. Thus, the additional circuit for the calibration is considerably small. This area-efficient calibration contributes to reduce the total area of the pulsed radar baseband SoC with beamforming that requires multiple high-speed ADCs. The foreground calibration can be executed during periodical intervals prepared in a pulse signal transmission scheme to track temperature and voltage drifts, resulting in no system performance overhead. Considering the above facts, a fast foreground calibration is more suitable for applying to the radar systems than a background calibration whose execution time is unpredictable due to the signal dependence.

This paper is organized as follows. Section II describes considerations of ADC architecture for the pulsed radar systems. Section III presents design details of the proposed TI-ADC including timing-skew calibration. Section IV

Manuscript received February 12, 2017; revised May 11, 2017 and July 20, 2017; accepted July 20, 2017. This paper was approved by Guest Editor Deog-Kyoon Jeong. *(Corresponding author: Takuji Miki.)*

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Digital Object Identifier 10.1109/JSSC.2017.2732732

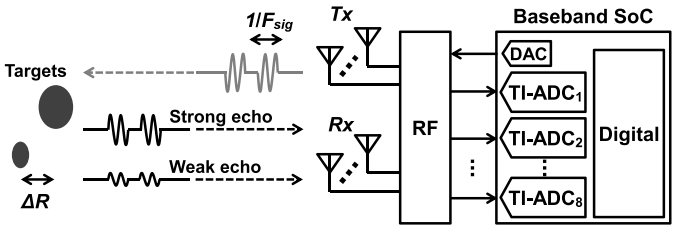


Fig. 1. Millimeter-wave pulsed radar system.

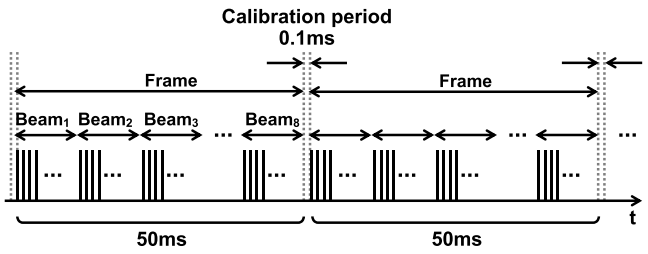


Fig. 2. Beam transmission sequence of the radar system and calibration period.

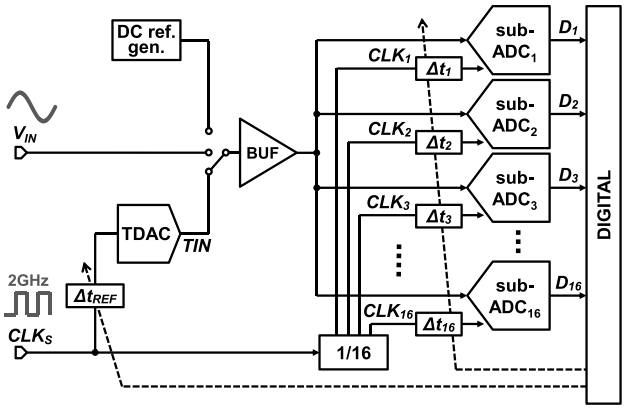


Fig. 3. TI-ADC architecture.

describes measurement results. Finally, Section V gives the conclusion.

II. Architectural Considerations of Baseband ADC for Pulsed Radar System

Fig. 1 shows a simplified sketch of the millimeter-wave pulsed radar system. This radar detects objects by transmitting a pulse signal and receiving the echo reflected by the targets. The range resolution ΔR is determined by the bandwidth of the pulse signal as $C/(2F_{\mathrm{sig}})$, where C is a speed of light and F_{sig} is a frequency of the pulse signal. To detect targets with 0.15-m spatial range using 1-GHz bandwidth pulse signal, a high-speed sampling operation of 2 GHz is required in the baseband ADC. After quantizing the echo signal by the ADC, a coherent summation is applied to the digitized data at the digital block of the baseband SoC, which relaxes SNR requirement of the ADC. However, the ADC has to receive the both strong and weak echoes at the same time, thus, a large dynamic range with more than 6-bit effective number of bits (ENOB) is needed. To achieve such high speed and middle resolution, TI SAR ADC is a practical solution for the ADC architecture, because flash-type ADC consumes high power to ensure that ENOB is more than 6 bit in every corner conditions [19]. However, in the TI architecture, several mismatch factors cause timing-skew errors. The first factor is sample/hold circuit mismatch between sub-ADCs such as a sampling switch transistor and a hold capacitor. Second, the clock path mismatch including clock buffer chains, and last one is input signal path mismatch. It is quite difficult to suppress these all factors completely by circuit design and layout. Although timing-skew calibration-free TI-ADCs are reported [15]–[17], they are not able to apply for higher sampling rate TI-ADCs with more number of interleaved sub-ADCs, which loses scalability of the interleaved architecture. Thus, the calibration technique for timing skew is required.

So far, background timing-skew calibration techniques are widely reported [5]–[14]. Though they do not need any explicit calibration period, the area overhead for the calibration is large such as redundant ADCs [5], [7]–[10]. Several techniques require one redundant comparator to reduce the area overhead. However, the required calibration time cannot be estimated due to signal dependence such as variance-based calibration technique which operates only when an input signal is within the window region [14]. On the other hand, foreground calibration can be realized with small area overhead and short calibration time, because its configuration is simple and desired reference signal can be given to the ADCs. In this pulsed radar baseband SoC, eight channels of ADCs are used to perform digital beamforming to estimate target directions accurately as shown in Fig. 1, which results in large size of total ADC area. Hence, the foreground timing-skew calibration with small area overhead is efficient approach to reduce total chip area.

Since the timing-skew errors depend on temperature drift, the foreground calibration is required to be executed periodically. In this system, eight beams, beam_1 to beam_8, are sequentially transmitted with various angles for wide range scanning and composing a frame. This frame is updated every 50 ms and the calibration is executed during an existing idle time in the frame update intervals of 0.1 ms, as shown in the conceptual sketch of Fig. 2. Thus, the foreground-calibration scheme does not sacrifice system performance in the radar system.

III. Circuit Design

A. Time-Interleaved ADC Architecture

Fig. 3 shows the block diagram of the proposed TI-ADC. This is basically composed of 16 sub-ADCs, input buffer, clock divider, and digital circuit. The Rx baseband signal from the RF chip with limited range of 0.4 V_{pp} is delivered to 16 sub-ADCs via the input buffer. The sub-ADCs are 8-bit SAR ADCs, and they are operated by 125-MHz clocks with 16 phases, CLK_1 to CLK_{16}, which are created by the clock divider from 2-GHz sampling clock, CLK_S. The TI digital outputs from each sub-ADC, D_1 to D_{16} are aligned and serialized in the digital block. The digital circuit also controls several calibrations for the ADC. The offset and gain mismatch values between sub-ADCs are estimated by giving DC reference voltage to the input of the ADC during the calibration period, and they are applied to each output in the digital block. A capacitor mismatch calibration in each SAR ADC is performed based on capacitor trimming technique [20]

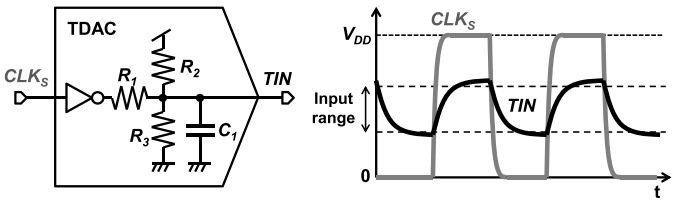


Fig. 4. Circuit schematic of TDAC and its operation waveform.

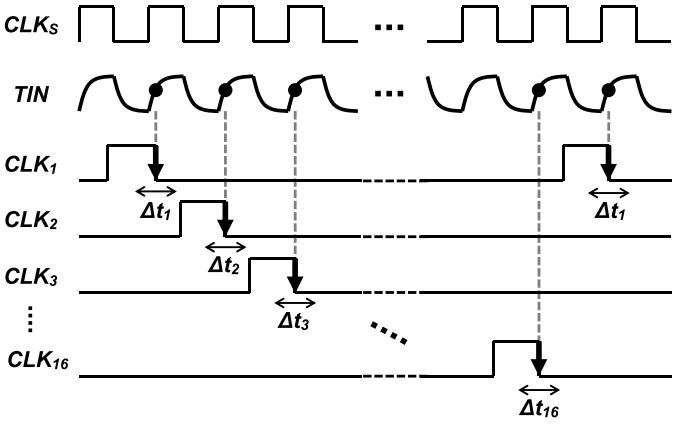


Fig. 5. Timing diagram of the skew calibration.

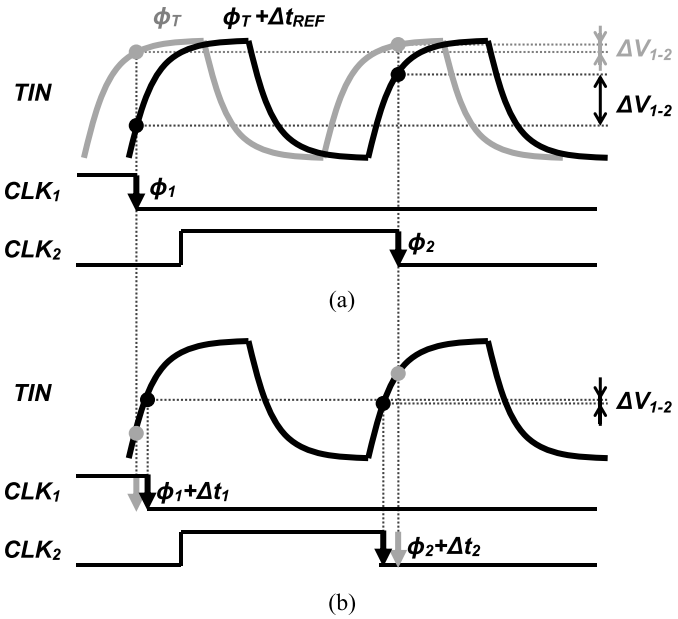


Fig. 6. Calibration sequence. (a) Searching maximum ΔV with TIN phase shift, (b) minimizing ΔV with clock phase shift.

at the startup sequence, which will be explained later. In addition to the typical configuration of TI-SAR ADC, several additional circuits for timing-skew calibration are implemented. As a timing reference, digital-to-analog converter (DAC) to generate analog test signal from clock signal, TDAC, is added to the input path. To estimate the timing skew due to the all mismatch factors including the input path, the timing reference signal has to pass the same way as the main signal path. Thus, the TDAC is implemented in front of the input buffer. The timing reference signal, TIN, is given to the input buffer by connecting the switch during the timing-skew calibration period. The switch is NMOS IO transistor with large size to reduce the ON-resistance and avoid the distortion. To adjust the clock phases and correct the timing skew, the variable delay lines (VDL) are inserted on each clock path. Fine tunable VDLs, Δt_1 to Δt_{16}, are for the divided clocks of each sub-ADC and coarse VDL, Δt_{REF}, is for the sampling clock CLKs which is input to the TDAC. All VDLs are controlled by the digital circuit.

B. Proposed Timing-Skew Calibration

The circuit schematic of TDAC is shown in Fig. 4. It consists of only clock inverter, several resistances, and capacitor. The 2-GHz clock, CLK_S, is input to the TDAC, and is low pass filtered by the R_1 and C_1. Its amplitude is shrunk to the range of the input buffer by the voltage divider of R_1 and R_2, R_1 and R_3. In the result, the output of the TDAC, TIN, becomes an *RC* step response waveform as illustrated in Fig. 4. The TIN is given to the input buffer as a timing reference for skew estimation during the calibration period.

Fig. 5 shows the timing diagram of the proposed timing-skew calibration. Each sub-ADC samples the slope of the TIN at the negative edges of CLK_1 to CLK_{16}. If the timing skew is not occurred, all sub-ADCs sample almost the same voltage of TIN and output the same digital values because the TIN is produced by CLK_S and has an ideal phase of 2-GHz clock. However, the timing skew induces each clock to sample the different points of TIN. Thus, the timing-skew calibration is to minimize the difference between the output values of sub-ADCs by adjusting each clock phase using VDL from Δt_1 to Δt_{16}.

Fig. 6 shows the proposed timing-skew calibration sequence which is an example of timing skew between CLK_1 and CLK_2. Each clock samples the different voltages of TIN at the phase of φ_1 and φ_2 due to timing skew. However, the voltage difference, ΔV_{1-2}, is too small when the settled points of TIN are sampled as shown in the gray line of the TIN phase φ_T in Fig. 6(a). All clock signals for the sub-ADCs are required to sample the steep points of TIN to estimate skew errors accurately. Then, at first, maximum voltage difference ΔV is searched by moving the phase of TIN with coarse VDL, Δt_{REF}, implemented in front of TDAC. Incrementing the delay value of Δt_{REF}, the phase of TIN is shifted and the voltage difference ΔV is changed. When the maximum ΔV is found as shown in the black line in Fig. 6(a), the phase shift of TIN is fixed. These sampling points include the highest slew rate in the slope of TIN, and it is required to be higher than the maximum slew rate of 1-GHz sine wave to remove skew errors at full-Nyquist input frequency. At this time, the slope direction is determined whether rise or fall, and is used for the control direction at the following process. After fixed TIN, the voltage difference, ΔV_{1-2}, is minimized by adjusting fine VDLs of Δt_1 and Δt_2 located in each clock path as shown in Fig. 6(b). These processes are actually applied to all clocks from CLK_1 to CLK_{16}. At the first step of the minimizing process, the median value of ΔV_{1-16} is defined. Next, each fine VDLs from Δt_1 to Δt_{16} is incremented or decremented

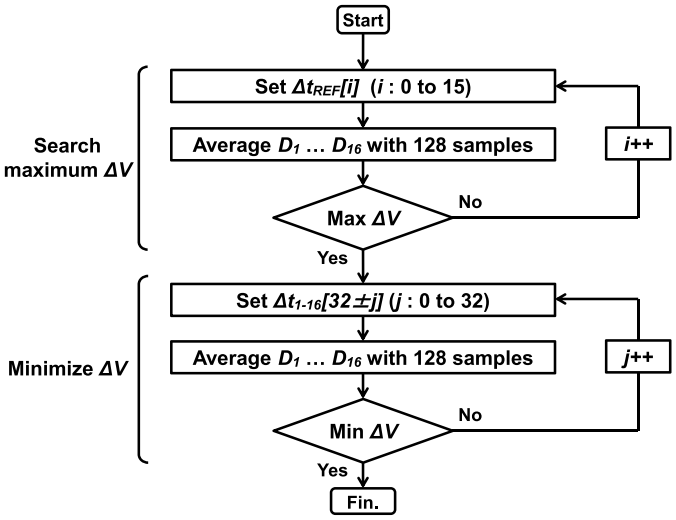
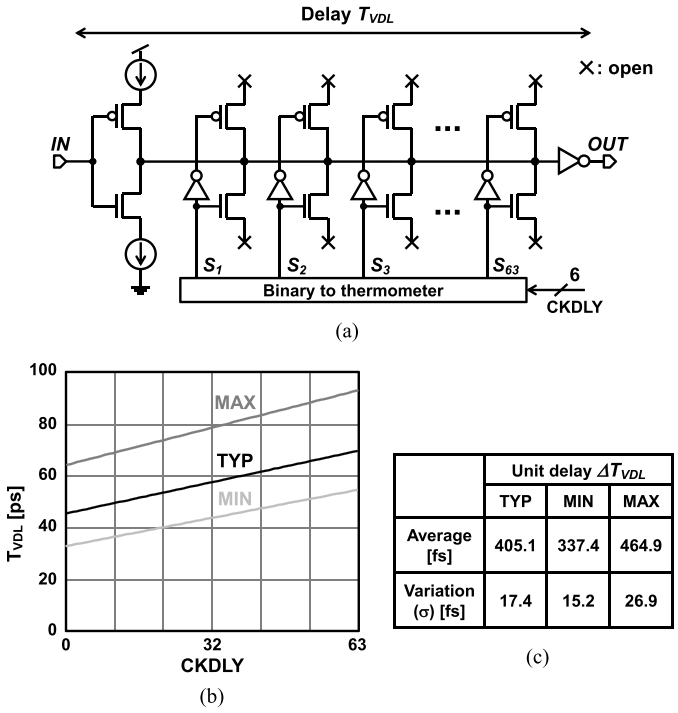


Fig. 7. Flowchart of the timing skew calibration scheme.

to reduce the distance between each output and the median value. In this way, the timing-skew calibration is completed when the output difference among all sub-ADCs, ΔV_{1-16}, is minimized.

The process-voltage-temperature (PVT) variation causes a degradation of the slew rate of the TIN slope. The design consideration of TDAC is to guarantee the maximum slew rate of the slope at the worst case PVT condition to be higher than that of the Nyquist input frequency of 1 GHz. Thus, the TDAC is designed by tuning internal R_1 and C_1 in Fig. 4 using post layout simulation with PVT corner conditions. The simulation is required to include the load capacitance of the input buffer and the ON-resistance of the switch implemented before the input buffer. The voltage and temperature drifts also shift the phase of TIN relative to the sub-ADC sampling clock. Thus, every periodical calibration starts from maximum ΔV searching process to track the drift.

Fig. 7 shows the timing-skew calibration procedure and required time to complete the calibration. In the both searching and minimizing process, each sampled point is averaged to filter out the random jitter and noise of the ADC. According to thermal noise simulation including on-chip phase-locked loop and the VDL, sampling jitter is estimated to be approximately 1 ps. Since 1 LSB error is caused by the sampling timing error of 500 fs in an 8-bit ADC with 1-GHz input, the sampling jitter of 1 ps must be suppressed to less than 1/2 to fix the calibration. In this design, 128-data averaging is performed to reduce the jitter and the ADC noise to less than 1/10, which is enough to stabilize the calibration scheme. Linear search is done to find maximum ΔV_{1-16} with incrementing the 4-bit delay control of coarse VDL from 0 to 15. The minimizing process starts from the center value of 6-bit delay controls of each fine VDLs. Since the control directions whether increment or decrement are already defined at the TIN moving process, the control range is less than 32. The total calibration scheme requires less than 10 000 clock cycle, which is 0.08 ms at 125-MHz operation of sub-ADCs. It is short enough to be operated in the existing calibration intervals in the beam transmission sequence as shown in Fig. 2,



	Unit delay ΔT_{VDL}		
	TYP	MIN	MAX
Average [fs]	405.1	337.4	464.9
Variation (σ) [fs]	17.4	15.2	26.9

(c)

Fig. 8. Variable delay line. (a) Circuit schematic. (b) Simulation result of delay time. (c) Summary of mismatch simulation.

which enables to track the temperature and supply voltage drift.

C. Variable Delay Line

Fig. 8(a) depicts the circuit schematic of the fine VDL for each clock path, Δt_1 to Δt_{16}. It consists of 63 CMOS capacitor units to realize variable delay control of 64 steps. The CMOS capacitor can be integrated with small area compared to the other variable delay circuits such as weak buffer chain with large channel length or method of moments capacitor array with trimming switches. The unit capacitor value corresponds to gate capacitance of CMOS transistor when delay enable signals, S_k (k:1, 2, . . . , 63), are "HI." Thus, the delay time of clock transition is determined by the number of activated gate capacitances. The unit delay time of fine VDL is approximately 400 fs at a typical condition, which means the maximum timing skew after calibration can be suppressed within 400 fs. It is an acceptable skew range to realize 8-bit resolution at 1-GHz input. To realize such fine delay step, minimum-size transistors are used in each CMOS capacitance unit. In addition, the opposite nodes to the common signal path are opened to reduce almost half of gate capacitor value, resulting in 400-fs delay per unit. The calibration range is ±12.5 ps with 64 steps, which is determined by a mismatch simulation between the sub-ADCs with several margins. The delay enable signal, S_n, is 63-bit thermometer code converted from 6-bit delay control signal, CKDLY[5:0]. Using CMOS-type as load capacitance, the VDL operates for both the rising and falling edges of clock signal. Then, similar delay change is generated at both edges to avoid too much duty cycle disturbance. In order to make the delay values stable under a temperature or power supply voltage

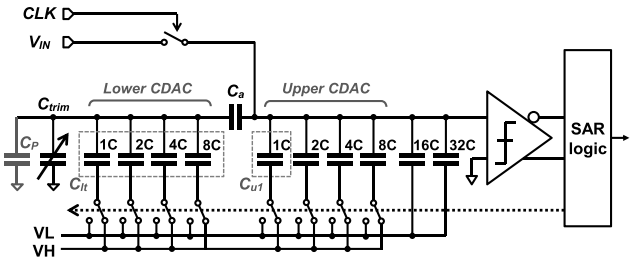


Fig. 9. SAR ADC configuration.

drift, constant current inverters are applied to drive the variable CMOS capacitors.

The post-layout simulation results of the fine VDL with typical case and corner conditions of MIN and MAX are shown in Fig. 8(b). MIN condition indicates FF process, $V_{\mathrm{DD}} = 1.2$ V and $-40°$ temperature, and MAX condition is SS process, $V_{\mathrm{DD}} = 1$ V and 125° temperature. The slope of the characteristic line for the delay time, T_{VDL}, is shifted at each corner condition, and the values of unit delay time, ΔT_{VDL}, at MIN and MAX are changed to approximately 340 and 460 fs, respectively. Fig. 8(c) shows the summary of mismatch simulation using Monte Carlo. The sigma values of the unit delay ΔT_{VDL} variation due to mismatch at the condition of TYP, MIN and MAX are 17.4, 15.2, and 26.9 fs, which are small relative to the average of the unit delay time, thus, mismatch and PVT variation do not induce much degradation of the skew calibration results.

Since the proposed calibration technique uses the slope of *RC*-filtered clock as a timing reference and estimates with digitized value, sampling range of the effective slope is wide compare with comparator-based estimation technique [13]. It enables to search the effective sampling point of TIN with coarse step when the phase is shifted due to temperature and voltage drift, which reduces the searching step and calibration time. Thus, the unit delay time of the coarse VDL for adjusting the phase of TIN is 12.5 ps. The coarse VDL is based on the fine VDL configuration, and the unit delay is realized by connecting 32 CMOS capacitors with common control signal. The delay control signal of coarse VDL is 4 bit, thus, the controllable range of TIN phase is ± 100 ps. Since the VDL is composed of multiple inverters, extra jitter is injected into the sampling clock. Thermal noise simulation of post layout VDL indicates the extra jitter is about 200 fs in the worst condition.

D. SAR ADC

An 8-bit SAR ADC architecture is employed, as shown in Fig. 9. It is traditional configuration including binary-weighted capacitive-DAC (CDAC), comparator, sampling switch, and SAR logic. The SAR ADC employs top-plate sampling to eliminate sample/hold operation of CDAC and reduce the number of SAR cycles. The sampling switch is bootstrap type [21] to realize low distortion and small size of switch transistor, thus, charge injection and clock feedthrough can be suppressed. The CDAC is divided into upper and lower CDAC with connecting capacitor C_a to reduce the total amount of capacitors. Both upper and lower CDACs have 4-bit binary array whose bottom node is connected to VH or VL controlled by the SAR logic. The switching technique of the CDAC is based on a split-capacitor type as described in [22]. To receive an input signal with 0.4 V_{pp} range which is about a quarter of rail-to-rail, extra 2-bit MSB capacitors of 16C and 32C with fixed bottom node are implemented in the upper CDAC. The unit capacitor value C is 6 fF to reduce the settling time and achieve fast operation. In SAR ADC, capacitor mismatch in CDAC causes non-linearity error and degrades integral non-linearity (INL) and differential non-linearity (DNL). The largest error comes from the mismatch between upper and lower CDAC, which induces a code-dependent errors at every 16 LSB and generates spurs on the output spectrum. It is quite difficult to eliminate the mismatch between the both CDAC with appropriate value of connecting capacitor C_a during circuit design, because the parasitic capacitance at lower CDAC C_p and process mismatch cannot be estimated. Thus, trimming capacitor C_{trim} is added to the lower CDAC to calibrate capacitance mismatch. The C_{trim} is adjusted to equalize the total capacitor value of lower CDAC C_{lt} with series C_a and LSB capacitor in upper CDAC C_{u1} as shown in the following equation

$$C_{u1} = \frac{C_a \cdot (C_{lt} + C_{\mathrm{trim}})}{C_a + (C_{lt} + C_{\mathrm{trim}})}. \tag{1}$$

The capacitor mismatch calibration is executed at startup sequence, when the system is powered ON. Since the calibration changes the total capacitor value of CDAC by trimming the C_{trim}, the output gain is also varied. It is different in each sub-ADC, resulting in gain mismatch among sub-ADCs. The gain mismatch is also caused by the reference voltage shift, VH and VL. Moreover, comparator offset in each SAR ADC causes offset mismatch between sub-ADCs. These errors depend on temperature and voltage drift unlike the capacitor mismatch, thus, the periodical calibration is needed. To calibrate these errors, foreground calibration using DC voltage reference input can be executed because there is the calibration period in this radar system as with the timing-skew calibration. Thus, the offset and gain values of all sub-ADCs are estimated in foreground during the same calibration period in the beam transmission sequence, and corrected in digital domain.

E. Input Buffer

The Rx baseband signal from the RF chip and the output signal of the TDAC are distributed to each sub-ADC via the input buffer. It is required to drive more than 1-GHz signal with large output load due to the sampling CDAC capacitor of SAR ADC and long-distance signal paths for equal-length wiring among 16 sub-ADCs. Moreover, input signal swing is specified for less than 0.2 Vpp, which is too small to obtain enough SNR above 6 bit. Thus, as a design consideration of the input buffer, some gain is needed to amplify the narrow input swing. Fig. 10(a) shows the circuit schematic of the input buffer. In this topology, the output gain is theoretically determined by R_2/R_1, which is more robust against PVT variation and mismatch compared to widely used buffer topology whose gain is determined by g_m and resistor

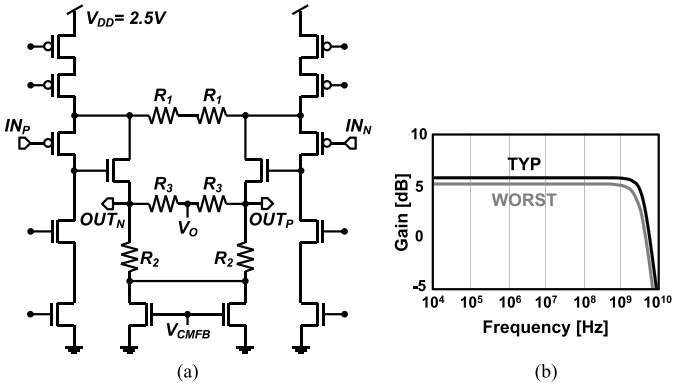


Fig. 10. Input buffer (a) circuit schematic and (b) bandwidth simulation result with corner condition.

values [23]. However, the R_2 cannot be much enlarged because output resistance must be as small as possible to realize wide bandwidth. In the practical design, the R_2 is double the value of the R_1, which is a minimum output resistance value to satisfy 1-GHz bandwidth. Fig. 10(b) shows the simulation result of gain versus frequency with PVT variation. Over 1-GHz bandwidth is obtained at the worst corner condition. The output gain, (OUT_P-OUT_N)/(IN_P-IN_N), is approximately 2, thus the output signal swing of the input buffer becomes 0.4 Vpp. The output common mode V_O, which is a median value of OUT_P and OUT_N using voltage divider R_3, is fed back to the V_{CMFB} via output common mode reference amplifier. To ensure the constancy of the current and suppress the distortion of the output signal, cascade transistors are inserted between current sources and input transistors, resulting in high linearity of 54-dB SNDR by post-layout simulation for the input buffer. Due to the stacked topology, power supply for the input buffer is 2.5 V, which increases power consumption as described in the measurement result in Section IV.

IV. Measurement Results

The TI-SAR ADC was embedded in the baseband SoC fabricated in 40-nm CMOS process. The microphotograph of the chip is shown in Fig. 11. The zoomed-in view of the TI-ADC and layout image of the TDAC are also shown in Fig. 11. The eight channels of TI-ADCs for implementation of digital beamforming occupy a large area of total baseband chip. The area of single TI-ADC is 1000 μm $\times$ 540 μm, including 16 sub-ADCs, input buffer, reference generator, clock generator, and calibration circuits. Since the calibration circuit of TDAC consists of only several resistors and capacitor, its area is 0.0022 mm^2 that occupies only 0.4% of total area. The calibration control logic with less than 0.002 mm^2 is implemented in the post-digital processing area. The both fine and coarse VDLs, Δt_1 to Δt_{16} and Δt_{REF}, occupy 0.004 mm^2, thus, the total additional area for timing-skew calibration is 0.0082 mm^2, which is only 1.5% of the TI-ADC.

Fig. 12 shows the measured output during the calibration period, when the reference signal for timing-skew calibration, TIN, is input to the TI-ADC. The TI output code from

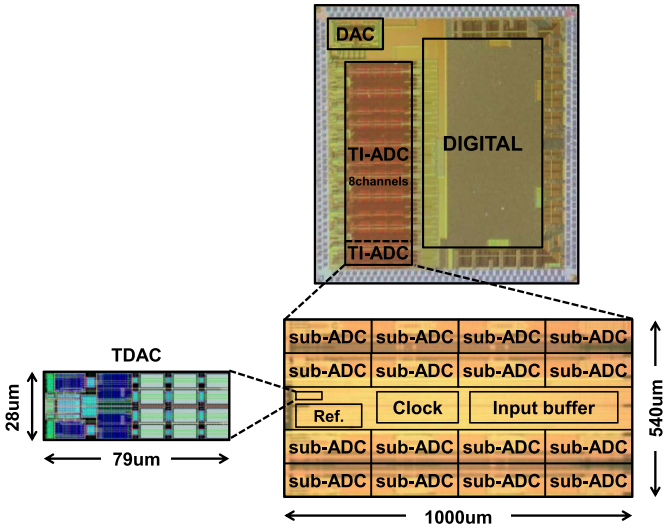


Fig. 11. Microphotograph of the radar baseband SoC and layout image of the calibration circuit.

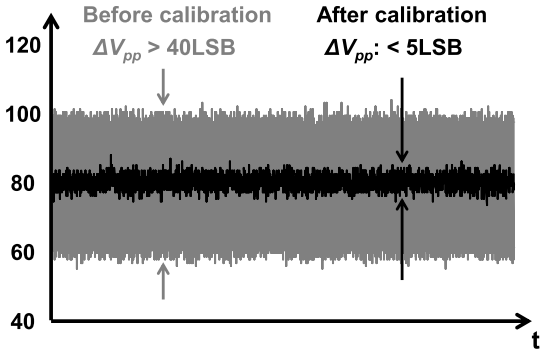
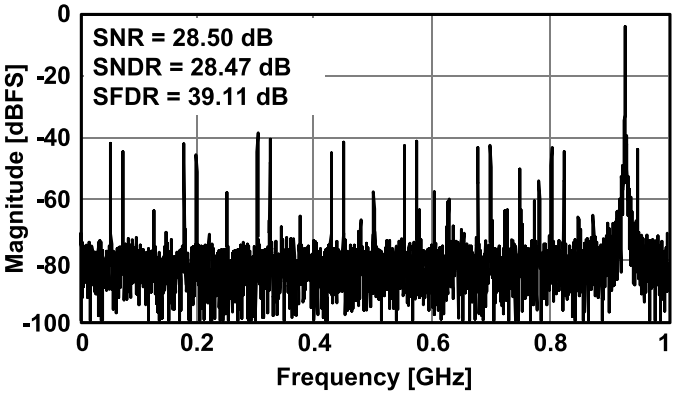


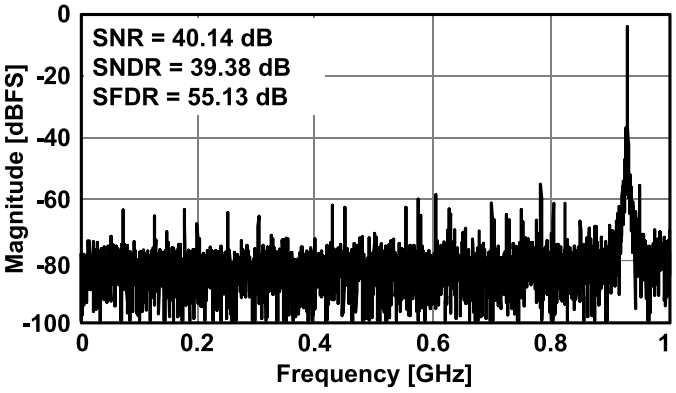
Fig. 12. Measured output during timing skew calibration period.

sub-ADC_1 to sub-ADC_{16} without the timing-skew calibration is a broad output range with more than 40 LSB, Δv_{1-16}, which indicates that each sub-ADC samples different points of TIN due to timing skew. The proposed calibration adjusts the delay lines from Δt_1 to Δt_{16}, by itself, and shrinks the Δv_{1-16} to narrow range with less than 5 LSB at peak to peak. This value includes thermal noise only, thus, almost the same output values are obtained from all sub-ADCs after 128 times averaging.

Fig. 13 shows the output spectrum of the proposed TI-ADC with before and after executing the timing-skew calibration. The TI-ADC operates at 2 GHz with near Nyquist frequency of 927-MHz sine-wave input. The supply voltage VDD is 1.1 V. Offset and gain error between sub-ADCs and capacitor mismatch in SAR ADC have already removed by the calibration. Without timing-skew calibration, the output fast Fourier transform (FFT) spectrum of the TI-ADC is shown in Fig. 13(a). Many spurs are appeared in the output spectrum and degrade the SNR, SNDR, and spurious-free dynamic range (SFDR). These spurs are caused by the timing-skew errors, which are generated at the frequency of $F_s/M \pm F_{sig}$, where F_s, F_{sig}, and M are sampling frequency, input frequency, and the number of interleaved sub-ADCs, respectively. Fig. 13(b) shows the FFT result after the proposed



(a)



(b)

Fig. 13. Measured FFT spectrum. (a) Before timing skew calibration. (b) After timing skew calibration.

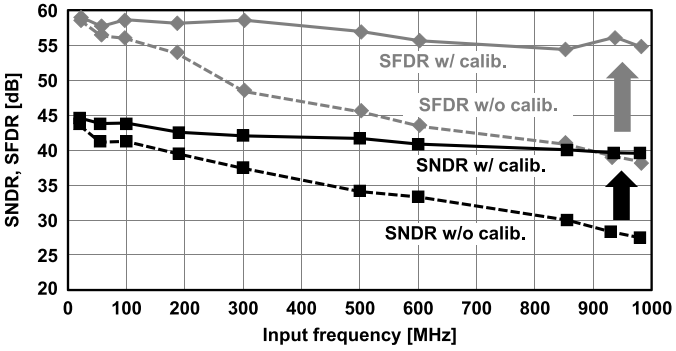


Fig. 14. Measured SNDR and SFDR versus input frequency.

timing-skew calibration. The spurs are compressed and the calibration improves the SNR, SNDR, and SFDR by 11.6, 10.9, and 16 dB, respectively.

Fig. 14 shows the measured SNDR and SFDR versus input frequency. When the timing-skew calibration is not applied, the SNDR and SFDR are degraded in high input frequency area. However, the calibration improves them, and the TI-ADC achieves the SNDR of 39.4 dB and the SFDR of 55.1 dB at Nyquist input frequency.

The measured SNDR with PVT variation is plotted in Fig. 15. Eight samples of each process corner, FF and SS, were measured with ±10% voltage change and temperature condition from −40° to 125°. From these plots, 6-bit ENOB specification is satisfied in every corner conditions. Fig. 16

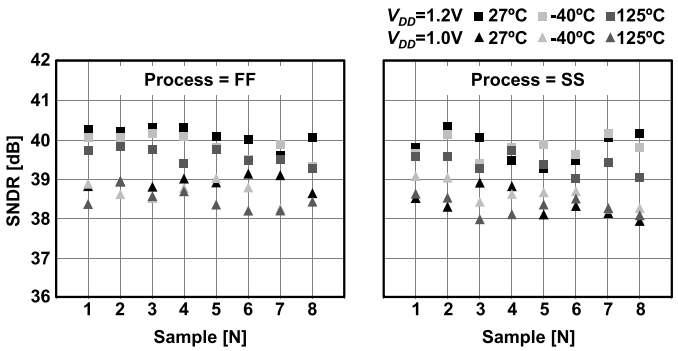


Fig. 15. Measured SNDR with PVT variation.

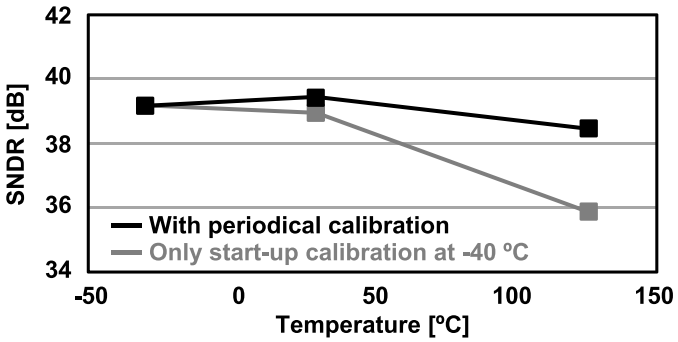


Fig. 16. Periodical calibration against temperature drift.

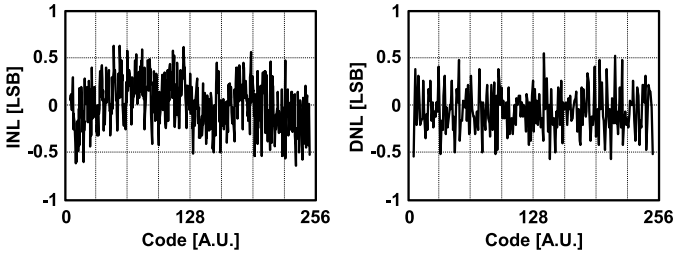


Fig. 17. Measured INL and DNL.

shows the evaluation of robustness against temperature drift. This experiment assumes that the power is ON at −40° and heats up to 125°. When the calibration is only executed in startup sequence at cold condition, the SNDR is decreased by 3 dB and below 6-bit ENOB at hot condition. The breakdown of the SNDR degradation is that 2 dB is caused by offset and gain value drifts, and the other is by timing skew. However, periodical re-calibration with every 50 ms keeps the SNDR above 6 bit across temperature drift.

Fig. 17 shows the DC characteristic of the TI-ADC. The INL and DNL are measured to examine a linearity which might be degraded by offset and gain mismatches among the sub-ADCs and capacitance mismatch in each SAR ADC. The startup capacitance mismatch calibration and periodical offset and gain calibration keep the INL and DNL within +/−0.6 LSB.

The power consumption breakdown is shown in Fig. 18. The total power of the TI-ADC is 54.2 mW including reference buffer and input buffer. The input buffer consumes 55% of total power. Since the TDAC is only activated during the calibration

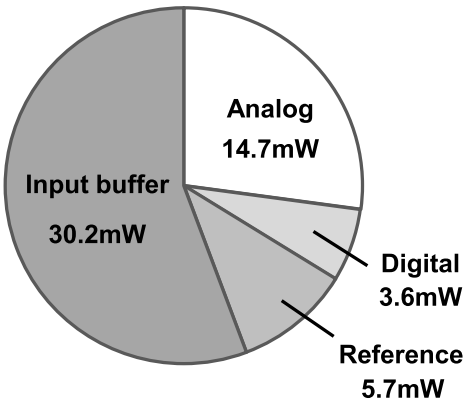


Fig. 18. Power break down.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	ISSCC 2014 [6]	ISSCC 2013 [14]	JSSC 2013 [5]
Technology [nm]	40	40	65	65
Sampling rate [GS/s]	2	1.62	3.6	2.8
Power [mW]	54.2	93	795	44.6 *1
Area [mm^2]	0.54	0.83	7.4	0.55 *1
Input range [Vpp]	0.4	1	1.2	1.8
$SNDR_{@Nyquist}$ [dB]	39.4	48	47	48
$SFDR_{@Nyquist}$ [dB]	55	62	50	55
$FoM_{@Nyquist}$ [fJ/step]	355	283	1207	78 *1
Calibration circuit area [mm^2]	0.0082	0.332 *3	- No calib.	0.013 *2

*1 : Without input buffer and references
*2 : Estimated area of two additional ADCs
*3 : Including offset and gain calibration

period, the power overhead for the calibration is less than 0.1% when the frame cycle is 50 ms.

Table I shows the performance summary and comparison with other TI-SAR ADCs which operate around 2 GS/s and are likely to be used for industrial applications. Due to the limited input range of only 0.4 V_{pp}, the SNDR of the TI-ADC is lower than the other works. However, the calibration area overhead is smaller compared to the other timing-skew calibration techniques such as full digital calibration and additional redundant ADCs.

V. CONCLUSION

An area-efficient timing-skew calibration in high-speed TI-ADC for pulsed radar system is demonstrated. A simple DAC is added to an input path to generate a reference signal that is utilized for timing-skew estimation. Hence, the additional circuit for the calibration is significantly smaller than the other background techniques. Since the foreground calibration runs during the calibration period in the pulse transmission sequence, it does not cause system overhead. The 2-GS/s 8-bit TI-ADCs are embedded on the pulsed radar baseband SoC in 40-nm CMOS. Owing to the calibration technique, the TI-ADC successfully achieves the SNDR and SFDR of 39 and 55 dB at Nyquist input frequency under system evaluation environment.

ACKNOWLEDGMENT

The authors would like to thank Associate Prof. N. Miura from Kobe University, Kobe, Japan, for his helpful comments and suggestions.

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