A Single-Bit 500 kHz-10 MHz Multimode Power-Performance Scalable 83-to-67 dB DR CT$\Delta\Sigma$ for SDR in 90 nm Digital CMOS

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***Abstract*—Wireless environments, high data rates and increased digitization require A/D converters with high dynamic range and large bandwidth at the lowest possible power consumption. A fully flexible continuous-time (CT) $\Delta\Sigma$ with programmable bandwidth, resolution and power consumption in 1.2 V 90 nm CMOS is presented able to satisfy those demands. By introducing flexibility into the core building blocks, a DR of 67/72/78/83 dB is achieved in maximum performance mode for WLAN, DVB, UMTS and BT for a power consumption of 6.8/5.5/6.4/5.0 mW, respectively. GSM operation is also feasible with a DR of 87 dB. For a given bandwidth, the flexibility allows to obtain the lowest power consumption for a desired performance. The overall energy efficiency is reached with a single-bit CT$\Delta\Sigma$ modulator avoiding high speed DEM circuits. Its low power consumption especially for high bandwidths is realized thanks to architecture and circuit level optimization. Linearity enhanced integrators, a threshold configurable comparator enabling loop delay compensation and optimized DAC implementations for jitter and avoiding signal dependency in the feedback pulses due to a large voltage swing are employed to increase the performance. The respective FOM equals 0.24/0.27/0.41/0.85 pJ per conversion.**

***Index Terms*—Continuous-time $\Delta\Sigma$, flexible, low power, multimode, reconfigurable, software-defined-radio.**

I. Introduction

THE increasing number of wireless standards drives the need for flexible receiver systems that can operate optimally in different modes [1]. Such a fully reconfigurable receiver should handle present and future standards seamlessly and should not consume more power than dictated by the required performance. This energy scalability feature is a key enabler for software-defined radio (SDR) as the total power consumption is defined not only by the standard but also by the channel conditions and user preferences. The resulting variety in standard requirements imposes therefore highly flexible analog circuitry.

To date, most multimode CT$\Delta\Sigma$ implementations are able to handle up to three discrete modes [4]–[6]. CT$\Delta\Sigma$ are preferred when a large bandwidth (BW) needs to be covered as they do not suffer from severe settling time requirements present in SC-integrators [2], [3]. They also offer an inherent anti-alias filter function. A recent implementation [7] proposes a CT$\Delta\Sigma$ with a large continuous range of signal BW and DR. All these designs introduce flexibility by employing a fixed topology with reconfigurable passive component (R and C) arrays and tunable bias current. However, since the specifications of the building blocks (e.g., OTA) are different depending on the standard and desired resolution, the optimal power–performance tradeoff is not achieved.

This paper presents a fully flexible CT$\Delta\Sigma$, programmable over all signal bandwidths from 500 kHz (Bluetooth) up to 10 MHz (WLAN) illustrating multimode operation. A high resolution (DR from 83 dB to 67 dB) with low power consumption is obtained thanks to large flexibility in the core circuitry (OTA, DAC, and quantizer) of the modulator. At circuit level, the complexity can be controlled if modular structures are used consisting of replicating basic architectures [8], [9]. Such an approach allows efficient digital control and limits the complexity of both layout and multimode verification. Hence, by implementing every building block as a matrix of switchable unit cells, the lowest power consumption for a specific resolution and bandwidth is reached for a given architecture choice. As will be illustrated for UMTS, lowering the resolution by 1 bit can save one third in power. For all modes, figures-of-merit (FOMs) well below 1 pJ/conversion are achieved [10].

The architecture choice will obviously limit the achieved FOM. Section II illustrates that a feedback topology looks more suitable for large BW–moderate resolution while feedforward is more appropriate for high resolution–low BW applications. However, this paper focuses on reconfigurability at circuit level, guaranteeing optimal bias conditions over a large tuning range. Therefore, a fixed architecture optimized for large BW standards has been selected. In order to improve the FOM for lower bandwidths, the reconfigurability should also be extended to the architectural level, which, however, is not considered in this work.

Apart from introducing flexibility which optimizes the efficiency for a given architecture, the CT$\Delta\Sigma$ architecture is optimized as well. Special interest is given to improve the power efficiency of large-bandwidth CT$\Delta\Sigma$ which are required to cope with the high data rates and increased digitization present in future wireless systems. Previous reported large-BW CT$\Delta\Sigma$ designs (10–20 MHz) [11]–[18], which consume 20–100 mW de-

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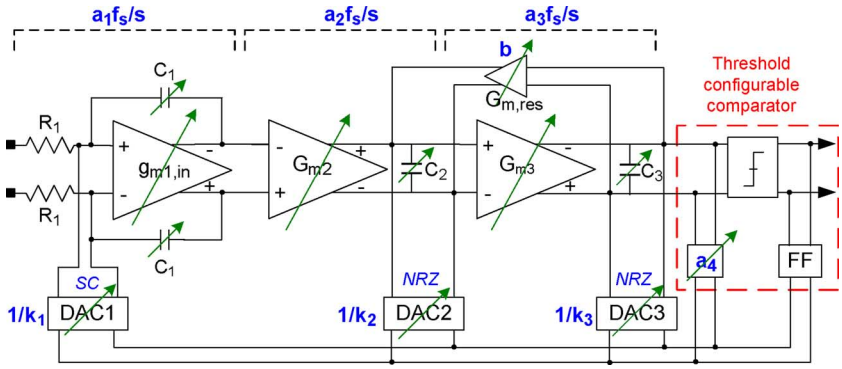

Fig. 1. Feedback architecture of the third-order flexible CT$\Delta\Sigma$.

pendent on their resolution, all have in common that they use multibit solutions. They require feedback DACs as linear as the desired resolution. Typically, dynamic element matching (DEM) is applied which adds to the overall complexity and power consumption especially when it operates at high speed. This work shows that for moderate resolutions up to 11 bits, although the bandwidth is high (10 MHz), a single-bit architecture provides a power efficient solution [19]. The lower implementation margin (loss in resolution compared to SQNR due to circuit nonidealities) is compensated for by innovations at circuit level such as linearity enhanced integrators and a threshold configurable comparator enabling perfect loop delay compensation. The presented design succeeds in keeping the total power consumption below 7 mW for all modes. High efficiency together with high flexibility makes this design an attractive candidate for future SDR implementations. Section II discusses the architecture of the modulator. In Section III, the flexibility strategy is elaborated and circuit level details are presented. Section IV reveals integration and timing details and Section V presents measurement results and compares them with the state-of-the-art.

II. CT$\Delta\Sigma$ Architecture Optimization

A. Design of the Loop Filter

Fig. 1 presents the architecture of the single-bit CT$\Delta\Sigma$ which consists of a third-order loop filter with distributed feedback. Due to local feedback, a resonator is created and two zeros of the noise transfer function (NTF) are moved from DC to the edge of the signal band creating a notch in the NTF. This results in a more uniform suppression of the quantization noise over the entire signal band. The specifications for the different integrators of the loop filter depend on the loop filter topology which can be implemented as feedforward or feedback. An in-depth analysis can be found in literature [20].

1) Motivation for Feedback Topology: In a feedback topology, the gain–bandwidth product (GBW) relaxes the further away from the quantizer. Therefore, the first integrator will only have a moderate GBW specification opposed to very strict specifications for noise and linearity. The feedback topology hence allows decoupling high speed from high DR requirements which is especially beneficial for large BW applications. However, a feedback topology has one major drawback: the integrator output nodes contain a significant signal component as well as quantization noise. Therefore, the unity gain frequency of the first integrator has to be reduced leading to less suppression of noise and distortion of the second integrator but remains still significantly higher than the bandwidth.

This explains the fundamental tradeoff at architectural level: a feedback topology is more suitable for large BW–moderate resolution while feedforward is more appropriate for high resolution–low BW applications. However, CT$\Delta\Sigma$ with a low BW only consume a few mW while current state-of-the-art CT$\Delta\Sigma$ having a large BW consume several tens of mW. Because the presented reconfigurable CT$\Delta\Sigma$ handles both applications, the lowest average power consumption can be achieved when optimizing for large BW standards. The decoupling of speed and DR requirements is hence the dominant factor in the selection of the feedback topology.

As illustration, a system level simulation has been performed assuming that all integrators consist of a closed loop RC-structure for the case of optimal coefficients normalized to the sampling frequency (0.3; 0.3; 1) and $k_i = 2$. These coefficient change dependent on the scale factors k_i which determine the signal swing while maintaining the same NTF. Fig. 2 plots the GBW for the three integrators for WLAN. The specification indeed becomes stricter for the last integrator. It is important that the absolute frequencies depend on the effective coefficient values. The closer this coefficient is chosen to the stability boundary, the tougher the specification becomes. Typically, the higher order pole should be x times higher than the integrator pole. This factor hence depends on the chosen coefficients. Because the last coefficient in a feedback is the highest, also the bandwidth specification will be the highest for a given x. Finally, the absolute bandwidth specification also depends on the loop delay compensation set by a_4. This is explained in [21] where finite GBW is modeled as finite gain and a delay. This delay affects the phase margin of the loop filter and can be compensated thanks to loop delay compensation.

Fig. 3 plots the noise specifications and proves an opposite trend for nonidealities affecting DR. The specifications are more strict for the first integrator as this error is suppressed for subsequent integrators by the gain of previous stages, thereby illustrating the decoupling property.

Another property of the feedback topology is the optimal signal transfer function (STF). The STF is flat in-band and

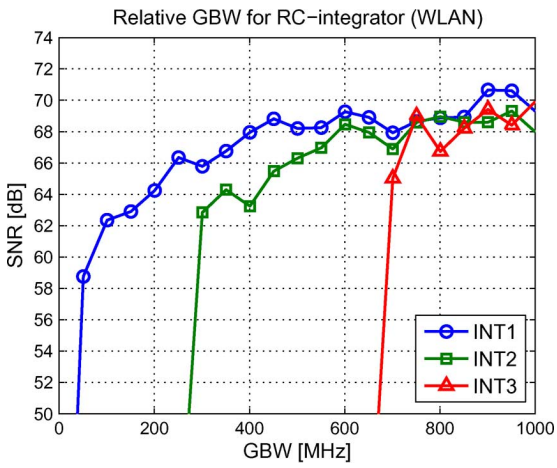

Fig. 2. Relative GBW for a third-order RC-integrator for WLAN example. The GBW clearly increases for the integrator closest to the quantizer.

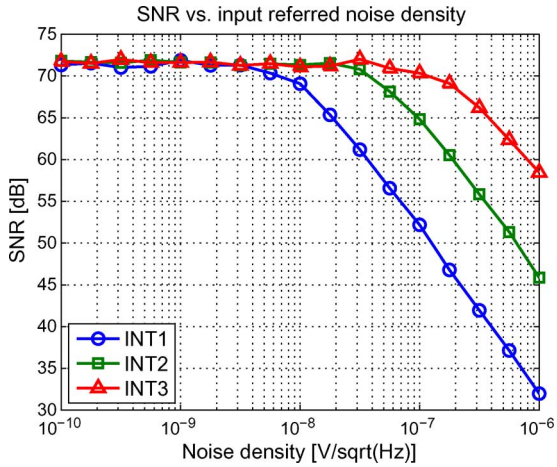

Fig. 3. Noise specifications for a third-order RC-integrator for WLAN example. The specification relaxes for the integrator closest to the quantizer.

has the maximum roll-off out-of-band, resulting in better anti-aliasing properties compared to feedforward topologies. In addition, the large BW and thus power-hungry summing amplifier for feedforward paths at the input of the quantizer are avoided.

2) Integrator Type Selection: The decoupling property of the feedback architecture results in high DR and moderate GBW specifications for the first integrator. Therefore, an OTA-RC stage is selected. The reduced speed requirement is beneficial to limit the power consumption of this first integrator. Noise and linearity requirements are relaxed for the successive stages as they are suppressed by the loop gain of the previous stages. By appropriately choosing the scale factors k_i, the signal swing can be reduced such that G_m-C integrators can handle the required specifications in a power-efficient way. Integrators 2 and 3 are therefore implemented as G_m-C stages. Especially for the last integrator, this open-loop structure is desirable as it has the most relaxed dynamic range requirements but the toughest bandwidth requirements.

3) Behavioral Modeling: Finally, extensive behavioral modeling has been performed to derive specifications for all building block parameters for various standards. For an OTA-RC stage, it is crucial to consider the effect of nonlinearities and finite GBW

TABLE I
INTEGRATOR SPECIFICATIONS OF THE THIRD-ORDER FEEDBACK CT$\Delta\Sigma$

Specification	UMTS	WLAN
SNDR system level	13bit=80dB	11bit=68dB
BW IQ	1.92MHz	10MHz
OSR	64	32
f_s	245.76MHz	640MHz
DC gain	60dB	50dB
OTA-RC integrator 1		
GBW	200MHz=0.8f_s	450MHz=0.7f_s
Noise density k_1=1	20nV/$\sqrt{Hz}$	20nV/$\sqrt{Hz}$
Noise density k_1=2	10nV/$\sqrt{Hz}$	10nV/$\sqrt{Hz}$
Input distortion	*Ok if good virtual ground*	
Output distortion	*Ok if appropriate output swing*	
$G_m - C$ *integrator 2*		
Int. pole f_{int} k_2=2	11.7MHz	30.5 MHz
Second pole k_2=2	70MHz	180 MHz
Noise density k_2=2	95nV/$\sqrt{Hz}$	55nV/$\sqrt{Hz}$
Noise density k_2=3	55nV/$\sqrt{Hz}$	35nV/$\sqrt{Hz}$
Distortion: IIP3 k_2=2	22dBV	20dBV
Distortion: IIP3 k_2=3	17dBV	15 dBV
$G_m - C$ *integrator 3*		
Int. pole f_{int} k_3=2	19.6MHz	56MHz
Second pole k_3=2	78.4MHz	204MHz
Noise density k_3=2	600nV/$\sqrt{Hz}$	250nV/$\sqrt{Hz}$
Noise density k_3=3	400nV/$\sqrt{Hz}$	150nV/$\sqrt{Hz}$
Distortion: IIP3 k_3=2	15dBV	17dBV
Distortion: IIP3 k_3=3	10dBV	12dBV

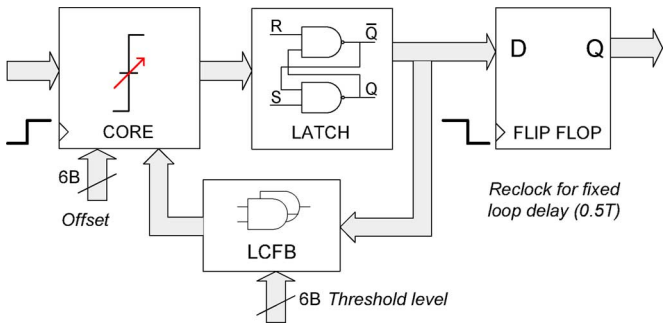

Fig. 4. Block diagram of the quantizer with loop delay compensation. The local feedback coefficient is implemented by shifting the threshold of the comparator: the output decision is fed back to reconfigure the new threshold. The absolute value of the threshold is known because of the fixed loop delay.

together because the GBW determines the quality of the virtual ground at higher frequencies. This is especially important in oversampled systems. As illustration, all integrator specifications for two relevant standards are summarized in Table I. Also the impact of programmable scaling factors k_i becomes clear. Consequently, the optimal noise versus linearity tradeoff is found by adapting the signal swing on the internal nodes at the input of the G_m-C integrators. The power consumption of those integrators hence becomes adaptive based on the channel conditions and desired performance.

B. Single-Bit Quantizer With Perfect Loop Delay Compensation

In continuous-time modulators, loop delay impacts the stability [22]. A common technique is to insert an extra local feedback path a_4 around the quantizer (Fig. 1) to alleviate performance degradation. This enhancement is, however, only optimal

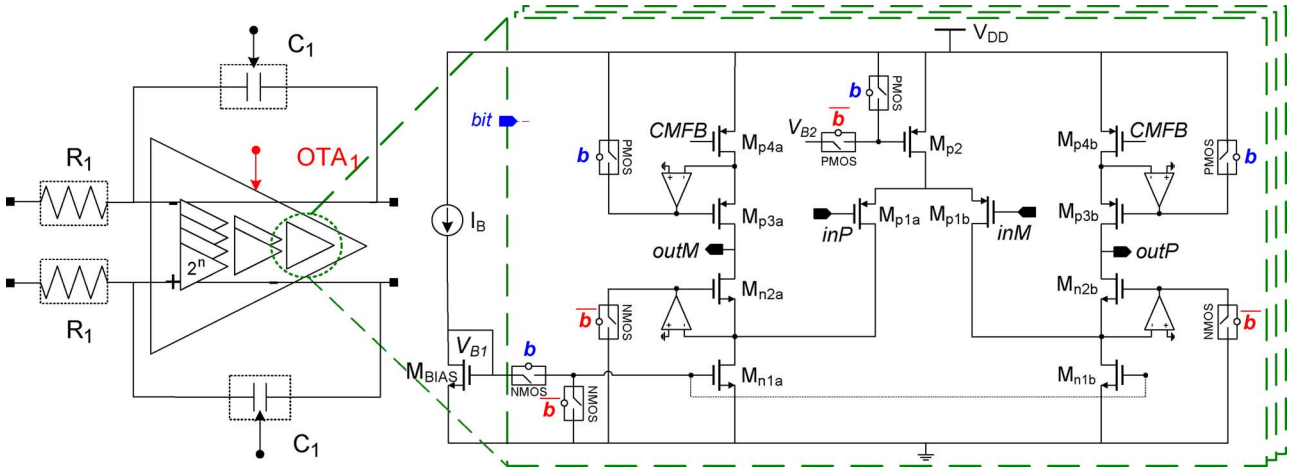

Fig. 5. Flexible OTA-RC integrator consisting of a fixed resistor, a capacitor bank, and a reconfigurable OTA. The OTA is split up in a matrix of switchable unit cells based on a gain-boosted folded cascode.

if the loop delay is constant. The output of the quantizer is therefore reclocked in a flip-flop with half a period delay, avoiding any signal dependency due to comparator settling (Fig. 4). The single-bit quantizer uses a threshold-configurable comparator whose threshold adaptation provides the direct feedback path a_4 needed for loop delay compensation [19]. In this way, the feedback DAC is inherently present in the quantizer and can be implemented using a capacitor and a switch. Therefore, a power-hungry summer before the quantizer can be avoided. The operation principle can be described as follows. When the comparator has settled, the output decision is captured in the latch. This output is fed back instantaneously as it determines whether a positive or negative threshold shift is required at the next sampling instant. The absolute value of the threshold shift corresponds to the feedback value set by a_4 which remains constant due to the fixed loop delay. While the comparator is resetting, the threshold can be reconfigured by activating the capacitance value corresponding a_4 either left or right dependent on the decision of the quantizer. Finally, offset correction is possible using the same technique of threshold configuration. Since this error is suppressed by the loop gain, no influence on the resolution due to offset is expected.

C. Feedback DACs

Obviously, no DEM is required as a single-bit DAC is inherently linear. Apart from linearity, clock jitter is crucial when designing the first feedback DAC. The error on the feedback charge is not suppressed by any loop gain and has therefore a direct impact on the modulator's resolution, resulting in an increased noise floor in the spectrum. To alleviate jitter, a switched-capacitor implementation (SC) has been selected for the first feedback DAC [4], [23]. Unfortunately, this stresses the linearity and GBW requirements of the first integrator but this is indispensable as jitter would deteriorate the performance too much, justifying a slight increase in power consumption. Note that the first integrator is still CT maintaining the anti-aliasing property. Finally, the SC-DAC is easily integrated with an OTA-RC integrator using the virtual ground.

Because of the reduced jitter sensitivity of the second and third DAC, these DACs have been implemented as switched-current non-return-to-zero (NRZ) DACs. Their current is fed back into a low impedance node (source cascode) of the G_m-C integrators.

III. Flexible Circuits for a Multimode Power–Performance Scalable CT$\Delta\Sigma$

A. Flexibility Approach

Traditionally, the sampling frequency and the filter coefficients are modified at system level. The highest sampling frequency is 640 MHz (WLAN) and is scaled down for other standards according to the desired OSR. To control the bandwidth, the local resonator branch is tuned to optimally place the notches of the noise transfer function. In this design, also the feedback scaling coefficients k_i are scalable up to a factor three. This enables independent control of the internal integrator nodes allowing the best noise–linearity tradeoff dependent on the signal conditioning. To further enhance the flexibility, extensive reconfigurability is introduced at circuit level. This is achieved by bringing this flexibility into the core of all building blocks in combination with passive component arrays and adjustable biasing. As a starting point, the design with all the toughest specifications is selected and is split into a matrix of switchable unit cells, as shown on the left side of Fig. 5 [10]. Careful design of these unit cells ensures that the performance is not deteriorated by the switches. Cells which are deactivated are powered down completely. To keep the control manageable, a binary weighted structure is employed. Such a binary cell consists of equally designed unit cells for better matching purposes. They will be uniformly spread at layout to limit the impact of process variations. Hence, optimal performance and high flexibility is achievable at low power consumption as the circuit always operates in optimal bias conditions.

B. OTA-RC Integrator

To achieve adequate linearity, the first integrator is implemented as an OTA-RC integrator. Single-stage solutions are more power efficient when high speed is required. Therefore,

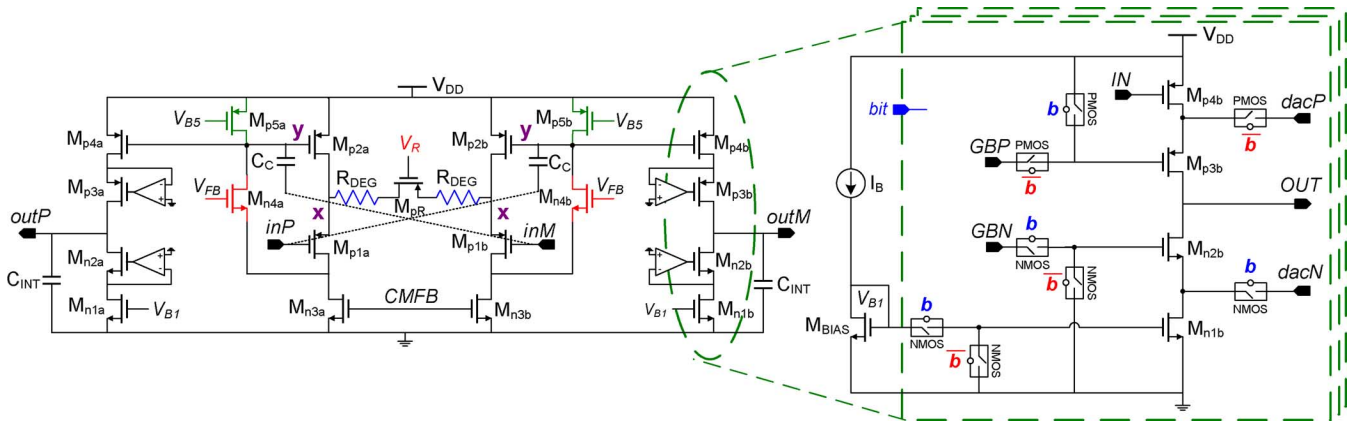

Fig. 6. Flexible G_m-C integrator with linearized transconductor and reconfigurable output stage consisting of switchable unit cells. Switching on/off corresponds to changing the mirror factor without affecting the linearity set by the input stage.

a gain-boosted folded cascode, as illustrated on the transistor schematic part of Fig. 5, is chosen as it offers both high DC gain (70 dB) and good output swing. This gain-boosting circuit is a simple common-source amplifier. This single-stage topology results in a high GBW/P ratio, obviously dependent on the load capacitance.

The absolute values of R and C are fixed based on dynamic range of the integrator. The noise specification fixes the resistor value, and the integration capacitor C is then configured employing a capacitor bank such that the RC time-constant matches the integrator coefficient a_1 covering all frequencies and scale factors. To minimize distortion, a good virtual ground is crucial and therefore the DC gain and GBW should be sufficiently high. Because in a folded cascode, the current consumption is proportional to this GBW via (2), it is the most important parameter of the flexible OTA as it enables energy scalability proportional to the performance. Clearly, a relaxed noise specification results in a larger R and smaller C and therefore the same GBW can be achieved for less current. The parameters are derived based on system level modeling as follows:

$$a_1 \cdot f_s = \frac{1}{R_1 C_1} \quad \text{with} \quad a_1 = a_{1,\text{ref}} \cdot \frac{k_1}{k_2} = 0.3 \cdot \frac{k_1}{k_2} \tag{1}$$

$$G_m = 2\pi \cdot \text{GBW} \cdot (C_1 + C_{\text{PAR}}). \tag{2}$$

The OTA circuit configuration with the highest GBW is split up into 15 smaller switchable unit cells. Each unit cell consists of a scaled gain boosted folded cascode. A 4 bit binary control word selects the number of active cells. Consequently, the bias point remains fixed and optimal and the current consumption scales proportionally to the number of active cells. The parasitic output capacitance important for GBW is mainly determined by the input capacitance of the next stage and equals the sum of the input capacitances of all unit cells. Their value is only slightly different for activated and deactivated cells and can be considered constant allowing an accurate control of the GBW. The common mode circuit is shared and remains fixed. Splitting up the CMFB into unit cells would only have a limited impact as its power consumption is already small compared to the core circuit ($I = 168\ \mu$A). The unit cell's transconductance equals 0.5 mS and the current consumption is 150 μA of which 25 μA is consumed by the gain boosting circuits. With a 4 bit control word, a G_m range from 0.5 mS up to 7.5 mS is obtained which covers the required range defined by behavioral simulations.

The flexibility concept is illustrated, again in Fig. 5. The right hand side shows the switchable folded cascode unit cell. No switches are present in the signal path minimizing their impact on the performance. If not, the on-resistance of the switch would cause a voltage drop or a parasitic pole could be introduced if placed before e.g. the gate of the input pair. The unit cell is disabled by turning off the cascode branches; their gate is grounded (M_{n2}) or pulled up to V_{DD} (M_{p3}). This also isolates the output node when deactivated. Furthermore, the current from the input stage is blocked by turning off the current source. To avoid a leakage path, also the big current source M_{n1} is deactivated. This is implemented via a T-switch to isolate the biasing node. The proposed implementation has the advantage that the CMFB loop is never interrupted ensuring stability. Clearly, when deactivated, the unit cell consumes zero current and when it is active, the system sees the same OTA as in a dedicated design working at the same operating point.

C. G_m-C Integrators

The second and third integrator are implemented as G_m-C integrators for high speed. Their dynamic range specifications are an order of magnitude less stringent than the first integrator. The more linear these integrators are, the higher the allowed signal swing and the more efficient (noise) the modulator becomes. In an open loop structure, the main nonlinearity contributor is the input transconductor. By combining resistive source degeneration and local feedback around this input pair, the linearity of the OTA is enhanced (left side of Fig. 6). This feedback forces a linear copy of the input voltage to the source of M_{p1}. This linear voltage appears over the source degeneration resistance R_{DEG} causing a circular current i_c to flow. A small linear MOS is added in series with R_{DEG} for fine tuning controlled by V_R. The linear current is then mirrored into a high gain output stage similar to the output stage of the gain boosted folded cascode. The input stage is biased so that the current is equally divided between input branch and local feedback branch. The explained feedback operation improves if the current source M_{p5} is as

ideal as possible. Hence, this transistor needs to be in saturation in all circumstances. To create more room, a high V_T transistor is chosen for M_{p2}. In this case, an IIP3 of about 20 dBVp can be achieved until the swing has become too high and the current sources M_{p2} go out of saturation. Finally, a compensation capacitor C_C is placed to guarantee high frequency stability.

In this open loop topology, the integrator coefficient directly depends on the effective transconductance and capacitance ratio of the G_m-C integrator. Making the input stage flexible (thus by adding switches) could degrade the linearity. Reconfiguring the core OTA is actually not required because it is more straightforward to modify the scaling factors k_i instead. When the linearity specification is reduced, the signal swing can be increased. This higher signal swing relaxes the thermal noise specification and therefore lowers the required effective transconductance which in turn reduces the power consumption. By adjusting the mirror factor, the effective transconductance changes and hence the integrator coefficient becomes adjustable without changing the input stage. The parameters are derived as follows:

$$a_2 \cdot f_s = \frac{G_{m,\mathrm{eff}}}{C_2} \approx \frac{B}{R_{\mathrm{DEG}} C_2} \quad \text{with} \tag{3}$$

$$a_2 = a_{2,\mathrm{ref}} \cdot \frac{k_2}{k_3} = 0.3 \cdot \frac{k_2}{k_3}. \tag{4}$$

The global architecture of the flexible G_m-C integrator consists of a tunable OTA and a capacitor bank. The input stage is hence kept fixed while flexibility is introduced in the output stage by modulating the mirror factor (Fig. 6). This output stage is again implemented in switchable unit cells consisting of a scaled version of the original output stage. A 4 bit binary control word configures 15 identical unit cells. The total G_m range starts at 61 μS and goes up to 915 μS covering all standards. A smaller unit cell is useless as the current consumption is now only 56 μA. The total current consumption scales linearly with the number of active cells. In this implementation, the gain boosting circuit is shared ($I = 110$ μA). If it would be part of the unit cell, both current and transistor sizes would be unrealistically small. Because it cannot be scaled down in the same way, the current budget of the 15 gain boosting circuits would be a considerable part of the total current consumption. The CMFB circuit is also shared such that this loop is not interrupted and consumes 224 μA. The third integrator is built exactly the same way but is scaled with a factor 4 as allowed by the relaxed specifications. As flexible output stage, the same unit cell is used. Consequently, only a 2 bit control word is required.

Zooming in to the right hand side of Fig. 6, the switchable output stage unit cell used in both integrators 2 and 3 is depicted. Again, the cell is deactivated by turning off the cascodes and current sources. However, switching becomes more complex. Turning off the cascodes also requires a T-switch because the gate of the cascode is connected with the shared gain boosting circuit which can never be switched off. As explained in the next section, the current from the NRZ DACs is injected at the source of the cascode transistors M_{n2} and M_{p3}. This feedback current is only allowed to flow into the active cells. Therefore switches need to be added isolating these nodes. Its resistivity should be as low as possible to limit the voltage drop.

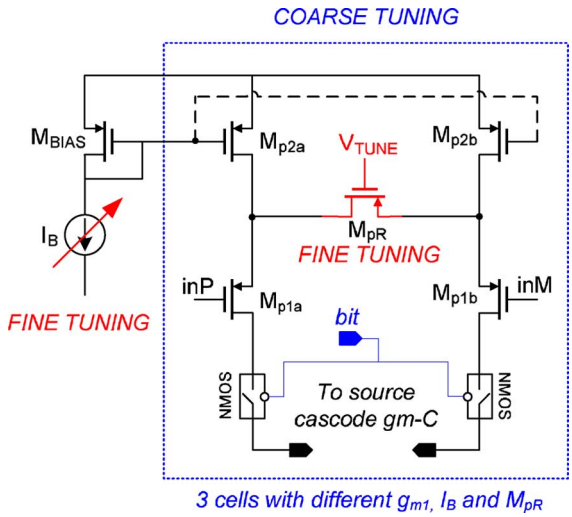

Fig. 7. Transconductor (input stage) implementing the local resonator branch b. Its output stage is shared with the one of the second integrator. The output current is injected on the same node as the feedback DAC and is labeled on Fig. 6 as dacN. Coarse (three branches) and fine tuning (resistor control) are combined to cover the large transconductance range.

D. Local Resonator Branch

Due to the large bandwidth variation, there exists a large required range in transconductance of the local resonator branch. Its output current is injected at the same node as the feedback DAC current sharing the output stage of the second integrator (Section III-F). The values are dependent on the local resonator feedback coefficient b and the effective transconductance of the second integrator.

$$G_{m,\mathrm{lcfb}} = b \cdot G_{m2} = \frac{(2\pi \cdot \mathrm{BW} \cdot 0.75)^2}{a_2 \cdot f_s \cdot a_3 \cdot f_s} \cdot G_{m2}. \tag{5}$$

The large range is efficiently covered by combining coarse and fine tuning (Fig. 7). To implement the coarse tuning, the transconductance range (1.2 up to 30 μS) is split into three subranges (combinations are possible). Three switchable differential pairs with source degeneration are designed. Each of them has a different bias current, input transconductance and degeneration resistance implemented as a MOS in triode regime. Switching a branch is done using a series switch placed at the output node of each branch. This approach has the advantage over turning off the current source that it isolates the different branches which is important because of the low transconductance values. Only the parasitics of the small switch are then seen at the output. To adjust the position of the notch in one subrange, the gate voltage ($V_{\mathrm{TUNE}} = 0$–450 mV) of the M_{pr} is controlled. The current consumption is limited to 20 μA.

E. SC-DAC

To limit the impact of jitter, an accurate clock generator is required, careful design of the clock distribution network is crucial and less sensitive feedback pulses (e.g., exponentially decaying) have to be used. Therefore, the first DAC has a SC-implementation (Fig. 8). During the first half period when the comparator is sampling, the capacitor is charged and during the second half, the charge is injected on the virtual ground of the OTA-RC integrator making it less sensitive to the initial peak

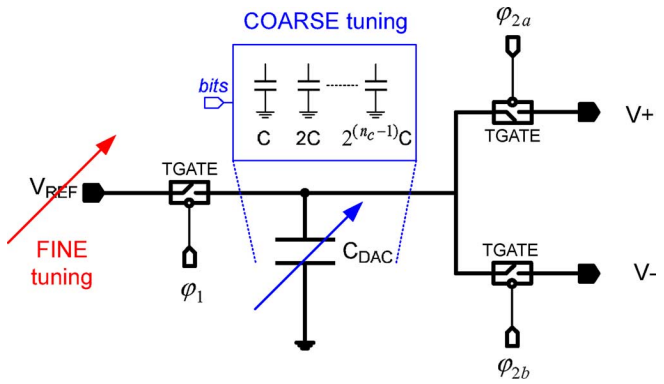

Fig. 8. SC-DAC combining coarse (C) and fine tuning (V_{REF}). Extra switches can be avoided if the control signals are multiplexed.

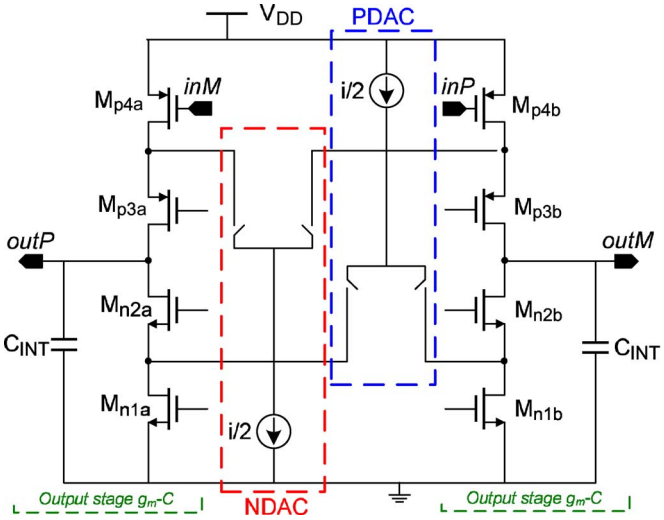

Fig. 9. Low sensitive integration between NRZ SI-DAC and G_m-C integrator (output stage is shown): The current is fed back into a low impedance node.

current. No additional loop delay has been inserted. A tradeoff between capacitance value and the reference voltage together with accurate switch design has been performed. Together they define the feedback charge ($C_{\mathrm{DAC}} \cdot V_{\mathrm{REFc}}$), the peak current ($V_{\mathrm{REFc}}/R_{\mathrm{ON}}$) and the slope ($R_{\mathrm{ON}} \cdot C_{\mathrm{DAC}}$) of the pulse. The switch has been implemented as a transmission gate to lower its on resistance and enhance its linearity. The control of the switches is done by a clock phase generator delivering strictly nonoverlapping pulses.

To cover the large range of feedback charge (85–320 fC), again coarse and fine tuning are combined. The coarse digitally controlled tuning divides this range by means of a capacitor bank. The fine tuning is performed with the reference voltage and allows a continuous tuning within the subrange set by the capacitor bank ($C_{\mathrm{min}} = 290$ fF and $C_{\mathrm{max}} = 1.05$ pF at $V_{\mathrm{REFc}} = 0.3$ V) (Fig. 8). However, extra switches on top of the capacitor unit cells (like in traditional capacitor banks) are preferably avoided as it increases the total on resistance and adds extra parasitics modifying the pulse shape at the sensitive input node. The extra switches can be avoided if the original switches defining the non-overlapping charge and discharge phase are duplicated. By means of a simple multiplexer (MUX), these phases can be passed through to the DAC or can be set to zero.

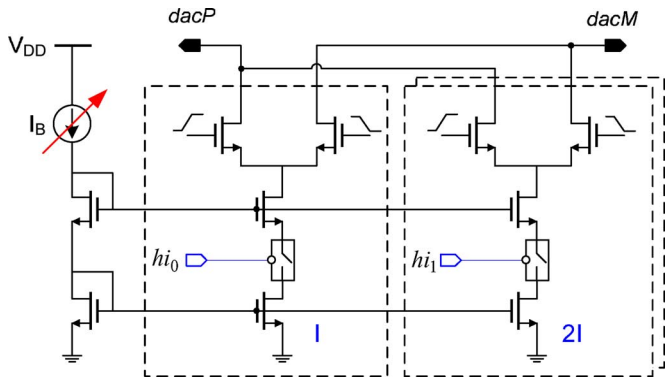

Fig. 10. SI-DAC combining coarse tuning (digitally controlled unit cells) and fine tuning (I_B).

F. SI-DAC

The second and third DAC are current switched cascoded NRZ DACs. A uniform pulse shape is preferred as no virtual ground is present. NRZ pulses are preferred because of their higher duty cycle compared to RZ making them less susceptible to jitter and keeping the amplitude of the pulse limited. The cascode ensures high output impedance and shields the drain node of the current source from the non-constant output node. Additionally, the high parasitic capacitance of the large current source is shielded and clock feedthrough is minimized. Timing of the switches ensures that the current source is always active avoiding transients. The current is fed back into a low impedance node (source cascode) of the G_m-C integrators to avoid output loading and signal dependent feedback pulses due to the large output swing. The DAC is implemented complementary (PDAC and NDAC) (Fig. 9). This implementation offers a very large headroom guaranteeing a robust DAC design.

Because the modulator should cope with a wide range of standards, all values in that continuous range must be easily obtainable. A large range (factor 3) together with a small step size (5 μA) would complicate the implementation of the DAC when this DAC only consists of switchable unit cells. Therefore, a combination of coarse and fine tuning is proposed. The coarse tuning has been implemented with switchable digital controlled unit cells while the fine tuning has been implemented in an analog and continuous manner by adjusting the biasing current.

The NRZ current feedback DAC is shown in Fig. 10. It consists of a 2 bit binary weighted structure where the control bits select the I or $2I$ branch (or both). For the second DAC, tunable current branches of $I = 50$ μA and $2I = 100$ μA are available. This is scaled down to $I = 15$ μA and $2I = 30$ μA for the third DAC. Each current can be tuned by 20%. For the digital tuning, an extra switch is placed between current source and cascode. Finally, the large headroom allows an easy biasing for the cascode stage without additional bias branches. Decoupling capacitors have been added to the bias nodes.

G. Threshold Configurable Comparator

1) Regenerative Dynamic Comparator Core: A dynamic latch-type comparator similar to [24] has been employed

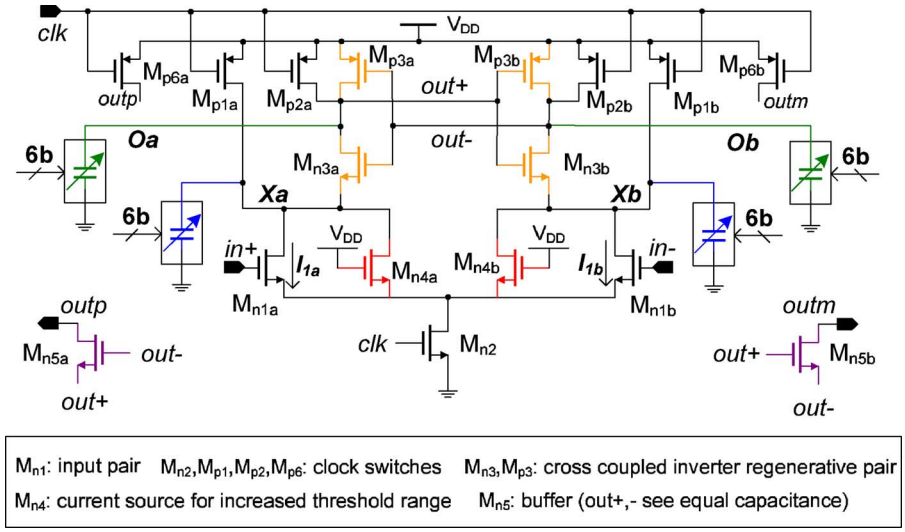

Fig. 11. Threshold configurable dynamic comparator core for loop delay control implemented with switched capacitor banks to create an imbalance between the internal nodes.

(Fig. 11) avoiding all static power consumption. Typically, such implementation suffers from offset caused by mismatch especially when no pre-amplifier is present. Because this design requires only a single-bit quantizer (maximum spread of reference levels) and because the comparator is positioned at the least sensitive point of the $\Delta\Sigma$ (offset will be suppressed by the loop gain), no degradation is expected for limited offset levels. Nevertheless, offset calibration can be performed with tuning capacitance on the internal capacitance nodes [24]. The comparator core has been extended with transistors M_{n5} between the output of the regenerative pair and the real output of the core $outp$ and $outm$ (Fig. 11). They act as a buffer and shield the (state dependent) input capacitance of the latch. The output of the core only changes when the comparator has taken a decision. Thanks to the large comparator gain, realized by minimizing the time constant of the regenerative pair (sufficient G_m, small C), metastability is sufficiently low to have no impact on the SNDR. Because of the cascade of latch, buffers and flip-flop following the comparator (Fig. 4), this probability is even further minimized. For an input of 0.5 mV, the delay is limited to 300 ps $(= T_s/4)$ illustrating the large margin. The overall average power consumption is about 85 μW at sampling speed of 640 MHz.

2) Threshold Reconfiguration: A threshold different from zero can be obtained by modifying the decision point of the comparator. An intentional imbalance is obtained by creating a different capacitive load at the drain node of the input pair (X-node) (Fig. 11). PMOS transistor capacitance offers an easy control through the gate node and a high density implementation [24], [25]. A configurable threshold range of 200 mV is required corresponding to $a_4 = 0.2$. The range and step size determine the design of the capacitor bank. A 6 bit binary weighted capacitor bank is employed at both sides (Xa and Xb). However, a proportional increase of the maximum threshold by adding more bits is not feasible as a saturation effect on the V_{TH}–ΔC curve occurs.

To enlarge the calibration range, small current sources M_{n4} are added (Fig. 11). Its current leads to a larger threshold variation with the same capacitor bank as it modifies the slew rate during the evaluation phase. The threshold range increases by a factor 3 and the linear range extends. The increased input referred offset (3σ rises from 46 to 87 mV) and the input sensitivity are not critical. Offset can be calibrated by a similar capacitor bank at the O node and sufficient settling time is available even for very small inputs.

IV. Integration, Timing, and Clock Circuitry

Generating an accurate clock is crucial for the performance of high speed CT$\Delta\Sigma$ ADCs. Clearly, when designing clock circuitry, the relative timing and position needs to be correct taking into account several delays introduced by settling times and long propagation of signals. Layout floor planning and buffers required to drive those long lines have to be taken into account.

The quality of the clock is of key importance for the SC-DAC (a few ps rms jitter). Therefore, the amount of circuitry which can introduce jitter is minimized. The reclocking flip-flop is placed close to the SC-DAC and the master clock. This clock is directly fed into the phase generator. One of its phases is then used to control this reclocking (sensitive) flip-flop. Because this flip-flop is positioned very close, the propagation delay is minimal and the edges are steep as no long wires with high distributed capacitance need to be driven. Fig. 12 illustrates the two parts of the clock circuit: a first part close to the SC-DAC and a second part near the quantizer.

An extra advantage of placing the reclocking flip-flop close to the SC-DAC is that the propagation delay from the output of the quantizer does not add to the loop delay because the reclocking happens at the end of the line. This is feasible thanks to the fast regeneration time of the 90 nm comparator. An extra buffer is added at the output latch of the comparator able to drive the long wire. The driving strength is not crucial as the signal

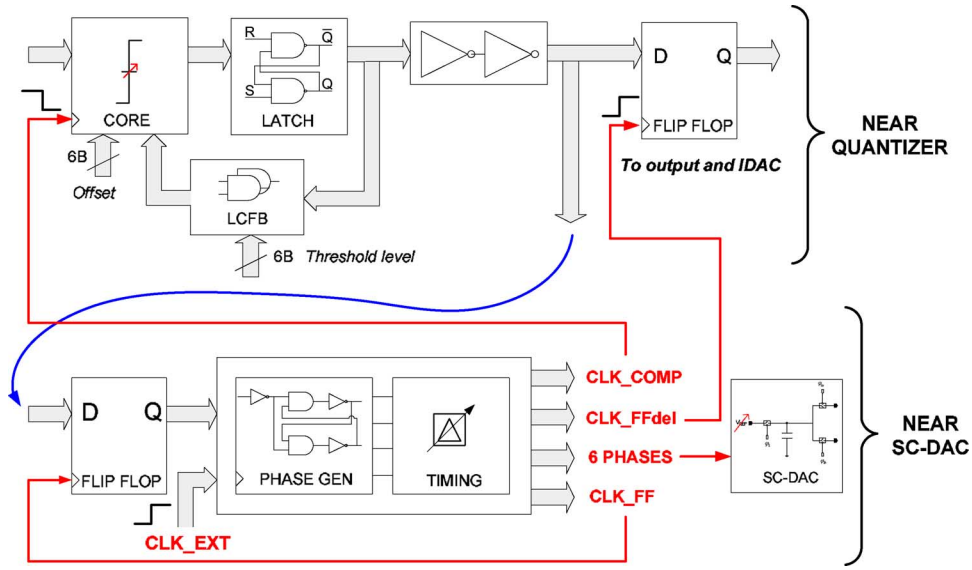

Fig. 12. Timing diagram and clock circuitry illustrating its location in the modulator. The reference reclocking flip-flop (bottom-left) is located as close as possible to the master clock and the SC-DAC.

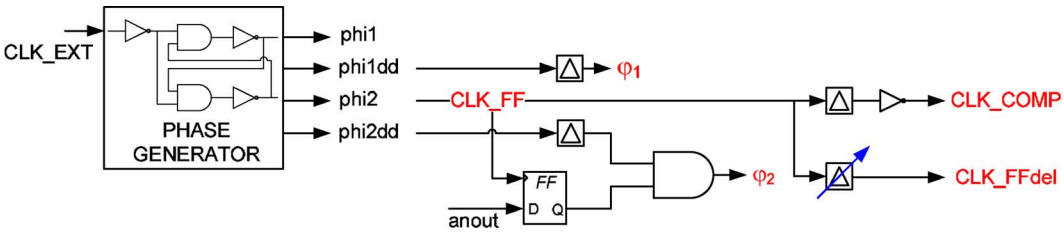

Fig. 13. Detailed view of the timing block generating all clock signals. One of the phases is used as reference for the reclocking flip-flop (CLK_FF). Other clocks are derived from it. The charging phase (φ_2) depends on the decision of the quantizer $(anout)$.

is reclocked anyway. Remember that reclocking the DAC control signals exactly half a period later than the sampling clock, fixes the loop delay and allows an easy compensation. The direct feedback path compensating the delay consists of only an addition and hence half a period is available to reconfigure the capacitor banks in the quantizer making the timing straightforward.

The output decision of the quantizer is not only needed to control the SC-DAC, it also drives the SI-DACs and the output of the modulator. Therefore the reclocking flip-flop is repeated near the quantizer. The timing of this flip-flop is little delayed compared to the flip-flop near the SC-DAC. This controllable delay is needed to define the relative timing between SC and SI-DAC. It compensates the delay introduced by the extra circuitry generating all phases. A detailed view of the timing circuit near the SC-DAC is given in Fig. 13. Finally, the sensitive digital circuits near the SC-DAC have a separate supply and ground rail. Together with sufficient decoupling, an accurate clock signal is realized.

V. Measurements Results

A. Prototype Measurements

A prototype chip has been fabricated in digital 90 nm CMOS process with a 1.2 V supply (Fig. 14). The core area occupies 0.4 mm^2. Based on the derived specifications and used topologies, all building block parameters (R, C, g_m) and bias settings

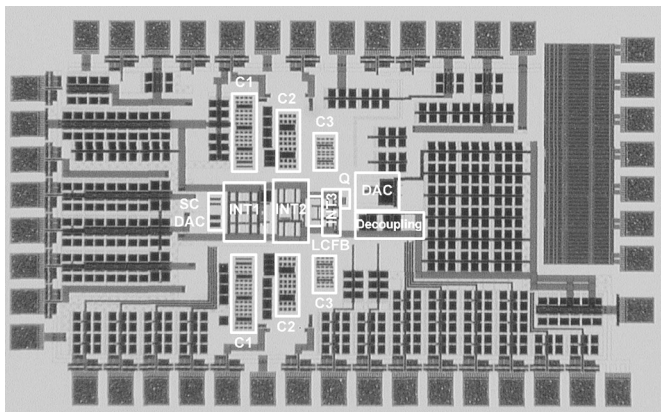

Fig. 14. Die micrograph. The core area occupies $0.58 \times 0.69 = 0.4$ mm^2.

are uniquely defined by solving a system of equations. Reconfiguring the modulator becomes then very straightforward by shifting in new control bits and can hence be automated. Only few fine tuning control knobs such as the current of the feedback DAC need to be done manually.

Fig. 15 shows the measured spectra for different modes at SNDRp. The spectrum also reveals the SFDR. Table II summarizes the performance. Multimode operation is easily verified and state-of-the-art energy efficiency is achieved. For all modes,

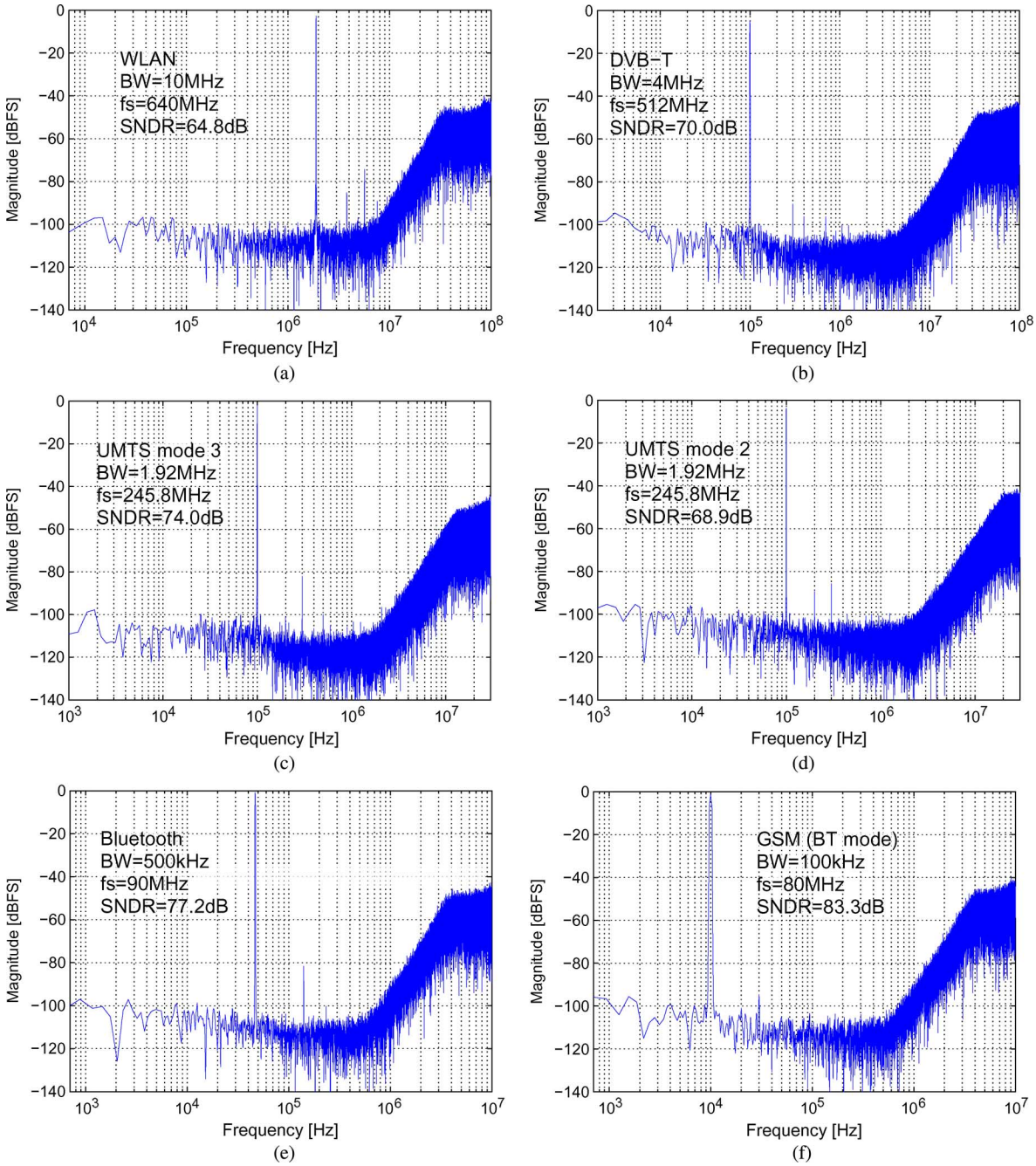

Fig. 15. Measured spectra for different standards and performance modes proving multimode operation. (a) WLAN with scale factors $k_i = 122$; (b) DVB with scale factors $k_i = 122$; (c) UMTS with scale factors $k_i = 133$; (d) UMTS with scale factors $k_i = 122$; (e) BT with scale factors $k_i = 122$; (f) GSM with scale factors $k_i = 122$.

this energy efficiency (FOM) is well below 1 pJ per conversion step (Table II).

For UMTS, the spectrum is measured in a high resolution–moderate power mode (SNDRp = 74 dB for 6.44 mW) and in a moderate resolution–low power mode (SNDRp = 69 dB for 4.34 mW). The former uses a larger scale factor k_i (3 instead of 2) to reduce the signal swing at the input of the G_m-C integrator. Clearly, power can be saved when less resolution is required. This UMTS example illustrates how the flexibility is exploited to obtain the minimum possible power consumption for a desired resolution for a given architecture choice. Measurements of power scaling are limited to only one standard as we preferred to stress the flexibility over a large range of standards. Therefore, the best achieved results (lowest FOM) per standard were reported in order to compare the performance to other works.

In Fig. 16, the SNDR is plotted vs. the input amplitude for different modes to extract the dynamic range. Two definitions exist for the upper bound: the input amplitude where the modulator turns unstable and the full scale input amplitude (0 dBFS). The first one is referred to as DRout and the second as DRin. The respective DRout and DRin are reported in Table II.

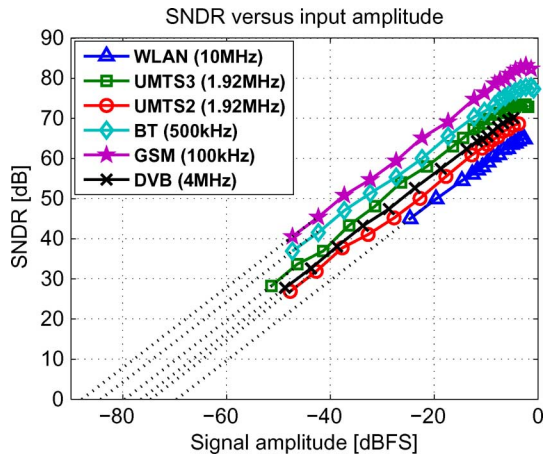

Fig. 16. Dynamic range: SNDR versus input amplitude.

TABLE II
PERFORMANCE SUMMARY

CTΔΣ	BT	UMTS2	UMTS3	DVB	WLAN
BW	500k	1.92M	1.92M	4M	10M
f_s	90M	245.8M	245.8M	512M	640M
DRout	83.4dB	70.9dB	77.7dB	71.7dB	67.0dB
DRin	84.2dB	74.6dB	79.6dB	76.4dB	69.6dB
SNDRp	77dB	69dB	74dB	70dB	65dB
SFDR	81dB	82dB	80dB	86dB	72dB
IM3		>75dB			70dB
Dif. inp. range	$1.6V_{pp}$	$1.7V_{pp}$	$2.1V_{pp}$	$1.9V_{pp}$	$1.9V_{pp}$
P_{DC} $(1.2V_{DD})$	5mW	4.34mW	6.44mW	5.5mW	6.8mW
FOM (pJ/conv)	0.85	0.5	0.41	0.27	0.24

For low bandwidth modes, the feedback architecture together with the choice of first integrator limits the power efficiency due the large load capacitor as expected from simulation. However, GSM operation is still achieved but with a non-scaled power consumption. In 500 kHz mode, GSM operation is obtained providing a DRin of 87 dB (BW = 100 kHz) consuming 5 mW of power.

Finally, Fig. 17 shows an intermodulation measurement for both UMTS2 and UMTS3 at peak SNDR (tones at −9.7 dBFS and −7.9 dBFS, respectively). The measured IM3 is indeed better for UMTS3 where the internal signal swing has been reduced. For other modes, an IM3 around 75 dB has been achieved except for WLAN where IM3 = 70 dB. From the spectra, it can be concluded that the resolution is limited not by distortion but by the noise floor caused by clock jitter.

B. Comparison With State-of-the-Art

The performance of the modulator is summarized by calculating the figure of merit (FOM).

$$\text{FOM} = \frac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{\text{ENOB}}} \quad \text{with} \tag{6}$$

$$\text{ENOB} = \frac{\text{SNDRp} - 1.76}{6.02}. \tag{7}$$

This FOM is used to compare this work to recently published CTΔΣ in the solid-state society. A full overview with extracted data and references is given in Table III. A graphical representation (Fig. 18) illustrates the wide tuning range and high energy efficiency. This design proves to be extremely efficient for large bandwidth standards realized with a single-bit design applying the described architectural and circuit techniques.

TABLE III
STATE-OF-THE-ART COMPARISON RANKED AS IN FIG. 18

Ref.	Bandwidth (MHz)	SNDR (dB)	Power (mW)	FoM (pJ/conv)
[17, Park]	20	78	87	0.34
[26, Huan]	2	79	4.52	0.16
[18, Dhan]	20	60	10.5	0.32
[27, Veld8]	0.2	77	1	0.43
[11, Yang]	10	82	100	0.49
[28, Shu]	8	70	50	1.21
[12, Bree]	20	69	28	0.30
[7, Ouzo]	0.2	82	1.44	0.35
	1	75	3.4	0.37
	2	71	4	0.35
	10	52	7	1.08
[13, Mitt]	20	74	20	0.12
[29, Kulc]	7.5	67	89	3.24
[30, Song]	2	63.4	2.7	0.56
[16, Stra]	10	72	40	0.61
[31, Li]	2.5	80.5	50	1.16
[5, Aria]	10	54	16	1.95
[32, Bakk]	0.6	74	6	1.22
[33, Cald]	20	49	103	11.1
[6, Vadi]	0.2	76	2.1	1.01
	2	60	7.2	2.20
[14, Redd]	15	64	20.7	0.53
[34, Ande]	2	62.4	12.5	2.90
[15, Pato]	15	64	70	1.80
[4, Veld3]	0.2	92	7.68	0.58
	0.6	83	4.1	0.30
	2	74	4.5	0.29
This work	0.5	77	5.0	0.85
	2	74	6.4	0.41
	4	70	5.5	0.27
	10	65	6.8	0.24

The trend in Fig. 18 reveals a drop in efficiency for lower bandwidths which can be explained by the choice of the feedback architecture (Section II). In this paper, flexibility was introduced at circuit level with the switchable unit cell approach, but the results also indicate that reconfigurability at the architectural level (e.g., hybrid loop filter) would also be needed to maintain the state-of-the-art FoM trend also at lower bandwidths.

VI. CONCLUSION

A multimode CTΔΣ ADC has been presented which is programmable in terms of bandwidth, resolution and power consumption. The lowest power for a desired performance is obtained by leveraging flexibility into the core of the analog circuits. The overall energy efficiency is achieved by an architectural and circuit level optimization of a single-bit modulator. Advantages of OTA-RC integrators and G_m-C integrators are combined, unnecessary additions are avoided, perfect loop delay compensation is realized thanks to a threshold configurable quantizer and feedback DACs are integrated at low sensitivity nodes. State-of-the-art performance (FOM = 0.24–0.85 pJ/conv) and high flexibility maintaining the optimal operating point is achieved making this design attractive for software-defined radio systems.

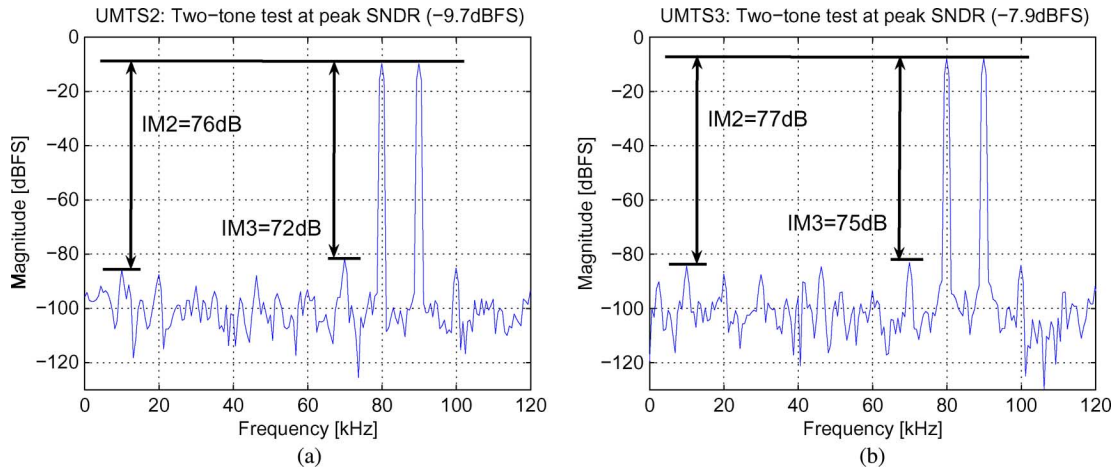

Fig. 17. IM3 and IM2 measurement for UMTS with different scale factors at peak input amplitude. UMTS3 mode has a better linearity (for even higher input power) thanks to rescaling and reconfiguring of the internal signal swing. (a) UMTS with scale factors $k_i = 122$; (b) UMTS with scale factors $k_i = 133$.

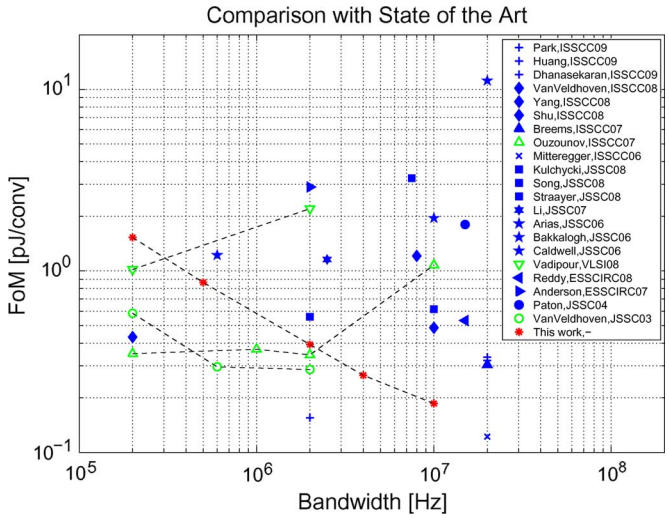

Fig. 18. Comparison with recent work in the solid-state circuit society. The markers are grouped per journal/year. Filled markers are dedicated designs while unfilled markers are multimode designs.

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