A 112–134-Gb/s PAM4 Receiver Using a 36-Way Dual-Comparator TI-SAR ADC in 7-nm FinFET

Pedro Wilson de Abreu Farias Neto, *Member, IEEE*, Kay Hearne, Ilias Chlis, Declan Carey, Ronan Casey, Ben Griffin, Frantz Stephane F. Ngankem Ngankem, James Hudner, Kevin Geary, Marc Erett, Asma Laraba, Haritha Eachempatti, *Member, IEEE*, Jae Wook Kim, Hongtao Zhang, *Member, IEEE*, Santiago Asuncion, and Yohan Frans, *Member, IEEE*

***Abstract*—This letter describes a 112–134-Gb/s PAM-4 wireline receiver (Rx) designed and fabricated in 7-nm CMOS FinFET technology. The Rx includes a T-Coil-assisted on-die termination (ODT), an adaptable continuous-time linear equalizer (ACTLE), a time-interleaved ADC (TI-ADC), clock generation, clock distribution, feed-forward equalizer (FFE), decision feedback equalizer (DFE), and calibration. The TI-ADC is implemented as a 56–67-GSa/s, 36-way arrangement of dual-comparator SAR ADCs (SAR subADCs). The Rx achieves BER better than 1e-4 for a data rate as high as 127 Gb/s, with 3.2e-4 BER at 134.4 Gb/s, over a 15-dB die-to-die loss channel and achieves 3e-6 BER over a 33-dB die-to-die channel loss at 28-GHz Nyquist while consuming 5.1 pJ/b of power, excluding DSP power.**

***Index Terms*—Calibration, CTLE, dual-comparator SAR, SAR ADC, SERDES, time-interleaved ADC (TI-ADC).**

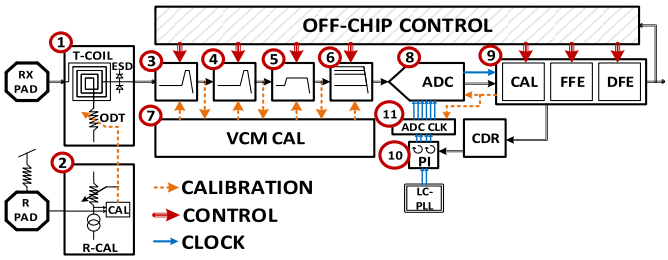

Fig. 1. Receiver simplified diagram: 1) Pad termination. 2) ODT calibration. 3) and 4) ACTLE high-frequency peaking. 5) ACTLE mid-frequency peaking. 6) Variable gain amplifier. 7) Common-mode voltage calibration. 8) TI-ADC. 9) DRP. 10) Phase interpolator. 11) Multipath clock generation and distribution.

I. Introduction

The state-of-the-art in high-speed wireline transceivers is converging toward PAM4 signaling standards [2] with ADC-based receivers, where the ADC is preceded by adaptable continuous-time linear equalization (ACTLE) and followed by digital recovery and processing (DRP) of clock and data [1].

The clear advantage of PAM4 is the encoding of two bits on each symbol, halving the required bandwidth for a given data rate. The main disadvantages are the reduced eye openings (≈ -9.5 dB), increased crest factor ($\approx +12$ dB), the more stringent linearity demands and the increase on the overall system design complexity (time-interleaved ADC (TI-ADC), multibit DFE, and FFE) [3].

Although some debate remains on the optimum ADC resolution targeting error free PAM4 signaling, for long (LR) and medium (MR) reach channels, most of the high-speed designs reported to date ($\geq$ 56GSa/s) fall in the range between 6 and 8 bits [3]–[5]. Due to the speed and power limitations on single path ADCs at 56 GSa/s (OIF CEI-112 compliant Rx [2]), TI-ADCs are a frequent choice, which requires precise (low skew and low jitter) multiphase clock sources to be generated and distributed through the design, with minimum power dissipation.

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Pedro Wilson de Abreu Farias Neto, Kay Hearne, Ilias Chlis, Declan Carey, Ronan Casey, Ben Griffin, Frantz Stephane F. Ngankem Ngankem, Kevin Geary, and Marc Erett are with the WWG Department, Xilinx Ireland, Cork, T45 YW71 Ireland (e-mail: pedrow@xilinx.com).

Asma Laraba, Jae Wook Kim, Hongtao Zhang, Santiago Asuncion, and Yohan Frans are with Xilinx, San Jose, CA 95124 USA.

James Hudner is with Kandou Bus SA, 1015 Lausanne, Switzerland.

Haritha Eachempatti is with Ayar Labs, Santa Clara, CA 95050 USA.

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The Nyquist frequency for the nominal 112 Gb/s Rx is 28 GHz, requiring bandwidth extension techniques (generally employing inductors and/or T-Coils) at the input termination network and in the ACTLE. The complexity of the multibit interface between the ADC and the DRP is addressed by digital techniques, such as pipelining and data partitioning, which reduce complexity while saving significant amounts of power.

In this letter, new techniques on the TI-ADC clock generation and distribution, as well as in the SAR ADC calibration are proposed and implemented for the first time in 7-nm FinFET CMOS technology. Section II introduces the Rx architecture, Section III is focused on the design of its continuous-time portion, Section IV presents the ADC, while Section V describes the clock generation and distribution. Section VI contains the experimental data obtained with the acknowledgment in the last section.

II. Receiver Architecture

The proposed Rx (Fig. 1) is protected by ESD diodes and contains a digitally controlled ODT, calibrated to 50 Ohm. An asymmetric T-coil is added to the design, ensuring wideband impedance matching and extended input bandwidth beyond 36 GHz. The adaptable continuous-time equalization is performed in four stages: two high-frequency peaking stages, aiming to equalize the precursor and the first few post-cursors ISI; one mid-frequency peaking stage, aiming for the equalization of the long tail response; and one variable gain amplifier (VGA) stage, the main function of which is to maximize the SNR at the ADC inputs while avoiding clipping. The ACTLE common mode voltage is also calibrated to improve linearity over PVT variations, with the full calibration circuit implemented on-chip.

The ADC was designed as a 36-way, time interleaved, dual comparator, SAR ADC, with 7-bit resolution and a sampling rate of 56GSa/s, using a two-rank track and hold multiplexing tree, similarly to [3]. A dedicated clock generation circuit converts the 14 GHz

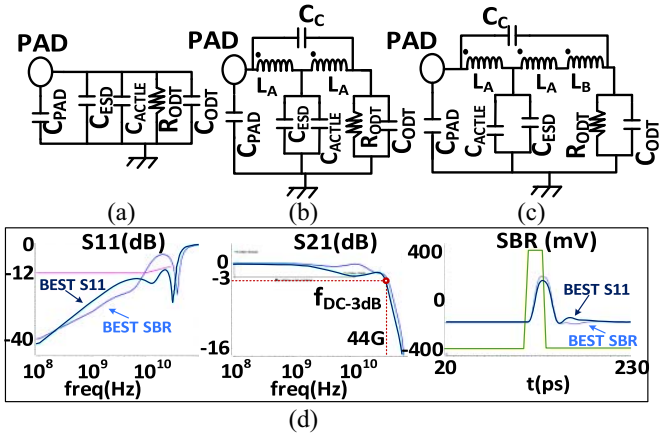

Fig. 2. Pad termination (a) without a T-coil, (b) with a symmetric T-coil, and (c) with an asymmetric T-coil. (d) Simulation for two asymmetric T-coil designs.

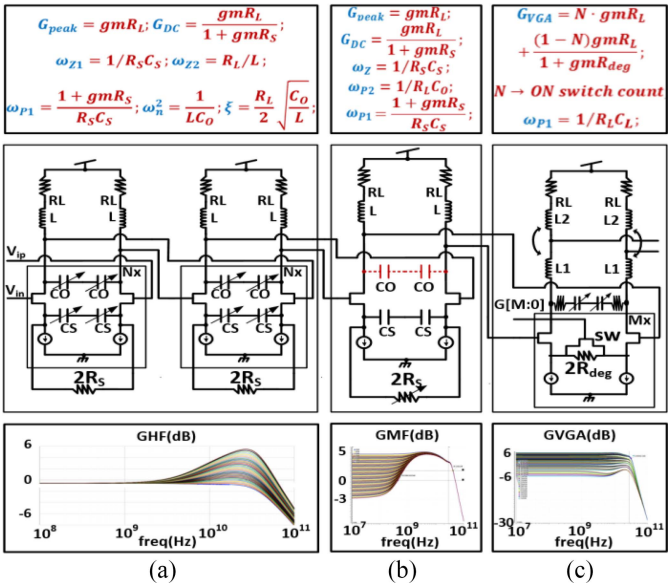

Fig. 3. ACTLE stages and frequency response.

(2-phase) clocks from the phase interpolator into the ADC time interleaved clocks: 6-phase, nonoverlapping, 9.333 GHz for rank1 and 36-phase, nonoverlapping, 11% duty-cycle clock for rank2. Delay calibration was introduced in the rank1 clock paths to minimize the ADC performance degradation due to clock skew. The rank1 skew calibration, as well as the 36-path gain and offset correction algorithms [10], are implemented off-chip, through an auxiliary FPGA controller. The digital data is directly corrected for gain and offset, while the calibration codes for skew and dual comparator offset alignment are fed back from the external control to the ADC and clock generation through the internal logic. The DRP handles the interface between the off-chip control and the Rx, implements a one tap 2-bit DFE with loop unrolling and a 31-tap pipelined FFE. It also generates the error data for the adaptation algorithm and for the baud rate CDR.

III. Pad Termination and ACTLE

To minimize return loss, a replica of the ODT is calibrated by a dedicated circuit, which uses an external resistor as reference and searches the digital code for the best fit to 50 Ohm (Fig. 1).

This strategy significantly improves the return loss performance at low speeds, but the input capacitance from the circuit components [Fig. 2(a)] will lower the input impedance at high speeds and harshly degrade the return loss performance.

By using a T-Coil [Fig. 2(b) and (c)], the ESD and ACTLE capacitors can be decoupled from the input impedance over a large frequency range. The input impedance could, in theory, be made constant over frequency by properly tuning a symmetric T-Coil [6] (this method ignores Pad and ODT capacitances). Unfortunately, once Pad and ODT capacitances are considered, the symmetric T-Coil design will not suffice to ensure good performance and an asymmetric T-Coil should be used to reduce the impact of the PAD/ODT capacitances on the return loss [Fig. 2(c)]. The T-Coil also extends the bandwidth as discussed in [7]. The simulated return loss (S11), insertion loss (S21), and single bit responses (SBR) for two tested T-Coils can be seen in Fig. 2(d). It is worth realizing the tradeoff between SBR and S11: although both coils achieve similar bandwidth, one presents better S11 results (dark blue waveforms) while the other presents better SBR performance (light blue waveforms), where the dark blue curves show the simulation results for the coil used in the final design.

The ACTLE is described in Fig. 3, where the relevant equations (valid in the frequency range of interest) are listed on top and the simulated waveforms at the bottom of the circuit diagrams. Note that for the first two stages [Fig. 3(a)], the peaking amplitude and frequency can be independently controlled by varying the values of CS and CO, while keeping the dc gain constant. Each stage achieves a maximum peaking of 6-dB around Nyquist, with constant 0-dB gain at dc and a near constant peaking frequency.

The mid-frequency equalizer is also implemented as a degenerated differential pair with a shunt peaking inductor added for bandwidth extension. The zero frequency and the peaking gain are controlled by varying the values of the degeneration resistor RS as discussed in [4].

The VGA stage [Fig. 3(c)] is also based on a degenerated differential pair, where the degeneration is purely resistive. The degenerated pair is segmented in 64-unit cells with a switch connected in parallel with each degeneration resistor. As a result, the current gain on each segment of the array can be varied between two distinct values, depending on the state of its switch, and the total gain will be the sum of the individual current gains multiplied by the load resistance. Due to the relatively large capacitive load present at the VGA outputs, a T-coil was added to this design, providing bandwidth extension [7] and better parasitic isolation. An *RC* filter is also added between the VGA differential pair drains to reduce the high-speed load impedance, countering the effect of the stray capacitors at the degeneration point (unwanted high-speed boost at low gain settings).

IV. ADC

The main challenges on the design of such a high-speed TI-SAR ADC are the required accuracy, speed, and linearity of sampling frontend (SFE), clock distribution, and SAR ADC (subADC) circuits. The subADC speed is improved by means of a dual comparator architecture, asynchronous operation, and careful conversion time margin budgeting, with the two comparator offsets aligned by a calibration loop to improve its linearity. The clock circuit utilizes injection-locked oscillators (ILOs) with quadrature error detection (QED) and skew correction to suppress deterministic jitter sources. The SFE relies on wideband bias-peaked source follower buffers (Fig. 4) [11], as well as layout symmetry to mitigate bandwidth mismatch between the interleaved paths.

The SFE diagram as well as the rank1 and rank2 clocks are shown in Fig. 4, where the SFE is described as two layers of voltage buffering followed by bootstrapped track and hold circuits. It is

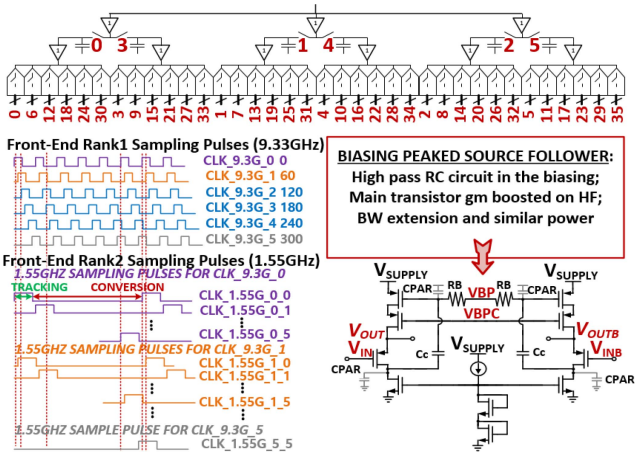

Fig. 4. SFE simplified diagram and clock waveforms.

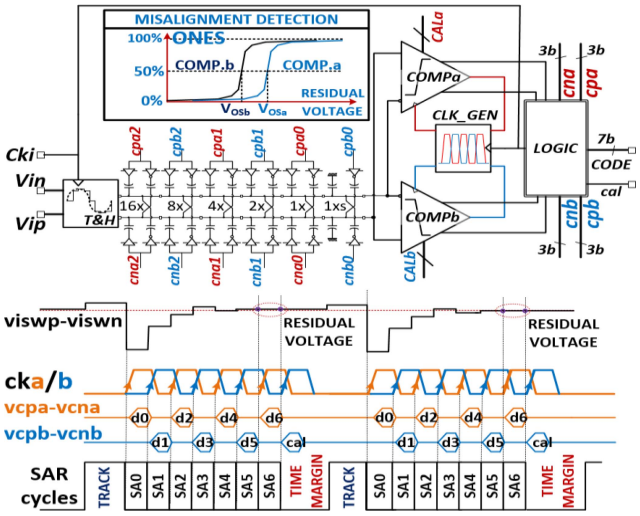

Fig. 5. subADC architecture and functional diagrams.

worth noting that the rank1 accuracy and linearity are of paramount importance for the overall ADC performance. The signal at the rank1 inputs varies during the tracking period and any skew between clocks or any bandwidth mismatch between input-to-switch paths will corrupt the output signal with a pattern that repeats itself at each six clock cycles. In contrast, the signals at the second layer inputs (rank2) are held constant during the tracking phase, relaxing the clock accuracy and bandwidth mismatch requirements significantly.

The subADC (Fig. 5) uses dynamic comparators in an asynchronous SAR loop with seven successive approximation cycles. The time margin is added for metastability error probability reduction and is budgeted for a last bit metastable error probability smaller than the last bit error probability due to noise. Two comparators are used to make the conversion time independent of the comparator reset period, in such a way that the conversion time is solely defined by the comparator, logic, and CDAC delays. The SAR logic is designed to offer, at the comparator's outputs, a variable load through the successive approximation cycles, optimizing the comparator's delay and power. The state machine is implemented by dynamic logic cells, precharged on each tracking phase.

The subADC will be impaired by significant nonlinearities (DNL) if the two comparator offsets are different from each other. The presented circuit detects the misalignment by comparing the "ones" probabilities after each comparator samples the subADC final residual error. Banks of capacitors are embedded on each comparator, allowing for digitally controlled offset voltage variation with a range around

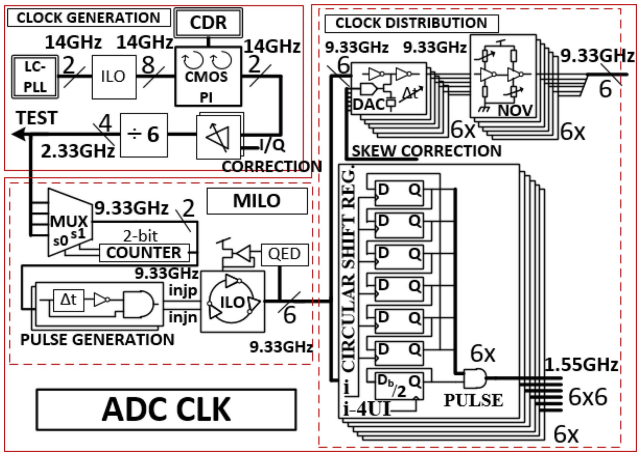

Fig. 6. Receiver clocking diagram.

12LSBs. The alignment loop is closed in the off-chip control system ensuring comparator offsets aligned on all subADCs.

V. Clock Generation and Distribution

The ADC rank1 and rank2 clocks are generated from the PLL clocks through a few stages of interpolation, division, multiplication, and distribution (Fig. 6).

In the first stage, the 14-GHz PLL clock is injected into a four-stage ILO. The ILO generates eight 14-GHz clocks with 45° difference between phases. The CMOS PI interpolates between these eight phases, accordingly with the code supplied by the CDR, delivering a 14-GHz two phase clock to the frequency divider. The frequency divider generates four 2.33-GHz (division by 6) clocks with 90° between phases. The next stage is a multiplying ILO, where the four clock phases from the previous stage will be multiplexed, generating two clock phases at four times the input frequency (9.33 GHz). The two resultant clock phases are shaped by a pulse generator and injected into a six-phase ILO. It is worth noting that even if the width of the pulse generated is poorly controlled over corners, the time stamps are precisely tracking the clock rising edges at the input of the MUX, preserving the clock frequency and phase relationships.

The ILO will generate six clock signals at 9.33 GHz (60° apart). The clocks are distributed to the rank1 switches through skew correction and nonoverlapping circuits. Each skew correction circuit is implemented as a variable delay chain, where the delay is controlled by an R-2R DAC, modulating the load resistance in an *RC* load placed between two inverters. The R-2R DAC-based architecture is chosen as it allows for tighter delay resolution if compared to starved inverter delay lines and less parasitics if compared to capacitive bank solutions, previously reported in the literature.

The rank2 clocks (stream of 4UI wide pulses at 1.55 GHz) are generated by inputting clock phases 4UI apart into a 6-bit circular shift register (CSR) and a divide-by-two circuit (DIV2). The resultant six phases from the CSR (6UI wide pulse stream at 1.55 GHz) are multiplied by the DIV2 clock through an AND gate, generating the 4UI rank2 pulses.

VI. Experimental Results

The circuit performance was tested by connecting a PAM4, PRBS-31 pattern generator to its inputs through ∼9 dB and 27 dB loss cables (Figs. 7 and 9), for total losses of about 15 dB and 33 dB from bump to bump, at 112 Gb/s. The comparator offset alignment capability was tested on all subADCs by keeping the comparator offset code constant at zero in one comparator (COMPa) while sweeping the offset correction code in the other comparator (COMPb). The plot in Fig. 8(a) shows the difference in the average results for both

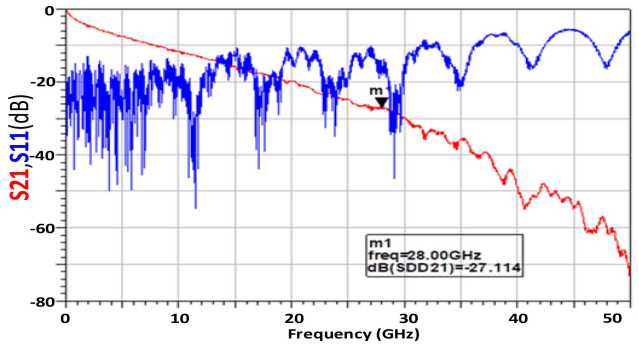

Fig. 7. Channel insertion and return loss plots (−27-dB loss cable).

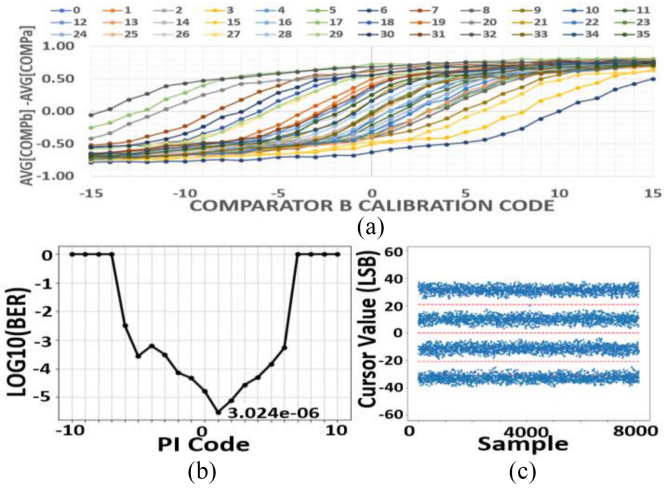

Fig. 8. (a) Difference of averaged last decisions for comparators A and B versus calibration code, across subADCs. (b) Bathtub plot. (c) Recovered data.

TABLE I
COMPARISON AGAINST PREVIOUS PUBLICATIONS

	THIS WORK	[11]	[4]
TECHNOLOGY	7nm FinFET	10nm FinFET	16nm FinFET
SUPPLIES (V)	0.88/1.2/1.5	0.95/1.5V	0.9/1.2/1.8
DATA RATE	112Gb/s	112Gb/s	112Gb/s
RX EQUALIZATION	CTLE, 1-TAP DFE 31-TAP FFE	CTLE, 1-TAP DFE 16-TAP FFE	CTLE, 1-TAP DFE 31-TAP FFE
AREA	0.383 mm2	0.281mm2	0.664mm2
POWER	5.1pJ/b	4.2pJ/b	5.27pJ/b
CHANNEL LOSS	33dB	35dB	20dB
BER (PRBS 31)	3e-6	1e-6	2e-5

comparators sampling the SAR residual voltage (residual misalignment). Each line represents one subADC and all lines cross the zero line (comparators aligned). The residual misalignment was kept below 10% in this design.

Fig. 8(b) shows the bathtub results obtained with the on-chip BER estimator. The plot in Fig. 8(c) shows the cloud of data samples versus sample index over several sampling batches. Fig. 9 shows the Tx output and Rx recovered eye diagrams at the nominal data rate (112 Gb/s), Fig. 10 shows the BER and eye diagram variation with data rate when the circuit's operation is pushed to its limits, while Table I presents the performance summary as well as the comparison against the state-of-the-art. At 112 Gb/s, the Rx achieves a BER of 3e-6, pre-FEC, for a power consumption of 5.1 pJ/b excluding the DSP power.

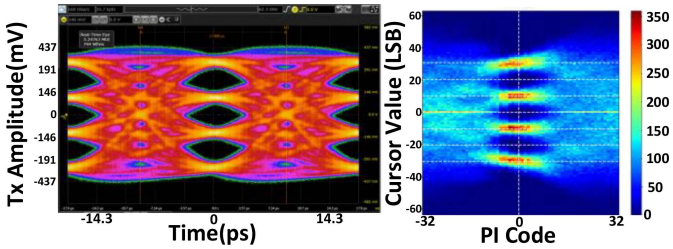

Fig. 9. Tx output and Rx recovered eye diagrams.

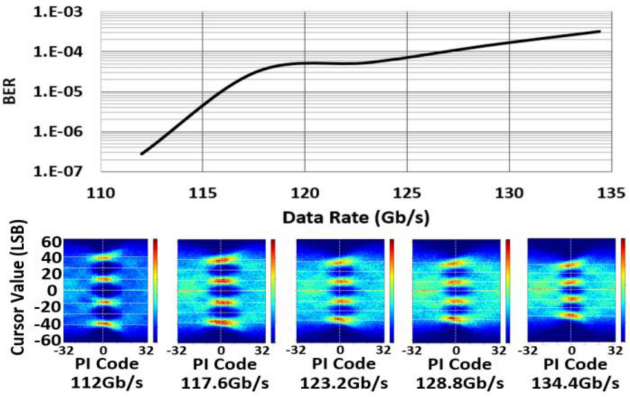

Fig. 10. BER and eye scan versus data rate for a 15-dB loss channel.

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