A 0.8 ps DNL Time-to-Digital Converter With 250 MHz Event Rate in 65 nm CMOS for Time-Mode-Based $\Sigma\Delta$ Modulator

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***Abstract*—A time-to-digital converter (TDC) is proposed to replace the multi-bit quantizer and the multi-bit feedback DAC of traditional voltage-mode $\Sigma\Delta$ modulator. Since time-mode systems process analog signals encoded in the time dimension rather than the voltage dimension, the proposed time-mode TDC makes the multi-bit $\Sigma\Delta$ ADC digital friendly and more suitable for nanometric technologies. A pulse-width-modulator (PWM) converts the sampled-and-held voltage-sample to a digital pulse whose width is proportional to the voltage level of the sample. Then, the TDC generates a digital code that corresponds to the pulse width. Simultaneously, the TDC provides a time-quantized feedback pulse for the $\Sigma\Delta$ modulator, emulating the voltage-DAC in a conventional $\Sigma\Delta$ ADC. Linearity, jitter and data-dependent-delay effects on the performance of the proposed architecture are analyzed. A chip prototype is fabricated in TI 65 nm digital CMOS process. THD of 67 dB is achieved which corresponds to a TDC's DNL of less than 0.8 ps without calibration. Measurements show that the $\Sigma\Delta$-modulator achieves a dynamic range of 68 dB and the TDC consumes 5.66 mW at 250 MHz event rate while occupying 0.006 mm^2.**

***Index Terms*—Time-to-digital, TDC, $\Sigma\Delta$ ADC, DAC, time-mode, mixed signal circuits.**

I. Introduction

RAPID scaling in technology has introduced new challenges in the realm of traditional analog design. Scaling of supply voltage directly impacts the available voltage-dynamic-range. On the other hand, nanometric technologies with cutoff frequency f_T in hundreds of GHz range opens opportunities for time-resolution-based signal processing, which was not a viable option in previous technology nodes [1]. With reduced available voltage-dynamic-range and improved timing resolution, it is convenient to devise analog solutions whose performance depends on timing precision rather than voltage levels. Thus, instead of representing the data/information in the voltage-mode, as a difference between two node voltages, it can be represented in time-mode as a time-difference between two rising and/or falling edges. Time-mode signal representation has been proposed in [2]. In [3]–[5], new low-THD-oscillator and ADC architectures were proposed to implement analog circuits whose design bottleneck is the timing precision of digital signals instead of voltage levels. A major advantage of processing signals encoded in the time-mode is the digital-friendly nature of the system, which scales down with the technology. In addition, migrating to smaller technologies is expected to improve the performance of the same time-mode-based design as timing resolution is improved.

In this paper a TDC that replaces the quantizer and the feedback DAC in a $\Sigma\Delta$ ADC is presented. The proposed technique transforms the performance bottleneck which is usually the accuracy of the multiple current sources and linearity of the multi-bit DAC in $\Sigma\Delta$ ADCs to the timing-precision of the TDC. The paper is organized as follows. Section II introduces the TDC-based ADC and the motive for using $\Sigma\Delta$ architecture instead of an open loop one. System level design is discussed in Section III. Sections IV and V discuss the TDC architecture and the transistor level implementation. Measurement results are given in Section VI along with a comparison with the state-of-the-art TDCs. Finally, concluding remarks are presented in Section VII.

II. TDC-Based ADC

The TDC is a block that provides a digital code corresponding to the width of the input pulse (which is the data in the time-mode circuits). The diagram in Fig. 1 shows how a sinusoidal input of peak-to-peak amplitude of $V_{\rm pp}$ centered at $V_{\rm FS}/2$, where $V_{\rm FS}$ is the full scale voltage, is digitized using time-mode circuits. The input signal is sampled-and-held at frequency f_s then a PWM block transforms the voltage-sample into a pulse-width which is digitized using the TDC. The transformation of the analog signal into the digital format is performed in the time-mode. The only part that is performed in voltage-mode is the pulse width modulation. In general, the same PWM design can be utilized as a front-end in time-mode systems to convert the signal from voltage-mode to time-mode prior to further processing.

Since the input signal is sampled at frequency f_s, the zero-voltage input is mapped to a pulse of width $T_s = 1/f_s$ while the full scale voltage input, $V_{\rm FS}$, is mapped to a pulse of zero width. Consequently, the conversion gain of the PWM is given by $-T_s/V_{\rm FS}$. Since the amplitude of the voltage-sample ranges from $V_{\rm FS}/2 * (1 - V_{\rm pp}/V_{\rm FS})$ to $V_{\rm FS}/2 * (1 + V_{\rm pp}/V_{\rm FS})$, the width of the output pulse will range from $T_s/2*(1 + V_{\rm pp}/V_{\rm FS})$

Manuscript received October 25, 2010; revised April 08, 2011; accepted April 13, 2011. Date of publication June 27, 2011; date of current version August 24, 2011. This paper was approved by Associate Editor Lucien Breems.

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Digital Object Identifier 10.1109/JSSC.2011.2156990

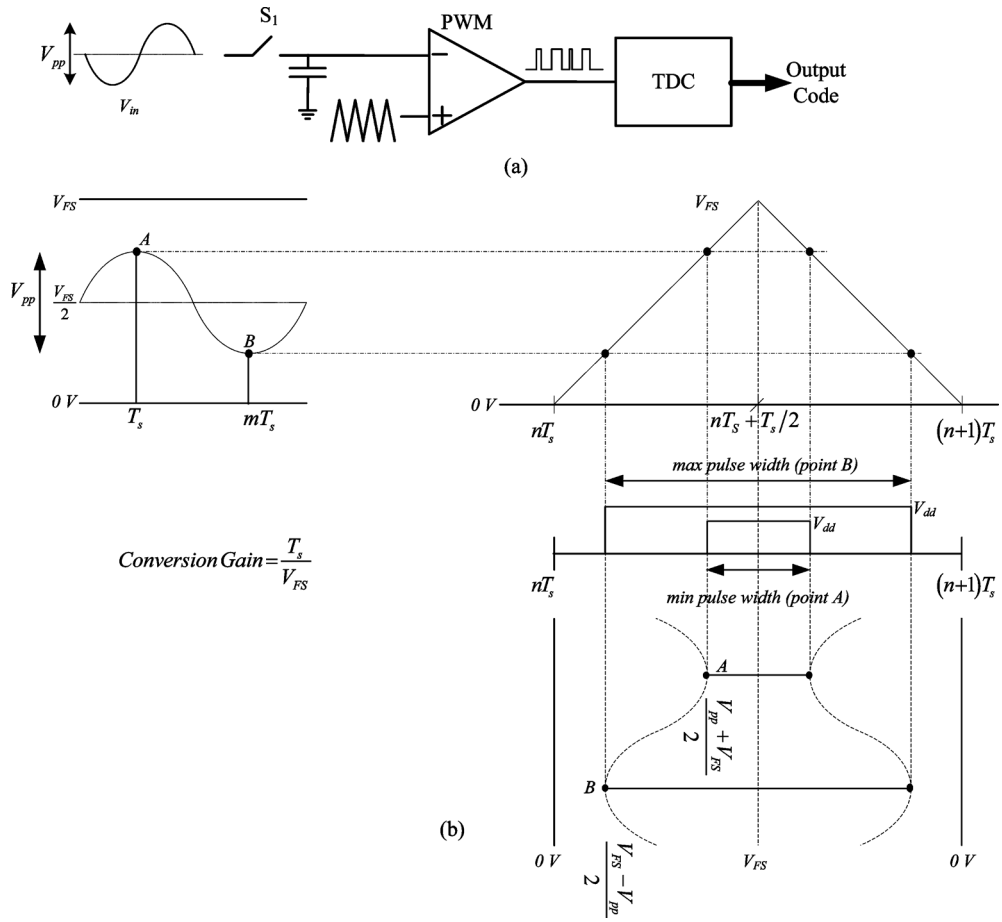

Fig. 1. (a) Open-loop time-mode-based ADC. (b) Timing illustration of the PWM.

to $T_s/2 * (1 - V_{\rm pp}/V_{\rm FS})$, i.e., centered around $T_s/2$, as illustrated in Fig. 1(b) at points "A" and "B". Since the output pulse is symmetric and centered around $T_s/2$, the change in the output pulse width corresponding to the change of the input can be modeled as if there were two virtual sinusoids around $T_s/2$, as shown in Fig. 1(b) and the pulse width is modulated with the amplitude of the pulse. Such model will be useful when analyzing the effect of transistor mismatchs on the TDC performance. The amplitude of the PWM output pulse is $V_{\rm dd}$ in all cases but on Fig. 1(b) it is different, at points "A" and "B", just for clarity purposes. The output pulse is then digitized using a TDC.

A major issue that hinders the full utilization of the aforementioned time-mode ADC architecture is the trade-off between the resolution of the TDC and both latency and dead-time [6]. Latency, or the conversion time, is defined as the time the TDC requires after the signal is tracked till the digital output is available. The dead time is the minimum time required between two acquisitions. Both latency and dead time limit the maximum sampling frequency that can be used and, as a consequence, put an upper limit on the bandwidth of the ADC. On the other hand, the resolution is the minimum time step the TDC can resolve. To achieve a high ADC dynamic range and a high signal-to-quantization-noise ratio (SQNR), a time-resolution of less than one gate delay may be required. This can be achieved using different techniques but will be at the expense of the latency and/or the dead time. For example, Vernier-line-based TDC uses two delay lines one of them employs minimum size inverters with time delay t_1 while the other line employs inverters of slightly larger delay t_2 [7]. Compared to the conventional delay-line-based TDC, the resolution is improved by a factor given by $t_1/(t_2 - t_1)$; however, the latency also increased by the same factor. In conclusion, the ADC bandwidth, which is limited by the latency, and SQNR, which is limited by the minimum time-resolution that the TDC can resolve, are compromised.

To resolve this trade-off, the concept of the ΣΔ modulator is adopted in time-mode designs [8], [9]. Fig. 2 shows the analogy between the voltage-mode ΣΔ modulator and its time-mode counterpart. The multi-bit quantizer and the multi-bit voltage-mode feedback DAC are replaced by a PWM and a modified TDC. The PWM transforms the input voltage-sample into a pulse and the TDC generates a multi-bit digital output, $D_{\rm out}$, that corresponds to the pulse-width and provides a time-quantized feedback pulse, $p_q(t)$, which emulates the DAC output in traditional ΣΔ modulators. Owing to the over-sampling and noise shaping offered by the ΣΔ loop structure, the quantizer (TDC) is not required to have a number of levels in the order of the targeted signal-to-noise ratio (SNR). On the other hand, the timing-accuracy of the feedback signal (the feedback pulse-width $p_q(t)$) should be in the order of the targeted SNR or better. For example, if we target a 10-bit voltage-mode ΣΔ modulator, we do not have to use a 10-bit quantizer. We can use, for

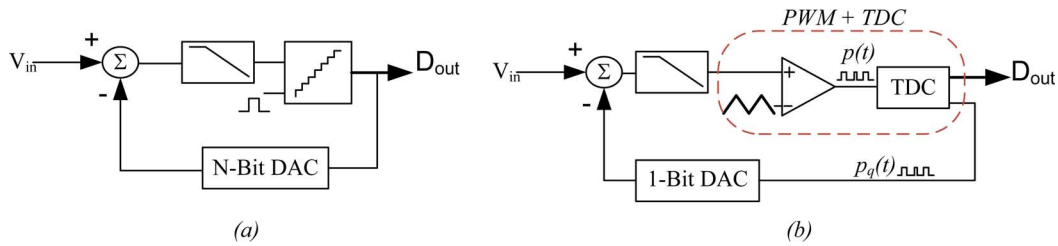

Fig. 2. Voltage-mode versus time-mode ΣΔ modulator. (a) Voltage-mode ΣΔ modulator. (b) Time-mode ΣΔ modulator.

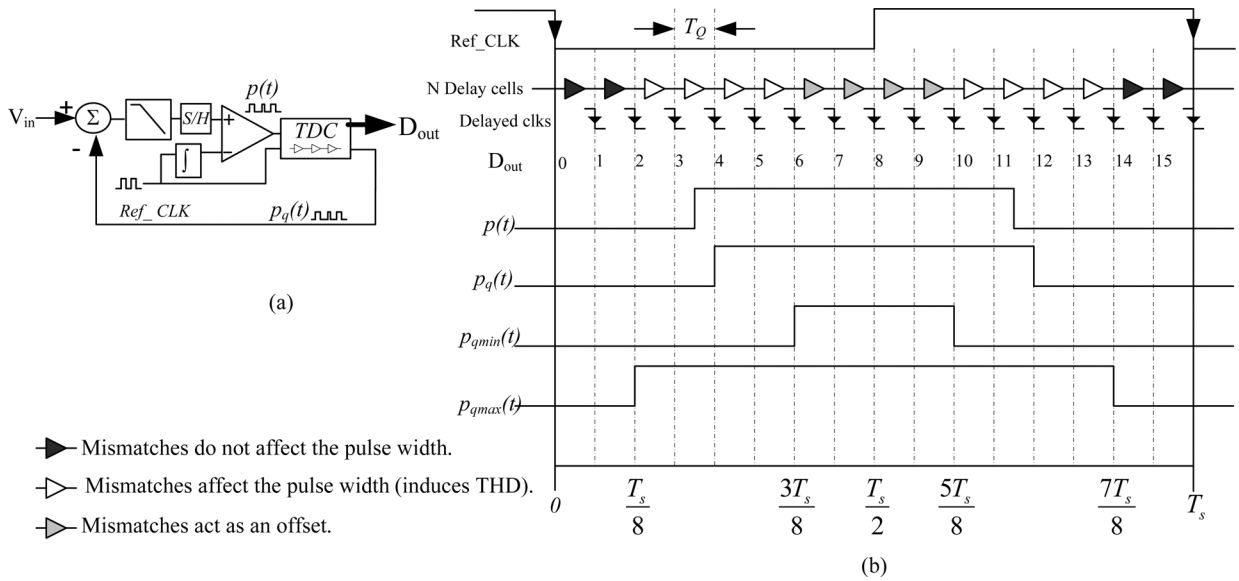

Fig. 3. TDC-based ADC: (a) Block diagram. (b) Timing diagram and $p_q(t)$ generation.

example, a 3-bits quantizer. In that case the quantizer step is $\mathrm{V_{FS}}/2^3$ and the voltage step of the feedback DAC will also be $\mathrm{V_{FS}}/2^3$. However, the error in the feedback signal, the DNL, should be less than $\mathrm{V_{FS}}/2^{10}$. By analogy from the voltage-mode to the time-mode ΣΔ modulator, the error, DNL, in the feedback signal $p_q(t)$ should be less than a single bit as it will not be shaped by the loop filter. These two remarks can be mapped as specifications for the TDC as follows: First, the number of quantization steps of the TDC can be decreased compared to the open loop case, shown in Fig. 1(a), which means that we can use time-quantization steps that are larger than one gate delay. That directly allows the use of TDC architectures with low latency and low dead-time. Thus, wide bandwidth ADC can be achieved. Second, the accuracy of the feedback signal, i.e., the width of the $p_q(t)$ pulses, is proportional to the targeted SNR which puts a constrain on the DNL (timing mismatch) of the TDC steps. As a numerical example, assume a 10-bit ADC that is designed using the open loop architecture shown in Fig. 1(a). The time-quantization step of the TDC will be given by $T_s/2^{10}$. On the other hand, if a third order ΣΔ architecture with an over-sampling ratio (OSR) of 6 is used then the time-quantization step of the quantizer can be as low as $T_s/2^{4.5}$ which relaxes the resolution of the TDC. On the other hand, the linearity of the feedback-pulse-width should be maintained higher than 10 bits which means that the DNL of the TDC should be better than 10 bits. In conclusion, by replacing the multi-bit voltage-mode feedback DAC by a TDC, the performance bottleneck is transformed to the timing-precision of the feedback pulse of the TDC, $p_q(t)$. Compared to the voltage-mode ΣΔ modulators, the multi-bit DAC became digital friendly and can be easily scaled down with the technology. In addition, minimizing the analog portion of the system (only the filter and the PWM are analog) makes the TDC-based ΣΔ modulator more suitable to nanometric technology. Since a reduced number of time-quantization steps is required compared to the open loop case, along with small latency to minimize the excess loop delay, inverter-chain-based TDC [10]–[13] is a suitable choice for time-mode based ΣΔ modulators.

III. System Level Design

Fig. 3 shows the timing diagram of a 16-level TDC-based ΣΔ modulator. The full scale input, $[0, T_s]$, is split, in time, into N (in Fig. 3 $N = 16$) time-quantization steps using inverter-chain-based delay cells which is driven by the sampling clock. Assuming perfect matching between the delay cells, the time-quantization step T_Q is given by T_s/N. The TDC performs two main functions. First, it identifies the position of the rising and falling edges of the PWM signal with respect to the falling edge of the PWM reference clock (4 and 12 on the diagram). Second, it emulates the multi-bit DAC operation by providing a time-quantized feedback pulse $p_q(t)$ whose edges are aligned to the time-quantization steps as shown in Fig. 3(b).

Since the TDC emulates the multi-bit DAC, two relevant specifications are the signal-to-jitter ratio (SJR) of the feedback

pulse and the maximum error, DNL, of the TDC time-steps. Note that the "signal" in this case corresponds to the pulse-width while the "noise" corresponds to its jitter.

A. Signal-to-Jitter Ratio (SJR)

Assuming a maximum input signal of -6 dBFs ($V_{\rm pp} = V_{\rm FS}/2$), where dBFs refers to the full scale input, and assuming that it is centered around $V_{\rm FS}/2$ and the PWM conversion gain is $T_s/V_{\rm FS}$, then the maximum feedback-pulse-width, $p_{q\max}(t)$, will be given by $T_s/2 * (1 + V_{\rm pp}/V_{\rm FS}) = 3T_s/4$ as shown in Fig. 3(b). Since the maximum pulse width corresponds to the peak-to-peak signal in the voltage domain, by analogy, its RMS value will be given by $3T_s/4 * 1/2\sqrt{2} = 3T_s/8\sqrt{2}$. Consequently, the signal-to-(pulse-width-jitter) ratio is given by

$$\mathrm{SJR} = 10\log\left(\frac{\left(3T_s/8\sqrt{2}\right)^2}{\sigma^2_{j-\mathrm{pw}}}\right) \tag{1}$$

where $\sigma_{j-\mathrm{pw}}$ is the standard deviation of the pulse-width jitter of the feedback pulse integrated over the frequency band of interest.

B. DNL of TDC's Time Steps

If perfect matching between the delay cells in Fig. 3(b) is assumed, the DNL should be zero. Due to inevitable mismatches, the delay of the different steps will change introducing nonlinearities in the time-quantized feedback pulse $p_q(t)$. Since the input voltage-sample ranges from $V_{\rm FS}/4$ to $3V_{\rm FS}/4$ (assuming $V_{\rm pp} = V_{\rm FS}/2$), the pulse width will change from $T_s/4, p_{q\,\min}(t)$, to $3T_s/4, p_{q\,\max}(t)$, as shown in Fig. 3(b). The delay cells that are excited by the reference clock during the time intervals $[0, T_s/8]$, $[7T_s/8, T_s]$ will seldom interact with the output pulse width (black delay cells on Fig. 3(b)). Hence, their mismatch does not affect the performance. On the other hand, the mismatch of the cells excited during the time interval $[3T_s/8, 5T_s/8]$ (gray cells on the timing diagram) will contribute equally to all the pulse widths so their contribution will be transformed as offset in the pulse width rather than a harmonic distortion. Consequently, the time mismatches that contribute to THD are those of the cells who are active during the time intervals of $[T_s/8, 3T_s/8]$ and $[5T_s/8, 7T_s/8]$ (white cells on the timing diagram). Since the output pulse is symmetric and centered around $T_s/2$ as shown in Fig. 1(b), in the following analysis single side of the pulse-width will be considered then a 3 dB improvement in the THD will be considered due to having the two sides at the output. Another observation is that the time-quantized feedback pulse consists of the summation of the individual delays of the different delay cells where each delay cell represents one LSB. Consequently, the TDC can be considered as a time-mode thermometric DAC, where each delay cell corresponds to a time-mode 1-bit DAC. This observation is useful while analyzing the harmonic distortion of the TDC.

For simplicity of the harmonic distortion analysis, an M-level voltage-mode thermometric DAC will be considered then an analogy is performed to get the mismatch specification on the time-mode counterpart. Fig. 4(a) shows the output of an M-level (12-levels as an example) DAC for a one period of a digital sinusoidal signal of frequency $\omega_{\sin}$ with OSR of 15. Since the DAC architecture is a thermometric one, it can be represented as M 1-bit DACs followed by a summer as shown in Fig. 4(b). Each square wave signal, the outputs of the 1-bit DACs, can be expanded in terms of its harmonics using Fourier series:

$$x_{\mathrm{sq.}(i)}(t) = \sum_{k=1}^{\infty} \frac{2}{\pi k} A \sin(k\phi_i)\cos(k\omega_o t),$$
$$\text{where } x_{\mathrm{sq.}(i)}(t) = 1 \text{ for} |t| \le \frac{\phi_i}{\omega_{\sin}},$$
$$i = 1, \ldots, M, 0 < \phi_i < \pi. \tag{2}$$

Consequently, the M-level DAC output is given by

$$x_{\rm DAC}(t) = \sum_{k=1}^{\infty}\left\{\frac{2}{\pi k}\sum_{i=1}^{M}\left[A\sin(k\phi_i)\right]\,\cos(k\omega_o t)\right\} \tag{3}$$

where A represents the step height in voltage-mode DAC, k is the harmonic index and ϕ_i represents the phases of the different 1-bit signals.

To estimate the effect of the 1-bit DAC mismatches on the THD, a third-harmonic-free and fifth-harmonic-free digital sinusoidal signal similar to the one shown in Fig. 4(a) is generated using the technique proposed in [3]. The condition to generate such input signal is

$$\sum_{i=1}^{M}\sin(k\phi_i) = 0, \quad \text{for } k = 3, 5. \tag{4}$$

If the above condition is satisfied, the third and fifth harmonics will vanish according to (3). Assuming amplitudes mismatches in the different 1-bit DACs, the M-level DAC output will be given by

$$x_{\rm DAC}(t) = \sum_{k=1}^{\infty}\left\{\frac{2}{\pi k}\,\sum_{i=1}^{M}\left[(A+\Delta A_i)\sin(k\phi_i)\right]\cos(k\omega_o t)\right\}. \tag{5}$$

Thus, its third and fifth harmonic are no longer zero. The harmonic distortion of $x_{\rm DAC}(t)$ becomes

$$\mathrm{HD}_k = \frac{1}{k}\frac{\displaystyle\sum_{i=1}^{M}\left[(1+\Delta A_i/A)\sin(k\phi_i)\right]}{\displaystyle\sum_{i=1}^{M}\left[(1+\Delta A_i/A)\sin(\phi_i)\right]}. \tag{6}$$

Since $\sum_{i=1}^{M}\sin(k\phi_i) = 0$ for $k = 3, 5$ and $\Delta A_i/A \ll 1$, the expression can be simplified to

$$\mathrm{HD}_k \cong \frac{1}{Ak\displaystyle\sum_{i=1}^{M}\sin(\phi_i)}\sum_{i=1}^{M}\left[\Delta A_i\sin(k\phi_i)\right], \quad k = 3, 5. \tag{7}$$

Assuming a Gaussian distribution for the amplitude mismatches ΔA_i with standard deviation $\sigma_{\Delta A_i}$, the distribution

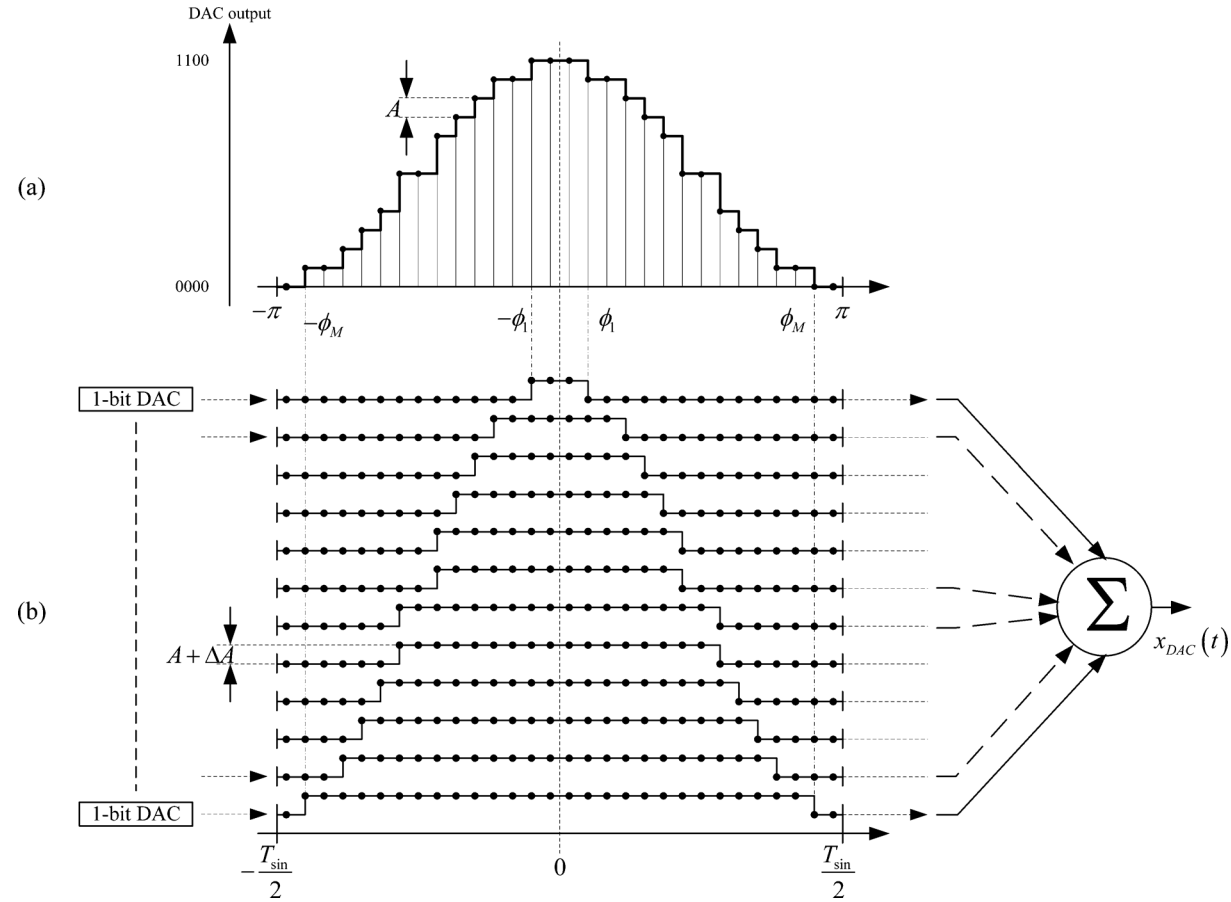

Fig. 4. M-level feedback DAC: (a) DAC output signal. (b) Thermometric DAC architecture.

of HD_k will also be Gaussian with zero mean and standard deviation σ_{HD_k} as it is a summation of Gaussian distributions.

$$\sigma_{\mathrm{HD}_k} = \frac{\sigma_{\Delta A_i}}{Ak\sum_{i=1}^{M}\sin(\phi_i)}\sqrt{\sum_{i=1}^{M}\sin^2(k\phi_i)} \tag{8}$$

For $\mathrm{HD}_k < B$, then σ_{HD_k} should be $< B/2$ for a 95% yield (2σ on Gaussian distribution covers 95% of the area under the curve). Thus, the standard deviation of the mismatch will be given by

$$\sigma_{\Delta A_i} < \frac{B}{2}Ak\frac{\sum_{i=1}^{M}\sin(\phi_i)}{\sqrt{\sum_{i=1}^{M}\sin^2(k\phi_i)}}. \tag{9}$$

Consequently, once the system level simulations of the $\Sigma\Delta$ modulator is performed and the maximum distortion of the DAC, B, and the time-quantization step in the TDC, T_Q which corresponds to A in voltage-mode DACs, are specified, both can be plugged in the above equation to obtain the maximum tolerable mismatch between the different time-steps which corresponds to the DNL of the TDC.

System level simulations for the $\Sigma\Delta$ modulator were performed targeting 10+ bits resolution over a bandwidth of [100 kHz, 20 MHz] [7]. A third-order active-RC inverse-Chebyshev loop filter is used. The PWM signal is generated by comparing the input with a ramp waveform V_r. V_r is generated by switching currents into capacitors using a clocked differential pair. The comparators are implemented by using inverters as transconductors with outputs tied together and fed to a cascade of two inverters that generate $p(t)$ [9]. The nonlinearity due to sampling switches, non-ideal ramp waveform and the signal-dependent comparator delay can easily be tolerated up to 40 dB due to noise shaping. An OSR of 6.25 is used which corresponds to a sampling rate of 250 MHz (sampling period $T_s = 4$ ns). The SNR of the TDC and its digital output buffer should be better than 72 dB over the signal bandwidth. The TDC is required to have 50 quantization steps which correspond to a step size of 80 ps. Since T_s is 4 ns, the standard deviation of the jitter of the time-quantized feedback pulse width, $\sigma_{j_{-\mathrm{pw}}}$, must be kept less than 266 fs for SJR $>$ 72 dB according to (1). Finally, targeting 65 dB THD assuming -3 dBFs input implies a standard deviation of the delay of the different TDC steps of around 480 fs according to (9) with ± 40 fs variations depending on the choice of the harmonic-free digital input signal (the choice of ϕ_i). However, system level simulations of the $\Sigma\Delta$ modulator along with the TDC model indicate that the mismatch specifications can be relaxed to be around 800 fs for a -3 dBFs input. In addition,

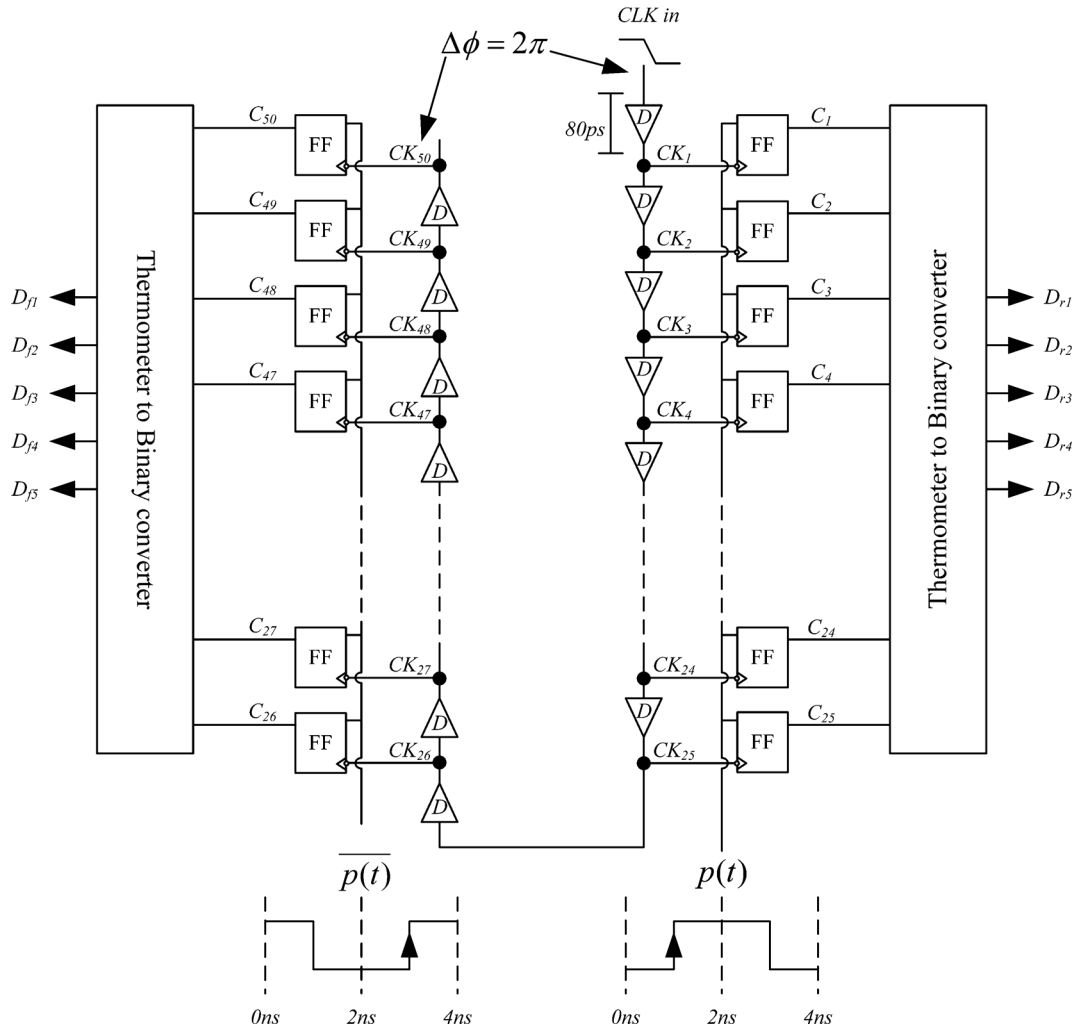

Fig. 5. Block diagram of the output code generation of the TDC (left side captures $p(t)$ falling edge while the right side captures the rising edge).

the delay of the feedback pulse should be minimized to have minimum effect on the excess loop delay of the ΣΔ loop. System level simulations indicate that a TDC delay larger than 600 ps can push the loop outside the stable region of operation. Moreover, the delay must be constant to avoid data-dependent delay which distorts the signal.

IV. TDC Architecture

The TDC architecture is split into two parts: output code generation and the time-quantized feedback pulse, $p_q(t)$, generation. Fig. 5 shows the block diagram of the output code generation part of the TDC. A 50-cell inverter-based delay line whose total delay matches the period of the reference clock, 4 ns, is used. The first half of the line captures the rising edge of the input pulse while the second half captures its falling counterpart. The input signal, $p(t)$, is applied to the inputs of the flip-flops while the falling edge of the clock is applied to the delay line. As the clock propagates through the first half of the delay line it triggers the flip-flops sequentially in 80 ps steps to capture the time-position of the rising edge of $p(t)$ in a thermometric fashion. To capture the time-position of the falling edge of $p(t)$ by the second half of the line while maintain the symmetry of the design, $p(t)$ is inverted before being applied to the flip-flops of the second half of the TDC. Consequently, the second set of flip-flops captures the time-position of the rising edge of $\overline{p(t)}$ which corresponds to the time-position of the falling edge of $p(t)$. Since the flip-flop outputs are thermometric, a thermometer-to-binary converter is used to encode the thermometric output before it is further processed.

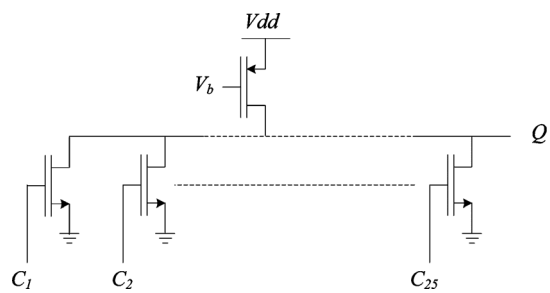

Fig. 6. Uniform-delay wired-NOR architecture for the feedback pulse, $p_q(t)$ generation.

Since the flip-flops in Fig. 5 are clocked through the delay elements, its outputs are aligned to the delay element outputs which are 80 ps apart. The rising and falling edges of the feedback pulse can be generated by applying the OR operator on

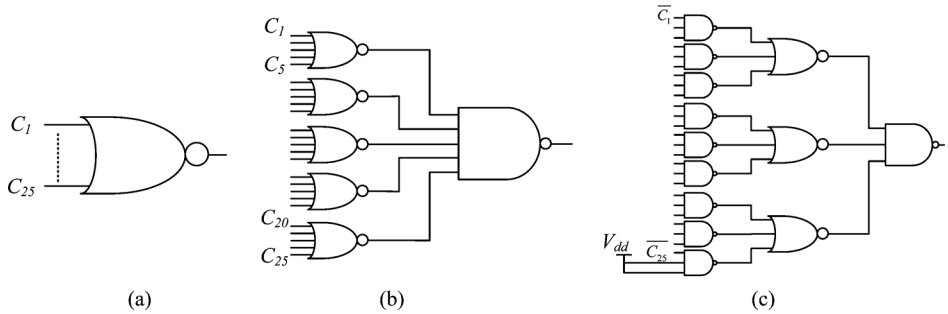

Fig. 7. Block diagram of the different architectures for implementing 25-inputs OR gate of Fig. 6(a) 1-level NOR gate. (b) 2-levels OR gate. (c) 3-levels OR gate.

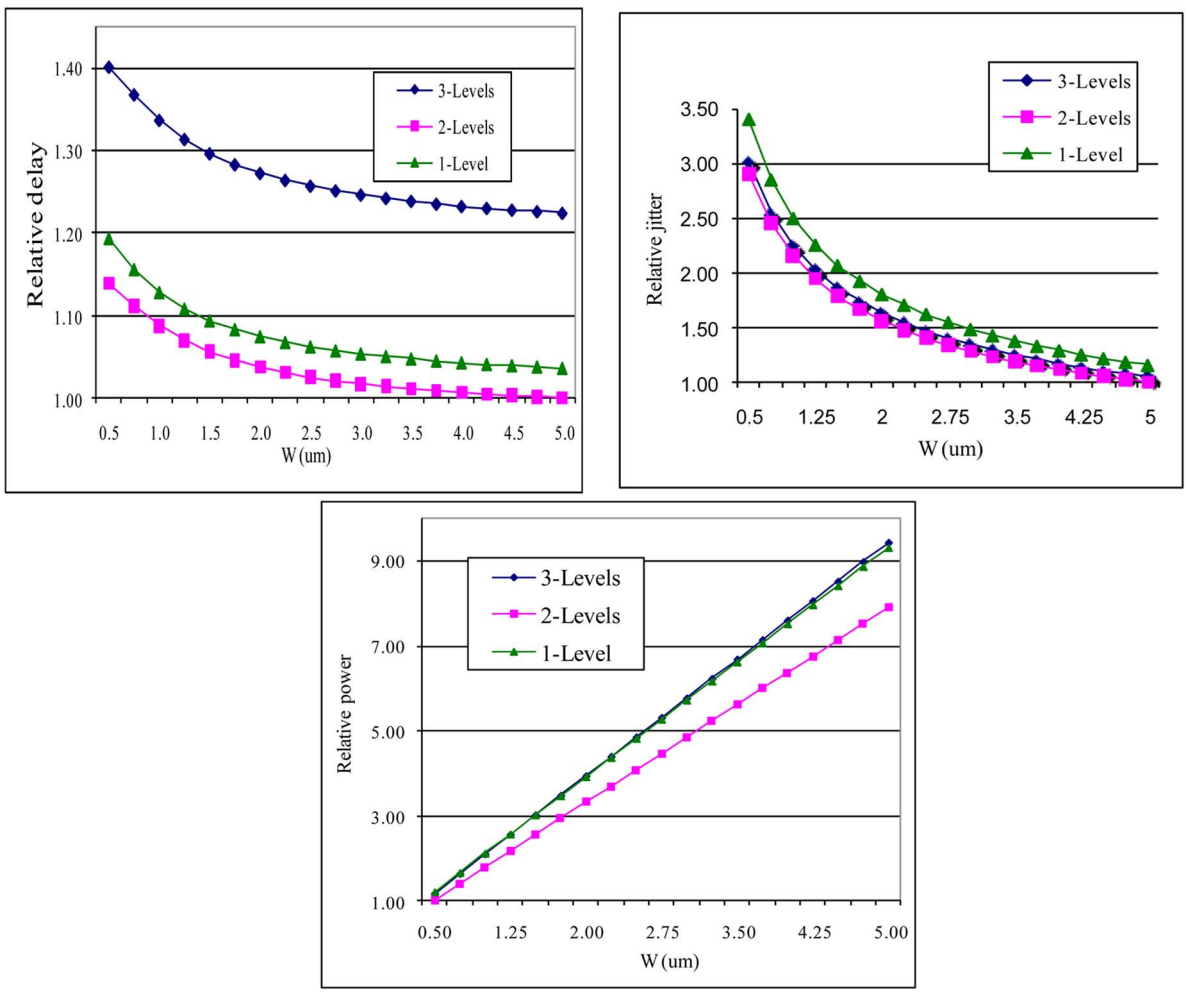

Fig. 8. Relative jitter of the different OR gate architectures versus transistor's width.

the first and second 25-outputs sets of the flip-flops (C_1 through C_{25} and C_{26} through C_{50}) respectively. In this case the feedback pulse edges are aligned to the delay-element-output edges with one flip-flop and OR gate delay. To ensure uniform delay from all inputs, (C_1 through C_{25} and C_{26} through C_{50}), to the output of the OR gate, the wired-NOR structure shown in Fig. 6 is used to generate the quantized signal $p_q(t)$.

Many techniques can be used to implement 25-inputs OR operation in wired-structure. The simplest one is to use a single NOR gate with 25 inputs as shown in Fig. 7(a). Other techniques are to use 2-levels or 3-levels OR operation as shown in Fig. 7(b) and (c), respectively. The 2-level OR is implemented using *NOR-NAND* structure while the 3-level OR is implemented using *NAND-NOR-NAND* structures. Three factors should be considered when choosing the optimum OR implementation: delay, jitter and power consumption. Fig. 8 shows the relative delay, jitter and power consumption of the three designs versus transistor width. In this case, it is clear that the 2-level architecture provides the best performance.

Since the timing-precision of the feedback pulse is required to be better than 0.8 ps, the metastability of the flip-flop should be within that limit which is impractical. To overcome this

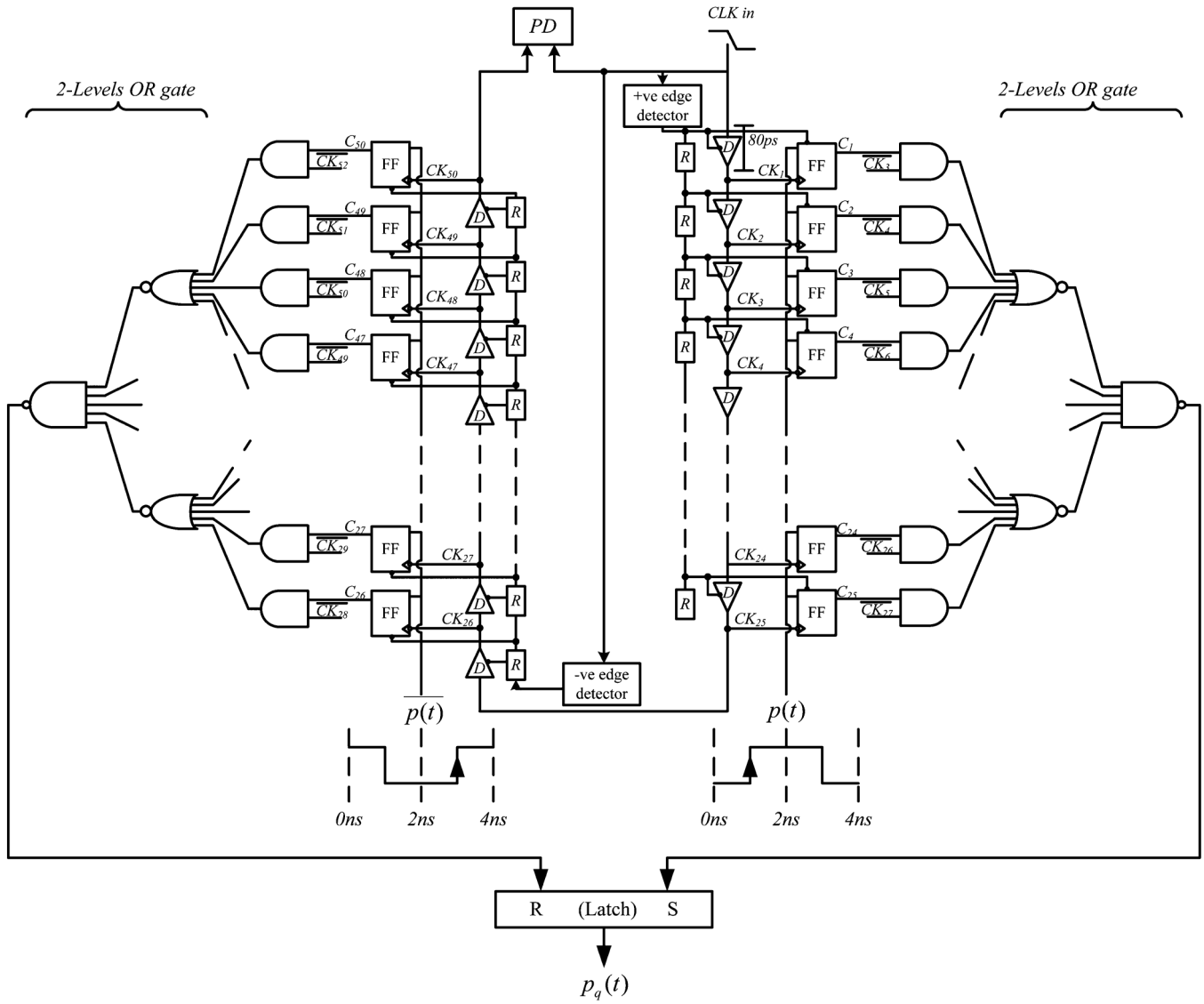

Fig. 9. Block diagram of the TDC with the feedback pulse generator $(p_q(t))$.

problem, the output of the flip-flop, that is triggered by CLK_n, is gated by another clock, $\overline{\mathrm{CLK}_{n+2}}$, to leave time for the flip-flop output to settle as shown in Fig. 9. In this case the flip-flop output edges are still aligned to the outputs of the delay elements but the feedback pulse will be delayed by two time steps, 160 ps, which adds to the total excess loop delay.

One important remark regarding the feedback generation part of the TDC is the mismatches between its time steps. The DNL of each time-step is contributed from the mismatches of the delay cells as well as the mismatch between the different paths of the 2-levels OR gate. Consequently, both the delay cell design and the OR-gate design are critical for the distortion performance of the TDC. In the following section the transistor level design of the TDC blocks are presented.

V. Transistor Level Implementation

Fig. 9 shows the block diagram of the TDC with the feedback pulse generator. The TDC consists of five sub-blocks: delay cells (D), flip-flop (FF), 2-levels OR gate, SR latch and reset unit (R). In addition, a phase detector (PD) is used to adjust the total delay of the line to be 4 ns. A DLL should be used to automatically tune the delay of the delay line; however, in the fabricated prototype the DLL was not included and manual tuning of the delay is performed. Having a DLL on chip will improve the performance since it will eliminate the temperature variations and the supply voltage variations.

The bottleneck of the TDC is its jitter and mismatch performance. The jitter includes the jitter of the delay line (50 delay cells), 2-level OR gate, SR latch, feedback buffer and supply noise. On the other hand, the mismatch includes process variations, systematic design mismatch, periodic noise from the supply, metastability and data dependent delay. For critical sections, transistors' length is set as double the minimum length of the process to reduce the effect of PVT variations. Monte Carlo simulations were used to provide a lower limit on the width such that the variation in the unit time-step is below the targeted DNL.

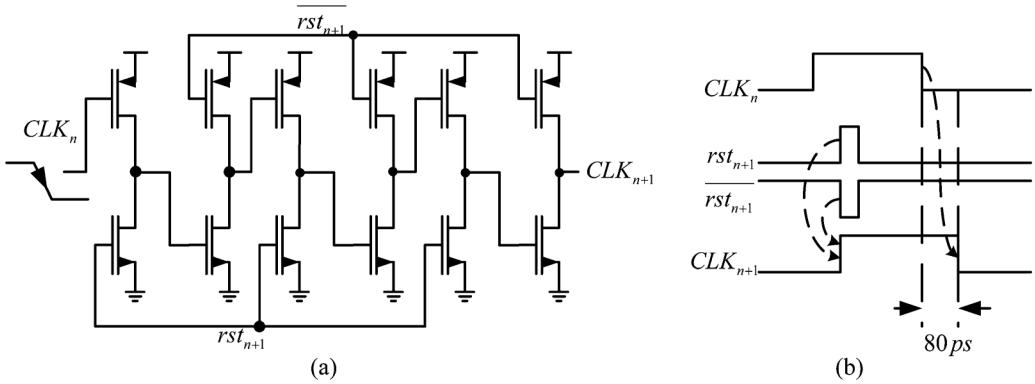

Fig. 10. Dynamic-logic-based delay cell (D) (a) Transistor level implementation. (b) Timing diagram.

A. Delay Cell

The delay cell incorporates even number of inverters to avoid the mismatch between the rising and falling edges of the different cells. Aiming for compact layout and minimum parasitic capacitance, each transistor is laid out as two fingers such that the source terminals (the supply and ground) are common between the successive inverters. To optimize the timing-jitter of the delay line, two design parameters are considered: output-referred transistor's voltage noise, v_n, integrated over 20 MHz bandwidth and the inverters' slew rate (SR). Timing jitter of a single inverter is approximately given by $J = (v_n)/(\mathrm{SR})$.

Transistor's noise can be decreased by increasing the width of the transistor. By doubling the transistor width a 3 dB is gained in the noise as well as the timing jitter. Unfortunately, the power consumption also doubles due to the increased capacitance in the circuit. In addition, SR does not improve significantly as both the driving capability of the transistor as well as the capacitive loading double. Moreover, increasing the power consumption increases the supply noise and affects the timing precision of the neighboring circuits ending up with a degraded overall performance. To overcome this drawback, innovative circuit techniques are employed to maintain the jitter within the required specifications. Assuming an N-inverters delay line and assuming uncorrelated noise sources, the total jitter of the line is given by

$$J = \sqrt{N}\frac{v_n}{\mathrm{SR}}. \tag{10}$$

By increasing the SR by a factor m the number of required inverters to produce the same total delay will roughly increase by the same factor leading to

$$J = \sqrt{N}\frac{v_n}{\mathrm{SR}} \Rightarrow J_{\mathrm{new}} = \sqrt{mN}\frac{v_n}{\mathrm{SR} * m} = \frac{1}{\sqrt{m}}\left(\sqrt{N}\frac{v_n}{\mathrm{SR}}\right). \tag{11}$$

As a rule of thumb, increasing the SR of the transitions by a factor m improves the jitter per unit delay by a factor $\sqrt{m}$. For example, having 8 transitions within 80 ps provides 30% less jitter compared to having 4 transitions only. To increase the SR without doubling the width of the transistor, dynamic logic techniques are used. A dynamic-logic-based delay-cell is shown in Fig. 10(a). The main advantage of dynamic logic is that the driver transistor drives one load transistor instead of two. Theoretically the slew rate is improved by a factor of two and the number of stages is doubled per unit delay compared to the static CMOS delay line. Although the number of stages doubled, the power consumption will slightly increase as the pre-charging/pre-discharging transistors are designed using minimum length. For example, if $L = 2L_{\min}$ is used for matching purposes in the static CMOS delay line, the same length can be used in the signal path in the dynamic-logic-based cell while the pre-charging/pre-discharging transistors are designed using $L_{\min}$. Thus, their width is also divided by two without losing their current driving capability. Consequently, the total capacitance of the delay line, as well as the power consumption, increases by 25% only per unit delay compared to the static CMOS delay line.

B. Flip-Flop

Fig. 11(a) shows the dynamic-logic implementation of the flip-flop while Fig. 11(b) and (c) shows two timing diagrams in case of capturing/missing the input data. The input signal, $p(t)$, is normally low while the CLK is normally high. If the CLK falling edge leads $p(t)$ as shown in Fig. 11(c) the output will not change. However, if the rising edge of $p(t)$ leads the falling edge of the CLK as shown in Fig. 11(b) the output node discharges and the flip-flop captures the data. Static inverters, I_1 and I_2, are designed to be unbalanced such that the transition of the output, Q, from low to high is enhanced.

C. 2-Levels OR Gate

To minimize the additional loop delay due to the AND stage that gates the flip-flop outputs, the AND gate is embedded in the two-levels OR gate as shown in Fig. 12. Dynamic logic ensures uniform and minimum delay for the different inputs. Transistor M_1 acts as an AND gate while M_2 is driven by the flip-flop output. Five of such branches are connected in parallel to implement the 5-input NOR gate. The second level *NAND* gate is implemented using five *PMOS* transistors in parallel to ensure uniform delay. MonteCarlo simulations indicate that the variations in the time step due to transistor mismatch in the different

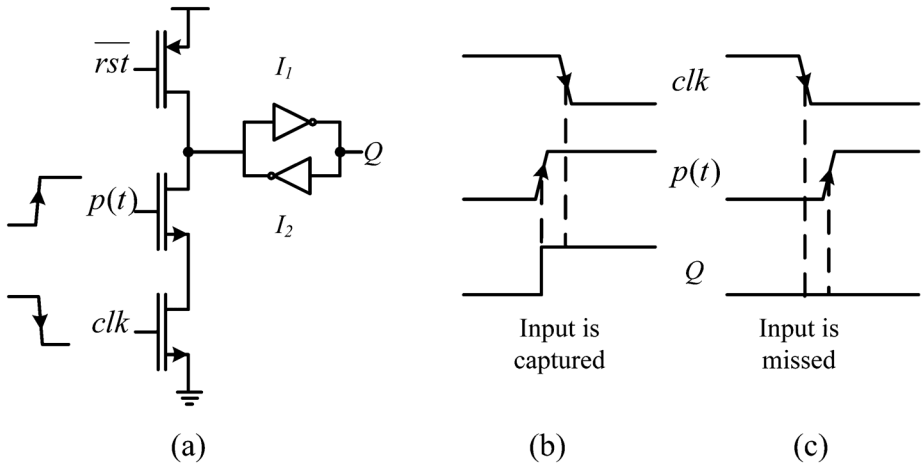

Fig. 11. Dynamic-logic-based flip-flop (FF).

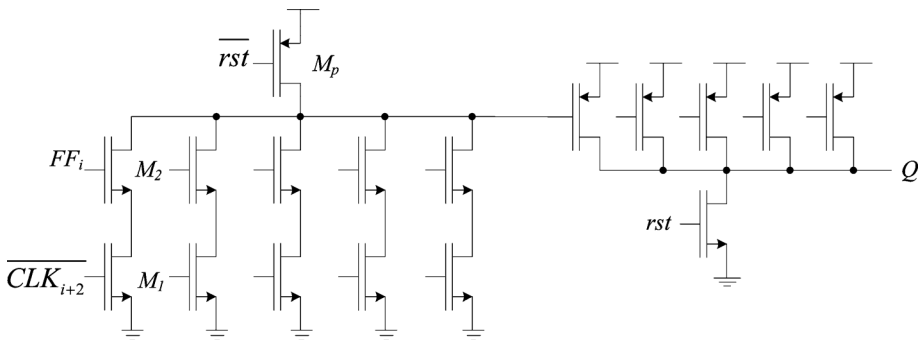

Fig. 12. Dynamic-logic-based OR gate.

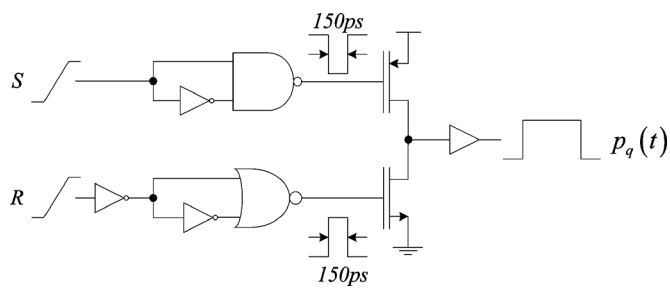

Fig. 13. SR latch for the feedback pulse generation.

paths including the delay cell is around 0.78 ps which fulfills the DNL specifications.

D. SR Latch

SR latch provides the feedback pulse of the ADC. Fig. 13 shows the block diagram of the circuit. The *set* input *(S)* is driven by the OR gate of the first half of the TDC which detects the rising edge of the input signal while the *reset* input *(R)* is driven by the OR gate of the second half that detects the falling edge. An edge detector detects the *set/reset* signals and generates a 150 ps pulse that charges/discharges the high impedance output node to generate the feedback pulse. The output node is buffered using a static CMOS inverter to eliminate the leakage effect of the high impedance node.

E. Reset Unit

The reset cell provides the reset signals to the dynamic-logic circuits. The TDC is split into two halves, one that handles the rising edge of the input pulse and one that handles its falling counterpart. Employing the fact that the two halves do not operate at the same time, the reset signal can be applied to the second half while the first half is handling the rising edge of $p(t)$ and vice versa as shown in Fig. 14. To prevent large instantaneous supply currents, the reset signal is applied sequentially to the 25 cells of each half incorporating a static minimum-size delay-line as shown in Fig. 9.

F. Jitter Analysis

The pulse-width of $p_q(t)$ is defined by its rising and falling edges. Consequently, the jitter of the pulse-width will be given by the root-mean-square of the independent jitters of its rising and falling edges. Since the rising and falling edges are both driven by the same edge of the reference clock, the jitter of the reference clock will affect the rising and the falling edges of $p_q(t)$ equally and will not affect the pulse width. On the other hand, the worst case jitter happens with a full scale signal. In this case the rising edge is captured by the first stages of the TDC, C_1 on Fig. 9, while the falling edge is captured by the very last stage of the TDC, C_{50} on Fig. 9. The jitter in the time difference between C_1 and C_{50} is contributed from the 50 cells of the delay line, $J_{\mathrm{Delay\_line}}$. In addition, each output, C_1 and C_{50}, will propagate through an OR gate, the SR-latch and the

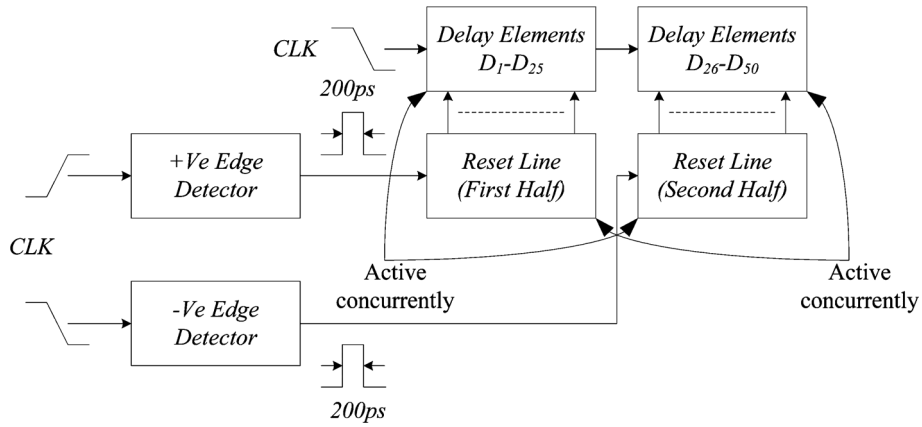

Fig. 14. Block diagram of the reset architecture of the TDC.

feedback buffer. Consequently, their jitter (the jitter of the OR gate, the SR-latch and the feedback buffer) will count twice in the pulse-width jitter of $p_q(t)$. Simulation results indicate that the integrated jitter of the 50-cell delay line is around 160 fs while the OR gate, SR latch and feedback buffer contribute with 90 fs. Hence, the worst case RMS jitter is given by

$$J_{\rm tot} = \sqrt{J^2_{\rm Delay\_line} + (\sqrt{2} * J_{\rm OR\_SR\_buf})^2} = \sqrt{160^2 + (90\sqrt{2})^2} = 205 \text{ fs}. \quad (12)$$

This timing jitter meets the system specs and leaves a margin for supply-induced jitter and noise injected from the substrate.

G. Data Dependent Delay

A major issue in time-mode analog systems is the data-dependent delay, which is a variation in the time-quantized feedback pulse-width depending on the timing of the input signal. One cause of this phenomenon is the flip-flop metastability. Another source of data-dependent delay is due to the use of dynamic logic gates. Feed-through from nearby switching circuits affect the high impedance nodes causing its output voltage to change. To overcome such problem, it is required to use static CMOS circuits to buffer the critical high impedance nodes. One example of this problem occurs when the flip-flop outputs toggle and the switching feeds through to the high impedance nodes of the delay elements as shown in Fig. 15. When the flip-flop output changes from low to high, the signal passes through the gate-source capacitance of M_2 of the OR gate then through the drain-gate capacitance of M_1. Since the gate of M_1 is a high impedance node, the voltage on the capacitance connected to this node changes its switching time when the clock reaches this stage in the delay line. To overcome this problem, a static CMOS inverter is inserted between the delay cell and the OR gate to isolate the high impedance node of the delay element from the feed-through of the flip-flop transition.

The high impedance node at the output node of the first level of the OR gate, $Q_{\rm NOR\_GATE}$, also induces data-dependent delay. $Q_{\rm NOR\_GATE}$ is supposed to be V_{dd} before discharging independent of the inputs to ensure uniform delay. Due to the toggling of the FF from low to high, two factors affect the voltage of $Q_{\rm NOR\_GATE}$ before discharging. The first factor is the feed-through of the gate-drain capacitance of M_2. The second factor is the charge sharing between the capacitance at the output and the parasitic capacitance, C_p, between M_1 and M_2. In the reset phase of the TDC, the FF and the delay line are both reset then the OR gate is reset. Consequently, the voltage across C_p is zero after resetting. The feed-through increases the voltage of $Q_{\rm NOR\_GATE}$, however, the charge sharing effect dominates and the overall change in $Q_{\rm NOR\_GATE}$ is a drop in its output voltage. Depending on the number of flip-flops that catches the input data, the output voltage changes at least by ΔV and at most by 5 ΔV before discharging because the flip-flop implementation, shown in Fig. 11, is level sensitive not an edge triggered one. This change induces unequal delay for the different inputs of the NOR gate leading to harmonic distortion in the time-quantized feedback pulse. To prevent such effect, the flip-flop outputs are gated using static CMOS AND gates which are controlled by the delay line and spaced in time by one quantization step (80 ps) as shown in Fig. 16. Consequently, the flip-flop outputs are applied sequentially to the OR gate instead of being applied simultaneously. Assume that flip-flop number 3 is the first flip-flop to catch the input signal, then the outputs of the first two AND gates will not toggle. When $\rm AND_3$ toggles, M_{23} turns ON and $Q_{\rm NOR\_GATE}$

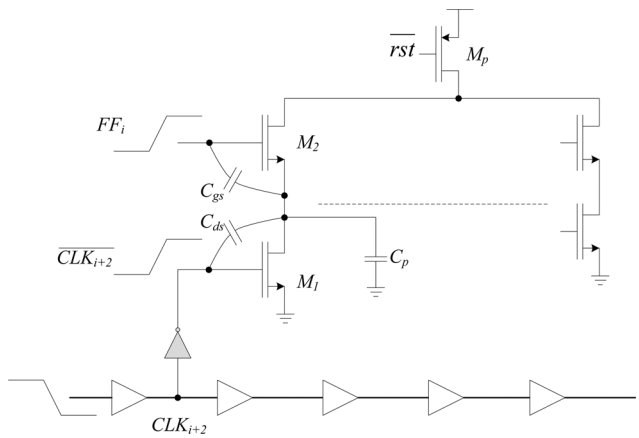

Fig. 15. Effect of flip-flop transition on the delay of the delay elements.

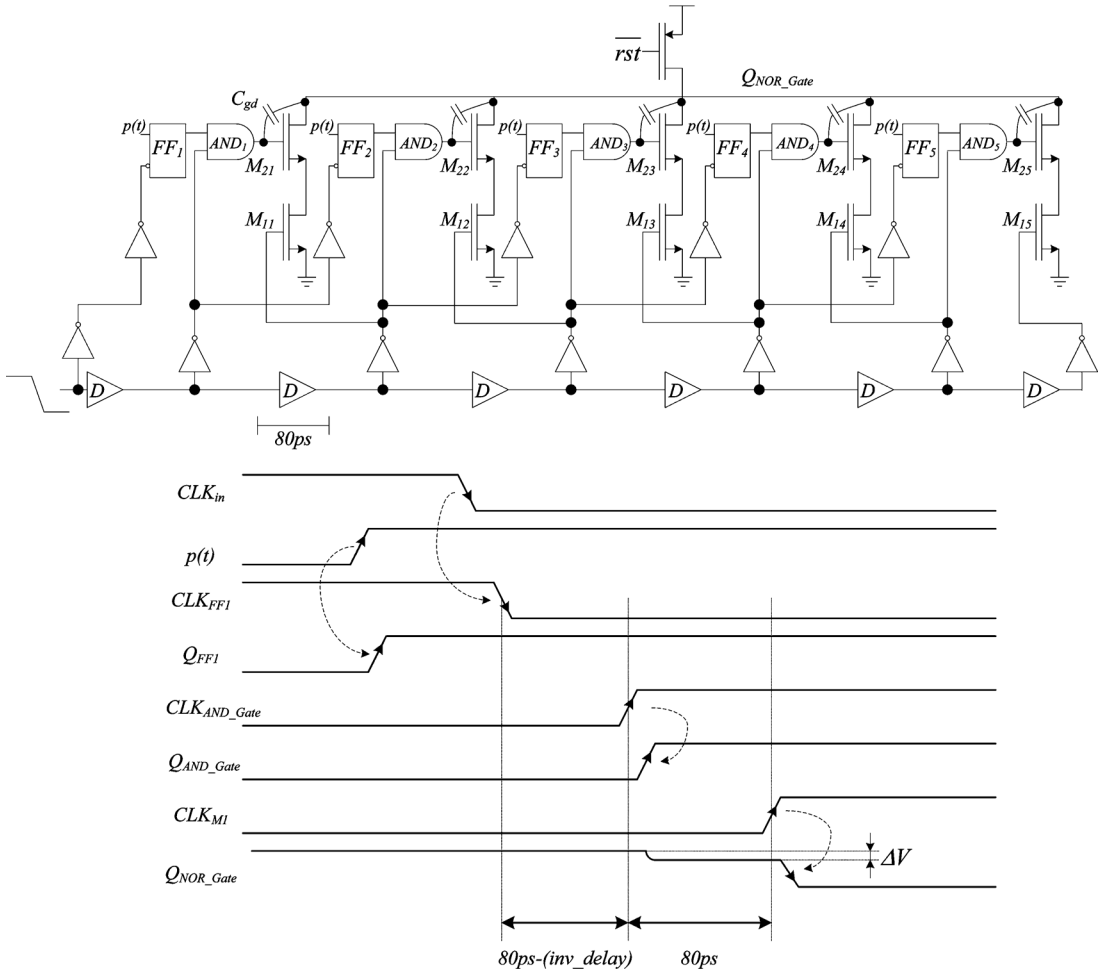

Fig. 16. Effect of flip-flop transition on the OR gate response.

drops by ΔV. Since the clock that triggers M_{13} takes a long time to propagate through AND_4 and to turn M_{24} ON compared to the time required to turn M_{13} ON and discharging $Q_{\mathrm{NOR\_GATE}}$, $Q_{\mathrm{NOR\_GATE}}$ will discharge before the toggling of AND_4 significantly affects its voltage. Simulations indicate that the implementation shown in Fig. 16 provides a linearity that is better than 80 dB which is far better than the targeted TDC linearity. In conclusion, the output node of the OR gate always drops by one ΔV before discharging leading to a uniform delay for the different inputs.

VI. Layout Considerations and Experimental Results

The TDC is implemented in TI 65 nm CMOS technology with a sound layout that matches the interconnects and the boundary conditions for the different signals. In addition, N-well guard rings are used to reduce the effect of substrate noise. Since recent research shows that asymmetric metal filling on different transistors can cause mismatches up to 30% [14], [15], metal filling is performed manually such that each cell and each signal see the same pattern of metal coverage. Fig. 17 shows the layout of the TDC while Fig. 18 shows the chip micrograph. The TDC occupies 0.006 mm^2 with a gate count higher than 2.5 K.

The input signal is generated from a moderate performance signal generator (Agilent E4432B) and a high-Q, passive, LC bandpass filter was used to remove the noise and distortion of the signal source to get an input signal of THD < -75 dB. Power supply lines were filtered using off-the-shelf line filters to remove noise and spurious tones and was further regulated using on-board adjustable regulators. A 5-bit low-voltage differential signal (LVDS) interface running at 500 MHz clock speed was used to capture the data with a high-speed logic analyzer (Agilent 16950 B). The low capacitance differential probe (E5387A) was used to connect the on-board LVDS buffers to the logic analyzer. The data captured from the logic analyzer represents the quantized pulse timing edges and are used to reconstruct the PWM waveform in MATLAB®.

The output spectrum for a -6 dBFs input signal is shown in Fig. 19. The THD of the output is -67 dB and the SNDR is 60 dB which corresponds to an effective number of bits (ENOB) of 9.67. This THD is the upper limit of the harmonic distortion of the TDC as the THD includes the effect of the HD of the filter and the PWM generator. Fig. 20 shows the measured SNR and SNDR of the ΣΔ modulator versus the input signal level for 20 MHz bandwidth. The ADC dynamic range, defined as the range of SNR > 0 dB, is 68 dB. Since the in-band noise floor has the shaping of the noise-transfer-function of the filter, it is expected that it is not resulted from the TDC since the TDC is located in the feedback path. Consequently, the TDC's dynamic

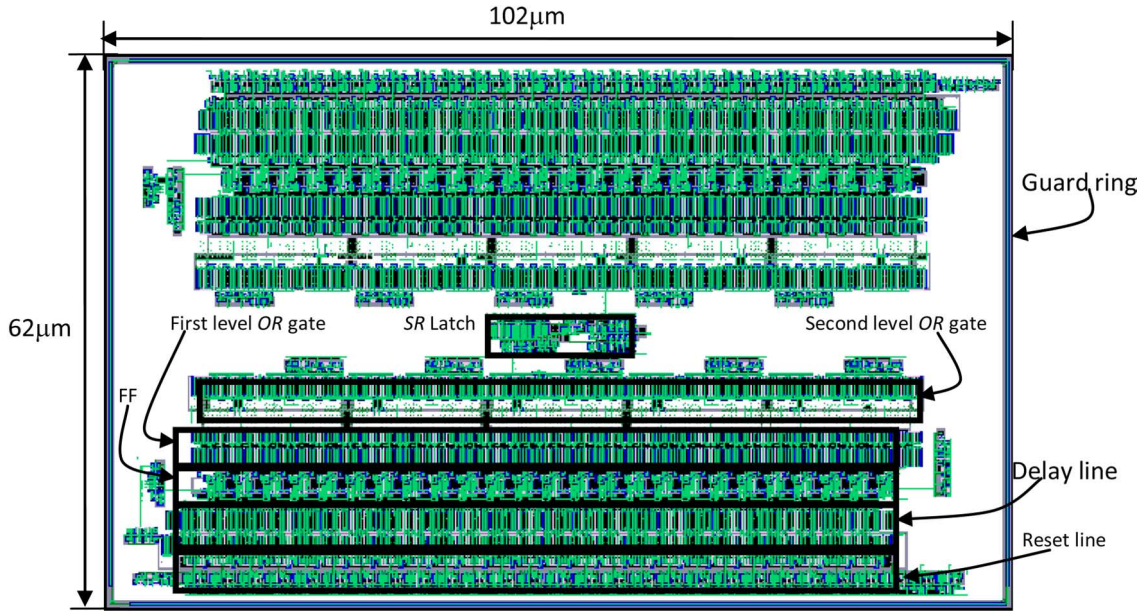

Fig. 17. Layout of the TDC.

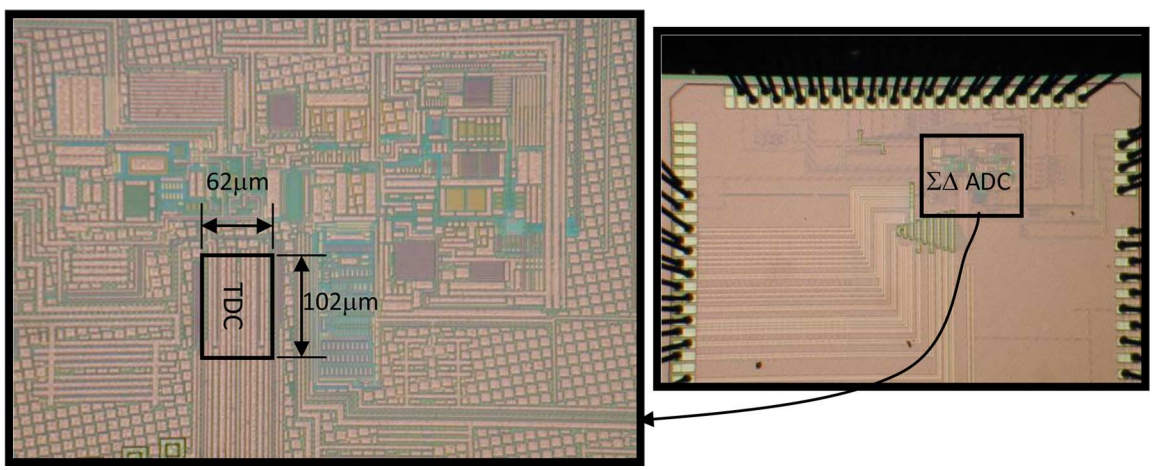

Fig. 18. Chip micrograph.

range is higher than 68 dB. The measured THD corresponds to a DNL better than 0.8 ps including mismatch and systematic power supply noise. Since harmonic distortion of the ADC is limited by the filter not the TDC [9], the linearity of the TDC is higher than 70 dB.

The TDC consumes 4.2 mA from 1.33 V supply with conversion rate of 250 MHz and provides an ENOB of 5.64 bits at the output and 9.67 bits at the feedback node. The number of bits at the output corresponds to the 50 quantization steps used in the quantizer ($2^{5.64} = 50$) while the 9.67 bits corresponds to a measured SNDR of 60 dB. For the power-consumption figure-of-merit $\mathrm{FOM}_P = P/f_{\mathrm{conv}}2^{\mathrm{ENOB}}$, the modulator and the feedback pulse shaper achieve 450 fJ/conv-step and 27.8 fJ/conv-step, respectively. For the area figure of merit defined as $\mathrm{FOM}_A = A/f_{\mathrm{conv}}2^{\mathrm{ENOB}}$, the modulator output and the feedback PWM shaper efficiencies are 0.505 nm^2/conv-step and 0.0309 nm^2/conv-step, respectively. Table I compares the measurement results with the state-of-the-art TDCs. It is observed that the proposed TDC incorporated in the $\Sigma\Delta$ loop outperforms the existing state-of-the-art TDCs in DNL, event rate along with FOM_A and FOM_P.

VII. Conclusion

A TDC in 65 nm technology that is capable of providing DNL better than 800 fs while employing simple inverter-chain is presented. Combining $\Sigma\Delta$ architecture and the dynamic logic implementation, an event rate of 250 MHz was achieved. Measurement results show that timing-precision of sub-ps in 65 nm technology is possible without calibration. Since the jitter is inversely proportional to the slew rate as shown in (10), migrating to new technology is expected to improve the jitter and to provide more timing precision that allows higher dynamic range. The TDC shows competitive area and power consumption that makes it suitable for mobile devices for long battery life and cost as well.

TABLE I
TDC MEASUREMENT RESULTS COMPARED WITH THE STATE-OF-THE-ART TDCS

	[16]	[17]-[18]	[19]	[20]	This work
Topology	Coarse-fine	4x interpolation	Pulse-shrinking	Cyclic SAR	Inverter-chain
Technology	90nm	90nm	-	0.35μm	65nm
ENOB	9 bits	7 bits	11 bits	13	9.67@ feedback
LSB	1.25ps	4.7ps	50ps-1ns	1.22ps	80ps
Input range	640ps	601ps	>100ns	327μs*	4ns
Event rate (MHz)	66	180	1	5	250
DNL	1ps	2.82ps	0.5LSB	~1.2ps	**Better than 0.8ps**
Supply voltage	1V	1.2V	-	3.3V	1.33V
Power consumption	3mW @ 10MHz	3.6mW	10mW @ 100kHz	33mW	5.66mW @ 250MHz
Area (mm^2)	0.6000	0.0200	-	4.4500	0.0063
FOM_A (*nm^2/conv-step*)	17.755	0.868	-	108.64	0.505@ output 0.0309@ feedback
FOM_P (*fj/conve-step*)	88	156.25	49407	805.66	450@ output 27.8@ feedback

* Input range depends on the jitter of an external clock.

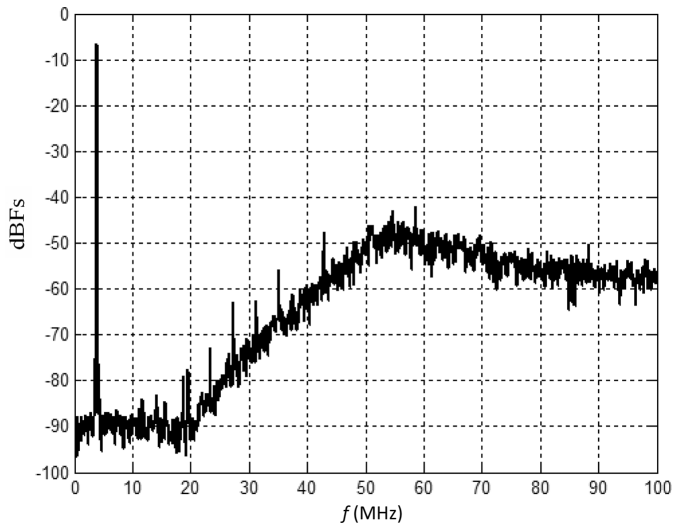

Fig. 19. Output spectrum for a −6 dB input signal.

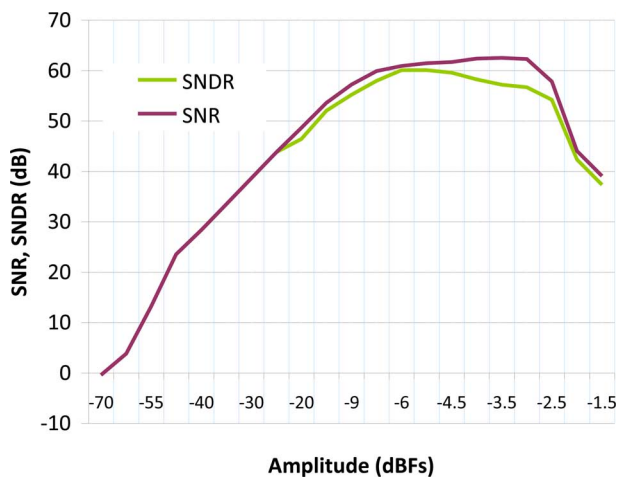

Fig. 20. SNR and SNDR of the ADC versus the input amplitude.

ACKNOWLEDGMENT

The authors would like to thank Alexander Reyes and Gaurav Chandra from Texas Instruments for the valuable discussions, Erik Pankratz, Chinmaya Mishra, and Lei Chen for layout support, and Texas Instruments Inc. for chip fabrication.

REFERENCES

[1] R. Tsuchiya, K. Ohnishi, M. Horiuchi, S. Tsujikawa, Y. Shimamoto, N. Inada, J. Yugami, F. Ootsuka, and T. Onai, "Femto-second CMOS technology with high-k offset spacer and SiN gate dielectric with oxygen-enriched interface," in *IEEE Symp. VLSI Technology*, 2002, pp. 1510–151.

[2] Y. Tsividis, "Continuous-time digital signal processing," *Electron. Lett.*, vol. 39, no. 21, pp. 551–1552, Oct. 2003.

[3] M. M. Elsayed and E. Sánchez-Sinencio, "A low THD, low power, high output-swing time-mode-based tunable oscillator via digital harmonic-cancellation technique," *IEEE J. Solid-States Circuits*, vol. 45, pp. 1061–1071, May 2010.

[4] M. Z. Straayer and M. H. Perrott, "A 10-bit 20 MHz 38 mW 950 MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based quantizer and DEM circuit in 0.13 um CMOS," in *Proc. IEEE VLSI Circuits Symp.*, Kyoto, Japan, June 2007, pp. 246–247.

[5] S. Naraghi, M. Courcy, and M. Flynn, "A 9b 14 μW 0.06 mm^2 PPM ADC in 90 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2009, pp. 168–169.

[6] S. Henzler, *Time-to-Digital Converters*. New York: Springer, 2010.

[7] X. Kang *et al.*, "A simple smart time-to-digital convertor based on Vernier method for a high resolution LYSO MicroPET," in *IEEE Nuclear Science Symp.*, Oct. 2007, vol. 4, pp. 2892–2896.

[8] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sánchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. Pankratz, "A 20 MHz BW 68 dB DR CT ΔΣ ADC based on a multi-bit time-domain quantizer and feedback element," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2009, pp. 174–175.

[9] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sánchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. Pankratz, "A continuous time multi-bit DS ADC using time domain quantizer and feedback element," *IEEE J. Solid-States Circuits*, vol. 46, pp. 639–650, Mar. 2011.

[10] T. E. Rahkonen and J. T. Kostamovaara, "The use of stabilized CMOS delay lines for the digitization of short time intervals," *IEEE J. Solid-states Circuits*, vol. 28, pp. 887–894, Aug. 1993.

[11] Y. Arai, M. Ikeno, and T. Matsumura, "Development of a CMOS time memory cell VLSI and a CAMAC module with 0.5 ns resolution," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 784–788, Aug. 1992.

[12] Rothermel and F. Dell'ova, "Analog phase measuring circuit for digital CMOS IC's," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 853–856, 1993.

[13] M. Santos, "A CMOS delay locked loop and sub-nanosecond time-to-digital converter chip," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 3, pp. 1717–1719, 1996.

[14] X. Wu, J. Trogolo, F. Inoue, Z. Chen, P. Jones-Williams, I. Khan, and P. Madhani, "Impact of sinter process and metal coverage on transistor mismatching and parameter variations in analog CMOS technology," in *IEEE ICMTS'07*, pp. 69–73.

[15] H. P. Tuinhout and M. Vertregt, "Characterization of systematic MOSFET current factor mismatch caused by metal CMP dummy structures," *IEEE Trans. Semiconductor Manufacturing*, vol. 14, no. 4, pp. 302–310, Nov. 2001.
[16] M. Lee and A. Abidi, "A 9 b, 1.25 ps resolution coarse—Fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.
[17] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1666–1676, Jul. 2008.
[18] S. Henzler, S. Koeppe, W. Kamp, H. Mulatz, and D. Schmitt-Landsiedel, "90 nm 4.7 ps-Resolution 0.7-LSB single-shot precision and 19 pJ-per-shot local passive interpolation time-to-digital converter with on-chip characterization," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2008, pp. 548–549.
[19] K. Karadamoglou, N. Paschalidis, E. Sarris, N. Stamatopoulos, G. Kottaras, and V. Paschalidis, "An 11-bit high-resolution and adjustable-range CMOS time-to-digital converter for space science instruments," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 214–222, Jan. 2004.
[20] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3067–3078, Nov. 2009.

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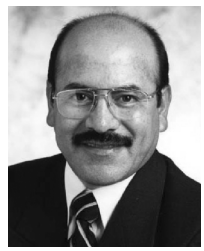
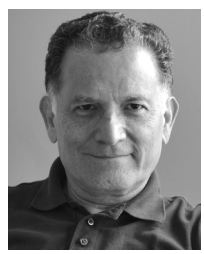


Jose Silva-Martinez (F'10) received the M.Sc. degree from the Instituto Nacional de Astrofísica Optica y Electrónica (INAOE), Puebla, México, in 1981, and the Ph.D. degree from the Katholieke Univesiteit Leuven, Leuven, Belgium, in 1992.

From 1981 to 1983, he was with the Electrical Engineering Department, INAOE, where he was involved with switched-capacitor circuit design. In 1983, he joined the Department of Electrical Engineering, Universidad Autónoma de Puebla, where he remained until 1993. He pioneered the graduate program on Opto-Electronics in 1992. In 1993, he re-joined the Electronics Department, INAOE, and from May 1995 to December 1998, was the Head of the Electronics Department. He was a co-founder of the Ph.D. program on Electronics in 1993. He is currently with the Department of Electrical and Computer Engineering of the Texas A&M University, at College Station, where he currently holds the position of Texas Instruments I Professor in analog engineering. He has published over 90 journal and 140 conference papers, one book and ten book chapters. His current field of research is in the design and fabrication of integrated circuits for communication and biomedical applications.

Dr. Silva-Martinez is an IEEE Fellow. He has served as IEEE CASS Vice President Region-9 (1997–1998), and as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 1997–1998 and 2002–2003, Associate Editor of IEEE TCAS I 2004–2005 and 2007–2009, and currently serves on the board of editors of six other major journals. He was the recipient of the 2005 Outstanding Professor Award by the ECE Department, Texas A&M University, co-author of the paper that won the RF-IC 2005 Best Student Paper Award, co-advised in testing techniques the student who was the winner of the 2005 Best Doctoral Thesis Award, presented by the IEEE Test Technology Technical Council (TTTC) of the IEEE Computer Society, and he was the recipient of the 1990 European Solid-State Circuits Conference Best Paper Award.



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His research work has more than 2 800 citations according to the Thomson Reuters Scientific Citation Index. He has graduated 46 M.Sc. and 36 Ph.D. students. He is a co-author of six books on different topics, such as RF circuits, low-voltage low-power analog circuits, and neural networks. He is currently the TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center at Texas A&M University. His current interests are in the area of power management, analog and medical electronics circuit design.

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