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A 40-nm CMOS 7-b 32-GS/s SAR ADC with Background Channel Mismatch Calibration

Dong-Shin Jo, Ba-Ro-Saim Sung, Min-Jae Seo, Woo-Cheol Kim and Seung-Tak Ryu

***Abstract* — This brief presents a 7-b 32-GS/s SAR ADC using a massive time-interleaving (TI) architecture. For low-skew multi-phase clocks, generation utilizing a delay-locked loop (DLL) phase-detector (PD) with a reduced offset is proposed to minimize skew between the clocks. Different clock path delays caused by distributed sub-ADCs over a large area in a massive TI-ADC are compensated for by multiplexing master clocks from the DLL. Offsets and skews in the sub-channels are calibrated on chip in the background via an additional dedicated sub-channel. A prototype chip was implemented in a 40-nm CMOS process with an active area of 0.36 mm^2. The measured SFDR and SNDR of the prototype ADC at a conversion rate of 32 GS/s are 43.1 dB and 31.4 dB, respectively. The ADC, including the input buffers, consumes 125 mW under a single 0.9 V supply.**

***Index Terms*—Analog-to-digital converter (ADC), time-interleaving, massive, successive approximation register (SAR), input buffer, offset, skew, calibration, DLL, phase-detector(PD).**

I. Introduction

In this early era of big data, the amount of communication data is increasing rapidly, increasing the need for advanced communication systems with wider bandwidths [1]. Due to the significant losses along communication media (channels) at high frequencies as the signal bandwidth increases, a higher level of quantization is required at the receiver front-end for digital equalization, as in ADC-based receivers [2] and coherent fiber-optical receivers [3]. The implementation of ADCs which operate at several tens of gigahertz for such applications requires a time-interleaving (TI) architecture in which mismatches between sub-channels must be taken into account [4-6].

Among the sources of channel mismatch in low-to-medium-resolution gigahertz TI-ADCs, sampling skew has the most significant effect on performance [7]. For this reason, various skew-calibration techniques have been investigated. A known timing reference assigned to the ADC input can eliminate the need for a wide-sense stationary process [8], but at the design overhead cost of the DAC and the external clock for time reference generation. One scheme [9] differs from an earlier one [8] in that the timing reference is internally generated by dividing the master clock, with skew detection conducted by means of reference clock sampling without a dedicated DAC. The present work utilizes the advantage of sensing simplicity in one study [9] while generating a multi-phase clock to eliminate the need for a high-frequency external clock. This is done by utilizing a low-skew delay-locked loop (DLL) with a new phase detector (PD).

The distribution of multi-phase sampling clocks to every sub-channel over the entire chip area is also an important design issue. T/Hs grouped together at the front end of the sub-ADC array can minimize routing-induced sampling skew, but the clock phase mismatch and corresponding sub-ADCs due to the distance can be another issue. An intentional delay to the T/H clocks may solve this problem [10], but an additional delay to the sampling clocks is not desirable in terms of sampling jitter. In the proposed work, sub-ADCs take the most suitable clock phase from the clock multiplexer, while T/Hs maintain minimized clock delay.

In this brief, a prototype 7-b TI SAR ADC with a 32-GS/s conversion rate is implemented with a major focus on the aforementioned clock-related issues. The rest of the paper is organized as follows: Section II briefly describes the overall ADC architecture. Section III explains the background offset and skew calibration processes in detail. Section IV presents the detailed circuit implementation, followed by the measurement results in Section V and the conclusion in Section VI.

II. Overall ADC Architecture

Fig. 1 shows the overall architecture of the designed 7-b 32-GS/s TI-SAR ADC. It consists of 16 slices ($SLICE_{1\text{-}16}$), each containing a T/H + input buffer and four sub-ADCs, and one additional slice ($SLICE_{CAL}$) for background calibration which has a T/H + input buffer and one sub-ADC. A T/H + input buffer helps to improve the bandwidth of the input sampling network. Each $SLICE_{1\text{-}16}$ operates with an interleaving period of 16 T_S, where T_S is the sampling period of the entire ADC, and each sub-ADC in a SLICE takes 64 T_S to convert a sampled input. A DLL is used for multi-phase clock generation for time-interleaved channels, generating $\Phi_{M<1:16>}$, each having a period of 16 T_S. The sub-channel SAR ADC is a conventional asynchronous SAR ADC [11] with a 7 b full-binary split-capacitor CDAC. V_{CM} is the input common level used for offset calibration, and T_{REF} is the reference clock for the purpose of

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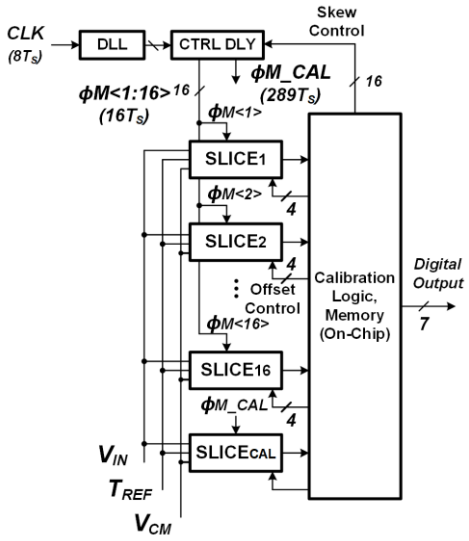

Fig. 1. Overall architecture of the TI-SAR ADC.

skew calibration. Both are provided externally. All required functional blocks, in this case the control logics for background calibration of the offset and the skew, are implemented on chip, as is the memory array for non-decimated output data capturing.

III. Offset and Skew Calibration

Unlike the ADC in earlier work [9] which assigns additional clock cycles in each sub-ADC for background calibration, the proposed design employs a dedicated ADC in $SLICE_{CAL}$ as a replacement for each channel. It is periodically selected and retired for calibration. If additional clock cycles are assigned in each sub-ADC, as in the aforementioned study [9] in this design, the next channel cannot sample a new input until the previous channel finishes calibration because the calibration reference (V_{CM} or T_{REF}) must be retained via the T/H. The dedicated ADC in $SLICE_{CAL}$ avoids this timing issue and enhances the conversion speed of the sub-ADCs.

While an interleaving operation occurs in the proposed design, as in typical TI ADCs, channel replacement for background calibration occurs as follows (refer to Fig. 2): First, SAR_{1_1} (the first SAR in $SLICE_1$) is selected for offset calibration and replaced by SAR_{CAL} (in $SLICE_{CAL}$). After offset calibration for SAR_{1_1} is done, SAR_{2_1} (the first SAR in $SLICE_2$) is replaced by SAR_{CAL} for the next offset calibration. This offset calibration process continues until each sub-ADC is calibrated once including SAR_{CAL} in $SLICE_{17}$, following the offset calibration of the last ADC in the last normal SLICE (i.e., SAR_{16_4} in $SLICE_{16}$). Once offset calibration is done for each sub-ADC, skew calibration begins with the same operational sequence used for offset calibration, beginning with SAR_{1_1} and finishing with SAR_{16_4} and SAR_{CAL}. As one complete cycle of skew calibration for all T/Hs is done, the offset calibration cycles begin again, and the two calibration operations run in an iterative manner. This calibration sequence is illustrated at the bottom of Fig. 2. Note that while $SLICE_{CAL}$ (= $SLICE_{17}$) has only a single ADC, SAR_{CAL}, the corresponding calibration timing is designed as if it has four sub-ADCs.

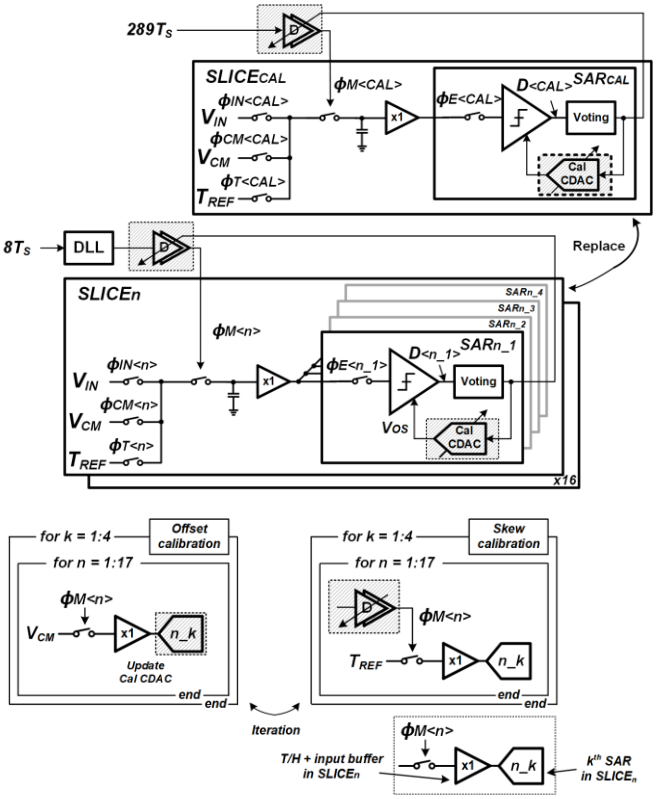

Fig. 2. Block diagram for background offset and skew calibration.

According to earlier work [12], channel calibration for an N-channel TI ADC needs a calibration period of (N+1) T_S. In an existing 8-channel TI ADC [12] as an example, the calibration period for each channel was 9 T_S. As the sampling rate of a TI-ADC reaches several tens of gigahertz, power consumption stemming from the calibration process during the (N+1) T_S period can be considerable. In order to slow down the calibration cycle, the calibration period can be set to (N+α) T_S, where α is a coprime of N. In this design, the calibration cycle is set to 289 T_S (α=272) for 17 SLICEs.

As illustrated by the input network of each SLICE shown in Fig. 2, when SAR_{n_k} is in the skew-calibration mode, it receives the timing reference clock, T_{REF}, as an input through the analog 3-to-1 multiplexer (MUX). T_{REF} is sampled by the T/H in the form of voltage at the falling edge of the sampling clock $\Phi_{M<n>}$ for $SLICE_n$. If the falling edge of $\Phi_{M<n>}$ is faster than that of T_{REF}, the output of the comparator, $D_{<m>}$, will be zero. Accordingly, the path delay of $\Phi_{M<n>}$ will be controlled to increase. In the opposite case, the delay of $\Phi_{M<n>}$ will be decreased. After the layout step, a Monte-Carlo simulation estimated that the 1σ skew is approximately 9.5 ps. Considering the design burden of the skew calibration circuitry, the skew control range of $\Phi_{M<1:16>}$ was designed to be 19.2 ps ($\approx 2\sigma$) with a step size of 153 fs.

The offset of each channel is calibrated by adjusting the comparator offset in each sub-ADC. When SAR_{n_k} is selected for calibration, it samples V_{CM} for a zero-differential input via the 3-to-1 MUX while the comparator indicates the offset polarity.

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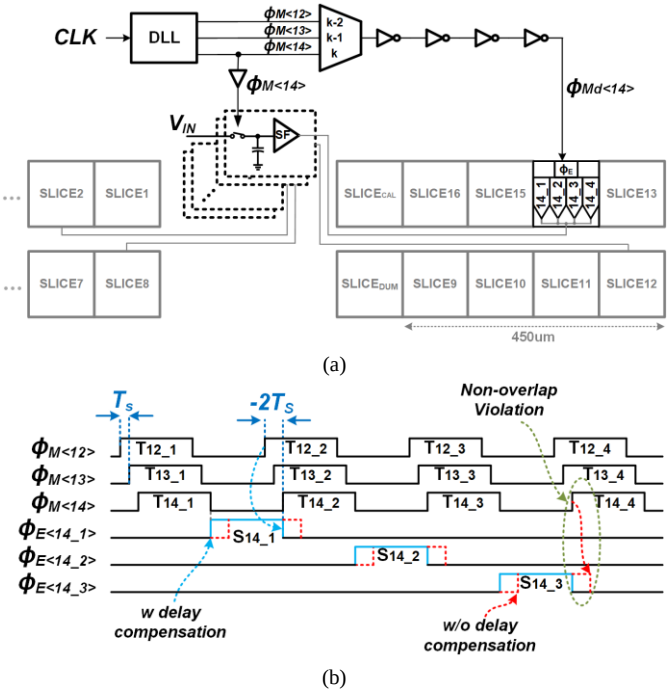

Fig. 3. (a) Conceptual floor plan of TI-ADC (b) Timing diagram for delay compensation.

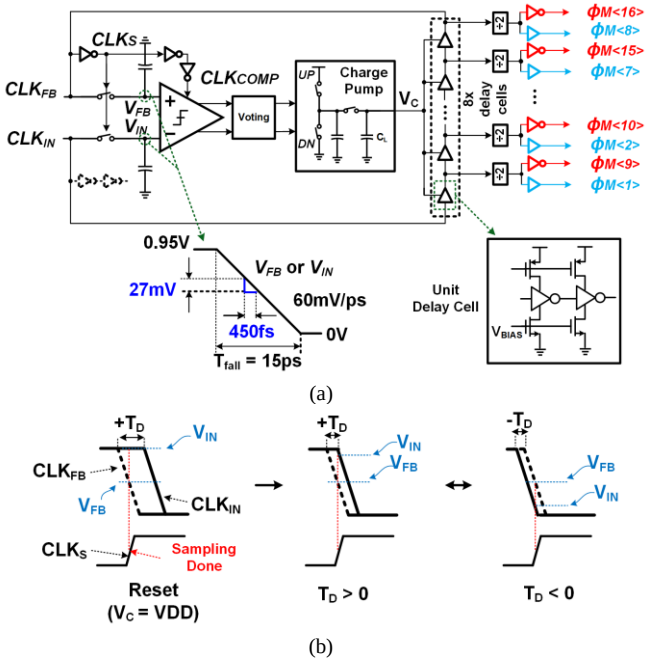

Fig. 4. (a) Architecture of the proposed PD. (b) Voltage control for DLL locking.

The comparator in this case is a well-known strong-arm structure with an additional input pair for offset calibration. The calibration logic controls the offset calibration CDAC (Cal CDAC) to reduce the offset. In order to guarantee 7-b linearity, the step size of the offset calibration is designed to be less than 1/4 LSB.

As the calibration sequence for each channel takes 289 T_S and there are two calibration modes (offset, skew), the offset calibration for each sub-ADC returns every 39304 T_S (= 2 modes × 17 SLICEs × 4 ADCs/SLICE × 289T_S), which corresponds to 1.28 μs in a 32 GS/s operation. In order to avoid the leakage problem during this long calibration period, the offset calibration CDAC resets after every SAR conversion and reloads the calibration code.

IV. Circuit Implementation

A. Clock Paths to T/H and Sub-ADCs

Fig. 3(a) shows the floor plan, presenting the location of the T/H + input buffer array and that of the sub-ADC array. Note that all T/Hs + input buffers are located in close proximity to each other and to the clock generator ($\Phi_{M<1:16>}$ generated by the DLL) to minimize the sampling clock skew. The ADCs are placed in two rows with sampled signals (by T/Hs) running through the center for the shortest signal connection. The clock paths to the sub-ADCs are spread over the chip with multiple stages of repeaters. Despite the fact that the clock skews in the sub-ADCs are greatly relaxed owing to the sampled signals on the front-end T/Hs, the phase relationship between a T/H and its corresponding sub-ADC is still very important for proper operation. Because there could exist a serious clock delay mismatch between them, this design compensates for the delay mismatch by choosing the best-matched sub-ADC clock via a MUX. For example, sampling clock $\Phi_{M<14>}$ is assigned to the T/H in $SLICE_{14}$, whereas the sampling clock for the sub-ADCs in $SLICE_{14}$, $\Phi_{Md<14>}$, is dedicated to the generation of sub-ADC sampling clocks, $\Phi_{E<14\_1,\ 14\_2,\ 14\_3,\ 14\_4>}$. The 14th T/H samples the input during the period of T_{14_3}, after which the SAR_{14_3}, ideally, then samples the output of the 14th T/H during S_{14_3} with $\Phi_{E<14\_3>}$. However, when $\Phi_{E<14\_3>}$ is delayed from the ideal phase, S_{14_3} overlaps with T_{14_4} and, thus, the SAR_{14_3} samples an incorrect signal near the beginning of T_{14_4}.

For correct operation, in this case, $\Phi_{M<12>}$ instead of $\Phi_{M<14>}$ can be chosen through the MUX for the generation of $\Phi_{E<14\_1,\ 14\_2,\ 14\_3,\ 14\_4>}$. The maximum delay difference between the two paths, to the T/H and to the ADC slice, is estimated to be in the range of 58 ps to 111 ps in various PVT conditions (post-layout simulation). Considering this possible phase mismatch range, the MUX for the delayed $\Phi_{M<k>}$, $\Phi_{Md<k>}$, is designed to have three possible inputs of $\Phi_{M<k-2>}$, $\Phi_{M<k-1>}$ and $\Phi_{M<k>}$.

B. Voltage Domain Phase-Detector (PD) for DLL

As a DLL is utilized to generate the sampling clocks of $\Phi_{M<1:16>}$, it affects the clock skew. PD is one of the key building blocks determining the phase offset in a DLL. Conventional XOR or flip-flop-based PDs are known to have a phase offset ranging from a few ps to several tens of ps, requiring calibration [13]. To improve the accuracy of the PD, we designed a new PD using a voltage-domain dynamic comparator for low input-referred errors by virtue of the high gain, as shown in Fig. 4 (a). It consists of a pair of sampling networks that performs time-to-voltage conversion. CLK_{IN} is the externally given main clock of the ADC, and CLK_{FB} is the feedback clock from the delay cells in the DLL. In order to compare the phases of these two clocks, CLK_{IN} and CLK_{FB} are sampled by CLK_S, which is an inverter-delayed version of CLK_{FB}.

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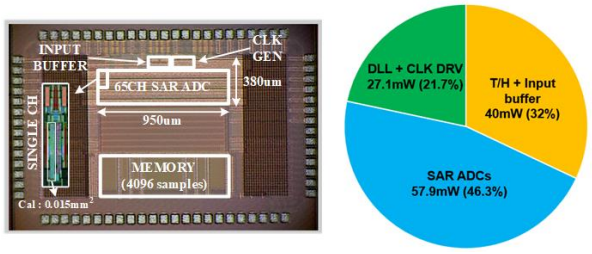
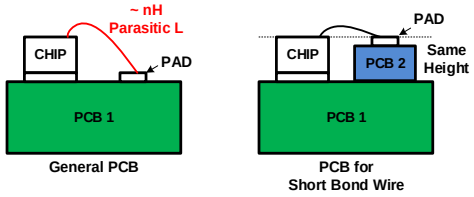
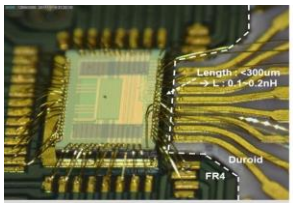


(a) (b)

Fig. 5. (a) Chip micrograph of the TI-SAR ADC. (b) Power breakdown



(a)



(b)

Fig. 6. (a) Hetero structure PCB for reducing parasitic inductance. (b) Bonding micrograph.

The sampled voltage, V_{IN} will vary according to the phase, as shown in Fig. 4 (b). Initially, the charge-pump output, V_C, is reset to VDD, giving the delay cells the shortest delay. In this case, the falling edge of CLK_{FB} arrives sooner than that of CLK_{IN}. Consequently, the sampled voltage V_{FB} is lower than V_{IN}, as CLK_{FB} discharges earlier. When CLK_{FB} must be delayed, the voting logic controls the charge pump with DN = H to reduce V_C. When the falling edge of CLK_{FB} appears later than that of CLK_{IN} (Fig. 4(b)), the magnitude of the relationship of the sampled voltages is reversed, indicating the minimum level of phase error. Once it reaches this point, the comparator output will toggle repeatedly.

The factors that determine the offset of the proposed PD are the offset of the dynamic comparator and the time-to-voltage gain. The time-to-voltage gain is the rate at which the time difference between CLK_{IN} and CLK_{FB} is converted into the voltage difference. In this design, the falling time of the clocks, T_{fall}, is designed to be about 15 ps, as shown in Fig. 4(a), corresponding to a 60mV/ps time-to-voltage gain. The dynamic comparator used in the proposed PD is identical to that of the SAR ADCs. The estimated 3σ offset of the comparator is 27 mV, equivalent to a time skew of 0.45 ps. The effect of this PD offset will be corrected in each sub-ADC by the background skew calibration process, covering the full correction range of 19.2 ps.

V. Measurement Results

A prototype 7-b 32-GS/s TI-ADC was fabricated in a 40-nm CMOS process. Fig. 5(a) shows the chip micrograph. Active area of the ADC is 0.36 mm^2. A custom-designed on-chip memory with 4096 samples capacity is integrated in order to capture the real-time 32 GS/s output data. The on-chip background offset/skew calibration logic (detection and correction) occupies 0.015 mm^2. The input full-scale is 360 mV_{pp_diff}. Under a single 0.95 V supply, the entire TI-ADC including the clock driver consumes 125 mW during operation at 32 GS/s. Fig. 5(b) shows the power breakdown. In this case, 46.3 % of the total power was consumed by the SAR ADCs, 32 % by the T/H + input buffer, and 21.7 % by the DLL and the clock driver. The main clock with an 8 Ts period is applied externally (Agilent E8257D).

In order to minimize the ringing at the input and the clock, the bond-wire inductances were minimized with a specially designed test board in which an RT-Duroid substrate was stacked on a typical FR4 type substrate, as illustrated in Fig. 6

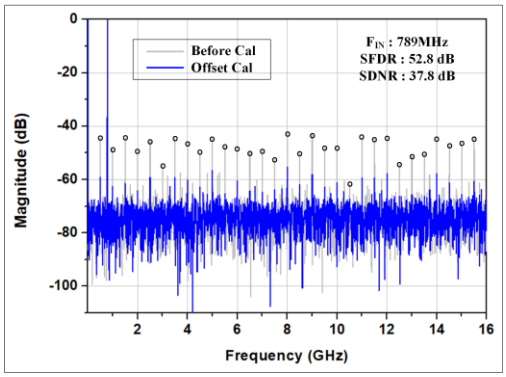


Fig. 7. Measured output spectrum of F_{IN} = 789MHz before and after offset calibration.

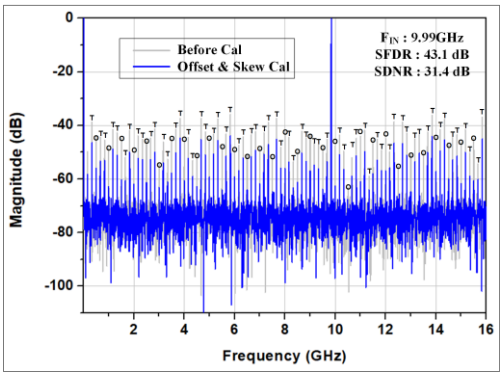


Fig. 8. Measured output spectrum of F_{IN} = 9.99GHz before and after offset & skew calibration.

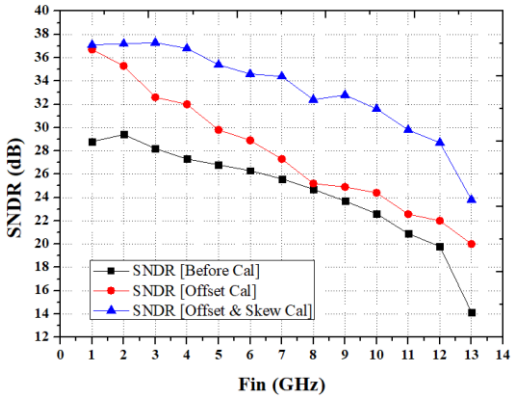


Fig. 9. Measured dynamic performance versus input frequency at 32GS/s sampling frequency.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON (>20GS/S)

	L.Kull ASSCC 2014 [4]	B.Xu VLSI 2016 [15]	S.Cai VLSI 2015 [16]	This Work
Architecture	TI SAR	TI Two-Step	TI Binary	TI SAR
Channel	32	16	8	64
Tech [nm]	32	28	65	40
Power Supply [V]	1/0.9	0.95/0.85	1	0.95
Sampling Rate [GS/s]	36	24	25	32
Resolution [bit]	6	6	6	7
SNDR @ fin,high [dB]	32.1	28.9	29.7	31.4
Area [mm^2]	0.048	0.03	0.24	0.36
$F_{in,high}$ [GHz]	19.9	11.9	12.1	13
Power [mW]	110	23	88	125
FoM [fJ/cs]	88	42	143	126
Calibration Type	OS (BG) SK (UNK)	OS (UNK) SK (BG)	OS (FG) SK (FG)	OS (BG) SK (BG)

S: Offset, SK: Skew

FG: Foreground Calibration, BG: Background Calibration, UNK: Unknown

(a). Because the height of the chip is approximately 300 μm and the thickness of the RT-Duroid board sitting on the FR4 is also about 300 μm, the bond-wires could be as short as 300 μm (Fig. 6(b)) with inductance of around 0.2 nH.

Fig. 7 shows the output spectrums, before and after offset calibration, with a 789 MHz input at FS = 32 GS/s. Before offset calibration, SFDR and SNDR were 38.9 dB and 28.7 dB, respectively, limited by the offset tones. Owing to the calibration, the offset tones are reduced to nearly -60 dB and the SFDR and SNDR are improved to 52.8 dB and 37.8 dB, respectively, corresponding to 4.92 bits in ENOB.

The effect of the skew calibration is shown in Fig. 8. When calibration is disabled, the SFDR and SNDR are 35.4 dB and 22.3 dB, respectively, with an input frequency of 9.99 GHz at F_S = 32 GS/s. After both offset and skew calibrations were enabled, the skew tones were reduced to nearly -50 dB and the SFDR and SNDR were improved to 43.1 dB and 31.4 dB, respectively. Fig. 9 shows the measured SNDR performance versus the input frequencies at F_S = 32 GS/s. At low input frequencies up to 2 GHz, the performance degradation due to the offset mismatch is dominant, and no significant effect by the skew calibration is observed. However, the SNDR drops rapidly due to residual skew with an input signal exceeding 5 GHz; thus, skew calibration is required to improve the SNDR. The residual skew amount, estimated from the measured results, is close to 200 fs [14]. As the skew by the delay cells in $\Phi_{M<1:16>}$ path mainly determine the amount of residual skew and the correction step by skew calibration was estimated to be approximately 153 fs/step from the post-layout simulation, the measurement result shows relatively good agreement with the estimation. Table I provides a performance summary and comparison with prior ADCs with conversion rates in the range of 20-40 GS/s. With background offset and skew calibration implemented on chip, a competitive FoM of 126 fJ/c-s was obtained at 32 GS/s, including the calibration power burden.

VI. CONCLUSION

This brief presents a massively time-interleaved 7-b 32-GS/s SAR ADC with background offset and skew calibration. The dedicated T/H + input buffer and the proposed DLL based on the voltage-domain phase-detector contribute to the reduction of skew down to 200 fs. The proposed clock-delay matching scheme between the T/Hs and the ADCs using a simple MUX could enable robust operation without adding additional jitter to the sampling network.

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