A 2.4-GHz Fractional-N PLL with a PFD/CP Linearization and an Improved CP Circuit

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***Abstract*—this paper reports a PFD/CP linearization technique and a new charge pump circuit to enhance the performance of a delta-sigma (ΔΣ) fractional-N PLL. The proposed method improves the PLL linearity by forcing the PFD/CP to operate in a linear part of its transfer characteristic; while the CP circuit minimizes the current mismatch between the up and down currents by feedback. These circuit techniques are employed in the design of a 2.4-GHz ΔΣ fractional-N PLL. This chip has been fabricated in the TSMC 0.18-μm CMOS process. The experimental results demonstrate that the proposed techniques considerably improve the fractional-N PLL performance. This fully-integrated PLL dissipate 22 mW under a 1.8-V supply.**

I. INTRODUCTION

Fractional-*N* PLLs are employed in many applications. Compared with an integer-*N* PLL, a Fractional-*N* PLL has the benefits of fast locking, fine frequency resolution, and is able to accommodate various reference frequencies. The operation principle of a fractional-*N* PLL lies in dithering the divide ratios to create a fractional divider. The classical fractional-*N* PLL dithers the divide ratio with an accumulator [1]. But it suffers from the appearance of fractional spur and elevated quantization noise caused by the periodical phase error. The problem of periodic phase error may be alleviated by compensating these errors with opposite phase patterns [1]. However, finite matching accuracy limits the effectiveness of such approach.

Other than the classical approach, an alternative is to control the dithering by a ΔΣ modulator. Over-sampling and noise-shaping characteristics of a ΔΣ modulator effectively shape the quantization noise to higher frequencies; hence the low-frequency in-band signal-to-noise ratio (SNR) is improved. However, if non-linearity exists in a ΔΣ fractional-*N* PLL system, the quality of noise shaping is corrupted. The modulated quantization noise will be folded back to lower frequencies, and degrades the SNR. In order to meet the stringent performance requirements, one technique is proposed in this work to improve the circuit linearity.

This paper is organized as follows: in section II, the impact of non-linearity on the design of a ΔΣ fractional-*N* PLL is discussed and is investigated using a phase-domain model. In section III, the proposed techniques are described. The implementation of the 2.4-GHz fractional-*N* PLL is presented in section IV. Finally, measurement results and conclusion are given in section V and VI, respectively.

II. IMPACT OF NON-LINEARITY ON A ΔΣ FRACTIONAL-N PLL

The block diagram of a typical ΔΣ fractional-*N* PLL is depicted in Fig. 1. Fractional division is accomplished by dithering the divide ratio of the feedback multi-modulus divider. However, in this system, highly-linear circuits are required, for non-linearity can severely degrade the phase noise and generate fractional spurs.

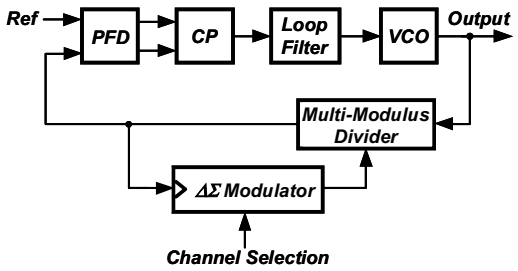

Figure 1. Block diagram of a ΔΣ-modulated fractional-*N* PLL

In a fractional-*N* PLL system, the non-linearity is mainly attributed to the phase-frequency detector and charge pump (PFD/CP) non-linear transfer function, and the jitters accumulated through the frequency dividers [2]. In the PFD/CP circuits, non-linearity is mainly caused by the mismatch between the up/down currents and the gain variation (dead zone) near zero phase error region. To examine the impact on the noise due to the non-linearity, a phase-domain model is devised in Fig. 2(a).

In Fig. 2(a), the ΔΣ modulator output is first subtracted by the fractional number to remove the DC component. The subtractor output represents the frequency fluctuation due to the modulation. The phase fluctuation is obtained by integrating the frequency fluctuation. To see how this model can be used to study the system noise, considering the CP current mismatch. Since the output charge deposited on the loop filter is affected by the CP current variation, the non-linearity from the CP can be represented as a non-linear transfer function after the integrator to model this effect. Fig.

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2(b) and (c) shows the simulation results when 0% and 2% CP current mismatches are applied to this model, respectively. Clearly, the non-linearity considerably raises the in-band phase noise.

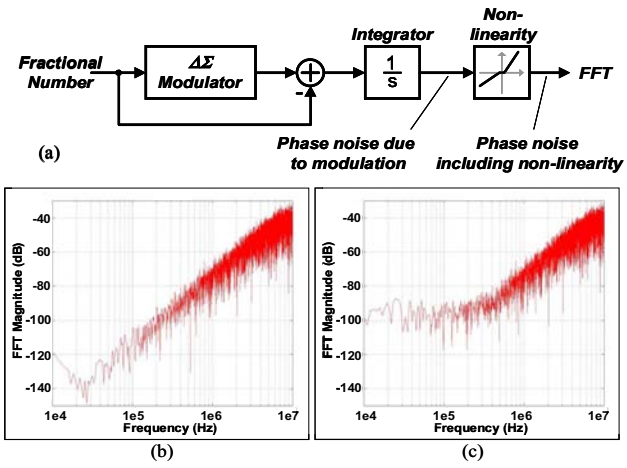

Figure 2. (a) Phase-domain model; (b) simulated phase noise at divider output with matched CP up/down currents; (c) with 2% current mismatch.

III. Linearity Enhancement Techniques

In this section, the proposed CP circuit and the PFD/CP linearization technique are described.

A. Charge Pump with Feedback

Charge pump up/down current mismatch is a major source of non-linearity in a ΔΣ fractional-*N* PLL. Conventionally, long-channel devices are employed to alleviate the channel-length modulation effect and improve the current matching accuracy [3]. However, the channel width must be scaled proportionally to maintain a low overdrive voltage. Hence, large transistors are used in the CP. Large devices not only occupy larger chip area, but also slow the circuit transient response and require large switch buffers, which can greatly degrade the circuit noise performance. Here, a novel CP architecture is proposed in Fig. 3(a). Compare with a conventional CP, two additional feedback transistors, M_{fbN} and M_{fbP}, are added to the circuit. The main idea is to incorporate feedback to a small-sized CP, to achieve the good current matching of a large-sized one for area efficiency and minimizing unwanted transient effect.

The circuit operates as follows: when the output voltage rises, the down current (I_{dn}) increases while the up current (I_{up}) decreases, owing to the channel-length modulation phenomenon. As the voltage increases further, transistor M_{fbN} enters deep triode region eventually. The lowered device on-resistance reduces the amount of current mirrored to the output down current branch; hence it reduces the difference between I_{up} and I_{dn}. Similarly, if the CP output voltage decreases, transistor M_{fbP} enters the triode region. The lowered device on-resistance reduces the current mirrored to the output up current branch, and improves the up/down current matching. The proposed CP circuit adjusts the bias condition of the feedback transistors, M_{fbN} and M_{fbP}, and dynamically balances the I_{up} and I_{dn}. Note that the proposed CP circuit only required two additional devices; therefore, this technique is quite area-efficient. Fig. 3(b) and (c) show the simulated results with and without feedback, respectively. When the feedback is applied, the I_{up}/I_{dn} current mismatch reduces significantly. The proposed CP improves the current matching without employing an opamp to regulate the currents; hence this circuit is area efficient and is less noisy.

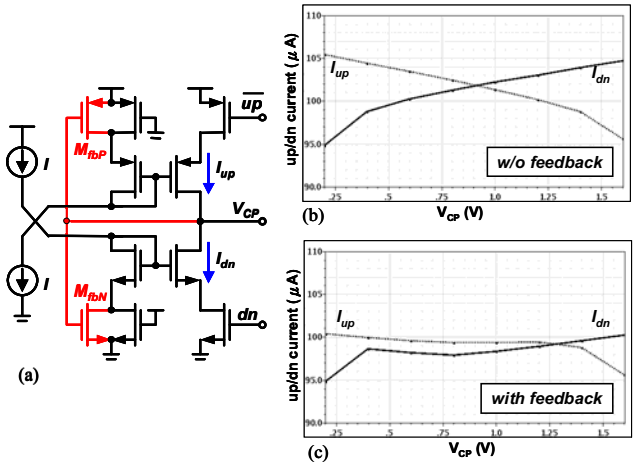

Figure 3. (a) Proposed CP circuit with feedback; (b) simulated up/down current without feedback, (c) with feedback.

B. Linearization Priciple

The PFD/CP (Fig. 4(a)) introduces non-linearity. A typical fractional-*N* PLL operates at a region around zero phase error ($\Delta\phi$) when the loop is settled. Unfortunately, the linearity near the center is often the worst. If the operation region can be shifted to a linear part of the transfer curve, as illustrated in Fig. 4(b), the system non-linearity can be improved. One way to realize the shifting operation is to add a DC offset current at the CP output [2], which moves the PFD/CP operation to a linear region.

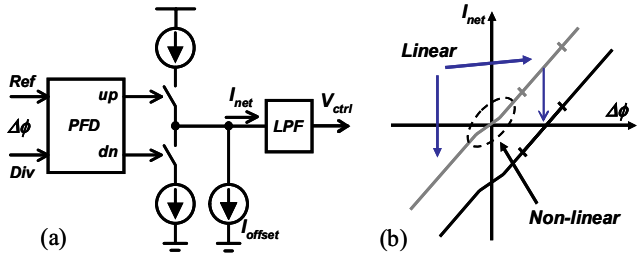

Figure 4. (a) PFD/CP linearized by adding an offset current at CP output; (b) illustration of shifting the PFD/CP transfer curve.

C. Proposed PFD Linearization Technique

The above principle is effective in improving the PLL linearity. However, adding an active circuit at the CP output directly injects extra noise to the loop filter, and may even

alter the loop characteristic [4]. In this work, a technique is proposed to accomplish the shifting operation without adding the current source. This is achieved within the PFD circuit, rather than on the CP.

In Fig. 5(a), an extra delay τ is added to the *dn* reset path. This added delay forces the CP discharging current to remain "on" for an extra duration τ, as shown in the timing diagram of Fig. 5(b). This is equivalent to adding a "gated" offset current to the PFD/CP, only without using the actual current source. Therefore, same linearization effect as adding an offset current (see Fig. 4(a)) is realized.

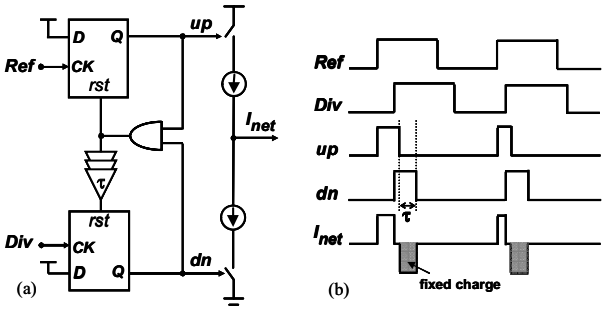

Figure 5. (a) PFD/CP linearization by adding an unbalanced reset delay (τ) in the PFD; (b) the corresponding timing diagram.

One issue with this method is that a non-zero average phase error exists between *Ref* and *Div* when the PLL is locked. Hence, the reference spurs increases. Fortunately, this is typically not a major concern, since the reference frequency is much higher than the PLL bandwidth, and the high-order loop can effectively suppress the reference spurs.

IV. Implemetation of The ΔΣ Fractional-N PLL

The proposed techniques are employed in the design of a 2.4-GHz ΔΣ fractional-*N* PLL. The simplified PLL block diagram is shown in Fig. 1. PFD and CP are discussed in the previous section. Other key building blocks of the PLL are described in this section.

A. Multi-Modulus Divider (MMD) & ΔΣ Modulator

Fig. 6 shows the block diagram of the MMD, which is comprised of seven divide-by-2/3 stages [5, 6]. The MMD can support a division range from 64 to 255. In such an asynchronous divider structure, the jitter introduced in each stage accumulates and raises the output phase noise. Furthermore, the jitter degrades the system linearity and causes additional noise folding. An effective way to reduce jitter is to resynchronize the MMD output with a cleaner source signal, e.g. VCO signal.

Directly re-synchronizing to the high-frequency VCO signal (at 2.4 GHz) can be challenging, for the long propagation delay across the delay stages will exceed one VCO cycle. In this MMD, the toggle signal (TG_1) of the first divide-by-2/3 stage is taken as the MMD output, since it appears once in every output cycle periodically. This signal experiences small propagation delay from the input; hence, it is suitable for a high-speed re-timing operation (by DFF_1). The following 2 flip-flops (DFF_2 and DFF_3) are added to ensure this strobe-based output signal has an adequate pulse width to drive the following PFD circuit.

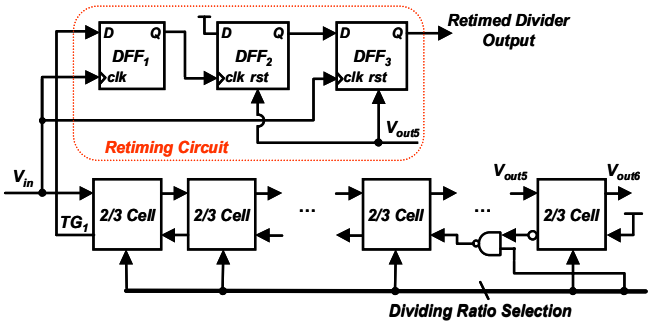

Figure 6. Block diagram of the MMD with retiming.

The ΔΣ modulator that controls the MMD dividing ratio adopts the MASH-111 structure, for it can accommodate a wide-range input and is always stable. A passive 3-order loop filter is integrated on-chip to suppress the shaped modulation noise.

B. Voltage-Controlled Oscilattor (VCO)

The VCO adopts a P-core topology with a tail current source (Fig. 7). A 4-bit capacitor tuning array is employed to cover a wide tuning range, while maintains a low VCO frequency tuning gain (K_{vco}). A small K_{vco} is beneficial in achieving low phase noise and spurs. The varactors employ the accumulator-depletion structure. A DC voltage, V_{DC} (at half V_{DD}) is applied to bias the varactor and shift its operation region to around the middle of the available CP output voltage range.

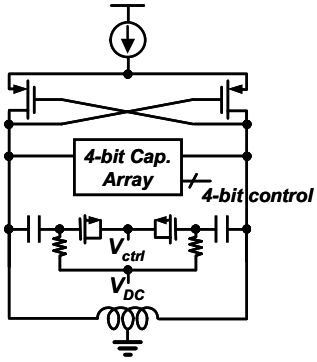

Figure 7. VCO circuit

V. Experimental Results

The 2.4-GHz ΔΣ fractional-*N* PLL including the proposed techniques are fabricated in the TSMC 0.18-μm CMOS process. This fully-integrated PLL occupies an area of 1.5 mm by 1.5 mm. This chip consumed 22 mW from a 1.8-V

supply voltage. The PLL reference frequency is chosen to be 20 MHz. Fig. 8 shows the measured output spectra with the proposed PFD/CP linearization method enabled/disabled. As an extra reset delay (τ) of around 6 ns are enabled, the PLL output spectrum is considerably improved. This illustrates the effectiveness of the proposed technique. However, the reference spurs increased (to -39 dBc) as a result of the offset operation. The amount of phase noise improvement and spur degradation can be balanced by a proper choice of the delay time τ.

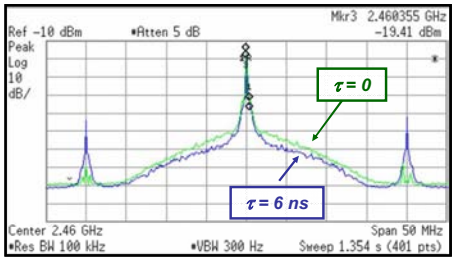

Figure 8. PLL output spectra with and without the proposed PFD/CP linearization scheme.

The measured output phase noise results when the PLL is configured to an integer channel and a fractional channel are both shown in Fig. 9. The plot shows that the in-band phase noises are about the same in both cases. This indicates that the fractional-*N* PLL is quite linear; hence the noise folding phenomenon (due to non-linearity) does not occur. The chip micrograph is shown in Fig. 10. Finally, Table I summaries the experimental results of the proposed fractional-*N* PLL.

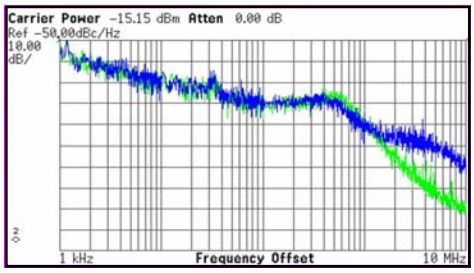

Figure 9. Measured PLL phase noise for both the fractional and integer channels.

VI. Conclusions

In this paper, a novel CP circuit and a PFD/CP linearization technique are proposed to improve the performance of a fractional-*N* PLL. The CP incorporates two feedback devices to compensate for the channel-length modulation effect. The proposed CP improves the up/down current matching without using large current source devices; hence, also improving the circuit transient behavior. Furthermore, by simply adding an extra delay to one of the PFD reset paths, the PFD/CP operation is shifted to a linear region, avoiding the dead-zone and other non-linearity. These techniques are successfully demonstrated in a fully-integrated, 2.4-GHz $\Delta\Sigma$ fractional-*N* PLL.

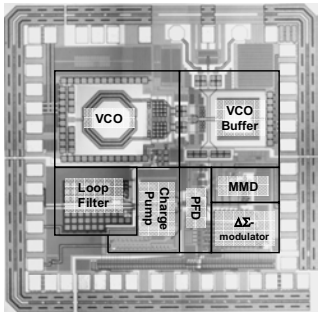

Figure 10. Chip photo

TABLE I. Performance Summary

Technology	TSMC 0.18-µm CMOS
Supply Voltage	1.8 V
Frequency Range	2.2 GHz ~ 2.6 GHz
PLL Phase Noise	-81 dBc/Hz @ 100 kHz
Frequency Resolution	4.88 kHz (12-bit $\Delta\Sigma$)
Loop Bandwidth	400 kHz
Reference Spur	-39 dBc
Power Consumption	22 mW
Chip Size	1.5 mm x 1.5 mm

Acknowledgment

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