A 0.076 mm^2 12 b 26.5 mW 600 MS/s 4-Way Interleaved Subranging SAR-$\Delta\Sigma$ ADC With On-Chip Buffer in 28 nm CMOS

Alessandro Venca, Nicola Ghittori, Alessandro Bosi, and Claudio Nani, *Member, IEEE*

***Abstract*— A 0.076 mm^2 12b 28 nm 600 MS/s 4-way time interleaved ADC with on chip buffer is presented. The usage of a subranging scheme consisting of a coarse SAR ADC followed by an incremental $\Delta\Sigma$ fine converter provides better suppression of thermal noise added during conversion for a given power compared to a conventional SAR. The ADC area has been optimized by using a segmented charge-sharing charge-redistribution DAC. The prototype achieves an SNDR of 60.7 dB and 58 dB at low and high frequency, respectively, while consuming 26 mW.**

***Index Terms*— Analog-to-digital converter (ADC), Delta sigma converter, SAR, successive approximation.**

I. Introduction

INTEGRATION of low-power and area-efficient ADCs is a key differentiator in modern mixed-signal SoCs in both consumer and industrial applications. The increasing adoption of software radio like approaches for the design of wireline communication receivers calls for medium to high resolution ADCs with both high sampling rate and extremely low power consumption [1], [2]. At the same time, other emerging wireline standards like the G.hn Gen 2 [3] that employ MIMO strategies often require the integration of a large number of wide bandwidth analog front ends that must be low-power *and* extremely area-efficient. In order to address these requirements, wide-bandwidth high-resolution ADCs with both high power efficiency and extremely small area are of primary importance. Given the large number of channels integrated in the SoC, the usage of off-chip components should be minimized in order to reduce the Bill of Materials (BoM).

In scaled technologies, power challenges have been addressed using SAR architectures, often in combination with techniques like redundancy, asynchronous operation, and time interleaving to meet the application sampling rate requirements. However, for high-resolution ADCs (9b+ENOB), a traditional SAR is intrinsically energy-inefficient since it reuses the same low-noise comparator to perform both coarse conversions (where little accuracy is needed) and fine conversions (where thermal noise is of paramount importance) [8].

In recent literature, this challenge is addressed by combining SAR with different conversion techniques like, averaging [4], noise shaping with oversampling [5] [7], single slope [6], and pipelining. The strategy is a divide et impera approach where different conversion techniques are combined in a single design and each of them is used in a resolution and signal amplitude range where it performs at its maximum power efficiency. For high-resolution and medium-sampling rates converters, excellent power efficiency figures have been achieved with hybrid SAR-pipeline architectures [8], [9] that employ SAR as subADCs, but whose noise performance is determined by a high-efficiency interstage amplifier as opposed to the comparator.

SAR area has also been greatly reduced in recent years with the introduction of digital DAC linearity calibrations [12] that relax matching requirements, allowing scaling down the SAR DAC capacitance to the kT/C limit. In noise-limited ADCs, for every extra bit of resolution, the sampling and DAC capacitance grows $4\times$ while, at the same time, the ripple on the converter reference voltage has to be reduced $2\times$ to preserve linearity. Such a trend sets very tough requirements for the reference generator of high resolution charge-redistribution DAC (CR-DAC) SAR ADCs, especially when no external components can be used, hence requiring the integration of very large on-chip capacitors [9]. Another approach to address this issue in literature is using DAC switching schemes that optimize the current drawn from the reference [8], [9] or with DAC topologies more immune to reference ripple, like current-steering [10] or charge-sharing DACs (CS-DAC) [11].

In this paper, a 12 b 4-way interleaved 600 MS/s ADC with on-chip input signal and reference buffer is presented. The energy efficiency challenge is addressed with a subrange scheme that employs a SAR as a coarse ADC and an incremental Delta–Sigma as a fine ADC, while drastic area reduction is achieved with a segmented charge-sharing charge-redistribution DAC architecture. The converter delivers 58 dB SNDR at Nyquist for 26.5 mW of power with a total area of only 0.076 mm^2 and does not require any external component.

Sections II and III discuss the thermal noise performance of incremental $\Delta\Sigma$ ADCs and compare it with SAR. The subrange SAR-$\Delta\Sigma$ ADC architecture is then introduced in Sections IV and V. Section VI reviews the requirements for the reference generator of high-resolution charge-redistribution DAC and introduces the segmented charge-sharing charge-redistribution DAC architecture. The overall ADC architecture and calibrations are presented in Section VII while in Section VIII the circuit-level implementation is presented.

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The authors are with Marvell Italia s.r.l., Pavia 27100, Italy.

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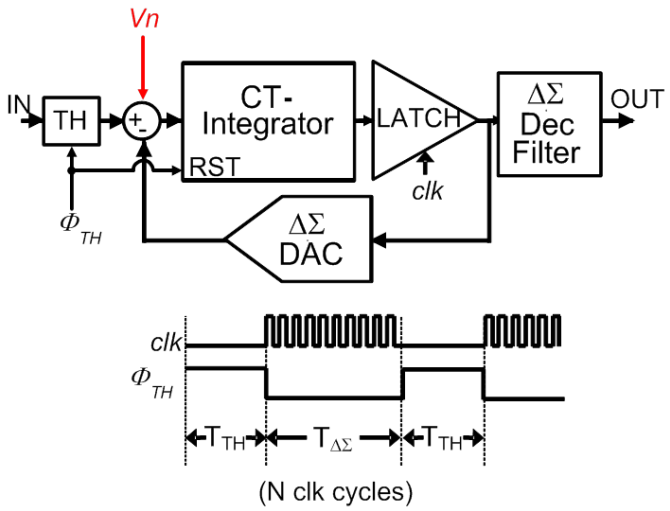


Fig. 1. Incremental ΔΣ converter block diagram and timing.

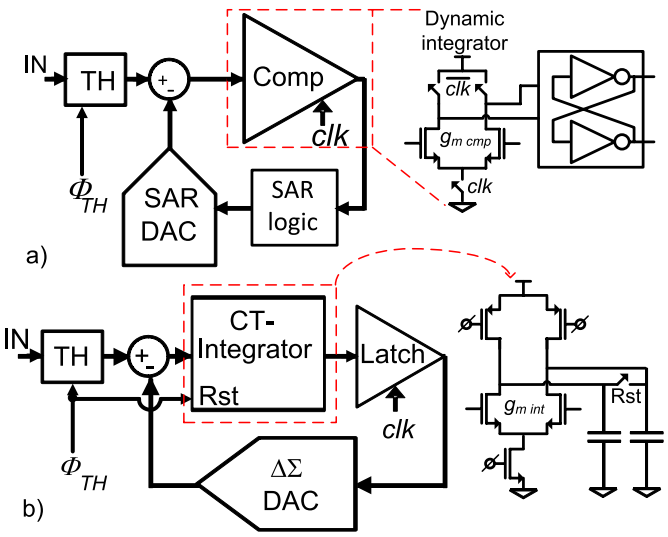


Fig. 2. (a) SAR and (b) first-order ΔΣ ADC block diagrams and circuit-level implementations of the blocks considered as main contributors to noise–power performance.

Section IX presents the measurements results, and conclusions are drawn in Section X.

II. Thermal Noise Filtering in Incremental ΔΣ ADCs

Incremental ΔΣ ADCs [14], [15] are a class of A/D converters often used in instrumentation and measurement applications [13]. The basic block diagram of this converter is shown in Fig. 1. It consists of a T/H stage followed by a ΔΣ modulator whose internal state can be reset. After the sampling phase, the input signal is held constant at the input of the ΔΣ modulator and it is converted for N clock cycles ($NT_{clk} = T_{\Delta\Sigma}$). At the end of conversion, the state of the ΔΣ modulator, that is the loop filter capacitances, is reset and the N samples output sequence is then filtered using an FIR filter and decimated by N.

A very interesting property of continuous time (CT) incremental ΔΣ modulators is their behavior with respect to thermal noise added at the modulator inputs, mainly ascribed to DAC and loop filter integrators (V_n in Fig. 1). Unlike the input signal, this noise source is not sampled and therefore is filtered by the CT-ΔΣ modulator signal transfer function and appears at the quantizer output. The digital FIR decimation filter then suppresses the out of band noise before the final decimation. By assuming a white Gaussian input thermal noise power spectral density S_{Vn}, the final output noise power is given by the following expression:

$$P_n = \int_0^{fclk/2} S_{Vn}\,|H_{FIR}(f)|^2 \cong S_{Vn} B w_n \text{with } B w_n = \frac{\sum_{i=1}^{N} c_i^2}{2T_{clk}} = \frac{1}{\varphi T_{\Delta\Sigma}} \quad (1)$$

where $H_{FIR}(f)$ is the FIR frequency response and Bw_n is the equivalent analog noise bandwidth of the FIR filter. The φ parameter depends on the actual FIR filter coefficients and it can be proven that it is maximized ($\varphi = 2$) when all of the FIR coefficients are equal (dumped integrator). If we implement the loop filter using a simple open-loop integrator (first-order ΔΣ modulator), this result is similar to the one in [8]. However, in the approach proposed in this paper, the integrator, being inside a ΔΣ loop, does not need gain calibration nor stringent linearity performance.

In practical implementations, however, the total output noise of the incremental ΔΣ converter contains also other noise components (e.g., quantization noise and thermal noise from the quantizer latches) which are high-pass frequency-shaped according to the modulator order. This requires a design optimization of the FIR filter coefficients to provide better suppression of high-frequency noise components at the cost of an increased filter equivalent analog bandwidth ($\varphi < 2$).

III. Incremental ΔΣ and SAR Converter Thermal Noise Comparison

In order to compare the incremental ΔΣ and SAR thermal noise performance we consider the ΔΣ integrator and the SAR dynamic comparator as only noise (and power) limiting blocks for the two architectures (see Fig. 2). The latter is usually implemented as a dynamic integrator followed by a CMOS latch (see Fig. 2(a)) and its input referred thermal noise is dominated by the contribution of the input differential pair that can be written [16] as

$$P_{N_{SAR}} = S_{Vn} B w_n \cong \frac{8kT\gamma}{g_{mcmp}} \frac{1}{2T_{int}} \quad (2)$$

where T_{int} is the duration of the dynamic integrator integration phase. If a simple open-loop integrator is used in an incremental ΔΣ ADC (assuming no linearity constraints; see Fig. 2(b)), the resulting noise power using (1) is

$$P_n = S_{Vn} B w_n \cong \frac{8kT\gamma}{g_{mint}} \frac{1}{\varphi T_{\Delta\Sigma}}. \quad (3)$$

Equations (2) and (3) have very similar structure and show that, for both architectures, the thermal noise is proportional

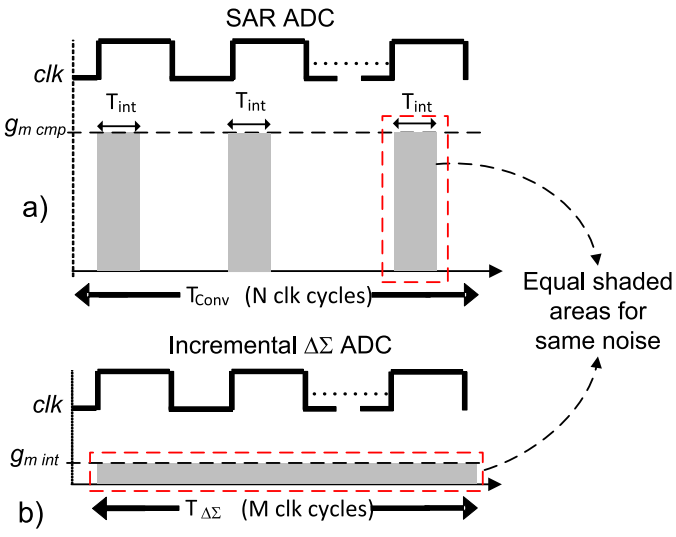


Fig. 3. Timing diagram with highlighted when the g_m is used to suppress thermal noise (a) for SAR ADC and (b) for a first-order ΔΣ ADC.

to the inverse of the product g_mT. If we assume the same input pair overdrive (V_{ov}), the product $g_mT = 2I_d/V_{ov}T$ is proportional to the total charge drawn by the integrators.

While in an incremental ΔΣ ADC this charge ($g_{mint}T_{\Delta\Sigma}$) is drawn only once during the complete ΔΣ conversion time ($T_{\Delta\Sigma}$; see Fig. 3(b)), in a SAR approximately the same charge ($g_{mcmp}T_{int}$) must be drawn every time the comparator is activated (see Fig. 3(a)). That means that, in a N bit SAR converter, the total charge drawn by the SAR comparator is N times the one used by an incremental ΔΣ integrator for the same level of thermal noise. In redundant SAR [17], the comparator power and noise can be optimized during conversion but also in this case more than one conversion cycle with the final comparator noise level are required when the quantization noise approaches the comparator thermal noise.

IV. SAR-ΔΣ Subrange ADC Architecture

While CT-incremental ΔΣ converters are very efficient in mitigating the thermal noise components from the loop filter integrators, their key weakness is the large oversampling ratio, that is, number of clock cycles required to bring quantization noise to the target level. This challenge is addressed in this design with a subrange scheme that employs a SAR as coarse ADC and a Delta-Sigma as fine ADC. The block diagram of the ADC architecture is shown in Fig. 4.

By resolving a significant number of bits using the coarse SAR algorithm, the number of clock cycles required by ΔΣ-sub-ADC to get to the target final resolution can be reduced drastically. In our implementation, the coarse nonbinary SAR ADC provides 9 b of equivalent resolution and the fine ADC (ΔΣ-sub-ADC) implemented as 1-bit first-order CT incremental ΔΣ ADC resolves the remaining 3 b to get to the final 12 b resolution. A 1 b overrange is added between the coarse SAR ADC and the ΔΣ-sub-ADC in order to correct for the coarse SAR ADC error induced by the SAR loop thermal noise leading to a final ΔΣ-sub-ADC resolution of 4 b after filtering and decimation.

The operation phases are shown in Fig. 4. After the sampling and the coarse SAR conversion phase (10 clock cycles), the SAR residual error is converted by the fine ΔΣ-sub-ADC in 8 clock cycles. The 8 ΔΣ-sub-ADC comparator decisions are filtered using an 8-taps low-pass FIR filter and decimated by 8 before being recombined with the SAR output to get a 12 b final code.

Once the ΔΣ-sub-ADC and coarse SAR output are recombined the only residual noise is the sampling kT/C noise and the ΔΣ-sub-ADC noise, i.e. ΔΣ quantization noise, latch thermal-noise, and loop filter thermal-noise. All of these components are low-pass filtered by the ΔΣ-sub-ADC FIR filter with the equivalent bandwidth of the FIR (approx $1/\varphi T_{\Delta\Sigma}$ where $T_{\Delta\Sigma}$ is the ΔΣ-sub-ADC conversion time) as shown in Section II. Since both quantization and latch thermal noise are first-order shaped, they are strongly suppressed by the FIR leaving as dominant terms the sampling (kT/C) noise and the input-referred noise of the ΔΣ integrator (with integration time $T_{\Delta\Sigma}$). Artifacts due to first-order shaping are dithered by the thermal noise added by the latch.

ΔΣ-sub-ADC is implemented with minimum hardware overhead by merging ΔΣ-DAC with SAR-DAC and reusing the comparator latch. Reconfiguring the SAR comparator static preamp-stage (G_{mint}) into the ΔΣ integrator only requires stopping the reset of its load capacitor (C_{int}) after the last SAR cycle as shown in Fig. 5. All timing signals required for the conversion are generated internally using a self-timed loop approach [18]. While during SAR conversion the duration of each conversion cycle depends on the actual comparator decision time, during the ΔΣ phase, a fixed time is allocated to comparator decision in order to minimize jitter on the internal clock. The FIR filter frequency response has been designed in order to maximize the final ADC ENOB performance in presence of all the sources of thermal noise as well as quantization noise. The resulting filter shows a φ factor of approximately 1.8. Given the limited number of ΔΣ-sub-ADC conversion cycles, the digital FIR filter can be implemented in a simple direct form as weighted sum of the 8 ΔΣ-sub-ADC comparator decisions.

V. SAR-ΔΣ ADC Noise Contributors

The main driving reason in choosing a first-order incremental ΔΣ is that it offers the opportunity for a minimum HW overhead reconfiguration between the SAR and ΔΣ phase.

A consequence of this choice is that the transconductance of the resetting-integrator in the SAR phase and of the loop integrator in the ΔΣ phase are the same. The transconductance is designed to have a 3σ thermal noise to be less than the coarse LSB (LSB_{SAR}) to guarantee the SAR noise (quantization + thermal) to be within the input range of the fine ΔΣ ADC. The integrator thermal noise power at the output of the ΔΣ can then be derived from (2) and (3) as

$$P_n = P_{N_{SAR}} \cdot \frac{2T_{int}}{\varphi T_{\Delta\Sigma}} \tag{4}$$

where it can be easily appreciated the suppression of the integrator thermal noise since $T_{\Delta\Sigma} = N \cdot T_{CLK}$ where N is

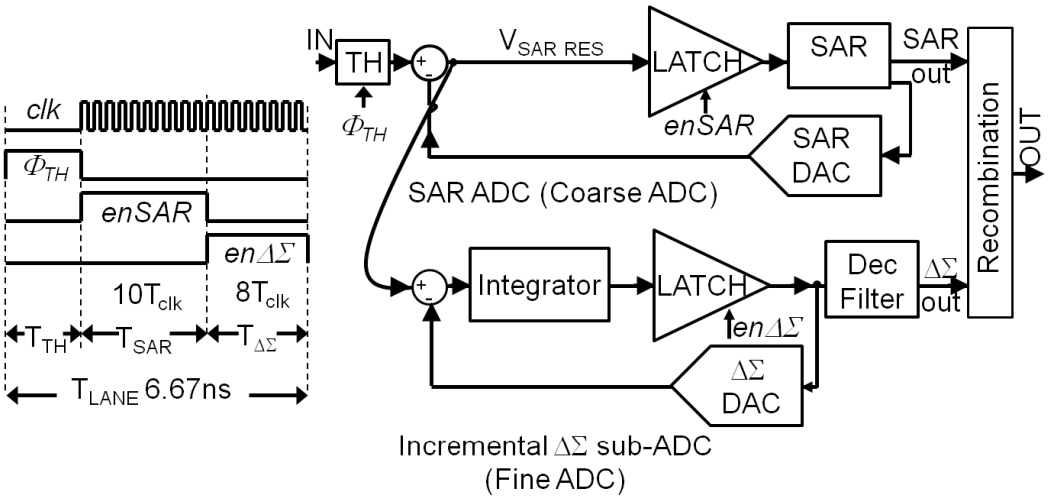


Fig. 4. SAR-$\Delta\Sigma$ subrange lane ADC conceptual block diagram and timing.

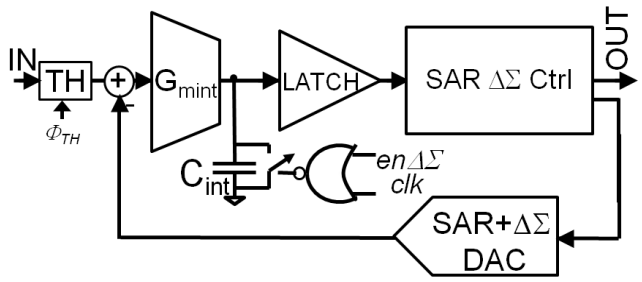


Fig. 5. SAR-$\Delta\Sigma$ subrange lane ADC minimum hardware overhead implementation.

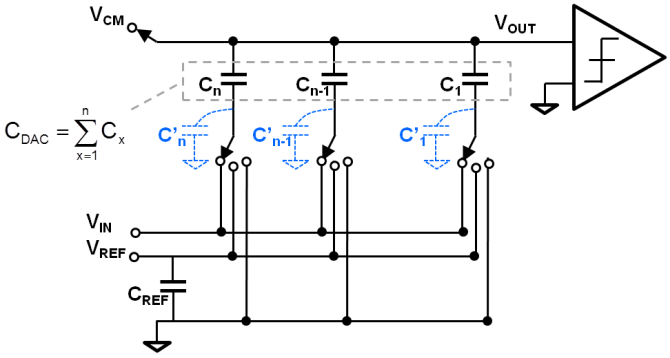


Fig. 6. Single-ended charge-redistribution DAC (CR-DAC) shown in track mode.

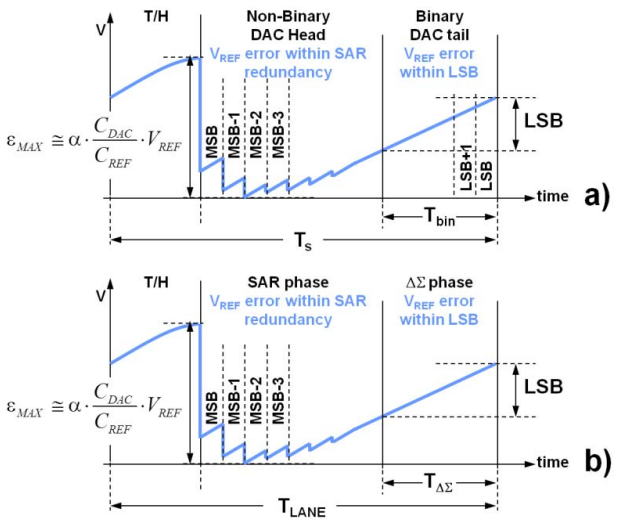


Fig. 7. Qualitative reference voltage ripple ripple (a) in a nonbinary CR-DAC and (b) in a nonbinary SAR-$\Delta\Sigma$ architecture using a CR-DAC.

the number of $\Delta\Sigma$ clock cycles whereas T_{int} is a fraction of T_{CLK}.

Since a first-order $\Delta\Sigma$ suppresses the quantization noise with the inverse of the oversampling (OSR $= T_{\Delta\Sigma}/T_{CLK}$) at the power of 3 it can be calculated that a first-order modulator is enough to suppress the quantization noise in $N = 8$ $\Delta\Sigma$ cycles to roughly the same level as the thermal noise. The result of this analysis matches well with the simulated noise contributions (cf. Fig. 16).

VI. Segmented Charge-Sharing Charge-Redistribution SAR-DAC

The D/A converter of SAR ADCs is commonly a capacitive-based topology due to the inherent high matching of metal capacitors in deep-submicron technology. Among capacitive-based DAC topologies, the charge-redistribution DAC (CR-DAC) (Fig. 6) [19] is extensively used mainly for its small area. Since the DAC switches are on the bottom plate (the side opposite to the comparator), the CR-DAC is inherently insensitive to switch parasitics (C'_n, $C'_{n-1,\ldots,}C'_1$), since these undesired capacitances are always connected to the reference generator. This property allows scaling down the DAC capacitance eventually to the kT/C noise limit and it represents the main reason for the small area achieved by the CR-DAC topology.

A key limitation of CR-DAC is that it requires a very accurate reference voltage not to impact the linearity performances. In a CR-DAC, in fact, the reference voltages are connected through the DAC switches and capacitors to the comparator inputs during the SAR phase of the ADC. The transfer function from the reference voltage node to the input of the comparator is not linearly code dependent, ranging from a unity transfer function when the DAC has all of the capacitors connected between the comparator input node and

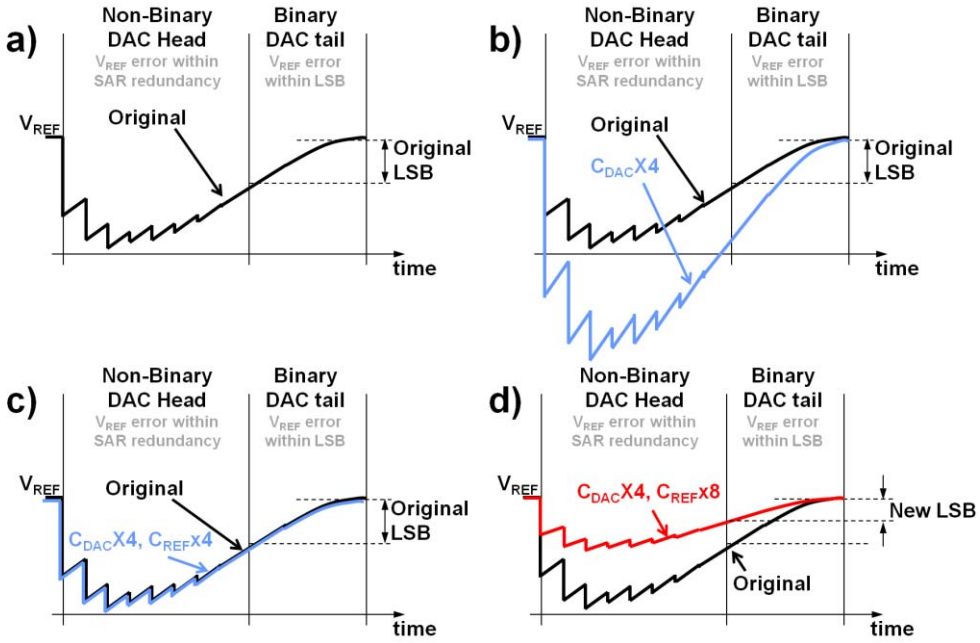


Fig. 8. Reference ripple and requirement on C_{REF} for one additional bit of resolution (T/H phase omitted to simplify the visualization). (a) Original ripple (black). (b) Ripple (blue) with C_{DAC} increased four times to meet kT/C requirements. (c) Ripple (blue) with C_{REF} increased by four to obtain the original ripple. (d) Ripple (red) with C_{REF} increased by 8 to meet linearity requirements.

the reference voltage to virtually infinite attenuation when the DAC has all of the capacitors connected between the comparator input node and the ground voltage. Therefore, ripples on the reference voltage greater than 1 LSB during the SAR phase can cause errors in the comparator decisions that if not corrected may produce distortion in the converted signal. Moreover, the net charge absorbed by the reference generator during one conversion, due to the switching of the DAC capacitors, is not linearly code-dependent as well, as described in [19]. The net switching charge per conversion is absorbed by the finite impedance of the reference generator and produces a low frequency code-dependent voltage ripple with a major spectral component at the ADC input signal second harmonic (in differential structures). This ripple, when mixed with the input signal fundamental, produces a third harmonic at the ADC output.

The two nonlinear mechanisms discussed above translate into very tough requirements for the reference generator of high-resolution charge-redistribution SAR ADC. To mitigate the effects of the non-linear reference-to-comparator transfer function a large decoupling capacitance is usually required to reduce the high-frequency ripple while low output peak impedance of the reference buffer is needed to attenuate the effects of the low-frequency nonlinear current drawn from the references by the switching DAC activity.

In a SAR ADC using binary weighted CR-DAC, the reference voltage is required to settle within 1 LSB accuracy at every conversion cycle. Non-Binary weighted CR-DAC implementations tolerate larger reference errors in the redundant part of the DAC, but still they require 1LSB settling accuracy during the last few conversion cycles where errors cannot be recovered by redundancy. The requirements on the reference voltage accuracy in a generic non-binary CR-DAC can be evaluated from Fig. 7(a) where the reference voltage ripple is sketched in steady state (ripple recovered within T_S). In this qualitative example, the reference generator has a bandwidth much smaller than the ADC conversion frequency f_S and the decoupling capacitance is equal to C_{REF}. In this condition, by approximating the ripple peak amplitude generated by the first few MSB transitions as $\varepsilon_{MAX} = \alpha C_{DAC}/C_{REF}$and assuming a linear reference voltage recovery the required C_{REF} can be estimated as

$$C_{REF} \geq \alpha \cdot \frac{T_{bin}}{T_S} \cdot 2^{N-1} \cdot C_{DAC} \tag{5}$$

where C_{DAC} is the total DAC capacitance and the factor α takes into account for the switching scheme adopted in the DAC. In the literature, several CR-DAC switching schemes have been presented aimed to reduce the current drawn from the reference and therefore also the associated reference voltage ripple. With the merged capacitor switching scheme proposed in [20], for example, the factor α can drop to 0.25 with minor implementation drawbacks, while a more aggressive scheme like in [21] reduces further the factor α but results in a code-dependent DAC output common mode.

In the case of a noise-limited charge-redistribution SAR ADC, it is interesting to analyze the scaling of the size of the C_{REF} as the required resolution increases, by using (5). In Fig. 8, it is shown an example for 1 bit of additional resolution requirement. Here, the C_{DAC} has been multiplied by a factor 4 to meet the kT/C noise requirement Fig. 8(b). To recover the original ripple the C_{REF} must be increased by a factor 4 as well [Fig. 8(c)]. However since the new LSB is half the original one (N is increased by 1), to preserve the linearity specification, the ripple must be reduced by another factor 2, hence requiring C_{REF} to be multiplied by

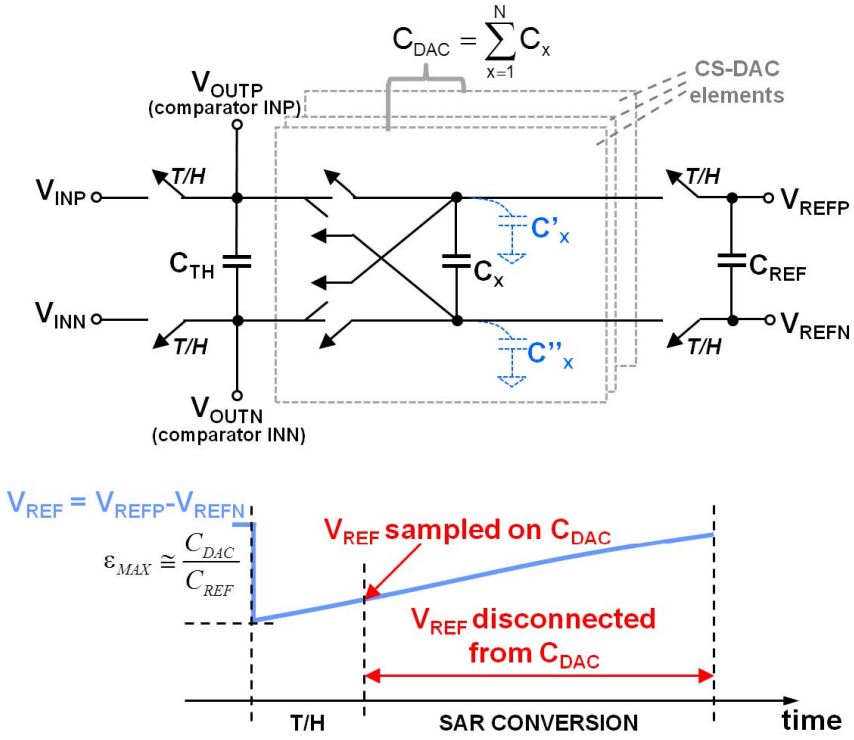


Fig. 9. CS-DAC and T/H.

a factor 8 [Fig. 8(d)]. As a consequence of that, in a noise-limited charge-redistribution SAR ADC, as the resolution increases, the size of the reference capacitance grows with double rate with respect to its core DAC capacitance eventually becoming the main integrated area contributor for resolutions beyond 9/10 b ENOB.

For the specific case of the 12 b SAR-$\Delta\Sigma$ architecture using a CR-DAC, the reference ripple can be tolerated to a certain extent in the SAR phase thanks to the DAC redundancy and to the $\Delta\Sigma$ overrange but during the fine $\Delta\Sigma$ phase the reference error must be kept within 1 LSB as in a non-binary-weighted SAR ADC (Fig. 7(b)). The required C_{REF} can be then calculated using (5) as

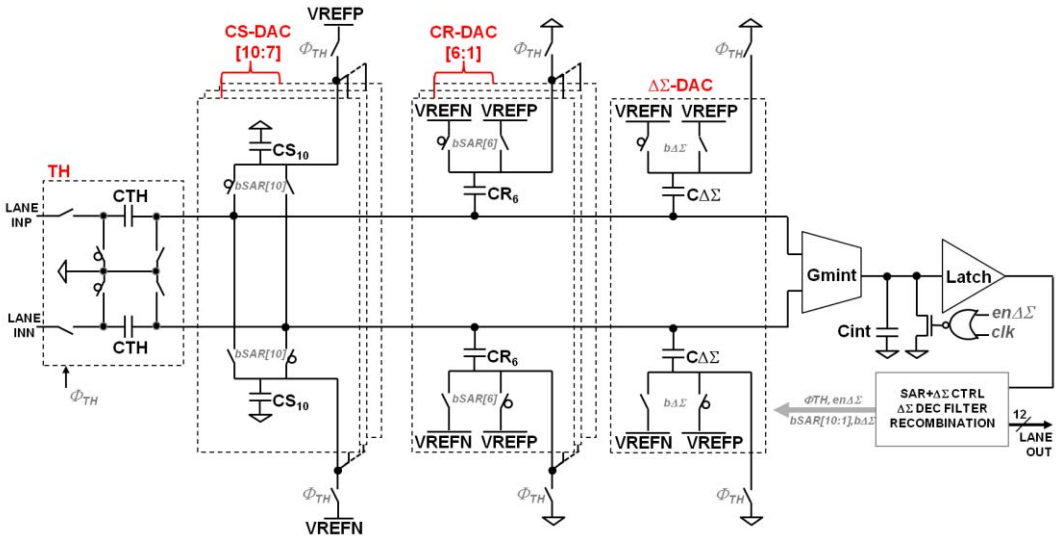
$$C_{REF} \geq \alpha \cdot \frac{T_{\Delta\Sigma}}{T_{LANE}} \cdot 2^{N-1} \cdot C_{DAC} \cong 50\text{pF} \qquad (6)$$

where $N = 12$, $C_{DAC} = 300$ fF, $\alpha = 0.25$, $T_{\Delta\Sigma} = 2.22$ ns, and $T_{LANE} = 6.66$ ns. Integrating such a capacitance would clearly result in exceeding the area budget of the project and led us to explore alternative DAC architectures.

The charge-sharing DAC (CS-DAC) has been introduced in [11] as an effective way to reduce the area of the reference generator. A CS-DAC is depicted in Fig. 9 together with the T/H capacitance on which the input signal is sampled at the end of the T/H phase. Simultaneously, the reference voltage V_{REF} is sampled on C_{DAC}. After sampling, the V_{REF} is disconnected from C_{DAC} for the entire SAR conversion phase. In this way, the comparator decisions are virtually insensitive to the noise/ripple on the references. Moreover, the C_{DAC} is reset to zero at end of the conversion phase by the SAR algorithm itself making the net charge absorbed by the reference generator during one conversion and the associated reference voltage ripple code independent. The combination of these two properties relaxes the noise/ripple requirements on the CS-DAC reference generator allowing a drastic reduction of the C_{REF} and easing the specifications on the reference buffer output peak impedance.

However, the CS-DAC is not as area-efficient as the CR-DAC. Each CS-DAC element requires, in fact, a top plate switch (that is a switch on the comparator side) in order to share the charge between C_{DAC} and C_{TH} in additive/subtractive way during the conversion phase. The parasitic capacitances associated with the top plate switches (C'x, C"x) affect the DAC element effective capacitance value. The scaling of the LSB capacitance in a CS-DAC is therefore dictated by the capacitance of a minimum size switch instead of kT/C noise. In deep-submicron technologies this usually leads to a significant core area penalty with respect to a CR-DAC.

To exploit the CS-DAC area advantage in the voltage references design while keeping competitive DAC core area in this work, a segmented SAR-DAC architecture (CS-CR-DAC) is adopted using a CS-DAC for the 4 MSBs and a CR-DAC for the remaining 6 LSBs (Fig. 10). The parasitic-insensitive 6 LSBs DAC capacitors can be scaled down as in a conventional CR-DAC to the kT/C noise requirements while the 4 MSBs CS-DAC capacitances are sufficiently large that the associated switch parasitics can be easily maintained proportionally small, hence impacting negligibly the DAC linearity. As the CR-DAC total capacitance (C_{CR}) is limited to the LSBs, the associated high-frequency ripple (ε_{MAX}) and the low-frequency code-dependent ripple are reduced roughly by 2 to the power of 4 (number of MSBs). Moreover, the transfer function from the reference voltage nodes to the comparator input benefits from the large attenuation (β) provided by the



TH and DAC weights (1=600aF)

CTH	CS[10:7]				CR[6:1]						CΔΣ
512	236	127	69	37	20	11	6	3	2	1	2

Fig. 10. CS-CR DAC and ΔΣ DAC.

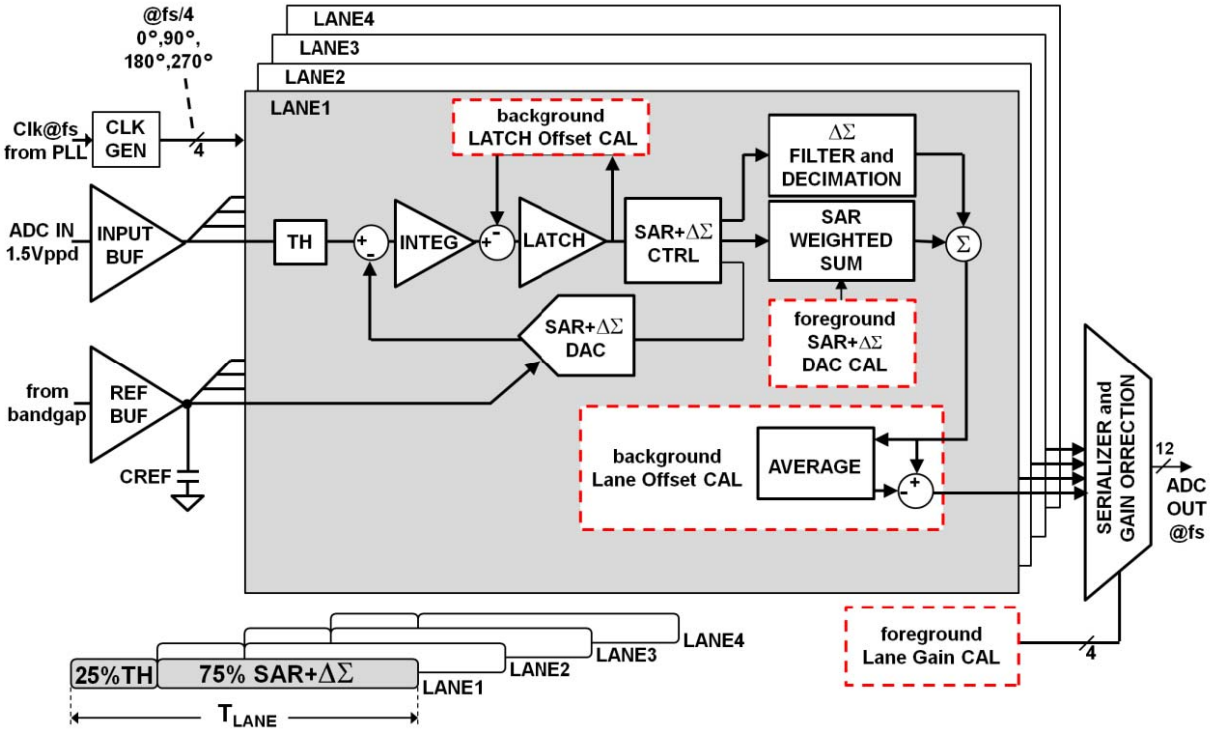


Fig. 11. Four-way interleaved SAR-ΔΣ ADC block diagram and calibrations.

4 MSBs of the C_{DAC} capacitance (C_{CS}) referred to ground. By keeping separate the reference generated voltages for the CR-DAC (V_{REFCR}) and for the CS-DAC (V_{REFCS}) segments, the former reference capacitance can be sized according to

$$C_{REFCR} \geq \alpha \cdot \beta \cdot \frac{T_{\Delta\Sigma}}{T_{LANE}} \cdot 2^{N-1} \cdot C_{CR} \cong 1.6\text{pF with}$$
$$\beta = \frac{C_{CR}}{C_{CS}} \quad (7)$$

where $N = 12$, $C_{CR} = 25.8$ fF, $\alpha = 1$, $\beta = 0.09$, $T_{\Delta\Sigma} = 2.22$ ns, and $T_{LANE} = 6.66$ ns. For the CS-DAC segment, the decoupling capacitance C_{REFCS} is chosen equal to 3.4 pF limiting the drop on the reference samples value to 10%. Each SAR ADC lane (with a core capacitance of 300 fF single-ended) requires a single-ended reference capacitor of only 5 pF ($C_{REFCS} + C_{REFCR}$). The V_{REFCR} and V_{REFCS} are shared among the four time-interleaved lanes for a total ADC reference capacitance of 20pF a quite large area saving when compared to the 200 pF (50 pF ×4) initially required with a charge-redistribution only solution. Both CR

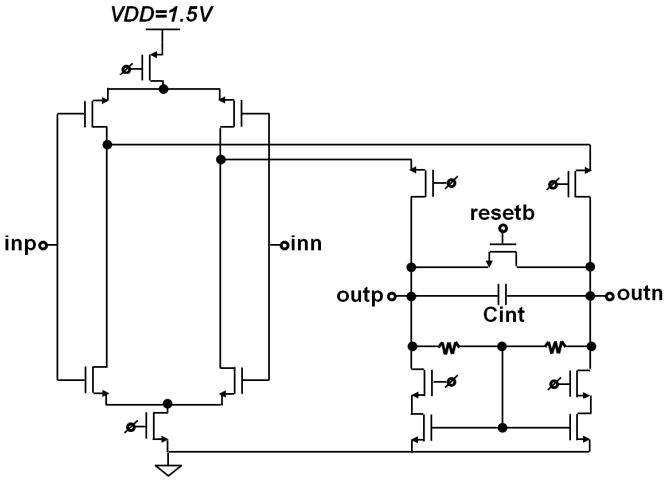


Fig. 12. Integrator with reset.

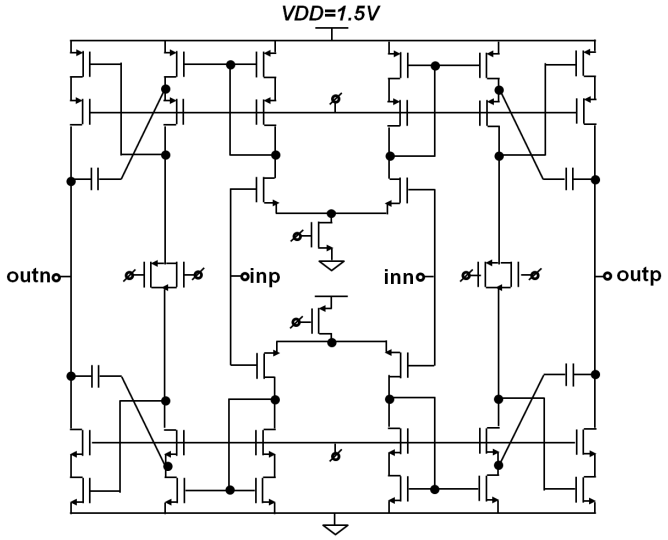


Fig. 13. Input buffer OTA.

and CS reference buffers are shared among the four lanes. Since they have relaxed specifications on the peak output impedance, each of them consumes only 100 μA from a 1.5 V power supply.

A main drawback of the charge-sharing operation is an input signal attenuation of 6 dB due to the sharing of the signal charge between sampling capacitor C_{TH} and C_{CS} capacitor. This increases the ADC input referred thermal noise from the comparator whose contribution to total noise is, however, reduced with respect to a conventional SAR ADC with the same power budget, by the SAR-$\Delta\Sigma$ ADC subrange architecture. Additionally, from a kT/C perspective, the CS-CR-DAC has roughly 3 dB more noise for the same DAC capacitance than a conventional CR-DAC since the reference voltages are sampled on the C_{CS} at the end of the tracking phase. This kT/C additional noise contributor is denoted in Fig. 16 as "Reference".

VII. ADC Architecture and Calibrations

The overall ADC architecture and the calibration scheme are shown in Fig. 11. The ADC uses four interleaved lanes driven

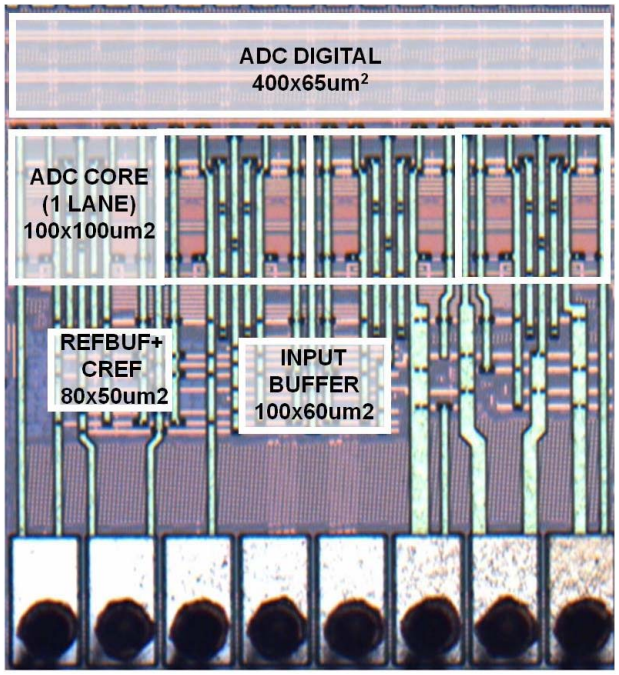


Fig. 14. Chip micrograph.

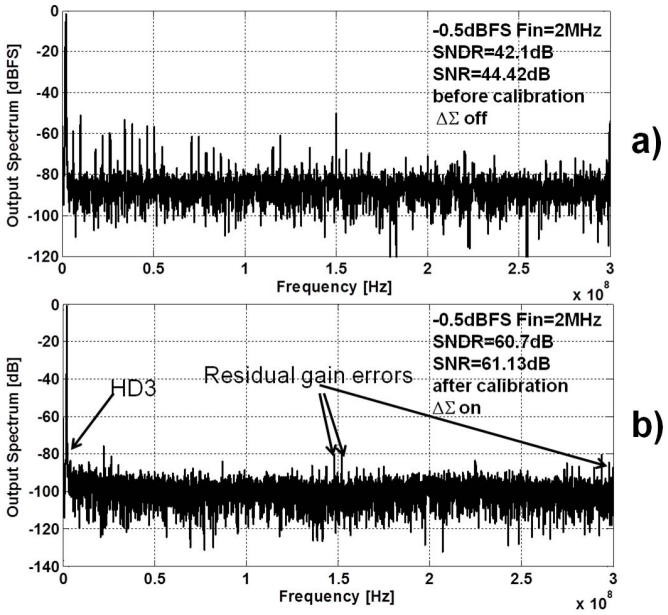


Fig. 15. ADC output spectrum at fin = 2 MHz (a) before calibration with $\Delta\Sigma$ off and (b) after calibration with $\Delta\Sigma$ on.

with a 25% duty-cycle clock generated from a 600 MHz PLL input clock. The ADC uses both foreground and background calibrations. At start-up, the offset and gain mismatches among lanes are calibrated as well as SAR-DAC mismatches. The latch offset calibration is performed both in foreground and in background. This is required to prevent $\Delta\Sigma$-sub-ADC saturation. At the end of the SAR phase the SAR residual error contains, in fact, the integrator offset plus the latch offset divided by the sampling data integrator gain. Since the integrator offset during the $\Delta\Sigma$ phase is the same as in the SAR phase it appears as a simple converter offset. On the contrary, the latch offset contribution during the SAR phase

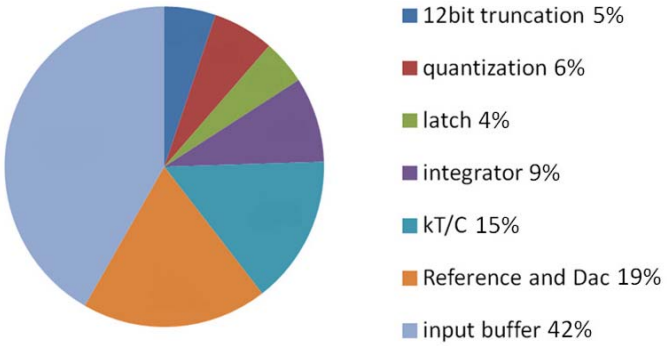


Fig. 16. Noise contributors of the SAR-ΔΣ ADC including input buffer at low frequency. SNR = 61.13 dB.

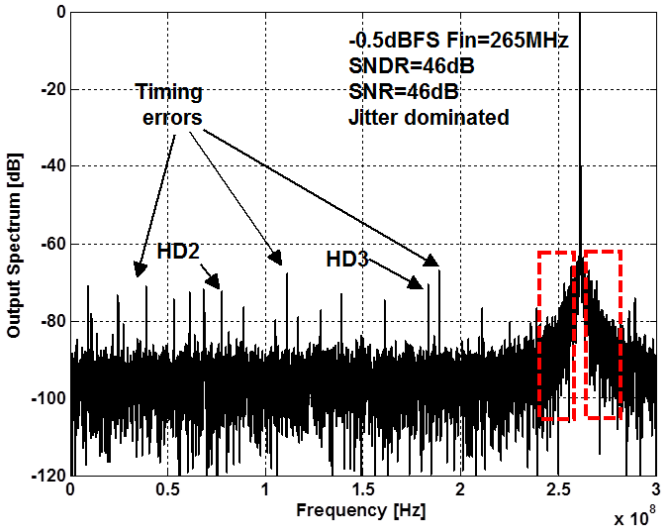


Fig. 17. ADC output spectrum at fin = 265 MHz (PLL jitter dominated).

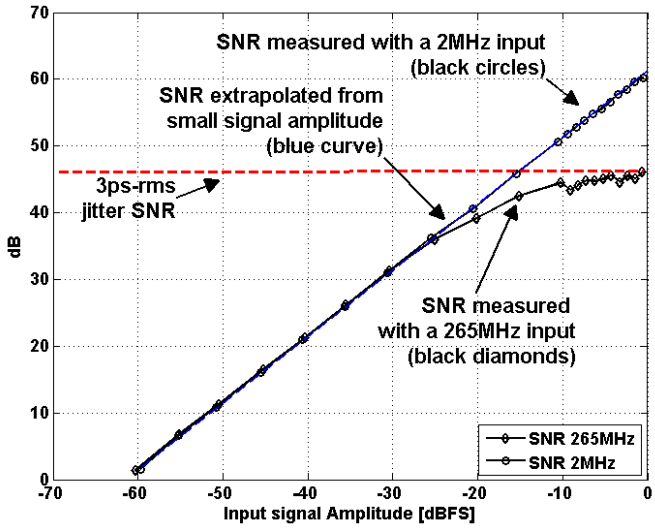


Fig. 18. ADC performance at 600 MS/s versus input amplitude at fin = 265 MHz.

is removed during the ΔΣ phase as the latch offset itself during ΔΣ phase is first-order high-pass filtered and highly attenuated. Therefore, the latch offset term must be kept within the ΔΣ-sub-ADC input range to avoid saturation. This is done

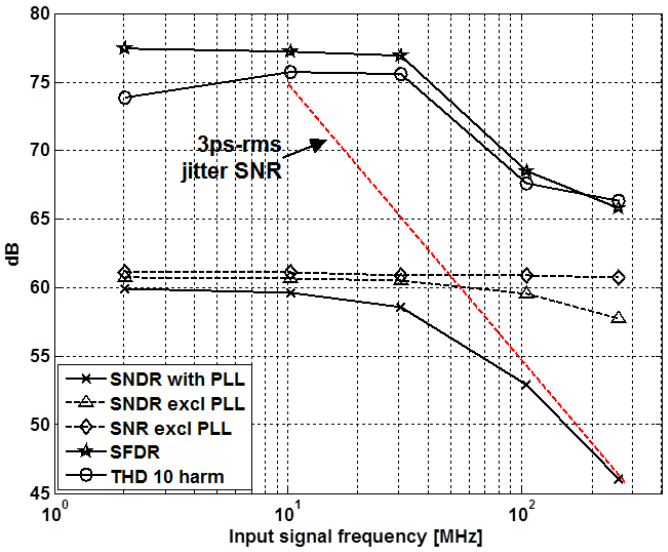


Fig. 19. ADC performance at 600 MS/s versus input frequency with and without PLL jitter.

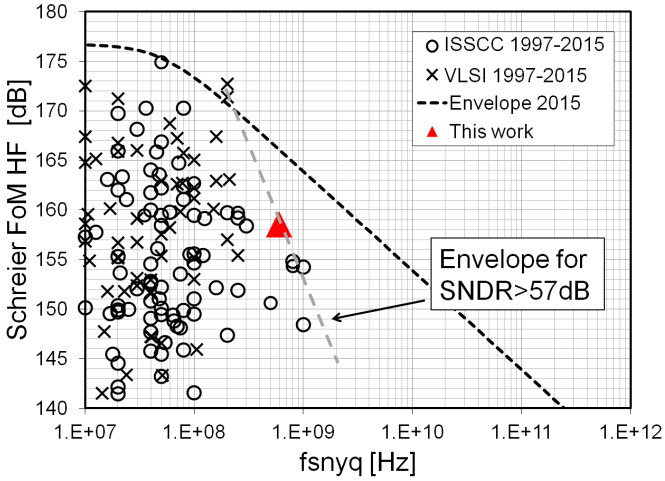


Fig. 20. Nyquist Schreier FoM versus Nyquist sampling frequency for ADCs published at ISSCC and VLSI between 1997 and 2015 with SNDR at Nyquist larger than 57 dB [25].

in background by detecting the ΔΣ saturation and applying an offset correction with an auxiliary differential pair in parallel to the latch input stage.

VIII. Circuit-Level Implementation

The static integrator (Fig. 12) that drives the dynamic latch uses a complementary input transconductor and a folding stage to increase the output impedance. The input unity gain signal buffer receives a 1.5 V peak-to-peak differential signal and drives the four interleaved ADC lanes T/H stages. The 25% duty cycle T/H sampling clock has been chosen such that always one lane is connected to the input signal buffer at a given time for best power efficiency. The T/H stage (see Fig. 10) consists of a couple of sampling capacitors (C_{TH} = 300 fF) in bottom plate sampling configuration. The C_{TH} are reset to a common mode voltage at the end of the conversion phase before being switched to the buffer output for

		[22] J. Mulder ISSCC 2015	[23] J. Mulder ISSCC 2011	[24] El Chammas ISSCC 2015	This work
Technology		28nm CMOS	40nm CMOS	180nm BiCMOS	28nm CMOS
Architecture		TI Pipeline	TI Pipeline	Pipeline	TI SAR-$\Delta\Sigma$
Resolution	bit	13	12	14	12
Fs	MS/s	800	800	500	600
Supply	V	1-1.8	1-2.5	1.8-3.3	1.2-1.5
Max input swing	Vppdiff	NA	NA	1.25	1.5
SNDR LF	dB	59.19	59	65	60.7
SNDR HF	dB	57	59	64	58
Power	mW	76.4	105	550	26.5
Walden FoM HF	fJ/c.s.	162.4	180.2	849.3	68.0
Schreier FoM HF	dB	154.3	154.8	150.6	158.5
Area tot	mm^2	0.23	0.88	2.5	0.076

Fig. 21. Performance summary and comparison with state-of-the-art ADCs (SNDR HF> 57 dB, Fs>300 MS/s) including on-chip buffering.

tracking. The buffer consists of an OTA in differential inverting configuration with a resistive ($R = 700\ \Omega$) feedback network. The OTA (Fig. 13) is a 2-stages single-slope with a class AB cascode compensated output stage. The unity-gain bandwidth is at 2 GHz to achieve the required gain at the edge of the signal bandwidth for linearity in tracking mode. The settling of the sampling capacitor from the reset condition to the tracking signal value is boosted by the OTA output stage that in the initial part of the settling drives the load with its low output impedance.

IX. Measurements

The ADC is fabricated in 28 nm CMOS process and consumes 17.5 mW from a dual 1.2 V/1.5 V supply. 1.5 V is used only for the reference generator and the integrator in order to improve the power supply rejection ratio. During operation, the power consumption of the digital calibration is less than 0.2 mW. The on-chip buffer, which drives the ADC full-scale of 1.5 V_{ppd}, has an SNR of 65 dB at Nyquist, and consumes 9 mW from 1.5 V. As the buffer cannot be bypassed, all of the measurements include buffer power consumption, distortions, and noise. The total area including input and reference buffer as well as digital calibration is only 0.076 mm^2 while the ADC core is 0.04 mm^2 as shown in Fig. 14.

With a 2 MHz input, the SNR and SNDR before calibration with $\Delta\Sigma$ off are 44 and 42 dB, respectively (Fig. 15(a)). After activating the fine $\Delta\Sigma$-sub-ADC and performing calibration, the SNR and SNDR performance increases to 61.13 dB and 60.7 dB, respectively (Fig. 15(b)). The simulated breakdown of the different contributors to the final SNR is shown in Fig. 16.

The ADC is integrated in a power-line communication (PLC) SoC and it is clocked by an on chip PLL with 3 ps rms jitter which cannot be bypassed. PLL jitter is measured between 300 kHz and 20 MHz frequency offset using an auxiliary clock output and a phase noise meter. Below 300 kHz, phase noise is considered as part of the input signal power, while above 20 MHz, the measurement is dominated by white noise of the auxiliary path buffer chain. This jitter figure is sufficient for the target application as the ADC input signal has a peak-to-average power ratio (PAPR) which is much larger compared to a sinewave. A spectrum with a 265 MHz input signal and PLL jitter included is shown in Fig. 17. The effect of the PLL jitter is visible in the skirts around the input tone. The SNR performance as a function of the signal amplitude for a 2 MHz and a 265 MHz input frequency (see Fig. 18) shows the typical jitter induced roll off the SNR when the input signal approaches full scale at high frequency. We can further verify this jitter measurement result by evaluating the ADC performance as a function of the input signal frequency (Fig. 19). The SNDR roll-off with the input signal frequency matches very well with a 3 ps-rms sampling time jitter induced SNR depicted in Fig. 19 as a red curve. Given the good agreement between the jitter measurement techniques, that is, the phase noise measurement and the SNDR roll off with input signal amplitude and frequency, we have extrapolated the ADC SNR performance from a small signal SNR measurement. The resulting SNDR performance has then been calculated by adding to the extrapolated SNR all the tones in the original spectrum. The results of this operation are depicted in Fig. 19 as dashed lines. After de-embedding the PLL jitter, the final SNDR performance at high frequency is 58 dB. The extrapolated SNDR degradation with the input signal frequency can be mainly ascribed to sampling time interleaving errors which are not calibrated in this design and to an increase in THD. This operation also removes the jitter of the ADC clock tree whose contribution (120 fs-rms estimated from post layout simulations) would nevertheless result in a negligible degradation of the 265 MHz SNDR.

Fig. 20 shows the Schreier FoM plot as a function of the Nyquist frequency for all converters published between 1997 and 2015 with Nyquist signal frequency and sampling speed larger than 10 MHz and SNDR at Nyquist higher

than 57 dB [25]. The presented work delivers 58 dB of SNDR with 26.5 mW of total power including input signal buffer, reference generator and biasing without requiring any additional BoM. The resulting HF Schreier FoM is 158.5 dB. The table in Fig. 21 shows a comparison between this design and other state-of-the-art ADCs with on-chip input buffers in the same speed and SNDR range. This work gives significant improvement in both FoMs and a drastic reduction in area.

X. Conclusion

In this paper, we presented a 12 b 600 MS/s 4-way interleaved ADC with on chip buffer that delivers 58 dB SNDR up to Nyquist. The total power including input signal buffer, reference generator, biasing and digital calibration is 26.5 mW resulting in a Schreier FoM of 158.5 dB. In 28 nm CMOS, the total area of this design is only 0.076 mm^2 and does not require any external component. The key enabling technologies for this design include the subranging SAR-$\Delta\Sigma$ architecture and the segmented charge-sharing charge-redistribution DAC. It achieves the state-of-the-art FoM in a very small total area.

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Alessandro Venca was born in Tortona, Italy, in 1970. He received the M.Sc. degree in electrical engineering from the University of Pavia, Pavia, Italy, in 1996.

He joined STMicroelectronics, Pavia, Italy, in 1997 and subsequently transferred to STMicroelectronics, San Jose, CA, USA, in 1999, where he was involved in analog mixed-signal IC design for Data Storage group. In 2007, he joined Marvell Semiconductor, Pavia, Italy, as an Analog IC Design Engineer. His main interests are in high-speed and high-performance analog/mixed-signal IC design.

Nicola Ghittori received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

During his Ph.D. work, he worked on CMOS analog circuits for wireless transceivers and analysis of package and substrate crosstalk in mixed-signal integrated circuits. In 2006, he joined Marvell Semiconductor, Pavia, Italy, as an Analog IC Design Engineer. His main interests are in high-speed and high-performance analog/mixed-signal circuit design.

Alessandro Bosi was born in Cremona, Italy, in 1975. He received the Laurea degree in electronic engineering and Ph.D. degree in electrical and computer engineering from the University of Pavia, Pavia, Italy, in 2000 and 2003, respectively.

In November 2003, he joined, as a Post-graduate Research Engineer, the Studio di Microelettronica, a University of Pavia–STMicroelectronics joint research center, where he focused on digitally assisted ADCs. In 2006 he moved to Marvell Italia as a Senior Analog Designer. His research interests include wide-band high-resolution analog-to-digital and digital-to-analog converters and digital calibration techniques.

Claudio Nani (M'15) was born in Brescia, Italy, in 1983. He received the M.Sc. degree in electrical engineering from the University of Pisa and Scuola Superiore Sant'Anna in 2007 and 2008, respectively.

From 2007 to 2010, he was with the Mixed Signal Circuits and Systems group of NXP Semiconductors Research, Eindhoven, The Netherlands, where he worked on high-speed ADC for cable tuners applications. Since 2010, he has been with Marvell, Pavia, Italy, working on high-performance data converters for telecommunications systems. His current research interests include high-speed power-efficient ADCs, data converter digital calibration systems and high-performance wireline interfaces.