A 25 GHz Fast-Lock Digital LC PLL With Multiphase Output Using a Magnetically-Coupled Loop of Oscillators

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***Abstract*—A fast-wakeup bang-bang LC digital phase-locked loop (DPLL) suitable for low-power wireline applications is presented. The PLL uses a novel oscillator design to generate eight output phases using magnetic coupling. The fast-wakeup feature improves power efficiency by allowing PLL power-cycling while accommodating latency requirements. Fast lock upon wakeup is achieved by calibrating the phase of the feedback clock with respect to the reference clock using a first-order loop and is further assisted by on-the-fly adjustment of loop parameters. The eight-phase output clock is generated using a loop of four digitally-controlled oscillators (DCOs) that are magnetically coupled through a passive structure. This structure enables magnetic coupling among oscillators with 2x area improvement over the prior art. As a result, in addition to eliminating the noise and parasitic capacitance of active coupling devices, the compact design reduces parasitic wiring capacitance, which is a significant limitation in high-frequency coupled oscillator design. Implemented in a 40 nm CMOS technology, the design achieves a 40-reference-cycle (100 ns) lock time and a 16% tuning range while producing an 8-phase output clock with less than 2° quadrature phase error up to 25 GHz. Measured PLL jitter is 392 fs (integrated from 100 kHz to 100 MHz) at 25 GHz while drawing 64 mW of power, 23 mW of which is consumed in the multiphase DCO. The DPLL occupies a total area of 0.1 mm^2.**

***Index Terms*—Digital LC PLL, digital phase-locked loop, digital PLL, fast-lock PLL, fast-wakeup, inductor coupling, LC oscillator, multiphase LC oscillator, oscillator, power cycling.**

I. Introduction

OVER the past few years, digital phase-locked loops (DPLLs) have progressively gained more popularity and become contenders to replace their analog counterparts. Some of the factors supporting this trend are better programmability, lower sensitivity to the poorly-controlled properties of nanoscale devices, ease of design porting and immunity to leakage currents. The continuous scaling of CMOS processes is expected to further strengthen these factors [1]. In addition to these advantages, DPLLs facilitate the design of fast-wakeup PLLs because digital values are easy to store and restore. Fast-wakeup PLLs are of particular interest for dynamic power-cycling, which can improve power efficiency [2], e.g., in a burst-mode memory interface, in which keeping the PLL active over long periods of inactivity can lead to power overhead. Another application area is low-power wireless communication systems such as Bluetooth or Global System for Mobile Communications (GSM) [3]. In the past, techniques based on injection locking have been proposed to achieve fast lock [4]. However, the jitter transfer functions of injection-locked systems are not well-controlled because of its dependence on the frequency difference between the center frequency of the oscillator and the injected signal as well as the injection power. Furthermore, imperfect locking can result in undesirable spurs in these systems. To alleviate this problem a fast-lock PLL can be used as proposed in [3], in which the properties of a DPLL were utilized. However, in the proposed solution, the need for frequency calibration prolonged the locking time. Furthermore, while the ability of DPLLs to store the latest state of the system prior to switching the operation state makes them a natural choice for fast-wakeup applications, their extension to higher frequencies, especially if multiphase outputs are desired, has proven to be quite challenging with few works reported in the literature that operate beyond 10 GHz [5]–[7].

Another important feature in many wireline applications is the ability to generate multiphase clocks, which is typically necessary for clock phase adjustment. At lower frequencies, multiphase clock generation can be readily accomplished by using ring oscillators. However, as the frequency of operation increases, jitter and speed considerations necessitate replacing ring oscillators with LC oscillators [8], [9], which do not generate multiphase outputs as easily as their ring counterparts. Multiphase clock generation through division needs a clock running at multiples of the desired frequency. Even if such a clock were available, the prohibitively large levels of power consumption for the required dividers would render a divider-based approach less attractive if not impractical. Recently, coupled oscillators have drawn significant attention in a variety of applications including low-phase-noise multiphase reference generation and high-power terahertz signal generation [10]–[13]. The advantages of coupled LC oscillators for multiphase generation are twofold: first, they exhibit superior phase noise performance compared to ring oscillators. Second,

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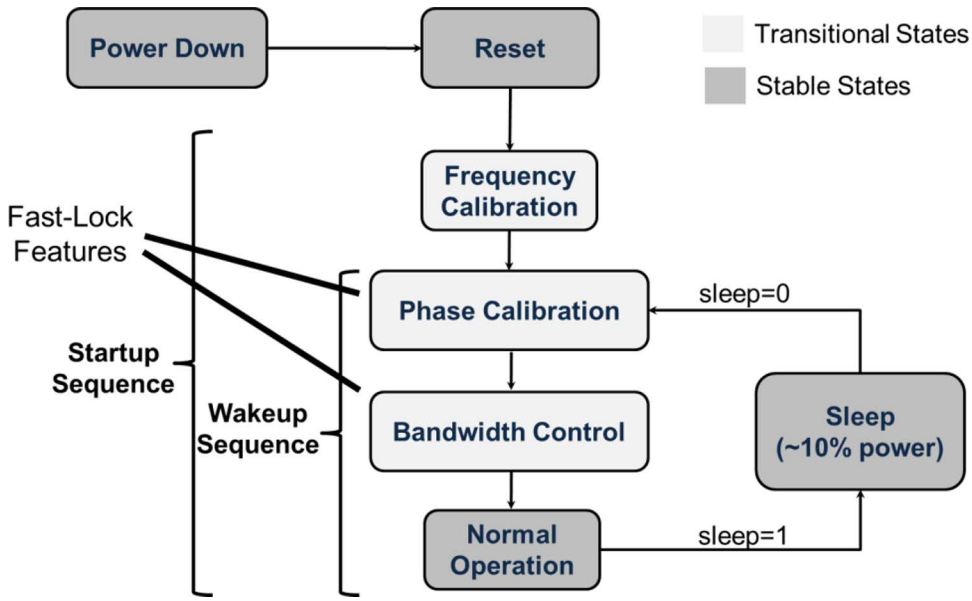


Fig. 1. State diagram of the proposed DPLL.

unlike divider-based approaches, where a reference oscillator running at multiples of the intended frequency is needed, coupled oscillators have blocks running at only the fundamental frequency or its sub-harmonics [12]. Conventional coupled oscillators employ active devices for coupling oscillators in the loop. The additional noise and capacitance of these devices can severely degrade the phase noise and tuning range of the oscillator [14], [12]. Recent work using inductive coupling through transformers has shown good performance as, unlike active coupling, passive coupling does not suffer from phase noise degradation. However, the use of transformers in passive coupling results in substantial area overhead [10].

This work addresses the two aforementioned issues, namely achieving fast lock and multiphase generation at high frequencies in DPLLs, by presenting detailed design of a fast wakeup DPLL that extends the frequency of operation of multiphase DPLLs to 25 GHz by employing a multiphase magnetically-coupled loop of LC oscillators [15]. The area overhead issue in a magnetically-coupled loop of four oscillators is addressed by proposing a new passive coupling structure. The proposed approach also eliminates the parasitic capacitances due to active coupling devices thus enhancing the tuning range of the oscillator. A high-resolution digitally-controlled oscillator (DCO) employing such a structure is demonstrated. The presented material is an extended version of [15] with additional details on the DPLL architecture, the implementation details of the fast lock feature and the multiphase coupled DCO and extra experimental results covering circuit performance.

The paper is organized as follows. Section II begins with an overview of the DPLL architecture along with its key features including the fast lock and the magnetically-coupled multiphase DCO. Section III discusses the details of circuit design for the implementation of the proposed architecture. Measured results covering circuit performance are presented in Section IV, and the work is summarized in Section V.

II. PLL Design

The proposed DPLL is an integer-N bang-bang loop that is suitable for wireline communication applications [7]. It is designed to be used in a power-cycle-able wireline link where, in the absence of active communication, the interface can enter a low-power state (hereafter referred to as sleep state) to improve the overall power efficiency. Upon wakeup, the interface needs to be ready for commination within accepted latency time of the system; thus, the PLL should be able to restore the clock of the interface to its proper phase within this allowed wakeup time.

Fig. 1 shows the state diagram of the proposed DPLL design. To facilitate effective power-cycling, the PLL has a sleep state in which power consumption is reduced by 10x. The PLL can wake up from this sleep state in an on-demand fashion. Upon waking up, it goes through a wakeup sequence and acquires phase lock within 100 ns (40 cycles of the reference clock). Such a short lock time is achieved through the fast-lock algorithm discussed in Section II-B. The DPLL provides a multiphase clock commonly needed for clock phase adjustment in wireline communication systems.

A. PLL Architecture

Fig. 2 shows the block diagram of the DPLL. The main loop of the DPLL consists of a 25 GHz multiphase LC DCO, the feedback path, a phase and frequency detector (PFD), and a digital loop filter. The frequency calibration loop includes the frequency calibration unit and shares the DCO and the feedback path with the main loop. Finally, the phase calibration loop uses all components of the main loop in addition to the phase calibration unit.

The DCO frequency is adjusted through fine and coarse control words. The fine word is controlled by a digital loop filter with conventional integral and proportional paths. The proportional path directly adjusts the DCO frequency while the integral path controls the frequency through digital accumulation of the phase error. A binary phase detector provides the

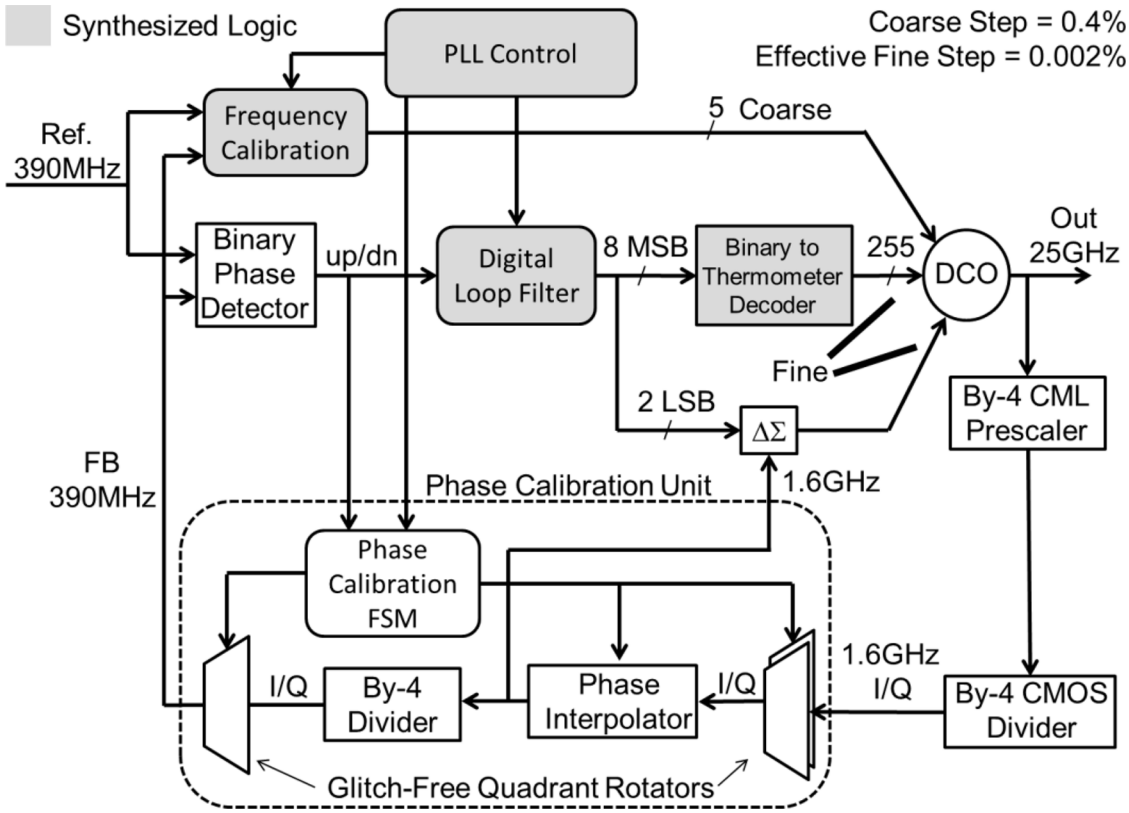


Fig. 2. Block diagram of the DPLL.

1 bit phase information (Up/Dn) for the loop filter. The integral path of the loop filter uses a 12 bit accumulator. Two LSBs of the accumulator output are discarded to create a built-in division by 4 in the integral path. The other 10 bits are summed with the proportional path to produce a 10 bit fine word. Of these 10 bits, 8 MSBs are converted to 255 thermometer-encoded lines, which control as many switches in the DCO. The remaining 2 LSBs drive a first-order $\Delta\Sigma$ modulator. Since the binary to thermometer encoder is implemented using synthesized logic, propagation delays from their inputs to their outputs are not well controlled, which can cause undesirable switching of the fine capacitors. To remove these undesired transitions, a retimer was added to the thermometer coded lines. This adds a half cycle to the latency around the DPLL loop but results in cleaner DCO output. Integral and proportional path coefficients are programmable and can be adjusted by the control unit during phase lock. The coarse word of the DCO is controlled by a frequency calibration unit, which is active only during PLL startup.

To cover voltage and temperature (VT) variations, DCO fine frequency control provides 2% tuning range in 255 steps of 0.008% each. The $\Delta\Sigma$ modulator, which is controlled by the 2 LSBs of the fine word, reduces the effective step size to 0.002%. With this step size, and a total loop delay of 2.5 clock cycles (1 for phase accumulation, 1 for DPLL accumulator, and 0.5 for all analog delays), peak-to-peak limit cycle jitter is predicted to be around 1 ps in a noise-free environment [16]. The $\Delta\Sigma$ modulator operates at four times the speed of the loop filter logic (1.6 GHz in this implementation). The 5 bit coarse control of the DCO provides 14% tuning range in 31 steps of 0.4% each. Fine tuning range of 2% and coarse step size of 0.4% guarantee that, after frequency calibration, the DCO has at least 0.6% tuning range margin in each direction to cover V_T variations. Simulation results show that temperature sensitivity is less than 20 ppm/°C, which after a temperature range of 50°C leaves enough room for 50 mV of supply variation in this implementation.

The phase calibration unit is the main component responsible for fast lock. At startup/wakeup, and before activating the main PLL loop, the phase calibration unit aligns the phase of the feedback clock with that of the reference clock to facilitate fast phase lock. This step is shown as phase calibration state in Fig. 1. The details of this unit will be discussed shortly.

The PLL control unit controls the state of the PLL and other digital circuits: phase calibration unit, frequency calibration unit, and loop filter coefficients. It invokes startup and wakeup sequences, shown in Fig. 1, as needed. During the startup sequence, it first activates the frequency calibration unit to set the coarse word of the DCO. Subsequently, it activates the phase calibration unit to align the phase of the feedback clock to that of the reference clock. Finally, it adjusts loop filter coefficients (bandwidth control state in Fig. 1) to further shorten lock time.

The control unit is also responsible for power cycling. It takes the PLL to sleep state when the sleep input is asserted. In this state, all circuits except for biasing circuitry are turned off, resulting in a 10x reduction in power consumption. Coarse and fine words of the DCO are stored to be used at wakeup. When sleep signal is de-asserted, the control unit restores fine and coarse words and takes the PLL through the wakeup sequence. The wakeup sequence is similar to the startup sequence except that it does not include frequency calibration. The advantages

and consequences of eliminating frequency calibration from the wakeup sequence are discussed in the next section.

B. Fast-Lock Features

The fast-lock features of the PLL aim at shortening the necessary time for phase lock acquisition after wakeup. To this end, the design tries to eliminate the need for frequency calibration when PLL wakes up from the sleep state. This is done by minimizing the shift in DCO center frequency (due to supply voltage and temperature variations) during the sleep interval. To minimize the shift due to supply voltage variations, in addition to using a differential LC oscillator, which is inherently less sensitive to supply variation, DCO biasing circuitry decouples the DCO from the supply rail by employing a V_T-based biasing scheme. To minimize the shift due to temperature variations, the duration of sleep is limited to a few microseconds. If the system requires longer sleep intervals, a master system control unit can divide each interval into shorter ones by periodically turning on the PLL. For example, this can be done by issuing mock transactions at a higher system level. Therefore, limiting the duration of the sleep state does not impose any serious limitations on the system. By minimizing the shift in the center frequency, we have made it possible to preset DCO frequency close to its target value at the beginning of the wakeup sequence without invoking frequency calibration. This is especially helpful in reducing total lock time because frequency calibration is often a lengthy process.

Unfortunately, presetting DCO frequency to the target frequency is not sufficient to guarantee fast phase lock because the PLL is a second-order system with two state variables: frequency and phase. In order to achieve fast phase lock, it is necessary to preset both state variables. Additionally, since the PFD is a sequential logic circuit with memory, it should be initialized properly to ensure that the PLL will take the shortest path towards phase lock, i.e., locks to the closest edge of the reference clock. In other words, to achieve fast phase lock, in addition to presetting DCO frequency, one needs to align the phase of the feedback clock to that of the reference clock and preset the PFD state to the right value.

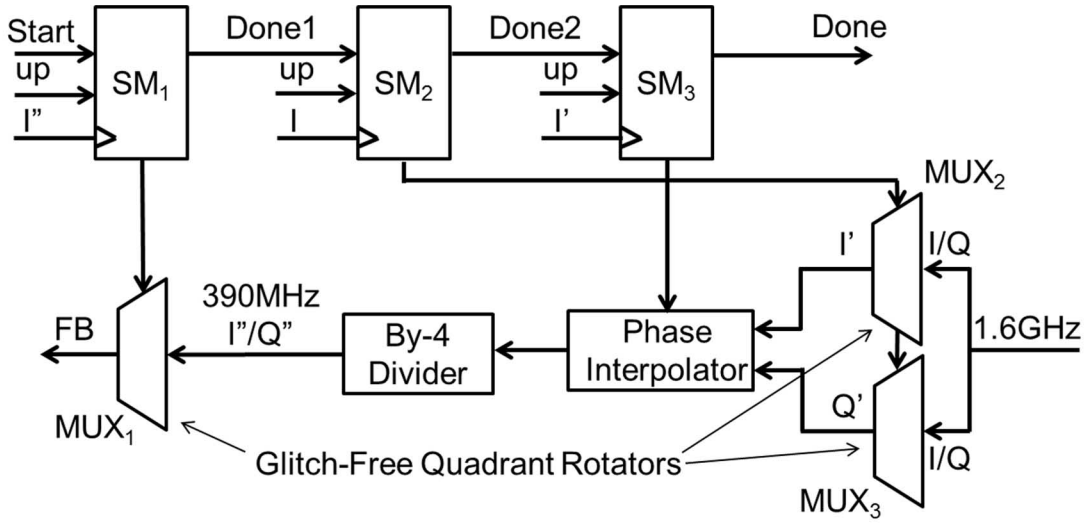
Based on this observation, the DPLL uses a phase calibration state machine to achieve fast lock. This operation is part of PLL startup/wakeup sequence. The phase calibration state machine aligns the phase of the feedback clock to that of the reference clock in a way that ensures the PFD has the correct state at the end of phase calibration. The output of the PFD (Up/Dn) is used by the phase calibration finite state machine (FSM) in a binary-search-like algorithm to bring the phase of the feedback clock close to that of the reference clock while preserving the number of edges on the feedback clock by avoiding glitches at the output. Such glitches can arise from the fact that this operation requires a multiplexer switching between two periodic signals with the possibility that the switching can inadvertently happen at the transition point of one of the two inputs. Avoiding these unwanted transitions is crucial to guarantee that the memory of the PFD stays undisturbed and PLL locks to the closest edge of the reference clock. Glitch-free quadrant rotators are used for this purpose. After phase calibration is complete, the control unit enables the main loop of the PLL. The PLL achieves steady-state phase-locked condition within a short time because 1) the frequency of the DCO is already close to its target value, 2) the phase of the feedback clock is close to that of the reference clock, and 3) the PFD is preset to choose the closest edge of the reference clock.

Fig. 3(a) shows the detailed implementation of the phase calibration unit. It consists of three finite state machines, SM_1, SM_2, SM_3, a phase interpolator, a divide-by-4 circuit, and three glitch-free quadrant rotators. Each quadrant rotator can shift the phase of its output by as much as one cycle in steps of 90° relative to its clock domain.

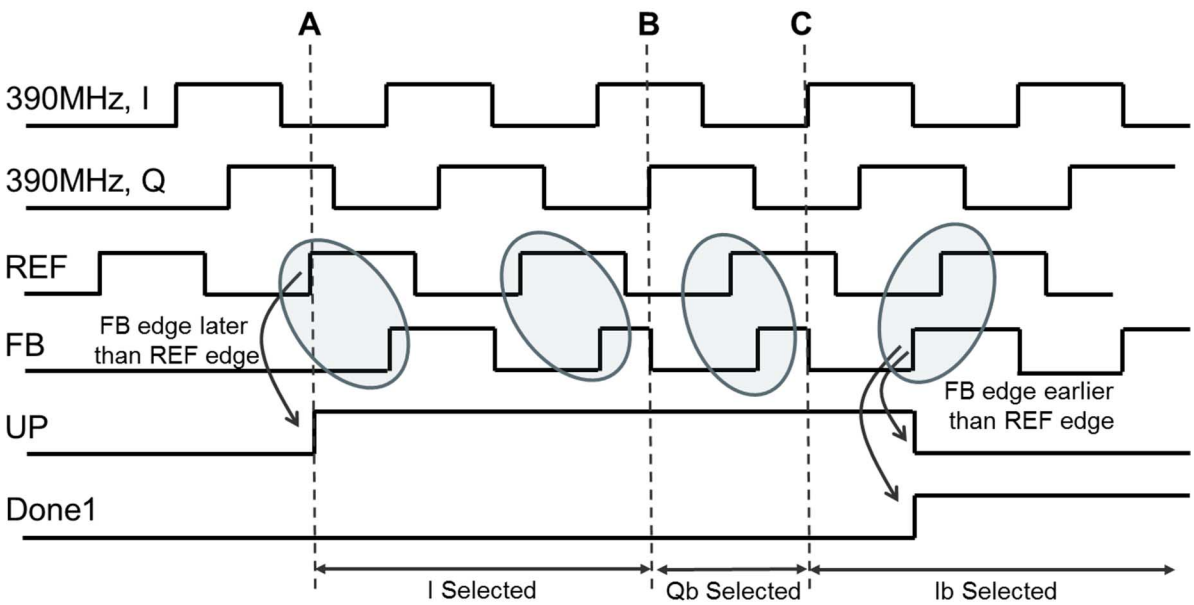
The operation of the phase calibration unit is as follows. Upon PLL wakeup, DCO settings are restored to their values prior to sleep and the DCO is free running. At this time, the frequency of the DCO is close to its target value but its phase is arbitrary. Next, the phase calibration unit halts the feedback clock (FB) until Up is asserted by the PFD. After reinstating the feedback clock, the finite state machine, SM_1, uses the left-most glitch-free quadrant rotator, MUX_1, to advance the phase of the feedback clock in 90° steps in the 390 MHz clock domain (each step = 641 ps steps) until Up transitions to low.

Fig. 3(b) shows a sample waveform of the operation performed by SM_1. At time A, Up gets asserted by the PFD because the feedback clock, FB, is halted. At time B, the quadrant rotator changes its selection from in-phase to quadrature-phase signal (I to Q_b), effectively advancing the phase of FB by 90°. However, since this phase shift is not enough to make the phase of FB ahead of the reference clock (REF), at time C, the quadrant rotator advances the phase of FB by another 90°. At this time, the phase of FB is ahead of REF (i.e., its edge arrives earlier), which causes Up to be de-asserted by the PFD prompting the completion of operation by SM_1. Note that at the end of this step, the phase difference between FB and REF is less than 90° or 641 ps. Next, the finite state machine SM_2 delays the phase of the feedback clock in 90° steps in the 1.6 GHz clock domain (or 22.5° in the 390 MHz clock domain, each step = 160 ps) until Up transitions to high. This operation is the same as that of SM_1 except that it is in the opposite direction (transition sequence is: I to Q to I_b to Q_b). Two quadrant rotators are used in this stage to generate I′/Q′ signals for the phase interpolator. One quadrant rotator will always select the signal that is 90° ahead of the one selected by the other one. At the end of this step, Up transitions to high prompting the end of SM_2 operation. Note that since the phase difference between FB and REF is 90° in the 390 MHz clock domain at the beginning of this step and since SM_2 can rotate the phase of the signal by as much as 4 steps of 22.5° each in the 390 MHz clock domain, this operation will always converge (i.e., Up will be asserted at the end of this step).

After completion of SM_2 operation, SM_3 uses a current-mode 32-step-per-quadrant phase interpolator to fine-adjust the phase of the feedback clock. It uses the Up output of the PFD to adjust the phase as needed. A combination of thermometer coding and step size limitation has been used to guarantee glitch-free operation when the code of the phase mixer is varied. Ideally, the phase difference between FB and REF is less than the LSB of the phase interpolator or 5 ps at the end of this operation. Since this operation is done without introducing any glitches on the feedback clock, the PLL will



(a)



(b)

Fig. 3. (a) Design details of the phase calibration FSM and (b) representative waveforms of phase calibration operation by SM_1 and the leftmost glitch-free quadrant rotator.

lock to this edge when the main loop is activated. It should be noted that the phase interpolator LSB was chosen based on a trade-off between phase calibration time and loop convergence time.

A bandwidth control scheme is also employed to further assist fast lock. After phase calibration is complete, the PLL enters the bandwidth control state. During this stage, the PLL control unit gradually reduces the value of integral and proportional path coefficients of the loop filter. This allows for starting with a large bandwidth to speed up the locking upon wakeup and gradually reducing the bandwidth to minimize dithering jitter. The step size and step time by which these parameters are reduced are programmable in order to allow post-fabrication optimization. The optimum values of these variables are dictated by the amount of supply noise and DCO frequency drift during the sleep interval. Although larger proportional path gain (K_p) and integral path gain (K_i) provide a larger bandwidth and faster lock time, they increase the dithering jitter in the DPLL. As such in a system with a small supply noise it is advantageous to choose smaller values of K_p and K_i to reduce dithering jitter; while in an application dominated by supply noise a larger K_p and K_i can lead to an improved overall jitter performance. Simulation results show that the proposed DPLL locks within 100ns of wakeup. In the presence of a 200 and 400

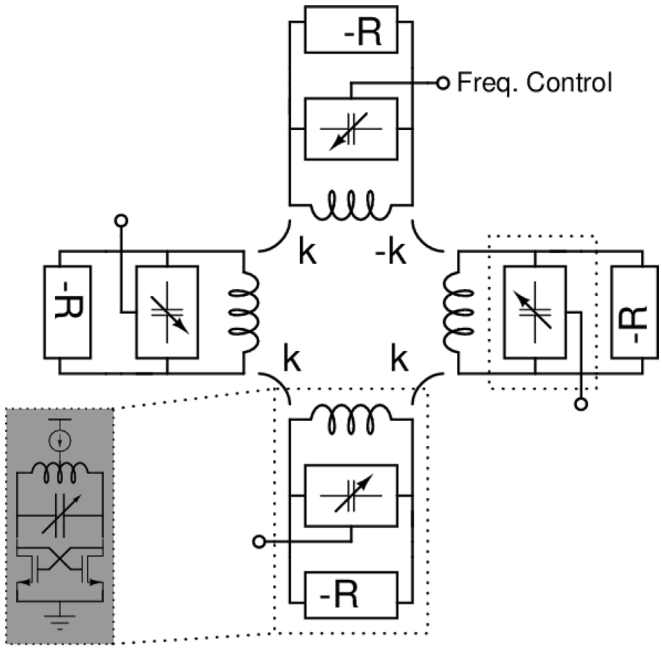


Fig. 4. Schematic of 8-phase loop of coupled oscillators.

ppm frequency offset, the lock time increases to 140 and 180 ns, respectively.

A few concluding remarks are in order regarding the proposed phase calibration scheme. First, note that phase interpolation is done in the 1.6 GHz clock domain to ensure a fixed phase relationship between the clock of the $\Delta\Sigma$ modulator and digital clock. Second, in many wireline applications, the relative phase of the PLL output clock with respect to the reference clock is of significance. When PLL phase calibration is invoked, this phase relationship changes each time the PLL goes through the wakeup sequence because, each time, the phase interpolator will have a different setting. To solve this issue, the code of the phase interpolator can be sent to the downstream phase interpolators to adjust the local clock phase accordingly. For systems that include downstream phase interpolators, e.g., most wireline applications, this does not impose any extra burden on the system. Finally, the effectiveness of the phase calibration technique depends on the accuracy of the DCO frequency and resolution of phase calibration. As we will see in Section IV, in the current design, the technique is effective enough to bring phase lock time to less than 100 ns (40 reference cycles) when used in combination with the bandwidth control technique.

C. Eight-Phase LC DCO

Fig. 4 shows the top-level schematic of the proposed multiphase DCO topology. The circuit comprises four identical LC oscillators, each of which is magnetically coupled to its two immediate neighbors. Multiphase operation is established by the single inversion in the sign of one of the couplings in the loop. Despite the seemingly straightforward underlying theory, the key design challenge is to implement the required coupling between various oscillators as well as the inversion in an area-efficient fashion.

In general, coupling in a loop of oscillators can be implemented using passive or active elements. The noisier nature of active devices can lead to degraded phase noise and additional power consumption. On the other hand, the need for large passive components typically makes an approach based on passive coupling undesirable in integrated oscillators because of area considerations. In this work we propose a passive structure that addresses the area issue in passive coupling. In our proposed structure, shown in Fig. 5, coupling between oscillators is implemented through a unified transformer without the need for additional noisy transconductance elements and individual area-consuming transformers used in previously-reported magnetically-coupled oscillators [10], [12]. The structure comprises four single-turn inductors, each divided into two parts. Magnetic coupling is established by overlaying inductor halves of neighboring oscillators thus effectively implementing transformers. The inversion in the loop is implemented by reversing the flow of the magnetic flux by reversing the direction of current flow in one half of one of the inductors. The proposed structure reduces the total required area for all four inductors to that of two inductors.

In conventional coupled oscillators, the extra capacitance due to the additional routing required for the coupling elements as well as the input capacitance of the coupling devices limits the tuning range. In the proposed topology, however, the only added parasitic capacitances are those between wirings of overlaid inductors, which are negligible compared to transistor capacitances. Furthermore, the compact transformer design helps to minimize wiring capacitance.

Symmetry in a loop of coupled oscillators is crucial in achieving reasonable phase accuracy. The analytical derivation of the impact of mismatch between tanks, transistors in each oscillator, or capacitive banks was reported in [14], [17], where the impact of mismatch on phase accuracy was shown to be a function of coupling strength. Note that the inversion in the loop inherently introduces a geometrical asymmetry in the loop. To mitigate the impact of this asymmetry, a U-bend was maintained even in the inductors that did not need inversion. Simulation results showed that this middle U-bend in the layout degrades the quality factor (Q) of the inductor by roughly 10%; however, it significantly improves the symmetry of the structure.

The multiport inductor was simulated using Agilent's Momentum simulator and a compact model is developed to facilitate oscillator design. A comparison of the impedance of the compact model (shown in Fig. 5) to that based on EM simulation results is shown in Fig. 6. Z_0 denotes the magnitude and phase of the impedance looking into the differential inputs of one of the non-inverting inductor loops, and Z_1 denotes the impedance of the inductor with the inverted half. The three inductors that have a similar structure show the same impedance curve, and thus only one is shown here. In order to achieve the best performance, both impedances should be identical, so that the resonance frequencies of all tanks are the same. In order to create a distinct resonance frequency and to improve the accuracy of the modeling procedure, an ideal 300 fF capacitor was added across all ports in simulations. The close agreement between EM simulation results and the

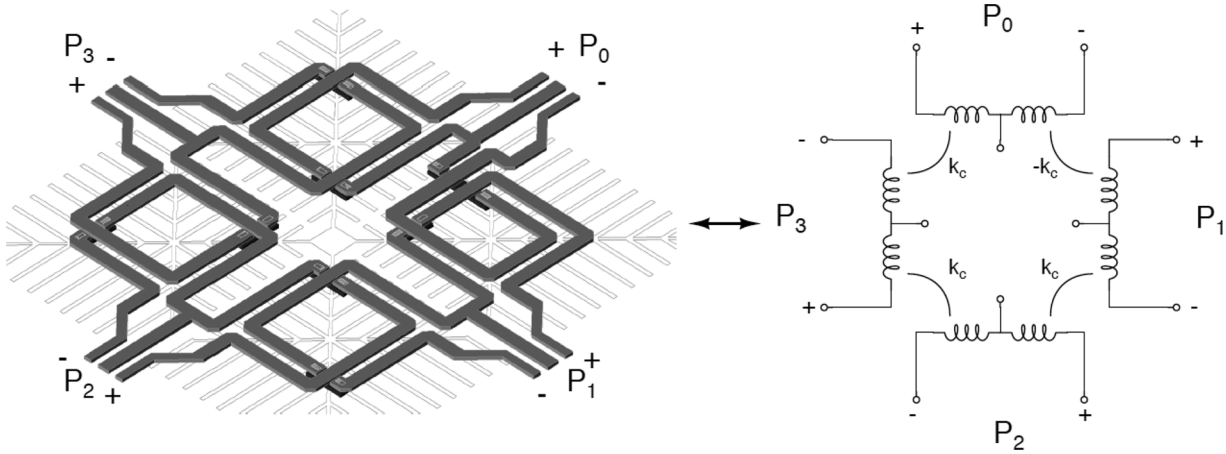


Fig. 5. Proposed multiport coupled inductor and its equivalent lumped model.

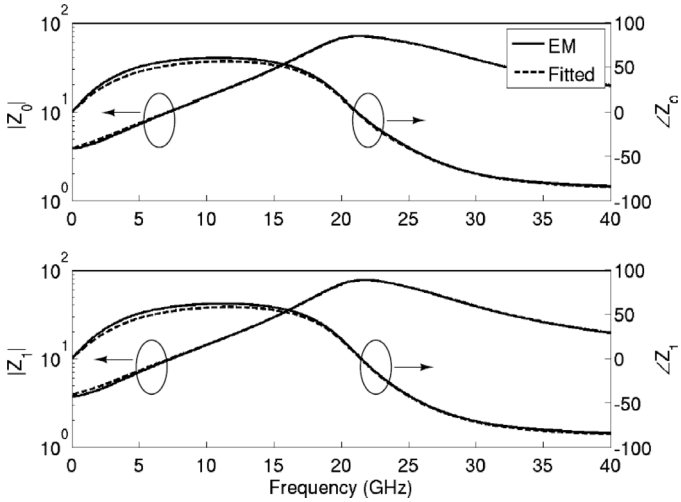


Fig. 6. Comparison of EM and lumped model simulations of the multiport inductor.

compact model across a wide range of frequencies is partly due to the relatively low Q of the structure in the design as well as the high self-resonance frequency.

The magnetic coupling increases the effective inductance of each oscillator tank. It can be shown that the oscillation frequency for coupled oscillators with a coupling factor, k, is given by

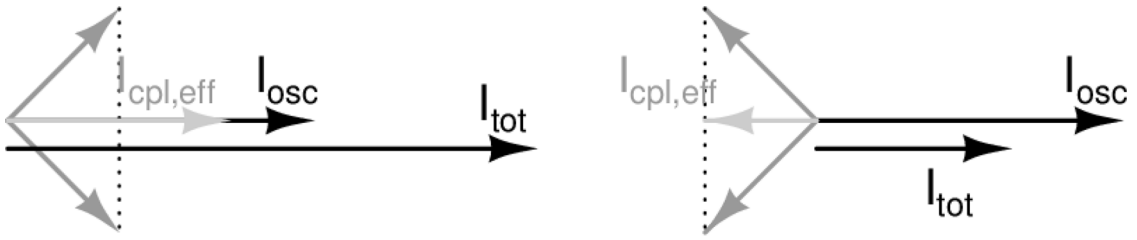
$$f_{osc} = \frac{1}{2\pi\sqrt{(1 + k\cos\frac{\pi}{n})LC}}$$

where n is the number of oscillators in the loop, L is the inductance of a single inductor, and C is the total capacitance.

It is noteworthy that the coupled loop of four oscillators has multiple modes of operation with two distinct phase relationships corresponding to $\pm 45^\circ$ and $\pm 135^\circ$ of phase difference between adjacent oscillators. The phasor diagrams of currents under these two modes are shown in Fig. 7. As can be seen in both cases, due to the bidirectional nature of the coupling, the out-of-phase components of coupling currents cancel out each other. However, only in the $\pm 45^\circ$ mode, the in-phase coupling adds up constructively with the oscillators own magnetic field, and thus the $\pm 45^\circ$ mode always prevails because of its larger amplitude [18].

Improving the overall phase noise is a desirable feature of coupled oscillators. It can be shown that under noiseless coupling conditions the overall phase noise of a loop of n oscillators improves by $10\log(n)$ in dB scale [19]. The primary reason for this effect is that any phase perturbation in the loop is divided among n oscillators, thus its power reduces by n^2, while the power of noise increases by only a factor of n. In practice, the achievable noise improvement has been limited by the additional noise of the coupling devices as well as the off-resonance operation of most coupled oscillators. The bidirectional coupling in this work enforces at-resonance operation [12]. Furthermore, the absence of noisy transconductors eliminates their typically significant contribution to phase noise. As will be shown in Section IV, in our measurement results, the phase noise improvement in the case of magnetically-coupled loop of oscillators is close to its theoretical value of 6 dB. Therefore, the multiphase output is generated virtually at no additional cost on the oscillator's figure-of-merit.

To implement digital frequency tunability, a digital-to-capacitance converter is required. A common way of implementing capacitor banks is to divide them into two groups of digitally-switchable fixed capacitors and an analog varactor. However, this approach requires a dedicated digital-to-analog converter (DAC) for voltage control [20]. In this work, we have employed a fully digital solution, shown in Fig. 8, in which all capacitors are directly driven by the output of the digital loop, thus eliminating the explicit voltage DAC. It should be noted that, due to the digital voltage levels driving the gates, the capacitance value for each transistor switches between two distinct values corresponding to on and off states. The coarse capacitive bank comprises binary-weighted metal-oxide-metal (MOM) capacitors that are controlled by NMOS switches. The fine thermometer-coded capacitive bank consists of a bank of 2×256 unit transistors used as NMOS capacitors. Each transistor acts as a switchable capacitor with the shorted source/drain terminals either pulled high or low by the digital control bit.



(a) (b)

Fig. 7. Phasor diagram of currents in $\pm 45^\circ$ and $\pm 135^\circ$ modes. (a) $\pm\pi/4$ mode. (b) $\pm 3\pi/4$ mode.

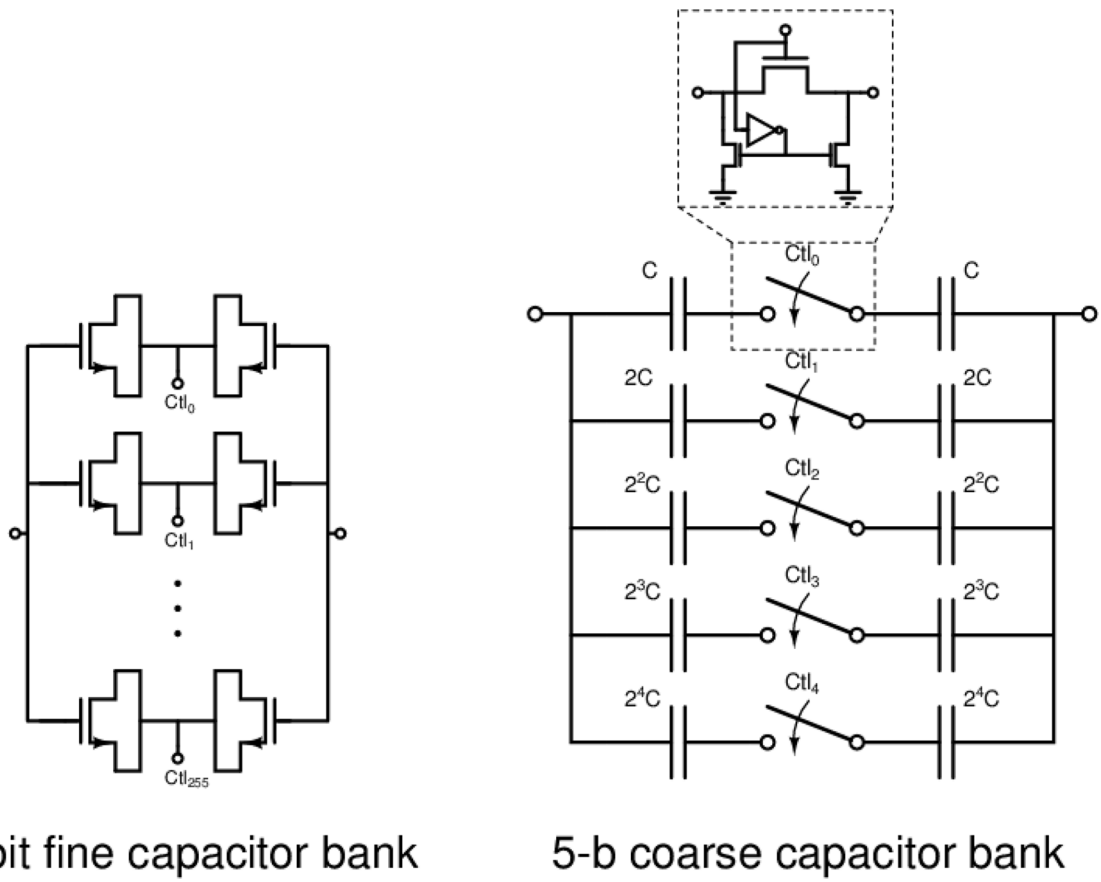


Fig. 8. 13 bit hybrid digitally-controlled capacitor bank.

III. Circuit Implementations

The proposed DPLL was designed in an LP 40 nm CMOS process with 7 metal layers. Standard logic flow is used to synthesize the frequency calibration unit, loop filter, binary-to-thermometer decoder, and the retiming flip-flops of the thermometer-coded fine word of the DCO. All synthesized logic is clocked using the 390 MHz feedback clock. The phase calibration unit is implemented using custom logic. The phase interpolator is a standard current interpolating structure similar to the one in [21].

The design of the glitch-free quadrant rotator is shown in Fig. 9. It consists of seven I/Q glitch-free multiplexers, three of which are used as dummy devices to equalize load on the input clock and the delay from all inputs to the output. Each I/Q multiplexer receives a pair of quadrature clocks and selects one of them at its output. It takes advantage of the known phase relationship between its two inputs to facilitate glitch-free switching between them. Specifically, by retiming the selection signal using the Q input (see the inset of Fig. 9), it guarantees that the internal select will only transition during the time when both I and Q are high. Therefore, the output can switch between I and Q in a glitch-free manner. Using this building block, the glitch-free quadrant rotator can rotate the phase of its output by as much as one cycle in 90° steps.

The DCO core comprises a cross-coupled NMOS transistor pair acting as a negative resistance, and a PMOS current source attached to the center point of each inductor. The passive multiport inductor was implemented on the top two metal layers. Electromagnetic simulations show that the quality factor of the DCO's inductors is about 5 at 25 GHz. The relatively low Q is primarily due to lack of a thick top metal layer.

The MOM capacitors were implemented by stacking the top three metal layers. Careful layout provisions were employed to

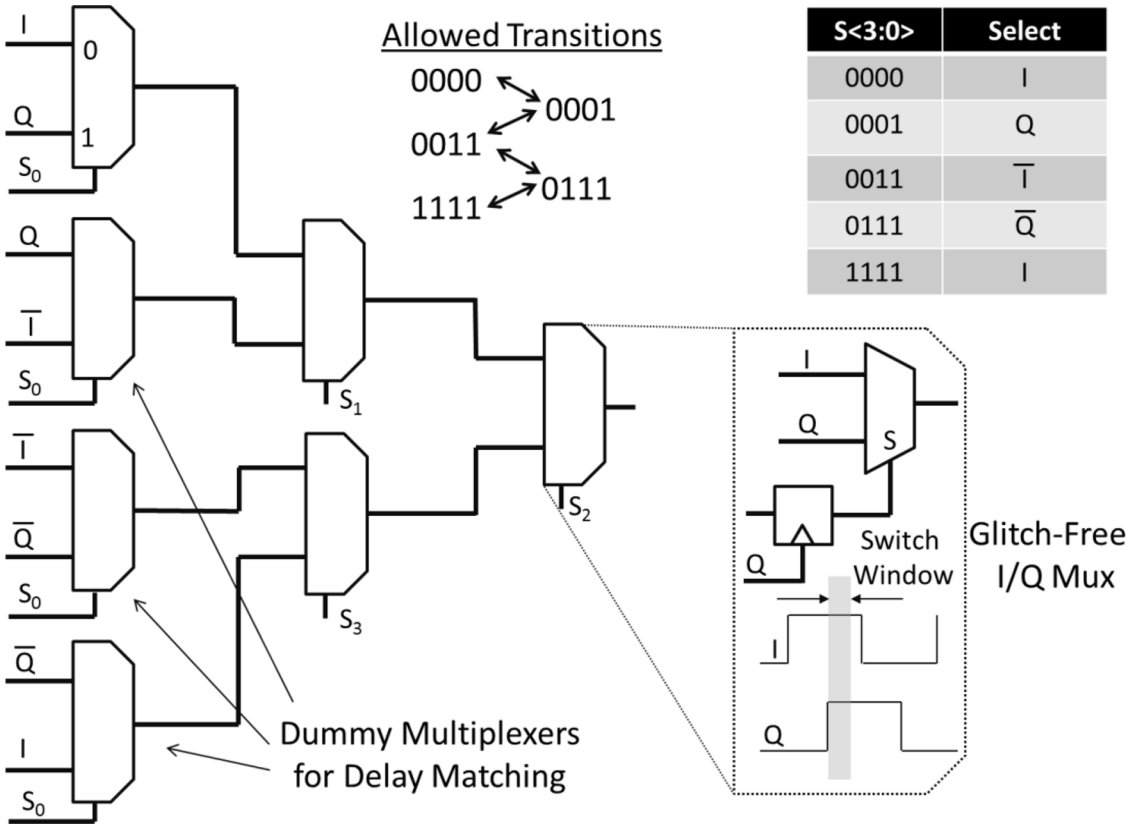


Fig. 9. Glitch-free quadrant rotator.

minimize parasitic capacitances due to the excessive amount of wiring required for high-frequency resolution, and to maintain wide tuning range. Instead of all DCO cap banks sharing the same capacitor code, provisions were also applied to enable local calibration of capacitor codes for each oscillator. This additional feature allows tuning of individual tanks to avoid frequency mismatch between individual oscillators (particularly between the one with inverted inductance and the rest) and thus improve phase accuracy and phase noise.

The BB-PFD consists of a PFD followed by a metastability filter and two SR latches to extend Up/Down pulses over one clock period [7]. Frequency calibration is done using a binary search and a high-accuracy counter-based frequency comparator.

The DPLL occupies an area of 0.1 mm^2 including DCO inductors and wiring for digital control lines but excluding pad driver inductors (Fig. 10). The DCO occupies 0.064 mm^2. Synthesized logic occupies 0.008 mm^2 of area (90 μm $\times$ 90 μm) with 59% area utilization. Half of this area is used by the 255 retiming flip-flops on fine control lines.

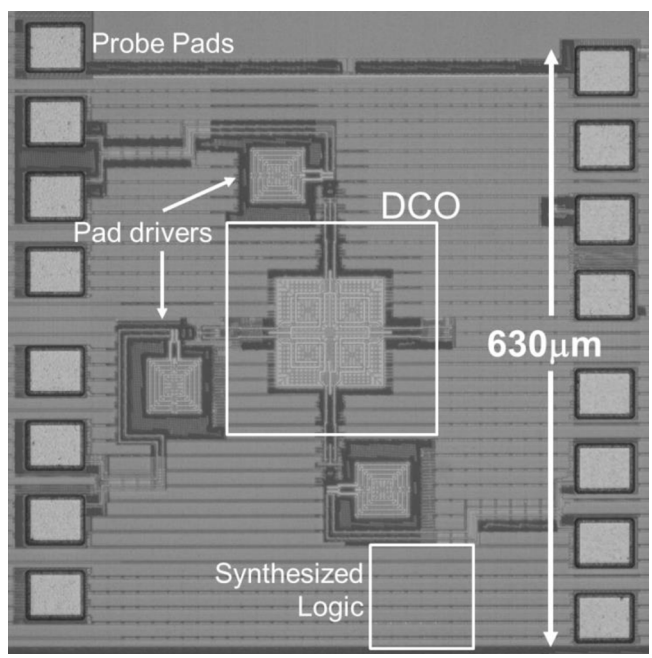


Fig. 10. Die micrograph.

IV. Measurement Results

To verify the effectiveness of the proposed architecture, PLL characterization was performed in both locked condition and during wakeup, and DCO performance was characterized in both open-loop and closed-loop configurations. Fig. 11 summarizes the measured phase noise of the DCO across the operating frequency range, and shows a snapshot of the phase noise profile at the mid-band. The reported phase noise numbers are measured on a divide-by-4 output and are pessimistic due to the noise of the divider and buffers. The results were adjusted to the full-range frequency assuming ideal noiseless dividers. The measured tuning curve of the DCO is shown in Fig. 12, where the monotonicity of frequency variation versus fine code

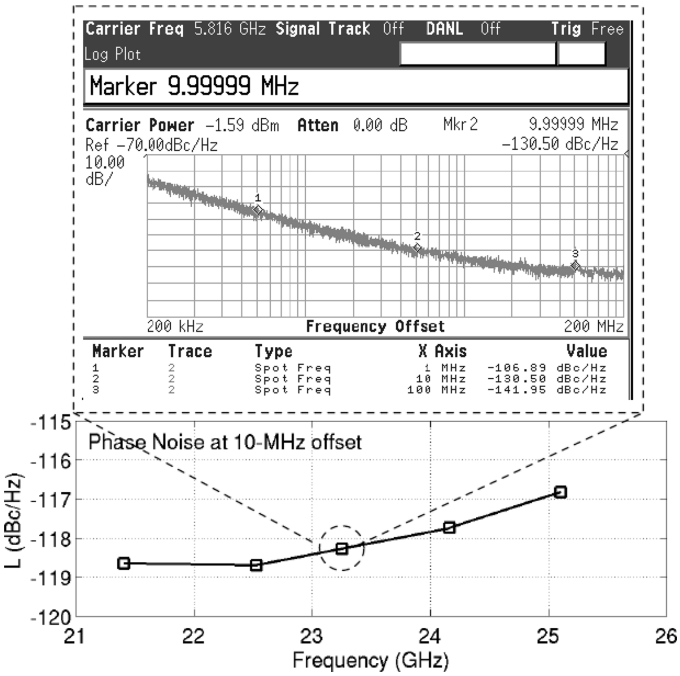


Fig. 11. Measured phase noise across tuning range and sample phase noise plot.

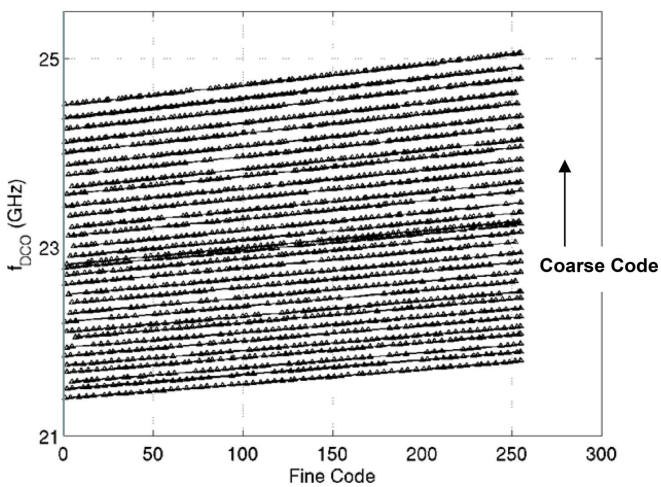


Fig. 12. Measured DCO tuning curve.

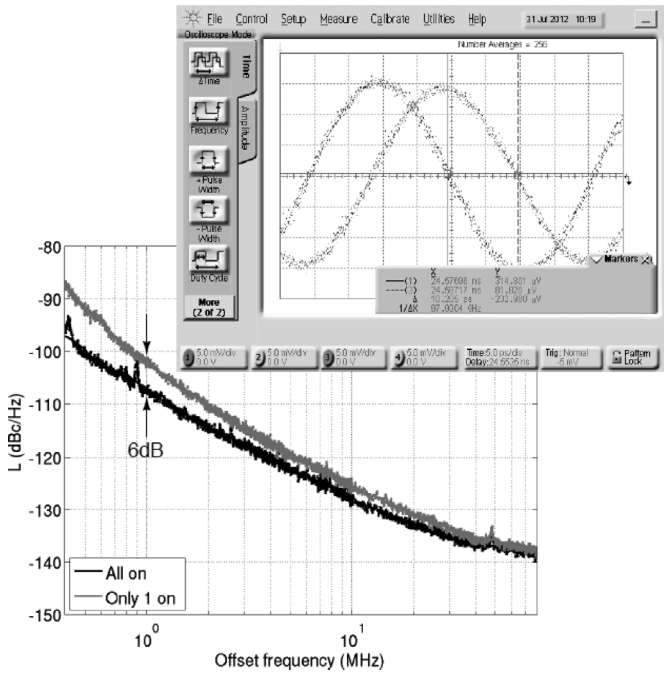


Fig. 13. Representative quadrature signals at 24 GHz and measured improvement in phase noise due to coupling.

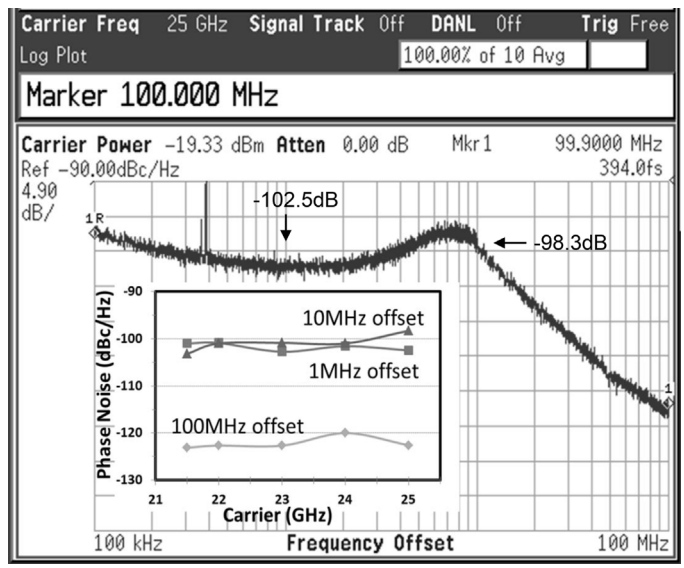


Fig. 14. Phase noise characteristics of the output clock.

is maintained thanks to the thermometer encoding scheme. The DCO achieves 16% of tuning range with fine tuning DNL and INL of better than 1.5 and 4 LSB, respectively. A snapshot of the quadrature output phases at 24 GHz is shown in Fig. 13. The measured quadrature phase error is less than 2° and is limited by the measurement setup. To achieve this level of phase accuracy, the wire lengths to all probe pads in the layout were matched. A similar load matching technique is required in an actual system implementation. Also shown in this figure is the impact of magnetic coupling on the phase noise, where the coupling improves the loop phase noise at 1 MHz offset by almost 6 dB compared to a single oscillator stage.

Fig. 14 shows phase noise characteristics of the 25 GHz output generated from a 390 MHz reference. At 1 MHz and 10 MHz offset frequencies, phase noise is −102.5 dBc/Hz and −98.3 dBc/Hz, respectively. Total integrated jitter from 100 kHz to 100 MHz is 394 fs. Bounded dithering jitter of the digital loop is included in this number. The figure also shows measured phase noise over tuning range as well as a sample phase noise spectrum. The breakdown of jitter components in time domain is shown in Fig. 15.

Fig. 16 shows the behavior of the PLL at wakeup where, to demonstrate repeatability, a periodic sleep signal is issued and traces are overlaid. Phase calibration takes place after the signal from the DCO and the dividers are stable. After phase calibration is completed, the PLL control unit adjusts the coefficients of the loop filter to further assist fast lock. This figure also shows peak-to-peak jitter of the feedback clock versus time after wakeup indicating phase error versus time from wakeup. The

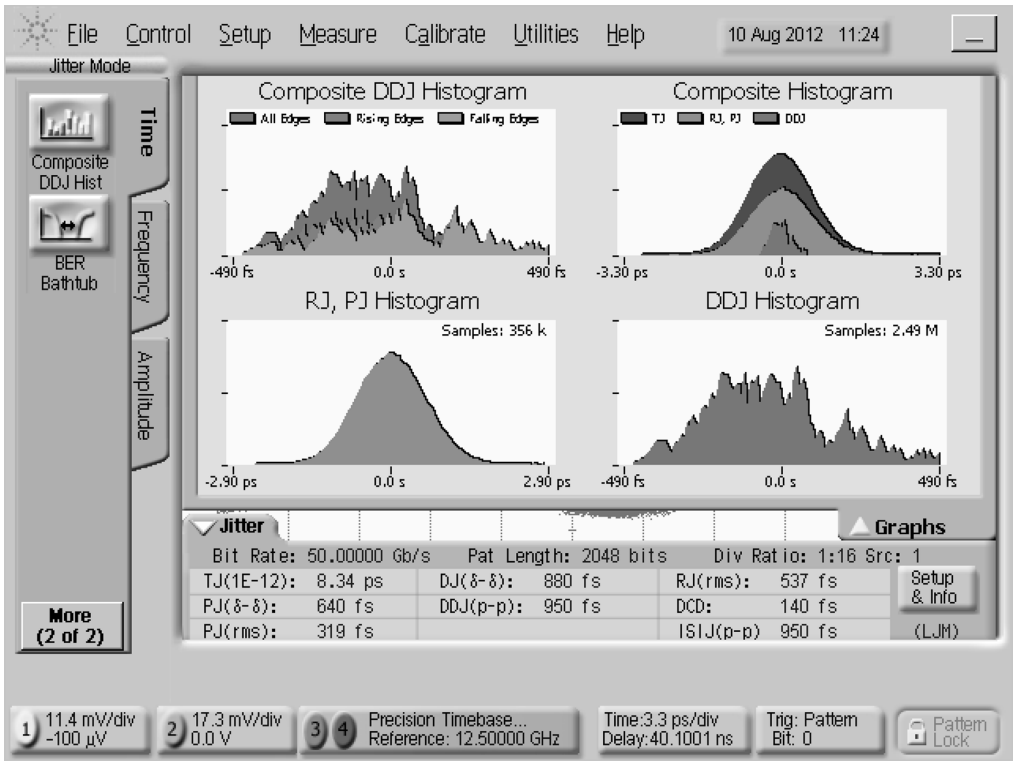


Fig. 15. Jitter component breakdown under locked condition.

baseline jitter (sleep signal zero) is 28 ps and is due to various sources of jitter in the feedback path of the PLL and CMOS pad drivers. Jitter after 100 ns from PLL wakeup moment flattens at 39 ps. The extra jitter is attributed to higher activity of digital circuits when PLL sleep signal is toggled. With a reference clock of 390 MHz, the DPLL achieved a lock time of 100 ns or 40 reference cycles. A higher frequency reference clock can reduce the lock time in two ways: the first one is by allowing a higher PLL bandwidth, and the second one is by speeding up the calibration state machine, which relies on the reference clock for its operation.

Table I summarizes the multiphase oscillator performance and compares it to state-of-the-art multiphase DCOs, highlighting the tuning range and significant area advantage of the proposed approach compared to references despite running at less than half the frequency and offering 8 output phases.

Table II compares the performance of the DPLL with the prior art. Compared to [2], this works achieves 3x faster lock time with respect to the reference frequency. Reference [9] reports lower jitter thanks to employing a hybrid solution despite larger spot phase noise at 1 MHz. None of the references included in Table II generate multiphase outputs.

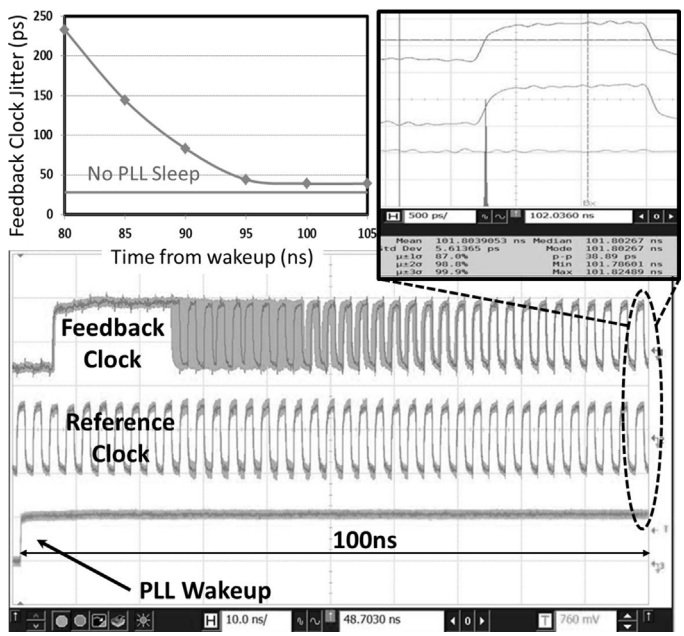


Fig. 16. PLL behavior at wakeup. PLL is periodically power-cycled; post-divider feedback clock and reference clock are delay-matched from the input of the PDF to the instrument.

V. Conclusions

A fast-wakeup DPLL for low-power wireline applications has been presented. Fast lock upon wakeup is achieved through two techniques: calibrating the phase of the feedback clock with respect to the reference clock using a first-order loop, and on-the-fly adjustment of loop parameters during lock acquisition. The LC PLL generates eight output phases using a loop of four LC DCOs that are magnetically coupled through a proposed passive structure. A high-resolution fully-digital capacitor bank allows for fine control of the output frequency. Implemented in a 40 nm CMOS technology, the design achieves a 100 ns lock time (40 reference clock cycles) and a 16% tuning range while producing output clock with less than 2°

TABLE I
MULTIPHASE DCO PERFORMANCE SUMMARY AND COMPARISON

	ISSCC 2011 [10]	JSSC 2011 [11]	ISSCC 2014 [22]	This work
Technology	65nm CMOS	0.13μm CMOS	40 nm CMOS	**40nm LP CMOS**
Frequency (GHz)	56.0-60.5	48.6-52.0	53.8-63.3	**21.4-25.1**
No. of phases	4 (Quad.)	8 (45°)	4 (Quad.)	**8 (45°)**
Area (mm^2)	0.075	0.09	0.06*	**0.063**
Power (mW)	22mW	35	30	**23**
Phase noise @10MHz (dBc/Hz)	-117/-115	-128	-108	**-119/-117**

* Estimated from die photo

TABLE II
DPLL PERFORMANCE SUMMARY AND COMPARISON

	JSSC 2010 [2]	JSSC 2014 [9]	ISSCC 2009 [7]	This work
PLL Architecture	Analog	Hybrid	Digital	**Digital**
Technology	40nm LP CMOS	32nm SOI CMOS	65nm CMOS	**40nm LP CMOS**
Frequency (GHz)	2.7-4.3	23.8-30.2	16.4-22.4	**21.4-25.1**
No. of phases	2 (Diff.)	2 (Diff.)	2 (Diff.)	**8 (45°)**
PLL area (mm^2)	-	0.022	0.1	**0.1**
PLL power (mW)	-	31	64	**64**
PLL lock time	250ns 130 ref cycles	-	-	**100ns 40 ref cycles**
PLL phase noise @ 1MHz (dBc/Hz)	-	-90	-100	**-102**
Integrated PLL jitter	-	200fs 0.001 to 10GHz	962 fs .001 to 10GHz	**394 fs 0.1 to 100MHz**

quadrature error up to 25 GHz. The measured PLL jitter is 392 fs (integrated from 100 kHz to 100 MHz) at 25 GHz while drawing 64 mW of power, 23 mW of which is consumed in the multiphase DCO. The DPLL occupies a total area of 0.1 mm^2.

REFERENCES

[1] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[2] B. Leibowitz *et al.*, "A 4.3 GB/s mobile memory interface with power-efficient bandwidth scaling," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 889–898, Apr. 2010.

[3] R. B. Staszewski and P. T. Balsara, "All-digital PLL with ultra fast settling," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 54, no. 2, pp. 181–185, Feb. 2007.

[4] J. Zerbe *et al.*, "A 5.6 Gb/s 2.4 mW/GB/s bidirectional link with 8 ns power-on," in *2011 Symp. VLSI Circuits Dig. Tech. Papers*, pp. 82–83.

[5] A. Goel, A. Rylyakov, H. Ainspan, and D. Friedman, "A compact 6 GHz to 12 GHz digital PLL with coupled dual-LC tank DCO," in *2010 Symp. VLSI Circuits Dig. Tech. Papers*, pp. 141–142.

[6] C.-C. Hung and S.-I. Liu, "A 40-GHz fast-locked all-digital phase-locked loop using a modified bang-bang algorithm," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 58, no. 6, pp. 321–325, Jun. 2011.

[7] A. Rylyakov *et al.*, "Bang-bang digital PLLs at 11 and 20GHz with sub-200fs integrated jitter for high-speed serial communication applications," in *2009 IEEE ISSCC Dig. Tech. Papers*, pp. 94–95, 95a.

[8] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May 2014.

[9] M. Ferriss, A. Rylyakov, J. A. Tierno, H. Ainspan, and D. J. Friedman, "A 28 GHz hybrid PLL in 32 nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1027–1035, Apr. 2014.

[10] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A mm-Wave quadrature VCO based on magnetically coupled resonators," in *2011 IEEE ISSCC Dig. Tech. Papers*, pp. 280–282.

[11] S. Rong and H. Luong, "Design and analysis of varactor-less interpolative-phase-tuning millimeter-wave LC oscillators with multiphase outputs," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1810–1819, Aug. 2011.

[12] M. Hekmat, D. K. Su, and B. A. Wooley, "A quadrature LO generator using bidirectionally-coupled oscillators for 60-GHz applications," in *Proc. 2011 Custom Integrated Circuits Conf.*, pp. 1–4.

[13] Y. M. Tousi, O. Momeni, and E. Afshari, "A 283-to-296GHz VCO with 0.76mW peak output power in 65nm CMOS," in *2012 IEEE ISSCC Dig. Tech. Papers*, pp. 258–260.

[14] U. Decanis, A. Chilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2943–2955, Dec. 2011.

[15] R. Navid, M. Hekmat, F. Aryanfar, J. Wei, and V. Gadde, "A 25GHz 100ns lock time digital LC PLL with an 8-phase output clock," in *2013 Symp. VLSI Circuits Dig. Tech. Papers*, pp. C196–C197.

[16] N. Da Dalt, "Linearized analysis of a digital bang-bang PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 55, no. 12, pp. 3663–3675, Dec. 2008.

[17] L. Romano, S. Levantino, C. Samori, and A. L. Lacaita, "Multiphase LC oscillators," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 53, no. 7, pp. 1579–1588, Jul. 2006.

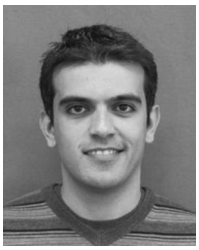
[18] A. Mirzaei, M. E. Heidari, R. Bagheri, and A. A. Abidi, "Multi-phase injection widens lock range of ring-oscillator-based frequency dividers," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.

[19] H.-C. Chang, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: theory and experiment," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 5, pp. 604–615, May 1997.

[20] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A 36mW/9mW power-scalable DCO in 55nm CMOS for GSM/WCDMA frequency synthesizers," in *2012 IEEE ISSCC Dig. Tech. Papers*, pp. 348–350.

[21] J. F. Bulzacchelli *et al.*, "A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, Dec. 2006.

[22] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk, and P. Wambacq, "A 42mW 230fs-jitter sub-sampling 60GHz PLL in 40nm CMOS," in *2014 IEEE ISSCC Dig. Tech. Papers*, pp. 366–367.



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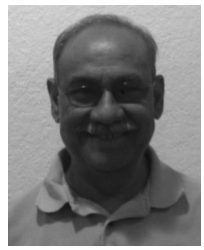

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