A 0.07-mm^2 162-mW DAC Achieving >65 dBc SFDR and < −70 dBc IM3 at 10 GS/s With Output Impedance Compensation and Concentric Parallelogram Routing

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***Abstract*— A digital-to-analog converter (DAC) with small-size non-cascoded current cells is proposed to achieve small area, low-power consumption, and high linearity over a wide bandwidth. An output impedance compensation (OIC) technique using a compensation resistor, implemented by a PMOS with code-dependent gate voltage control, is proposed to remedy the nonlinearity induced by the insufficient output impedance of the non-cascoded current cells. In addition, a proposed concentric parallelogram routing (CPR) technique, in which the subcells of each current cell are arranged such that they form a parallelogram shape with a common centroid, is used to reduce both the mismatch error and the routing-induced timing skew among the current cells. The DAC, implemented in a 28-nm CMOS process, achieves >65-dBc spurious-free dynamic range (SFDR) and < −70-dBc third-order intermodulation distortion (IM3) over the entire Nyquist bandwidth at 10 GS/s while consuming 162 mW from a single 1.1 V supply.**

***Index Terms*— Compensation, current steering, digital-to-analog converter (DAC), layout arrangement, output impedance, timing skew.**

I. Introduction

DIGITAL-TO-ANALOG converters (DACs) designed to directly synthesize the signals of advanced communication systems have gained increasing attention in recent years [1]–[3] due to the ability they provide to greatly simplify the system by removing the intermediate frequency stage. To maximize their operational advantage, such DACs should provide a high linearity over a wide bandwidth, while simultaneously consuming low power and small area. However, it is a critical challenge to realize such DACs due to the finite output impedance, mismatch error of the current cell, and transient-induced nonlinearity [4], which are described in the following.

The finite output impedance of the current cell induces distortion [5]–[7]. To reduce this distortion, the output impedance of the current cell is commonly enhanced by means of cascoded transistors [6], [7]. However, these transistors require additional voltage headroom. As a result, the power supply of the DAC must be increased and, hence, the power consumption of the device is also inevitably increased. The prior arts in [1] and [6] showed that the increase in the power consumption can be reduced by using a high-voltage supply for the current cells with cascoded transistors and a low-voltage supply for the remaining DAC circuits. In this work, an output impedance compensation (OIC) technique [8] is proposed instead to remedy the finite output impedance effect. Notably, the OIC technique enables the use of non-cascoded current cells. In addition, a compact layout and placement of the unit non-cascoded current cell for the more significant bits [4] are used to reduce the area and routing parasitic capacitance of the current cell array and, therefore, widen the bandwidth, relax the requirement of switch driver's driving ability, and reduce the power consumption. Furthermore, by removing the cascoded transistors, the DAC can be operated from a single low-voltage supply. Compared with the use of multiple supplies, the single low-voltage supply further reduces the power consumption; simplifies the signal grounding, wire routing on the PCB, and supply generation circuits; and eliminates the need for high-voltage components.

Current cells suffer from two types of mismatch errors, namely gradient mismatch error and random mismatch error [10]–[17]. Prior arts [10]–[13] have shown that the gradient mismatch error can be reduced by a careful arrangement of the current cells in the current cell array. However, the routing wires in [10]–[13] are complex and non-uniform and, therefore, induce a timing skew among the different current cells. The timing skew can be mitigated by increasing the switch driver's driving ability. However, this increases the switching current and power consumption. Therefore, in this work, a layout arrangement, referred to as concentric parallelogram routing (CPR) [8], is proposed to simultaneously reduce both the gradient mismatch error and the large-quantity-cell routing-induced timing skew. The other mismatch error of current cells, namely random mismatch error, can be suppressed by either dynamic element matching (DEM) [14] or calibration circuits [15]–[17]. Of these two methods, DEM has a lower circuit overhead and complexity and is hence chosen in this work. The gradient mismatch error is already substantially

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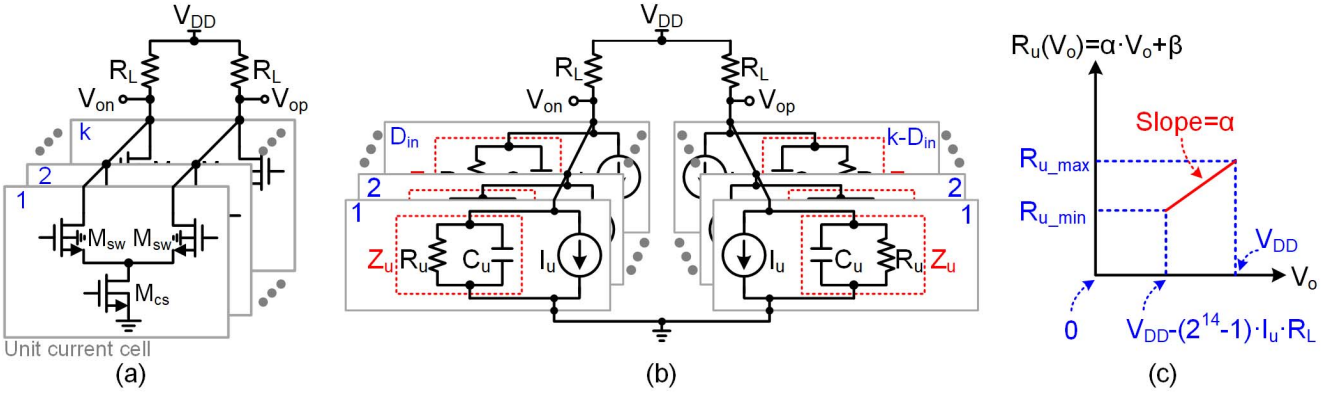

Fig. 1. Analysis of finite output impedance. (a) Simplified current cell array of 14-bit DAC. (b) Equivalent model of 14-bit DAC. (c) First-order function modeling of R_u.

reduced by the proposed CPR technique. Hence, in the proposed DAC, DEM is used only to randomize the random mismatch error. Consequently, the elevated noise floor caused by DEM is mitigated.

DACs suffer from transient-induced nonlinearity due to the previous-signal-dependent DAC output transition [4], [17]. Compared with current cells with cascoded transistors, non-cascoded current cells are more susceptible to transient-induced nonlinearity due to the larger drain voltage change of the current source during DAC output transition. Accordingly, in this work, the digital return-to-zero (DRZ) method [4], [17], which inserts a zero differential output between two adjacent signals, is used to prevent the DAC output transition from the influence of the previous signal, thereby reducing the transient-induced nonlinearity. Although the use of the DRZ method causes up to 6-dB output power loss in the first Nyquist zone, it results in both a flat signal amplitude over a wide bandwidth and an improved in-band spurious-free dynamic range (SFDR) performance [4].

As described above, the DAC proposed in this work utilizes the OIC technique to relax the requirement on the DAC output impedance and the CPR technique to reduce the gradient mismatch error and routing-induced timing skew. In addition, DEMDRZ [4] is used to further suppress the mismatch error of the current cell and reduce the transient-induced nonlinearity. Through the use of these techniques, together with small-size non-cascoded current cells, the DAC achieves high linearity over wide bandwidth, low-power consumption, small area, and the ability to use a single low-voltage supply. The remainder of this article is organized as follows. Section II presents a more accurate analysis of the relationship between the DAC linearity and the finite output impedance compared with the prior analysis. The basic concepts of the proposed OIC technique and its design tradeoffs are then introduced. Section III describes the circuit implementation of the proposed 14-bit DAC using the OIC and CPR techniques. Section IV presents and discusses the measurement results and comparisons. Finally, Section V presents brief concluding remarks.

II. OIC Architecture

Fig. 1(a) shows the simplified current cell array of a DAC with k unit current cells, where $k = 2^{14} - 1$ for a 14-bit DAC and the current sources (M_{cs}) are switched to either V_{op} or V_{on} depending on the digital input code. To illustrate the finite output impedance effect and the concept of the proposed OIC technique, Fig. 1(b) shows the equivalent model of the DAC with a digital input code D_{in} ($0 \le D_{in} \le 16383$). Note that I_u and Z_u are the current and output impedance of the unit current cell, respectively. As shown, Z_u is modeled by the parallel connection of a resistor R_u and capacitor C_u. Using this equivalent model of the DAC, Section II-A analyzes the finite output impedance of the current cell at low frequencies. Section II-B then elaborates the D_{in}-dependent compensation resistor, $R_{cp}(D_{in})$, used in the proposed OIC architecture. Section II-C examines the effect of the finite output impedance at higher frequencies on $R_{cp}(D_{in})$. Finally, Section II-D illustrates the approximation and process-voltage-temperature (PVT) variation of $R_{cp}(D_{in})$.

A. Finite Output Impedance at Low Frequencies

At low frequencies, the effect of C_u is negligible and, hence in examining the finite output impedance, only R_u needs be considered. According to prior arts [6], [17], $R_u(V_o)$ can be treated as a constant regardless of the output voltage V_o, where V_o is either V_{op} or V_{on} depending on whether M_{cs} is connected to V_{op} or V_{on}, respectively. However, due to the channel-length modulation effect of M_{cs} in saturation region, R_u actually reduces as V_o decreases. According to the data of foundry, the relationship between R_u and V_o can be approximated by the first-order function $R_u(V_o) = \alpha \cdot V_o + \beta$, where α is the slope of $R_u(V_o)$, in which R_u reaches its maximum value, R_{u_max}, and minimum value, R_{u_min}, at V_o equal to V_{DD} and $V_{DD} - (2^{14} - 1) \cdot I_u \cdot R_L$, respectively, as shown in Fig. 1(c).

Fig. 2 shows the ideal and nonideal transfer curves of the DAC output, V_{DAC}, versus D_{in} based on the equivalent DAC model presented in Fig. 1(b) and the first-order function modeling of R_u shown in Fig. 1(c). For an infinite value of R_u, the transfer curve of V_{DAC} versus D_{in} is linear, as shown by the solid line in Fig. 2. However, for a finite and output-voltage-dependent value of R_u, V_{DAC} varies nonlinearly with D_{in} and causes distortion, as shown by the dashed line in Fig. 2. According to the derivation in [5] and the first-order function modeling of R_u, for a full output voltage swing of

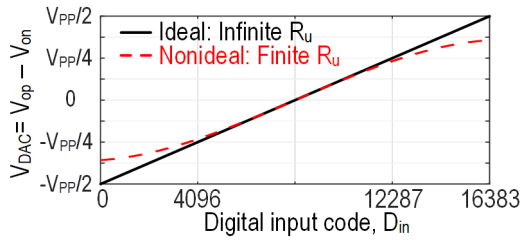

Fig. 2. Transfer curves of DAC output, V_{DAC}, versus digital input code, D_{in}, where V_{PP} is the peak-to-peak voltage swing of DAC.

the DAC, the third-order distortion can be expressed as

$$\mathrm{HD3} \approx 20 \cdot \log_{10}\left|\frac{R_L^2 \cdot k^2 \cdot (1-\alpha \cdot I_u)}{\{4 \cdot [\alpha \cdot (V_{\mathrm{DD}} - k \cdot I_u \cdot R_L) + \beta]\}^2}\right| = 20 \cdot \log_{10}\left|\frac{R_L^2 \cdot k^2 \cdot (1-\alpha \cdot I_u)}{\{4 \cdot R_{u\_\mathrm{min}}\}^2}\right|. \quad (1)$$

Compared with the analysis of prior arts based on constant R_u[5], [6], [17], the first-order function modeling of R_u described above leads to a more accurate expression for the third-order distortion, HD3. Besides HD3, other distortion components can also be derived according to the modeling of the finite output impedance in Fig. 1; however, HD3 dominates the SFDR for a differential DAC [5]. Fig. 3 compares the results obtained from (1) for the SFDR with different α and R_{u_min} with the equivalent results obtained from behavioral simulations. As can be seen, the SFDR is degraded when R_{u_min} decreases or α increases.

B. Operation Principle of the Proposed OIC

As shown in Fig. 4(a), the proposed OIC technique uses a D_{in}-dependent compensation resistor $R_{\mathrm{cp}}(D_{\mathrm{in}})$, connected between nodes V_{op} and V_{on}, to remedy the SFDR degradation caused by finite output impedance. The current induced by $R_{\mathrm{cp}}(D_{\mathrm{in}})$ changes the current through the load resistors, R_L, and hence compensates the transfer curve of the nonideal V_{DAC}. With $\alpha = 80$ MΩ/V, Fig. 4(b) shows the transfer curves of the nonideal V_{DAC} for $R_{u\_\mathrm{min}} = 20$ MΩ, and $R_{u\_\mathrm{min}} = 35$ MΩ, respectively. The required compensation amount, ΔV_{DAC}, is equal to the difference between the nonideal V_{DAC} and the compensated V_{DAC}. Compared with the nonideal V_{DAC} with a large R_u, the nonideal V_{DAC} with a small R_u is more nonlinear, and hence a larger ΔV_{DAC} is required. The resistance of the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ required to achieve the compensated V_{DAC} can be approximated as follows:

$$R_{\mathrm{cp}}(D_{\mathrm{in}}) \approx \frac{\text{Nonideal } V_{\mathrm{DAC}}(D_{\mathrm{in}})}{\Delta V_{\mathrm{DAC}}(D_{\mathrm{in}})} \cdot 2 \cdot R_L. \quad (2)$$

Fig. 4(c) shows the calculated ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ versus D_{in}, which are U-shaped, for $R_{u\_\mathrm{min}} = 20$ MΩ, and 35 MΩ, respectively. The resistance of the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ for $R_{u\_\mathrm{min}} = 20$ MΩ is less than that for $R_{u\_\mathrm{min}} = 35$ MΩ to get more ΔV_{DAC}.

C. Finite Output Impedance at High Frequencies

Fig. 5(a) shows the frequency response of Z_u, which is modeled by the parallel connection of R_u and C_u. Since the effect of C_u at low frequencies is negligible, the analyses

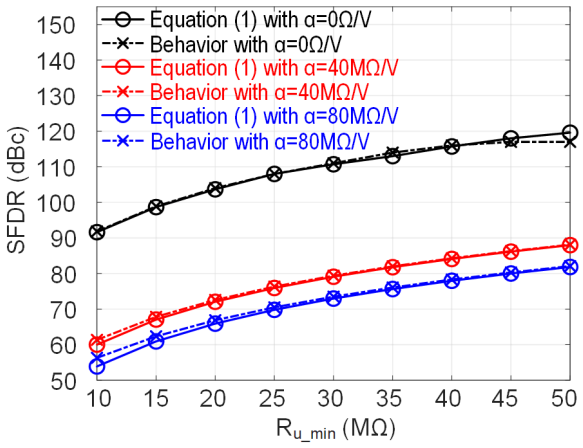

Fig. 3. SFDR versus R_{u_min} with different α.

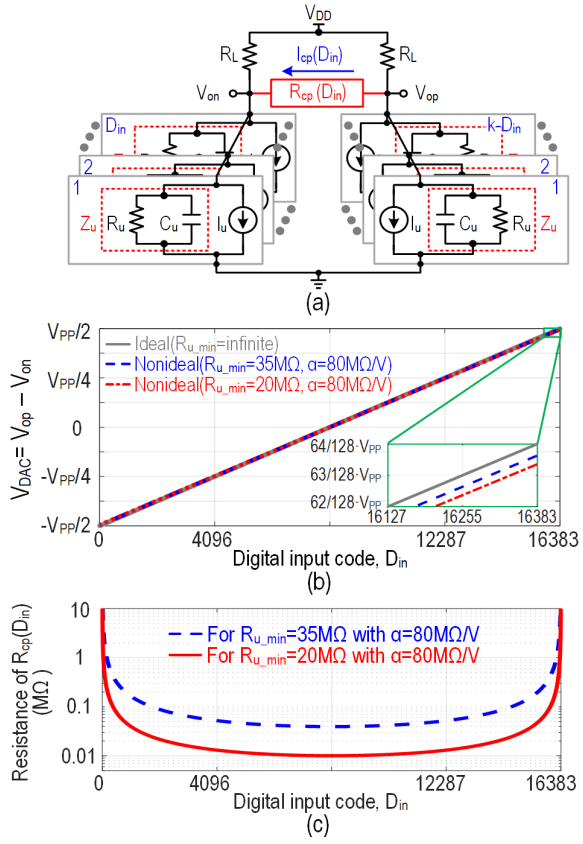

Fig. 4. Proposed OIC technique. (a) D_{in}-dependent compensation resistor, $R_{\mathrm{cp}}(D_{\mathrm{in}})$. (b) Transfer curves of ideal V_{DAC}, and nonideal V_{DAC} versus D_{in}. (c) Resistance curves of ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ for $R_{u\_\mathrm{min}} = 20$ MΩ and $R_{u\_\mathrm{min}} = 35$ MΩ.

presented in Sections II-A and II-B above assume that Z_u is equal to R_u. However, at higher frequencies, the magnitude of Z_u is decreased by C_u. To illustrate the effect of C_u on V_{DAC} in the time domain, Fig. 5(b) shows the V_{DAC} transition over a single sampling period for three different cases, namely, infinite R_u with zero C_u, finite R_u with zero C_u, and finite R_u with non-zero C_u. Note that the sampling period, T_s, is divided into two phases, namely the DRZ phase and the signal

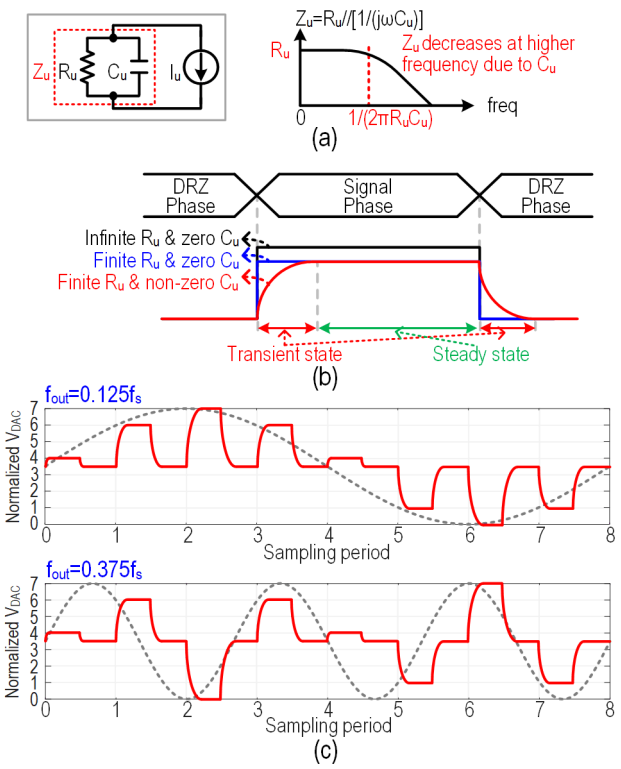

Fig. 5. (a) Frequency response of finite output impedance of unit current cell, Z_u. (b) V_{DAC} transition waveforms for infinite R_u with zero C_u, finite R_u with zero C_u, and finite R_u with non-zero C_u. (c) Normalized V_{DAC} of illustrative a 3-bit DAC example with different output signal frequencies, $f_{\mathrm{out}} = 0.125 f_s$ and $f_{\mathrm{out}} = 0.375 f_s$.

phase. As can be seen, the finite R_u causes a steady-state error, while the non-zero C_u causes a transient-state error. Since the transient state contains high-frequency components, and the magnitude of Z_u reduces at high frequencies, V_{DAC} is more nonlinear during the transient state than during the steady state. In this work, to reduce the effect of C_u on the resistance of the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$, a small-size unit non-cascoded current cell is used and placed at the 5th bit from the least significant bit. Therefore, when using OIC, the SFDR is greater than 70 dBc according to circuit-level simulations, while the equivalent C_u of the small-size unit non-cascoded current cell is less than 0.1 fF. Fig. 5(c) shows the V_{DAC} transitions of a 3-bit DAC example with different output signal frequencies (i.e., $f_{\mathrm{out}} = 0.125 f_s$ and $f_{\mathrm{out}} = 0.375 f_s$). The DRZ phase prevents the V_{DAC} transition of the present sampling period from the influence of the previous period. In other words, the V_{DAC} transition of the present sampling period is dependent only on the present D_{in} regardless of f_{out}. As a result, the required resistance of the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ is nearly independent of f_{out}. Fig. 6 shows the simulated SFDR versus f_{out} for a 14-bit DAC with and without the proposed OIC technique, respectively. In the simulation, DEMDRZ is enabled and the resistance of $R_{\mathrm{cp}}(D_{\mathrm{in}})$ is not changed for different f_{out}. The results confirm that the SFDR improvement yielded by the OIC technique is nearly independent of f_{out} over the entire Nyquist band at 10 GS/s.

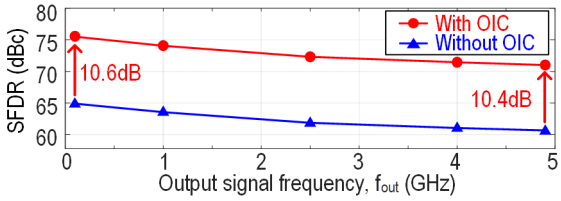

Fig. 6. Simulated SFDR versus f_{out} for 14-bit DAC with and without OIC.

D. Approximation of $R_{cp}(D_{in})$

The ideal U-shaped $R_{\mathrm{cp}}(D_{\mathrm{in}})$ can be approximated by a PMOS biased with a code-dependent gate voltage $V_G(D_{\mathrm{in}})$, as shown in Fig. 7(a). Fig. 7(b) shows two illustrative $V_G(D_{\mathrm{in}})$ voltage plots, namely, two-level $V_G(D_{\mathrm{in}})$ and three-level $V_G(D_{\mathrm{in}})$. For two-level $V_G(D_{\mathrm{in}})$, the PMOS operates in the cutoff region with a large resistance to reduce the approximation error when D_{in} is less than 512 or greater than 15871. By contrast, when D_{in} is greater than 512 and less than 15871, the PMOS operates in the triode region to approximate the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$. Based on Fig. 4(a) and (2), the thresholds of D_{in} and the PMOS resistance in the triode region can be chosen in such a way to minimize the approximation error, namely the difference between V_{DAC} compensated by PMOS with two-level $V_G(D_{\mathrm{in}})$ and V_{DAC} compensated by ideal R_{cp}. Fig. 7(c) shows the simulated maximum absolute value of the approximation error versus the PMOS resistance with different thresholds of D_{in} for the PMOS with two-level $V_G(D_{\mathrm{in}})$. It was found that the maximum absolute value of the approximation error is minimized when the PMOS resistance is equal to 30 kΩ and thresholds of D_{in} are set as 512 and 15871. Fig. 7(d) shows the resistance of the ideal $R_{\mathrm{cp}}(D_{\mathrm{in}})$ and the approximated resistance of the PMOS with two-level $V_G(D_{\mathrm{in}})$ in this work. Although $V_G(D_{\mathrm{in}})$ is constant for D_{in} between 512 and 15871, the PMOS resistance still changes slightly with V_{op} and V_{on}, thus better fitting the ideal resistance $R_{\mathrm{cp}}(D_{\mathrm{in}})$ and reducing the approximation error, which leads in turn to an additional improvement of around 2 dB in the SFDR in this work. In addition, the PMOS is designed as small as possible. Therefore, the additional parasitic capacitance introduced by the PMOS at the output node is only 0.15 fF. This value is much smaller than that of the current cell array. Consequently, the additional parasitic capacitance of the PMOS at the output node has only a negligible impact on the SFDR. Fig. 7(e) shows the approximation error versus D_{in} with the approximated $R_{\mathrm{cp}}(D_{\mathrm{in}})$ obtained using the PMOS with two-level $V_G(D_{\mathrm{in}})$ and PMOS with three-level $V_G(D_{\mathrm{in}})$, respectively. It is seen that the approximation error obtained using the approximated $R_{\mathrm{cp}}(D_{\mathrm{in}})$ is smaller than that obtained without the approximated $R_{\mathrm{cp}}(D_{\mathrm{in}})$. According to the results presented for three-level $V_G(D_{\mathrm{in}})$ in Fig. 7(b), (d), and (e), a better $R_{\mathrm{cp}}(D_{\mathrm{in}})$-fit PMOS resistor for an improved linearity can be obtained when $V_G(D_{\mathrm{in}})$ has more levels. However, two-level $V_G(D_{\mathrm{in}})$ is sufficient to achieve SFDR better than 70 dBc. Hence, for reasons of simplicity, two-level $V_G(D_{\mathrm{in}})$ was chosen for implementation in this work. Fig. 8 shows the simulated SFDR improvement versus the variation of R_{cp}/Z_u caused by PVT variation. It is seen that even with ±40%

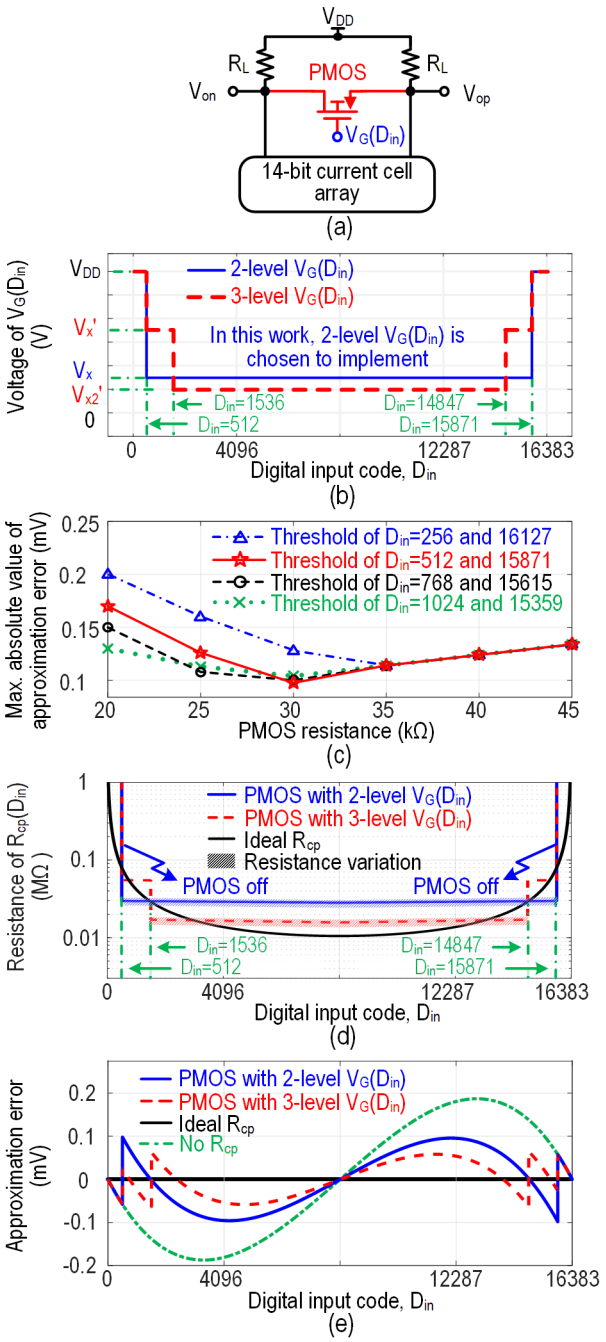

Fig. 7. (a) PMOS biased with code-dependent gate voltage, $V_G(D_{\text{in}})$. (b) Illustrative two-level $V_G(D_{\text{in}})$ and three-level $V_G(D_{\text{in}})$. (c) Simulated maximum absolute value of approximation error versus PMOS resistance with different thresholds of D_{in} for the PMOS with two-level $V_G(D_{\text{in}})$. (d) Approximated resistances of PMOS with two-level $V_G(D_{\text{in}})$ and three-level $V_G(D_{\text{in}})$. (e) Approximation error versus D_{in} with approximated $R_{\text{cp}}(D_{\text{in}})$ by PMOS with two-level $V_G(D_{\text{in}})$ and PMOS with three-level $V_G(D_{\text{in}})$.

variation of R_{cp}/Z_u, the simulated SFDR improvement is still larger than 5 dB by using the simple PMOS-based $R_{\text{cp}}(D_{\text{in}})$ with two-level $V_G(D_{\text{in}})$.

III. DAC With OIC and CPR Techniques

Fig. 9 shows a block diagram of the proposed 14-bit DAC architecture. A higher partition level of segmentation results in lower implementation area, including the current cells, switch drivers, and DEM [14]. Therefore, in this work, the digital

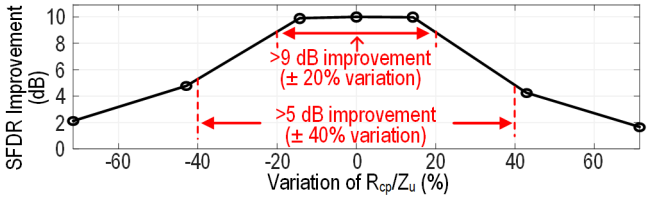

Fig. 8. Simulated SFDR improvement versus variation of R_{cp}/Z_u caused by PVT variation.

input code, D_{in}, is segmented into three unary MSB bits, three unary upper LSB (ULSB) bits, three unary LSB bits, and five binary lower LSB (LLSB) bits. The upper 9 bits and lower 5 bits pass through the DEM and delay equalizer, respectively, and enter the DRZ circuit. Depending on the DRZ outputs, the switch drivers control the switch pairs of the current cells in such a way as to generate the DAC output. In addition, during the DRZ phase, the DRZ turns ON all of the switch pairs of the current cells to produce a zero differential DAC output, i.e., $V_{\text{DAC}} = V_{\text{op}} - V_{\text{on}} = 0$.

Section III-A introduces the sizing and placement of the unit current cell in the proposed DAC. Section III-B describes the proposed CPR technique used to reduce the gradient mismatch error. Finally, Section III-C introduces the two-level $V_G(D_{\text{in}})$ generator used in the proposed OIC technique.

A. Compact Layout of Unit Current Cell

Fig. 10 shows the circuit diagram of the current cell array, where the unit current cell is used for the most significant bit of the LLSB, i.e., LL_5, rather than the least significant bit of the LLSB, i.e., LL_1, in order to reduce the total layout area of the current cell array. Conventional unit current cell comprises switch pair transistors M_{SW}, a cascoded transistor M_{CAS}, a current-source transistor M_{CS}, and a long metal interconnect [4]. However, the present non-cascoded current cells omit M_{CAS}. Furthermore, to shorten the metal interconnect and reduce the parasitic capacitance between M_{SW} and M_{CS}, M_{CS} is placed together with its own M_{SW} in a small area. To make the layout of the unit current cell compact, the width of M_{CS} is designed as the minimum layout width of two minimum-size M_{SW} plus the distance between them, as shown in the bottom-right of Fig. 10. The length of M_{CS} is obtained from the device mismatch data and the required full-scale DAC output current. The LSB (L_1–L_7), ULSB (UL_1–UL_7) and MSB (M_1–M_7) current cells are formed by the parallel connection of 2, 16, and 128 unit current cells, respectively. In addition, the LL_4 and LL_3 current sources are formed via the series connection of 2 and 4 M_{CS}, respectively. For the LL_2 and LL_1 bits, the width of the series-connected four M_{CS} is divided by 2 and 4, respectively.

Fig. 11 shows the simulated SFDR of the proposed DAC versus the random mismatch of the current source with and without DEM, respectively, where the random mismatch of the current source is modeled as a Gaussian distribution with standard deviation (σ). It is noted that each SFDR is the worst case in the 3σ range (i.e., 99.7% yield) over 10 000 Monte-Carlo simulation runs. As can be seen, for an SFDR larger than

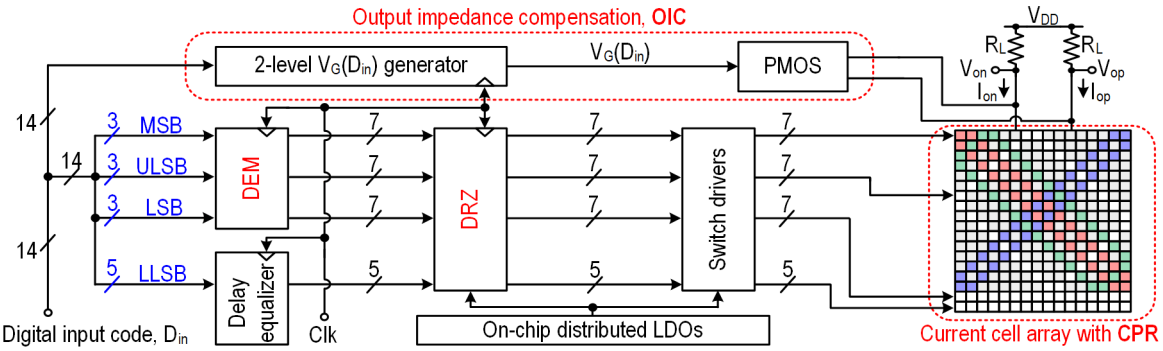

Fig. 9. Architecture of the proposed DAC with CPR and OIC techniques.

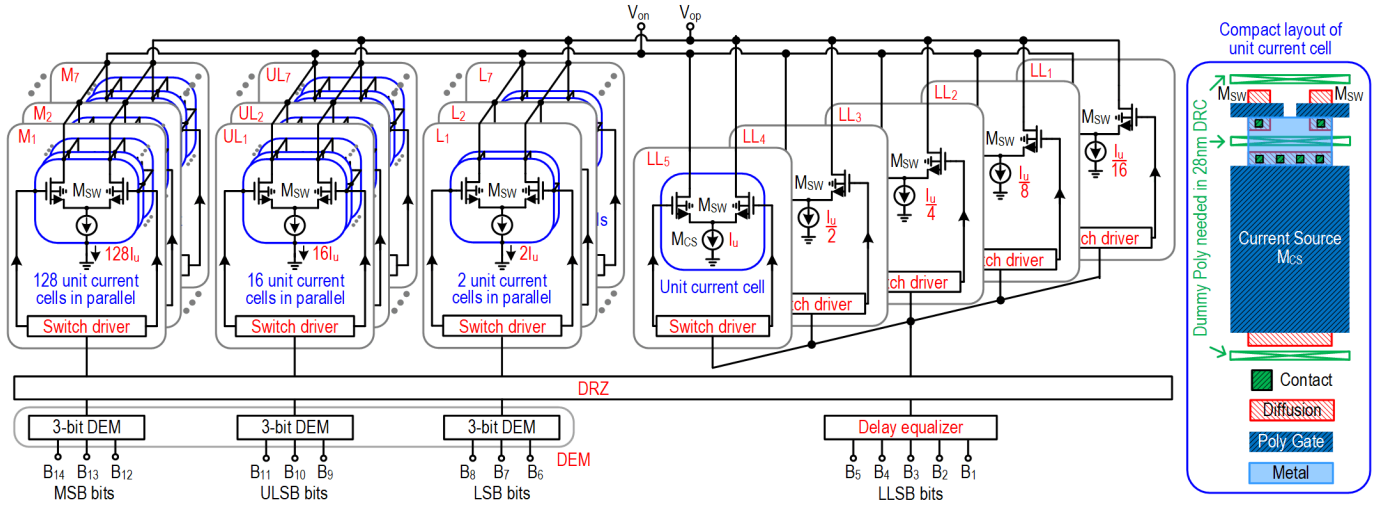

Fig. 10. Circuit diagram of current cells with 3 + 3 + 3 + 5 segmentation.

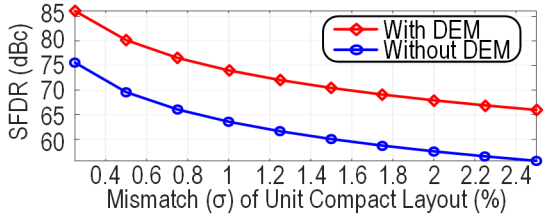

Fig. 11. Behavior simulation of DEM in the proposed DAC. (Note that current source mismatch of 1.6% (σ) is chosen for unit current cell).

70 dBc, the allowable σ of the random mismatch of current-source for the unit current cell without DEM is around 0.45%. However, when DEM is applied, the permissible value of σ increases to 1.6%. As described above, the M_{CS} length can be calculated from the device mismatch data. For 1.6% (σ) random mismatch, M_{CS} for the LL_5 bit is sized as follows: width = 0.44 μm and length = 0.85 μm, while M_{SW} is sized as width = 0.1 μm and length = 0.05 μm. As a result, the layout area of the unit current cell is around 0.8 μm^2.

B. Concentric Parallelogram Routing

The DEM reduces the distortion induced by the mismatch, including both the random mismatch and the gradient mismatch. However, it raises the noise floor. To mitigate this problem, this work reduces the gradient mismatch through a careful design of the layout arrangement of the current cells. The proposed DAC incorporates seven MSB (M_1–M_7) current cells, where each cell is divided into 32 identical subcells as shown in Fig. 12(a) and each subcell contains four unit current cells. Fig. 12(b) shows a simple layout arrangement of the seven current cells. The routing for the interconnection of the subcells within each MSB current cell is uniform. Hence, no timing skew occurs between the different MSB current cells. However, the reduction of the gradient mismatch error produced by this arrangement of the current cells is insufficient for high-resolution DACs. Fig. 12(c) thus shows an alternative layout arrangement based on the well-known Q^2 random walk method [10]. Compared with the simple arrangement in Fig. 12(b), the random walk arrangement has a common centroid and, therefore, achieves a lower gradient mismatch error. However, the total routing lengths used to connect the subcells of each MSB cell are different. Furthermore, the lengths of the routings used to connect any two adjacent subcells of the same MSB current cell are not the same. Hence, a timing skew is induced between the current cells.

To reduce the gradient mismatch error, while simultaneously equalizing the routing-induced delay, this article proposes the CPR arrangement shown in Fig. 13, in which the 32 subcells of each MSB current cell are arranged in the form of a

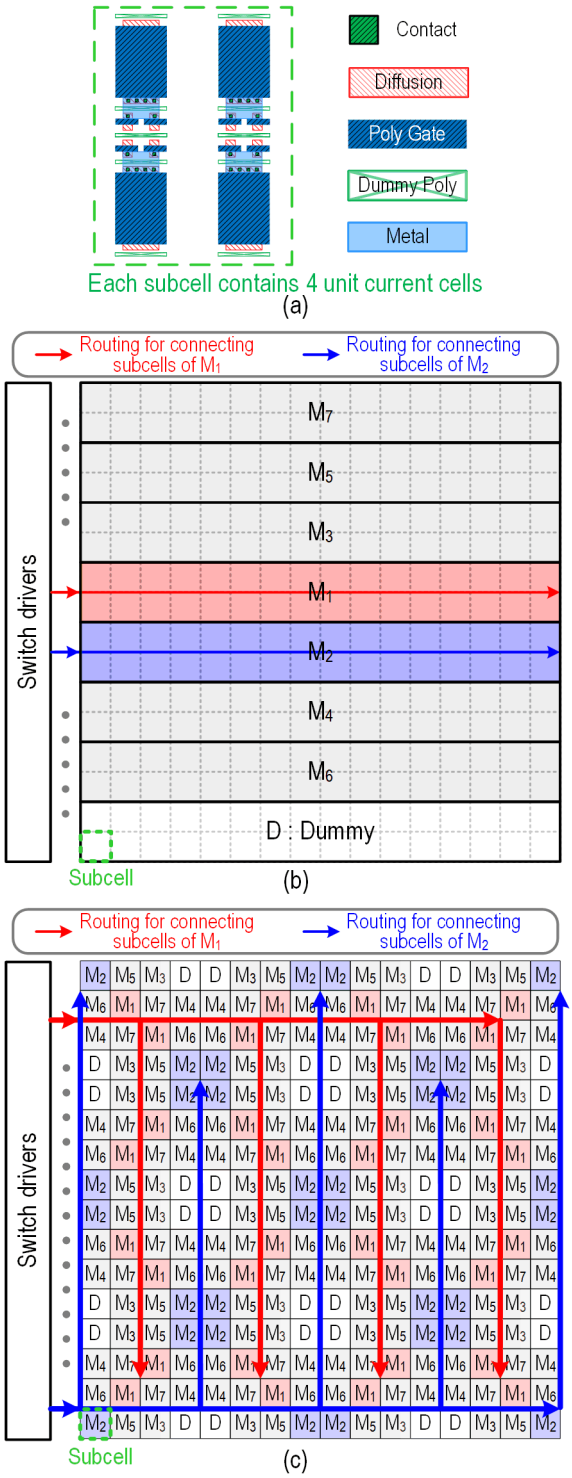

Fig. 12. Layout arrangements of seven current cells (note each cell has 32 subcells). (a) Illustration of a subcell, (b) simple layout (no common centroid), and (c) Q^2 random walk layout (common centroid).

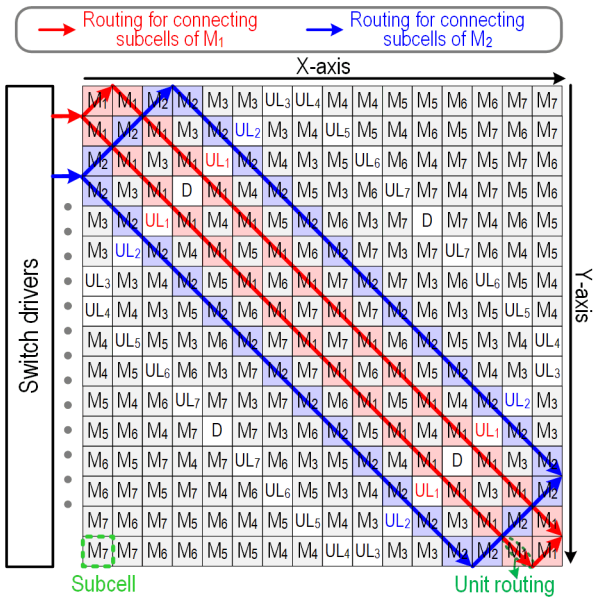

Fig. 13. Proposed CPR technique for seven MSB current cells and seven ULSB current cells.

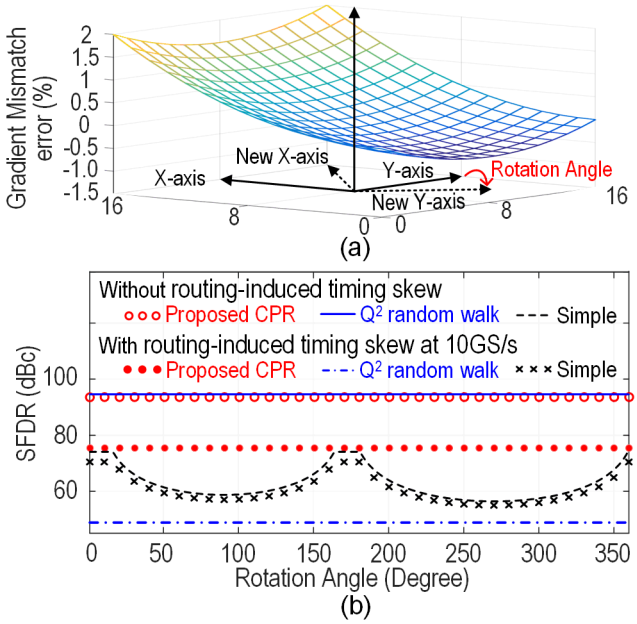

Fig. 14. (a) Gradient mismatch error profile with joint error distribution (rotation angle of profile is zero degree). (b) Simulated SFDR versus rotation angle for different current cell array layouts.

parallelogram evenly distributed over the x- and y-axes. Since the parallelograms of the seven MSB current cells are concentric, the gradient mismatch error among the cells is reduced. Furthermore, to mitigate the mismatch between the MSB and ULSB segments, each ULSB current cell, which is divided into four identical subcells, is allocated within the layout array of the MSB current cells. To deliver the switch control signal from the output of the switch driver to the 32 subcells of each MSB current cell, the routing wires used to interconnect the 32 subcells are arranged in the form, as shown in Fig. 13. As shown, each MSB current cell has two routing paths from the vertex (i.e., the output of the switch driver) to the diagonal vertex of the parallelogram. The number of connected subcells in each routing path of every MSB current cell is, therefore, always equal to 16. Moreover, the length of the routing for connecting any two adjacent subcells of the same MSB current cell is always equal to the length of the diagonal of the subcell. Given the routing path arrangement shown in Fig. 13, the delay of the switch control signal from the output of the switch driver to the subcells in the same column of each MSB current

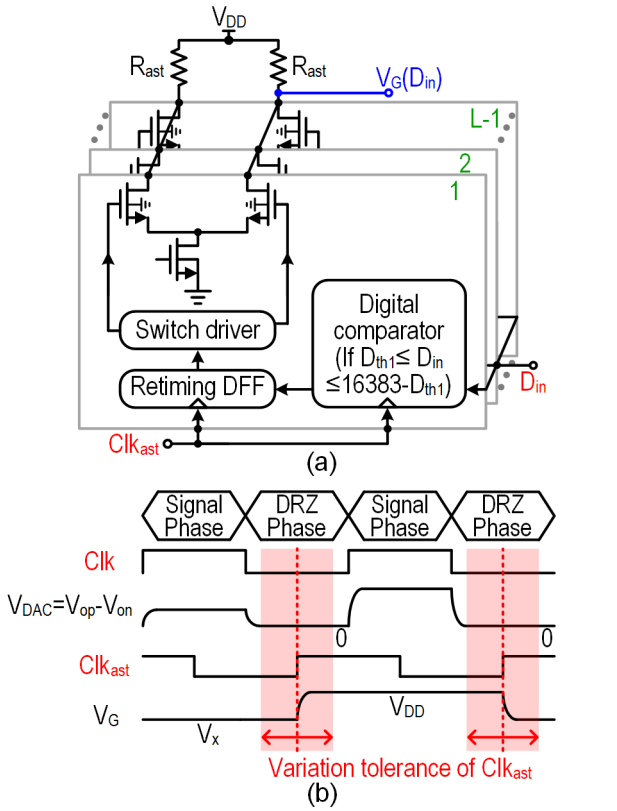

Fig. 15. (a) Circuit implementation of L-level $V_G(D_{\text{in}})$ generator for OIC. (b) Time-domain waveform of L-level $V_G(D_{\text{in}})$ generator with $L = 2$.

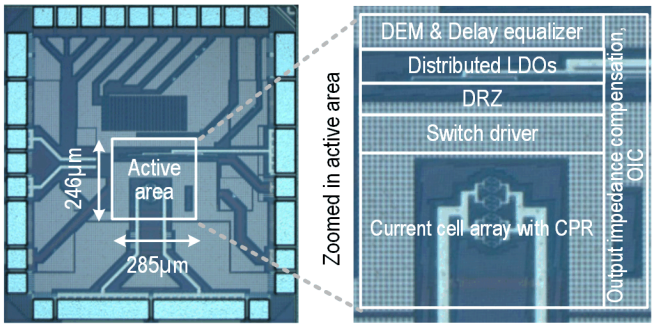

Fig. 16. Chip photograph.

cell is equal since the switch control signal passes through the same routing length and the same number of subcells. Consequently, the routing-induced timing skew error among the different MSB cells is greatly reduced.

In accordance with [4], [11], and [13], the gradient mismatch quantity of the proposed CPR design was verified by MATLAB simulations using a joint error distribution (50% linear +50% quadratic). The maximum gradient mismatch was equal to 2% and provided sufficient tolerance to maintain a high yield, as shown in Fig. 14(a). A rotation angle parameter was used to simultaneously rotate the x- and y-axes of the gradient mismatch profile in the clockwise direction in order to model the error distribution under various chip allocations within a silicon wafer. Fig. 14(b) shows the simulated SFDR versus the rotation angle for the three current cell array arrangements described above (i.e., simple, random walk and CPR). When the routing-induced timing skew is ignored in every case, the simulated SFDR of the proposed CPR and that of Q^2 random walk are comparable. When the routing-induced timing skew at 10 GS/s is introduced, the simulated SFDR of the Q^2 random walk layout degrades to less than 50 dBc. However, that of the proposed CPR remains higher than 70 dBc.

C. Two-Level $V_G(D_{in})$ Generator

Fig. 15(a) shows the circuit implementation of the L-level $V_G(D_{\text{in}})$ generator, where $L = 2$ is chosen in this work since two-level $V_G(D_{\text{in}})$ is sufficient to achieve SFDR better than 70 dBc. As shown, the L-level $V_G(D_{\text{in}})$ generator with $L = 2$ is composed of a digital comparator with a threshold of $D_{\text{th1}} = 512$, a retiming DFF, a switch driver, and a current cell. The assistant clock Clk_{ast}, for the $V_G(D_{\text{in}})$ generator is used to determine the timing of the V_G transition through the retiming DFF. To prevent V_{DAC} from V_G transition-induced non-linearity, the V_G transition point is located at the middle of the DRZ phase, as shown in Fig. 15(b). With this timing arrangement, the variation tolerance of the rising edge of Clk_{ast} is as much as ±25% of sampling period.

IV. Measurements and Comparisons

The DAC, which was fabricated in a 28-nm CMOS process, has an active area of 285 × 246 μm^2, as shown in Fig. 16. The DAC output current was converted to a voltage through an off-chip 50-Ω resistive differential load and coupled to a spectrum analyzer through a balun [4], [17], [18]. Unless otherwise specified, all of the following measurements were performed with DEM ON and a full-scale output current of 16 mA, which corresponds to a 400-mV peak-to-peak output voltage swing and generates a sine wave of −10 dBm due to the intrinsic DRZ effect. In addition, in this work, the output power of the DAC with finite output impedance is about 0.09 dB smaller than that of a DAC with infinite output impedance. Although the proposed OIC technique cannot recover the degradation of the output power caused by the finite output impedance, it can linearize the resultant nonlinearity.

Fig. 17(a) shows the measured spectra with a 117 MHz signal clocked at 10 GS/s. When DEM is OFF, the measured SFDR is 62.2 dBc, which is limited mainly by the random mismatch error of the current cell. When DEM is ON but OIC is not applied, the measured SFDR improves to 65.2 dBc and is limited by the finite output impedance effect. When the OIC is enabled, the measured SFDR further improves to 75.2 dBc. Fig. 17(b) shows the measured spectra for a 4570 MHz signal clocked at 10 GS/s. When DEM is OFF, the measured SFDR is 51.0 dBc, which is mainly limited by the random skew variation from the switch drivers. When DEM is ON but OIC is not applied, the measured SFDR improves to 57.8 dBc and is limited by the finite output impedance effect. When OIC is enabled, the measured SFDR further improves to 65.5 dBc. The power attenuation of the 4570 MHz signal is caused by the pad and PCB parasitics, and the balun insertion loss. Fig. 18 shows the measured output power versus output signal frequency, f_{out}, with and without the de-embedded power attenuation, respectively. As shown in Fig. 19(a) and (b), the measured third-order inter-modulation distortion (IM3), which was tested at signal frequencies of 4570 and 4648 MHz

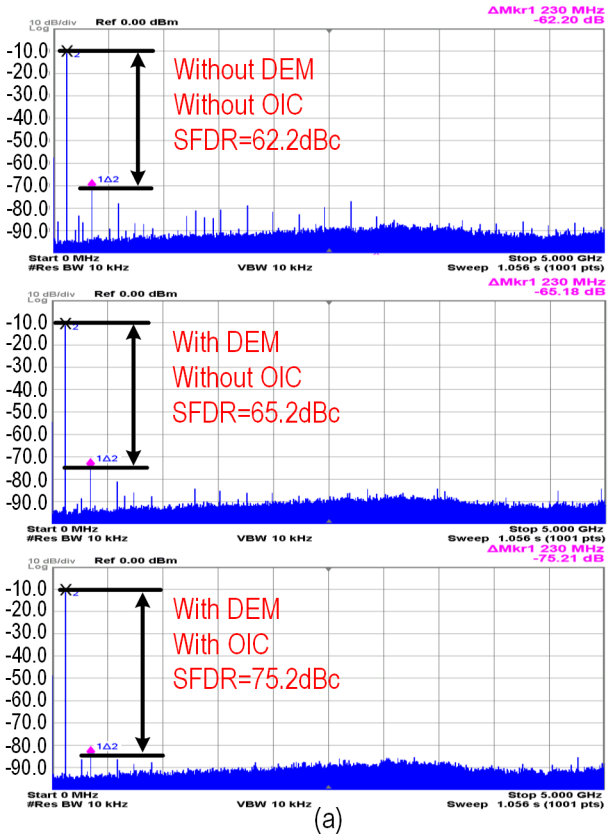

Fig. 17. Measured spectra for (a) SFDR with 117 MHz signal clocked at 10 GS/s and (b) SFDR with 4570 MHz signal clocked at 10 GS/s.

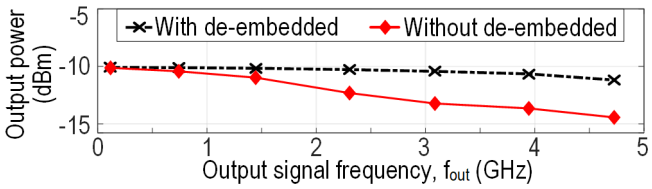

Fig. 18. Measured output power versus output signal frequency, f_{out}.

clocked at 10 GS/s, improved from −60 to −70.8 dBc when the OIC technique was enabled. In other words, the OIC technique effectively remedies the finite output impedance effect. Fig. 20(a) and (b) summarizes the measured SFDR and IM3 versus output signal frequency, f_{out}, clocked at 10 GS/s, respectively. The results show that the measured SFDR and IM3 improved by at least 7.7 and 10 dB, respectively, at 10 GS/s when the OIC technique is enabled. For the 4570 MHz signal clocked at 10 GS/s, Fig. 17(b) shows that the measured HD3 improvement with OIC is around 10 dB. Since both the power of HD3 and the power of the output signal are attenuated, another spur at low frequency becomes larger than HD3, as shown in the bottom-right corner of Fig. 17(b). As a result, the measured SFDR improvement with OIC is actually only 7.7 dB rather than 10 dB. In addition, Fig. 20(c) shows the measured noise spectral density (NSD) of signals clocked at 10 GS/s. As shown, the NSD varies from −161 to −158 dBm/Hz over the 5-GHz Nyquist bandwidth range.

Fig. 21 shows the measured SFDR versus the temperature, supply voltage, and full-scaled output current (with the other

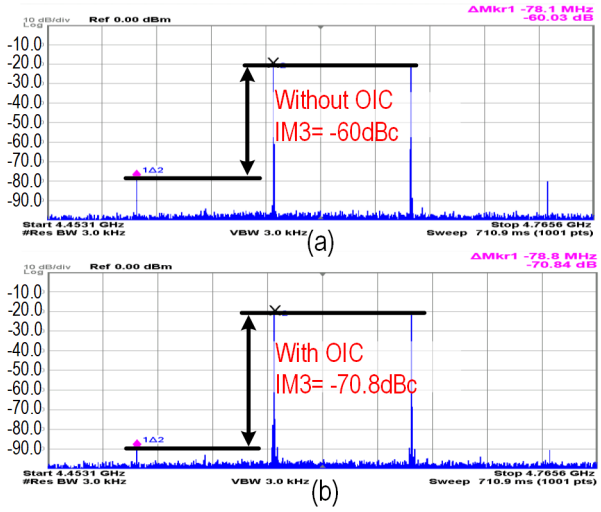

Fig. 19. Measured spectra for IM3 with signal frequencies of 4570 and 4648 MHz clocked at 10 GS/s. (a) Without OIC. (b) With OIC.

conditions unchanged). When the temperature is increased from 10 °C to 40 °C with a supply voltage of 1.1 V and a full-scale output current of 16 mA, the measured SFDR improvement with OIC is larger than 7.9 dB. In addition, when the supply voltage is increased from 1.07 to 1.13 V at a temperature of 25 °C and a full-scale output current of 16 mA, the measured SFDR improvement with OIC is greater than 6.6 dB. Finally, when the full-scale output current is increased from 14.5 to 17.5 mA with a constant temperature of 25 °C and

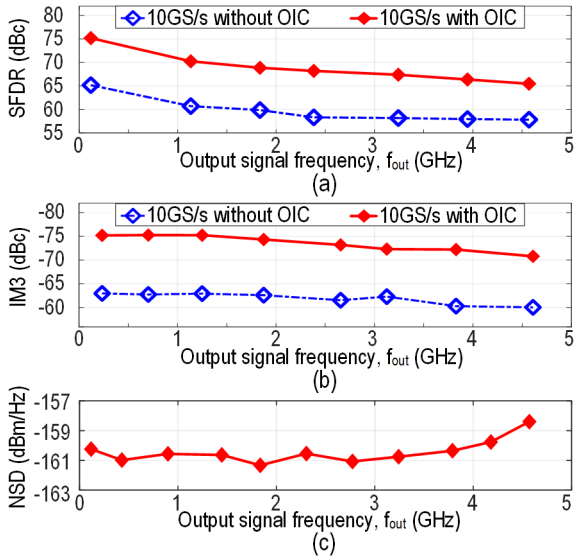

Fig. 20. (a) SFDR, (b) IM3, and (c) NSD versus output signal frequency, f_{out}, clocked at 10 GS/s.

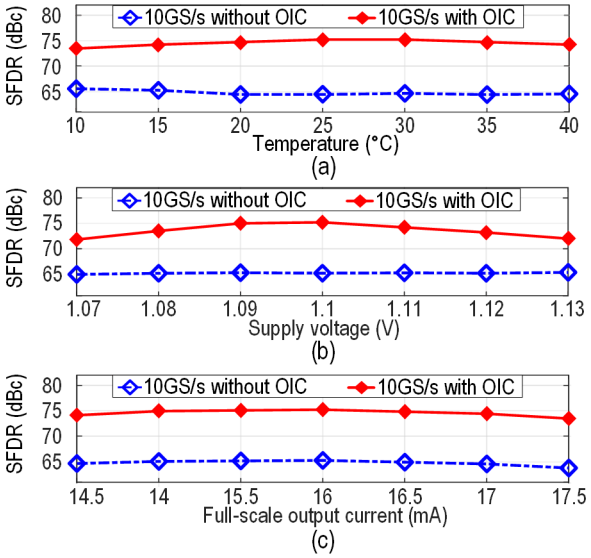

Fig. 21. Measured SFDR versus (a) temperature, (b) supply voltage, and (c) full-scaled output current with other conditions unchanged.

a supply voltage of 1.1 V, the measured SFDR improvement with OIC exceeds 9.5 dB.

For a smaller output swing, the nonlinearity caused by the finite output impedance is also smaller. In addition, if D_{in} is limited to the region between 512 and 15871, for which the output swing is 0.9375 of the full-scale range, the PMOS will always operate in the triode region with a fixed gate voltage in this work. However, the PMOS resistance still changes slightly with V_{op} and V_{on}. As a result, the measured SFDR with OIC at a small output swing still shows some improvement, e.g., a 2-dB measured SFDR improvement when output swing is −6 or −12 dBFS. Notably, if $V_G(D_{\text{in}})$ has more levels, the SFDR at small output swings will show further improvement.

Table I compares the measured performance of the DAC with that of other state-of-the-art CMOS Nyquist DACs with sampling frequency $f_s \geq 6$ GHz and resolution ≥10 bits [1], [3], [16], [18]. Using the OIC and CPR, the proposed DAC achieves a high linearity over a wide bandwidth and operates from a single 1.1-V supply. The power consumption from the single 1.1 V supply clocked at 10 GS/s is only 162 mW, which is much smaller than in [1], [3], [16], and [18]; even with a lower f_s. Furthermore, the active area of the IC is less than one seventh of that of the others. Fig. 22 plots a common figure-of-merit (FoM) [4], [14], [19] versus f_s for the proposed DAC and the compared state-of-the-art CMOS Nyquist DACs with $f_s \geq 1$ GHz and resolution ≥ 10 bits. The envelope is curve-fit by the two best prior state of the arts. It is seen that, compared with the envelope, this work achieves a 9× better FoM with f_s equal to 10 GS/s and a 1.6× higher f_s with the same FoM.

TABLE I

COMPARISON OF THE DAC WITH OTHER STATE-OF-THE-ART CMOS NYQUIST DACS WITH $f_s \geq 6$ GHz AND RESOLUTION ≥ 10 Bits

	This Work	JSSC 2018 [18]		ISSCC 2018 [16]	ISSCC 2017 [3]	VLSIC 2016 [1]
Process (nm)	28	65		16	16	40
Resolution, N	14	16		16	14	14
Active area (mm^2)	0.07	0.97		0.52	0.855	N/A
Supply (V)	1.1	1.0 / 2.5		1.0/3.0	N/A	1.0/±1.8
Full-scale output current, I_{load} (mA)	16	16		40	20	40
Output power, P_{load} (dBm)	-10.09	-3.98		3.98	-2.04	3.98
Sample frequency, f_s (Hz)	10G	9G	12G	6G	6.8G	8.9G
Power consumption, P_{total} (mW)	162	758	1065	350	330	1200
$SFDR_{best}$ (dBc)	75.2	82	76	88	84	71
$SFDR_{worst}$ (dBc)	65.5	56	52	67	62	50.5
FoM (Hz/fW)	450	63	19	650	280	5.9

$$FoM = \frac{2^{\frac{SFDR_{Best}-1.76}{6.02}} \cdot 2^{\frac{SFDR_{Worst}-1.76}{6.02}} \cdot f_S}{P_{total} - P_{load}}. \text{ The larger the better}$$

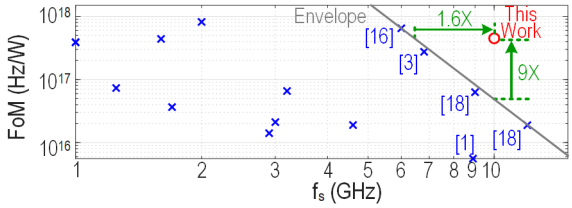

Fig. 22. Common FoM versus f_s for proposed DAC and other state-of-the-art CMOS Nyquist DACs with $f_s \geq 1$ GHz and resolution ≥ 10 bits.

V. CONCLUSION

This article has proposed a DAC with OIC and CPR techniques to improve the SFDR and IM3 performance. The two techniques additionally enable the use of small-size non-cascoded current cells, which reduce the area and routing parasitic capacitance of the current cell array, and hence widen the bandwidth, relax the requirement of switch driver's driving ability, and reduce the power consumption. The measurement results have shown that the implemented DAC achieves a high linearity over a wide bandwidth, a low-power consumption, a small area, and the ability to use a single low-voltage supply. Consequently, the proposed OIC and CPR techniques provide an effective means of resolving the low output impedance and critical strict timing skew issues of DAC when more advanced processes are used and wider bandwidths are targeted.

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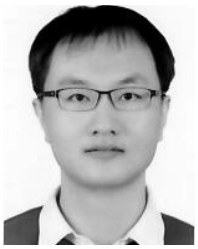

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