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A 4.5 mW CT Self-Coupled ΔΣ Modulator With 2.2 MHz BW and 90.4 dB SNDR Using Residual ELD Compensation

Chen-Yen Ho, *Member, IEEE*, Cong Liu, Chi-Lun Lo, Hung-Chieh Tsai, Tze-Chien Wang, and Yu-Hsin Lin

***Abstract*—This paper presents a power-efficient single-loop continuous-time (CT) ΔΣ modulator (DSM) that achieves a SNDR of 90.4 dB over a 2.2 MHz signal bandwidth. The modulator uses a fourth-order feed-forward architecture incorporating the continuous-time self-coupling (CTSC) technique. Moreover, to reduce hardware area, this design utilizes the residual signal for excess loop delay (ELD) compensation. To improve linearity, low-ripple DAC latches and low toggle-rate dynamic element matching (DEM) algorithm are adopted. This DSM is fabricated in a 55 nm LP CMOS technology. Operating at 140 MHz sampling rate, the chip consumes 4.5 mW from power supplies of 1.2 V and 1.8 V. It achieves 90.4 dB SNDR and 92 dB dynamic range (DR) with a 2.2 MHz signal bandwidth, resulting in a Schreier FOM of 177.3 dB and 178.9 dB based on SNDR and DR, respectively. The chip area is 0.09 mm^2.**

***Index Terms*—Analog-to-digital converter (ADC), continuous-time delta-sigma modulator (CT DSM), continuous-time self-coupling (CTSC), excess loop delay (ELD) compensation.**

I. Introduction

A HIGH dynamic range (DR) continuous-time (CT) ΔΣ modulator (DSM) is required to simplify and relax the RF analog front-end in highly integrated SoC for consumer electronics products. Recently, [1], [3] have introduced high DR and power-efficient CT DSMs. The CT DSM of [1] embeds a second-order active filter and a VGA to extend the DR from 82 dB to 92 dB. However, the additional active filter results in a complicated architecture as well as extra area. In [2], the self-coupled noise injection technique is introduced to add an extra order in the noise transfer function (NTF). This technique requires an accurate clock cycle delay which is only available in the discrete-time (DT) designs. The modulator of [3] uses a second-order dynamic element matching (DEM) to address nonlinearity issue of a multi-bit digital-to-analog converter (DAC) by reducing data-dependent switching. This modulator achieves a 97.3 dB SNR over 600 kHz BW but its SNDR is below 90 dB.

Manuscript received May 03, 2015; revised June 22, 2015, August 06, 2015, and August 18, 2015; accepted August 19, 2015. This paper was approved by Guest Editor Jieh-Tsorng Wu.

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Digital Object Identifier 10.1109/JSSC.2015.2475160

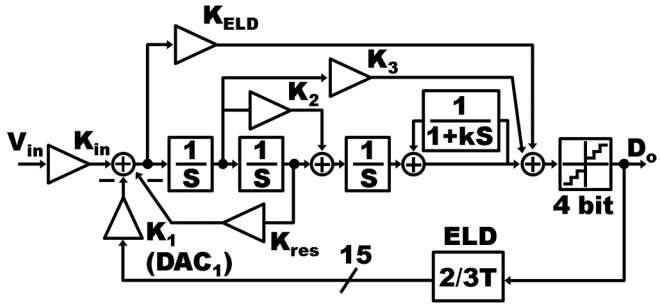

Fig. 1. The architectural block diagram of the proposed CT ΔΣ modulator.

Apart from DR considerations, power efficiency and area are also crucial. Conventional excess loop delay (ELD) compensation [4]–[6] is implemented using an inner DAC, which increases the power consumption and capacitive loading of the last integrator. As a result, a wide-bandwidth opamp is required for the last integrator to alleviate the phase delay of the loop filter.

In this paper, we present a CT DSM that achieves better than 90 dB DR within a bandwidth of 2.2 MHz. This single-loop CT DSM employs a continuous-time self-coupling (CTSC) scheme to implement a second-order integrator. The modulator uses a residual ELD compensation technique to simplify the modulator architecture. Furthermore, its DAC uses low-ripple latches to reduce the power-line ripple caused by the data-dependent short-circuit current, thus improving the DAC's dynamic linearity. This DSM chip achieves 90.4 dB SNDR and 104 dB SFDR while consuming 4.5 mW [7]. It has the state-of-the-art power efficiency. The Schreier FOM is 177.3 dB based on SNDR.

The paper is organized as follows. Section II describes the CT DSM architecture and discusses several architectural and circuit techniques. Section III presents the circuit implementation and describes the techniques used to improve performance and reduce power consumption. Finally, experimental results and conclusions are given in Sections IV and V, respectively.

II. Modulator Architecture Design

A. Architecture

The DR requirement of a CT DSM depends on the amount of pre-filtering preceding the ADC which attenuates large interferers. To avoid expensive and bulky analog channel-selection filters, which usually do not scale well with advanced technology, a high DR ADC is required. Fig. 1 shows the architecture of the CT single-loop fourth-order feed-forward loop filter

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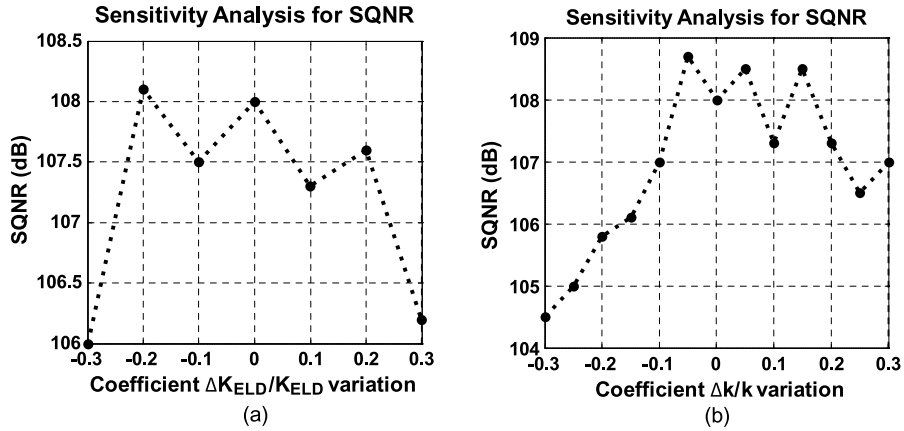

Fig. 2. (a) Sensitivity analysis for SQNR with $K_{ELD} + -30\%$ variation; (b) Sensitivity analysis for SQNR with $k + -30\%$ variation.

modulator with a 4-bit quantizer. The modulator can achieve better than 90 dB DR with an oversampling ratio (OSR) of 32. The sampling frequency is 140 MHz, yielding a 2.2 MHz signal bandwidth. The maximum out-of-band gain $\|\mathrm{NTF}\| = 5$ dB is chosen to provide sufficient quantization noise suppression, resulting in a signal-to-quantization-noise ratio (SQNR) of 105 dB. The additional SQNR margin is reserved for device noises and process-voltage-temperature (PVT) variations. This modulator structure was chosen over an all feed-forward topology because we can scale the output swing of the first integrator to reduce power consumption. As shown in Fig. 1, 2/3 of the clock period, i.e., 4.8 nsec, is allocated for 4-bit quantization, digital logic, and DAC switching.

In Fig. 1, the first integrator, the second integrator, and the local feedback K_{res} form a conventional resonator. The optimized NTF zero is placed by adjusting K_{res}. It is possible to reduce power and area by using single-opamp resonator [9]. It requires high-gain opamp to suppress in-band quantization noise. Thus, it is not suitable for our design. In Fig. 1, the third integrator and the following positive feedback loop form a second-order integrator. The self-coupling technique was first proposed in a discrete-time DSM design [10]. In our continuous-time self-coupling (CTSC) scheme, the accurate Z^{-1} delay is replaced by $1/(1 + kS)$, where K is determined by the NTF coefficient synthesis. Shown in Fig. 1, the K_3 high speed feed-forward path structure for S^{-1} term [5], which represents the signal path through one integrator of the loop filter, is adopted for robust stability design. The K_{ELD} path is to compensate ELD. Its value is derived from NTF coefficient synthesis.

Fig. 2(a) and Fig. 2(b) show the modulator SQNR sensitivity against K_{ELD} and self-coupling coefficient K. The plots show the simulation results that the SQNR is still better than 100 dB even if K_{ELD} or K deviates from its nominal value by 30%.

B. Continuous-Time Self-Coupling (CTSC) Integrator

In Fig. 1, the third integrator and the following positive feedback loop form a second-order integrator using the CTSC technique. In Fig. 3, the integrator and the positive feedback are merged into a single loop. The positive feedback becomes $S/(1+KS)$ to maintain the original transfer function. The entire

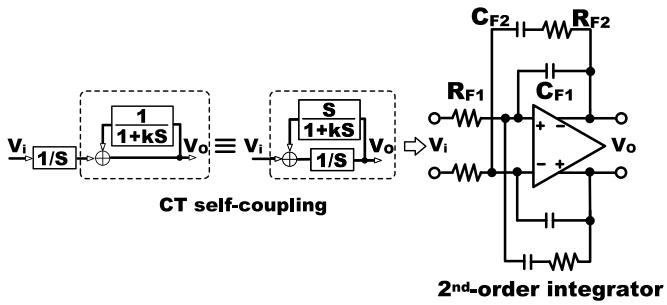

Fig. 3. Continuous-time self-coupling (CTSC) integrator.

loop can be implemented with a single-opamp circuit shown in Fig. 3. The integrator consists of the opamp and capacitor C_{F1}. The positive feedback is realized using the capacitor C_{F2} and resistor R_{F2}. By choosing $C_{F1} = C_{F2} = C$, the transfer function of the circuit is:

$$\frac{V_O}{V_i} = \frac{-(1 + SCR_{F2})}{S^2C^2R_{F1}R_{F2}} = \frac{-1}{S^2C^2R_{F1}R_{F2}} + \frac{-1}{SCR_{F1}}. \quad (1)$$

In our design, the CTSC path improves the SQNR of the DSM by 10 dB.

This CTSC integrator has the advantage in required chip area. A conventional second-order integrator can be implemented by using the ac-coupled integrator [8]. It requires additional capacitors to realize the feed-forward coefficient, which occupies area. An alternative is using the T-filter [9]. Fig. 4(a) shows both the CTSC integrator and the T-filter integrator. Noise performance is not considered, since the integrator is used only in the last stage of the DSM in this design. Its noise contributes less than 5% of the total noise budget. Both integrators realize the same transfer function of (1). Let $C_{F1} = C_{F2} = C_F$, and $C_{T1} = C_{T2} = C_T$. If $R_{F1} = R_{T1}$ and $R_{F2} = R_{T2}$, then $C_F < C_T$. It shows a 50% area reduction in our design. In this work, the C_{F1} and C_{F2} are 300 fF.

Fig. 4(b) shows another advantage of the CTSC integrator over the T-filter integrator. It is easier to reduce the order of the CTSC integrator. During power-on or when the DSM overload scenario occurs, it is a common practice to reduce the order number of the modulator to re-gain loop stability.

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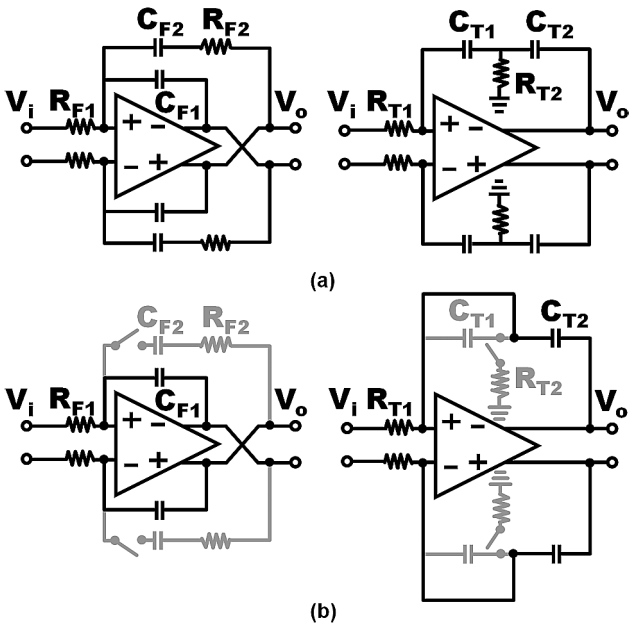

Fig. 4. (a) CTSC integrator and T-filer integrator; (b) Re-configuration of integrators.

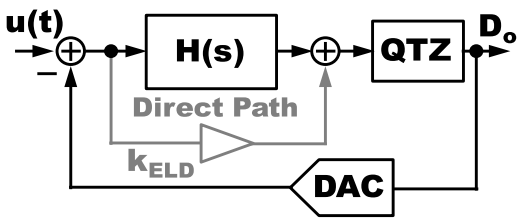

Fig. 5. The direct path technique for ELD compensation.

C. Residual ELD Compensation

Fig. 5 shows a direct path with coefficient K_{ELD} for ELD compensation [11], [12]. The difference between the input u(t) and the DAC output is extracted. This residual signal contains primarily quantization noise, and is used as the ELD compensation signal. We implement the residual ELD compensation in current mode. As shown in Fig. 6, the V_i input is converted into current I_{Vi} by resistor R_1. The residual current $I_{C1} = I_{Vi} - I_{DAC}$ is the difference between the input current I_{Vi} and the DAC current I_{DAC}. This I_{C1} flows through capacitor C_1 and into the opamp's output stage as I_{OP} and I_{ON}. As shown in Fig. 6, the output stage of the opamp contains current mirrors that duplicate and scale output current I_{OP} as I_{EP} and I_{ON} as I_{EN}. Both I_{EP} and I_{EN} from the first integrator are directed to resistors R_{ELD} as high-speed ELD compensation [5]. Note that the Ix current in Fig. 6 is much smaller than I_{OP} and I_{ON} to achieve a power efficient loop filter design.

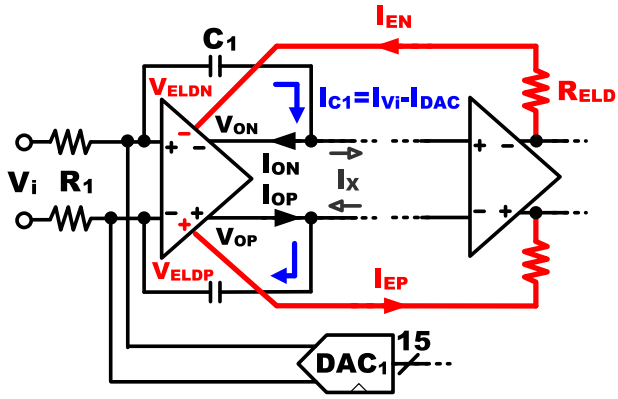

Fig. 6. Current flow of the first integrator and the residual ELD compensation scheme.

Fig. 7(a) shows a conventional ELD compensation and the associated signal waveforms. To compensate the delay of QTZ, the inner DAC (DAC2) comprises both the input signal and quantization noise. Therefore, the last integrator in filter H must provide large output current (blue) due to its input-dependent component. Fig. 7(b) shows the direct-path residual ELD compensation scheme and its associated signal waveforms. The DAC2 in Fig. 7(a) is replaced by DAC1 and K_{ELD}. The K_{ELD} value is the ratio of the DAC2's conversion gain to the DAC1's conversion gain. The residual signal in the K_{ELD} path (red) contains mostly quantization noise and is relatively small, relaxing the driving capability of the last integrator.

III. Circuit-Level Implementation

A. Modulator

Fig. 8 shows the circuit-level schematic of the CT DSM. The loop filter comprises of three active RC integrators. Their capacitors (C1 $\sim$ C4) are digitally adjustable with a range of $+-40\%$ to cover the worst-case RC variation. The capacitances are controlled by an on-chip calibration circuit [13]. The time constant of a RC replica is calibrated by a digital control loop to achieve an accuracy of 5%. The input resistor R_1 has a value of 555 Ω. It is a tradeoff between noise budget and DAC current consumption. At the output of the first integrator, the Ix current is designed to be as small as possible. As a result, R_2 is 112 kΩ and R_6 is 320 kΩ. The high speed feed-forward path for the S^{-1} term is realized by R_{f4} and R_4. These two resistors introduce an extra pole at the input of the quantizer. We want this pole to be larger than $3 * Fs$ (420 MHz) so that it does not affect the overall loop performance. We choose $R_{f4} = 24$ kΩ and $R_4 = 2$ kΩ. The transfer function for the modulator is shown in (2) at the bottom of the page. As described in the previous section, $C_3 = C_4 = C_{SC}$. In Fig. 8, the 4-bit quantizer employs the

$$\frac{V_O}{V_i} = -\left(\frac{\left(\frac{R_4}{R_4+R_{f4}}\right)}{C_1R_1}S^3 + \frac{1}{C_1C_{SC}R_6R_1}S^2 + \frac{1}{C_1C_{SC}R_1}\left(\frac{1}{C_2R_2R_3} + \frac{1}{C_{SC}R_6R_5}\right)S + \frac{1}{C_1C_2C_{SC}^2R_1R_2R_3R_5} \right) \Bigg/ \left(S^2\left(S^2 + \frac{1}{C_1C_2R_2R_{res}}\right)\right) \quad (2)$$

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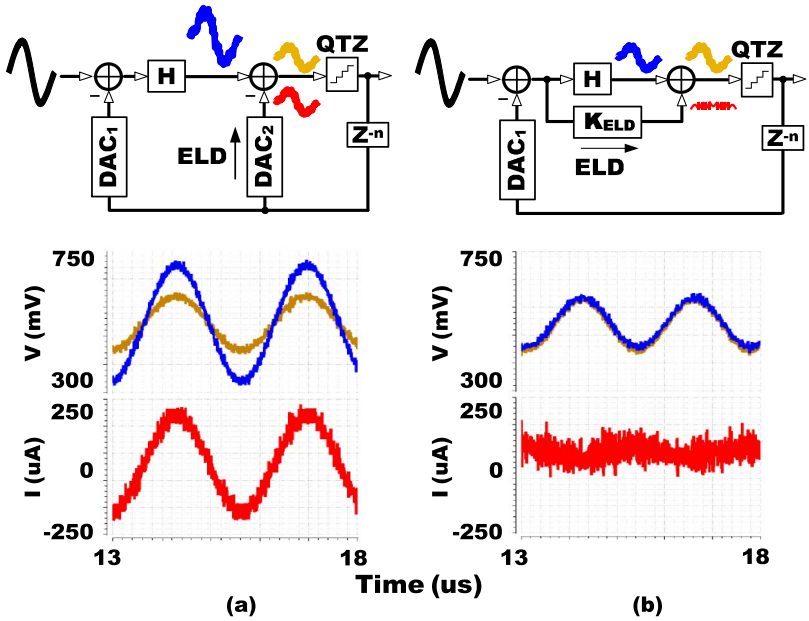

Fig. 7. (a) Conventional ELD compensation and the corresponding timing waveform; (b) residual ELD compensation and the corresponding timing waveform.

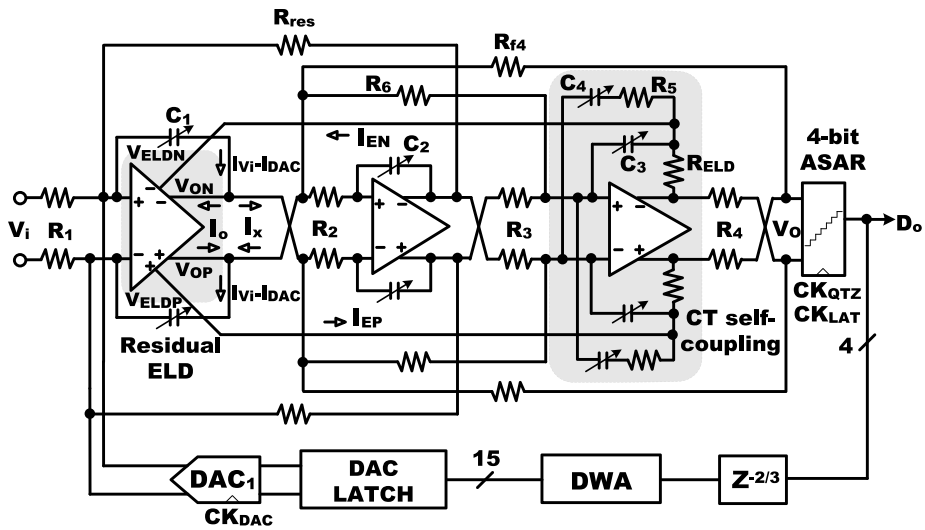

Fig. 8. CT DSM schematic.

asynchronous successive approximation register (ASAR) quantization scheme [4]. It includes a two-stage dynamic comparator [14], which consumes only dynamic power. The 15-level current-steering non-return-to-zero (NRZ) DAC_1 is used for the modulator feedback.

Fig. 9 shows the timing diagram of the system operation. During the high state of the CK_{QTZ} clock, the ASAR samples its input. The sampling phase is 1/3 of the entire clock period. ASAR operation is initiated at the falling edge of CK_{QTZ}. At the rising edge of the CK_{LAT} clock, the resulting ASAR output is latched and then processed using a modified data weighted averaging (DWA) technique [15]. At the rising edge of the CK_{DAC} clock, the DAC latches the input data and changes the output accordingly. As a result, 1/3 of the clock period is reserved for the ASAR operation. The delay from the quantizer input to the DAC output is 2/3 of the clock period.

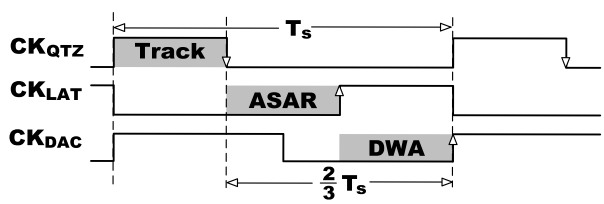

Fig. 9. System clock timing diagram.

B. Opamp

Fig. 10 shows the schematic of the first opamp with the ELD compensation path. It is a two-stage opamp with AC feed-forward paths through capacitors C_{f1} and C_{f2} [4]. Cascode stage M_3 and M_4 are added to provide high gain. Source degeneration resistors R_{d1} and R_{d2} are added to reduce flicker noise ef-

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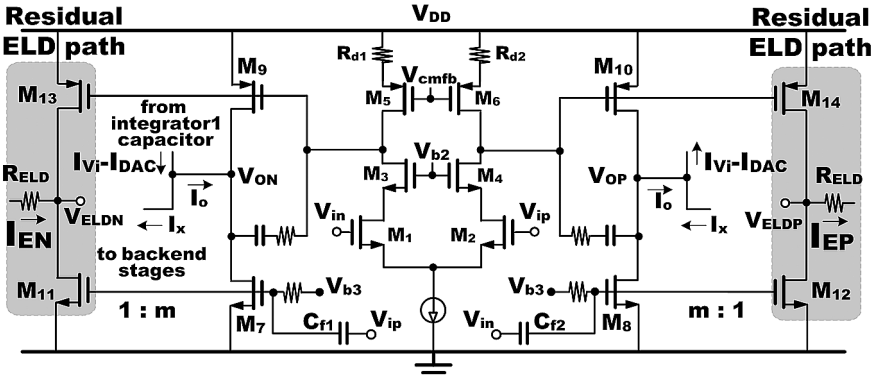

Fig. 10. opamp schematic with residual ELD compensation path.

fect. The opamp's differential output stage comprises of MOSFETs $M_7 \sim M_{10}$. Its output currents are mirrored by MOSFETs $M_{11} \sim M_{14}$ to produce I_{EP} and I_{EN} for ELD compensation. In this design, the current mirror ratio (m) is 6, and the resistor R_{ELD} is 700 Ω. A larger m leads to inaccurate mirrored current due to mismatch. An inaccurate compensation current may result in an unstable modulator. The second and the third integrators share the same opamp schematic with reduced bias currents and different bandwidths.

C. DAC Cell

In Fig. 8, the feedback DAC dominates the modulator noise as well as linearity. Fig. 11 shows the schematic of the DAC current cell. The bipolar-type DAC cell is operated under a 1.8 V supply. Comparing to a unipolar-type DAC, a bipolar-type DAC requires only half of the total current to produce the same output range. The cascaded current source structure is used for high output impedance and smaller parasitic capacitance at the common source node of the current switches M_{P3}, M_{P4}, M_{N3} and M_{N4}. To reduce the noise contribution, the transconductances of M_{P1} and M_{N1} are minimized. The source degeneration resistors R_{P1} and R_{N1} are added to reduce flicker noise effect. The voltage headroom for R_{P1} and R_{N1} are 400 mV and 300 mV respectively. Low-pass filters $R_{P2} - C_{P1}$ and $R_{N2} - C_{N1}$ are inserted to suppress thermal noise from the reference bias current. From simulations, using the DAC cells with a mismatch variance of 0.23%, the CT DSM of our design can achieve −103 dB total harmonic distortion (THD).

D. DAC Latch

As shown in Fig. 11, the DAC cell includes two latches that receive the same control input S and drive the N-MOSFET current switch $M_{N3} - M_{N4}$ and the P-MOSFET current switch $M_{P3} - M_{P4}$ separately. Fig. 12 shows a conventional eight-transistor DAC latch [16]. It provides the steepest transition and the smallest CK_{DAC} to Q delay. As shown in Fig. 12, if the previous state stored in Q_B is high and the input S is high, then a short-circuit current passes through M_{L5} and M_{L1} on the rising edge of the CK_{DAC} clock. The short-circuit current induces a voltage drop on the VDD supply line with resistance. This data-dependent ripple on the VDD line also appears on the Q and Q_B latch

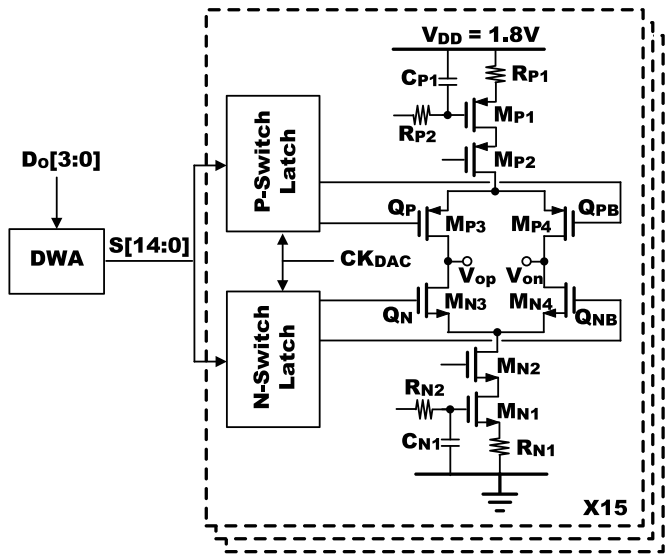

Fig. 11. DAC schematic.

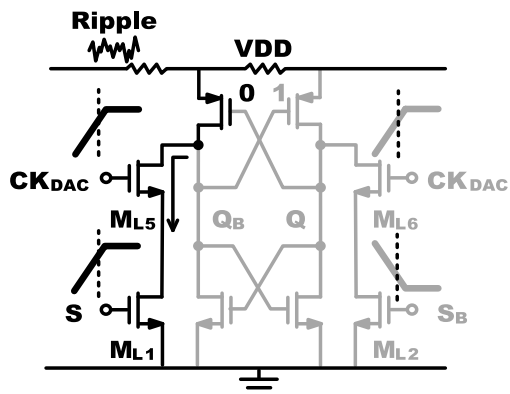

Fig. 12. Conventional DAC latch.

outputs, and shows up at the DAC output, resulting in degradation of the SNR and THD of the DSM.

Fig. 13(a) shows the proposed low-ripple latch to overcome this problem. We add additional input drivers, consisting of M_{L3}, M_{L4}, M_{L7}, and M_{L8}, and clock gating switches $M_{C1} \sim M_{C4}$. As shown in Fig. 13(b), if the previous state

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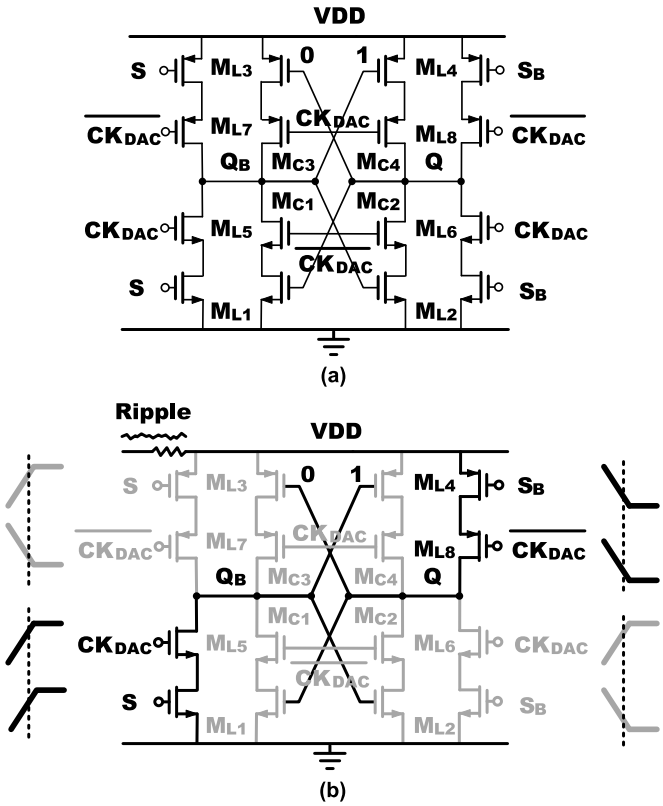

Fig. 13. (a) Low-ripple DAC latch. (b) Operation at $\mathrm{CK_{DAC}}$ rising edge.

stored in $\mathrm{Q_B}$ is high (Q is low) and the input S is high, then, on the rising edge of the $\mathrm{CK_{DAC}}$ clock, $\mathrm{Q_B}$ is pulled low and Q is pulled high without any short-circuit path.

As shown in Fig. 11, two latches are used to drive the N-switch $\mathrm{M_{N3}-M_{N4}}$ and the P-switch $\mathrm{M_{P3}-M_{P4}}$ separately. The two differential outputs, $\mathrm{Q_N-Q_{NB}}$ and $\mathrm{Q_P-Q_{PB}}$, have different cross points. They are optimized separately. The cross point of $\mathrm{Q_N-Q_{NB}}$ is chosen to minimize the glitches occurred at the common-source node of the N-switch, while the cross point of $\mathrm{Q_P-Q_{PB}}$ is chosen to minimize the glitches occurred at the common-source node of the P-switch. For the latch of Fig. 13, the output cross point is adjusted by sizing the input devices $\mathrm{M_{L1}}$, $\mathrm{M_{L2}}$, $\mathrm{M_{L3}}$ and $\mathrm{M_{L4}}$. Simulations show that our DAC latch design can improve the SFDR of the DSM by 10 dB.

E. Data Weighted Averaging (DWA)

As shown in Fig. 11, data weighted averaging (DWA) algorithm is used to select active DAC cells to mitigate the effect of current mismatches. Fig. 14(a) shows the conventional DWA operation. A selection cycle is completed if all cells have been selected once. The next cycle always starts from the first cell $\mathrm{I_0}$. For example, when the DAC input S is 8, cells $\mathrm{I_0}$ to $\mathrm{I_7}$ (cycle 1) are selected. When S changes to 9, cells $\mathrm{I_8}$ to $\mathrm{I_{14}}$ (cycle 1) are selected and cells $\mathrm{I_0}$ to $\mathrm{I_1}$ (cycle 2) are also selected. As a result, a total of 13 cells are toggled. When a cell toggles, a fixed amount of switching transient mismatch appears at the DAC output [19]. In the DWA operation, those transient mismatches appear as the second-order harmonic distortion in the DAC output [20]. Fig. 14(b) shows the modified DWA technique we use [15]. It reduces the number of toggling cells, thus

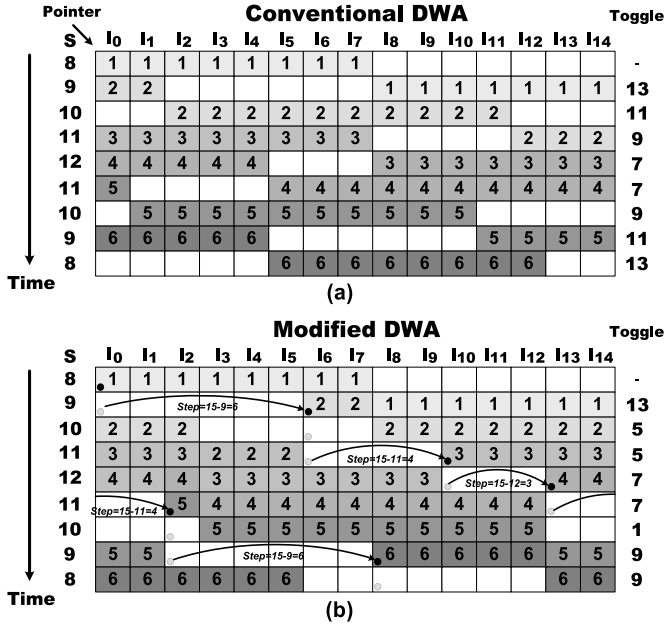

Fig. 14. (a) Conventional DWA operation. (b) Modified DWA operation.

mitigating the toggle-related distortion. Unlike the conventional DWA, the starting cell of a selection cycle is shifted forward from the starting cell of the previous cycle by an amount of N-S, where N is the number of total DAC cells and S is the current input. For example, when the DAC input S is 8, cells $\mathrm{I_0}$ to $\mathrm{I_7}$ (cycle 1) are selected. The starting cell of cycle 1 is $\mathrm{I_0}$. When S changes to 9, cells $\mathrm{I_8}$ to $\mathrm{I_{14}}$ (cycle 1) are selected. The remaining two cells are selected in cycle 2. The starting cell of cycle 2 is shifted forward from $\mathrm{I_0}$ by an amount of $15-9=6$, i.e. the starting cell is $\mathrm{I_6}$. This modified DWA reuses as many the previous-selected cells as possible to reduce the number of toggling cells. The number of toggling cells are also listed in Fig. 14(a) and Fig. 14(b) for comparison.

IV. Experimental Results

Fig. 15 shows the CT DSM chip fabricated in a 55 nm LP CMOS technology. This chip occupies 0.09 $\mathrm{mm^2}$ area, including reference generator, bias, and clock generator. Power domains are careful assigned to separate sensitive analog circuits from the noisy digital circuits. Decoupling capacitors are used to filter out the noise in the bias generator for all analog blocks and placed close to sensitive circuits to minimize the transient effects. Whenever possible, multiple bond pads are allocated for the power lines to reduce the perturbation caused by bond wires. The high-speed blocks are placed close to each other to minimize the feedback path delay induced by the parasitic resistance and capacitance of the metal wires. The residual ELD compensation cell in the first integrator occupies only 30 $\mu\mathrm{m^2}$, which is competitive to the conventional ELD DAC [4]–[6]. The routing from the DWA output to the DAC input is buffered for high-speed data transmission.

Fig. 16 shows the power consumption pie chart among different sub-circuits of the DSM. The total power consumption of the modulator is 4.5 mW. The loop filter, quantizer, and DAC latches are operated under 1.2 V, and the DAC cell under 1.8

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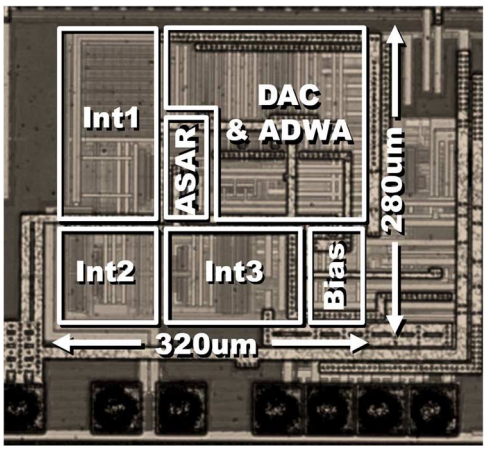

Fig. 15. Chip micrograph.

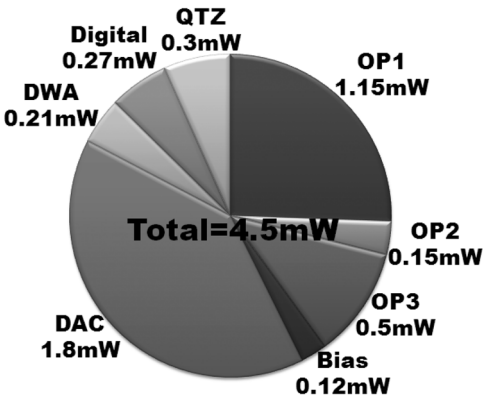

Fig. 16. Pie chart of power consumption.

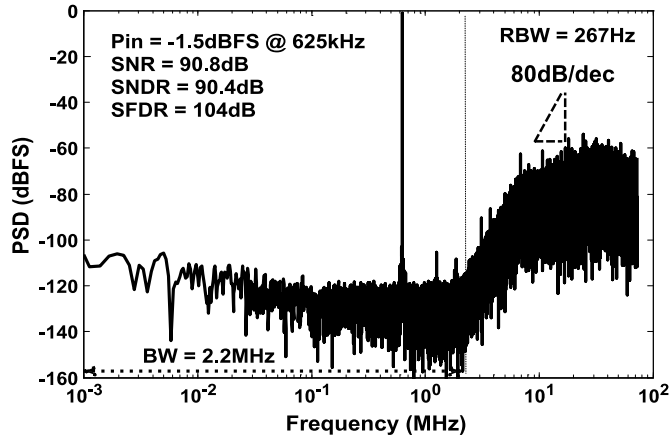

Fig. 17. Measured DSM output spectrum. Input is a 625 kHz −1.5 dBFS sine wave.

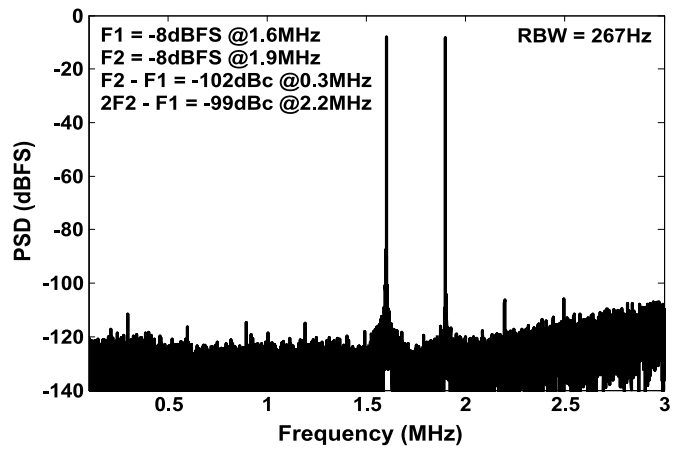

Fig. 18. Measured DSM output spectrum. The two tones are −8 dBFS sine waves at 1.6 MHz and 1.9 MHz.

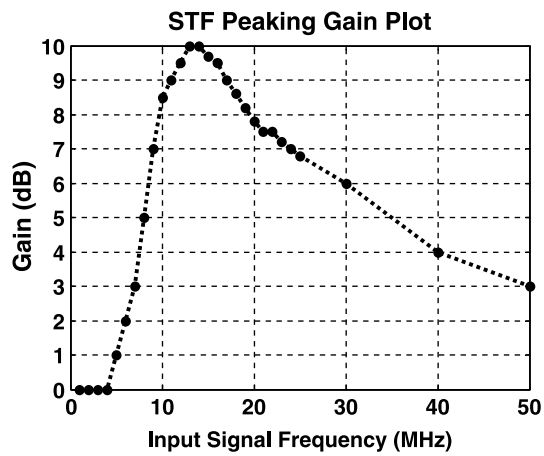

Fig. 19. Measured STF peaking.

V. Due to the use of residual ELD compensation scheme, the output loading for the third integrator is reduced, leading to less power consumption. It consumes 11% of the total power. Due to the stringent noise requirement, the first opamp and the DAC consume 66% of the total power.

The DSM is clocked at 140 MHz. The on-chip clock generator is a phase-locked loop. The measured rms jitter is below 4 psec. Assuming an oversampling ratio (OSR) of 32, the DSM signal bandwidth is 2.2 MHz. Fig. 17 shows a single-tone spectrum with an in-band input at 625 kHz. The DSM full scale is 2.0 Vpp. The measured SFDR is −104 dB with a −1.5 dBFS input. The measured SNR and SNDR are 90.8 dB and 90.4 dB respectively. The 80 dB/decade slope of the spectra validates the fourth-order noise-shaping using the CTSC technique. The in-band spectrum shows an increase in noise power density at low frequencies, which is attributed to the DAC flicker noise. Fig. 18 shows the two-tone test. The two tones are 1.6 MHz and 1.9 MHz sine waves with −8 dBFS amplitude. They are near the band edge. The measured second inter-modulation (IM2) and third inter-modulation (IM3) are −102 dBc and −99 dBc respectively.

Fig. 19 shows the signal transfer function (STF) gain peaking of the DSM. Input with the same power level is swept from DC to 50 MHz. The measured peak gain is around 10 dB, which is close to the design value. Comparing to a DSM using the conventional fourth-order feed-forward loop filter, our design exhibits a larger STF gain peaking by about 3 dB.

Fig. 20 shows the measured SNR and SNDR vs. the input power. The input is a 625 kHz sine wave. This modulator achieves 92 dB DR in a 2.2 MHz signal bandwidth. Table I. summarizes the performance of the modulator and compares to the state-of-the-art low-pass CT DSMs. This CT DSM

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TABLE I
PERFORMANCE SUMMARY

	This work	[1]	[3]	[4]	[6]	[9]	[17]	[18]
Technology (nm)	55	130	180	40	40	40	65	28
V_{DD} (V)	1.2/1.8	1.4	-	1.2	1.4/2.4	-	1.2	-
F_S (MHz)	140	256	57.6	65	245.76	300	128	640
BW (MHz)	2.2	2	0.6	1.92	1.92	10	2	18
IMD (dB)*	-99 (IM3)	-73 (IM3)	-	-90 (IM2)	-	-	-91.9 (IM3)	-
DR (dB)	92	92 (w/I VGA) 82 (w/o VGA)	-	83.4	83	70.6	80	78.1
Peak SNR (dB)	90.8	80.5	97.3	80	-	70.6	79.1	75.4
Peak SNDR (dB)	90.4	74.4	-	79.6	78	70	79.07	73.6
Power (mW)	4.5	5	31	1.91	2.8	2.57	4.52	3.9
Area (mm^2)	0.09	0.33	0.99	0.051	0.085	0.051	0.084	0.08
FOM_{S1} (dB)	177.3	160.4	-	169.6	166.4	165.9	165.6	170.2
FOM_{S2} (dB)	178.9	168	171.8 (w/I SNR)	173.4	171.4	166.5	166.5	174.7
FOM_W (fJ/step)	37.8	291.4	-	64	112.3	50	153	27.7

$\mathrm{FOM_{S1}} = \mathrm{SNDR} + 10\log(\mathrm{BW/Power})$
$\mathrm{FOM_{S2}} = \mathrm{DR} + 10\log(\mathrm{BW/Power})$
$\mathrm{FOM_W} = \mathrm{Power}/(2\mathrm{xBWx2}^{(\mathrm{SNDR}-1.76)/6.02})$
* Based on the worse case between IM3 and IM2

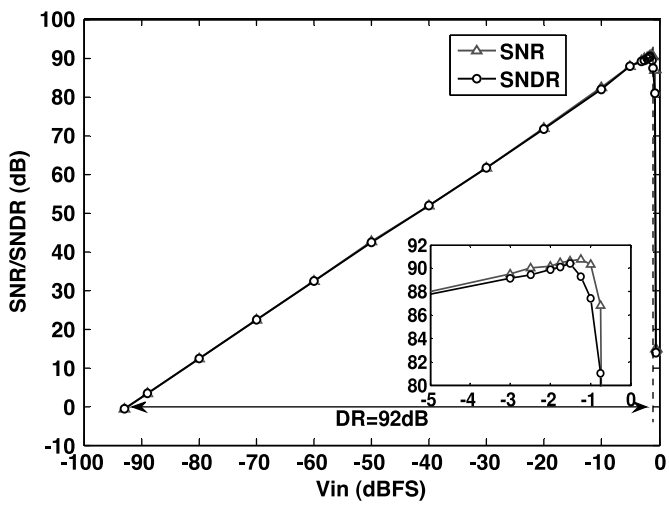

Fig. 20. Measured SNR/SNDR vs. input signal level.

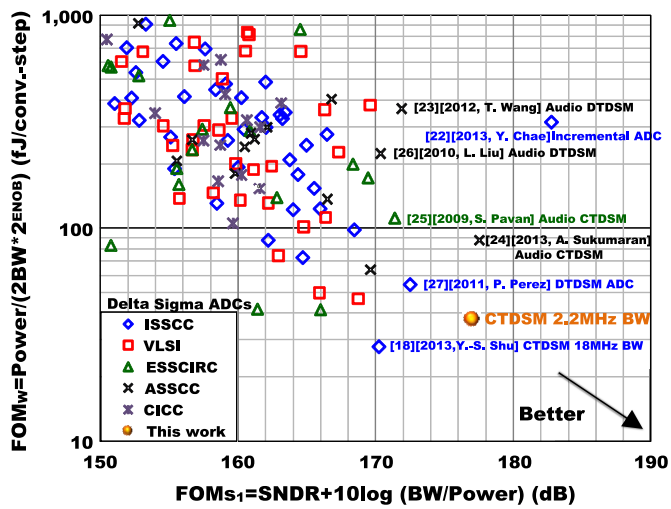

Fig. 21. Compared energy efficiency with the state-of-the-art CT/DT DSMs.

achieves a Schreier FOM of 177.3 dB and a Walden FOM of 37.8 fJ/conversion based on SNDR. Fig. 21 shows the FOM chart [21] based on SNDR with other published CT/DT DSMs ($\mathrm{FOM_{S1}} > 170$ dB). This modulator compares favorably not just to wide-bandwidth modulator, but also to audio-band application as well.

V. CONCLUSIONS

This paper presents a highly power-efficient CT DSM using the proposed residual ELD compensation technique and CTSC structure. The residual ELD compensation facilitates a small area and power-saving modulator architecture without impeding system stability. The CTSC structure realizes a

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second-order integrator which provides 40 dB/decade slopes for aggressive noise-shaping characteristic. Moreover, to address the noise limitation and nonlinearity of a multi-bit DAC, the low-ripple DAC latch is utilized to reduce data-dependent short-circuit current effect. These techniques are incorporated in the design of a high DR CT DSM and are demonstrated in this work. The resulting DSM achieves an audio-quality performance with the highest SNDR of 90.4 dB and the state-of-the-art Schreier FOM of 177.3 dB for CT DSM with larger than 1 MHz signal bandwidth.

ACKNOWLEDGMENT

The authors would like to thank Dr. T-H. Lin and Y-Y. Lin for technical discussion and paper review.

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