22.3 A 16b 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 Within DC-to-6GHz Tunable Passbands

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The agile allocation of signal bands over RF frequencies and high in-band spectral purity (both SFDR and NSD) can enable higher-order modulation in high-throughput flexible wireless/wireline transmitters, where signals are often channelized at certain center frequencies. Using a Nyquist DAC to cover the entire signal spectrum is thus unnecessary, as this trades the achievable dynamic range with the bandwidth. For such applications, a narrowband Nyquist DAC followed by a mixer, RF mixing DAC [1], or exploiting higher Nyquist zones [2] are typically adopted; these are either limited by deliverable output power or nearby spectral images due to lower input data rates. A dual-rate hybrid DAC [3] uses a delta-sigma modulated LSB path to compensate for the non-idealities of the Nyquist path, allowing high linearity and a low noise floor within the Nyquist band while limiting out-of-band quantization noise. Still, this only synthesizes the baseband signal and is difficult when covering wide RF spectra due to the DSM OSR requirements.

This paper presents a hybrid DAC with a tunable bandpass DSM that addresses the above DAC architecture constraints for high-linearity low-noise waveform synthesis over wide frequency spans. To achieve high-speed operation, a successive pipelined bandpass DSM structure is applied with shortened critical paths. We also use inverse-Sinc-shaped digital pre-distortion (DPD) to overcome roll-off from the finite DSM clock frequency, extending the effective calibration bandwidth by ~6x compared to the DPD scheme in [3]. The bandpass DAC architecture is reconfigurable for dual-rate hybrid operation, similar to [3] except for a different noise transfer function (it gains higher linearity but narrower Nyquist band compared to single rate operation). A proof-of-concept 16b 12GS/s prototype is implemented in 65nm CMOS that achieves <-170dBm/Hz in-band NSD and -85 to -67dBc IM3 from a DC-to-6GHz Nyquist band, which is lower than the state-of-the-art high-rate (>10GS/s) CMOS DACs.

Figure 22.3.1 shows the DAC implementation; 8 channels of 16b digital data are generated via 16 on-chip DDSs, each operating at 1.5GHz. A data-rate control module is used to: a) split an input word into 4b MSB and 12b LSB for DSM; and b) adjust the data rate of the MSB path to be 1, 2, 4, or 8x lower than the LSB path for dual-rate hybrid mode operation. This allows tradeoffs between DAC linearity and spectral-image location. (The higher the MSB data rate, the farther the image frequency.) The MSB paths are decoded to thermometer form and randomized via data weighted averaging (DWA). The mismatched amplitude and timing errors of those MSB current cells are measured and stored in on-chip memory and used by the inverse-Sinc-shaped DPD module. The output of the DPD is 13b wide and compressed to 4b via the successive pipelined $2^{nd}/3^{rd}$-order bandpass DSM. The DSM is only applied to the LSB portion of the input data, so the shaped noise of this hybrid DAC is far lower than conventional single-bit DSM DACs. The passbands of the bandpass DSM are also reconfigurable among 8 of 64 possible locations across the whole Nyquist band. Delay equalization is then used to align the MSB and LSB data phases, which are serialized into a single-channel 12GS/s data stream via a MUX controlled by multi-phase clocks and then synchronized by the CML latches prior to the current-steering cells.

High-speed DSM operation is crucial in this DAC architecture to tune the center frequency of the bandpass response over a wide frequency range, but conventional pipelining/unrolling techniques are often inapplicable for feedback systems with nonlinear truncation operations. Reference [4] proposes a high-speed lowpass DSM architecture, but that method cannot be applied in bandpass DSM design because: a) the operation along the feedback loop cannot be pipelined; and b) the critical path grows with the unrolling operation. This work presents a successive pipelined DSM structure that divides the DSM into 3 stages, each only compressing the incoming bit width by smaller amounts with the scaling factor shown in Fig. 22.3.2. This sharply reduces the critical path of the DSM from 13b to 3b arithmetic operations in each stage and allows high-speed operation. The 3b quantization noise from each stage is also correlated; the total quantization noise at the last-stage output is thus equivalent to a single-stage 13b DSM, as confirmed by our analysis and simulation. In each stage, the 3 LSBs of input data are processed by the error feedback DSM, while the other MSBs are added at the stage output, where extra pipelining is applied. To further shorten the critical path, the feedforward path of the DSM is pipelined and the same latency in the output adder is inserted accordingly for delay equalization as shown in Fig. 22.3.2. The center frequency of the DSM is selected by changing the 3 coefficients (a_1~a_3) of the feedback multipliers and enabling/disabling the chopping mixer inserted at the beginning/end of the DSM chain. In the multiplier implementation, parallel shift-and-sum blocks and a multiplexer are utilized for high-speed operation. In chopping mode, the input signal is chopped twice with $F_{dsm}/2$, while the DSM quantization noise is only chopped once, mirroring the shaped noise profile symmetrically to $F_{dsm}/4$, where F_{dsm} is the data rate of a single-channel DSM. Critical path and multiplier complexity are thus reduced due to replicated channels via chopping.

Figure 22.3.3 shows the inverse-Sinc-shaped DPD scheme. Reference [3] introduced a DPD scheme leveraging the fine timing and amplitude resolution of a DSM, which approximates the short timing pulse with digital pulses generated by the oversampling clock of the DSM. The approximated error pulses have wider duration compared with the actual error pulses and are equivalent to the actual errors shaped by a Sinc filter with the first notch frequency at F_s, where F_s is the overall data rate of DAC. The approximation is thus only accurate within the $F_s/8$ band and deviates further from the actual error as frequency increases. This imposes severe limits for the intended bandpass DAC operation, as the signal can operate close to $F_s/2$. The inverse-Sinc-shaped DPD scheme further processes the approximated error pulses with an inverse-Sinc filter to compensate the signal attenuation due to Sinc roll-off, especially for high-frequency harmonics. The inverse-Sinc filter is implemented with an FIR structure, where the coefficients are limited to the power of two for simplicity while maintaining sufficient accuracy for the expected filter response. As long as the filter gain can compensate the Sinc attenuation, the harmonic reduction will be enhanced.

The test chip is fabricated in 65nm CMOS and packaged in a 64-pin QFN. The DAC output is differentially loaded with a 50Ω resistor and delivers an output current of 16mA with the data rate set to 12GS/s. Sixteen 16b 1.5GS/s DDSs are implemented on-chip to synthesize full-scale digital sinusoids for single- or two-tone tests. Amplitude and timing errors are each measured by leveraging their orthogonality [5]. The inverse-Sinc-shaped DPD is capable of correcting the amplitude and timing errors within 250nA and 50fs accuracy, respectively. The NSD is measured <-170dBm/Hz in the passbands with DPD and <-128dBm/Hz in the out-of-bands.

Figure 22.3.4 shows spectrum snapshots with a 3015MHz signal frequency at 9GS/s and the measured SFDR in different frequencies/operation modes. The DWA and DPD can improve the SFDR by >18dB at low frequencies and maintain the improvement of 5–9 dB close to Nyquist frequency. The SFDR remains >65dB up to 3.1GHz at 9GS/s and >60dB up to 4.2GHz at 12GS/s.

Figure 22.3.5 shows spectrum snapshots of a two-tone test and the measured IM3 versus signal frequency. The IM3 is measured from -85 to -67dBc over the Nyquist band at 12GS/s and from -87 to -70dBc over the DC-to-3.2GHz band at 9GS/s.

Figure 22.3.6 shows the measured SFDR vs. signal frequency in dual-rate mode with DSM operating at 9GHz, demonstrating higher SFDR than single-rate mode operation, as expected. The performance is summarized and compared with state-of-the-art DACs. Figure 22.3.7 shows die micrograph.

References:

[1] C. Erdmann, et al., "A 330mW 14b 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz," *ISSCC Dig. Tech. Papers*, pp. 280–281, Feb. 2017.

[2] L. Duncan, et al., "A 10b DC-to-20GHz multiple-return-to-zero DAC with >48dB SFDR," *ISSCC Dig. Tech. Papers*, pp. 286–287, Feb. 2017.

[3] S. Su et al., "A 12-Bit 2GS/s Dual-Rate Hybrid DAC With Pulsed-Error Predistortion and In-band Noise Cancellation Achieving >74dBc SFDR and <-80dBc IM3 up to 1GHz in 65nm CMOS," *IEEE JSSC*, vol. 51, no. 12, pp. 2963-2978, Dec. 2016.

[4] S. Su, et al., "A 12 bit 1GS/s Dual-Rate Hybrid DAC with an 8GS/s Unrolled Pipeline Delta-sigma Modulator Achieving >75dB SFDR over the Nyquist Band," *IEEE JSSC*, vol. 50, no. 4, pp. 896-907, Apr. 2015.

[5] Y. Tang, et al., "A 14 bit 200MS/s DAC With SFDR >78dBc, IM3 <-83dBc and NSD <-163dBm/Hz across the Whole Nyquist Band Enabled by Dynamic-mismatch Mapping," *IEEE JSSC*, vol. 46, no. 6, pp. 1371-1381, June 2011.

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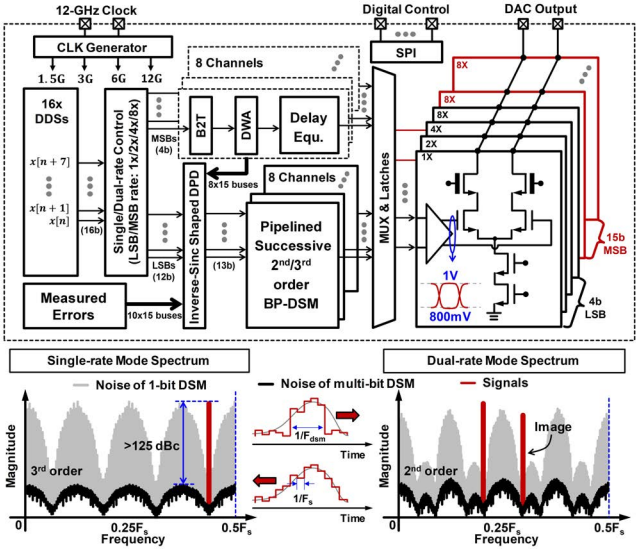


Figure 22.3.1: Architecture of the single/dual-rate bandpass DSM DAC.

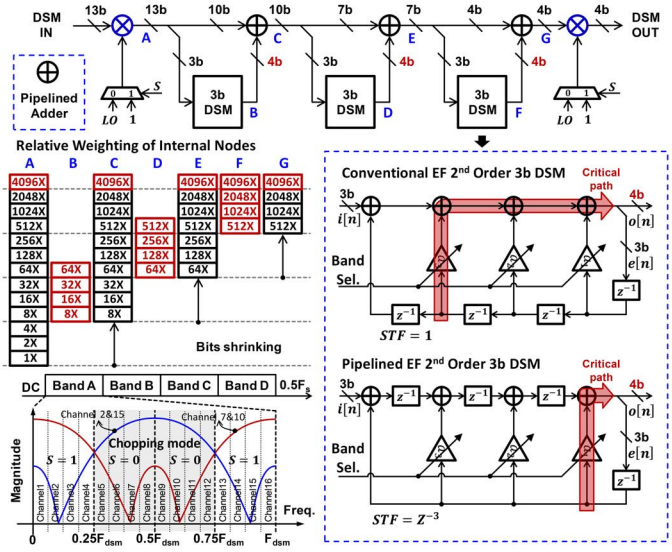


Figure 22.3.2: Implementation of the tunable successive bandpass DSM.

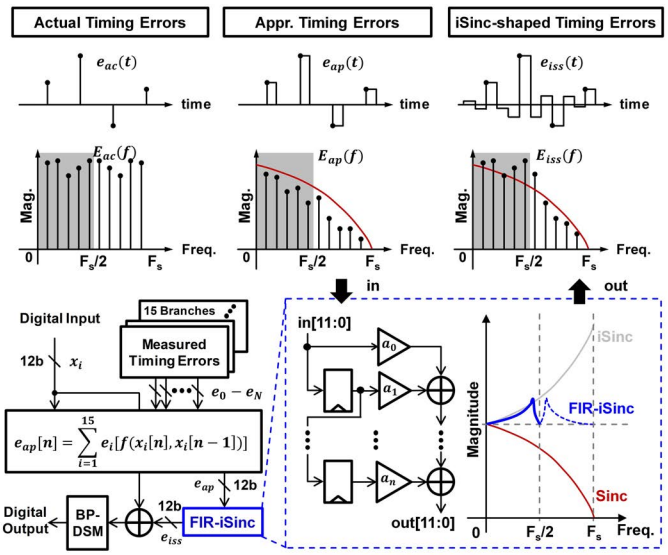


Figure 22.3.3: Inverse-Sinc shaped pre-distortion scheme.

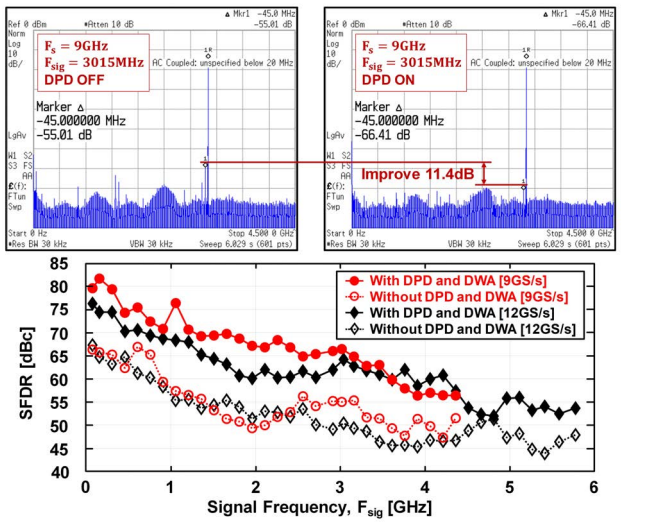


Figure 22.3.4: Measured spectrums for F_{sig} = 3015MHz in single-rate mode and measured SFDR over the Nyquist band with/without pre-distortion.

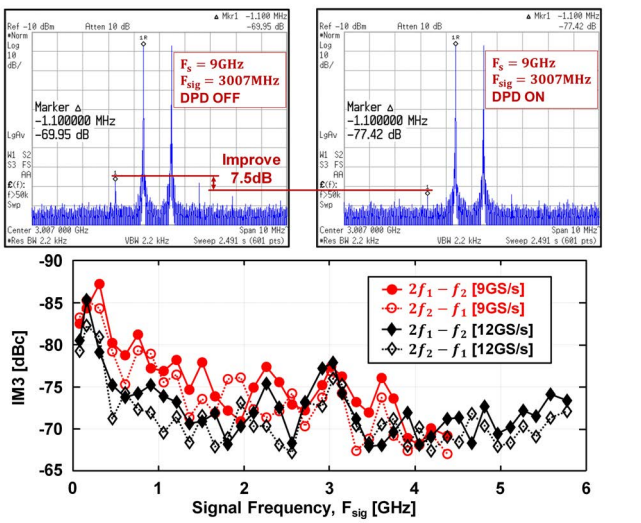
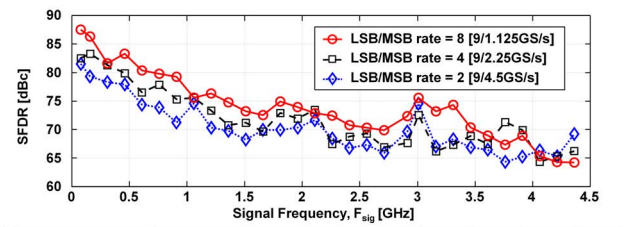


Figure 22.3.5: Measured spectrums for two-tone test and measured IM3 over the Nyquist band.



	This Work					ISSCC17 Erdmann	VLSI16 Ravinuthula	VLSI14 Olieman	VLSI13 Xiao
Technology	65nm					16nm	40nm	28nm	28nm
Resolution [bit]	16					12	14	9	13
Architecture	Single-rate		Dual-rate (LSB/MSB rate)			Mixing	Nyquist	TI	Nyquist
f_s [GHz]	12	9	9/4.5	9/2.25	9/1.125	6.8	8.9	11	9
Nyquist Bandwidth [GHz]	6	4.5	2.25	1.125	0.50625	3.4	4.45	5.5	4.5
Worst SFDR < 3GHz [dBc]	60	65	66(1)	67(1)	67(1)	63	50	53	N/A
Worst SFDR < 4GHz [dBc]	59	56	64(1)	66(1)	70(1)	59(1)	50	52	N/A
Best SFDR < 6GHz [dBc]	76	82	82(1)	83(1)	88(1)	84(1)	71	64	N/A
Worst IM3 < 6GHz [-dBc]	67	67	71(1)	77(1)	77(1)	66(1)	66	52	44
Best IM3 < 6GHz [-dBc]	85	87	89(1)	93(1)	94(1)	88(1)	93	69	75
Power [mW] Analog	250	240	230	230	230	330	1200	110	360
Power [mW] Digital	1510(2)	960(2)	910(2)	870(2)	850(2)				
Active Area [mm²] Analog	0.1					0.855	N/A	0.04	1.16
Active Area [mm²] Digital	1.61(2)								

(1) SFDR and IM3 are measured in higher Nyquist zones
(2) The measured power and area include 16 16b DDSs operating at 1.5GHz, they occupy >46% of all synthesized digital logic

Figure 22.3.6: Measured SFDR in dual-rate hybrid mode and performance comparison with state-of-the-art high-speed CMOS DACs.

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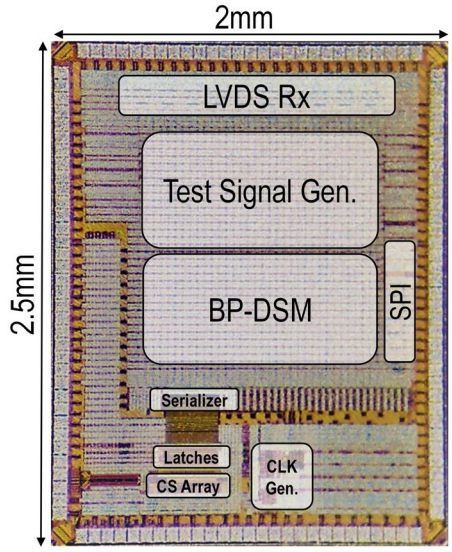

Figure 22.3.7: Die micrograph.

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