A 10-b 800-MS/s Time-Interleaved SAR ADC With Fast Variance-Based Timing-Skew Calibration

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***Abstract*— This paper presents a time-interleaved (TI) SAR analog-to-digital converter (ADC) with a fast variance-based timing-skew calibration technique. It uses a single-comparator-based window detector (WD) to calibrate the timing skew. The WD can suppress variance estimation errors and allow precise variance estimation from a significantly small number of samples. It has low-hardware cost and orders of magnitude faster convergence speed compared to prior variance-based timing-skew calibration technique. The proposed technique brings collateral benefit of offset mismatch calibration. After timing-skew calibration, a prototype 10-b 800-MS/s ADC in 40-nm CMOS achieves the Nyquist-rate SNDR of 48 dB and consumes 4.9 mW, leading to the Walden FoM of 29.8-fJ/conversion step.**

***Index Terms*— Offset calibration, SAR analog-to-digital converter (ADC), time-interleaved (TI) ADC, timing-skew calibration, variance-based timing-skew calibration.**

I. Introduction

THE power consumption of a single-channel analog-to-digital converter (ADC) tends to linearly increase with its sampling rate (f_s) when f_s is small. However, when f_s passes a certain point for a given technology node, the ADC power P increases at much higher rate and the normalized power efficiency (P/f_s) starts to degrade rapidly [1]. Thus, state-of-the-art high-speed ADCs boost the conversion rate not only by increasing the speed of a single-channel ADC, but also by time-interleaving multiple ADC channels running at a lower rate [1]–[13]. For an N-channel time-interleaved (TI) ADC operating at f_s, each sub-ADC channel only needs to operate at f_s/N. Therefore, each sub-ADC can operate in the linear power versus speed region, leading to a significant power saving compared to a single-channel ADC running at the same sampling rate. Despite of its power efficiency, TI-ADC suffers from mismatches among sub-ADC channels, including gain, offset, and timing mismatches. Among them, timing skew is one of the most difficult errors to calibrate as it is nontrivial to extract and its induced error depends on both the frequency and the amplitude of the input signal. It is known to be a performance bottleneck for TI-ADCs.

To reduce timing mismatches, various timing-skew calibration techniques have been developed. In [5] and [6], a foreground timing-skew calibration technique without an extra ADC channel is presented. A signal generator applies a test signal to the TI-ADC, and the relative timing information of sub-channel ADCs is extracted with a Fourier analysis. One limitation of this technique, however, is that it cannot track process, voltage, and temperature (PVT) variations because the system must interrupt the normal ADC operations until the calibration is complete. In [7]–[9], background timing-skew calibration with a dedicated reference channel is reported to address the limitation of the foreground calibration techniques. In [7], a full-blown reference ADC is employed for the calibration. In [8], two reference ADCs are utilized. One is used to estimate the input derivative and the other one functions as a timing-skew free reference. Despite their effectiveness, additional full-blown ADC replicas can substantially increase power and hardware overhead, especially when the interleaved number of channels (N) is small. Also, Chen and Pileggi [7] and Stepanovic and Nikolic [8] set a lower limit on the alignment (beat) period of the reference and each sub-ADC channels to $N(N+1)$ clock cycles, which reduce the calibration speed. Moreover, the alternatingly operated reference can introduce spurs by periodically changing the overall TI ADC input impedance [14]. In [9], the reference channel is simplified to a single comparator to minimize the power and hardware overhead. Nevertheless, the convergence speed of its algorithm is slow for random inputs when it runs in background due to large random variations in the autocorrelation estimation process. The works of [1], [10], and [11] present techniques to calibrate the timing skew in background without an additional reference. Without a separate reference, the ADC input impedance remains constant and no spurs arise from impedance variations. Nonetheless, Wei *et al.* [1] and Lin *et al.* [11] have a tight requirement on the shape of the ADC input autocorrelation function, and Dortz *et al.* [10] have a restriction on input characteristics that input signals must not be close to or above Nyquist rate. In [12] and [13], flash-assisted TI (FATI) SAR ADCs are proposed to address limitations such as tight input restriction and input-impedance variation by having a low-resolution flash ADC running at the ADC full rate. Thanks to the flash, each SAR channel can run faster. However, a flash ADC is power consuming. Lee *et al.* [12] remove the timing skew by reducing the

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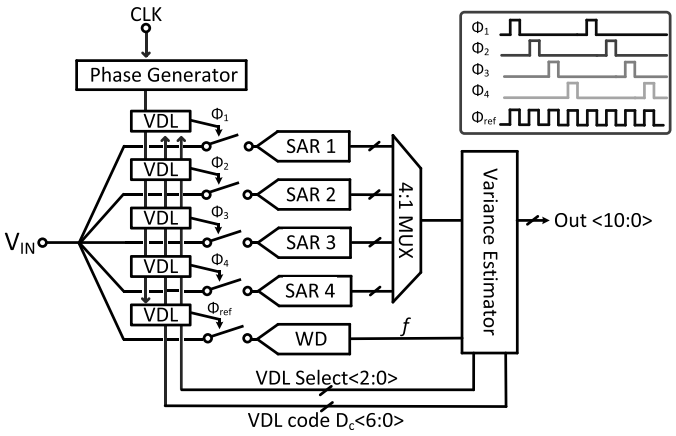

Fig. 1. Block diagram of a four-way TI SAR ADC with the proposed variance-based timing-skew calibration technique.

variance of each SAR channel's output. It is robust against the comparator offset and noise, but its convergence speed is slow when it operates in background with unknown inputs that can cause large fluctuations in the variance estimation.

This paper presents a novel variance-based timing-skew calibration technique for TI ADC. It exploits the relationship between the comparator input and its decision time to identify ADC inputs that are close to the comparator threshold. By using only these samples, the variance computation has much smaller estimation errors. Thus, the proposed technique substantially reduces the number of samples needed to obtain an accurate variance estimation and significantly boosts the convergence speed. Simulation results show that when running in background with random inputs, the convergence speed of the proposed technique is orders of magnitude faster than that of the prior variance-based timing-skew calibration technique of [12]. Furthermore, the proposed technique obviates the need for a flash ADC; instead, it only requires a single-comparator-based window detector (WD), which reduces hardware overhead and power. To verify the proposed technique, a prototype 10-b 800-MS/s ADC is built in 40-nm CMOS. It consumes 4.9 mW and achieves a post-calibration Nyquist-rate signal-to-noise-and-distortion ratio (SNDR) of 48 dB, leading to a Walden Figure-of-Merit (FoM) of 29.8-fJ/conversion step.

This paper is organized as follows. Section II introduces the proposed timing-skew calibration technique. Section III presents the convergence time analysis and the choice of the window width. Section IV discusses the practical design issues and the limitations of the proposed technique. Measurement results are shown in Section V. Conclusion is brought up in Section VI.

II. Time-Interleaved ADC With the Proposed Variance-Based Timing-Skew Calibration

A. Circuit Implementation

Fig. 1 shows the architecture of a four-way TI SAR ADC with the proposed timing-skew calibration technique. It consists of four SAR ADCs, a WD-based reference channel, an output MUX, a multi-phase clock generator, variable delay lines (VDLs), and a variance estimator block. Each of the four sub-ADCs samples the input signal V_{in} at the falling edge of its sampling clock ($\phi_1 \sim \phi_4$). The SAR ADC asynchronously resolves 11-b with 1-b redundancy [15], [16]. After the timing-skew estimation, the variance estimator controls the digitally controlled VDL to closely align the falling edges of $\phi_1 \sim \phi_4$ with those of the WD ϕ_{ref}.

Fig. 2 illustrates the block diagram of the WD. It consists of a replica sampling network, a dynamic latch comparator, a current-starved inverter chain, and a flag D flip-flop (DFF). The WD operates at the full ADC rate (f_s) and thus eliminates the potential spurs from input impedance variations. The variance estimator utilizes the WD to check whether a sampled ADC input V_{in} is within a fixed window, i.e., $|V_{\text{in}}|<W$, where W is the window width. When Φ_{ref} is high, bootstrap switch samples V_{in} and the comparator is reset. As soon as Φ_{ref} goes low, the comparator starts regeneration and the clock signal goes into the current-starved inverter chain. The window flag f is raised when the clock signal (Φ_{delay}) arrives at the DFF before the XOR output (Φ_{XOR}) goes high. The inverter chain is configured as $\tau_{\text{delay}} = \tau_{\text{comp}} + \tau_{\text{XOR}}$, where τ_{XOR} is the XOR delay and τ_{comp} is the comparator delay when $|V_{\text{in}}| = W$. If $|V_{\text{in}}|<W$, the regeneration time of the comparator is longer than that of τ_{comp} and hence raises the flag ($f = 1$). When the flag is high, the variance estimator collects the corresponding ADC output. On the other hand, if $|V_{\text{in}}| > W$, the flag f is not raised ($f = 0$). W can be tuned by adjusting τ_{delay} via controlling the bias current (I_B) into the current-starved inverter chain of the WD. Increasing I_B reduces τ_{delay} as well as W. By contrast, reducing I_B increases τ_{delay} and W.

Fig. 3 shows the schematic of the 10-b single-channel ADC. It uses 1/8 of the conversion period for sampling and the rest for 11-b conversions. Totally, 11 comparators are used for each of 11-b conversion. First stage consists of four conversions, and the second stage consists of seven conversions. The unit capacitor C is 2 fF, and the total digital-to-analog converter (DAC) capacitance is $272C$, including $16C$ of redundancy. A modified bidirectional single-side switching scheme of [16] is used to reduce the number of unit capacitors by 4 times compared to that of the conventional SAR switching technique. The conversion rate of 200 MS/s is achieved by using the loop-unrolled architecture, which greatly reduces the critical path delay [17]–[19]. Offset mismatches of 11 comparators are addressed by using stage segmentation, adding a redundancy bit, and sharing a single-dynamic pre-amplifier [19]. The pre-amplifier is a dynamic latch-based amplifier, driven by the clock Φ_{PRE}, which is active only in the second stage. The pre-amplifier amplifies the residual voltages before the comparison so that the residual voltages are not affected by the comparator offset mismatches in the second stage.

Fig. 4 shows the block diagram of the multi-phase clock generator. The low-voltage differential-signaling receiver converts 400-$\text{mV}_{\text{pk-pk,diff}}$ off-chip input to a single-ended clock ϕ_0 [20]. The transmission gates are controlled by the outputs ($S_1 \sim S_4$) of four DFFs arranged in a ring. One DFF is initialized to 1, and all DFFs are triggered by the falling edge of ϕ_0. This generates four 25%-duty-cycle signals that are 90° apart. Triggering the DFFs with the falling edge of ϕ_0 allows $S_1 \sim S_4$ to not get affected by clk-to-q delay of

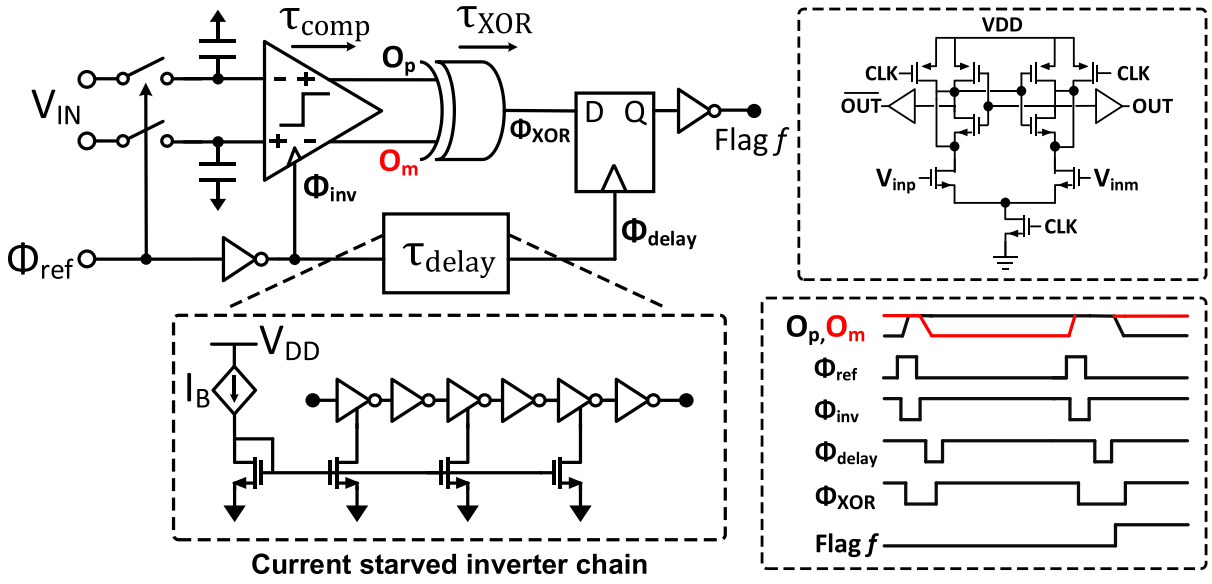

Fig. 2. Block diagram of the comparator-based WD.

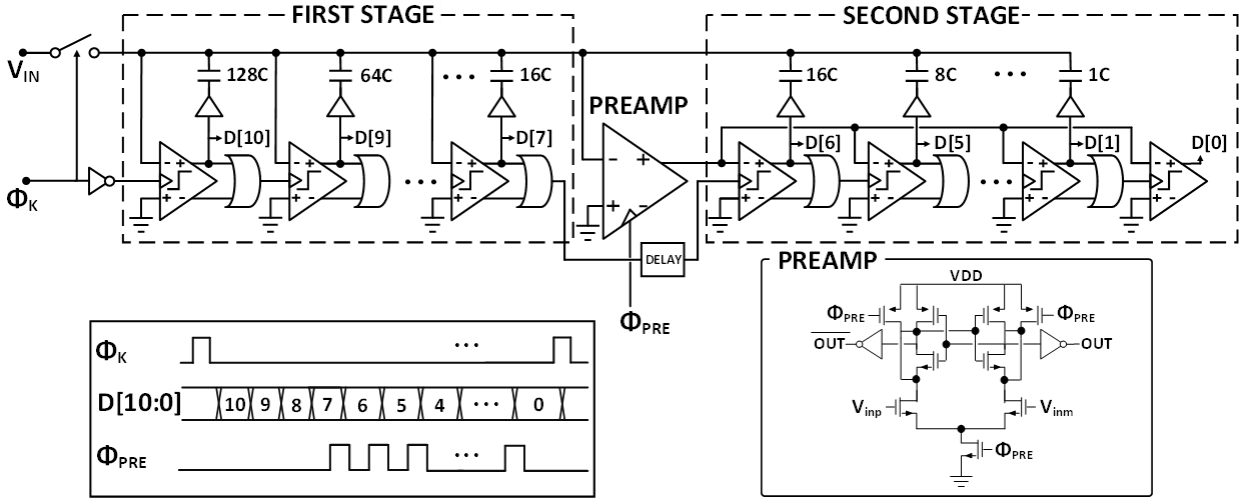

Fig. 3. Block diagram of the single-channel SAR ADC.

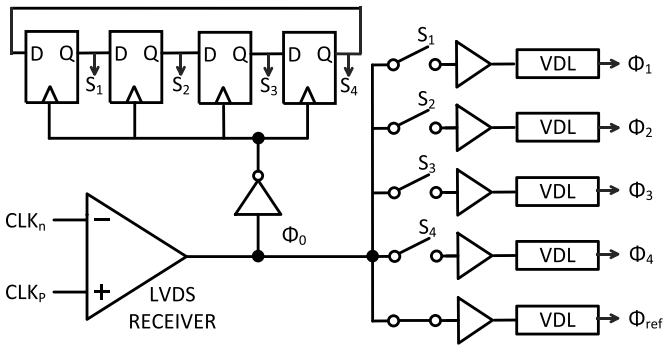

Fig. 4. Block diagram of the multi-phase clock generator.

the DFFs. These pulses control the transmission gates and sequentially pass ϕ_0 every four clock cycles. Given that ϕ_0 is 50% duty cycle, each sub-ADC sampling clock has a duty cycle of 1/8. The advantage of this scheme is low jitter as

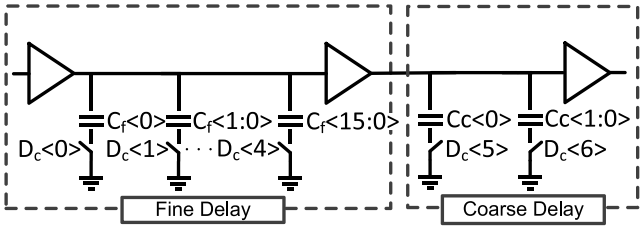

Fig. 5. Block diagram of the VDL for timing-skew calibration.

ϕ_0 only passes through the transmission gate, one buffer, and VDLs to produce $\phi_1 \sim \phi_4$ [21]. Jitters in control pulses ($S_1 \sim S_4$), generated by DFFs, do not affect the critical sampling edges of $\phi_1 \sim \phi_4$.

Fig. 5 shows the block diagram of the VDL. It has 5-b binary-weighted control code for a fine delay tuning of 300 fs per step and 2-b coarse control code with 2 ps per step.

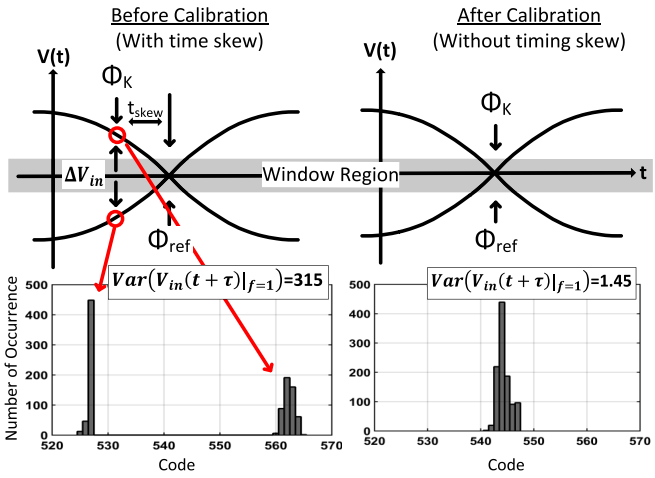

Fig. 6. Basic idea of the proposed variance-based timing-skew calibration.

B. Basic Idea of the Proposed Timing-Skew Calibration Technique

The variance estimator collects all ADC outputs with $f = 1$ and sorts them into four sets depending on which channel they come from. The estimator then computes the sample variance for each of the four sets. When timing skew between a single-channel ADC and the WD exists, the collected ADC outputs are scattered to side corners, which lead to a large variance ($\approx 315\ \mathrm{LSB}^2$), as shown in Fig. 6 for a single-tone sinusoidal input. By contrast, when the timing-skew between the ADC channel and the WD is minimized, the collected ADC outputs are distributed in the center among few codes, which indicates that the variance is at minimum ($\approx 1.45\ \mathrm{LSB}^2$). Thus, the variance is an indicator of the timing skew, which can be reduced by monitoring the sample variance and minimizing it through the VDL delay adjustment.

In addition to timing-skew calibration, the proposed calibration technique collaterally brings the benefit of offset mismatch calibration. When all ADC outputs with $f = 1$ are sorted into four sets, offset mismatch is determined by calculating the mean value of each of four sets. The offset mismatch can be digitally cancelled by subtraction from each channel outputs.

C. Mathematical Explanation of the Proposed Timing-Skew Calibration Technique

The variance of a single-channel ADC's outputs with $f = 1$, denoted as $\sigma_v^2(\tau)$, can be derived as

$$\sigma_v^2(\tau) \equiv \mathrm{Var}(V_{\mathrm{in}}(t+\tau)|_{f=1}) \cong Var\left(V_{\mathrm{in}}(t)+\tau \cdot \frac{dV_{\mathrm{in}}}{dt}|_{f=1}\right) = \sigma_v^2(0) + \tau^2 \cdot \sigma_{dv}^2 \quad (1)$$

where τ is the timing skew between the single ADC channel and the WD, and σ_{dv} represents the standard deviation of dV_{in}/dt conditioning on $f = 1$. In deriving (1), $V_{\mathrm{in}}(t)$ and dV_{in}/dt are treated as uncorrelated random variables due to their inherent orthogonality. It is clear from (1) that $\sigma_v^2(\tau)$ grows quadratically with τ at a rate proportional to σ_{dv} (i.e., input amplitude and frequency). To verify the validity of (1), behavioral simulations are performed for a 10-b 800 MS/s four-way TI ADC for single-tone sinusoidal inputs (amplitude at 0.8 V and frequencies at 99, 190, and 390 MHz), two-tone sinusoidal inputs (amplitude at 0.4 V each and two frequencies of 290 and 390 MHz), and a Gaussian random input with a standard deviation of 0.3 V and a bandwidth of [0, 200 MHz]. Thermal noise is not considered for simplicity. All the performed simulation results include quantization error unless it is noticed. The results are shown in Fig. 7 and match well with (1). Fig. 7 clearly shows the quadratic relationship. As the input frequency increases, $\sigma_v^2(\tau)$ grows more rapidly. For all cases, $\sigma_v^2(\tau)$ is, however, minimized at $\tau = 0$. Therefore, by estimating and minimizing $\sigma_v^2(\tau)$, the timing skew can be corrected, which is the basis of the proposed calibration technique.

III. Convergence Time Analysis and Choice of the Window Width

Convergence time is an important factor for any timing-skew calibration technique. It must be short enough to keep track of temperature and voltage variations due to their strong influences on the timing skew. For the proposed technique, its convergence time is limited by the number of ADC outputs M that is needed to ensure an accurate estimation of $\sigma_v^2(\tau)$. Note that $\sigma_v^2(\tau)$ in (1) is the expected value of the variance. In practice, $\sigma_v^2(\tau)$ needs to be estimated by calculating the sample variance of real ADC outputs with $f = 1$, which is denoted as $s_v^2(\tau)$ and is given by

$$s_v^2(\tau) \equiv \frac{\sum_{m=1}^{M} (V_{\mathrm{in}}[m] - V_{\mathrm{avg}})^2 f[m]}{\sum_{m=1}^{M} f[m]} \quad (2)$$

where V_{avg} represents the sample average, and $f[m]$ is defined as 1 for $|V_{\mathrm{in}}[m]| < W$ and 0 otherwise. The effects of the ADC thermal noise and quantization error are ignored in (2). They are considered in Section IV. Although $s_v^2(\tau)$ converges to $\sigma_v^2(\tau)$ when M goes to infinity, it is not equal to $\sigma_v^2(\tau)$ for any finite M due to the random nature of the input. To ensure the measured $s_v^2(\tau)$ is close to $\sigma_v^2(\tau)$, M must be sufficiently large, which limits the convergence speed.

For the proposed technique, the key parameter that determines M is the window width W. At first glance, a larger W is preferred because a larger portion of ADC input samples falls into the window, and hence more $f = 1$ samples are averaged to estimate more precise variance. However, a larger W substantially increases fluctuations in the variance estimation $\{s_v^2(\tau)\}$. Fig. 8 shows behavioral simulation results for four different W of 6, 12, 24, and 48 LSBs with the same Gaussian random input used in Fig. 7. For every W, a total of 100 sample variances $\{s_v^2(\tau)\}$ are collected, each of which is computed with $M = 10^5$. Fig. 8 clearly shows that the fluctuation in $\{s_v^2(\tau)\}$ significantly increases with W. The variation in $\{s_v^2(\tau)\}$, denoted as σ_s^2, increases by about 8 times for every doubling of W. An intuitive explanation is that a wider window allows input samples with various amplitudes to fall into the

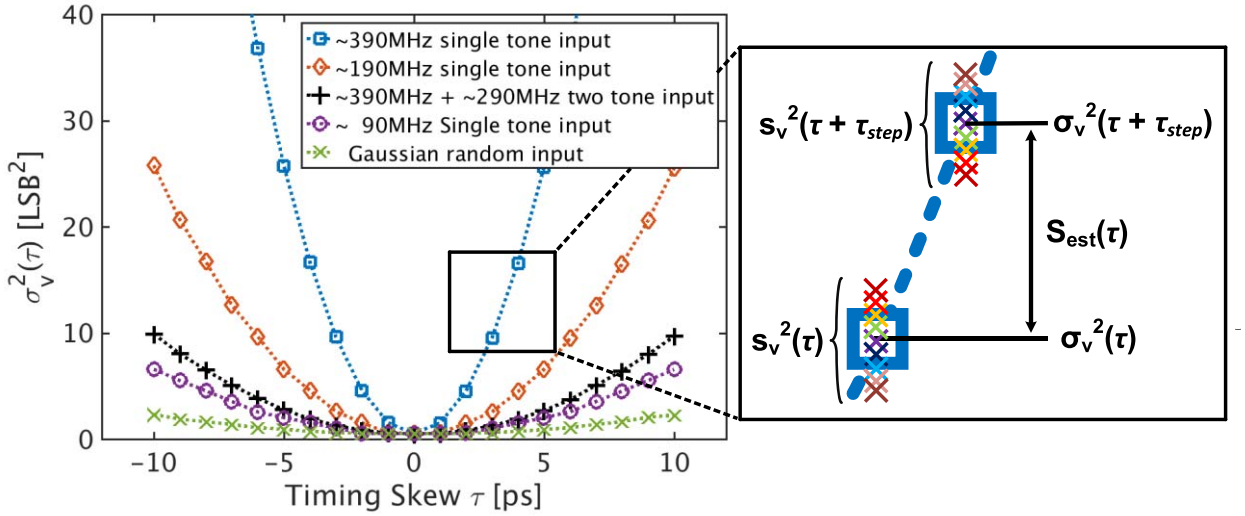

Fig. 7. Behavioral simulation illustrating the relationship between $\sigma_v^2(\tau)$ and τ.

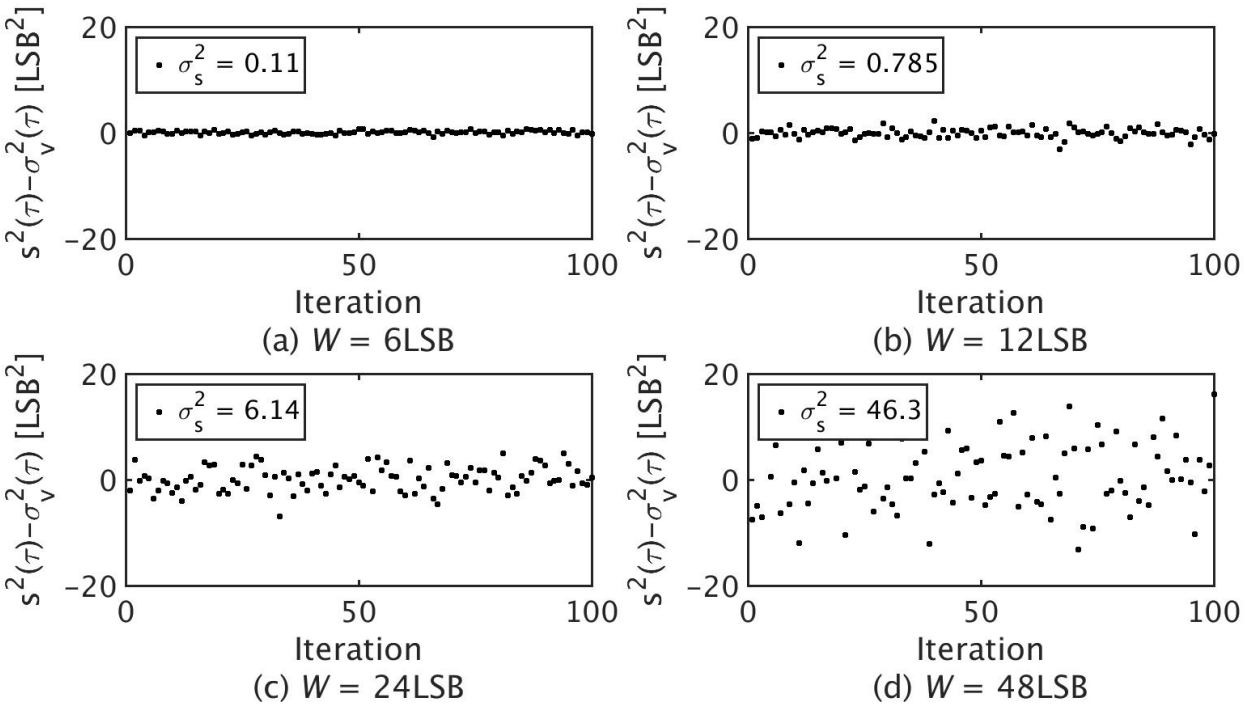

Fig. 8. Behavioral simulation illustrating the relationship between W and the distribution of $s^2(\tau) - \sigma_V^2(\tau)$, for 100 samples.

window and thus leads to greatly increased fluctuation. This fluctuation is considered as "noise" of the estimation process. If the "noise" is large, $s_v^2(\tau)$ will substantially fluctuate from $\sigma_v^2(\tau)$ and it may not accurately represent the timing skew $|\tau|$. To suppress the fluctuation and ensure an accurate timing-skew calibration, a substantially larger M is needed for a larger W, which reduces the convergence speed significantly.

The value of σ_s^2 can be calculated in the following way. For a single sample captured by the WD, the fluctuation in its variance is given by $\mathrm{Var}(V_{\mathrm{in}}^2(t+\tau)|_{f=1})$. Out of M sub-ADC input samples, the number of samples falling inside the window N_f can be expressed as

$$N_f = \sum_{m=1}^{M} f[m] \cong M \cdot P(f=1) = M \cdot p_0 \cdot W \qquad (3)$$

where $P(f = 1)$ is the probability of an input falling inside the window, and it is given by the product of W and the probability density of V_{in} inside the window, denoted as p_0. For simplicity, V_{in} is assumed to be uniformly distributed within the window $[-W, +W]$ in (3), which is valid especially for a small W. Averaging over N_f samples, the

fluctuation in the variance estimation is reduced by N_f times, and thus, σ_s^2 can be computed using the standard statistical analysis as in [22]

$$\begin{aligned}\sigma_s^2(\tau) &\cong \frac{\mathrm{Var}\left(V_{\mathrm{in}}^2(t+\tau)|_{f=1}\right)}{N_f} \\ &\approx \frac{\mathrm{Var}\left(\left(V_{\mathrm{in}}+\tau\cdot\frac{dV_{\mathrm{in}}}{dt}\right)^2|_{f=1}\right)}{N_f} \\ &\approx \frac{\frac{4}{45}W^4+\frac{4}{3}W^2\tau^2\sigma_{dv}^2+2\tau^4\sigma_{dv}^4}{M\cdot p_0\cdot W}. \end{aligned} \tag{4}$$

Similar to (1), the orthogonality of $V_{\mathrm{in}}(t)$ and dV_{in}/dt is used to derive (4). As shown in (4), although N_f linearly increases with W, $\mathrm{Var}(V_{\mathrm{in}}^2(t+\tau)|_{f=1})$ increases with W^4, and thus, the net effect is that $\sigma_s^2(\tau)$ increases with W^3, which explains the cubic relationship as shown in Fig. 8. Consequently, a smaller W is preferred to reduce the fluctuation σ_s^2 and increases the convergence speed. Nevertheless, the value of W should not be chosen to be too small. As can be seen from (4), if W is decreased until it is much smaller than $\tau\cdot\sigma_{dv}$, then $\sigma_s^2(\tau)$ increases back again because $\mathrm{Var}(V_{\mathrm{in}}^2(t+\tau)|_{f=1})$ is dominated by $\tau\cdot\sigma_{dv}$ instead of W. Thus, there exists an optimum value for W, which is comparable to $\tau\cdot\sigma_{dv}$.

So far, only the "noise" component in the variance estimation is discussed. In the calibration process, the "signal" component is also critical in determining the convergence speed. This work adopts the min–max search method similar to [9] to minimize the sample variance. Basically, it computes and compares the current sample variance $s_v^2(\tau)$ and its adjacent sample variance $s_v^2(\tau+\tau_{\mathrm{step}})$, where τ_{step} is the unit step size of the VDL, as shown in Fig. 7 (right). If $s_v^2(\tau) < s_v^2(\tau+\tau_{\mathrm{step}})$, it implies that $\tau > 0$ and the VDL must be adjusted to decrease τ. On the other hand, if $s_v^2(\tau) > s_v^2(\tau+\tau_{\mathrm{step}})$, then $\tau < 0$ and the VDL should be tuned to increase τ. Therefore, the "signal" component that directs the VDL to a smaller $|\tau|$ is the difference between $s_v^2(\tau)$ and $s_v^2(\tau+\tau_{\mathrm{step}})$, which is essentially the derivative of $\sigma_v^2(\tau)$ of (1). Thus, the magnitude of "signal" in the estimation process, denoted as $S_{\mathrm{est}}(\tau)$, can be computed as

$$S_{\mathrm{est}}(\tau) = \tau_{\mathrm{step}}\cdot\left|\frac{d}{d\tau}\sigma_v^2(\tau)\right| = 2\tau_{\mathrm{step}}\cdot|\tau|\cdot\sigma_{dv}^2. \tag{5}$$

$S_{\mathrm{est}}(\tau)$ is proportional to τ_{step} because the difference between $\sigma_v^2(\tau)$ and $\sigma_v^2(\tau+\tau_{\mathrm{step}})$ increases with τ_{step}. $S_{\mathrm{est}}(\tau)$ also increases with $|\tau|$ due to the quadratic dependence of $\sigma_v^2(\tau)$ on τ in (1).

To ensure a robust calibration, $S_{\mathrm{est}}(\tau)$ needs to be larger than the "noise" component in the variance estimation, which is σ_s of (4). Otherwise, the random fluctuation in the variance estimation can tune the VDL toward a wrong direction. Combining (4) and (5), the SNR in the proposed timing-skew calibration process quantifies how likely the VDL will move toward a correction and is defined as

$$\begin{aligned}\mathrm{SNR}_{\mathrm{est}}(\tau) &\equiv \frac{S_{\mathrm{est}}(\tau)}{\sqrt{2}\sigma_s(\tau)} \\ &= \frac{2\cdot\tau_{\mathrm{step}}\cdot|\tau|\sigma_{dv}^2}{\sqrt{\frac{2}{M\cdot p_0\cdot W}\cdot\left(\frac{4}{45}W^4+\frac{4}{3}W^2\tau^2\sigma_{dv}^2+2\tau^4\sigma_{dv}^4\right)}} \end{aligned} \tag{6}$$

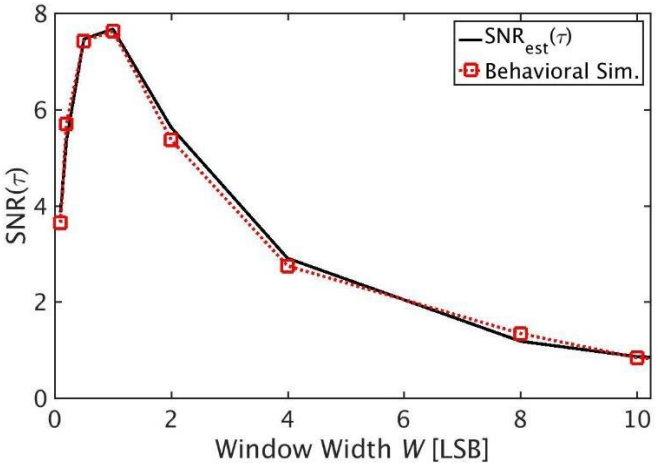

Fig. 9. Relationship between $\mathrm{SNR}_{\mathrm{est}}(\tau)$ and W.

where the $\sqrt{2}$ term comes from the fact that the "noise" power doubles when subtracting $s_v^2(\tau)$ from $s_v^2(\tau+\tau_{\mathrm{step}})$. A large SNR_{est} guarantees that the VDL tuning is on the right direction. For example, if $SNR_{\mathrm{est}} = 3$, it means that the "signal" is 3 times greater than the "noise" in the sample variance comparison. Thus, the probability of the VDL making a correct move toward minimizing τ is 99.85%, which is the cumulative distributive function 3σ of a normal distribution. By contrast, if $\mathrm{SNR}_{\mathrm{est}} = 1$, this probability drops to 84%. In other words, the VDL tuning is 16% incorrect, which may cause large residue timing-skew errors. The $\mathrm{SNR}_{\mathrm{est}}$ can be used as a barometer to check if the value of M is chosen appropriately. For instance, if $\mathrm{SNR}_{\mathrm{est}}$ is below the target (e.g., <3), M must be increased. Likewise, if $\mathrm{SNR}_{\mathrm{est}}$ is higher than needed, M can be reduced to increase the convergence speed.

Fig. 9 plots the simulated relationship between $\mathrm{SNR}_{\mathrm{est}}(\tau)$ and W of the proposed technique. The same Gaussian random input model is applied and $M = 10^5$ is used. Quantization error is not considered in the simulation for simplicity. The $\mathrm{SNR}_{\mathrm{est}}(\tau)$ is computed with $\tau = 5$ ps and $\tau_{\mathrm{step}} = 1$ ps. $\mathrm{SNR}_{\mathrm{est}}(\tau)$ is maximized at around $W = 1$ LSB. This is because the "noise" component $\sigma_s^2(\tau)$ is minimized as explained earlier when discussing (4). In the prototype ADC, W is set to 1 LSB to maximize $\mathrm{SNR}_{\mathrm{est}}(\tau)$. With $M = 10^5$ and each ADC channel operating at 200 MS/s, this translates to a short calibration step time of only 0.5 ms.

According to (4), if a wider W is used, M must be increased proportional to W^3 to maintain the same $\mathrm{SNR}_{\mathrm{est}}(\tau)$. The simulation results with Gaussian random inputs shown in Fig. 10 verify this cubic relationship, analytically derived in (4). Behavioral simulation also shows that the variance-based calibration technique of [12] would require $M = 10^9$ samples to obtain the same $\mathrm{SNR}_{\mathrm{est}}(\tau)$ as the proposed technique with $W = 1$ LSB and $M = 10^5$, under the same input signal condition. The reason for this significantly longer convergence time is that [12] essentially uses a 4-b flash ADC as 16 WDs, whose equivalent window size W is 64 LSB.

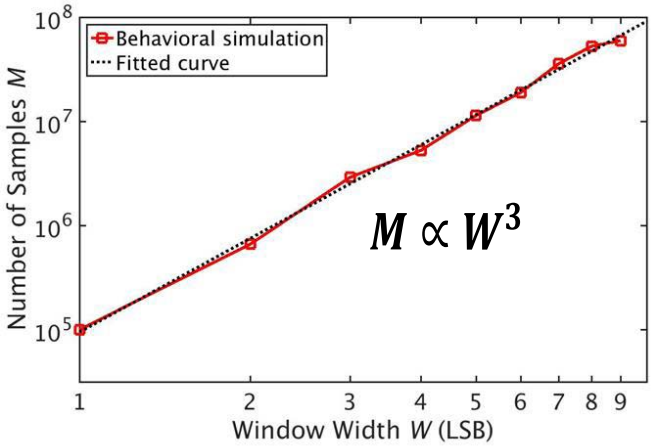

Fig. 10. Behavioral simulation results illustrating dependence of M on W.

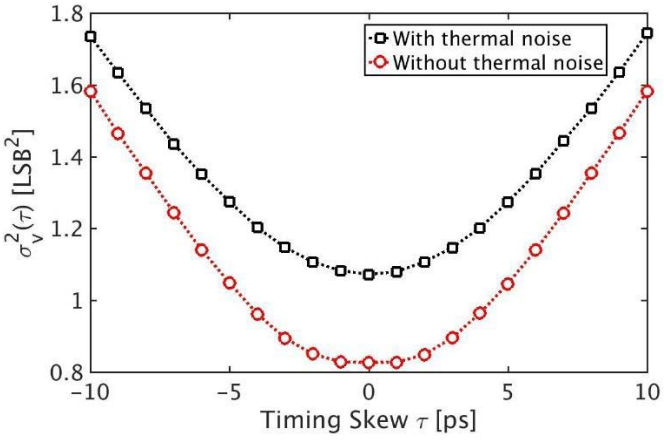

Fig. 11. Behavioral simulation that illustrates the relationship between variance $\sigma_v^2(\tau)$ and τ with and without thermal noises.

Thus, the convergence speed ratio of the 16 WDs with W of 64 LSB is approximately $64^3/16 = 2^{14} \approx 10^4$. Although Lee *et al.* [12] do not utilize the actual WD to collect ADC outputs, it computes variance points over the ADC outputs that are within the range of 64 LSB. Moreover, all ADC outputs are used for the computation and thus, it is equivalent to collecting ADC outputs with 16 WDs with W of 64 LSB.

In addition to a much faster convergence speed, the proposed calibration technique also substantially reduces the power consumption needed for the variation computation. For instance, if the calibration runs full time to track PVT variations, the calibration digital logics of [12] must run at full speed since all M ADC samples are used to compute the variance, which may consume a significant amount of power. By contrast, the proposed technique requires only a small number of samples (N_f) falling inside the window. The proposed technique therefore is inactive for most inputs and hence the power consumption can be greatly reduced.

IV. Effects of Nonidealities and Constraint of the Proposed Calibration Technique

A. Effect of Thermal Noise

The comparator dominates the input referred noise of both the ADC and the WD. Assuming the comparator input referred noise is v_n, $\sigma_v^2(\tau)$ can be re-derived as

$$\sigma_v^2(\tau) = \mathrm{Var}(V_{\mathrm{in}}(t+\tau) + v_n|_{f=1}) \cong \sigma_v^2(0) + \tau^2 \cdot \sigma_{dv}^2 + \sigma_n^2 \tag{7}$$

where σ_n is the rms input referred noise of the comparator. The quadratic relationship between $\sigma_v^2(\tau)$ and τ is maintained. Thus, the "signal" component of the proposed calibration technique is unaffected by v_n. The only change is that $\sigma_v^2(\tau)$ is up-shifted by the noise power. The behavioral-level simulation results shown in Fig. 11 with 1 mV rms noise confirm the result of (7).

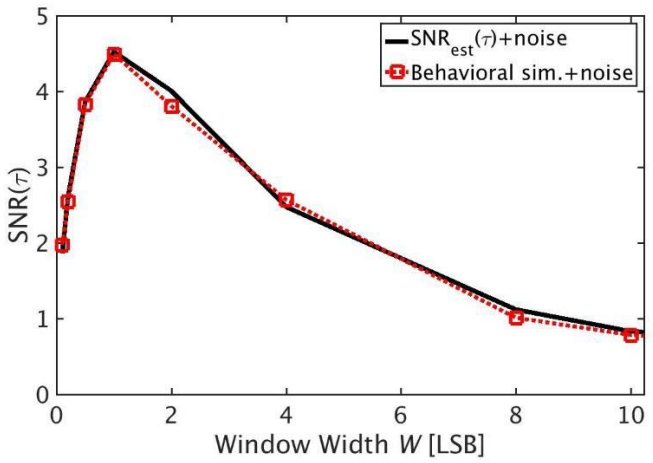

Fig. 12. Behavioral simulation that illustrates the relationship between $\mathrm{SNR}_{\mathrm{est}}(\tau)$ and W with thermal noises.

The "noise" component $\sigma_s^2(\tau)$ is re-derived by using the standard statistical calculation

$$\sigma_s^2(\tau) \approx \frac{\mathrm{Var}((V_{\mathrm{in}}(t+\tau) + v_n|_{f=1})^2)}{M \cdot P_n(f=1)} \approx \frac{\frac{4}{45}W^4 + \frac{4}{3}W^2\tau^2\sigma_{dv}^2 + 2\tau^4\sigma_{dv}^4 + \frac{8}{3}W^2\sigma_n^2 + 8\tau^2\sigma_{dv}^2\sigma_n^2 + 8\sigma_n^4}{M \cdot p_0 \cdot W}. \tag{8}$$

As expected, the presence of thermal noise increases the fluctuation of the sample variance, degrading $\mathrm{SNR}_{\mathrm{est}}(\tau)$. Fig. 12 shows $\mathrm{SNR}_{\mathrm{est}}(\tau)$ versus W with 1 mV rms noise. Like in Fig. 9, quantization error is not considered in this simulation for simplicity. The behavioral simulation results closely track the derived results based on (7) and (8). Compared to Fig. 9 without noise, the $\mathrm{SNR}_{\mathrm{est}}(\tau)$ in Fig. 12 reduces due to increaed $\sigma_s^2(\tau)$. However, it is still greater than three with $W = 1$ LSB, and thus, M of 10^5 is still sufficient to ensure the correct timing-skew calibration.

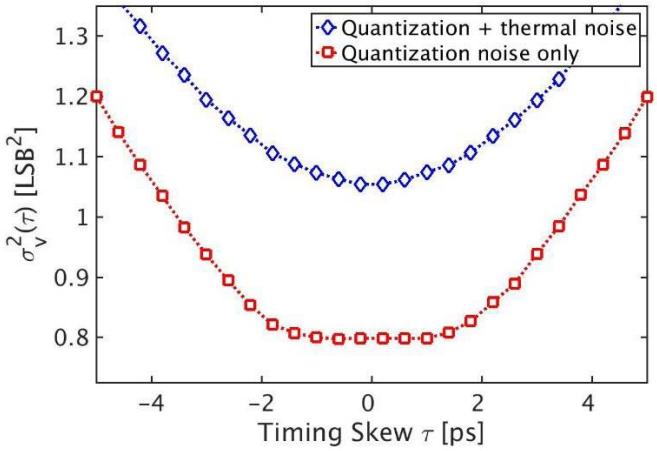

Fig. 13. Behavioral simulation illustrates the dead zone and its removal by thermal noise.

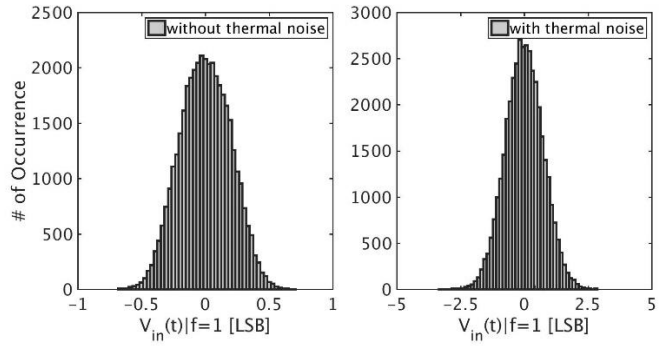

Fig. 14. Behavioral simulation demonstrates the distribution of $V_{\text{in}}(t)|f = 1$ samples with and without thermal noise of $1mV_{\text{rms}}$.

B. Effect of Quantization Error

Quantization error can potentially cause errors in the timing-skew calibration if the parameters are not chosen appropriately. For instance, if $W \ll 1$ LSB, $\sigma_n \ll 1$ LSB, and the timing skew τ is small, most of ADC inputs falling inside the window are converted to the same digital code, regardless of the exact value of τ. Thus, the variance cannot distinguish different τ values, leading to a flat region in the $\sigma_v^2(\tau)$ versus τ curve. Fig. 13 shows the behavioral simulation result with $W = 0.25$ LSB and $\sigma_n = 0$. $\sigma_v^2(\tau)$ is flat within τ of $[-1.5, 1.5]$ ps. Inside this dead zone, the variance estimator cannot determine the direction of the VDL, causing a failure in the timing-skew calibration. Fortunately, this problem can be addressed by the intrinsic thermal noise of the ADC and the WD. As shown in Fig. 14, in the absence of the thermal noise, the ADC input falling inside the window has a narrow distribution, and thus, most of them convert to the same middle code, leading to the dead zone. By contrast, in the presence of thermal noise $\sigma_n \approx 0.5$ LSB (i.e., 1 mV), the ADC inputs falling inside the window have a much wider spread. Quantization error is effectively linearized by the thermal noise dithering and hence can be considered as a random noise. As a result, the dead zone is removed as shown in Fig. 13. Since the ADC thermal noise is usually comparable or bigger than the quantization error in most situations, the effect of quantization error is minor and can be treated just as a slight increase in the overall ADC noise.

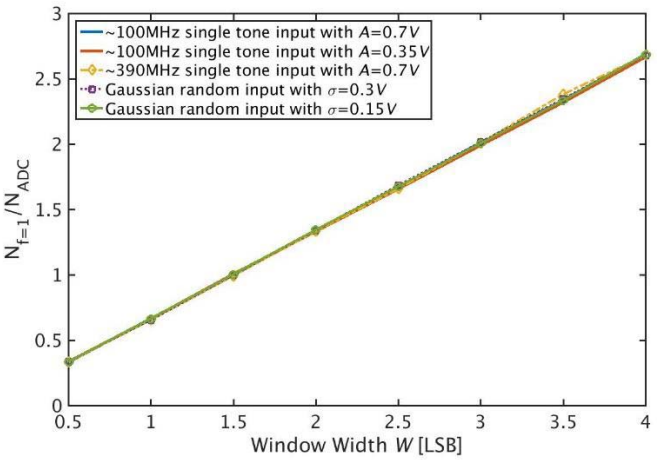

Fig. 15. Behavioral simulation demonstrates the relationship between N_f/N_{ADC} and the window width W with different inputs.

C. Background Tuning of the Window Width

As discussed earlier, the window width W has a strong influence on the convergence time and it is preferred to be set as 1 LSB. Unfortunately, W is sensitive to PVT variations because W is controlled by the current-starved inverter chain delay τ_{delay} (see Fig. 2). For this reason, it is necessary to develop a background calibration scheme that enables an accurate tuning of the bias current I_B to ensure W is always equal to 1 LSB, regardless of PVT variations. The key to the background calibration loop is a method to measure W. Since it is nontrivial to sense W directly, W is measured indirectly by monitoring the number of ADC input samples that fall into the window, which is N_f. As shown in (3), N_f is linearly proportional to W. Since N_f can be easily counted, if the mapping between N_f and W is known *a priori*, I_B and W can be adjusted to reach the target N_f that corresponds to $W = 1$ LSB. However, the problem of this approach is that the ratio between N_f and W depends on the input signal distribution. For a nonstationary input, the mapping coefficient is unknown and varies with time. To overcome this difficulty, instead of using the unreliable direct mapping between N_f and W, the number of ADC output samples that fall into the digital window of $\{-1, 0, +1\}$ LSB, denoted as N_{ADC}, is monitored. The code of 0 LSB represents the ADC middle code with $V_{\text{in}} = 0$ V. Since the high-level operation of the ADC is to map an analog input to a digital output with small random perturbations, it is easy to show that a digital window of $[-1, +1]$ LSB at the ADC output corresponds to an analog window of $[-1.5, +1.5]$ LSB at the ADC input, considering the effect of quantization error. Thus, $N_f/N_{\text{ADC}} = 2/3$ for $W = 1$ LSB, $N_f/N_{\text{ADC}} > 2/3$ for $W > 1$ LSB, and $N_f/N_{\text{ADC}} < 2/3$ for $W < 1$ LSB. Note that this relationship is robust and insensitive to the

input signal characteristics. The simulation results shown in Fig. 15 validate this key observation: regardless of the input signal types (sinusoidal or random) and amplitudes, $N_f/N_{\mathrm{ADC}} = 2/3$ for $W = 1$ LSB. Thus, by tuning I_B to ensure $N_f/N_{\mathrm{ADC}} = 2/3$, W can be always kept at 1 LSB, even in the presence of PVT variations.

The unit step size for W calibration (ΔI_B) is determined based on its effect on $\mathrm{SNR_{est}}$. From (6), $\mathrm{SNR_{est}}$ degrades by almost 10% when W is shifted by 1/2 LSB. Therefore, the unit step is designed to shift W by 1/4 LSB so that the $\mathrm{SNR_{est}}$ degradation is less than 10% after calibration. Based on the measurement results, approximately, ΔI_B of 70 μA shifts W by 1/4 LSB. Considering the full calibration range is from 0 to 5 LSB, 5 b of ΔI_B is sufficient for W calibration. About 10^4 samples are needed for an accurate estimation of N_f/N_{ADC} for each calibration cycle. The total calibration time for W considering all these design matters is still short (<100 μs).

D. Practical Limitations of the Proposed Timing-Skew Calibration Technique

As in many background timing-skew calibration schemes, the proposed technique has some restrictions on the ADC input signal. First, it requires the input to have frequent zero crossings to collect enough samples that fall into the window. In addition, the amplitude and frequency of the input signal need to be reasonably large so that the zero-crossing slope dV_{in}/dt is not too small, as otherwise, the influence of the timing skew τ on the sample variance may be too weak, leading to a slow convergence. Furthermore, input frequency (f_{in}) must not be equal to $N \times f_{S,\mathrm{CH}}$,where $f_{S,\mathrm{CH}}$ is the sampling frequency of single channel and N is an integer number. If f_{in} is equal to $N \times f_{S,\mathrm{CH}}$, each ADC channel samples the same input all the time and the variance will be 0. These requirements, however, are not difficult to satisfy in practical applications. As indicated in Fig. 7, the proposed technique works well for both sinusoidal signals and wideband random signals, which cover a wide application space. However, this technique does not work with dc or a pulse wave input, which does not satisfy the above specifications of the input signals.

V. Measurement Results

The proposed calibration technique is applied to an 800-MS/s four-way TI ADC in 40-nm CMOS. Fig. 16 shows the measured spectrum of the TI ADC before and after using the proposed offset calibration scheme (see Section II-B). The offset tone at 200 MHz is suppressed from −38 to −69 dBFS. The capacitor DAC (CDAC) mismatches of all four channels were not impeding the TI-ADC to achieve the targeted linearity of 48 dB, and thus, no calibration scheme was needed to calibrate CDAC mismatches. The gain mismatch is calibrated in the digital domain. Fig. 17 shows the measured spectrum of the TI ADC (left) and a single channel (right) before timing-skew calibration at a low input frequency $f_{\mathrm{in}} = 10$ MHz. The measured SNDR and spurious-free dynamic range (SFDR) of the single-channel ADC are 52 and 60 dB, respectively. The tones in the spectrum of the single-channel ADC are noticed

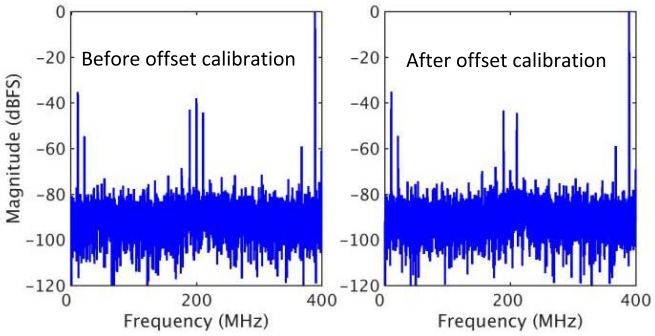

Fig. 16. Measured spectrum of the TI ADC (Left) before and (Right) after offset calibration with the proposed technique.

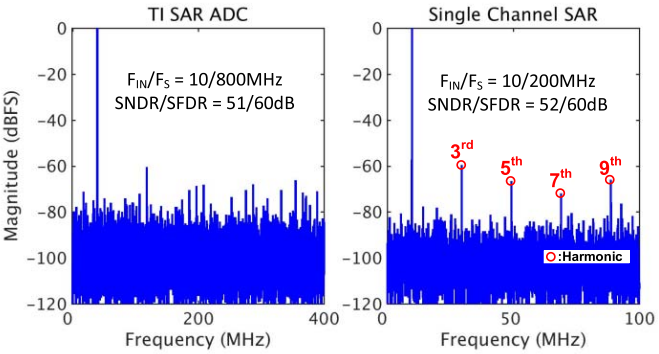

Fig. 17. Measured spectrum of the (Left) TI-ADC and a (Right) single channel before timing-skew calibration with the input frequency of 10 MHz.

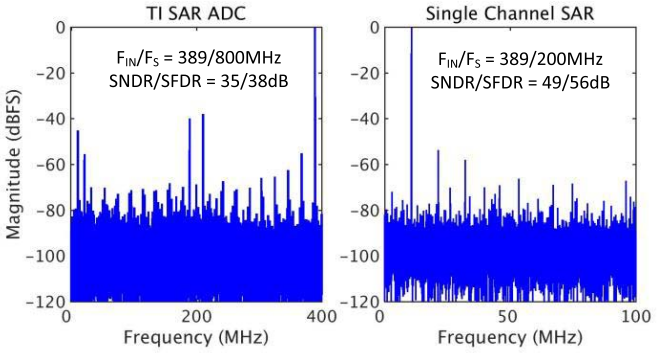

Fig. 18. Measured spectrum of the (Left) TI-ADC and a (Right) single channel before timing-skew calibration with the Nyquist input at 389 MHz.

to be the odd input harmonics. Timing-skew indicated errors are insignificant and do not limit the TI ADC performance. The measured 51-dB SNDR of the TI ADC is limited by the performance of the single-channel ADC. The 1-dB SNDR difference between the single-channel ADC and the TI ADC comes from remaining offset and gain mismatches among the four ADC channels. Fig. 18 shows the measured spectrum of the TI ADC (left) and the single channel (right) before timing-skew calibration with a near Nyquist input $f_{\mathrm{in}} = 389$ MHz. The measured single-channel ADC SNDR and SFDR are 49 and 56 dB, respectively. The 3 dB performance degradation compared to the low frequency (see Fig. 17, right) is mainly

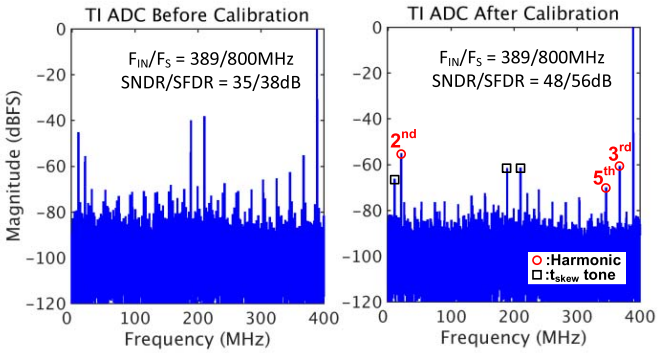

Fig. 19. Measured spectrum of TI-ADC (Left) before and (Right) after timing-skew calibration with the Nyquist input at 389 MHz.

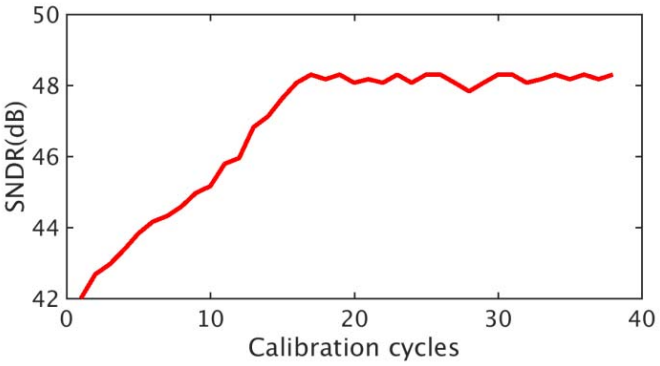

Fig. 21. Measured SNDR versus calibration cycles.

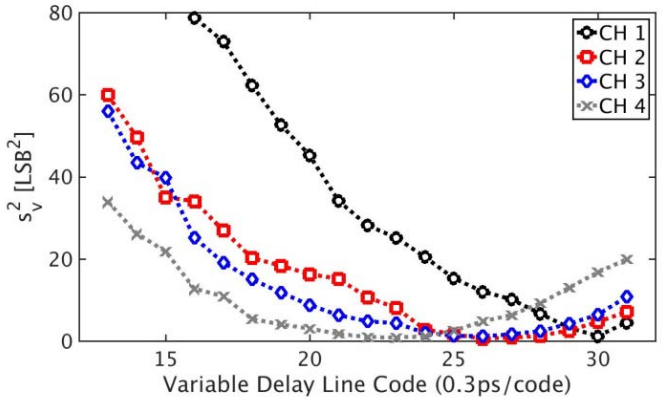

Fig. 20. Measured variance of inputs falling in the window s_v^2 versus VDL control code.

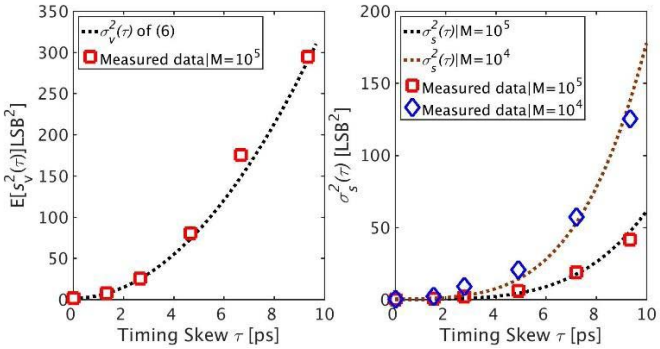

Fig. 22. Measured mean $E(s^2(\tau))$ and fluctuation $\sigma_s^2(\tau)$ of 100 samples of $s^2(\tau)$.

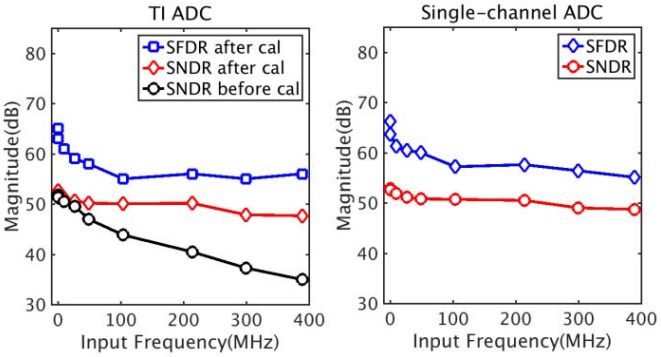

Fig. 23. Measured SNDR and SFDR versus the input frequency of TI ADC and a single channel.

due to increased distortions. The noise floor is almost the same, which indicates that the error due to clock jitter is negligible. The TI ADC SNDR and SFDR at Nyquist are 35 and 38 dB, respectively, which are limited by the timing-skew tones. Fig. 19 compares the spectrum of the TI ADC with the Nyquist rate input before (left) and after (right) timing-skew calibration. After calibration, the timing-skew tones are reduced to below -61 dBFS and the SFDR is limited by the second harmonic of input. The SNDR and SFDR are improved to 48 and 56 dB, respectively, which are close to the performance of the single-channel ADC [see Fig. 18 (right)], indicating that channel mismatches have been greatly suppressed.

Fig. 20 shows that the measured sample variance s_v^2 as a function of the VDL control code. s_v^2 for each channel reaches its minimum after the proposed timing-skew calibration. The minimum points are positioned at different locations due to random process variations, but only 1 minimum point is observed, and the overall quadratic shape matches the analyses in Section II and III. Fig. 21 illustrates the SNDR versus the calibration cycles. Seventeen cycles are needed to minimize variances of all four channels, and the SNDR improves from 42 to 48.3 dB and remains at 48 dB for the rest of the cycles.

Fig. 22 (left) shows the measured mean of the sample variance $\{s_v^2(\tau)\}$ across 100 times measurements with a full-scale 389-MHz sinusoidal input. As expected, the measurement results match well with $\sigma_v^2(\tau)$ of (6). Fig. 22 (right) shows the measured rms fluctuation of the sample variances for $M = 10^4$ and 10^5. The measurement results also closely track $\sigma_s^2(\tau)$ derived in (7), confirming the validity of the theoretical analyses. Measurements also show that for $M = 10^5$, only about 200 input samples fall into the window and are used to compute the sample variance $s_v^2(\tau)$ of each channel. Thus, the amount of digital computation and power is much less than that of [12], which requires the variance computation for every sample.

Fig. 23 shows the measured SNDR of the TI-ADC and single-channel versus the ADC input frequency. Before the timing skew calibration, the SNDR decreases monotonically as the input frequency increases. After the proposed

TABLE I
ESTIMATION TECHNIQUE COMPARISON SUMMARY

	ISSCC '02 Poulton	ISSCC '10 Greshishchev	JSSC '11 El-Chammas	JSSC '13 Stepanovic	ISSCC '14 Dortz	JSSC '14 Wei	JSSC '14 Lee	This Work
Calibration classification	Foreground (Require specific input)		Background (Can work with random input)					
Estimation technique	FFT analysis		Cross correlation-based estimation	Input slope estimation		Autocorrelation-based estimation	Variance-based estimation	
Extra hardware requirements	Test signal generator		Single comparator reference	2 full-blown ADCs	Digital FIR filters	None	Flash ADC	1 window detector
Limitations	Cannot track PVT		Requires sufficiently large dv_{in}/dt, $f_{in} \neq k \times f_{S,CH}$					
	Requires a signal generator		Inputs must cross zeros	Slope estimation heavily depends on f_{in}	f_{in} is constrained up to $f_s/2$	Constraint on shape of input autocorrelation function	Power hungry Flash ADC	Inputs must cross zeros
				Large hardware overhead	Power hungry digital FIR filters			

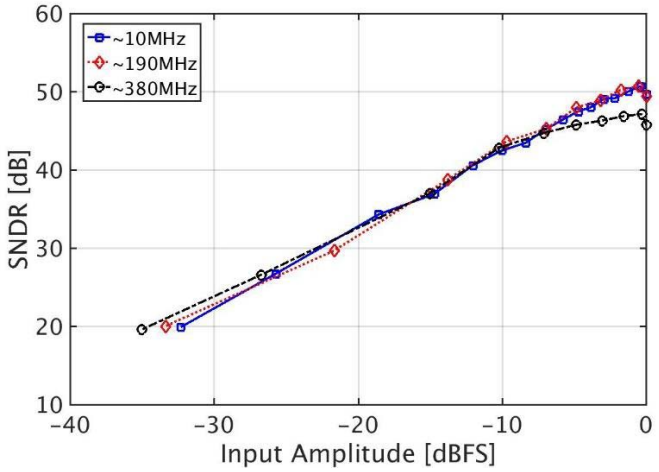

Fig. 24. Measured SNDR versus the input amplitude with three input frequencies.

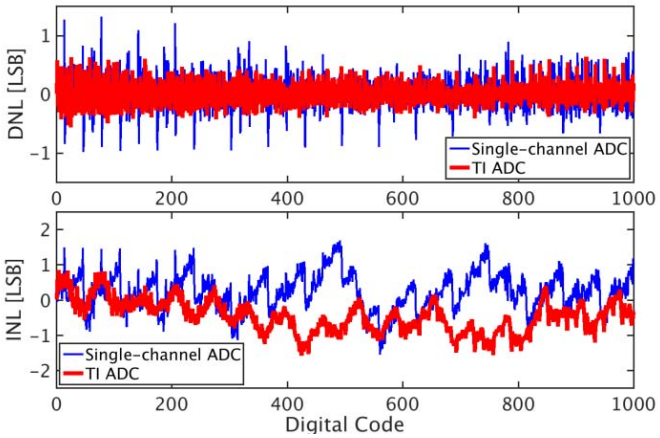

Fig. 25. Measured DNL and INL of TI ADC and a single channel.

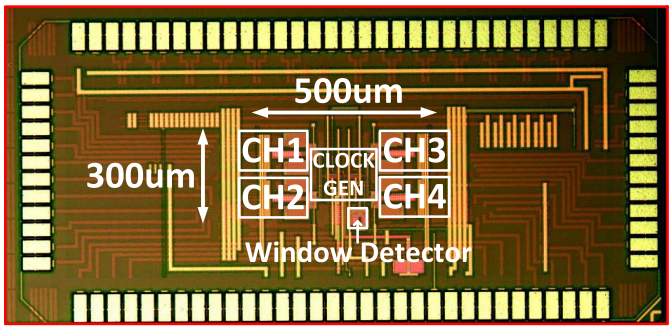

Fig. 26. Die photograph.

timing-skew calibration, the SNDR stays above 48 dB across the entire Nyquist band. What limits the linearity of the TI-ADC is noticed to be the linearity of a single channel. The SNDR/SFDR of the single channel in Fig. 23 closely track those of the TI-ADC after calibration. This also proves that the timing-skew errors are removed and the TI-ADC performance is no longer limited by timing skew. Fig. 24 shows the measured SNDR versus the input amplitude for three different frequencies. The measured INL and DNL of the TI-ADC and the single-channel ADC are shown in Fig. 25. The INL and DNL of the TI-ADC are +1/−1.5 LSB and +0.7/−0.6 LSB, respectively. The INL and DNL of the single-channel ADC are +1.7/−1.5 LSB and +1.3/−0.9 LSB, respectively. The INL and DNL of the TI-ADC are slightly improved due to the randomization effect from interleaving multiple channels.

Fig. 26 shows the chip microphotograph, and the active area is 500 μm by 300 μm. Clock generator is in the center and the four SAR ADCs are symmetrically placed around the clock generator. The WD is in the right corner of the clock generator and it only occupies a small area compared to the SAR ADC channels. The total ADC power is 4.9 mW with

TABLE II
PERFORMANCE SUMMARY

Parameters	JSSC '13 Stepanovic	ISSCC '14 Dortz	JSSC '14 Lee	ISSCC '15 Sung	ISSCC '16 Lin	This work
Architecture	TI-SAR	TI-SAR	FATI-SAR	FATI-SAR	TI-SAR	TI-SAR
Technology (nm)	65	40	65	45	40	40
Supply Voltage (V)	1.2	1.1	1	1.1	1.1	1.1
Fs (GS/s)	2.8	1.62	1	1.6	2.6	0.8
Resolution (bit)	11	9	10	10	10	10
Power (mW)	44.6	93	18.9	17.3	18.4	4.9
SNDR @Nyquist (dB)	50	48	51.4	56.1	50.6	48
FoM (fJ/conv-step)	78	283	62.3	21	25.6	29.8
Active Area (mm2)	0.63	0.83	0.78	0.36	0.825	0.15

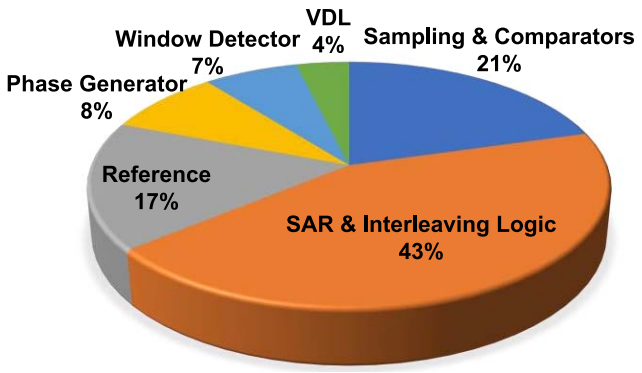

Fig. 27. Power consumption break down at $f_s = 800MHz$ and $V_{\mathrm{DD}} = 1.1V$.

1.1 V power supply. The power break down at $f_s = 800$ MHz and $V_{\mathrm{DD}} = 1.1$ V is illustrated in Fig. 27. The SAR and the interleaving digital logic consume the largest portion of power. The WD only consumes about 7% of the total power, which proves that its power overhead is small. To estimate the digital hardware cost to compute the variance of ADC outputs, the variance computation hardware is digitally synthesized. One of the key techniques that reduce the power of the proposed work is subtracting the middle code from the collected ADC outputs. Since all the collected ADC outputs are near $[-1, 1]$ LSB, the subtraction leaves only few LSB bits to be active in the hardware and substantially reduces the activity rate as well as the power. Based on the measurement results, where only 200 flags are raised among 10^5 ADC outputs, the hardware is assumed to be active with a frequency of $\approx$2 MHz and the estimated power consumption is less than 5% of the total ADC power. Table I summarizes and compares the estimation techniques and limitations of different calibration methods. Table II summarizes and compares the performance of this prototype ADC to previously published works with similar speed and resolution. Overall, it achieves a Walden FoM of 29.8-fJ/conversion step at the Nyquist frequency, which is comparable to that of the state of the arts.

VI. CONCLUSION

This paper presented a novel variance-based timing-skew calibration technique for TI ADCs. The proposed technique uses a simple low-power dynamic comparator and exploits the relationship between the comparator input and its decision time to identify ADC inputs that fall into a small window. By computing the variance only for inputs falling inside the window, the variance estimation error is significantly reduced, leading to a substantially boosted convergence speed. The proposed technique has low hardware and power cost. In addition, because the comparator-based WD runs at full ADC rate, it does not periodically perturb the ADC input impedance. This paper also presented analyses of the "signal" and "noise" in the timing-skew calibration process and showed the advantage of having a small window width in accelerating the convergence. Both simulation and measurement results match well with those from analyses.

ACKNOWLEDGMENT

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