A 10-b 600-MS/s 2-Way Time-Interleaved SAR ADC with Mean Absolute Deviation Based Background Timing-Skew Calibration

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***Abstract*—This paper presents a time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with a novel mean absolute deviation (MAD) based timing-skew calibration technique. It features two highlights. First, Its computation complexity is very low, only involving subtraction and taking absolute value. Second, its convergence speed is fast with even random signals. A prototype 10-b 600-MS/s 2-way TI-SAR ADC in 40-nm CMOS achieves the peak SNDR of 56dB and 52 dB across the entire Nyquist band. Power consumption is 4.7mW and it leads to the Walden FoM of 23.8-fJ/conversion step.**

I. Introduction

TI-SAR is an energy-efficient ADC architecture for high-speed and medium resolution applications, but it suffers from offset, gain, and timing-skew mismatches. Among them, timing skew is the most difficult error to calibrate as it is nontrivial to extract and it worsens proportional to the input frequency and amplitude. Currently existing background timing-skew calibration techniques have different trade-offs among hardware complexity, power and area cost, convergence speed, input-impedance modulation, and restriction on the input signal. [1] presents timing-skew calibration technique with fast convergence speed. This technique, however, has a large area and power cost, due to 2 additional full-blown reference channels. In addition, the ADC input impedance is periodically modulated, which can cause spur and inaccurate calibration. The autocorrelation-based technique of [2] employs only 1 comparator as a reference, reducing power and area. Nevertheless, trade-off for this technique is a slow convergence speed in background operation with random inputs. [3] and [4] present the techniques without any additional channel. These calibration methods, however, have tight restrictions on the shape of input autocorrelation function and the frequency range. Moreover, the technique of [3] requires intensive computations and it has a long convergence time. Variance-based calibration method of [5] relaxes the requirement on input signal, but it needs a power-hungry flash ADC and its background convergence-speed is slow. Additionally, the techniques of [4] and [5] use every ADC output for the skew estimation so that the digital power is substantial. [6] presents a variance-based technique that obviates the need for a flash and accelerates the convergence, but it still relies on variance calculations, which require a power-consuming multiplier.

This paper presents a novel background timing-skew calibration technique based on mean absolute deviation (MAD). Unlike [4], the proposed MAD technique incorporates a comparator-based window detector (WD), which establishes improved trade-offs between the above-mentioned factors: first, the proposed technique does not rely on a tight requirement on the shape of the input signal's autocorrelation function and its constraint on the input is moderate. It only requires the input to have zero crossings and sufficient slope. This constraint is common to many calibration methods and easily satisfied by many applications; second, although this technique needs a reference channel, extra power and area cost is low. Furthermore, the WD runs at full ADC rate and thus, the ADC input impedance does not vary; third, its convergence speed is fast and each calibration cycle requires only 10^5 ADC samples even for random inputs; fourth, its computation is simple because only taking absolute value and averaging are needed. Compared to [6], it does not require any multiplication, which substantially reduces the digital power cost.

This paper is organized as follow. Section II presents the proposed MAD-based timing-skew calibration technique. Section III discusses measurement results and conclusion is brought up in section IV.

II. The Proposed MAD-based Timing-Skew Calibration Technique

Figure 1 shows the block diagram of the prototype TI-SAR. It is composed of 2 SAR channels, a WD, and a MAD estimator. Each SAR is consisted of 10-b with 1-b redundancy. It adopts the bidirectional single-side switching technique to reduce the total DAC array size by 4 times to 272C. The WD acts as a reference channel running at the full ADC rate (Φ_R). The MAD estimator extracts the timing skew of each SAR channel and adjusts the variable delay line (VDL) for skew corrections. The VDL has 6-b binary-weighted control code with a fine delay tuning of 300fs and a total correction range of 19ps.

Figure 2 shows the block diagram of the WD. It consists of a sampling network, a comparator, a tunable delay cell, and a DFF that acts as a 1-b TDC that compares the comparator

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decision time (CDT) with a reference delay τ_D. The WD is used to identify if a sampled input $V_{in,R}$ is within a small window W by exploiting CDTs dependence on the input amplitude. If $V_{in,R}$ is near the zero-crossing and falls within $[-W, +W]$, the CDT is longer and Φ_{XOR} arrives later than Φ_{delay}, leading to flag $f = 1$. By contrast, if $V_{in,R}$ is outside $\pm W$, Φ_{XOR} arrives earlier than Φ_{delay}, leading to $f = 0$. W is set to 1 LSB to identify samples very close to zero. To ensure $W = 1$ LSB across PVT variation, the value of W is monitored by checking and comparing the number of flags ($f = 1$) to the number of ADC outputs that are within ± 1 LSB. If these two numbers match, then $W = 1$. If not, τ_D is tuned in the background to enlarge or shrink W until they match. Fig. 2 also shows the schematic of a 3-stage comparator used in both WD and SAR. The first 2 dynamic pre-amplifier provides sufficient gain to reduce the input-referred noise and offset from the last-stage latch. It also greatly reduces the regeneration time constant by driving both latch inputs to VDD and removing the tail transistor, leading to a faster speed than the Strong-Arm latch.

Figure 3 illustrates the principle of the proposed MAD-based calibration technique using a single-tone sinusoidal input as an example. The basic estimation procedure is as follow: first, the WD checks if the sampled input is near the zero-crossing (dark shaded region) and raises the flag ($f = 1$). When the MAD estimation engine detect $f = 1$, it collects the output $D_{out,f=1}$ of the corresponding SAR that has converted the same input that the WD raised the flag. When there is no timing skew, the collected $D_{out,f=1}$ are near 0, where 0 is the middle code and D_{out} spans ± 512. The distribution of the collected $\{D_{out,f=1}\}$ and $\{|D_{out,f=1}|\}$ are shown on the right side of Fig. 3. The distribution is very narrow, leading to a small MAD value, $E(|D_{out,f=1}|)$. On the other hand, if timing skew exists, the SAR channel samples inputs before or after the zero crossing, which results in a wider spread of $\{D_{out,f=1}\}$ and $\{|D_{out,f=1}|\}$ distribution (see Fig. 3 left), leading to a larger MAD value.

The fundamental principle that MAD value is proportional to timing-skew τ can be proved with the equation given by

$$\begin{aligned} MAD(\tau) &\equiv E(|V_{in}(t+\tau)|_{f=1}|) \\ &= E(|V_{in}(t)|_{f=1} + \tau \cdot \frac{dV_{in}}{dt}|) \\ &\cong \frac{W}{2} erf(\frac{W}{\sqrt{2}\sigma_{dv}|\tau|}) + \frac{\sigma_{dv}^2\tau^2}{2W} erf(\frac{W}{\sqrt{2}\sigma_{dv}|\tau|}) \\ &\quad + \frac{\sigma_{dv}|\tau|}{\sqrt{2\pi}} \exp\frac{-W^2}{2\sigma_{dv}^2\tau^2} \end{aligned} \quad (1)$$

where σ_{dv} represents the standard deviation of dV_{in}/dt conditioning on $f = 1$. In deriving (1), $V_{in}(t)$ and dV_{in}/dt are treated as uncorrelated random variables due to their inherent orthogonality. Additionally, V_{in} is assumed to be uniformly distributed within the window $[W, +W]$, which is valid for small W. For small τ, the right-hand side of (1) is approximated as:

$$MAD(\tau) \cong \frac{1}{2}W + \frac{\sigma_{dv}^2\tau^2}{2W} \quad (2)$$

For large τ, the right-hand side of (1) is approximated as:

$$MAD(\tau) \cong \frac{\sigma_{dv}|\tau|}{\sqrt{2\pi}} \quad (3)$$

(2) and (3) illustrate that the MAD can serve as a timing-skew indicator and thus, the timing skew can be corrected in background by adjusting the VDL in the direction that minimizes the MAD value.

The proposed calibration technique has a fast convergence speed as the timing skew can be accurately estimated from MAD by using a small amount of ADC samples. The estimation accuracy depends on the value of W. At first glance,

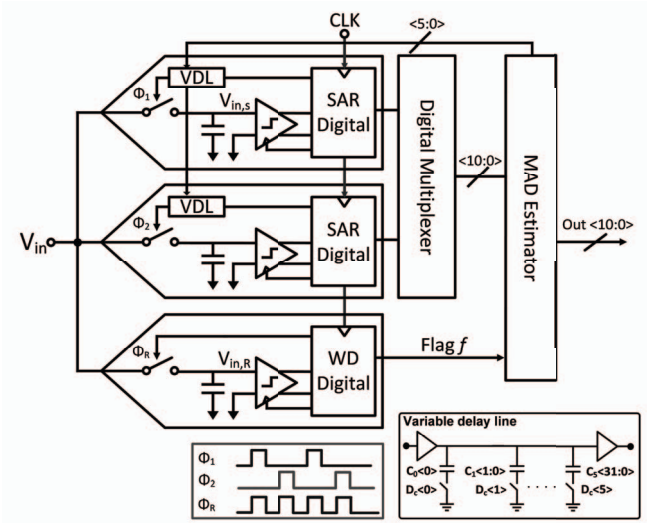

Fig. 1. Architecture and timing diagram of the proposed 2-way TI-SAR.

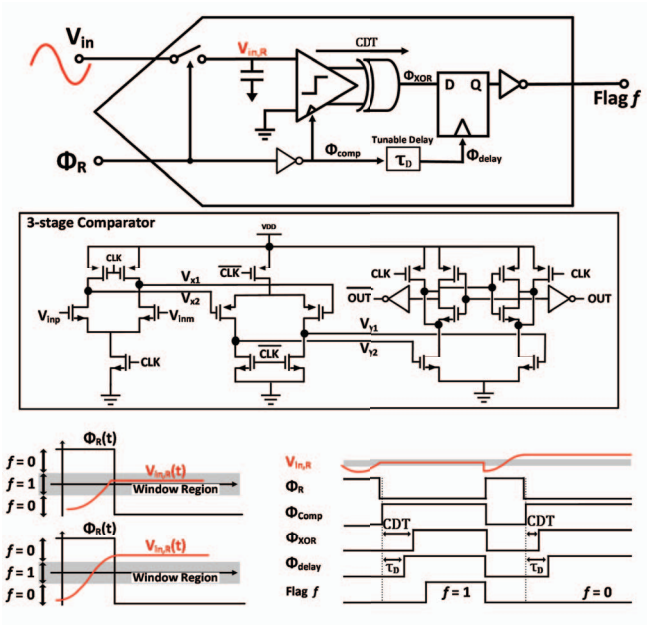

Fig. 2. Architecture and timing diagram of the proposed window detector.

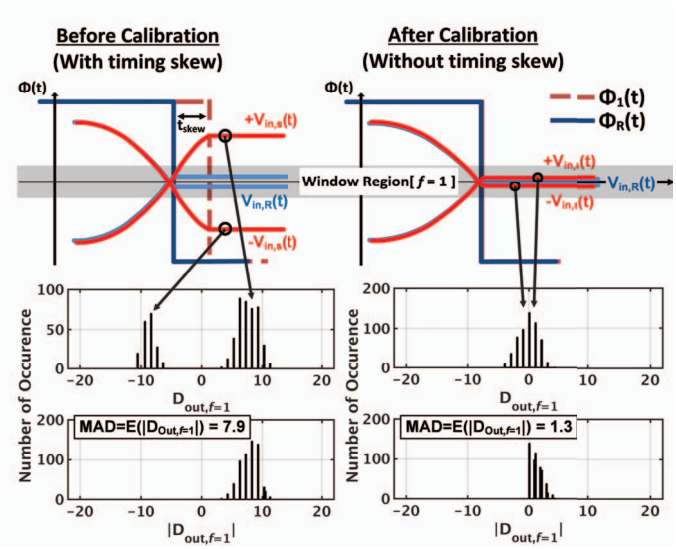

Fig. 3. Fundamental idea of the proposed timing-skew estimation technique.

a large W would allow more samples to be collected and averaged; however, it substantially increases the variation of the collected $\{D_{out,f=1}\}$, and the net effect is more fluctuation in the MAD estimation, leading to a slow convergence. On the other hand, W cannot be too small, as otherwise the comparator thermal noise and quantization error would corrupt the MAD estimation accuracy. The optimum value for W that balances the tradeoff is 1 LSB, leading to a fast convergence.

The power required for MAD calculation is very low due to the following reasons. First, the computation is simple. It only involves taking absolute value and averaging. Second, activity factor for the MAD calculation is low. The MAD computation is performed only for inputs falling inside the window. Since the probability is low due to a small window size, the MAD computation engine remains inactive for most of the time. For example, for a total of 10^5 ADC input samples, only several 100s are inside the window and are processed for MAD calculation. Third, because the collected $\{D_{out,f=1}\}$ samples are close to 0, the bit width required for the computation can be reduced to only the last 4 LSB, further reducing digital computation power.

The WD not only enables timing skew calibration, but also facilitates offset mismatch calibration. It can be proved that $E\left(D_{out,f=1}\right)$ is a low fluctuation estimator for the channel offset. The classic method for offset background calibration is to use $E\left(D_{out}\right)$ as an estimator for the offset; however, $E\left(D_{out}\right)$ fluctuates substantially with a random ADC input, resulting in a slow convergence. By contrast, using $E\left(D_{out,f=1}\right)$ significantly reduces the fluctuation in the offset estimation, as the large amplitude variation is eliminated (only samples inside the window are used to estimate the offset mismatch). This results in over 2 orders of magnitude faster convergence and significantly reduced computation power due to low activity factor. As in any background calibration technique, the proposed technique has restrictions on the input. It requires the input to have zero-crossing samples and have a sufficient slope. Even so, these requirements are satisfied easily in many practical applications. It works well for both narrow-band and wide-band signals.

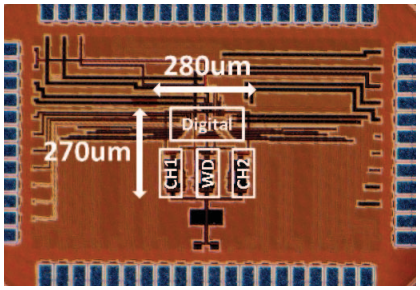

Fig. 4. Die photo.

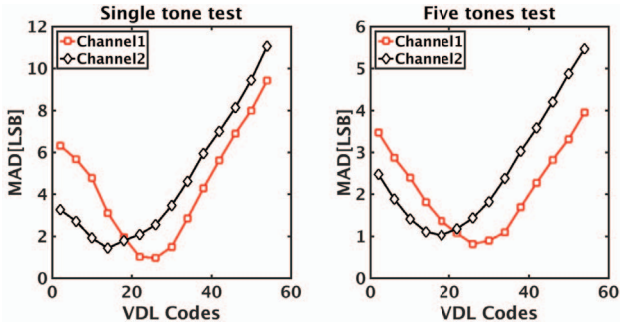

Fig. 5. Measured MAD of inputs falling in the window versus VDL control code with a single-tone input and five-tone input.

III. Measurement Result

A prototype 2-way TI ADC running at 600MS/s is built in 40nm CMOS and its die photo is shown in Fig. 4. Fig. 5 shows the measured MAD versus the VDL codes, confirming the quadratic and linear relationship between MAD and timing skew τ, derived in (2) and (3), with a single-tone f_{in} of 295-MHz and a five-tone f_{in} of 137, 177, 201, 214, and 251-MHz. The five-tone measurement result illustrates that the proposed method is capable to run in background. The MAD computation is realized off-chip. With the same test-bench, the digital synthesis of the proposed technique shows the average computation power of only $5\mu W$ that is 50% lower than that of [6]. The measured convergence curve is plotted in Fig. 6. Each calibration cycle takes 10^5 of ADC samples and the ADC reaches the peak SNDR within 30 calibration cycles or within 10ms. Fig. 7 shows the measured SNDR versus input frequencies before and after calibration. Before calibration, the SNDR is limited by timing-skew tones, which monotonically aggravates with the input frequency. After calibration, timing-skew tones are removed and the SNDR remains above 52dB, which is limited by the performance of the single-channel ADCs. Spectra with near-Nyquist frequency input before and after correction is illustrated in Fig. 8. The timing skew tone is reduced from -33 dB to -75 dB after calibration. The peak SNDR is 56 dB and is maintained above 52 dB across the entire Nyquist band. Fig. 9 shows the measured SNDR versus the input amplitude for three different frequencies. The total

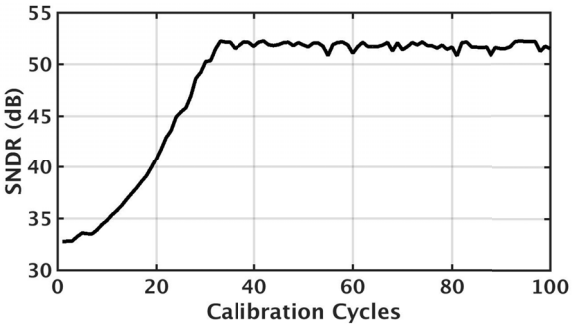

Fig. 6. Measured SNDR versus calibration cycles.

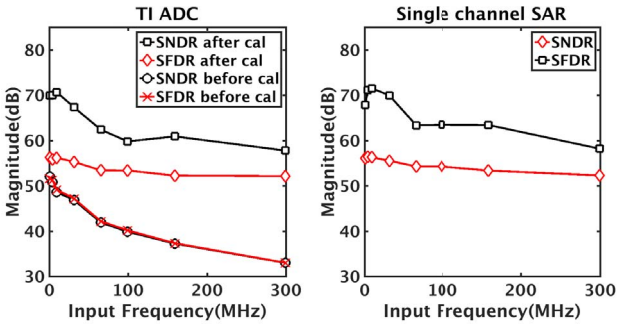

Fig. 7. Measured SNDR and SFDR versus the input frequency of TI ADC and a single channel.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	This work	[1]	[3]	[4]	[5]	[8]
Architecture	TI-SAR	TI-SAR	TI-SAR	TI-PIPELINE	FATI-SAR	TI-SAR
Calibration technique	MAD	Input slope estimation	Input slope estimation	Auto correlation	Variance	Auto correlation
Technology (nm)	40	65	40	65	65	40
Supply voltage (V)	1.2	1.2	1.1	1.2	1	1.1
Fs (GS/s)	0.6	2.8	1.62	4	1	2.6
# of sub channels	2	24	12	4	8	16
Sub channel fch (MS/s)	300	117	135	1000	125	163
Resolution (bit)	10	11	9	8	10	10
Power (mW)	4.7	44.6	283	120	18.9	18.4
SNDR @Nyquist (dB)	52.1	50	48	44.4	51.4	50.6
FoM (fJ/conv-step)	23.8	78	283	219	62.3	25.6
Active area (mm^2)	0.076	0.63	0.83	1.35	0.78	0.825

power is 4.7mW, leading to a Walden FoM of 23.8-fJ/step. Table I summarizes the performance of this work.

IV. Conclusion

This paper presents 2-way TI-SAR with a novel MAD-based background timing-skew calibration technique. The convergence speed is fast and the digital computation power is very low, since only few 100s of samples are used and taking absolute value and averaging are needed. prototype achieves a peak SNDR of 56dB and SNDR of 52dB at Nyquist. The

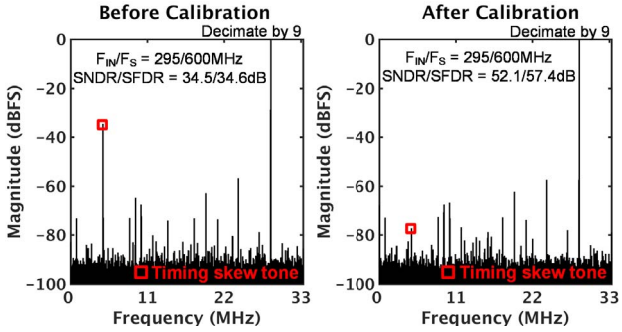

Fig. 8. Measured spectrum of TI-ADC (Left) before and (Right) after timing-skew calibration with the Nyquist input at 295 MHz.

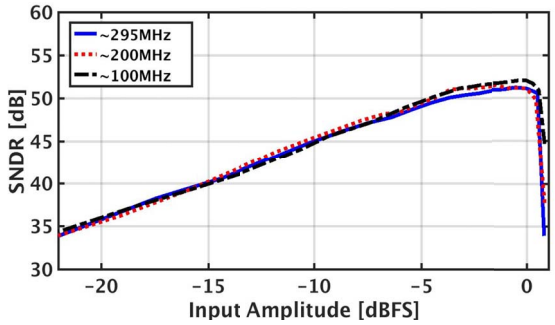

Fig. 9. Measured SNDR versus input amplitudes.

power consumption is 4.7mW and it leads to the Walden FoM of 23.8-fJ/conversion step.

V. Acknowledgement

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