A 10-mW 10-ENoB 1-GS/s Ring-Amp-Based Pipelined TI-SAR ADC With Split MDAC and Switched Reference Decoupling Capacitor

Mingtao Zhan, *Graduate Student Member, IEEE*, Lu Jie, *Member, IEEE*, Yi Zhong, *Member, IEEE*, and Nan Sun, *Senior Member, IEEE*

***Abstract*— This article presents a 12-bit 1-GS/s ring-amp-based analog-to-digital converter (ADC) with a pipelined and time-interleaved successive approximation register (TI-SAR) hybrid architecture. This architecture utilizes backend time-interleaving for power and design complexity reduction while eliminating the sampling time skew. A ring amplifier (ring-amp) is used in this architecture to significantly reduce the power of residue amplification by about ten times over a prior work. A high-speed PVT-robust ring-amp with split input by splitting the multiplying DAC (MDAC) is proposed to guarantee the performance of the ring-amp under low supply voltage. To improve the power supply rejection ratio (PSRR) of the reference buffer and lower the reference noise without degrading the reference settling speed, a switched reference decoupling capacitor (de-cap) technique is proposed. Flash ADC and backend successive approximation register (SAR) ADCs are also optimized to meet the challenging power efficiency requirement. The ADC implemented in a 28-nm CMOS process achieves 62.5-dB SNDR for Nyquist input. The total power including the reference buffer is 10.6 mW, yielding a Schreier figure of merit (FoM$_S$) of 169.2 dB.**

***Index Terms*— Analog-to-digital converter (ADC), pipeline, ring amplifier (ring-amp), successive approximation register (SAR), time interleaving.**

I. Introduction

ADVANCEMENTS in wireless standards are leading to wider channel bandwidth and higher order modulation for higher data rates. For example, the forthcoming WiFi-7 (802.11be) is expected to support a maximum bandwidth of up to 320 MHz and modulation of up to 4096-QAM. This necessitates analog-to-digital converters (ADCs) with gigahertz sampling rate and 12b resolution. Compared to ADCs for WiFi-5 (802.11ac) [1], the sampling rate is quadrupled and the resolution is increased by 2b, resulting in at least 16 times more ADC power. Therefore, there is an urgent need to improve the energy efficiency of GS/s ADCs.

Pipelined successive approximation register (SAR) ADC is an efficient solution for ADCs with hundreds of MS/s sampling rates by using efficient SAR quantizers and reducing the required number of stages of a conventional pipelined ADC [2], [3], [4]. Nonetheless, for GS/s ADCs, the long SAR conversion time (more than 100 ps/cycle in 28 nm) limits the sampling rate, reduces the available amplification time, and results in increased residue amplifier (RA) power. Conventional "deep" pipeline ADCs can maximize the amplification time using a flash sub-ADC. However, it is difficult to increase the resolution of a flash sub-ADC to more than 4b for area and power considerations. Therefore, at least four pipelined stages are required for 12b resolution. The high-speed nonoverlapping clock distribution for many pipelined stages is complex and power-hungry. In [5], the clock tree consumes about half of the total ADC power. In [6], the control unit and line driver for asynchronous clocking consume 24% of the power, leading to reduced power efficiency.

Another low-power solution for GS/s ADCs is directly interleaving low-speed energy-efficient SAR or pipelined SAR sub-ADCs. However, this approach comes with significant overhead from background timing-skew calibrations. It also imposes limitations on the input signal. Many timing-skew calibration techniques cannot converge with a dc input, restricting their usage [7], [8], [9], [10], [11]. Additionally, the ADC area increases by the interleaving factor. Therefore, a single-channel ADC remains the preferred option for high-resolution wireless applications.

To address the above problems, the pipelined and time-interleaved SAR (TI-SAR) hybrid architecture has been proposed in [12]. It places a TI-SAR at the second pipeline stage as the backend ADC, as shown in Fig. 1(a). Because the frontend multiplying DAC (MDAC) samples the input signal, there is no timing-skew issue for the backend TI-SAR as the RA fully settles. Due to the asynchronous operation of SAR ADCs, only a set of interleaved sampling clocks with a relaxed skew requirement is needed for the backend ADC control, simplifying the clock distribution and reducing the backend power overhead. As a result, only about 10% of the total power is consumed on clocking in this work even including the input clock buffer. Also, compared to a dedicated sample-and-hold

Manuscript received 11 May 2023; revised 4 July 2023; accepted 11 August 2023. Date of publication 4 September 2023; date of current version 28 November 2023. This article was approved by Associate Editor Dominique Morche. This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFB2205003, in part by the Beijing National Research Center for Information Science and Technology, in part by the Beijing Innovation Center for Future Chip, in part by the Academician Expert Open Fund of Beijing Smart-chip Microelectronics Technology Company Ltd., and in part by the NSFC under Grant 62090042 and Grant 61934009. *(Corresponding authors: Nan Sun; Lu Jie.)*

Mingtao Zhan, Yi Zhong, and Nan Sun are with the Department of Electronic Engineering, Tsinghua University, Beijing 100084, China (e-mail: nansun@tsinghua.edu.cn).

Lu Jie is with the School of Integrated Circuits, Tsinghua University, Beijing 100084, China (e-mail: jielu@tsinghua.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3307435.

Digital Object Identifier 10.1109/JSSC.2023.3307435

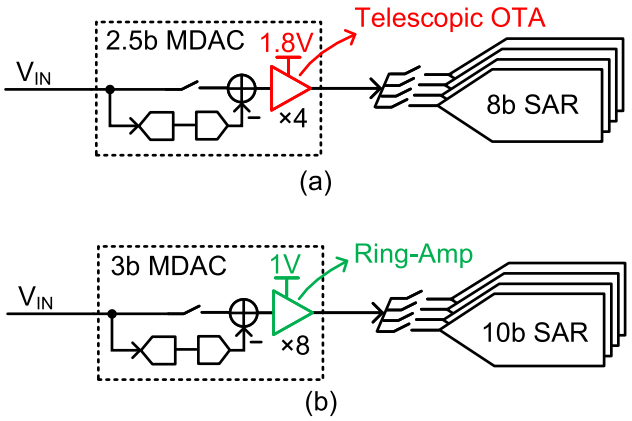


Fig. 1. Pipelined/TI-SAR hybrid architecture (a) in [12] and (b) in this work.

stage, the gain of the MDAC alleviates the noise requirement of the backend SAR, resulting in a small area.

Despite the architectural advantages, the power efficiency of [12] is shaded by its power-hungry telescopic operational transconductance amplifier (OTA) with a high supply voltage. The interleaved 2.5-GS/s ping-pong MDACs achieve a 56.5-dB SNR and consume 55 mW in [12], leading to a low overall Schreier figure of merit (FoM_S) of 154.2 dB. In this work, a ring amplifier (ring-amp) is used as the RA to reduce power. However, most prior ring-amps are either sensitive to PVT variations [2], [4], [5], [13], [14], [15], [16] or have limited speed [3], [17], [18], [19]. To improve the speed and PVT robustness of the proposed ring-amp, the split MDAC technique is used in this work. The proposed ring-amp-based MDAC achieves a 62.5-dB SNDR and only consumes 2.7 mW. This enables a 1-GS/s 10-ENoB ADC with only 6.9 mW power excluding the reference buffer, yielding a state-of-the-art FoM_S of 171.1 dB.

In addition to the RA design, the power and area overhead of the reference buffer are other critical issues for high-speed pipelined ADCs. The reference buffer should provide a charge for the MDAC within a short period while rejecting interference from the power supply. However, a fast response can contradict the power supply rejection ratio (PSRR). A reference decoupling capacitor (de-cap) can increase the PSRR, but it slows down the reference settling. To break the tradeoff between reference settling speed and high-frequency PSRR, this work proposes a reference de-cap switching technique. The proposed reference buffer power is only 3.7 mW. The total de-cap size is only 44 pF, which is about ten times smaller than in [16]. The total ADC power including the reference buffer is 10.6 mW, yielding a competitive overall FoM_S of 169.2 dB.

This article is an extension of [20]. It is organized as follows. Section II describes the proposed high-speed current-biased ring-amp design with split MDAC. Section III describes the proposed switched reference de-cap technique. Section IV describes the implementation details of the prototype hybrid ADC, and the measurement results are reported in Section V. Section VI concludes this article.

II. High-Speed Current-Biased Ring-Amp Design

The performance of the RA is the bottleneck of pipelined ADCs. Recently, both open-loop Gm-R amplifiers [21], [22]

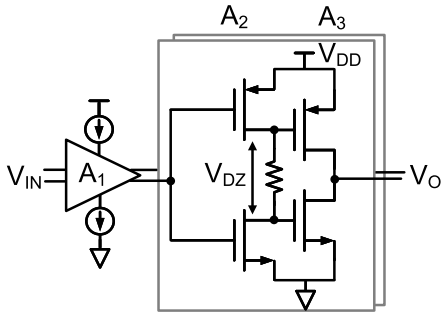


Fig. 2. Commonly used ring-amp structure in previous works.

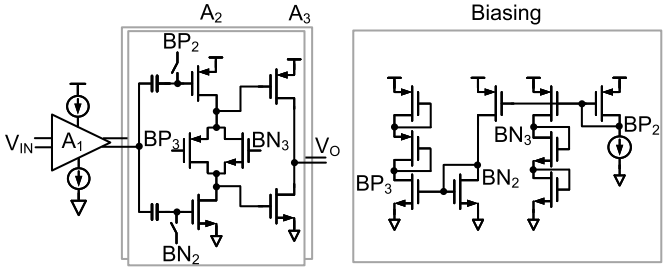


Fig. 3. Ring-amp with current biasing proposed in [3].

and closed-loop ring-amps [2], [3], [4], [5], [13], [14], [15], [16], [17], [18] have been developed to significantly improve the efficiency of the RA. However, the gain of an open-loop amplifier is sensitive to PVT variations. Moreover, its gain is nonlinear, requiring nonlinearity calibration, which is more complicated than a first-order gain error calibration [22], [23]. To obviate the need for nonlinearity calibration, a minimum resolution of 4b is needed in the first pipeline stage for a smaller residue voltage for 12b resolution [21]. However, this significantly increases the power consumption of a flash quantizer or elongates the decision time of an SAR quantizer. By comparison, ring-amp exhibits inherent high linearity due to its closed-loop operation. Using ring-amps, pipelines with 1.5-b/stage for 12b resolution without nonlinearity calibration have been reported [5], [14], [15].

Most of the recent ring-amp designs have severe PVT robustness problems and require bias tuning, with the ring-amp structure shown in Fig. 2 [2], [5], [14], [15], [17], [18]. This is because the operating points of A_2 and A_3 depend strongly on V_T and supply voltage, and thus are highly sensitive to PVT. Therefore, the loop unit-gain bandwidth (UGB) and phase margin change greatly. This results in either over-damped or unstable response over corners if without any bias tuning.

A recent work of [3] inserts split capacitors in front of A_2 to bias the PMOS and NMOS inputs of A_2 separately, as shown in Fig. 3. This makes the current of A_2 well-defined with current mirrors. With a stable A_2 current, class-AB biasing can be utilized to bias A_3, and good PVT robustness is achieved. However, the sampling rate of [3] is only 200 MS/s, and the time for residue amplification is about 1.25 ns, which is about four times longer than in this work. For higher-speed operation, the speed of A_1 and A_2 should be higher to push up the nondominant poles with larger overdrive voltage (V_{ov}). The problem of [3] is that A_1 with complementary input [as shown

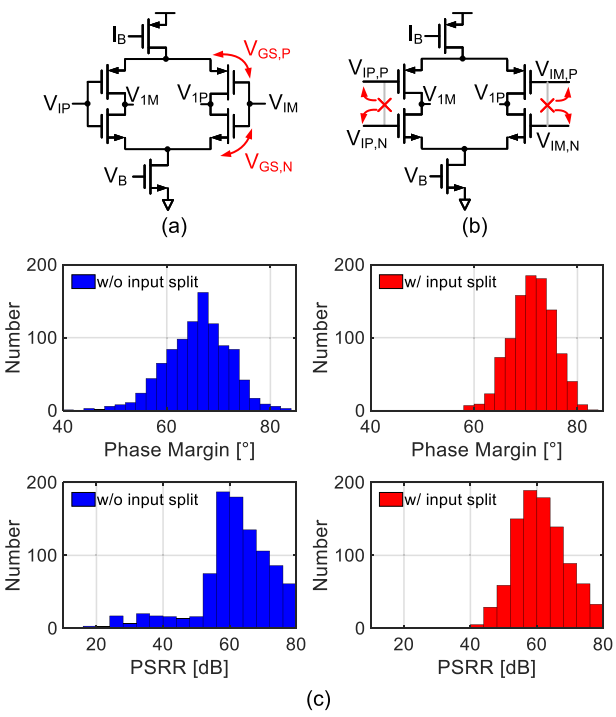


Fig. 4. (a) Implementation of ring-amp A_1 in the previous work. (b) Proposed A_1 with a split input. (c) Phase margin and PSRR comparison by Monte Carlo simulation (2000 runs).

in Fig. 4(a)] limits the voltage supply range, requiring $2V_T + 4V_{ov}$. Under low supply and slow corners, the tail transistor may work in the linear region. As a result, A_1 current can vary over two times across process and temperature corners. The reduced A_1 current degrades its speed and results in an insufficient phase margin of the ring-amp. The tail transistor working in the linear region also reduces the PSRR. These are shown in the Monte Carlo simulation results in Fig. 4(c), left. Notably, this problem exists in all previous ring-amp designs and is not limited to the structure in [3].

A. Proposed PVT-Robust Ring-Amp With Split MDAC

To solve the voltage headroom issue and retain the current reuse property in the first stage, the input dc of A_1 is split, as shown in Fig. 4(b). Thus, higher overdrive voltages for complementary input pairs are possible even in the slow corner with a low supply voltage and low temperature. This pushes up the nondominant pole frequency and increases the settling speed. As shown in Fig. 4(c), right, the variation of the ring-amp phase margin and PSRR significantly reduces with a split input.

A level-shifting capacitor (C_{LS}) can be used to split the dc biases [24], [25]. However, the cost is the extra kT/C noise and area of C_{LS}. The feedback factor is also reduced by the inevitable parasitics of C_{LS}. A split-capacitor biasing technique is proposed in [26] to bias a single-stage class-AB amplifier by splitting the 1.5b MDAC capacitors into two parts, avoiding the drawbacks of using C_{LS}. In this work, we apply the split-capacitor technique for multibit MDAC. The first-stage capacitor digital-to-analog converter (CDAC) is split into bias the input PMOS and NMOS pairs of A_1 with different dc voltages BP_1 and BN_1, as shown in Fig. 5(a).

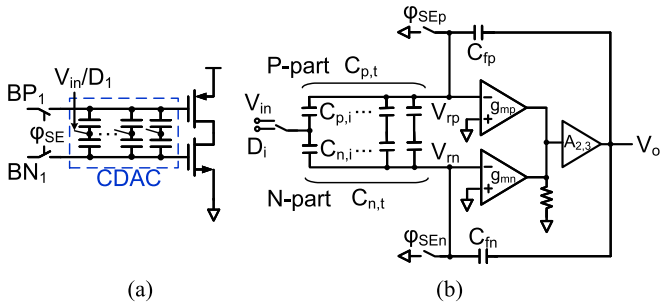


Fig. 5. (a) Half circuit of A_1 with the split MDAC. (b) Circuit model of split MDAC using a ring-amp.

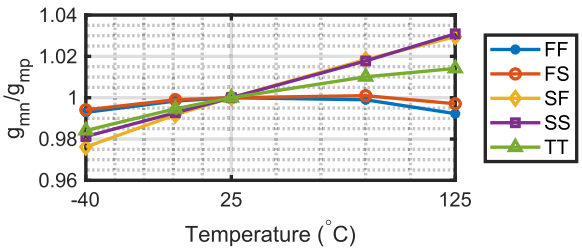


Fig. 6. Simulated input pair g_{mn} and g_{mp} ratio with temperature variation (normalized to room temperature).

Compared to using C_{LS} for the split input, there are two digital-to-analog converter (DAC) parts (P-part and N-part) for split MDAC as shown in Fig. 5(b). This introduces the following design considerations.

1) Sampling Bandwidth and Timing Mismatch: For split MDAC, the virtual ground node is split into V_{rp} and V_{rn}. As a result, there are two signal sampling paths. The differences between the virtual ground sampling switch resistances and the sampling instants between the P and N parts cause a voltage difference ΔV between the sampled voltages of the two parts. If the MDAC output is a linear combination of the signal of each part, a nonzero ΔV does not cause nonlinearity. However, the existence of ΔV causes the virtual ground of each part to depart from 0 to about $\pm\Delta V/2$, even if the amplifier dc gain is infinite. This is because A_2 and A_3 of the ring-amp force the output of A_1 to zero. As a result, a large ΔV can make g_{mp} and g_{mn} nonlinear. This work uses bootstrapped virtual ground switches with a small resistance, driven by a sharpened sampling clock falling edge. This reduces ΔV to be within 2 mV, thus ΔV does not degrade the linearity of the ADC.

2) DAC Weight Mismatch Caused by Capacitor Mismatch and g_m Variation: One-time foreground calibration is used to address capacitor mismatch in the MDAC. However, for the split MDAC, the effective capacitor weight is the average of the P and N part DAC weights. The average is performed by g_{mp} and g_{mn}. With mismatches between the P and N part DAC weights, if the ratio between g_{mp} and g_{mn} changes greatly, the effective DAC weights would change over temperature. Although interstage gain error caused by the variation can be addressed by background calibration, this can make one-time CDAC mismatch calibration invalid. Quantitative analysis is shown in the Appendix. For this design, the input pair g_m ratio variation is less than 5% over temperature, as the simulation result shown in Fig. 6. For 12b level matching, we need the

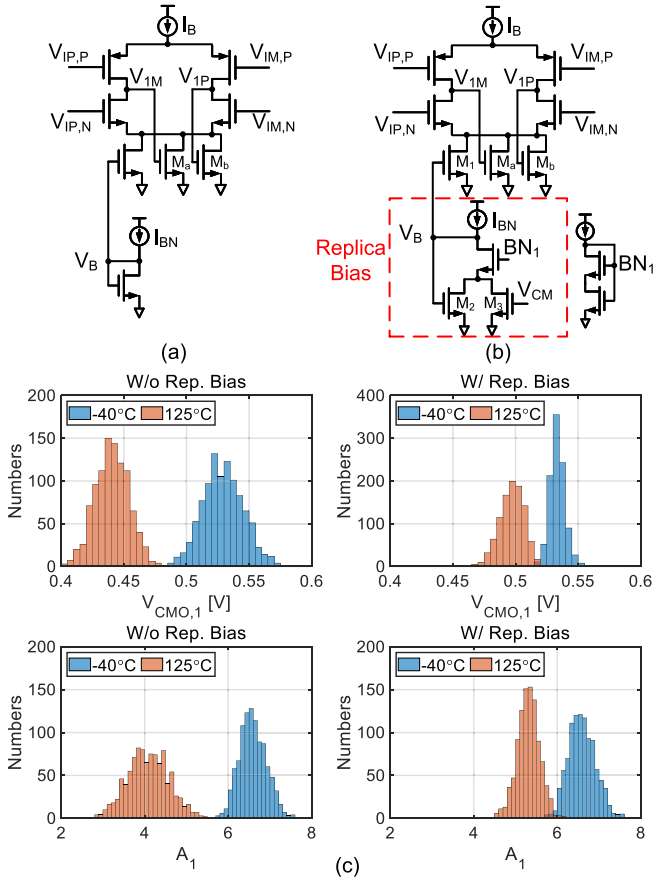


Fig. 7. (a) A_1 CMFB in prior works. (b) Proposed A_1 CMFB using replica bias. (c) Monte Carlo simulation results of A_1 output CM and gain at −40 and 125 °C with and without replica bias.

MSB weight variation $|\Delta W_i|$ less than 0.1%. According to the Appendix, this requires the matching of the MSB unit-caps in the P and N parts to be better than 4%, which is feasible with a careful layout with 20 fF unit-caps. Therefore, there is no concern about the mismatch problem in this work.

B. Proposed Robust CMFB Design

A_1 output common mode (CM) in previous works [3], [15] can vary over 200 mV across corners with the changing NMOS threshold voltage. This is because they directly connect A_1 output to its tails (M_a and M_b) for a fast local CM feedback (CMFB) loop, as shown in Fig. 7(a). As the currents flow through M_a and M_b are fixed, A_1 output CM (defined by V_{GS}) changes over process and temperature. As the low output CM pushes the input NMOS pair near the linear region, A_1 gain is affected, especially in a fast-NMOS and high-temperature corner. A switched-capacitor CMFB can be used to solve the problem, but it has extra loading on A_1.

To resolve the A_1 output CM variation issue, a replica bias scheme is used in this work. This maintains a fast local CMFB while keeping the output CM stable over process and temperature. This is done by generating the dc bias of M_1 (V_B) using a replica bias structure shown in Fig. 7(b). V_{CM} is a reference CM voltage about $V_{DD}/2$. As the gate of M_3 is connected to V_{CM}, its current is changing with V_T. As a result,

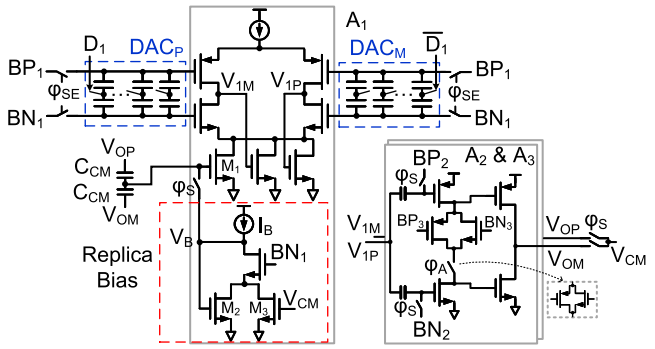


Fig. 8. Ring-amp design in this work.

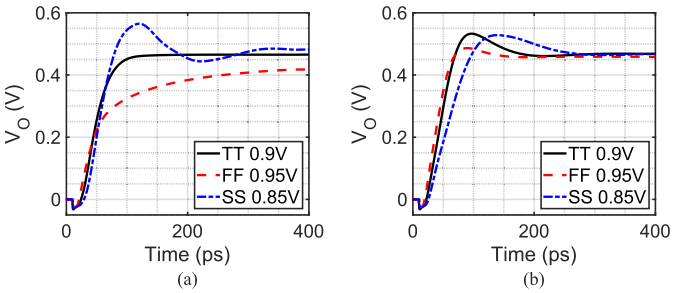


Fig. 9. Closed-loop response of the (a) previous ring-amp shown in Fig. 2 and (b) proposed ring-amp.

the currents of M_2 and M_1 are adjusted to make A_1 output CM near V_{CM}. As shown in Fig. 7(c), with the replica bias, the A_1 output CM and gain are more stable compared to prior works without a replica bias.

C. Proposed Complete Ring-Amp Schematic

The overall design of the ring-amp in this work is shown in Fig. 8. The global CMFB loop is realized as follows. During the sampling phase ϕ_S, the CM reference V_{CM} and dc bias V_B of M_1 are sampled on capacitors C_{CM}. During the amplification phase ϕ_A, the global output CM is fed back to M_1 through C_{CM}. Care should be taken when sizing M_3 to avoid it taking all of the I_B and cutting off M_2 and M_1, which cuts off the global CMFB loop.

The simulated ring-amp closed-loop response is shown in Fig. 9(b). This design is significantly more robust than previous high-speed designs [14], [15] [Fig. 9(a)]. No bias tuning is required for the ring-amp over PVT. Only background calibration of interstage gain to compensate for insufficient open-loop gain (nominal 50 dB) is required.

III. Switched Reference De-Cap

Reference buffer design is a challenge for high-speed pipelined ADCs. It typically consumes a large portion of the total power and area, especially after the RA power and area are greatly reduced by the ring-amp. In each conversion cycle, V_{REF} provides signal-dependent charges (Q_e) for the MDAC. The error voltage V_e of V_{REF} (compared to its static value) after time t can be expressed as

$$V_e(t) = \frac{Q_e}{C_{DAC} + C_{DEC}} e^{-\frac{t}{r_o(C_{DAC}+C_{DEC})}} \quad (1)$$

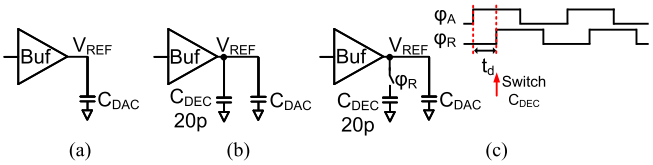


Fig. 10. Reference for MDAC (a) without a de-cap, (b) with a de-cap, and (c) with a switched de-cap.

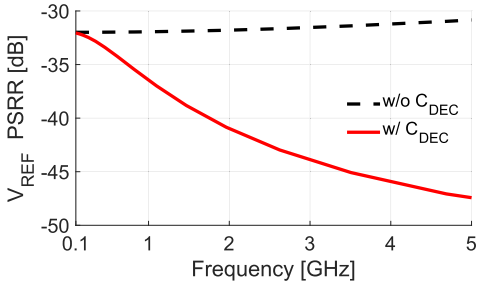


Fig. 11. Reference PSRR with and without a 20-pF de-cap.

where r_o is the output impedance of the reference buffer and C_{DEC} is the de-cap on V_{REF}. V_e should be within 1 LSB before the RA final settling without degrading the ADC performance. This can be done in two directions as follows.

1) Making C_{DEC} large enough to minimize the first term in (1). This can keep V_e induced by Q_e negligible. However, for C_{DAC} with hundreds of fF capacitance and 12b resolution, C_{DEC} has to be on the order of nF. Then C_{DEC} occupies a very large area (on the order of 0.2 mm^2, which is about ten times larger than the core area of this work). This is undesired in this design. Recently, a fully dynamic reference regulator has been proposed in [16]. A dirty and clean reference scheme effectively reduces Q_e for its clean reference and relaxes the requirement for C_{DEC} (reservoir capacitors in [16]). However, C_{DEC} on the order of hundreds of pF is still needed.
2) Not using any C_{DEC} to minimize the exponential term in (1). This can help V_e settle fast to zero [Fig. 10(a)]. However, there is a practical concern about the reference supply noise. A low-dropout regulator (LDO) can regulate the reference buffer power supply and provide low impedance within its bandwidth, which is typically less than several MHz. Therefore, the high-frequency PSRR of the reference buffer is more important. The PSRR of a source follower used as the reference buffer is limited to only 30 dB.

De-caps can improve the high-frequency PSRR. A 20-pF de-cap (C_{DEC}) added at the buffer output [as in Fig. 10(b)] can enhance the PSRR by 10 dB at 3 GHz, as shown in Fig. 11. However, a de-cap increases the reference buffer settling time constant and exponentially slows down the recovery of V_{REF}. The resulting code-dependent V_{REF} can severely degrade the ADC linearity.

To resolve this problem, we propose to switch C_{DEC}. A switch controlled by ϕ_R is connected between 20 pF C_{DEC} and V_{REF}, as shown in Fig. 10(c). During a short period t_d after the amplification starts, the switch is open. This substantially reduces the reference buffer settling time constant. Most of Q_e are drawn from V_{REF} during the ring-amp slewing phase [16]. They are provided by the buffer in a short time. After the amplifier slewing is done and the reference settles near the desired value, the switch is closed and connects C_{DEC} to V_{REF}. Here, t_d is about several times the reference buffer settling time constant. After a short time of charge sharing (limited by the resistance of the switch), C_{DEC} absorbs the remaining error charges and further reduces the voltage error on V_{REF} by 20 times. It stabilizes V_{REF} for accurate ring-amp settling and rejects the power supply interference. The few lost charges of C_{DEC} are replenished by the reference buffer during this period.

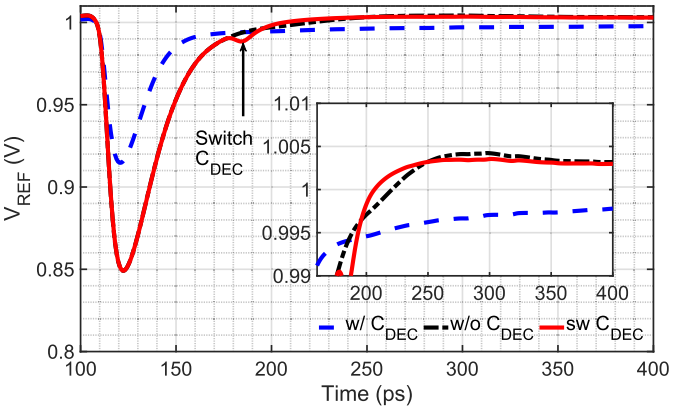


Fig. 12. Reference waveform with a de-cap, without a de-cap, and with a switched reference de-cap.

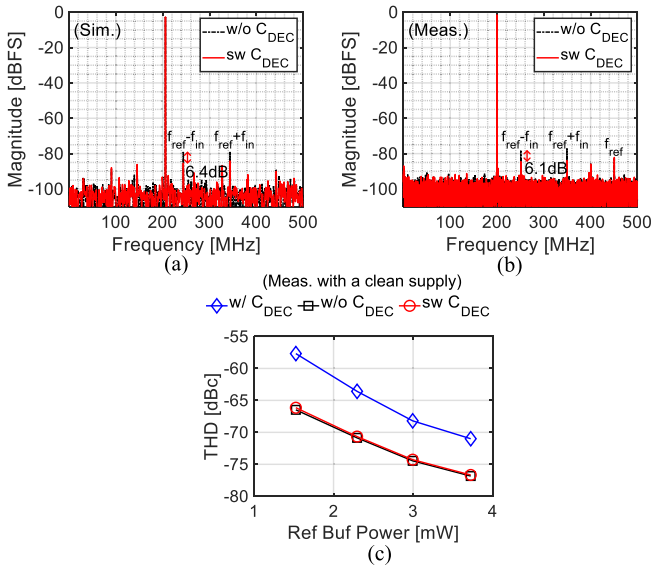


Fig. 13. (a) Simulated and (b) measured ADC output spectra with a 450-MHz interference on reference buffer power supply and (c) comparison of measured THD versus reference buffer power with different C_{DEC} configurations.

The simulated V_{REF} transient waveform is shown in Fig. 12. With switched C_{DEC}, the initial drop of V_{REF} is large, but its settling is very fast. This is the same as the case without C_{DEC}. After t_d, C_{DEC} is connected back to protect V_{REF} during the ring-amp's final settling period. With switched C_{DEC},

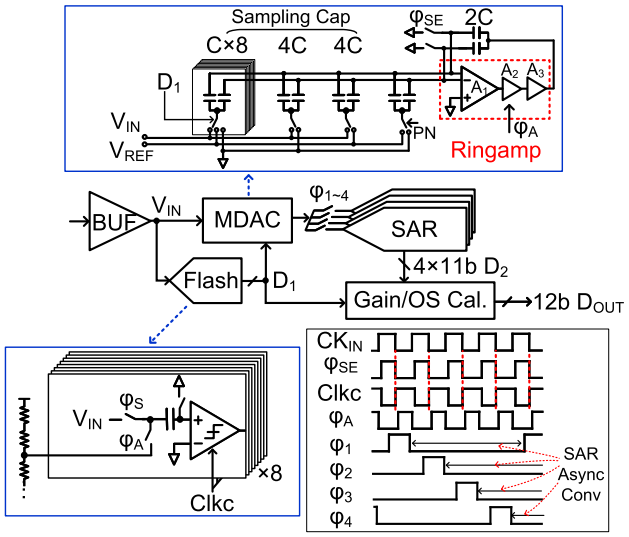


Fig. 14. Block diagram and timing diagram of the proposed ADC.

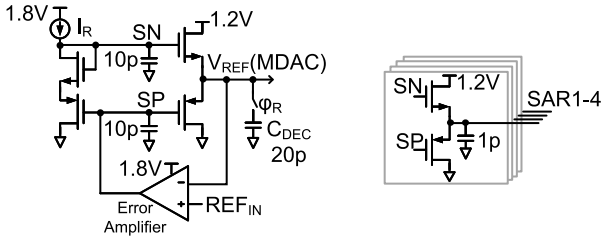
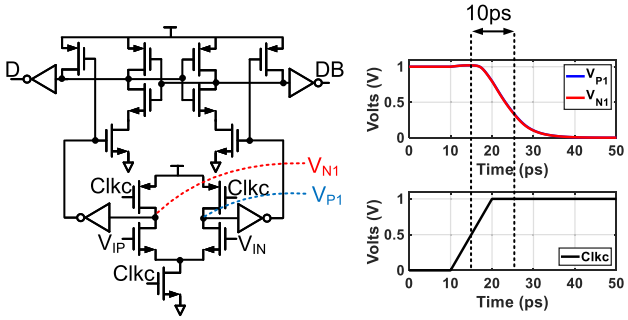


Fig. 15. Reference generation in this work.



(a) (b)

Fig. 16. (a) Three-stage dynamic comparator for flash ADC. (b) Simulated comparator preamp output waveform.

we can improve the reference PSRR at high frequency. This is shown in Fig. 11 by ac simulation and in Fig. 13(a) by transient simulation of the ADC with an intentionally added high-frequency supply interference (450 MHz and 25 mVpp). The measured spectra without C_{DEC} and with switched C_{DEC} with a 450-MHz reference supply interference are shown in Fig. 13(b). With switched C_{DEC}, the mixing spurs due to reference interference are suppressed by about 6 dB. The reference buffer settling speed is not degraded compared to directly adding C_{DEC}. Therefore, with the same reference buffer power, the THD is not degraded [Fig. 13(c)].

IV. ADC Implementation

A. Schematic Overview

Fig. 14 shows the block and timing diagram of the proposed ADC. As the single-ended input full-swing requirement for the system is 0.5 Vpp, we use half of the sampling capacitors connecting to the reference, controlled by the 3b flash decision. As a result, a 1-V reference voltage can be used for lower PMOS switch resistance, compared to a 0.5-V reference. The single-side sampling capacitance is 640 fF for kT/C noise requirement and the unit-cap in each of the split DAC is 20 fF. Taking advantage of the large output swing of the ring-amp, the interstage gain for the input signal path is set to 8 to suppress the backend noise, relaxing the backend SAR comparator design. The 1-V reference voltage is applied to the backend 10b SAR ADCs. The scaled reference for the MDAC creates about 1b interstage redundancy. Dither is injected for interstage gain error calibration.

Push–pull source followers are used as reference buffers. They are separated for the MDAC and each second-stage SAR to minimize crosstalk, as shown in Fig. 15 [27]. The bias voltages SP and SN are generated by a slow analog loop supplied by 1.8 V and are decoupled with 10-pF capacitors. 1-pF de-caps are added to each of the buffers for backend SARs to reduce the disturbance of SN and SP. The reference voltage mismatches among buffers are equivalent to interstage gain errors and are calibrated.

Resetting the sampling capacitor of the backend SAR before amplification can speed up the RA settling. This is done by connecting the next SAR to the MDAC output shortly after the previous amplification.

B. Flash ADC With Dynamic Comparators

To maximize the effective amplification time for the ring-amp, the decision of the flash ADC should be as fast as possible. This is done by sampling the flash reference voltages during the residue amplification phase and firing the comparators near the falling edge of the sampling clock [28]. This also prolongs the flash reference settling time and reduces the static reference power consumed by the resistor ladder to 100 uW.

To save the flash ADC power, a 3-stage dynamic comparator, the same as the design in [29], is selected [Fig. 16(a)]. It has a much smaller signal-dependent kickback with the 2-stage amplification before the latch, compared to a StrongArm latch. Moreover, the dynamic preamp's short integration time minimizes the sampling aperture, which is essential for an SHA-less architecture. Postlayout simulation shows that the sampling aperture can be as narrow as 10 ps with a careful layout to reduce the parasitic on the preamp integration nodes V_{P1} and V_{N1}, as shown in Fig. 16(b). Thus, MDAC skew calibration is not needed up to Nyquist frequency (500 MHz) with careful design and layout of the signal and clock paths. The comparator offsets are calibrated by observing the maximum and minimum of the backend ADC output codes as in [30].

C. Backend SAR ADC

Top-plate sampling with bidirectional switching with the last DAC cell switched to V_{CM} is applied [31]. Therefore, only 256-unit capacitors are needed for 10b resolution, greatly

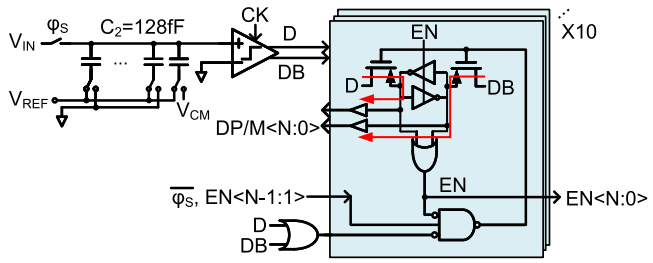


Fig. 17. Backend SAR ADC implementation.

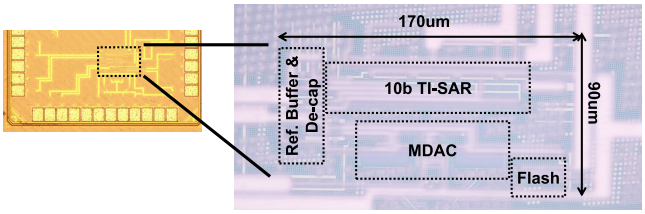


Fig. 18. Die photograph.

reducing the area. The systematic gain error caused by the top-plate parasitics is corrected by the interstage gain calibration. Latch-based asynchronous SAR logic similar to [32] is used for the backend SAR, as shown in Fig. 17. This reduces 50% of the digital power by eliminating a sequencer which consists of 11 flip-flops driven by a high-speed asynchronous comparator clock in [33]. Moreover, it minimizes the delay from the SAR comparator output to the buffers of the CDAC switches to only 1 PMOS transmission gate delay. This offers a longer time for DAC settling and relaxes the requirement for reference settling.

V. Measurement Results

The prototype ADC is fabricated in a 28-nm process. Fig. 18 shows the micrograph of the ADC core, which occupies an area of 0.016 mm^2. The offset mismatches among backend SARs can cause a fixed spur at $f_s/4$. They are calibrated in the digital domain by comparing the long-term averages of 4-channel SAR outputs. The gain errors among backend SARs are calibrated by applying different interstage gain parameters. Capacitor weights of the MDAC are foreground calibrated once and fixed in the measurement.

The ADC core consumes 6.9 mW from a 1-V supply when running at 1 GS/s (2.7 mW for the ring-amp, 1.3 mW for the flash and SAR comparators, 1.9 mW for digital, and 1 mW for clock generation and the input clock buffer). The reference buffer consumes 3.7 mW from a 1.2-V supply.

Fig. 19 shows the measured output spectra with 20- and 500-MHz 1-Vpp-diff inputs. The measured SNDR is 62.5 dB at Nyquist. The FoM$_S$ is 171.1 dB and the FoM$_W$ is 6.3 fJ/conv-step excluding the reference buffer power. The FoM$_S$ is 169.2 dB and the FoM$_W$ is 9.7 fJ/conv-step including the reference buffer power.

The input frequency sweep result is shown in Fig. 20. Above 62-dB SNDR can be achieved over the first Nyquist zone. The SFDR peak near the Nyquist input frequency is found

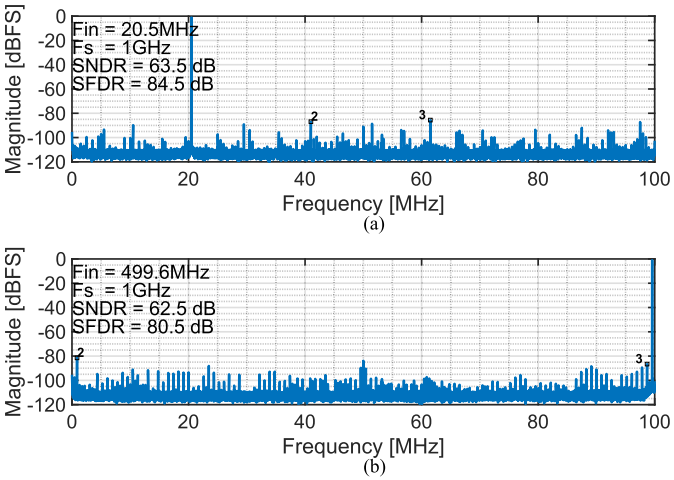


Fig. 19. Measured ADC output spectra with (a) 20-MHz and (b) 500-MHz 1-Vpp-inputs (131 072 points and decimated by 5).

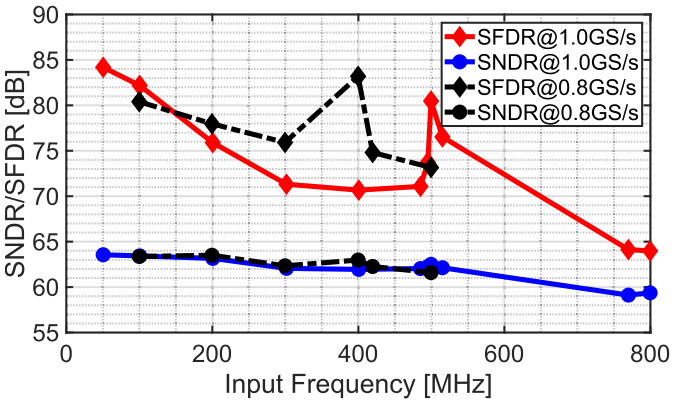


Fig. 20. Measured ADC performance with input frequency sweep.

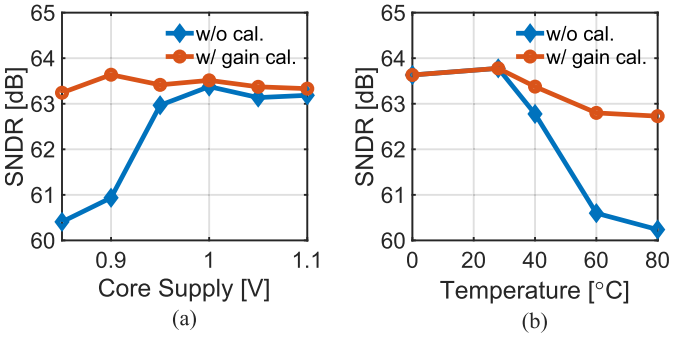


Fig. 21. Measured ADC performance with (a) core supply and (b) temperature sweep.

to be nonlinearity cancellation between the reference voltage and the input buffer. Because the reference bias generation in Fig. 15 directly sends V_{REF} to the error amplifier, the long-term settled reference voltage is larger for a dc input with more charges drawn. For an input near Nyquist, the pattern of charges drawn from the reference is similar to a dc input. As the MDAC draws more charges with a larger input and draws minimum charges with a zero input, this creates an expansion nonlinearity, canceling the input path compression nonlinearity. Using a separate reference buffer cell to generate SP and SN in Fig. 15 as in [27] can avoid this problem.

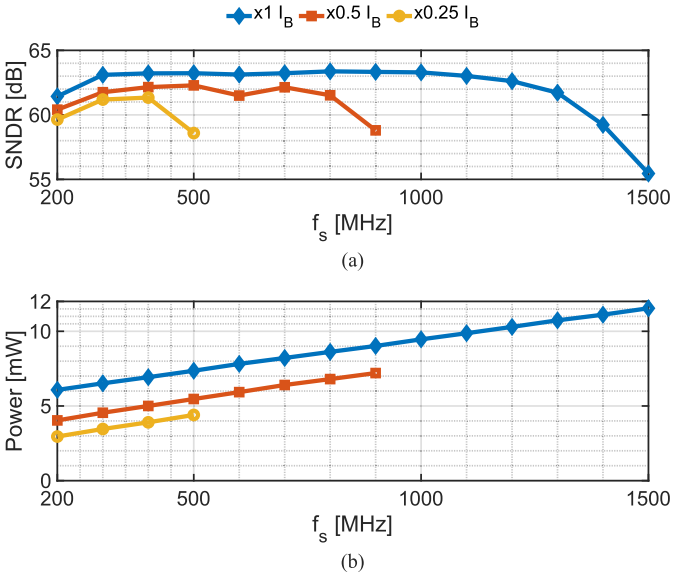


Fig. 22. Measured ADC (a) SNDR and (b) total power with sampling frequency sweep with scaled current bias for ring-amp and reference buffers.

TABLE I
COMPARISON WITH STATE-OF-THE-ART PIPELINE-BASED ADCS

	This work		ISSCC '19	VLSI '20	ISSCC '17	ISSCC '21
Process	**28nm**		28nm	16nm	14nm	7nm
Architecture	**Ringamp Pipe TI-SAR**		Gm-R Pipe SAR	Ringamp Pipe	Gm-R Pipe SAR	Pipe SAR & TI-DSM
Area [mm^2]	**0.016**		0.0091	0.095	0.0016	0.037
Supply [V]	**1**		1	0.9	0.95	0.8
Sampling Rate [MS/s]	**1000**		1000	1000	1500	600
Resolution [bit]	**12**		12	11	10	12
Input Swing [Vpp]	**1**		1.2	1.6	0.65	1
SNDR @Nyq [dB]	**62.5**		60.0	59.5	50.1	55.3
SFDR @Nyq [dB]	**80.5**		74.6	75.9	58.4	67.8
Total Reference De-cap [pF]	**44**		-	375	-	-
Include Ref. Buf. Power?	**No**	**Yes**	No	Yes	Yes	No
Power [mW]	**6.9**	**10.6**	7.6	10.9	6.9	13
FoM$_S$ [dB]	**171.1**	**169.2**	168.2	166.1	160.5	158.9
FoM$_W$ [fJ/step]	**6.3**	**9.7**	9.3	14.1	17.7	45.6

- Not reported

The supply voltage sweep and the temperature sweep results with and without recalibrating the interstage gain are shown in Fig. 21. The SNDR variation is within 0.5 dB for ±50 mV (5%) supply variation without recalibrating the gain. With gain calibration, over 62-dB SNDR can be achieved with 10% supply variations and over 80 °C temperature variations (range limited by the test equipment).

The performance and power consumption with sampling frequency sweep and scaled biasing currents (for ring-amp and reference buffers) are shown in Fig. 22. With nominal biasing currents, the ADC can work up to 1.3 GS/s within 1-dB SNDR degradation.

Table I summarizes the performance of this chip and compares it with other state-of-the-art pipelined ADCs. Our design achieves the best FoM$_S$, showing the potential of this hybrid pipelined TI-SAR architecture when combined with the ring-amp.

VI. CONCLUSION

This article describes a compact 1-GS/s 10-ENoB ADC with 10 mW power consumption. The pipelined/TI-SAR hybrid architecture simplifies the clock distribution and reduces the backend ADC overhead. The bottleneck of this architecture is the RA, and the use of the ring-amp greatly reduces the RA power. Splitting the input makes the current-reused first stage of a ring-amp work at high speed under low supply. This is achieved by splitting the MDAC into two parts rather than using level-shifting capacitors. This eliminates the drawbacks of level-shifting capacitors. The reference de-cap switching technique improves the high-frequency PSRR of the reference buffer without degrading the reference settling speed. Low-power implementations of flash ADC and backend SAR ADCs are also important to improve overall energy efficiency. This work provides a promising low-power ADC solution for receivers of next-generation wireless standards.

APPENDIX
MISMATCH ISSUE OF SPLIT MDAC

As mentioned in Section II-B, the variation in the input pair g_{mp} and g_{mn} changes the effective DAC weights in split MDAC. As in Fig. 5(b), assume that the capacitors controlled by flash decisions for P and N parts are $C_{p,t}$ and $C_{n,t}$, respectively. The ith unit-caps for P and N parts are $C_{p,i}$ and $C_{n,i}$, respectively. Hence, the ith MSB weights in each part are $C_{n,i}/C_{n,t}$ and $C_{p,i}/C_{p,t}$, respectively. The effective weight of the ith MSB is the weighted average of each part by g_{mn} and g_{mp}. It can be expressed as

$$W_i = \frac{C_{p,i}}{C_{p,t}} \cdot \frac{g_{m,p}}{g_{m,p}+g_{m,n}} + \frac{C_{n,i}}{C_{n,t}} \cdot \frac{g_{m,n}}{g_{m,p}+g_{m,n}}. \tag{2}$$

Assume g_m ratio $\alpha = (g_{m,p}/g_{m,n})$, we can get

$$W_i = \frac{C_{p,i}}{C_{p,t}} \cdot \frac{\alpha}{\alpha+1} + \frac{C_{n,i}}{C_{n,t}} \cdot \frac{1}{\alpha+1}. \tag{3}$$

If α changes to $\alpha+\Delta\alpha$, then the ith MSB weight changes to

$$W_i + \Delta W_i = \frac{C_{p,i}}{C_{p,t}} \cdot \frac{\alpha+\Delta\alpha}{\alpha+\Delta\alpha+1} + \frac{C_{n,i}}{C_{n,t}} \cdot \frac{1}{\alpha+\Delta\alpha+1}. \tag{4}$$

For $\alpha \approx 1$ (by proper sizing) and $\Delta\alpha \ll 1$, we can get

$$|\Delta W_i| = \left| \frac{\Delta\alpha}{(\alpha+1)^2} \cdot \left(\frac{C_{p,i}}{C_{p,t}} - \frac{C_{n,i}}{C_{n,t}} \right) \right| \tag{5}$$

$$\approx \left| \frac{\Delta\alpha}{4} \cdot \left(\frac{C_{p,i}}{C_{p,t}} - \frac{C_{n,i}}{C_{n,t}} \right) \right|. \tag{6}$$

This gives

$$\left|\frac{C_{p,i}}{C_{p,t}}-\frac{C_{n,i}}{C_{n,t}}\right|<\frac{4|\Delta W_i|}{\Delta\alpha}. \tag{7}$$

Assuming the mismatch properties in the P and N parts are the same, according to (7), the matching of the MSB unit-caps in the P and N parts should be better than $(2|\Delta W_i|)/(\Delta\alpha)$.

REFERENCES

[1] C.-C. Liu, C.-H. Kuo, and Y.-Z. Lin, "A 10 bit 320 MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2645–2654, Nov. 2015.

[2] J.-C. Wang, T.-C. Hung, and T.-H. Kuo, "A calibration-free 14-b 0.7-mW 100-MS/s pipelined-SAR ADC using a weighted-averaging correlated level shifting technique," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3271–3280, Dec. 2020.

[3] M. Zhan, L. Jie, X. Tang, and N. Sun, "A 0.004 mm^2 200 MS/S pipelined SAR ADC with kT/C noise cancellation and robust ring-amp," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 164–166.

[4] J. Lagos et al., "A 10.1-ENOB, 6.2-fJ/conv.-step, 500-MS/s, ringamp-based pipelined-SAR ADC with background calibration and dynamic reference regulation in 16-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1112–1124, Apr. 2022.

[5] J. Lagos, B. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, "A single-channel, 600-MS/s, 12-b, ringamp-based pipelined ADC in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 403–416, Feb. 2019.

[6] B. Hershberg et al., "Asynchronous event-driven clocking and control in pipelined ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 7, pp. 2813–2826, Jul. 2021.

[7] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.

[8] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.

[9] J. Song, K. Ragab, X. Tang, and N. Sun, "A 10-b 800-MS/s time-interleaved SAR ADC with fast variance-based timing-skew calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2563–2575, Oct. 2017.

[10] Y. Zhou, B. Xu, and Y. Chiu, "A 12-b 1-GS/s 31.5-mW time-interleaved SAR ADC with analog HPF-assisted skew calibration and randomly sampling reference ADC," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2207–2218, Aug. 2019.

[11] M. Guo, J. Mao, S.-W. Sin, H. Wei, and R. P. Martins, "A 1.6-GS/s 12.2-mW seven-/eight-Way split time-interleaved SAR ADC achieving 54.2-dB SNDR with digital background timing mismatch calibration," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 693–705, Mar. 2020.

[12] M. Brandolini et al., "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.

[13] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring amplifiers for switched capacitor circuits," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.

[14] J. Lagos, B. P. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, "A 1-GS/s, 12-b, single-channel pipelined ADC with dead-zone-degenerated ring amplifiers," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 646–658, Mar. 2019.

[15] B. Hershberg et al., "A 4-GS/s 10-ENOB 75-mW ringamp ADC in 16-nm CMOS with background monitoring of distortion," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2360–2374, Aug. 2021.

[16] B. Hershberg, N. Markulic, J. Lagos, E. Martens, D. Dermit, and J. Craninckx, "A 1-MS/s to 1-GS/s ringamp-based pipelined ADC with fully dynamic reference regulation and stochastic scope-on-chip background monitoring in 16 nm," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1227–1240, Apr. 2021.

[17] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 bit, 2.46 mW comparator-less pipeline ADC using self-biased ring amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015.

[18] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.

[19] A. ElShater et al., "A 10-mW 16-b 15-MS/s two-step SAR ADC with 95-dB DR using dual-deadzone ring amplifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3410–3420, Dec. 2019.

[20] M. Zhan, L. Jie, and N. Sun, "A 10 mW 10-ENOB 1GS/s ring-amp-based pipelined TI-SAR ADC with split MDAC and switched reference decoupling capacitor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 272–274.

[21] W. Jiang, Y. Zhu, M. Zhang, C.-H. Chan, and R. P. Martins, "A temperature-stabilized single-channel 1-GS/s 60-dB SNDR SAR-assisted pipelined ADC with dynamic Gm-R-based amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 322–332, Feb. 2020.

[22] A. M. A. Ali et al., "A 12-b 18-GS/s RF sampling ADC with an integrated wideband track-and-hold amplifier and background calibration," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3210–3224, Dec. 2020.

[23] J. K. Kim and B. Murmann, "A 12-b, 30-MS/s, 2.95-mW pipelined ADC using single-stage class-AB amplifiers and deterministic background calibration," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2141–2151, Sep. 2012.

[24] J. Wu et al., "A 5.4 GS/s 12 b 500 mW pipeline ADC in 28 nm CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. 92–93.

[25] S. Devarajan et al., "A 12-b 10-GS/s interleaved pipeline ADC in 28-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3204–3218, Dec. 2017.

[26] M. S. Akter, R. Sehgal, F. van der Goes, K. A. A. Makinwa, and K. Bult, "A 66-dB SNDR pipelined split-ADC in 40-nm CMOS using a class-AB residue amplifier," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2939–2950, Oct. 2018.

[27] R. Kapusta et al., "A 4-channel 20-to300 Mpixel/s analog front-end with sampled thermal noise below kT/C for digital SLR cameras," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 42–43.

[28] A. M. A. Ali et al., "A 14 bit 1 GS/s RF sampling pipelined ADC with background calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, Dec. 2014.

[29] S.-S. Wong, U.-F. Chio, Y. Zhu, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A 2.3 mW 10-bit 170 MS/s two-step binary-search assisted time-interleaved SAR ADC," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2012, pp. 1–4.

[30] A. M. A. Ali et al., "A 14-bit 2.5 GS/s and 5 GS/s RF sampling ADC with background calibration and dither," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.

[31] A. Sanyal and N. Sun, "An energy-efficient low frequency-dependence switching technique for SAR ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 294–298, May 2014.

[32] Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, and C.-H. Lu, "A 8.2-mW 10-b 1.6-GS/s 4x TI SAR ADC with fast reference charge neutralization and background timing-skew calibration in 16-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.

[33] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

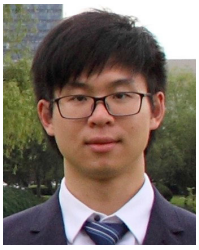
[34] L. Kull et al., "A 10 b 1.5 GS/s pipelined-SAR ADC with background second-stage common-mode regulation and offset calibration in 14 nm CMOS FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 474–475.

[35] S. Baek et al., "A 12 b 600 MS/s pipelined SAR and 2x-interleaved incremental delta-sigma ADC with source-follower-based residue-transfer scheme in 7 nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 172–174.

Mingtao Zhan (Graduate Student Member, IEEE) received the B.S. degree (Hons.) from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 2020, where he is currently pursuing the Ph.D. degree.

His research interests include high-performance data converter design and compute-in-memory.

Dr. Zhan is a recipient of the 2022–2023 Solid-State Circuits Society (SSCS) Predoctoral Achievement Award.



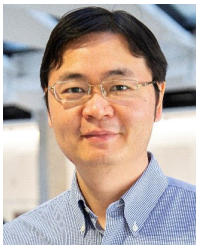
Lu Jie (Member, IEEE) received the B.Eng. degree in electrical and electronic engineering from Zhejiang University, Hangzhou, Zhejiang, China, in 2017, the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Michigan, Ann Arbor, MI, USA, in 2021.

Since 2021, he is currently with Tsinghua University, Beijing, China, as an Assistant Professor. His research interests include hybrid-architecture ADCs, high-speed circuits, and mixed-signal computation.

Yi Zhong (Member, IEEE) received the bachelor's and Ph.D. degrees in electronics engineering from the Beijing Institute of Technology, Beijing, China, in 2013 and 2020, respectively.

He was a Visiting Ph.D. Student with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX, USA, from 2015 to 2018. He was a Post-Doctoral Researcher at Tsinghua University, Beijing, from 2020 to 2022. He is currently an Assistant Research Follow with Tsinghua University. His current research is focused on time-based oversampling data converter design techniques, low-noise sensor interfaces, and high-performance synthesized ADCs.

Dr. Zhong serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.



Nan Sun (Senior Member, IEEE) received the B.S. degree (Hons.) from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 2006, and the Ph.D. degree from the School of Engineering and Applied Sciences, Harvard University, Cambridge, MA, USA, in 2010.

He is currently a Professor with the Department of Electronic Engineering at Tsinghua University. He was an Assistant Professor and then tenured an Associate Professor, with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX, USA. He has published over 200 journal and conference papers, including over 50 JSSC and ISSCC papers. He has also written seven book chapters and held seven US patents. As advisor or co-advisor, he has graduated 26 Ph.D. students, ten of whom are professors at top universities in the USA and China. His current research interests include analog, mixed-signal, and RF integrated circuit (IC) design, analog circuit design automation, sensor interfaces, miniature spin resonance systems, and solid-state platforms to analyze biological systems for biotechnology and medicine.

Dr. Sun received the NSF Career Award in 2013, and the inaugural IEEE Solid-State Circuits Society New Frontier Award in 2020. He holds Zhou Bingkun Endowed Professorship at Tsinghua University. He was the holder of the AMD Endowed Development Chair, Texas Instruments Jack Kilby Endowed Fellowship, Temple Foundation Endowed Fellowship, and Silicon Laboratories Endowed Fellowship. He has served as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, the Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS, and an Associate Editor for *Journal of Semiconductor*. He serves in the technical program committees (TPC) of ISSCC, CICC, and ASSCC. He has also served as conference chair and TPC chair for the Integrated Circuits Advances in China (ICAC) Workshop since 2019. He was the Co-Chair of the IEEE Solid-State-Circuits Society and Circuits-and-Systems Society Joint Chapter in the Central Texas Section between 2011 and 2018 and won the Chapter of the Year Award in 2014. He served as the IEEE Circuits-and-Systems Society Distinguished Lecturer from 2019 to 2021 and the IEEE Solid-State-Circuits Society Distinguished Lecturer from 2021 to 2022. He is currently the TPC Chair of CICC 2024.