A 0-dB STF-Peaking 85-MHz BW 74.4-dB SNDR CT ΔΣ ADC With Unary-Approximating DAC Calibration in 28-nm CMOS

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***Abstract*— This article presents a continuous-time (CT) ΔΣ analog-to-digital converter for wireless communication systems with a high tolerance against blockers. The zero-cancellation technique is introduced to eliminate the peaking in the signal transfer function (STF) to achieve better out-of-band-blocker immunity. An on-chip unary-approximating calibration is implemented to calibrate the mismatch of the outer current-steering digital-to-analog converter. A discrete-time (DT) second-order noise-shaping (NS) 2b/cycle asynchronous successive-approximation-register (ASAR) quantizer further reduces the quantization noise and the excess loop delay, achieving a CT-DT hybrid sixth-order NS without suffering from neither the problem of the CT-DT transfer function matching in a CT multistage NS topology nor the stability issue in a single-loop fully CT sixth-order topology. The prototype is fabricated in 28-nm bulk CMOS and is clocked at 1.7 GHz. With a bandwidth of 85 MHz, the analog-to-digital converter achieves 0-dB peaking STF, 74.4-dB signal to noise and SNDR and 87.5-dB spurious-free dynamic range, while consuming 61.8-mW power, resulting in an excellent Schreier Figure-of-Merit (FoM$_S$) of 165.8 dB.**

***Index Terms*— 2 b/cycle asynchronous successive-approximation-register (ASAR), continuous-time (CT) ΔΣ analog-to-digital converter (ADC), flat signal transfer function (STF), noise-shaping (NS) QTZ, on-chip digital-to-analog converter (DAC) calibration, out-of-band blocker (OBB).**

I. Introduction

THE ever more crowded radio spectrum causes great challenges to the design of wireless communication systems, in terms of increasing signal bandwidth (BW) as well as spectral performance. This makes continuous-time (CT) ΔΣ analog-to-digital converters (ADCs) more attractive for use in wireless applications due to their high dynamic range (DR), good power efficiency and implicit anti-aliasing property [1]–[3]. Fig. 1 shows the received spectrum at the antenna of the long-term-evolution advanced (LTE-A) standard [2], [4], [5]. For an inter-band contiguous carrier aggregation of 60 MHz, the narrowband blocker (NBB), the in-band blocker (IBB) and the out-of-band blocker (OBB) signals can be tens of dB higher than the desired signal. The OBBs can go up to more than a range of 10 GHz. Without explicit or implicit channel select filtering (CSF), the blockers significantly reduce the in-band signal DR of the backend ADC. Unfortunately, this important consideration is often not reflected in reported figure-of-merit (FoM) values for ADCs described in the literature, where the FoM values are based on in-band data only, ignoring the impact of the blockers [2], [4]. Typically, improving the out-of-band performance of converters will come at the expense of some reduction in in-band performance or some higher power.

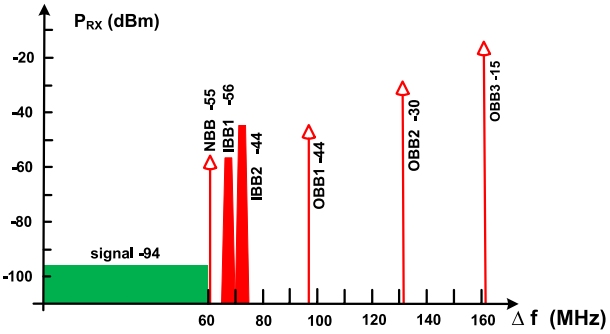

Fig. 1. Received spectrum at the antenna of the LTE-A standard.

Conventional CT ΔΣ ADCs can be divided into three subcategories, as shown in Fig. 2(a)–(c), according to their loop filter topologies: cascade of integrators with feedforward (CIFF), cascade of integrators with feedback (CIFB), and CIFF and feedback (CIFF-B) [6]. In the CIFF topology, the band-edge gain of the preceding integrator is larger than its later stages, resulting in a better suppression of the thermal noise and distortion of these later stages [1]. The CIFF topologies have achieved FoM$_S$ larger than 165 dB with BWs over 50 MHz [3], [7]–[9]. However, the peaking in the signal transfer function (STF) of the CIFF topology, as shown in Fig. 2(e), amplifies the blockers in Fig. 1 and reduces the in-band signal DR. For example in [9], an STF peaking of 8.7 dB reduces the in-band signal DR by around 10 dB [4]. The band-edge gain of the preceding integrator in the CIFB topology is lower than its counterpart in the CIFF topology resulting in a lower FoM$_S$, but the low-pass STF of the CIFB topology, as shown in Fig. 2(e), makes it popular in applications against blockers [10]–[12]. The combination of the CIFF and CIFB topology forms the CIFF-B topology, the

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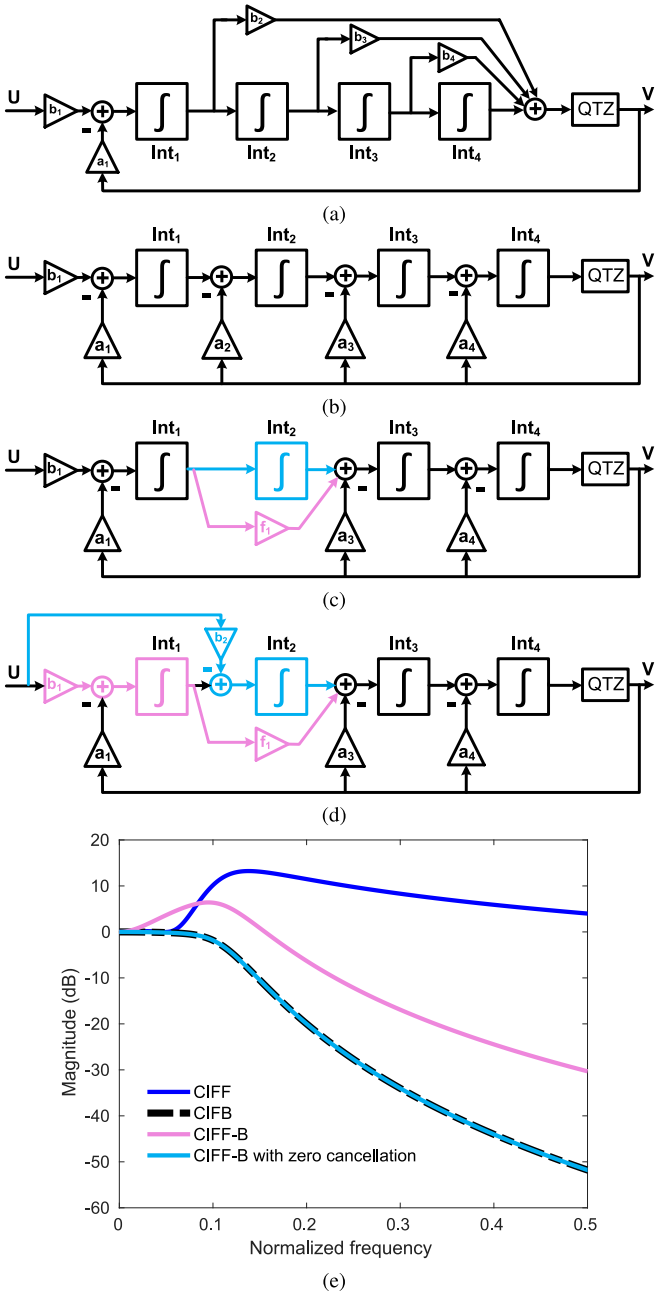

Fig. 2. (a) CIFF topology. (b) CIFB topology. (c) CIFF-B topology. (d) Proposed ZC technique. (e) STFs of different topologies.

STF peaking of which is between the CIFF case and the CIFB case [6].

Besides the single-loop CIFB topology, another way to achieve a flat or low-pass STF is adopting the multistage noise-shaping (MASH) topology [1], [13]. However, the good matching of the CT-discrete-time (DT) transfer functions of different loops is always troublesome. In [14], a method has successfully been implemented to track the process-voltage-temperature (PVT) variations of the transfer function of [1]. However, the method suffers from high complexity and results in a high power dissipation.

This work presents a CT $\Delta\Sigma$ ADC that uses several proposed techniques to simultaneously achieve a low-pass STF, a wide BW, a high power efficiency and a high linearity,

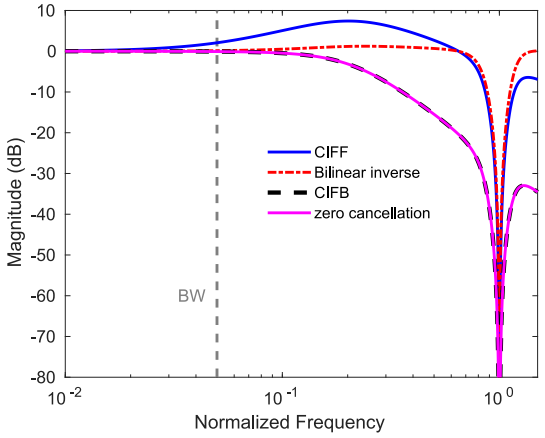

Fig. 3. STFs of CIFF $\Delta\Sigma$ ADC with ZC technique, and with the bilinear inverse technique.

resulting in an excellent FoM$_S$ as well as out-of-band performance. It uses the CIFF-B topology, but applies a zero-cancellation (ZC) technique to eliminate the STF peaking of the CIFF-B topology. A 5-bit unary-approximating digital-to-analog converter (DAC) calibration is designed and integrated on-chip to calibrate the mismatch of the outer DAC. Because of the low oversampling ratio (OSR) to achieve the high signal BW of 85 MHz, the quantization error limits the performance of the ADC. Therefore, a DT second-order noise-shaping (NS) 2 b/cycle quantizer is used to further reduce the quantization noise, achieving an excellent FoM$_S$ value without suffering from neither the problem of the CT-DT transfer function matching in a CT MASH topology nor the stability issue in a single-loop fully-CT sixth-order topology.

This article is organized as follows. Section II will describe the architecture of the proposed design. Section III will present the details of the circuit implementations. The experimental results will be described in Section IV. Conclusions will be given in Section V.

II. Architectural Design

A. ZC Technique

The diagram of the conventional CIFF-B topology is shown in Fig. 2(c) [6]. The band-edge gain of the first integrator of the CIFF-B topology is larger than that of the CIFB topology [15], which makes the input-referred noise and distortion of the second stage lower than that of the CIFB topology. However, because of the different frequency responses of the second integrator, Int_2, and the feedforward path, f_1, in Fig. 2(c), a zero occurs, which causes peaking in the STF of the CIFF-B topology, as shown in Fig. 2(e). The undesired peaking in the STF amplifies the OBBs, i.e., both the NBBs and the IBBs shown in Fig. 1. In the worst case, the amplified blockers can saturate the ADC. To suppress the STF peaking, the bilinear-inverse method has been proposed in [16] and has been implemented in silicon [2]. In this method, to suppress the STF peaking in a second-order CIFF $\Delta\Sigma$ ADC, for example, two feedforward paths are needed from the input to the second integrator and the quantizer, respectively. With this method, the STF is around unity from dc to the edge of the sampling

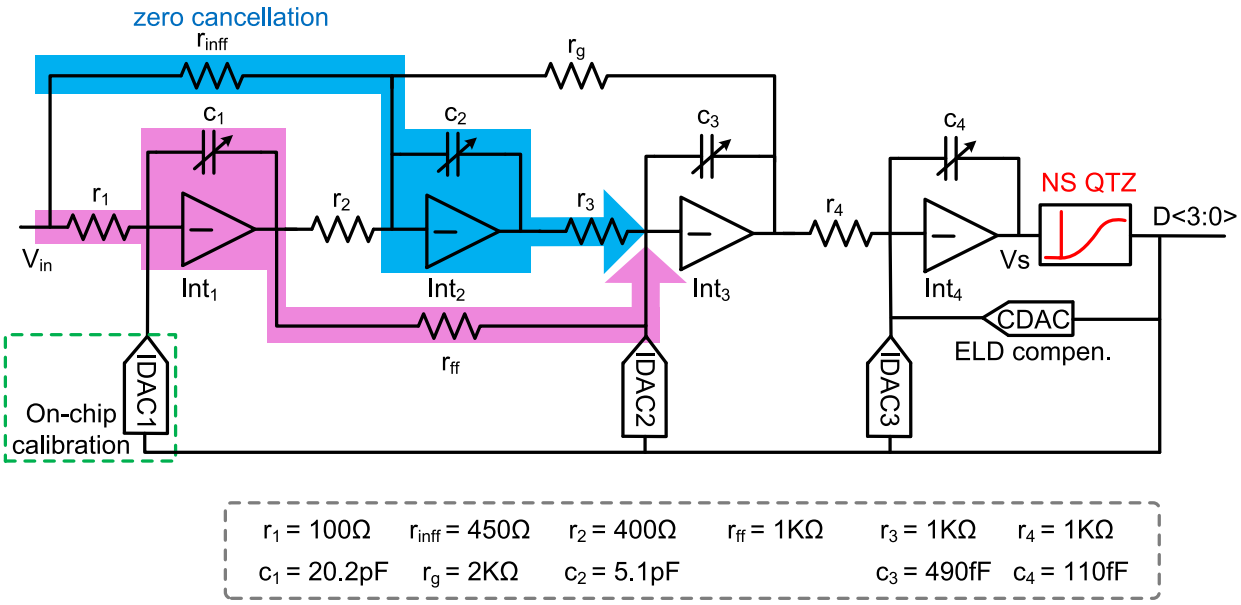

Fig. 4. System-level schematic of the presented CT ΔΣ ADC.

frequency, as shown in Fig. 3. However, the anti-aliasing property is degraded, due to the feedforward path from the input to the quantizer.

In our work a ZC technique is proposed as shown in Fig. 2(d). One more feedforward path is added from the input of the ADC to the second integrator without changing the desired noise transfer function (NTF). The signal paths, b_2-Int$_2$ and b_1-Int$_1$-f_1, have the same gain, but opposite polarity. As demonstrated in Fig. 2(e), the ZC technique eliminates the STF peaking in the conventional CIFF-B topology, to achieve a low-pass STF that suppresses the impact of OBBs. The proposed ZC technique is also applied to the aforementioned second-order CIFF ΔΣ ADC, and the result is shown in Fig. 3. When the ZC is applied, the achieved STF is the same as that of the corresponding CIFB topology.

Fig. 4 shows the system-level schematic of the proposed design, mainly consisting of a fourth-order feedforward and feedback loop filter, four 4-bit feedback DACs, the calibration of the outer current-steering DAC (IDAC1) and a second-order NS 2 b/cycle asynchronous successive-approximation-register (ASAR) quantizer. All the circuit implementations are differential. The ADC outputs 4-bit digits per sampling. The excess loop delay (ELD) of three quarters of the sampling period is compensated by the 4-bit capacitive DAC [1], [17].

The ZC path, b_2 in Fig. 2(d), is implemented by the resistor, r_{inff}, in Fig. 4. To cancel the zero in the STF, the r_{inff}-Int$_2$-r_3 path, and the r_1-Int$_1$-r_{ff} path must have the same gain, but opposite polarity, which is implemented by connecting the differential resistors oppositely. The gain of an *RC* integrator mainly depends on its resistor and capacitor, because the PVT variances of the amplifier in the integrator are suppressed by the closed loop. Therefore, the gain matching between the r_{inff}-Int$_2$-r_3 path and the Int$_1$-r_{ff} path mainly depends on the matching between r_{inff}-c_2-r_3 and r_1-c_1-r_{ff} in Fig. 4. This just needs good matching of the corresponding resistors and the corresponding capacitors, which is not problematic to

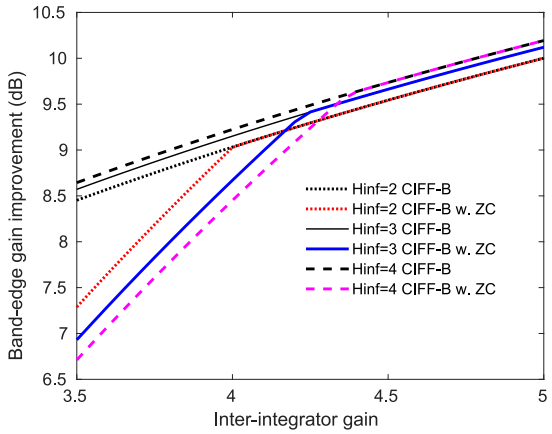

Fig. 5. Band-edge improvements of the first integrator of the CIFF-B topology with and without the proposed ZC technique.

achieve in CMOS technology. All the capacitors are digitally programmable to tune the time constant of the integrator. With an H_{inf} (maximum magnitude of the NTF) of 2 and an OSR of 10, the proposed design has the same low-pass STF as the CIFB topology, as shown in Fig. 2(e), but with improved band-edge gain of the first integrator, as shown in Fig. 5. With small inter-integrator gain, the band-edge-gain improvement of the proposed topology, compared to the CIFB topology, is worse than that of the conventional CIFF-B topology. As the inter-integrator gain increases, the gap between these two topologies becomes smaller and smaller. For example, for an inter-integrator gain of 5 like in [1], the proposed topology and the CIFF-B topology have the same band-edge gain improvement for all H_{inf} values (2, 3, and 4). In our design, a smaller inter-integrator gain is chosen due to the consideration of the post-layout parasitics, and the band-edge gain of the first integrator is 8.6 dB higher than that of the conventional CIFB topology, which relaxes the thermal noise and linearity requirements of the second stage by 8.6 dB.

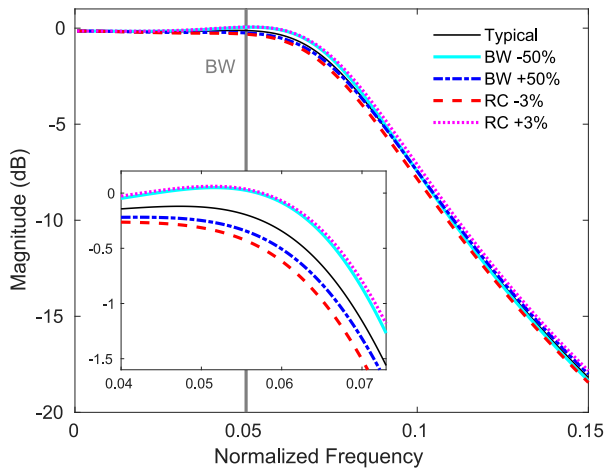

Fig. 6. STF variations versus frequency as a function of the BW mismatch of the amplifiers in INT1 and INT2, and of the *RC* mismatch in the ZC path.

The STF variations due to the BW mismatch of the amplifiers in the ZC path, are shown in Fig. 6. When the BW of the amplifier varies ±50%, the STF has a variation of 0.42 dB at 1.2 × BW. Moreover, the STF variations caused by the *RC* mismatch in the ZC path, are also shown in Fig. 6. The mismatch (δ) of r_{inff} (r_1), c_2 (c_1), and r_3 (r_{ff}) is assumed to be 1%, which is not a challenge in the used 28-nm CMOS technology. The corresponding gain mismatch of the r_{inff}-Int$_2$-r_3 path is 3%, which results in an STF variation of 0.48 dB at 1.2 × BW.

B. DAC Calibration Scheme

The distortion of IDAC2/IDAC3/CDAC in Fig. 4 is suppressed by the gain of the prior stages, while the distortion of IDAC1 directly contributes to the output. Hence, IDAC1 requires the highest linearity among all DACs. The most direct method to increase the linearity of IDAC1 is to increase the transistor size of the DAC unit [13]. However, a larger size of DAC unit introduces more loop delay and a larger dynamic error, which are not acceptable in high-speed and high-linearity design. In [18], the data-weighted averaging (DWA) technique is proposed, which achieves a high linearity. However, this method requires complex circuitry and introduces extra loop delay. Several other on-chip DAC calibration methods that do not increase the ELD, have been developed. Current-copying DAC calibration is presented by [19] and is widely adopted [3], [8]. Frequent refresh is performed to charge the capacitors, which store the calibrated voltage. Several issues are, however, caused by the refresh [20]. First, due to the frequent toggling of the calibrating switches, high-frequency noise folds back to lower frequencies. Second, the charge leakage and frequent refresh generate distortions or spurs in the frequency domain. Moreover, the refresh also consumes extra power. In [21], a dithering-based background calibration technique is implemented, but only achieves an improvement of the spurious-free DR (SFDR) with several dB, which is not sufficient for high-linearity applications. The technique in [1] and [22] is power and area efficient.

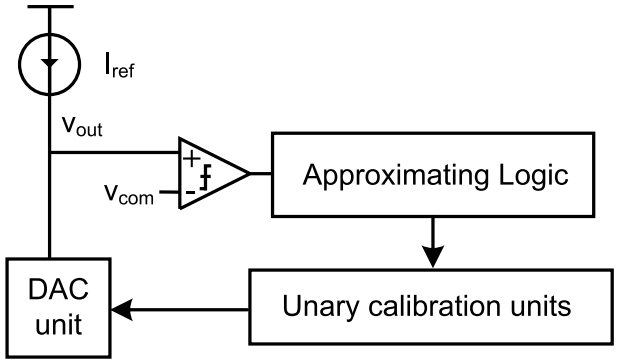

Fig. 7. Principle schematic of the proposed unary-approximating DAC calibration.

However, an on-chip microprocessor is needed to compute the calibration coefficients [1], which greatly increases the complexity of the design.

Fig. 7 illustrates the principle schematic of the proposed unary-approximating DAC calibration, which leads the calibrated DAC unit to unarily approximate the reference current during the calibration phase. The presented DAC calibration consists of four parts: the DAC unit to be calibrated, the current reference I_{ref}, the approximating logic circuit and the unary calibration units. The DAC unit to be calibrated is connected to I_{ref}, the output of which is quantized by a comparator. If the current of the DAC unit is less than the reference current, the comparator outputs "1," and the approximating logic injects one more unit current (current of a calibration unit) to the DAC unit through the unary calibration units. If the current of the DAC unit is more than the reference current, the comparator outputs "0," and the approximating logic takes off one more unit current from the DAC unit through the unary calibration units. In this way, the current of the DAC unit approximates I_{ref}. Once the calibration is finished, the status of the unary calibration units is digitally locked by the approximating logic. The proposed method has simple logic circuitry, does not have any static power consumption and does not need a frequent refresh.

The proposed calibration technique is aiming at reducing the static errors of the DAC. However, the dynamic errors of the DAC are related to the size of the DAC unit [1]. With the proposed unary approximating calibration technique, a smaller size of the DAC unit is possible to achieve the same linearity compared as the uncalibrated DAC, which thus helps to reduce the dynamic errors.

C. Second-Order NS 2 b/Cycle Quantizer

The theoretical maximum signal-to-quantization-noise ratio (SQNR) of a single-loop ΔΣ ADC is as follows: [23]:

$$\text{SQNR(dB)} \approx 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log_{10}(\text{OSR}) \quad (1)$$

where N and L are the (effective) number of bits of the quantizer and the loop filter order, respectively. As indicated in (1), increasing either of N, L, and OSR improves the

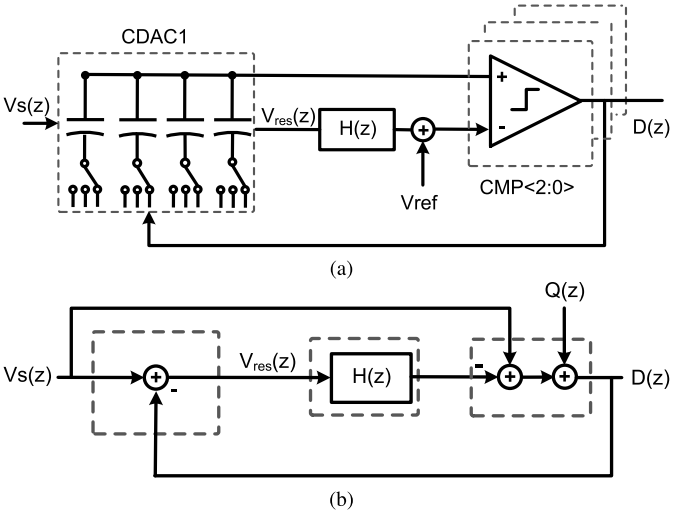

Fig. 8. (a) Schematic and (b) equivalent signal flow of the proposed NS 2 b/cycle quantizer.

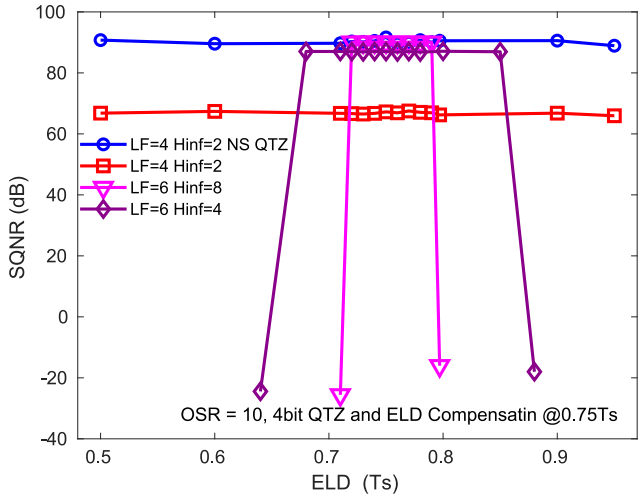

Fig. 9. SQNR robustness versus the ELD for the presented topology and for conventional topologies.

SQNR. However, N is generally not larger than 4, because the ELD compensation and the DAC calibration are troublesome for N larger than 4. The higher the loop filter order, the more unstable the closed loop is. Hence, this design chooses a loop filter of 4. The OSR of this design is limited to 10 by the given technology in combination with the high input BW of 85 MHz. With a 4-bit QTZ, a fourth-order loop filter, an OSR of 10, and an H_{inf} of 2, the SQNR would be 68.7 dB, which limits the performance of the ADC. In order to further increase the SQNR, the MASH topology is another option. However, it is always challenging to extract and match the digital transfer function of the different loops. Alternatively, the sturdy version of the MASH (SMASH) topology could be used, but requires a good match between the DACs of the different loops and the second loop increases the loop delay of the ADC [3]. The SMASH topology also suffers from a quantization noise penalty, compared to a standard MASH system [13].

In order to avoid the matching challenges of a CT MASH configuration and the stability issue in single-loop higher-order topology, NS quantizers (NS-QTZs) emerged and were widely used to increase the SQNR in single-loop CT ΔΣ ADCs [7], [24], [25]. Among all NS-QTZs, the NS SAR (NS-SAR) topology, presented in [26], is preferred for its simple logic circuitry and high-order NS. In the conventional NS-SAR [26], four comparisons are operated to output four digital bits, and the long conversion time reduces the sampling frequency.

In our design, a second-order NS 2 b/cycle ASAR QTZ is proposed, the schematic of which is shown in Fig. 8(a). It consists of three parts: a CDAC1, a residue error filter with a transfer function of H(z), and three comparators. After each conversion, the residue error on the CDAC1, $V_{res}(z)$, is fed to the H(z) block. Its output together with the reference voltage, V_{ref}, are used to generate the negative input of the three comparators, CMP⟨2:0⟩, for the next conversion.

The equivalent signal flow of Fig. 8(a) is shown in Fig. 8(b) [26]. Based on the signal flow, the STF of the QTZ, STF_{QTZ}, is 1, which does not change the overall STF discussed in Section II-A. The NTF of the QTZ, NTF_{QTZ}, is a

$$NTF_{QTZ} = \frac{D(z)}{Q(z)} = \frac{1}{1 - H(z)} \tag{2}$$

where $Q(z)$ is the quantization error. In order to get a second-order NS ($NTF_{QTZ} = (1 - z^{-1})^{-2}$), $H(z)$ is derived as

$$H(z) = \frac{2z^{-1} - z^{-2}}{(1 - z^{-1})^2} = \underbrace{\frac{2z^{-1}}{1 - z^{-1}}}_{\text{1 Int. with gain 2}} + \underbrace{\frac{z^{-2}}{(1 - z^{-1})^{-2}}}_{\text{2 Int. in series}}. \tag{3}$$

The first part of $H(z)$ is an integrator with a gain of 2 and the second part of $H(z)$ is two integrators in series, which are easy to implement with switched-capacitor circuits. With an OSR of 10 and second-order NS, the proposed NS-QTZ achieves more than 60-dB SQNR. The overall NTF of the CT ΔΣ ADC is

$$NTF = NTF_{LF} \cdot NTF_{QTZ} \tag{4}$$

where NTF_{LF} is the NTF generated only by the loop filter. The overall NTF achieves an equivalent sixth-order NS. Because of the low autocorrelation of the quantization noise, the filtered residue error is similar to a dithering signal injected to the loop [27]. Hence, the stability is comparable to a fourth-order ΔΣ ADC. To verify this conclusion, simulations have been performed, as shown in Fig. 9. All topologies are compensated for an ELD of 0.75 T_s, where T_s is the sampling period. With an OSR of 10- and 4-bit QTZ, sixth-order NS is needed for a conventional single-loop topology to achieve an SQNR over 90 dB, which however degrades drastically as the actual ELD deviates from 0.75 T_s. In our presented topology, Fig. 9 shows that the SQNR remains as robust as the conventional single-loop fourth-order ΔΣ ADC.

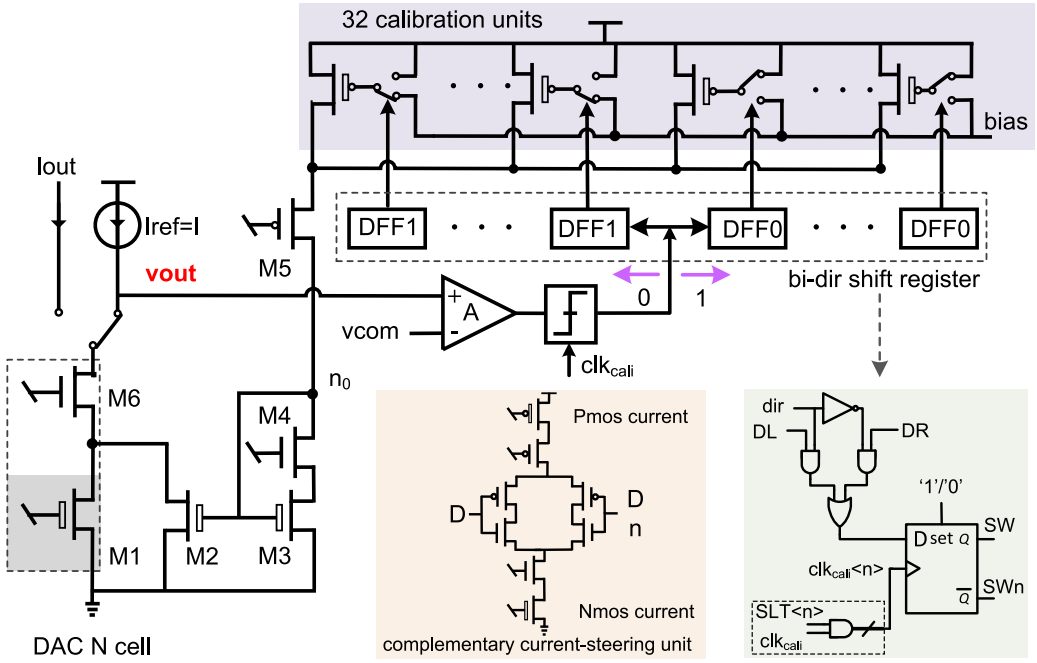

Fig. 10. Schematic of the on-chip 5-bit unary-approximating DAC calibration.

III. Circuits Implementations

A. DAC Calibration Circuits

The complementary current-steering DAC, as shown in Fig. 10, is widely used in CT ΔΣ ADCs for its high power efficiency and low thermal noise [13], [28], [29]. Since the thermal noise and distortion of IDAC1 directly contribute to the output similar to the input signal, a supply of 1.5 V had to be used in IDAC1 to achieve sufficient voltage headroom for lower noise, while all other DACs are powered with a low supply of 1.1 V.

IDAC1 is calibrated on-chip. The schematic of the proposed 5-bit unary-approximating DAC calibration is shown in Fig. 10. The calibration of an nMOS current source is given here as an example. A reference current source, an amplifier, a comparator and 32 calibration units constitute the calibration block for each DAC cell. All drain terminals of the calibration units are connected together. The gates of the calibration units are controlled by bi-directional shift registers, which can be set to "1" or "0." When the bi-directional register outputs "1," the gate of the calibration unit is connected to the bias voltage and the calibration unit outputs a unit of the calibration current. When the bi-directional register outputs "0," the gate is connected to the source and the calibration unit is cutoff. All gates of the calibration units are connected to the cascode p-type transistor, M_5, to reduce the channel length modulation. The drain current of M_5 goes through a cascode current mirror, consisting of M_2, M_3, and M_4, and is then injected into the DAC cell. The output of the DAC cell, the drain of M_6, is connected to the reference current, I_{ref}. The output node of the reference current, V_{out}, is amplified and then quantified by the comparator, the output of which determines the gate voltage of the calibration unit by changing the state of the bi-directional shift register.

By default, half of the 32 unit currents are injected into the DAC cell, through the current-mirror transistor, M_2, and the other half of the 32 unit currents are cutoff. In the calibration phase, the comparator is clocked by the calibration clock signal, clk_{cali}. If V_{out} is lower than V_{com}, which means that the current of the DAC cell is higher than I_{ref}, the comparator outputs "0," after the rising edge of clk_{cali}. Then the bi-directional register moves to the left and the gate of one calibration unit is connected to its source, leading the current of the current mirror to be reduced by one unit of the

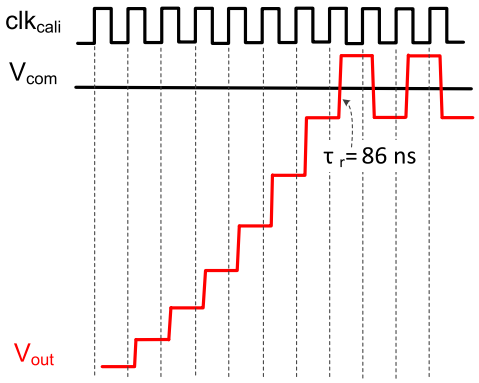

Fig. 11. DAC calibration timing.

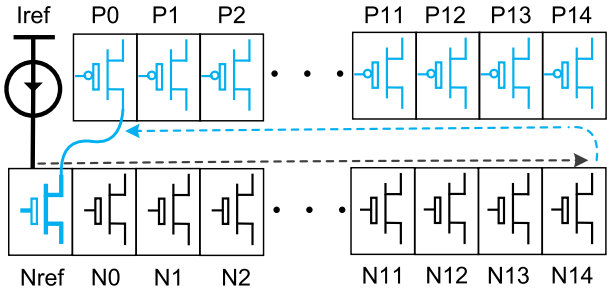

Fig. 12. DAC calibration sequence.

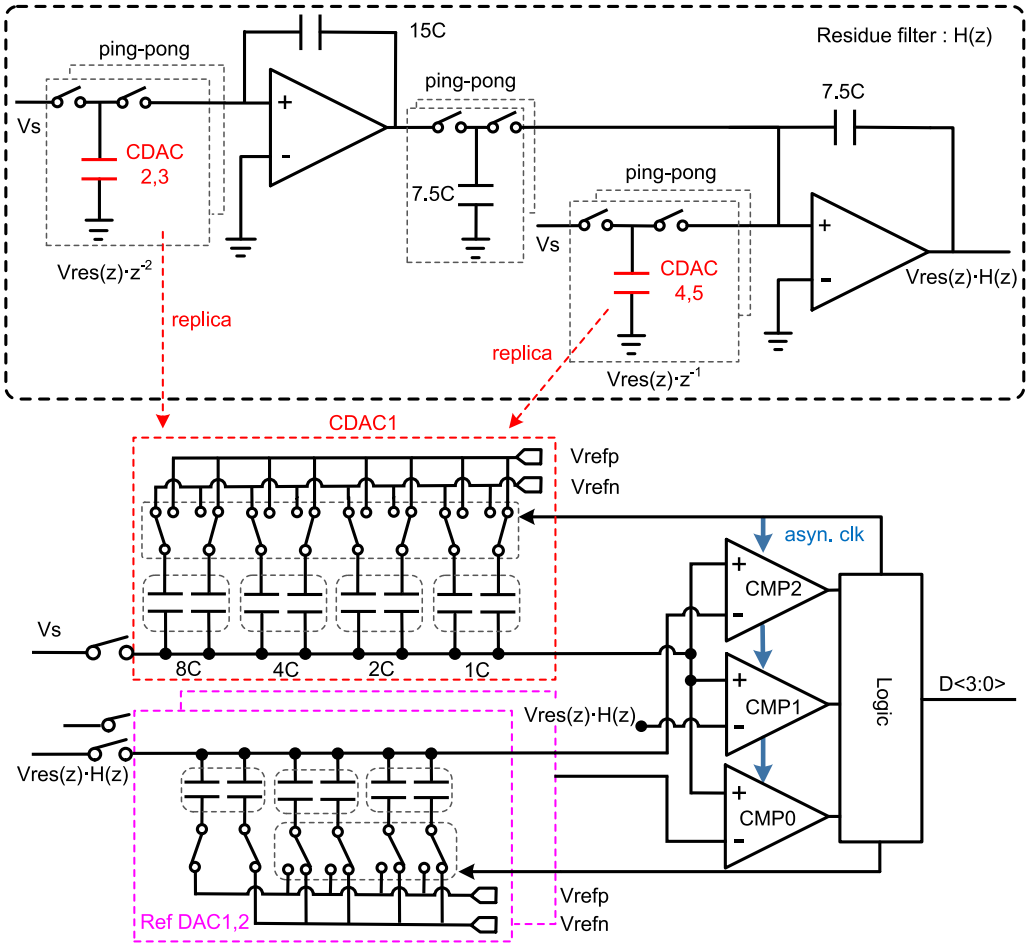

Fig. 13. Single-ended schematic of the proposed second-order NS 2 b/cycle ASAR quantizer (note that the actual implementation is differential).

calibration current. Since the drain current of M_6 is reduced and approximates I_{ref} more closely, V_{out} increases in the first few clock cycles as shown in Fig. 11. If V_{out} is higher than V_{com}, which indicates that the current of the DAC cell is less than I_{ref}, the comparator outputs "1." Then the bi-directional register moves to the right and the gate of one calibration unit is connected to the bias voltage, resulting in increasing the drain current of M_6, which also approximates I_{ref} more closely, as shown in the last few clock cycles in Fig. 11. Hence, the current cell is made as closely as possible to the reference current. After the calibration of one DAC cell, the values of the involved shift registers are locked and kept constant for the remainder of the operations.

The entire calibration sequence is illustrated in Fig. 12. First, the nMOS current reference is calibrated. Second, the 15 nMOS current sources of IDAC1 are calibrated, one after another by I_{ref}. Thereafter, the 15 pMOS current sources of IDAC1 are calibrated similarly by the nMOS current reference. The implemented on-chip calibration is operated at 0.83 MHz. Around the common-mode voltage, V_{out} has a rise time of 86 ns, which is 7% of the period of the calibration clock. The amplifier and comparator in Fig. 10 are shared by the calibration of all DAC cells and are turned off after all calibrations have been done to avoid static power consumption. Monte Carlo simulations show that the DAC cell has a standard deviation (δ) of 0.5%. The 32 calibration units cover a range from $-1.1\% \cdot I_{\text{ref}}$ to $+1.1\% \cdot I_{\text{ref}}$. The calibrated DAC achieves a linearity over 14 bits [25]. Furthermore, unlike the DAC current-copying calibration in [3] and [8], frequent refreshing is not needed in our proposed method.

B. NS-QTZ Circuits

Fig. 13 shows the single-ended schematic of the proposed NS QTZ, including the residue-error filter H(z) (at the top) and the 2 b/cycle ASAR (at the bottom). Note that all actual implementations of the circuits are differential.

The ASAR consists of the signal capacitive DAC (CDAC1), the reference capacitive DACs, the comparators and the logic circuits. The output of the loop filter, V_s in Fig. 4, is sampled by CDAC1. The residue filter processes the residue error, $V_{\text{res}}(z)$, and its output, $V_{\text{res}}(z) \cdot H(z)$, is sampled by the reference DACs, which performs the summation of $V_{\text{res}}(z) \cdot H(z)$ and the reference voltage in Fig. 8(a). The sampled voltage of CDAC1 is quantized by the three dual-input comparators, as shown in Fig. 14, for its simple clock distribution [30]. The logic circuits provide an asynchronous clock for the three comparators, and then switch CDAC1 and the reference DACs according to the comparison result. The output of the

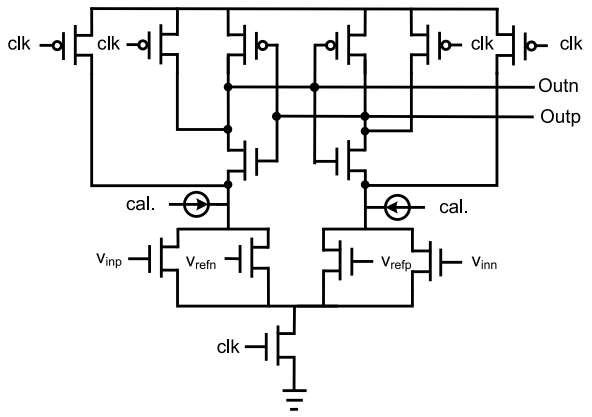

Fig. 14. Schematic of the dual-input comparator [30].

comparators is converted into binary code for off-chip data capture. Both CDAC1 and the reference DACs use a split-capacitor array for all the weights. The unit capacitor of the QTZ CDACs is 1 fF, which is split into two 0.5-fF capacitors. To design all capacitors in Fig. 13, metal 7 is used because of its reduced parasitic contribution [31].

In the proposed QTZ, the key to enhance the conversion speed is to generate $V_{\text{res}}(z)$. In [21], the residue error is generated and sampled after the conversion of the last bit, which increases ELD. Therefore, the method to generate the residue error from [32] is adopted here. Four independent replicas (CDAC2 to CDAC5) of the core CDAC1 are used to generate the required delayed versions of the residue error ($V_{\text{res}}(z) \cdot z^{-2}$ and $V_{\text{res}}(z) \cdot z^{-1}$). These replicas work pairwise in ping-pong mode: one CDAC transfers the residue error to the integrator and waits for the settling of the amplifier, while the other CDAC samples and holds the output of the loop filter. For instance, when CDAC2 is transferring $V_{\text{res}}(z) \cdot z^{-2}$ to the integrator, CDAC3 samples and holds V_s. For the next clock period, the two CDACs are operated the other way around. The operation of CDAC4 and CDAC5 is the same as that of CDAC2 and CDAC3.

The QTZ completes the entire conversion in two asynchronous cycles and outputs 4-bit digital outputs in total. A duration of 295 ps is allocated to the whole conversion of the QTZ to ease the metastability issue of the asynchronous logic. The on-chip signal propagation and the toggling of the DACs take 146 ps. Together with the 0.25 T_s for the ELD compensation, the minimum free time for $H(z)$ to settle is 250 ps, without causing additional loop delay. With an OSR of 10, the post-layout simulations show that the QTZ should achieve an in-band signal to noise and distortion ratio (SNDR) of 54.5 dB.

C. Amplifier

All amplifiers in the integrators adopt the topology from [21], but with double current tails in the second stage to achieve a better common-mode rejection, as shown in Fig. 15. For the common-mode signal, the output resistance of the second stage is almost the same, with or without the PMOS tail. However, the transconductance of transistor M_2 is

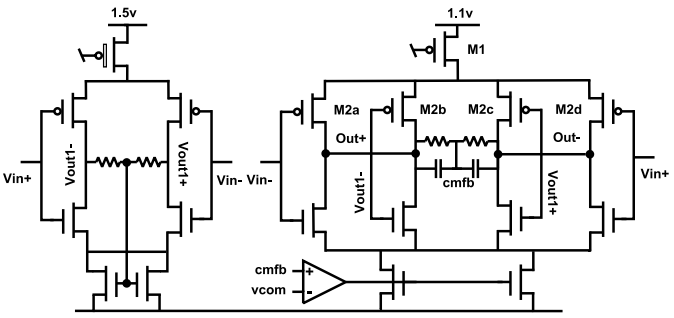

Fig. 15. Schematic of the fully differential class-A push-pull amplifier.

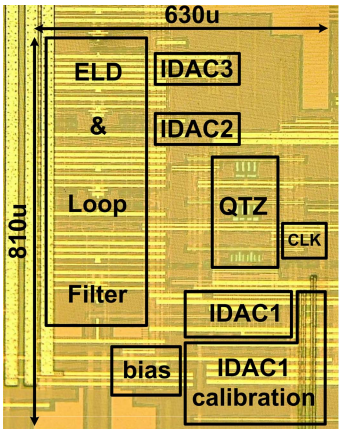

Fig. 16. Die photograph of the chip designed in 28-nm bulk CMOS technology.

reduced, due to the source degeneration caused by the output resistance of the tail transistor M_1. Therefore, the second stage achieves a lower common-mode gain with the double current tails. The second stage of the amplifiers has a low output resistance to isolate the small resistor of the following stage and to minimize the load effect as occurring in [28].

IV. Experimental Results

The prototype of the CT $\Delta\Sigma$ ADC has been fabricated in 28-nm bulk CMOS. Fig. 16 shows the die photograph of the test chip, which has a core active area of 0.51 mm^2. The ADC is clocked at 1.7 GHz and the signal BW is 85 MHz, resulting in a relatively low OSR of 10. Fig. 17 plots the 16K-point fast Fourier transform (FFT) results of the measured digital bits for a 7.5-MHz −4.0-dBFS input signal with and without the DAC calibration. Without the DAC calibration, the mismatch of IDAC1 severely degrades the performance and limits the SFDR and SNDR to 66.3 and 63.7 dB, respectively. When the DAC calibration is on, an SFDR of 87.5 dB and an SNDR of 74.4 dB are achieved, with corresponding improvements of 21.2 and 10.7 dB, respectively. The performance improvements validate the effectiveness of the proposed DAC calibration. The measured STF is shown in Fig. 18, which indeed has the desired low-pass characteristic. The measured STF not only has 0-dB STF peaking, but also exhibits an excellent −13.6-dB attenuation at 255 MHz (= 3 times the BW), which is excellent for wireless communications.

TABLE I
PERFORMANCE COMPARISON TO PRIOR WORKS

Specifications	**This work**	Dong [13] JSSC 2014	Yoon [3] JSSC 2015	Loeda [2] JSSC 2016	Dong [1] JSSC 2016	Qi [9] JSSC 2020
Architecture	**CT FF-FB**	CT MASH	CT FF	CT FF	CT MASH	CT FF
Process (nm)	**28**	28	28	40	28	28
Fs (GHz)	**1.7**	3.2	1.8	2.4	8.0	1.2
OSR	**10**	30	18	30	8.6	12
Supply Voltage (V)	**1.5/1.1/1.0**	1.8/0.9/-1.0	1.8/1.0	N.A.	1.8/1.0/-1.0	1.5/1.2
Active Area (mm^2)	**0.51**	0.9	0.34	0.02	1.4	0.085
Power (mW)	**61.8**	235	80.4	5.3	890	29.3
BW (MHz)	**85**	53	50	40	465	50
Peak SNR (dB)	**76.4**	83.1	76.1	N.A.	68	77.5
Peak SNDR (dB)	**74.4**	71.4	74.9	66.9	67	76.6
DR (dB)	**79.3**	88	85	67.8	72	80.0
STF Peaking (dB)	**0**	0	6.0	2.0	0	8.7
Attenuation @3xBW (dB)	**-13.6**	0	∼0	∼-2.5	∼-5	–
FoM_S (dB)*	**165.8**	154.9	162.8	165.7	154.2	168.9

* $FoM_S = SNDR + 10\log_{10}(\frac{BW}{Power})$ (dB)

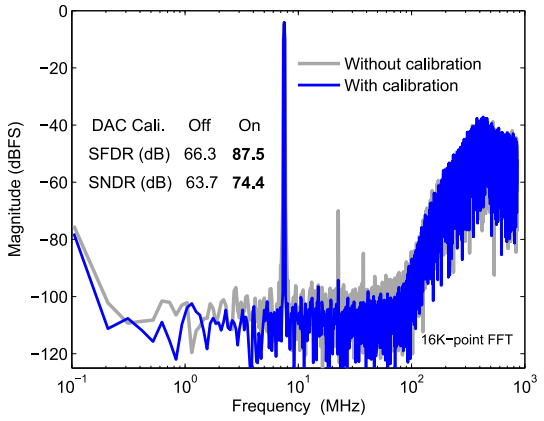

Fig. 17. Measured spectra of a 7.5-MHz −4.0-dBFS input with and without the on-chip DAC calibration.

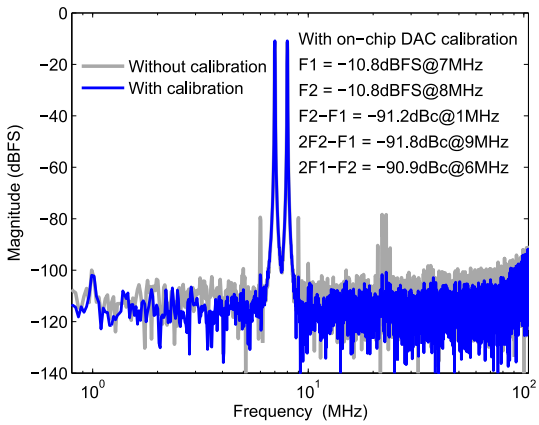

Fig. 19. Measured spectra of a two-tone input signal at 7 and 8 MHz with and without the on-chip DAC calibration.

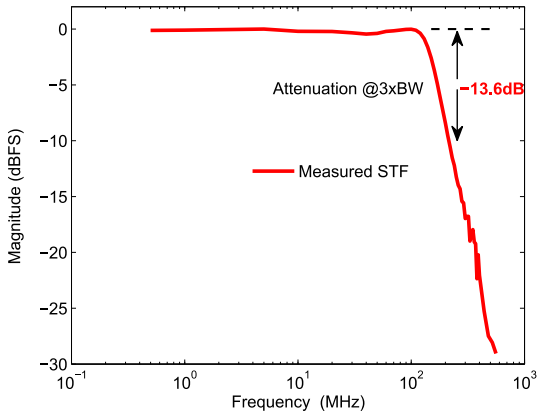

Fig. 18. Measured STF with no peaking and high low-pass attenuation.

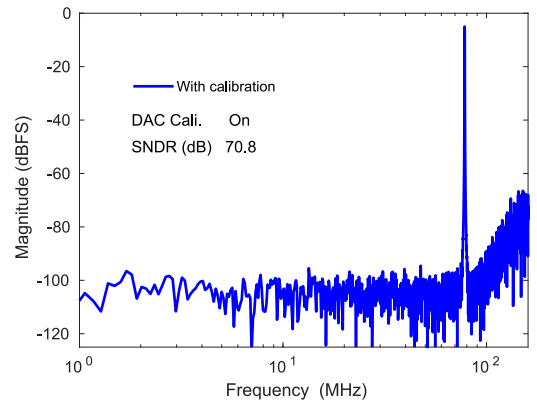

Fig. 20. Measured spectrum of a 78.125-MHz −4.0-dBFS input with the on-chip DAC calibration.

Fig. 19 shows the spectra for two −10.8-dBFS input tones at 7 MHz (F_1) and 8 MHz (F_2), with DAC calibration on and off. Without the DAC calibration, IM3 is −68.6 dBc at 6 MHz ($2F_1 - F_2$) and is −68.6 dBc at 9 MHz ($2F_2 - F_1$). When the DAC calibration is on, IM3 is improved to −90.9 dBc at 6 MHz and to −91.8 dBc at 9 MHz. After the DAC

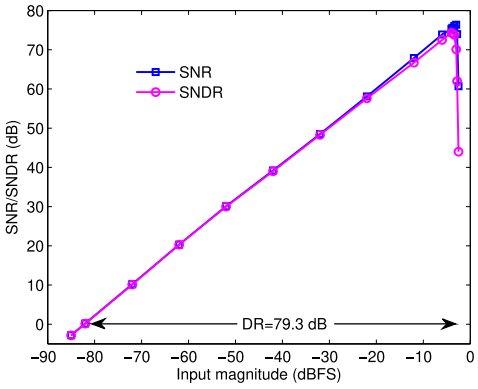

Fig. 21. Measured SNR and SNDR versus the input amplitude with input signal at 7.5 MHz.

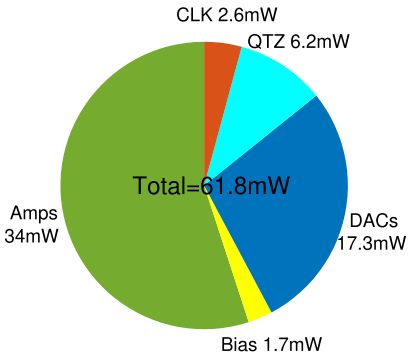

Fig. 22. Power consumption distribution.

calibration, IM2 is not improved a lot and is −91.2 dBc at 1 MHz ($F_2 - F_1$). With the on-chip DAC calibration, the measured spectrum for a 78.125-MHz −4.0-dBFS input is shown in Fig. 20. The corresponding SNDR is 70.8 dB, which is 3.6 dB worse than that of the low-frequency input, most probably due to the increased errors of the IDACs at high frequencies.

Fig. 21 shows the measured SNR and SNDR versus the input amplitude for an input signal of 7.5 MHz. The peak SNR is 76.4 dB, and the corresponding DR is 79.3 dB. The power consumption distribution is illustrated in Fig. 22. The ADC consumes 61.8 mW from the 1.5/1.1/1.0 V supplies, which leads to a FoM$_s$ of 165.8 dB. The majority of the power consumption (34 mW) is dissipated by the amplifiers to reduce the thermal noise of the first two integrators.

Table I summarizes the measured performances of the presented ADC and compares it to other state-of-the-art wideband CT $\Delta\Sigma$ ADCs. With the proposed ZC technique, the design achieves a flat-STF ADC and a −13.6 dB attenuation at 3 × BW, which is the largest attenuation among all the state-of-the-art designs listed in Table I. The described design achieves a Schreier FoM$_S$ of 165.8 dB, which is comparable to feedforward $\Delta\Sigma$ topologies and is the best among all CT $\Delta\Sigma$ ADCs with flat STFs.

V. Conclusion

This article has described a 0-dB STF-peaking 85-MHz BW 74.4-dB SNDR CT $\Delta\Sigma$ ADC. The excellent performance results are achieved by applying several proposed techniques. First, ZC is used to eliminate any STF peaking in the CIFF-B topology, while keeping the CIFF-B advantages. Second, an on-chip 5-bit unary-approximating DAC calibration, without static power consumption, is implemented to reduce the mismatch of the outer current-steering DAC in the loop. Third, a DT second-order NS 2 b/cycle ASAR quantizer is used to further reduce the quantization error. The overall ADC, implemented in 28-nm bulk CMOS, achieves an STF attenuation of −13.6 dB at three times the BW, and obtains the best FoM$_S$ value of 165.8 dB among all wideband CT $\Delta\Sigma$ ADCs with flat STF.

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