Design of High-Resolution Continuous-Time Delta–Sigma Data Converters With Dual Return-to-Open DACs

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***Abstract*— We present design techniques for single-bit continuous-time delta–sigma modulators that attain high resolution (>16 bits) over a bandwidth (BW) that is more than ten times the audio range. We introduce the zapped, virtual-ground-switched dual return-to-open DAC which is immune to ISI and other transition-dependent errors. FIR feedback facilitates chopping, improves clock-jitter sensitivity and the loop filter's linearity. We show that the compensation FIR DAC, which is typically bulky, can be implemented in an extremely power- and area-efficient manner in a single-bit modulator using a capacitive DAC and passive summation. Thanks to these techniques, the fabricated prototype achieves 103.2-/104.3-dB signal to noise and distortion ratio (SNDR)/signal to noise ratio (SNR) in a 250-kHz bandwidth while operating at 48 MS/s. Consuming 17.7 mW from a 1.8-V supply, the modulator occupies 1.1 mm^2 in a 180-nm CMOS process. The Schreier (SNDR) figure of merit (FoM) is 174.7 dB.**

***Index Terms*— Chopping, compensation, continuous-time, delta-sigma, feedforward, finite impulse response (FIR) feedback, flicker noise, oversampling, passive summation, precision, return-to-open (RTO), return-to-zero (RZ), single-bit, three-stage, virtual-ground-switched.**

I. Introduction

SEVERAL emerging applications, such as condition monitoring for predictive maintenance, sonars, acoustic, and seismic measurements use wide-bandwidth (BW), low-noise sensing technologies [1], [2]. Such signal chains require ADCs with low noise (signal to noise and distortion ratio (SNDR) > 100 dB) and wide input bandwidth (>100 kHz). A CTΔΣM is an attractive choice, thanks to its resistive input and inherent anti-alias filtering. Consequently, a continuous-time signal chain does not require an explicit input driver or anti-alias filter. The reference-buffer design is also simplified. As a result, the board area can be greatly reduced [3].

The CTΔΣM described in this work aims to achieve 105-dB SNDR over a 250-kHz bandwidth in a 180-nm CMOS process. A survey of state-of-the-art high-resolution CTΔΣMs shows that almost all designs that achieve SNDR > 96 dB (16 + bits) do so over audio or lower BWs [4]–[10]. An exception is a design reported in [11], which was our first attempt to achieve 18-bit precision over 10× the audio BW. That design employed a nine-level quantizer and an 8-tap FIR DAC. The use of FIR feedback improved the linearity of the input integrator of the CTΔΣM, facilitated chopping, and reduced the sensitivity of the converter to clock jitter. As discussed in detail in [11], reference-path resistance, inter-symbol interference in the feedback DAC, and flicker-noise suppression were the key challenges encountered in the design. They were addressed using the virtual-ground-switched-resistor DAC and by chopping, respectively.

The converter of [11] performed well. In retrospect, however, there were two aspects that needed improvement. The first was the manner in which element mismatch in the feedback DAC was addressed. Theertham *et al.* [11] employed data-weighted averaging (DWA) in view of its simplicity. This, however, resulted in in-band tones and a kink in the SNDR-amplitude characteristic. This could be problematic in some applications, as will be described in Section II.

Another avenue for improvement was power dissipation. Analysis of the current draw of the CTΔΣM indicated that a large portion of the power was due to switching. The reason turned out to be the following. Of the active area of 2.85 mm^2 occupied by the CTΔΣM, 60% (1.6 mm^2) was occupied by the main-FIR feedback and compensation-FIR DACs. This was due to a large number of unit elements (≈70) needed to realize them. Consequently, long routing traces were required to distribute the clock across the chip, which resulted in significant power dissipation in the clock-drive circuitry. Another contributor to the current-draw of the converter was the circuitry used to drive the DAC switches. The post-layout power audit of the converter thus indicated that the large number of DAC unit elements are primarily responsible for a significant portion of the modulator's power dissipation and area.

Recognizing that multibit operation and a large number of unit elements limit the performance of [11], this work explores the use of a single-bit CTΔΣM architecture with FIR feedback and fewer unit elements (12 in our design) as an alternative approach to achieve similar design goals. Moving to a single-bit quantizer will necessarily reduce the maximum stable amplitude (MSA) of the modulator, which will, in turn, increase power drawn from the references and that dissipated in the input integrator. However, the design of the quantizer and that of the OTA driving it will be much simpler. Since the number of unit elements is reduced, switching power is expected to reduce greatly. Furthermore, it turns out that single-bit operation also allows the realization

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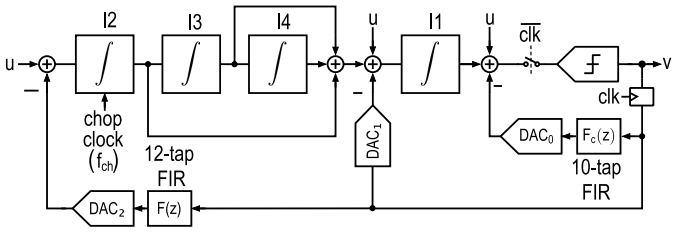

Fig. 1. Simplified high-level architecture of the CTΔΣM.

of the compensation FIR DAC in a very area- and power-efficient manner. Finally, single-bit CTΔΣM avoids the problems associated with dynamic element matching.

Based on the thought process described above, we decided to design and fabricate a single-bit CTΔΣM test chip. It turned out that we needed to pay special attention to inter-symbol-interference (ISI) in the main feedback DAC. We addressed it through the use of a zapped virtual-ground-switched dual return-to-open (RTO) DAC structure. The details of the testchip, measurements, and comparison with the multibit design of [11] form the subject of the rest of this article, which is organized as follows. In Section II, we describe the architecture and justify our design choices. Section III discusses challenges with the resistive NRZ DAC. Although the virtual-ground-switched-resistor DAC [11] is a promising solution to deal with reference path parasitic resistance and inductance, it suffers from the data-dependent transient errors due to switch and parasitic capacitance mismatch. A solution to these problems is the zapped virtual-ground-switched dual RTO (DRTO) DAC, which we describe in Section IV. Section V gives circuit design details. Measurement results from a prototype CTΔΣM chip, fabricated in a TSMC 180-nm CMOS process, are given in Section VI. Thanks to the architectural choices and the circuit innovations made, the design achieves an SNDR/signal to noise ratio (SNR) of 103.2/104.3 dB in 250-kHz BW while sampling at 48 MHz. The resulting Schreier (SNDR) figure of merit (FoM) is 174.7 dB. The converter occupies an area, which is about 2.5× smaller, compared to that occupied by [11]. Section VII concludes this article.

II. Architectural Choices

Fig. 1 shows the simplified architecture of the CTΔΣM. It employs a single-bit quantizer with 12-tap FIR feedback. The fourth-order, maximally flat noise transfer function (NTF) has an out-of-band gain of 1.4. The ADC is clocked at a sampling rate $f_s = 48$ MHz, resulting in an oversampling ratio (OSR) of 96. The simulated peak in-band SQNR is about 118 dB. The loop filter is implemented as a cascade of integrators with feed-forward and feedback (CIFF-B). Thanks to this architecture, the high-precision path (through DAC$_2$-I2-I3-I4-I1) and the high-speed (through DAC$_1$-I1) path can be independently optimized [12]. The integrators are realized using active-*RC* techniques for low noise and high linearity. *RC* time-constant variations are addressed by the use of digitally-switchable resistor and capacitor banks. The optimized zeros in the NTF are realized by weak resistive feedback around I2-I3 and I4-I1 (not shown explicitly in Fig. 1 to reduce clutter). The feed-ins from u to the output of integrators I4 and I1 ensure that there is no low-frequency component at the respective integrator outputs. Consequently, smaller integrating capacitors can be used I1 and I4. The 1-bit quantizer incorporates a half-clock cycle delay to give it sufficient time to regenerate. The flicker noise of the OTA used in the input integrator I2 is addressed by chopping.

The main feedback path $F(z) - \mathrm{DAC}_2$ is a 12-tap FIR DAC with identical tap weights. FIR feedback reduces the step size of the feedback DAC waveform, which not only relaxes I2's linearity requirements but also reduces the susceptibility of the modulator to clock jitter.[1] Finally, FIR feedback also facilitates chopping the input integrator in an artifact-free manner. The chopping frequency can be chosen to be low ($= f_s/24$), thanks to the spectral nulls introduced by the 12-tap FIR DAC at multiples of $f_s/12$ [13], [14]. The half-clock-cycle delay of the quantizer, as well as the delay due to the 12-tap FIR in the main DAC, is compensated by a ten-tap FIR filter $F_c(z)$ placed in the direct path (through DAC$_0$). While a 12-tap compensation structure is needed to restore the NTF perfectly, the last two taps were found to be very small and could be eliminated. It turns out, as we show in Section V that the quantizer, $F_c(z)$-DAC$_0$, and the summer can be implemented in a single unit in an extremely power- and area-efficient manner using passive techniques.

As mentioned in the Introduction, one motivation to move to a single-bit CTΔΣM from the multibit design of [11] was to avoid the problems caused by DAC element mismatch in the latter. To illustrate this, consider a fourth-order CTΔΣM with a nine-level quantizer and DWA, and a thermal-noise limited SNDR of 110 dB. Like in [11], DWA was chosen as the DEM technique to address element mismatch in the feedback DAC. Simulations show that for a full-scale input, DWA can handle DAC element mismatch of $\sigma = 0.2\%$ without degrading the in-band linearity. However, DWA results in several spurious tones at low input amplitudes [15], causing a kink in the dynamic-range plot, shown in Fig. 2. The figure plots the SNDR versus input amplitude for 30 Monte Carlo runs. We see kinks in the SNDR for almost all runs. A similar effect was also seen in the measurements of [11]. The root cause of this SNDR kink is element-rotation tones that appear in-band over a range of (small) inputs, as seen from the spectrum in the inset of Fig. 2. Notice that for inputs of about −40 dBFS, DWA can degrade the SNDR by as much as 15 dB. This degradation can be problematic in some applications, such as vibration analysis and condition monitoring by vibration measurement [16], where these in-band tones due to DWA can be misinterpreted and attributed to faults in an otherwise well-functioning system. A single-bit design, on the other hand, has no such problems. The price to be paid is the lower MSA of the modulator.

Two observations are in order here. First, the kink in the DR plot would not be prominent in designs that attempt a lower resolution, as the DWA tones would be largely masked by thermal noise. Second, tones could be avoided by using higher order mismatch-shaping techniques [12]. These algorithms,

[1] Calculations show that the CTΔΣM can tolerate an rms white jitter of 1 ps, which is easily achievable with a crystal-oscillator-based clock generator.

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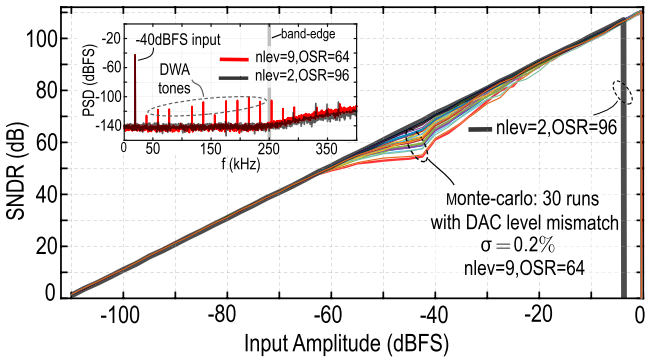

Fig. 2. Amplitude sweep of CTΔΣM with static DAC level mismatch invloving a nine-level quantizer running at an OSR of 64. The amplitude sweep for a single-bit CTΔΣM with an OSR of 96 is also shown for comparison.

however, are significantly more complex—simulations indicate that the logic needed to implement second-order noise shaping would consume upward of 10 mW in the 180-nm technology used in this work.

III. Feedback DAC Challenges

Resistive feedback DACs are the preferred choice in CTΔΣMs targeting low noise. The efficacy of switched-resistor NRZ DACs has been successfully demonstrated in several state-of-the-art high-resolution audio CTΔΣMs [5], [17], [18]. In this section, we describe various DAC alternatives that we considered and the problems that we encountered with them. Switched-resistor NRZ DACs used in most audio designs have employed reference-side switching. When attempting to achieve high resolution over a wide bandwidth like that attempted in this work, reference-side switching introduces significant distortion due to the parasitic resistance in the reference path. As described in detail in [11], distortion is caused by the data-dependent current drawn from the reference by the parasitic capacitors associated with the switches. A possible solution to these problems is to move the switches to the virtual-ground side of the integrator. As shown in [11], the virtual-ground-switched resistor NRZ DAC is a significant improvement over conventional reference-switched DACs. Even so, they have problems, as discussed below.

A. Nonidealities in Virtual-Ground-Switched Resistor NRZ DACs

Fig. 3(a) shows the simplified schematic of the input integrator of a CTΔΣM that uses a virtual-ground-switched resistive NRZ DAC. As the name suggests, the switches are moved to the virtual ground of the OTA. When the data bit D that controls a unit element is high, the *through* switch pair M1, M4 is ON. When D is low, the *cross* switch pair M2, M3 turns on. It turns out that, as described below, mismatch in the ON-resistance between the through and cross switch pairs injects data-dependent charge into the input integrator resulting in the even-harmonic distortion. Let c_p denote the parasitic capacitance at the resistor-switch junction nodes denoted by ⓐ and ⓐ.

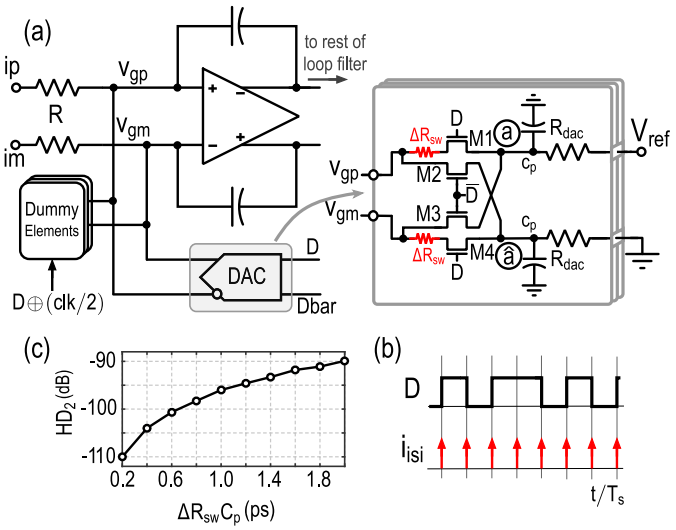

Fig. 3. Illustration of distortion due to ON-resistance mismatch. (a) schematic of virtual-ground-switched DAC. (b) Example drive bit waveforms and injected error charge. (c) HD_2 as a function of switch ON-resistance mismatch. ($R = 450\ \Omega$, and $f_s = 48$ MHz.)

In the discussion that follows, the OTA is assumed to be ideal so that the potentials v_{gp} and v_{gm} are identical. The nominal resistance of M1, M2, M3, and M4 is denoted by $R_{sw} \ll R_{dac}$. When D is low, M2 and M3 are ON. The difference between the voltages across the parasitic capacitors c_p is approximately given $\Delta V_0 = V_{ref} R_{sw}/R_{dac}$. When $D = 1$, M1 and M4 conduct. If the mismatch between the resistance of M1/M4 and that of M2/M3 is denoted by ΔR_{sw}, the new difference between the voltages across the capacitors c_p is given by $\Delta V_1 = V_{ref}(R_{sw} + \Delta R_{sw})/R_{dac}$. It thus follows that an error charge $c_p(\Delta V_0 - \Delta V_1) = c_p \Delta R_{sw}(V_{ref}/R)$ is injected by the DAC into the integrating capacitors at every data transition, as shown in Fig. 3(b). This data-dependent error is in the same direction irrespective of the direction of the transition, indicating that this is a nonlinear effect. Consequently, this error results in distortion. Fig. 3(c) shows simulation results, which indicates that $\Delta R_{sw} c_p = 1$ ps results in a HD_2 of -93 dBc. ΔR_{sw} can be reduced by using larger switches but at the cost of increased switch driver power and associated layout artifacts.

For HD_2 levels < -110 dB, $\Delta R_{sw} c_p$ must be less than 200 fs, which is quite a challenge in practice, especially with layout artifacts. Another mechanism that causes distortion is the following. Asymmetric parasitic coupling from the data lines D and $\overline{D}$ to the nodes ⓐ and ⓐ also results in error-charge injection at every data transition, resulting in distortion. While these challenges can be overcome, our experience with [11] indicated that the DAC had to be laid out *very* carefully, simulated after extracting resistance of the interconnect and iterating this procedure multiple times.

From the discussion so far, we see that data-dependent error is the root cause of distortion and is fundamental to the NRZ pulse shape. It is well known that the return-to-zero (RZ) DAC is immune to ISI since the error due to rise–fall asymmetry is data-independent [19], [20]. However, such a DAC suffers from jitter and linearity problems due to the large steps of the

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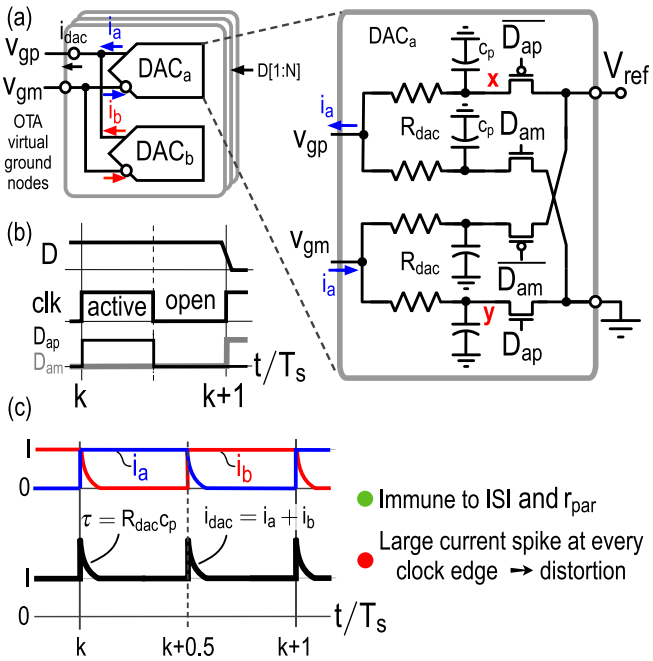

Fig. 4. (a) Schematic of reference-switched DRTO DAC. (b) Example drive waveforms for $D = 1$. (c) Example current waveforms illustrating the glitch current at $(k + 0.5)T_s$.

RZ pulse. When implemented with resistors, an RZ DAC has the additional problem of higher thermal noise since it injects noise even when the DAC current is zero. The dual return-to-open (RTO) DAC [21] attempts to address the problems associated with a resistive RZ DAC and appears to be a prime candidate to realize very linear DACs. Section III-B describes the conventional dual-RTO DAC in more detail and illustrates its problems.

B. Dual Return-to-Open DAC

Fig. 4(a) shows the schematic of a conventional reference-switched DRTO DAC [21]. v_{gp} and v_{gm} are the virtual-ground nodes of the OTA. Each DAC slice consists of two identical sub-DACs, denoted by DAC$_a$ and DAC$_b$. They operate in a complementary fashion. In the first half-clock cycle, DAC$_a$ is active, whereas DAC$_b$ is placed in the "open" state by turning off all the MOS switches. In the next half-cycle, DAC$_b$ is active, while DAC$_a$ is left "open." Fig. 4(b) shows example drive waveforms in DAC$_a$. For the time being, assume that the parasitic capacitors c_p at the switch-resistor junctions are zero. The current injected by DAC$_a$ is an RZ pulse that is active in the first half-cycle of the clock period. In a similar fashion, DAC$_b$ puts out an RZ pulse that is active in the second half-cycle of the clock period. The total current supplied by the dual-RTO DAC, therefore, is an NRZ pulse. Note that each sub-DAC does not add thermal noise when it is in an open state. Therefore, the noise and jitter sensitivity of the dual-RTO DAC are similar to that of a resistive NRZ DAC. However, thanks to the RZ pulse shape of the sub-DAC waveforms, rise–fall asymmetry causes data-independent errors. Any duty-cycle error of clk is benign as it simply alters the fraction of time for which each DAC is enabled. From the discussion above, it appears that the dual-RTO DAC is an excellent candidate for use as a feedback element in a high-resolution CTΔΣM. Unfortunately, the parasitic capacitance c_p degrades the linearity of the modulator, as described in the following.

The problem arises when a sub-DAC goes from the active state to the open state and is illustrated with the waveforms in Fig. 4(c). Assume that data-bit D is high. Ideally, DAC$_a$ should inject a perfect RZ pulse that lasts for half-clock cycle. Just before clk goes low, node x is at a potential V_{ref}, and c_p has a charge c_pV_{ref} stored on it. When clk goes low, DAC$_a$ is in the open state, and node x relaxes to a voltage $V_{ref}/2$ with a time constant $R_{dac}c_p$. In a similar fashion, the potential of node y, which was zero during the active phase, rises to $V_{ref}/2$ with a time constant $R_{dac}c_p$. Consequently, the sub-DAC current $i_a(t)$, which should ideally be an RZ pulse, has an exponentially decaying tail during the open phase, as shown in Fig. 4(c). $i_b(t)$ has a similar tail during its open phase. As a result, the current supplied by the dual-RTO DAC, $i_{dac}(t) = i_a(t) + i_b(t)$, has large spikes at every transition of the clock waveform. This glitch current, which needs to be absorbed by the OTA, degrades its linearity. A brute-force solution to this problem is to increase the current in the OTA. This, however, increases the power dissipation of the CTΔΣM. Fortunately, it turns out that the dual-RTO principle can be implemented in a power-efficient manner by moving the switches to the virtual ground of the OTA and using a technique called zapping. This leads to the zapped, virtual-ground-switched dual-RTO DAC, which is described next.

IV. Zapped Virtual-Ground-Switched Dual Return-to-Open DAC

Section III described the reference-switched DRTO DAC and the problems associated with it. We now describe the zapped virtual-ground-switched DRTO DAC as a solution to these problems.

Fig. 5 shows the basic idea behind the virtual-ground-switched DRTO DAC. v_{gp} and v_{gm} denote the virtual-ground nodes of the differential OTA. The DAC is composed of unit cells, with a unit cell comprising of two RTO DACs (DAC$_a$ and DAC$_b$), each of which is active for the half-clock cycle. They work in a complementary fashion to effectively create an NRZ DAC pulse. The call-out in Fig. 5 shows the schematic of DAC$_a$. It consists of two resistors connected to V_{ref} and ground on one side and to the OTA's virtual-ground nodes on the other. As the name suggests, the switches that control the DAC are placed on the virtual ground. DAC$_a$ is active when clk is high. During this phase, D_{ap} and D_{am} are complementary and take on values 0/1 depending on the data-bit D, while the signal zap$_a$ is low. Since v_{gp} and v_{gm} have a common-mode voltage of $(1/2)V_{ref}$, the differential current that flows into the integrator is given by $\pm V_{ref}/2R$. Thanks to switching at the virtual ground, only NMOS switches are necessary. This greatly simplifies the layout and the driving logic compared to a reference-switched RTO DAC [21]. The common-mode voltage of the virtual ground nodes is held at $(1/2)V_{ref}$ by a CMFB loop (not shown in Fig. 5).

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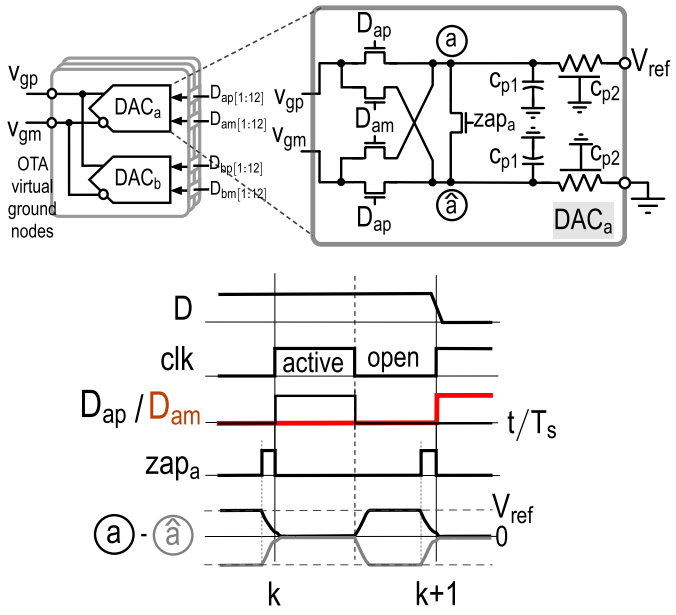

Fig. 5. Simplified schematic and timing of the virtual-ground-switched DRTO DAC.

When clk goes low, DAC_a is in its "open" phase, where D_{ap} and D_{am} are at the ground. As soon as the DAC enters this phase, nodes ⓐ and ⓐ̂ attain potentials V_{ref} and 0, respectively. Thus, the parasitic capacitors c_{p1} and c_{p2} corresponding to node ⓐ are charged to V_{ref}, while those corresponding to ⓐ̂ are charged to ground. To motivate the need for the zap switch, assume, for the time being, that it does not exist. Then, as soon as DAC_a attempts to enter the active phase from the open phase at the rising edge of clk, the parasitic charge on these capacitors would be steered into the integrating capacitors depending on the data-bit D. The resulting data-dependent spike of current needs to be absorbed by the OTA, and this causes an increased swing at the OTA's virtual-ground nodes, resulting in distortion. The zap switch in Fig. 5 avoids this problem, as described in the following.

zap_a is high for a small interval at the end of DAC_a's "open" phase and shorts' nodes ⓐ and ⓐ̂ together. This way, the potentials at these nodes attain $(1/2)V_{\text{ref}}$ at the end of the zap phase. Consequently, c_{p1} and c_{p2} do not inject charge into the integrator at the beginning of the DAC's active phase. The width of the zap phase is exaggerated in Fig. 5 for clarity—in practice, it is only a few inverter-delays wide.

Simulations, whose results are shown in Fig. 6, confirm the intuition above. Fig. 6(a) shows the waveforms of the current drawn from the OTA without and with the zap switch. It is seen that the magnitude of the current drawn is higher when the zap signal is disabled. The signal dependence of this current is apparent. The effect of zapping on the modulator's PSD is shown in Fig. 6(b). As expected, enabling the zap signal results in a distortion-free operation. The discussion above described the operation of DAC_a. DAC_b is identical to DAC_a, except that its drive waveforms are shifted by a half-clock cycle.

The noise of the DAC has a significant bearing on the SNR of the modulator. As discussed earlier, an advantage of the RTO structure (as opposed to a resistive RZ DAC) is

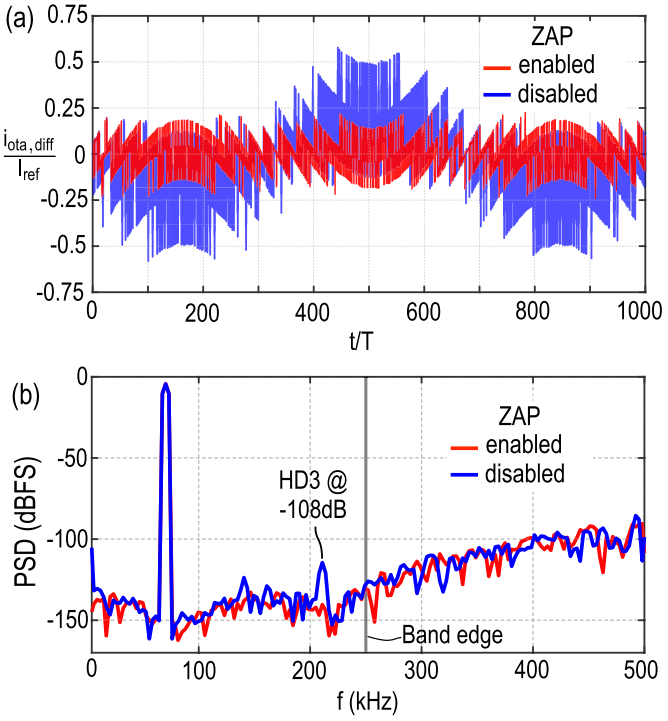

Fig. 6. (a) Differential output current drawn from the OTA with and without the zap switch. (b) Simulated output PSD depicting the linearity improvement to be had with the zap switch.

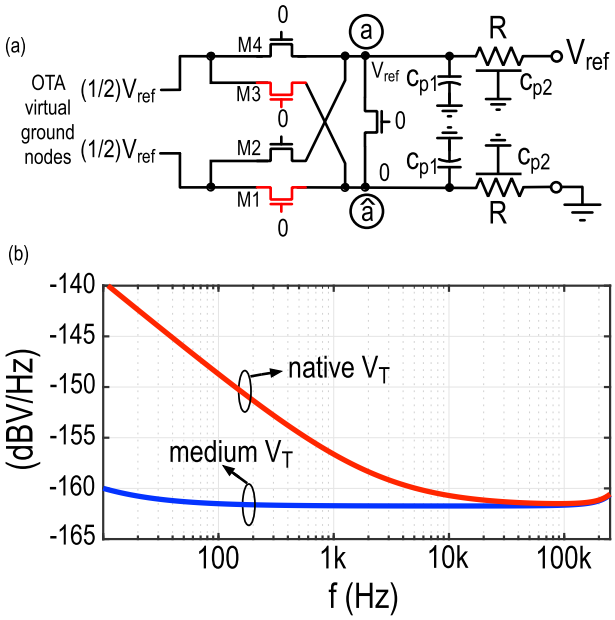

Fig. 7. (a) RTO DAC in its OFF-state. M1 and M3 inject flicker noise into the modulator. (b) Comparison of input-referred noise: using medium-V_T devices [(W/L) = 12(12/0.3)] versus native-V_T devices [(W/L) = 12(8/0.5)] for the switches. $R = 450\ \Omega$.

that it does not add thermal noise when it is open. Thus, as far as thermal noise is concerned, the noise of a dual-RTO DAC should be expected to be identical to that obtained with a resistive NRZ DAC supplying the same current. This is confirmed by analysis along the lines of [20]. The switching

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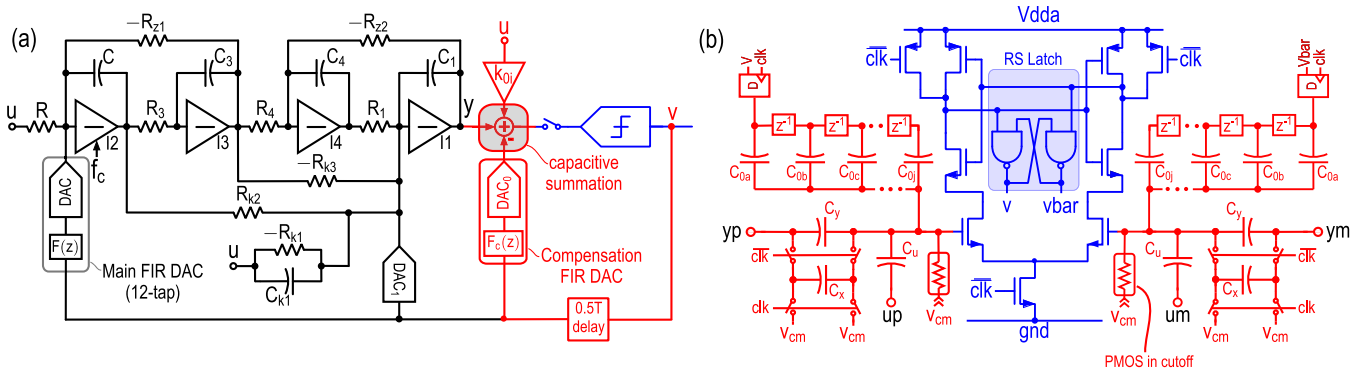

Fig. 8. (a) Simplified single-ended schematic of the modulator. (b) Quantizer and implementation of the direct path using capacitive summation.

parasitic capacitors in an RTO structure [c_{p1} and c_{p2} in Fig. 7(a)] also contribute to noise—however, analysis shows that their contributions are negligible since $Rc_{p1}, Rc_{p2} \ll T_s$.

We now describe an interesting aspect concerning the noise of RTO (and dual-RTO) DACs in their "open" state. This is applicable to all RTO DACs—reference-switched and virtual-ground-switched. This seems to have been missed in the prior literature. Fig. 7 shows the equivalent circuit of an RTO DAC in its open state. The gates of all transistors are grounded, and the potentials of ⓐ and ⓐ are V_{ref} and 0, respectively. Consider the devices M1 and M3. Their sources and gates are on the ground, and their drains are at $(1/2)V_{\text{ref}}$. They, therefore, operate in weak inversion and saturation, and inject noise into the modulator. The component of concern is their flicker noise, whose spectral density is proportional to the quiescent current flowing through them in the OFF-state.

An aspect that deserves attention is the choice of the type of MOS device used to implement the virtual-ground switches. Using native devices for the switches is attractive since smaller devices can be used. This, however, increases the flicker noise injected by these devices. Using medium-V_T devices can greatly reduce this problem at the expense of slightly bigger transistors. Simulations [see Fig. 7(b)] of input-referred noise with native-V_T and medium-V_T devices used in the DAC confirm the analysis above.

V. Circuit Design

Fig. 8(a) shows the simplified single-ended schematic of the CTΔΣM, where negative component values indicate the inversion in the fully differential version. The CIFF-B loop filter decouples the fast and precise feedback paths around the quantizer. Active-RC integrators are used to achieve low noise and high linearity. The main feedback DAC is a resistive 12-tap FIR structure that uses dual-RTO unit cells. All tap weights of the FIR DAC are identical. The first stage of the three-stage feedforward-compensated OTA used in the integrator I2 is chopped at a frequency $f_c = f_s/24$. Consequently, the dominant source of OTA flicker noise is modulated out of the signal band. Chopping, however, causes shaped quantization noise from multiples of twice f_c to fold into the signal band [5], [14]. Fortunately, the FIR DAC has nulls in the feedback DAC spectrum at multiples of $f_c/12$. This greatly reduces the amount of noise folding. Simulations using the model and methodology of [13] indicate that the folded-shaped noise due to chopping is about 12 dB lesser than the in-band quantization noise.

Integrators I1, I3, and I4 employ two-stage feedforward compensated OTA structures. The quantizer samples are on the falling edge of the clock. To give it sufficient time for regeneration, DAC_1 and the main FIR DAC are clocked using the rising edge, resulting in an excess delay of a half-clock cycle. The effect of this delay is addressed by well-known techniques [12]. DAC_1, which forms the fast path around the quantizer, should have very little excess delay. It is, therefore, implemented using a virtual-ground-switched resistive structure [11], [22], which is unaffected by the distributed capacitance of the resistor. R_{k1} and C_{k1} compensate for the low-frequency current injected by DAC_1 and consequently reduce the size of C_4 that would otherwise be needed.

This work uses a direct-path FIR DAC to compensate for the delay of the main FIR DAC. Thanks to the single-bit operation, the input feed-in path, compensation FIR DAC, and summing amplifier [as shown in red in Fig. 8(a)] can be compactly integrated with the quantizer (blue), as described in the following.

A. Quantizer and Compensation FIR DAC

Fig. 8(b) shows the simplified implementation of the colored parts of Fig. 8(a). The 1-bit quantizer is realized using a StrongArm latch, whose output is held for the rest of the clock period by the RS latch. The output of the quantizer (v) and its delayed versions (obtained using a chain of flip-flops) excite capacitors $C_{0a}, \ldots, C_{0j}$, which form the compensation FIR DAC. The loop filter output y and the input u are summed with the compensation DAC using the capacitors C_y and C_u, respectively. C_x is chosen to be about a tenth of C_y. Capacitive summation is robust as the relevant coefficients are set by capacitor ratios. It is also very compact since small capacitors can be used, which in turn reduces loading on the loop filter. The attenuation caused by capacitive summation and the parasitic input capacitance of the latch is not of much consequence since the quantizer output only depends on the sign of its input.[2] Though the main FIR DAC employs 12 taps, ideally necessitating a 12-tap compensation DAC, it turns out

[2]A potential problem is the increased regeneration time of the quantizer due to the attenuation caused by passive summation. The half-cycle delay greatly helps in this aspect.

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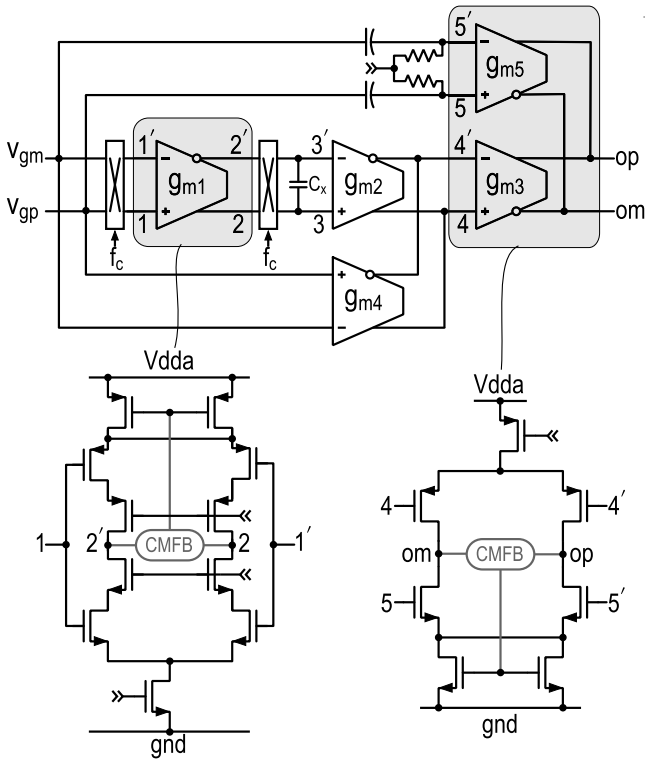

Fig. 9. Simplified schematic of the three-stage feed-forward compensated OTA. The input stage g_{m1} is chopped at $f_c = f_s/24$.

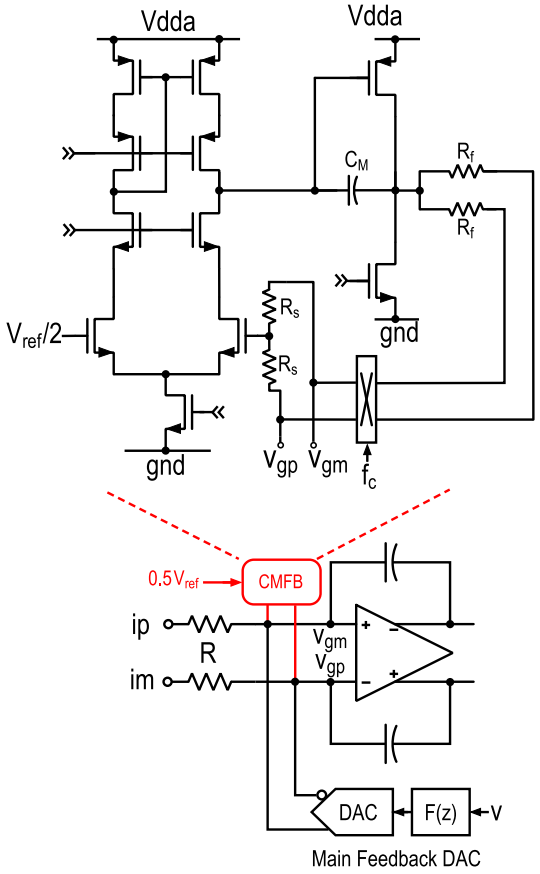

Fig. 10. Simplified schematic of the input integrator and the CMFB loop. R_s is used for CM sensing, and R_f is used for correction.

that the magnitudes of the last two taps are so small that they can be ignored.

As a result of the techniques described above, the compensation DAC and quantizer occupy very little space. This approach is fundamentally made possible due to single-bit operation; a multibit CTΔΣM would not benefit from this technique.

B. OTA Design Details

Fig. 9 shows the simplified schematic of the three-stage feed-forward compensated OTA used in the input integrator I2 [11]. The high-gain third-order path is formed by the cascade of $g_{m1} - g_{m2} - g_{m3}$, while the high-speed first-order path is realized using g_{m5}. C_x, which is deliberately added at the output of g_{m1}, improves the OTA's phase margin. The fast path through g_{m5} is ac coupled, with its input and output common-mode voltages chosen to maximize the OTA's output signal swing.

The input-referred noise of the OTA in the signal BW is largely dictated by that of the input-stage transconductor g_{m1}. For power-efficient operation, NMOS and PMOS signal paths are used to increase the transconductance for a given bias current. The input stage is chopped at $f_s/24 = 2$ MHz, thereby modulating the stage's flicker noise to frequencies outside the signal bandwidth. Cascodes are used to achieve high dc gain, which helps to suppress the flicker noise from subsequent stages. The cascode devices are considerably smaller than the input transistors. Consequently, the parasitic capacitance at nodes $2 - 2'$ is significantly smaller than what it would have been otherwise, thereby reducing chopping artifacts [13]. $g_{m2}-g_{m4}$ and $g_{m3}-g_{m5}$ stages employ current reuse to reduce power dissipation, as shown in Fig. 9.

C. Input CMFB Loop

The common-mode component of the virtual-ground nodes of the OTA used in the input integrator is regulated to 0.5 V_{ref} using an input CMFB loop. Fig. 10 shows a simplified schematic of the input integrator and the CMFB loop. Without this loop, imbalanced inputs would cause the common-mode component of v_{gm} and v_{gp} to contain a portion of the input. This, in turn, would modulate the virtual-ground switches in a signal-dependent manner and result in distortion [11]. Adopted from [23], the common-mode voltage at the virtual ground is sensed using a pair of resistors R_s, each of which is $\approx 50R$. It is compared to $(1/2)V_{\text{ref}}$ using a two-stage Miller-compensated error amplifier, whose output drives a pair of resistors R_f. These resistors, connected to the virtual-ground nodes v_{gp} and v_{gm} through a chopper, pull the common-mode potential of the virtual-ground nodes in the appropriate direction. Resistive correction (as opposed to using transistors acting as current sources, as in [11]) is advantageous in the sense that there is no flicker noise associated with the resistors R_f. The reason for chopping the resistors is the following. Without the chopper, the flicker noise at the output of the error amplifier can cause a

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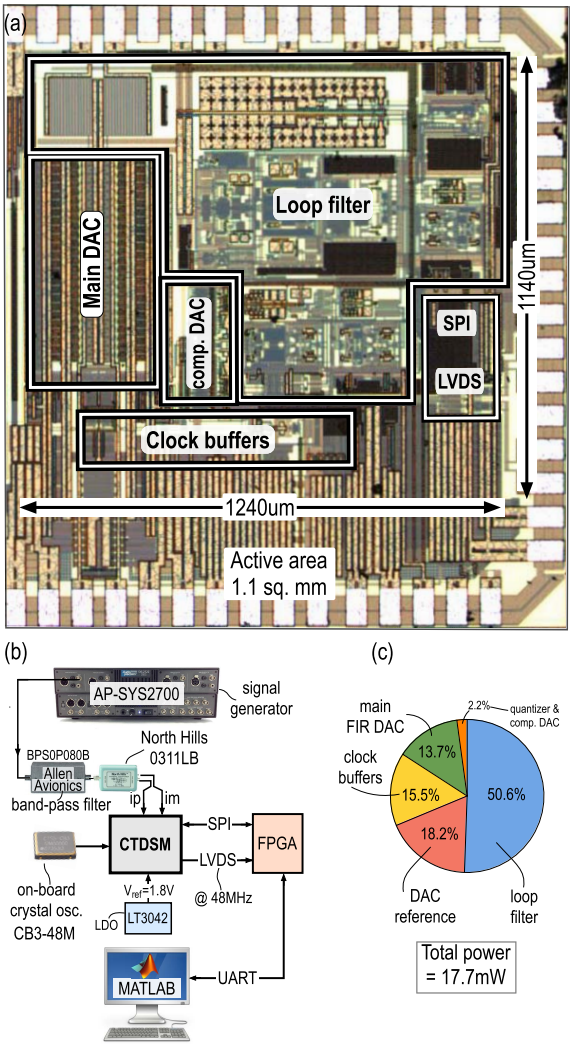

Fig. 11. (a) Die micrograph. (b) Test setup. (c) Pie chart depicting the power distribution in the prototype chip.

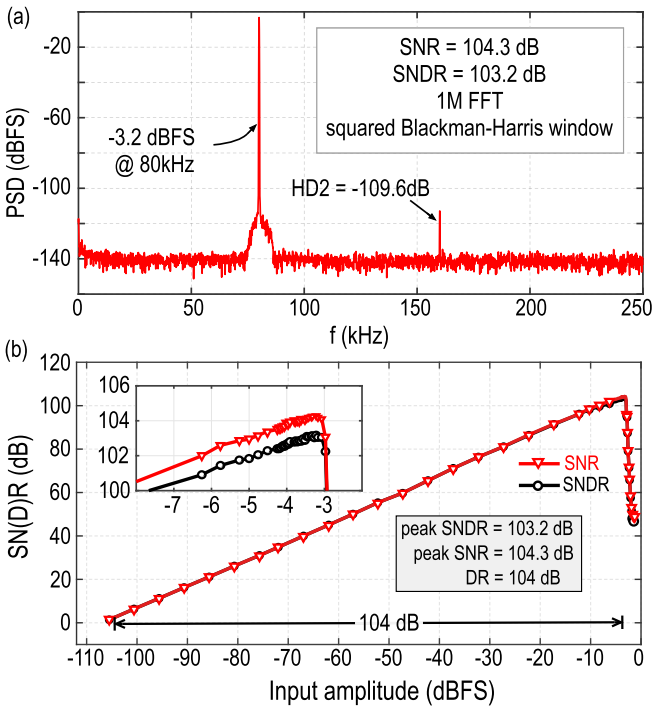

Fig. 12. (a) Measured in-band PSD with a −3.4-dBFS input at 80 kHz. (b) Measured SN(D)R as a function of input amplitude for an 80-kHz input.

differential current to be injected into the virtual ground nodes if the resistors R_f are mismatched. Chopping modulates this potential source of $1/f$ noise to frequencies outside the signal band.

VI. Measurement Results

The prototype chip was fabricated in a 180-nm CMOS process. Fig. 11(a) shows the die photograph. The CTΔΣM occupies an active area of 1.1 mm^2. Fig. 11(b) shows the measurement setup. The sine-wave input from an Audio Precision (AP-SYS2700) signal generator is filtered by a bandpass filter (Allen Avionics BPS0P080B) and converted into a differential form using a balun (North Hills 0311LB). The output of the balun drives the CTΔΣM input. An onboard low phase-noise crystal oscillator (CB3LV-48M) serves as the 48-MHz master clock. The modulator's reference voltage is supplied by a low dropout regulator (LT3042). The high-speed single-bit CTΔΣM output is brought out of the chip using an LVDS buffer, captured on an FPGA, and processed on a workstation.

The CTΔΣM consumes a total power of 17.7 mW. The distribution among various blocks is shown in Fig. 11(c). Almost half the total power is dissipated in the loop filter. 75% of this is consumed by the input integrator and is needed to achieve the desired noise and linearity. The DAC references and the clock generation and distribution circuitry consume 18.2% and 15.5% of the modulator's power. 13.7% of power is expended on the 12-tap FIR DAC (including the dual return to open circuitry). Thanks to single-bit operation and the merged compensation DAC, the quantizer and compensation DAC together consume just 2.2% of the CTΔΣM 's power.

Fig. 12(a) shows the measured output PSD for a −3.2-dBFS input at 80 kHz. A 1M-point squared Blackman–Harris window was used to estimate the power spectral density. The achieved peak SNDR and SNR are 103.2 and 104.3 dB, respectively. The measured HD_2 is −109.6 dB, while third-harmonic distortion cannot be observed in the PSD. The source of HD_2 could not be ascertained—it is suspected to be package feedthru. Fig. 12(b) shows the measured SN(D)R as a function of input amplitude for an input tone at 80 kHz. The achieved dynamic range (DR) is about 104 dB. Thanks to the single-bit quantizer, the DR plot is linear with respect to input amplitude. This is in contrast to the design using a multi-bit quantizer [11], where DWA used to shape DAC mismatch caused a kink in the DR plot at low input amplitudes.

To demonstrate the benefits of using the zap phase in the dual-RTO DAC, the prototype incorporated a provision to disable zapping. Fig. 13(a) compares the measured output PSD with zapping turned on and off. As expected, distortion increases when zapping is turned off. Consequently, the SNDR is limited to 95 dB. Fig. 13(b) demonstrates the efficacy of input CMFB circuit. When it is turned off, the imbalance in the differential input degrades HD_2 by about 9 dB to −100.8 dB.

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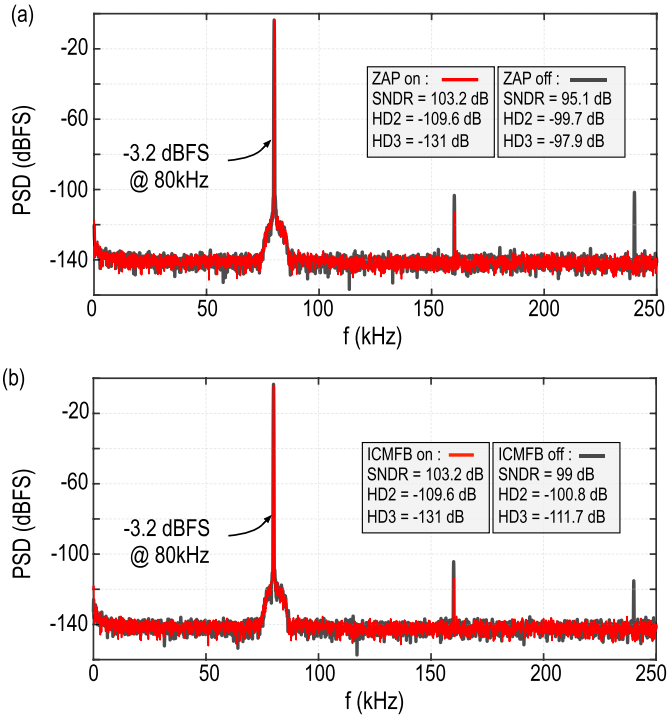

Fig. 13. Measured PSDs for −3.4-dBFS input demonstrating (a) zap ON versus zap OFF and (b) input CMFB enabled/disabled.

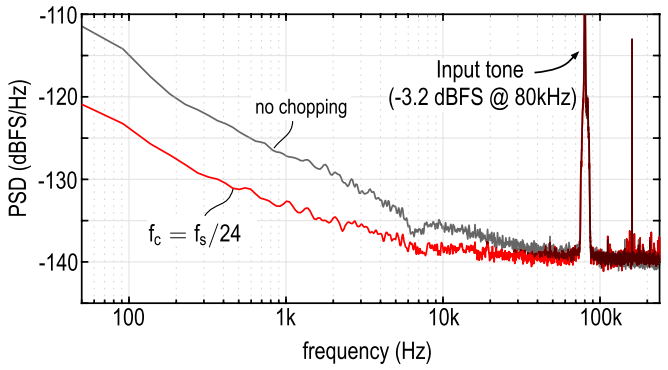

Fig. 14. Comparison of low-frequency power spectral density with chopping off versus chopping on, where $f_c = f_s/24$ and the input tone is at 80 kHz.

A. Flicker Noise and Alias Rejection

Fig. 14 demonstrates the effect of chopping on the in-band power spectral density. With chopping enabled (with $f_c = f_s/24$), the $1/f$ noise spectral density is observed to be only about 12 dB lower compared to the one without chopping. Simulations without chopping show a flicker-noise corner that is five times higher than what is measured, indicating that the models are overly pessimistic. This explains the somewhat low $1/f$ noise corner without chopping. Chopping practically eliminates the flicker noise of the OTA, but that due to the RTO DAC cannot be addressed by chopping. As discussed in Section IV, the $1/f$ noise of the open switches (implemented using native V_T devices) in the DAC results in residual noise. This can be easily addressed in a revision by using devices with a higher threshold voltage. This fix was confirmed using simulations.

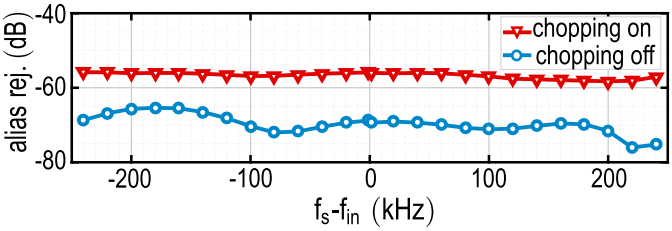

Fig. 15. Measured alias rejection for input frequencies around $f_s = 48$ MHz and a comparison between chopping on *versus* chopping off.

TABLE I
PERFORMANCE COMPARISON WITH STATE OF THE ART

	Node (nm)	Area (sq. mm)	Power (mW)	BW (kHz)	DR (dB)	Peak SNR (dB)	Peak SNDR (dB)	NSD[1] (dBFS /Hz)	FoM[2] (dB)
[5]	180	1.3	0.28	24	103.6	99.3	98.5	-143	177.8
[4]	160	0.27	0.618	20	108.5	108.1	106.4	-149	181.5
[7]	65	0.28	0.134	24	103.5	101	99.4	-143	181.9
[10]	65	0.39	0.139	24	104.8	102	100.9	-145	183.3
[6]	28	0.02	1.13	24	100.6	100.6	98.5	-142	171.8
[9]	28	0.07	1.16	24	104.4	100.6	100.6	-144	183.7
[1]	180	0.99	21	600	97.3	97.3	85	-143	159.5
[11]	180	2.85	24	250	107.5	108.5	105.3	-159	175.5
This work	**180**	**1.1**	**17.7**	**250**	**104**	**104.3**	**103.2**	**-157**	**174.7**

[1] Noise + Distortion Spectral Density: $-(\text{SNDR}_{\max} + 10\log(\text{BW}))$
[2] Schreier FoM : $\text{SNDR}_{\max} + 10\log(\text{BW/Power})$

Fig. 15 shows the measured alias rejection of the CTΔΣM. For these measurements, the modulator was excited with −20-dBFS tones in the frequency range 48 MHz ± 250 kHz. With chopping disabled, the alias rejection is about −70 dB, in line with circuit simulations. If the input integrator was ideal, calculations show that the rejection should be about −90 dB. This degradation from the ideal value turns out to be due to the nonlinearity of the OTA used in the input integrator [24]. When chopping is enabled, the switching parasitic capacitance of the chopper switches essentially samples the virtual-ground voltage [14] and limits the alias rejection to −56 dB.

B. Comparison With Prior Art

Table I summarizes the performance of our chip and compares it with that of state-of-the-art high-resolution CTΔΣMs. Barring [1] and [13], prior art designs have bandwidths that are restricted to the audio range. We see that the single-bit design presented in this work achieves a power efficiency which is close to that achieved by the multi-bit converter in [11], while reducing active area by a factor of 2.6.

It is interesting to compare the performance of the multibit design of [11] with that of this design and take stock of how the power and area of individual blocks compare in the single-

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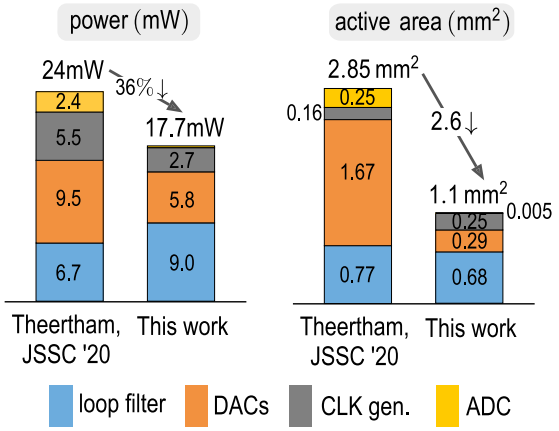

Fig. 16. Power and area comparison of the multibit CTΔΣM in [11] and this work. The DAC power includes power drawn from references by the FIR DFFs and the dual-RTO circuitry.

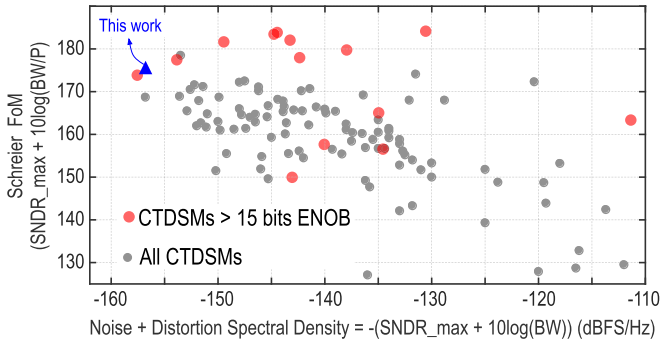

Fig. 17. Performance comparison on the Schreier FoM-NDSD plot.

and multi-bit cases. Fig. 16 shows this comparison. The single-bit design dissipates more power in the loop filter. This makes sense since it operates with larger step size and processes higher frequency signals (due to the increased clock rate). However, significant savings are achieved in the DAC (due to reduced switching power), quantizer, and clock generator even though the clock rate is 1.5× higher than that used in the multibit CTΔΣM.

Comparing the areas occupied by the modulators, we see that the compensation DAC and quantizer of the single-bit design are significantly smaller than those in their multibit cousin. A word of caution is in order here; the tolerance of the two designs to clock jitter is different, with the single-bit modulator being significantly more sensitive. Thanks to the crystal-oscillator clock source, noise due to clock jitter does not degrade the performance of our design.

Fig. 17 compares the performance of this work with all CTΔΣMs (published at International Solid State Circuits Conference (ISSCC) and the Symposium on VLSI Circuits) on the FoM-NDSD plot. We see that the design presented in this work achieves a low in-band NDSD and does so with a high Schreier FoM. Its performance is comparable to that of the multibit design of [11].

VII. Conclusion

State-of-the-art converters that achieve low NDSDs have used multibit techniques. We investigated the prospects of using single-bit operation and FIR feedback to achieve a very low in-band noise + distortion spectral density in an area and power-efficient manner. We introduced the zapped virtual-ground-switched DRTO DAC, which enables the realization of structures without nonlinear data-dependent errors. The single-bit operation also enables the realization of the compensation FIR DAC in a compact and power-efficient manner. The efficacy of our techniques is demonstrated by measurements from a prototype chip designed and fabricated in a 180-nm CMOS process. The converter achieves a peak SNDR of 103.2 dB in a 250-kHz BW while dissipating 17.7 mW from a 1.8-V supply. The active area occupied by the design is 1.1 mm^2, which is about 2.6× lower than the similarly performing multibit converter of [11]. From these results, it appears that single-bit operation combined with FIR feedback and a zapped, virtual-ground-switched dual-RTO DAC is a compelling design choice to realize high-resolution CTΔΣMs with low in-band noise spectral density.

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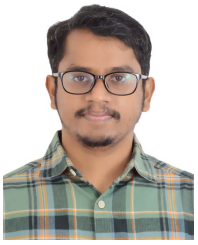

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