A 16-Bit 5 GS/s DAC With Redundant-MSB-Based Digital Pre-Distortion Achieving SFDR >61 dBc Up to 2.4 GHz in 40-nm CMOS

Xing Li, Lei Zhou, Xuan Guo, Hanbo Jia, Danyu Wu, Jin Wu, and Xinyu Liu

***Abstract*—This brief presents a 16-bit 5 GS/s current-steering digital-to-analog converter (DAC) with a redundant-MSB based digital pre-distortion (RMDPD) technique. 1-bit MSB is added during decoding to accommodate digital compensation of element mismatch errors, enhancing both the low-frequency and high-frequency linearity without penalty on the noise floor. In addition, an improved data/dummy-data scheme, which incorporates the dummy-data generation logic into the 2:1 multiplexer (MUX) with half-rate clock, is used to mitigate the code-dependent supply ripples and induced retiming errors. The implemented DAC achieves > 61 dBc spurious-free dynamic range (SFDR) and < −72 dBc third-order intermodulation distortion (IM3) for output frequencies up to Nyquist. The DAC core occupies 0.42 mm^2 active area and dissipates about 360 mW at 1.8V/1.0V/-1.8V supply.**

***Index Terms*—Digital-to-analog converter (DAC), current-steering, mismatch, digital pre-distortion (DPD), dummy-data.**

I. Introduction

HIGH-SPEED high-resolution current-steering digital- to-analog converters (DACs) are increasingly demanded for advanced wireline or wireless communication systems [1], [2], [3], [4], and a high spectral purity over a wide bandwidth is critical. The major error mechanisms of DACs are generally attributed to amplitude errors and timing errors [5], [6], with the main common source being element mismatches, including current sources, switches, latches, routing wires, etc. Finite output impedance and other code-dependent distortion are also partially responsible for the linearity degradation at high frequencies.

A conventional solution for matching dilemma is to increase the size of transistors, which becomes unacceptable for a high-speed high-resolution DAC due to area and parasitic issues. In this case, a few techniques have been proposed to reduce the negative impact of mismatch errors while holding the array scale. Various analog calibration techniques are introduced to correct the current errors, while the common problem is the additional circuit complexity [4], [6]. Dynamic element matching (DEM) techniques transform the harmonics into white noise by randomizing the mismatch patterns, at the expense of increased noise floor [6], [7], [8], [9], [10], [11]. In this brief, a calibration technique with less analog overhead, called redundant-MSB based digital pre-distortion (RMDPD), is presented. Without any additional fine current cells dedicated to calibration, we utilize all intrinsic LSBs instead, and 1-bit redundant MSB is added to provide extra quantization range.

The code-dependent distortion is another problem that limits the dynamic performance, and the supply fluctuation that occurs in the final retiming drivers is a significant part of it. Typically, a dummy-data path that works alternately with the main signal path, can be designed to mitigate above effect [2]. In this brief, an improved dummy path scheme is proposed to address the generation logic in half-rate clock domain, which is compatible with the multiplexers (MUXs) in high-speed DACs.

In this brief, we report a 16-bit 5 GS/s DAC fabricated in 40-nm CMOS process with the techniques described above. The remainder is organized as follows. Section II presents the overall architecture. Section III discusses details of circuit implementation. Section IV provides the measurement results. Finally, Section V concludes the work.

II. DAC Architecture

Fig. 1 provides a block diagram of the proposed 16-bit DAC. The input data is segmented into 5-bit thermometer codes and 11-bit binary codes. The upper 5 bits are converted to 31 MSBs with 1-bit redundant via a DEM decoder, while the randomization is also performed [10]. The lower 11 bits pass through the delay equalizer to align the bit streams. This set of segmented codes are corrected in the following RMDPD block.

After the pre-distortion, 16 lanes of data are multiplexed into a 5 GS/s bit-stream through four-stage 2:1 MUX circuits. In the final stage, a dummy path is introduced, hence while the real data triggers the final retiming flip-flops (FRFFs), the dummy data enters the replicas. An internal low-dropout regulator (LDO) is exploited to provide a clean supply for FRFFs. Finally, the tail current cells are switched to the

Manuscript received 28 February 2024; revised 29 May 2024; accepted 10 July 2024. Date of publication 15 July 2024; date of current version 26 November 2024. This work was supported by the Strategic Priority Research Program of Chinese Academy of Sciences under Grant XDC07020400. This brief was recommended by Associate Editor Y. B. N. Kumar *(Corresponding authors: Lei Zhou; Xinyu Liu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2024.3427767.

Digital Object Identifier 10.1109/TCSII.2024.3427767

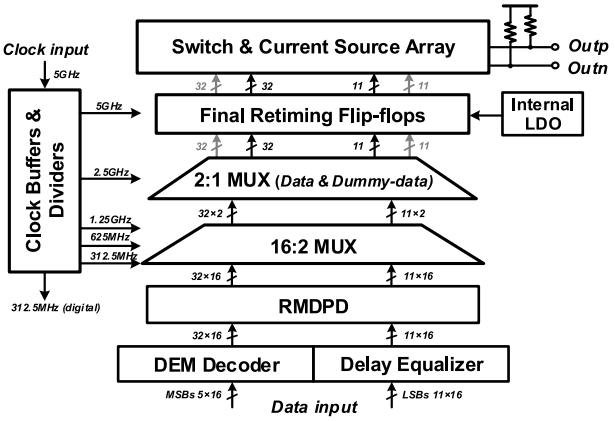


Fig. 1. Block diagram of the proposed DAC.

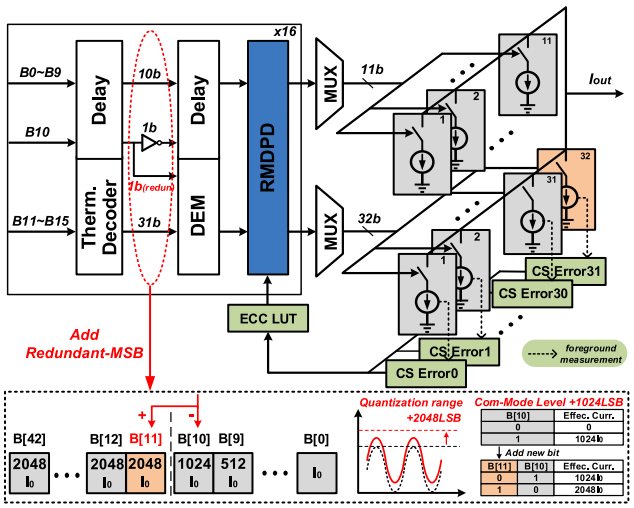


Fig. 2. Simplified DAC diagram using RMDPD technique.

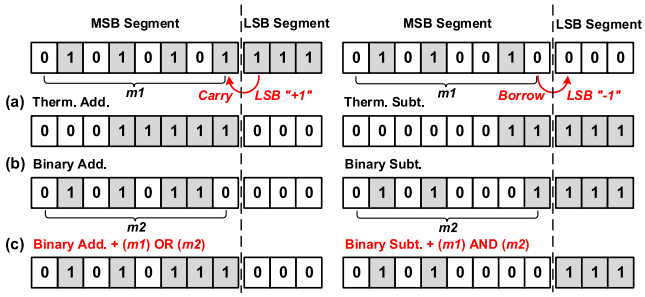


Fig. 3. Calculation examples when thermometer-codes receive a carry or borrow, following (a) the thermometer rule, (b) the binary rule, and (c) the proposed rule.

differential output nodes, and converted into a voltage signal through the terminal resistors.

III. Implementation Details

A. Proposed Redundant-MSB Based Digital Pre-Distortion

In a current-steering DAC, the digital calibration techniques can be classified broadly into two categories. One is essentially the switching sequence optimization techniques, such as dynamic-mismatch mapping (DMM) [5] and sort- and-combine (SC) technique [12], while the common operating criterion is to use the latter cell to offset the mismatch error of the previous cell to the maximum extent. The other type is DPD techniques, which make actual compensation instead. One of the strengths of DPD is that they are always used in conjunction with DEM, leading to a further improved performance with a lower noise floor.

Several DPD schemes have been reported in previous works [13], [14], [15], [16]. One redundant LSB is used for error correction as described in [13], achieving significant linearity improvement. Meanwhile, an extra MSB bit is also introduced for DEM. References [14], [15] extend the DPD concept to a hybrid architecture, without adding any extra current cells since the oversampled LSB path provides additional processing headroom. Reference [16] completely utilizes the original current array for calibration, but makes the overflow intractable at input word boundary (i.e., at peaks and troughs of a full-scale sinusoidal signal).

The basic idea of the proposed RMDPD technique is to treat the whole LSB segment as an ideal calibration DAC like [16], and one redundant-MSB is added to expand the quantization range, handling the possible overflow after the introduction of an error code. When the RMDPD is not enabled, the polarity of the highest LSB is inverted, and the newly inserted MSB bit takes over its original state, thus ensuring a constant input word and output swing, at the only cost of an upward shift in the common-mode level, as shown in Fig. 2. Since the thermometer decoding generates an odd number of MSB, many existing DEM and layout techniques [7], [8], [10], [11], [17] introduce 1-bit MSB as dummy. Herein, we utilize it to perform error calibration simultaneously with a minimum additional area introduced.

Although the proposed technique better combines DPD with traditional DEM, a problem arises here. In the case of pre-enabled DEM and an overflow occurs, the calculation on the thermometer codes (a carry or borrow) will rearrange the MSBs as their counting is always from low to high, as one example is shown in Fig. 3(a). Moreover, since the extracted error-correction-code (ECC) are dedicated for the originally opened MSBs, both DPD and DEM lose function.

To resolve this issue, a concise algorithm is implemented in our RMDPD. The input word, containing MSB and LSB, is treated as a whole: thermometer-binary-codes (TBC). It first performs addition and subtraction following the conventional binary calculation rules, and then completes a MSB correction logic by two basic logic gates, as shown in Fig. 3(c). This is a lower-cost approach compared to the thermometer-code-adder proposed in [16].

Fig. 4 shows the logic diagram of the proposed RMDPD. We query the look-up-table (LUT) first according to the logic "1" of the input MSBs, and the total correction-code Ecc_{total} is thus acquired. The digitally addition can be explained as:

$$TBC_{bin} = \{MSB_{in}, LSB_{in}\} + \sum_{k=0}^{31} H_k \cdot Ecc_k = TBC_{in} + Ecc_{total} \tag{1}$$

where TBC_{bin} is the sum of a binary type, H_k is the selection coefficient according to the value of input MSB ($H_k = 0, 1$).

The MSB correction logic is applied to the upper MSB segment, while the LSB segment is exported directly. There

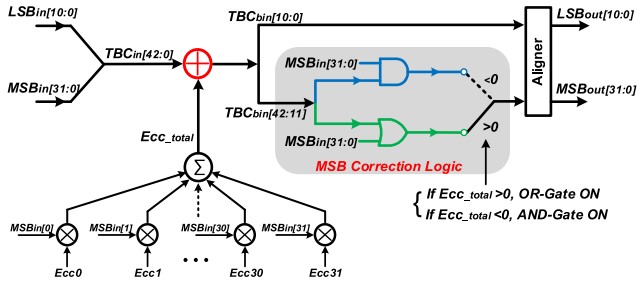


Fig. 4. Logic implementation of the proposed RMDPD technique.

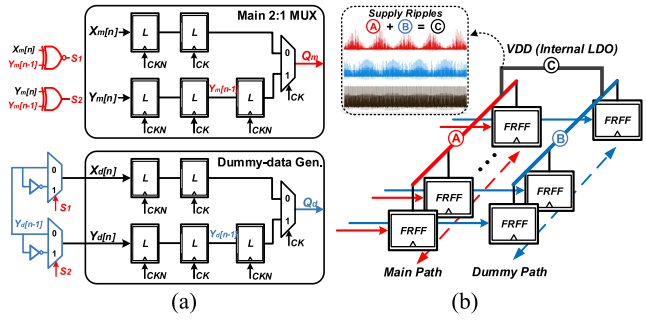


Fig. 5. (a) Implementation of dummy-data generation logic with conventional 2-1 MUX. (b) Supply scheme of the FRFF block.

are two optional paths, as illustrated in Fig. 4, and only one logic gate is opened at a time. When the Ecc_{total} is positive, performing the OR operation between the correctable MSBs and the original input MSBs, then the correct addition result is obtained regardless of whether a carry is generated. Similar AND operation is achieved for a possible borrow in the case of negative Ecc_{total}. The output MSB can be expressed as

$$MSB_{out}[31:0] = \begin{cases} TBC_{bin}[42:11] \,|MSB_{in}[31:0], & Ecc_{total} > 0 \\ TBC_{bin}[42:11] \& MSB_{in}[31:0], & Ecc_{total} < 0 \end{cases} \tag{2}$$

The constraint of this technique is the residual 1-bit MSB error in some special cases (introduced by a carry or borrow), but since it is small compared to the initial error of all MSBs, the linearity is sufficient to be improved significantly.

B. Dummy-Data Path Design

The data serialized by four-stage MUXs is synchronized by the FRFFs before being fed into the current switches. The imprecise retiming of FRFF, which results the switching time deviation, can usually be attributed to the code-dependent supply ripples.

Some effective solutions include dedicated LDO, random shuffling [13], separate decoupling [2], and dummy triggering [2], [3], [18]. As the sampling rate increases, the dummy-data generation may be constrained by the speed of digital standard cells.

Fig. 5(a) depicts a dummy-data generation scheme operating in the half-rate clock domain. Assuming the two inputs of the 2-1 MUX in the main path are $X_m[n]$, $Y_m[n]$, while dummy data are expressed as $X_d[n]$ and $Y_d[n]$. $Y_m[n\text{-}1]$ is the last word before one clock cycle. According to simple XNOR and XOR logic, two medium signals S_1 and S_2 are generated as

$$\begin{cases} S_1 = Y_m[n-1] \cdot X_m[n] + \overline{Y_m[n-1]} \cdot \overline{X_m[n]} \\ S_2 = Y_m[n-1] \cdot \overline{Y_m[n]} + \overline{Y_m[n-1]} \cdot Y_m[n] \end{cases} \tag{3}$$

In the 2-1 MUX replica of dummy path, S_1 and S_2 are used to control the selector that produces its inputs. The selectors are set up to resemble the XOR logic as

$$\begin{cases} X_d[n] = S_1 \cdot \overline{Y_d[n-1]} + \overline{S_1} \cdot Y_d[n-1] \\ Y_d[n] = S_2 \cdot \overline{Y_d[n-1]} + \overline{S_2} \cdot Y_d[n-1] \end{cases} \tag{4}$$

In the final output data streams, when $X_m[n] = Y_m[n]$, $X_d[n]$ is opposite to $Y_d[n]$; but when a transition occurs from $X_m[n]$ to $Y_m[n]$, $Y_d[n]$ coincides with $X_d[n]$, thus a complementary logic is built between the real data and dummy data.

Fig. 5(b) shows the power sharing scheme of the FRFF block and the simulation results of the supply ripples. Since the switching activity happened continuously from the view of supply, the code correlation of ripples is effectively eliminated. The power consumption introduced by the dummy design is less than 20mW, of which about 5mW comes from the dummy-data generation logic. The power consumed by the dummy-data path (FRFFs) varies with the signal frequency, but the sum with the power of main-data path remains stable. It occupies about 180 um ×20 um of silicon area.

C. Current-Steering Cells

Fig. 6 shows a typical current-steering cell structure with an NMOS tail current source. In the LSB part, the magnitude of current is changed by scaling the device size, and parallel (upper 7 bits) and series (lower 4 bits) transistors are mixed to reduce the total dimension. Both the tail current source (M0) and switch pair (M3, M4) employ cascodes (M1, M2, M5, and M6) to enhance output impedance and provide isolation.

A careful layout arrangement of the current cell array can effectively reduce the system nonlinearity upon the calibration technique. The MSB current sources are arranged in a double centroid symmetrical scheme, the LSBs are evenly distributed on both sides, and a large quantity of dummy transistors are located on the periphery. Note that the current source array is independent of the switch and cascode arrays to keep its compact configuration. In particular, the switch array is placed above the output cascodes to be close to the FRFF array, minimizing the parasitic capacitance and timing skew in the key signal path. Meanwhile, the upper cascode of tail current source are moved up together, given that the parasitic effect of the common source nodes also have a bad influence.

IV. Measurement Results

Fig. 7 shows the micrograph and the power breakdown of the test chip. The total power consumption is 360 mW, of which 280 mW is consumed by analog (current cells: 90mW, MUX and FRFFs: 56 mW, clock: 88 mW, references and LDOs: 46 mW), and 80 mW is consumed by digital circuits (excluding SerDes logics). The DAC delivers 25mA full-scale output current, and is terminated with a differential 50 Ohm on-chip resistor. The prototype is packaged in the QFN88.

For the measurement setup, all digital inputs come from DDS in FPGA, while the clock is produced by a signal

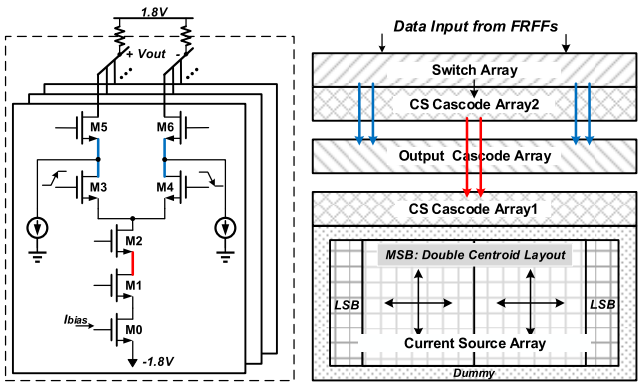
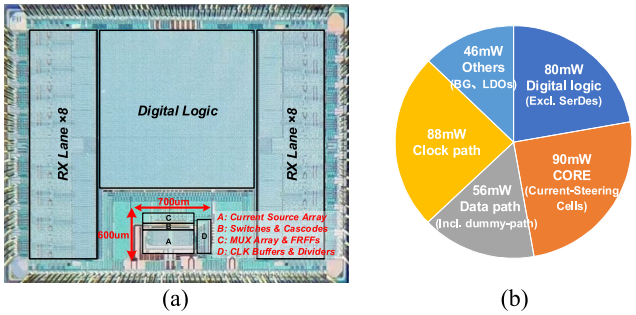
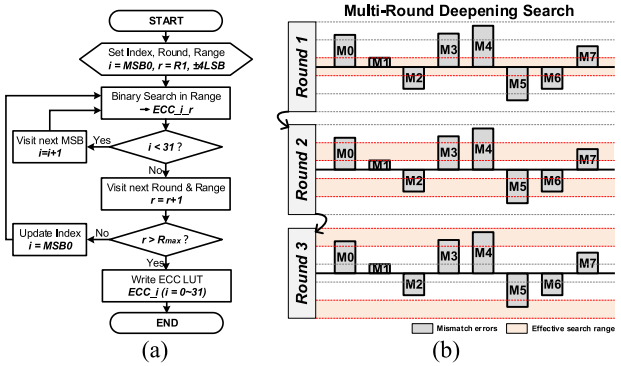


Fig. 6. Layout strategy for the current cells.



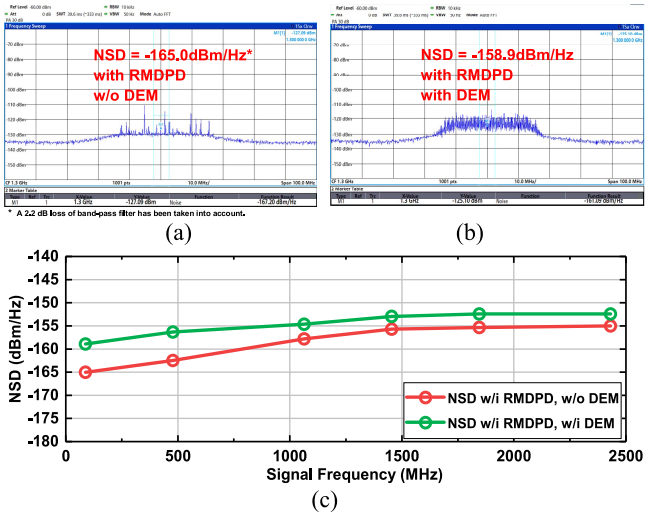
(a) (b)

Fig. 7. (a) Chip micrograph. (b) Power breakdown.



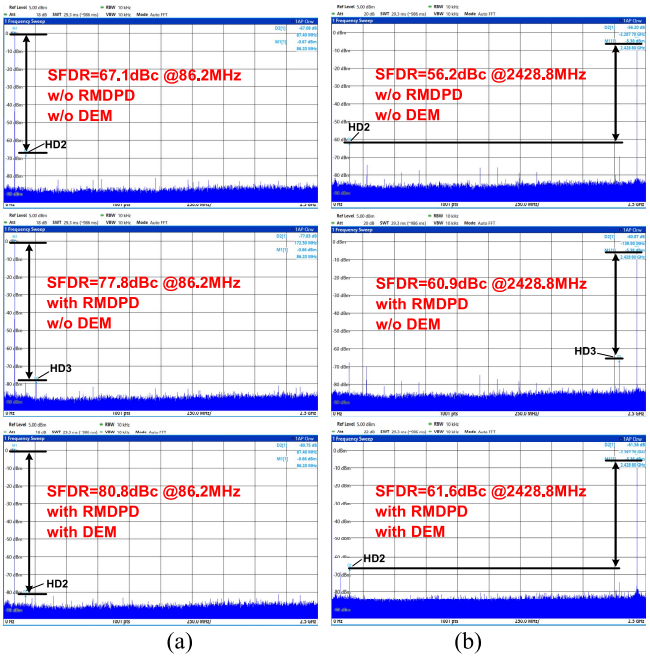
(a) (b)

Fig. 8. Error-correction-code search strategy: (a) Procedure flowchart, (b) Diagram of multi-round deepening search.



(a) (b) (c)

Fig. 9. Measured NSD at F_{out}=87.0 MHz with (a) DEM off, (b) DEM on. (c) NSD versus output frequency.



(a) (b)

Fig. 10. Measured SFDR using RMDPD and DEM with (a) F_{out}=86.2 MHz, (b) F_{out}=2428.8 MHz.

generator with 5GHz. An on-board balun is used for the single -to-differential conversion of clock input, and an off-board balun is used in the output before a spectrum analyzer.

The mismatch error used for DPD are measured as a combined error in the frequency domain. With a typical single tone input, the optimal ECC with minimum spur energy is searched in a finite code space (such as 6-bit, providing a correction range of ±32 LSB), and recorded into the LUT. In this way, the error of each MSB is quantized into a correction code for digitally subtracted from the original input codes.

The calibration procedure is executed one-time, and the search strategy is shown in Fig. 8. The binary search algorithm is first applied in sweeping one MSB, and this process should be repeated for all MSBs one by one. Considering the mutual influence as they are all switching, a multi-round deepening search scheme is proposed, which is based on the idea of breadth-first search algorithm. In each round, the search in one MSB ends after traversing only a limited range, and then starts the next MSB. It visits all MSB branches at current round before moving on to the next round. Therefore, we avoid searching too deep when considering the first few MSBs, which might make convergence difficult.

Fig. 9 shows the measured noise spectral density (NSD) with RMDPD enabled. A band-pass filter with 2.2dB loss is used to knock down the signal energy and isolate a section of the noise floor, while the internal preamp of the spectrum analyzer is set to 30dB. The noise floor reaches to −165dBm/Hz with a full swing 87 MHz sine wave, almost independent of DPD. The NSD measurement versus signal frequency shows in-band noise < −155dBm/Hz without DEM and < −152dBm/Hz with DEM.

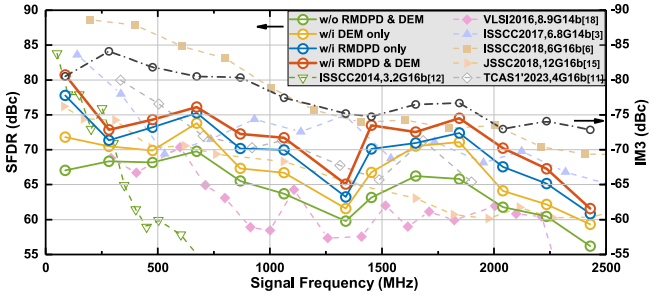


Fig. 11. Measured SFDR with and without RMDPD/DEM, and comparation with state-of-the-art high-speed high-resolution DACs, and measured IM3 versus signal frequency.

TABLE I
COMPARISON OF HIGH-SPEED HIGH-RESOLUTION DACS

	This work	[12]	[3]	[6]	[15]	[11]	[19]
Process(nm)	**40**	65	16	16	65	65	7
Sampling Rate(GS/s)	**5**	3.2	6.8	6	12	4	8
Resolution (bit)	**16**	16	14	16	16	16	14
CAL/DEM Technique	**DPD+ DEM**	3D-SC	N/A	CAL+ DEM	DPD+ DEM	DWA	CAL+ DEM
Supply(V)	**1.8/1.0/ -1.8**	1.2/3.3	N/A	1.0/3.0	1.0/2.5	1.0/2.5	1.8/1.2 /0.75/-0.3
Full Scale (mA)	**25**	20	20	40	16	16	20
Power(mW)	**360**	240	330	350	250	849	337
Area(mm^2)	**0.42**	N/A	0.855	0.52	0.1	0.85	0.5
$SFDR_{best}$ (dBc)	**80.8**	83	84	88	76	80	80
$SFDR_{worst}$ (dBc)	**61.6**	54 @700M	63	67	52	65	67
NSD (dBm/Hz)	**-165 @87M**	-168	-160 @5.2G	-165 @250M	-170 @1M	-146 @1G	-172 @1.6G
FoM (10^{16}Hz/W)	**12.8**	2.9	31.8	72.7	8.3	5.6	36.6

Fig. 10 shows the measured spectrum of the achieved DAC sampled at 5 GS/s. With the RMDPD, the dominant harmonic can be significantly suppressed and the SFDR is improved by more than 10dB at a low frequency. The DEM technique is capable of further purify the spectrum. With a combination of the two methods, the measured SFDR with output signal frequency at 86 MHz and 2429 MHz are 80.8dBc and 61.6dBc, respectively. In the two-tone test, the measured IM3 with a 10 MHz spacing maintains below −80dBc up to 870MHz, and below −72dBc up to 2.4GHz, as plotted in Fig. 11.

Fig. 11 also shows the SFDR performance measured in different modes, with comparison to the state-of-the-art high-speed high-resolution CMOS DACs. Table I summarizes these works with more details. With a similar power consumption, this brief obtains good SFDR and NSD performance in 40-nm CMOS process. The figure of merit (FoM) is defined as:

$$FoM = 2^{\frac{SFDR_{best}-1.76}{6.02}} \times 2^{\frac{SFDR_{worst}-1.76}{6.02}} \times f_s/(P_{DAC} - P_{load}) \quad (5)$$

V. CONCLUSION

In this brief, a 16-bit 5 GS/s current-steering CMOS DAC has been presented, achieving > 61dBc SFDR and < −72dBc IM3 up to 2.4GHz. A calibration technique named RMDPD is proposed and verified, which can process the mismatch errors by adding one redundant-MSB and operating with a low overhead algorithm. A dummy-data scheme with a half-rate generation logic is applied, which is conducive to expand the sampling rate. By adopting the proposed techniques, the measurement results show a 5-13 dB SFDR improvement across the whole Nyquist band.

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