A Time-Interleaved Multimode $\Delta\Sigma$ RF-DAC for Direct Digital-to-RF Synthesis

Jamin J. McCue, *Member, IEEE*, Brian Dupaix, *Member, IEEE*, Lucas Duncan, *Student Member, IEEE*, Brandon Mathieu, *Student Member, IEEE*, Samantha McDonnell, *Student Member, IEEE*, Vipul J. Patel, *Senior Member, IEEE*, Tony Quach, and Waleed Khalil, *Senior Member, IEEE*

***Abstract*—A multimode delta-sigma ($\Delta\Sigma$) RF digital-to-analog converter (RF-DAC) is proposed for direct digital-to-RF synthesis. The proposed circuit uses a single clock frequency (f_s) and provides a $\Delta\Sigma$ modulator (DSM) that operates in bandpass (BP) and highpass (HP) modes to synthesize signals around $f_s/4$, $f_s/2$, or $3f_s/4$. The on-chip 14 bit second-order DSM implements an array of 1 bit pipelined subtract functions to generate 3 bit f_s rate RF-DAC input data. Analog interleaving via a second 3 bit DAC is used to reject the first DAC image, simultaneously doubling the usable bandwidth of the HP DSM and increasing the SNR. Calibration circuits are added to the DAC to compensate for amplitude and timing variations. The proposed RF-DAC is implemented in 130 nm SiGe BiCMOS with an area of 0.563 mm^2. Measurements at $f_s = 2$ GHz yield an output power of -0.6 dBm with 76.2 dB signal-to-image-rejection ratio (SIRR), 76.2 dB SFDR over a 100 MHz bandwidth, -80 dBc IM3, -67.2 dB WCDMA ACLR, and -66.4 dBc LTE ACLR. Changing f_s to 3 GHz allows frequencies of 2.25 GHz to be generated with output power of -16.6 dBm, 65.2 dB SFDR, -62 dBc IM3, -59.3 dB WCDMA ACLR, and -59.2 dBc LTE ACLR.**

***Index Terms*—Delta-sigma modulation, highpass (HP) modulation, image rejection, interleaved digital-to-analog converter (DAC), interleaving, LTE, multiple Nyquist, reconfigurable noise shaping, RF-DAC, WCDMA.**

I. Introduction

OVER the last decade, advances in digital and RF integration have led to the development of mixing-digital-to-analog converters (also called RF-DACs) capable of low-noise and high-linearity direct digital-to-RF synthesis [1]. Unlike traditional D/A conversion where the output signal is restricted to less than half of the DAC sample rate, mixing-DACs [Fig. 1(a)] decouple the sample rate and output frequency by combining the upconversion mixer and DAC into a single, typically current-mode design capable of low-distortion RF signal generation via weighted current sources mixed by a local oscillator (LO) [2], [3]. However, the low resolutions of early designs do not meet the noise floor specifications of current communications' standards [4]. More recently, architectures have sought to satisfy these stringent noise requirements through both higher resolution and increased sample rate. In [5], an oversampling 14 bit polar mixing-DAC is designed for low far-out noise, critical for 2G/3G communications, while [6] increases resolution further, implementing a highly linear 16 bit mixing-DAC, sampled in the GS/s range and tunable across multiple GHz. However, to realize these high-resolution topologies, dozens of DAC cells are required, dramatically increasing the analog and digital footprints of the design. Due to this expanded footprint, the amplitude and timing mismatches among the DAC cells are increased, degrading the DAC linearity and introducing data-dependent distortion. Moreover, DAC current mismatch is exacerbated by reducing the size of the cell current source, limiting attempts to shrink the large DAC core. To minimize the impact of these mismatches, calibration and dynamic element matching (DEM) techniques have been proposed, correcting [7], [8], sorting and combining [9], or randomizing [10] the error between DAC cells. However, even with these techniques, a large number of cells are still needed to achieve the desired noise floor, increasing the area and complexity of the design as well as adding long calibration time during *in situ* operation. In addition to the costs of calibration, the large number of DAC cells limits the high-frequency performance of a design by loading the DAC output node and modulating the DAC output impedance [11].

As an alternative to high-resolution low-noise mixing-DACs, $\Delta\Sigma$-mixing architectures significantly reduce the size of the DAC with a preceding $\Delta\Sigma$ modulator (DSM). The DSM shapes excess quantization noise away from an RF passband, allowing low-noise signal synthesis within a narrow bandwidth. The mixing-DAC is then implemented with minimal resolution (1–3 bits), thereby leveraging scalable digital processing to reduce analog complexity [12]. Furthermore, the low-resolution DAC core reduces output loading and internal mismatch while minimizing the overhead of calibration circuitry and limiting the time needed to run a given calibration technique.

These advantages are first described in [13] where the performance of a conventional $\Delta\Sigma$ DAC is compared to that of a $\Delta\Sigma$-mixing architecture. The work in [14] digitally upconverts a lowpass (LP) DSM output to an intermediate frequency (IF) before RF mixing with an LO. This operation offsets the signal bandwidth from the LO, clearing the output band of unwanted LO leakage and mixing images which result from I/Q mismatch. Another digital IF architecture, reported in [15],

Manuscript received September 01, 2015; revised January 01, 2016; accepted January 11, 2016. Date of publication March 22, 2016; date of current version April 28, 2016. This paper was approved by Guest Editor Salvatore Levantino. This work was supported by the Air Force Research Laboratory.

J. J. McCue, B. Dupaix, L. Duncan, B. Mathieu, S. McDonnell, and W. Khalil are with the Electroscience Laboratory, The Ohio State University, Columbus, OH 43210 USA (e-mail: mccue.28@buckeyemail.osu.edu).

V. J. Patel and T. Quach are with the Air Force Research Laboratory, Wright-Patterson AFB, Dayton, OH 45433 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2521903

0018-9200 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

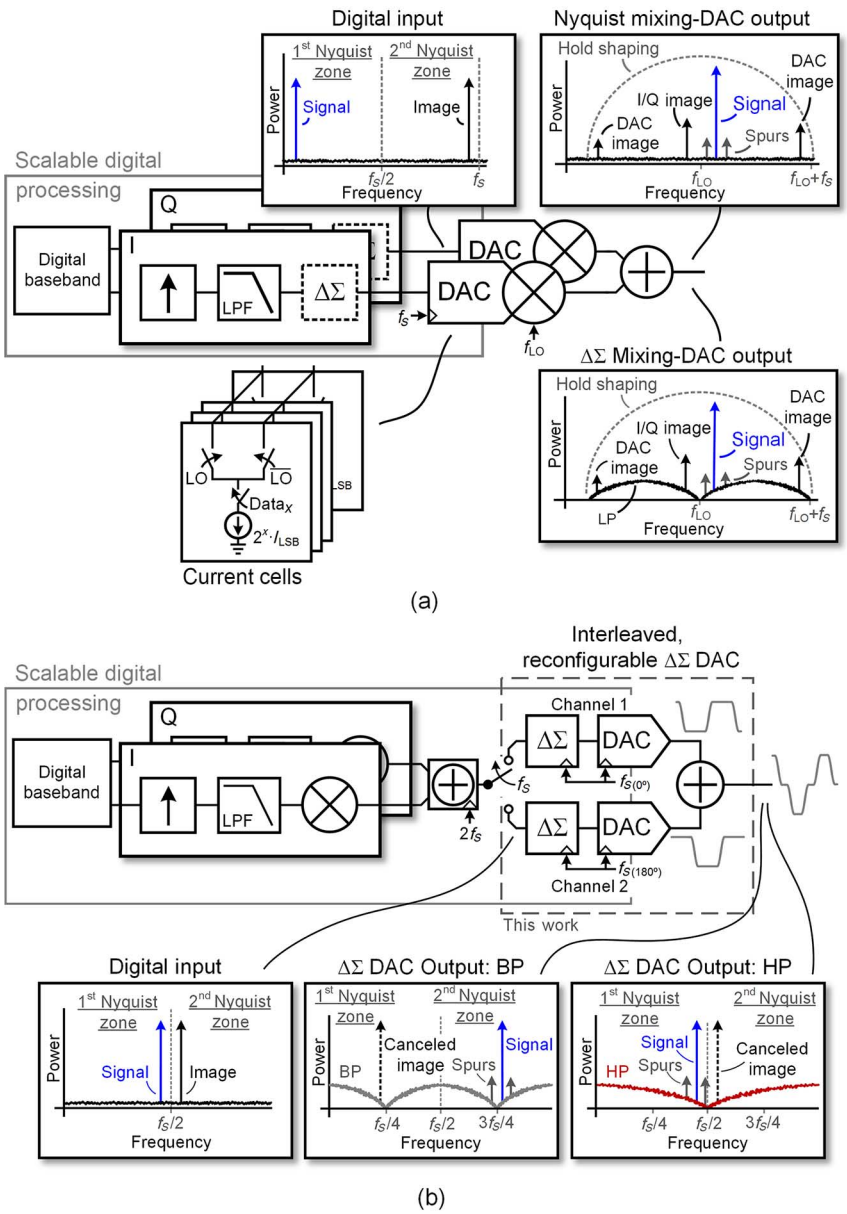

Fig. 1. (a) Nyquist rate or $\Delta\Sigma$ mixing-DAC exhibiting finite sideband image suppression and DAC replica images attenuated by hold shaping. (b) Direct digital-to-RF transmitter utilizing the proposed time-interleaved reconfigurable $\Delta\Sigma$ DAC and depicting HP and BP modulation enabled by interleaved image cancelation.

implements a bandpass (BP) DSM at IF, creating a low-noise passband subsequently upconverted to RF via an inherently linear 1 bit mixing-DAC. In [16], a $\Delta\Sigma$ topology enables digital I/Q mixing beyond IF by directly upconverting high-speed DSM data with an all-digital mixer, the output of which is fed into weighted I and Q current cells for dynamic power control.

Despite the advantages of $\Delta\Sigma$ modulation, the mixing-DAC architecture has several inherent limitations. First, the absence of a reconstruction filter before upconversion gives rise to close-to-carrier images in the DAC output. Even with the attenuation of hold shaping, [17], mixing-DACs have shown a maximum image suppression of 54 dB [18]. Instead, designs sample the baseband signal at frequencies which approach or exceed the LO frequency [14], [16], pushing DAC images further out of band. However, these high-frequency sampling clocks must be accurately aligned to the LO signal to mask the jitter of incoming data and maintain in-band noise performance [15]. Additionally, since I/Q mixing and combining are performed in the analog domain, both amplitude and timing mismatches can corrupt the output error vector magnitude and induce mixing images. This is further exacerbated by the challenge of multi-band operation where the LO must provide both wide frequency tuning and low phase noise.

This is in contrast to fully digital mixing which does not introduce IQ mismatch nor does it require the alignment of a widely tuned analog LO [19]. Instead, up-sampled data is multiplied by a clock signal to digitally synthesize RF signals. While the output frequency is limited by the digital sample rate of the system, the speed and performance of digital mixing will continue to improve with technology scaling. Therefore, a viable

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

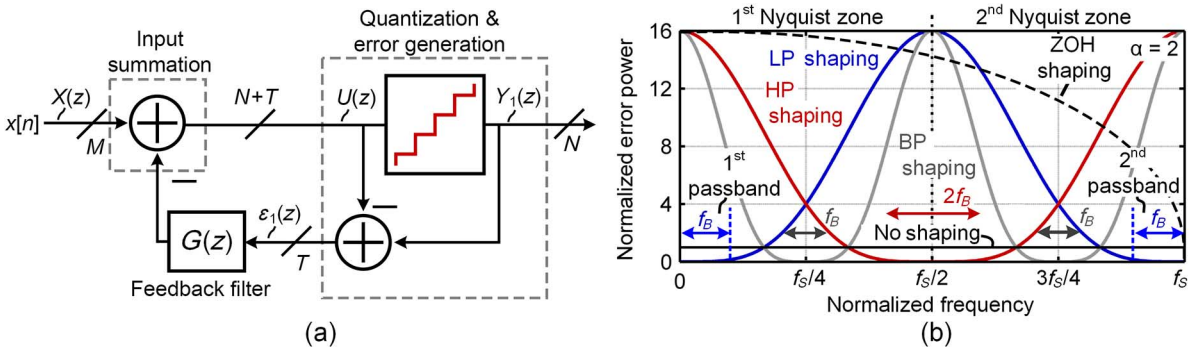

Fig. 2. (a) Error FB ΔΣ modulator. (b) Noise shaping of a second-order ($\alpha = 2$) LP, BP, and HP DSM with f_B representing the usable ΔΣ bandwidth.

alternative to the mixing-DAC architecture becomes that of fully digital I/Q mixing coupled with a high-speed ΔΣ DAC. Such a system is described in [20] where a single high-speed clock is used for both a LP DSM and to directly synthesize the results of all-digital mixing and I/Q combining. To demonstrate this, [20] employs an inherently linear 1 bit inverter to directly synthesize a GHz-range RF output by leveraging the first image of the sampled waveform. However, due to its supply noise sensitivity, the single-bit inverter topology contributes high jitter and, as a result, increases in-band noise. Additionally, when utilizing outputs in the second Nyquist zone, a high-power image is present in the first, requiring high stopband attenuation in the subsequent reconstruction filter.

In this work, a multiorder multiband ΔΣ DAC is proposed to leverage the advantages of all-digital I/Q upconversion while also improving jitter performance and canceling unwanted, high-power image replicas. This is accomplished by arraying two time-interleaved channels containing both the DSM and DAC while utilizing readily available 180° clocks. When summed, the channel outputs cancel the unwanted images and reject their associated nonlinearity spurs, leveraging multiple Nyquist zones to achieve high-frequency RF signal synthesis [21]. By canceling the first DAC image, the proposed design uniquely enables highpass (HP) ΔΣ modulation which, as can be seen in Fig. 1(b), has twice the bandwidth of BP ΔΣ modulation due to its near Nyquist operation [22]. Additionally, the residual DAC image is located in-band, acting as a self-interfering signal as opposed to an out-of-band spurious emission. It is worth noting that including the DAC as part of the interleaved data channel minimizes the speed and timing constraints compared with other interleaving schemes which focus exclusively on the DSM and require a high-speed multiplexer and DAC [23], [24]. Taking advantage of the all-digital DSM, a reconfigurable modulator is created by switching between various MASH stages and filter functions, synthesizing RF passbands at 1/4, 1/2, or 3/4 of the system clock rate.

The proposed design is implemented in a $0.13\,\mu\mathrm{m}$ SiGe process where the DSM and data alignment are accomplished with the available CMOS. The use of a ΔΣ architecture enables area efficient integration of the high-performance SiGe HBTs into the DAC core, thus improving DAC linearity and switching speed. Additionally, CML clocking and retiming are used to limit data jitter, improving in-band noise performance, while amplitude and timing calibration ensure DAC linearity and replica image cancelation.

Section II gives a brief overview of the design, highlighting the reconfigurable DSM, the channel interleaving, and the effects of amplitude and timing errors on system performance. Section III discusses the circuit design of the reconfigurable DSM, data drivers, and DAC current cells. Measurement results and comparison to other designs are then discussed in Section IV with concluding remarks given in Section V.

II. Interleaved Multimode ΔΣ DAC

Given the fundamental link between sample rate and bandwidth in ΔΣ modulation, a significant focus of recent DSM work has been on high-speed (GS/s) operation of DSMs, achieved through a combination of novel digital architectures [14], phase unrolling [25], pipelining [26], and time interleaving [23], [24]. However, existing architectures target baseband synthesis, utilizing LP DSMs to generate near-dc signals. In contrast, this section discusses a time-interleaved design which includes both the DSM and the DAC. This design increases the effective sample rate of the system without requiring a high-speed mux and a subsequent higher frequency clock domain to reconstruct the modulated signal. The proposed DSM also leverages its all-digital architecture to switch between multiple filter functions and orders.

A. Reconfigurable ΔΣ Modulation

The proposed DSM utilizes the error feedback (FB) topology shown in Fig. 2(a) due to its short critical path and straightforward digital implementation [27]. A general expression for the N bit modulator output $Y_1(z)$ is given in (1) and is calculated from the quantization error $\varepsilon_1(z)$, the FB filter $G(z)$, and $X(z)$, the z-transform of the M bit modulator input $x[n]$

$$Y_1(z) = X(z) + \varepsilon_1(z)\left(1 - G(z)\right). \tag{1}$$

In (1), the error shaping of the noise transfer function $(\mathrm{NTF} = 1 - G(z))$ creates a low-noise bandwidth in the modulator output. For a LP design of order α, the filter described in (2) can be used to achieve the required shaping. This is demonstrated for a second-order design ($\alpha = 2$) in Fig. 2(b) where (2)

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

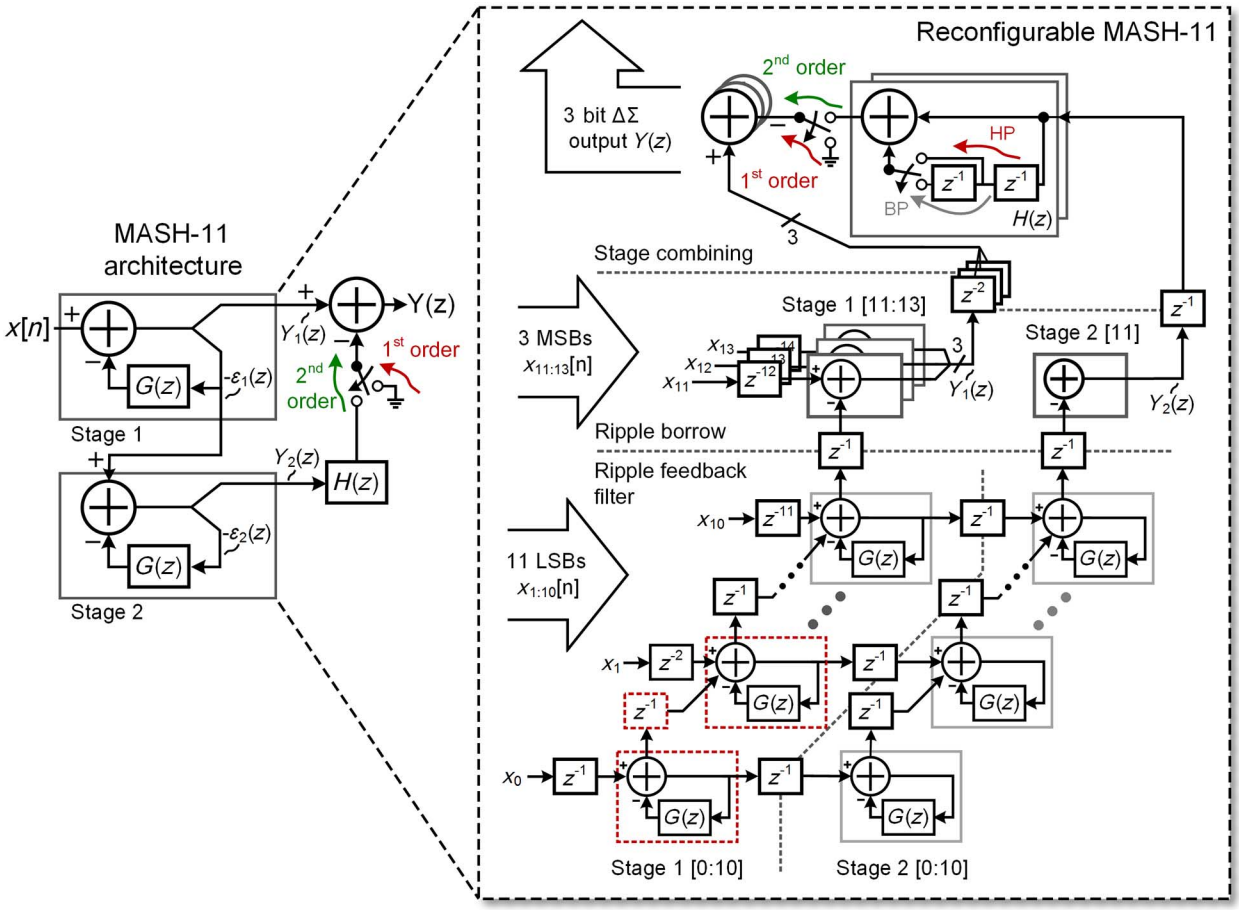

Fig. 3. MASH-11 modulator pipelined with 1 bit unit cells.

is plotted as a function of frequency, normalized by the sample rate f_S, using the identity $z = e^{j2\pi f/f_S}$

$$G(z)_{\mathrm{LP}} = 1 - \left(1 - z^{-1}\right)^{\alpha}. \tag{2}$$

As seen from this figure, the first LP passband is of no use for direct RF synthesis due to its low frequency while higher Nyquist passbands, occurring at multiples of f_S, prove impractical due to the attenuation of the DAC zero-order hold (ZOH). Instead, the proposed design implements BP and HP filter functions derived from (2) by substituting $z^{-1} \rightarrow -z^{-2}$ and $z^{-1} \rightarrow -z^{-1}$, respectively. The shaping that results is also plotted in Fig. 2(b) and shows the $\Delta\Sigma$ passbands shifted to $f_S/4$ and $3f_S/4$ for BP and $f_S/2$ for HP shaping. This frequency shift corresponds to a rotation in the NTF zero locations and results in the doubling of the HP bandwidth to $2f_B$, now composed of passbands in adjacent Nyquist zones. Taken together, the two filter functions allow the DSM to synthesize several RF passbands, one with double bandwidth, without the need to tune the system clock or alter the DSM sample rate.

For the DSM to integrate both of these filter functions at RF sample rates, a MASH-11 architecture, depicted in Fig. 3, is used to pipeline the order of the design. Two first-order stages, consisting of single-tap filters [Fig. 4(a)], reduce FB latency compared with a higher order single-stage DSM. As in (1), the first MASH stage shapes the quantization error $\varepsilon_1(z)$. This error is also passed to the second stage whose output is given by

$$Y_2(z) = \varepsilon_1(z) + \varepsilon_2(z)\left(1 - G(z)\right). \tag{3}$$

Multiplying this output by $H(z)$ allows $Y_2(z)$ to be scaled such that $\varepsilon_1(z)$ is completely canceled in the DSM output summation, and the remaining error $\varepsilon_2(z)$ is shaped with a higher order NTF [27]. By setting $H(z) = G(z) - 1$, the MASH output becomes

$$Y(z) = X(z) - \varepsilon_2(z)\left(1 - G(z)\right)^2. \tag{4}$$

Switching between the second-stage output and zero, as depicted by the output combining in Fig. 3, allows the design to be configured for first- or second-order shaping.

To further maximize the speed of the modulator, each MASH stage is itself pipelined using 1 bit unit cells. In this way, the logic operation performed during a single clock period is reduced to that of a 1 bit subtractor with the borrow propagated via a ripple architecture. A total of eleven of these cells [0:10] are used to shape the LSB quantization error in each MASH stage while MSB cells account for any borrow signal emerging from the noise shaping.

Within the LSB cell and the output combining, reconfigurable filters are used to realize both BP and HP shaping. Since

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

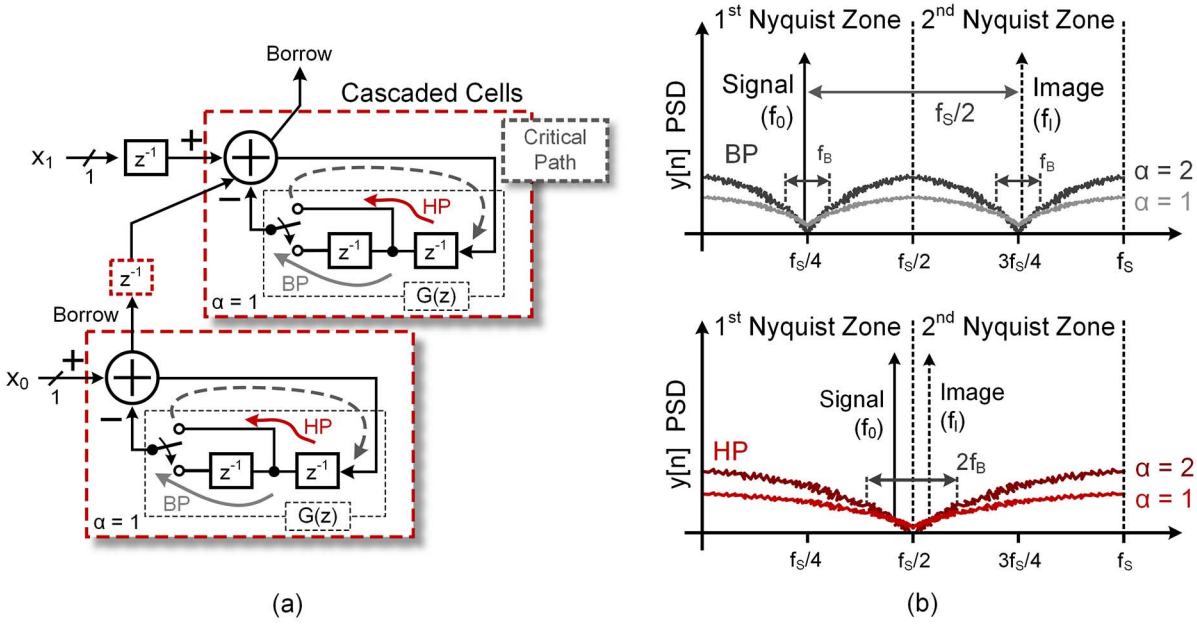

Fig. 4. (a) Two reconfigurable bit cells and (b) multimode ΔΣ shaping with both the signal and first image shown.

the desired functions differ by a single delay (z^{-1}), implementing both simply requires alternating between two delay values, as highlighted in Fig. 4(a). Altogether, the pipelined structure allows the proposed DSM to synthesize the outputs depicted in Fig. 4(b): first- and second-order shaping for both BP and HP passbands. While this architecture requires staggered data input and several alignment stages, increasing the power, area, and latency through the design, it also creates a robust, highly modular architecture based on the design of a single bit cell, subsequently described in Section III.

B. Multi-Nyquist Operation

For a sampled output signal of frequency f_0, there exist image replicas of the signal in every Nyquist band. The frequency of the kth image is represented by f_I as

$$f_I = kf_S \pm f_0 \,[k = 0, 1, 2, 3, \ldots]\,. \tag{5}$$

In the case of a BP-configured DSM, the filtering can be relaxed due to the inherent $f_S/2$ offset between the signal and the image, as shown in Fig. 4(b). However, in HP operation, the image cannot be effectively filtered since the signal and interfering image occupy the same passband. To mitigate this replica, works such as [28] propose a guard band between the image and signal, sacrificing useable bandwidth while marginally relaxing filter requirements. Alternatively, the addition of parallel channels can be used to cancel all replica images up to the effective Nyquist rate of the system. This method of interleaving described generally in [21] and specifically for a 2 channel system in [29], differs from those described in previous DSMs [23], [24]. Typically in DSM interleaving, the outputs of a channel FB filter are passed to an adjacent channel, enabling P low-speed paths to achieve equivalent noise shaping to that of a single channel running P times as fast. In this work, the independence of each channel is maintained, eliminating the speed and timing requirements created by passing data between parallel paths. While this channel independence does not produce the same effective increase to the oversampling ratio (OSR) of the DSM, it does enable the output of the interleaved channels to be easily summed, eliminating high-speed multiplexing which increases the sample rate of the subsequent DAC and folds shaped noise back in-band [30].

The proposed ΔΣ interleaving is depicted in Fig. 5(a) and (b) with the number of parallel data paths P set to two. As highlighted by Fig. 5(a), the input data $x\,[n]$ is alternately fed into the two channels, each operating at a clock rate of f_S but phase offset from one another by 180° $(360°/P)$. Inputs to each channel can then be modeled using down-sampled versions of $x\,[n]$. For the even samples of Channel 1, the signal is first delayed (z^{-1}) and then downsampled, as depicted in Fig. 5(b). The expression of these two operations is given in (6) where $X_{\mathrm{CH1}}\,(z)$ defines the z-transform of $x_{\mathrm{CH1}}\,[n]$ and P is used as the down-sampling factor

$$X_{\mathrm{CH1}}\,(z) = \frac{1}{P}\sum_{n=0}^{P-1}\left(z^{1/P}\cdot e^{-j2\pi n/P}\right)^{-1} X\left(z^{1/P}\cdot e^{-j2\pi n/P}\right). \tag{6}$$

To obtain the odd samples for the Channel 2 input, no delay is needed and the input becomes

$$X_{\mathrm{CH2}}\,(z) = \frac{1}{P}\sum_{n=0}^{P-1} X\left(z^{1/P}\cdot e^{-j2\pi n/P}\right). \tag{7}$$

Setting $P = 2$ results in

$$X_{\mathrm{CH1}}\,(z) = \frac{z^{-1/2}}{2}\left(X\left(z^{1/2}\right) - X\left(-z^{1/2}\right)\right) \tag{8}$$

and

$$X_{\mathrm{CH2}}\,(z) = \frac{1}{2}\left(X\left(z^{1/2}\right) + X\left(-z^{1/2}\right)\right) \tag{9}$$

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

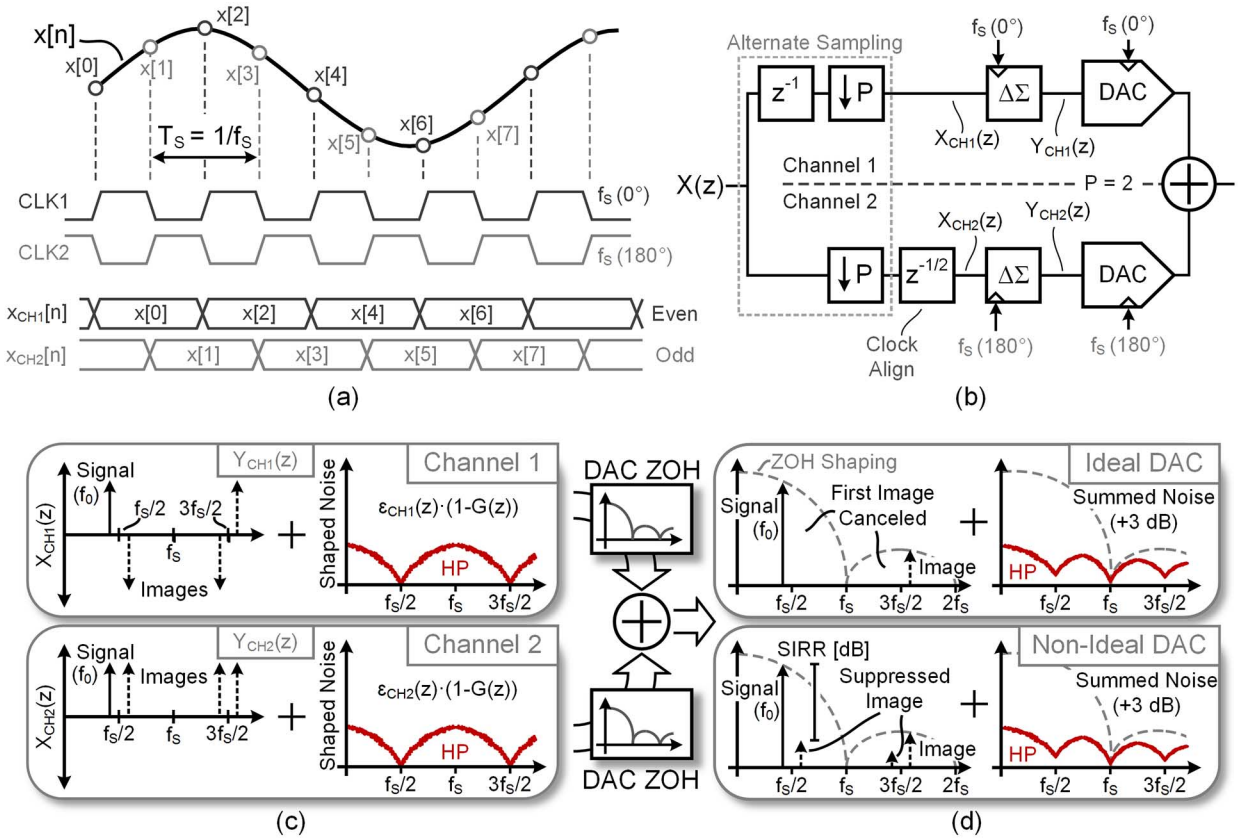

Fig. 5. (a) Alternate data samples are aligned to 180° clocks and fed into (b) two parallel DSM and DAC channels. (c) Each DSM spectrum is composed of the input $X_{\mathrm{CH1,2}}(z)$ and shaped, uncorrelated error $\varepsilon_{\mathrm{CH1,2}}(z)$. Upon D/A conversion, (d) unwanted (antiphase) images are canceled.

where $X\left(z^{1/2}\right)$ describes the signal and its even images [$k = 0, 2, 4, \ldots$] while $X\left(-z^{1/2}\right)$ describes the odd images [$k = 1, 3, 5, \ldots$].

After aligning Channel 2 to the 180° clock (equivalent to adding a half period delay of $z^{-1/2}$), the data is passed through the $\Delta\Sigma$ modulators. Substituting $X_{\mathrm{CH1}}(z)$ and $X_{\mathrm{CH2}}(z)$ into (1), respectively, yields the output of each DSM

$$Y_{\mathrm{CH1}}(z) = \frac{z^{-1/2}}{2}\left(X\left(z^{1/2}\right) - X\left(-z^{1/2}\right)\right) + \varepsilon_{\mathrm{CH1}}(z)\left(1 - G(z)\right) \quad (10)$$

$$Y_{\mathrm{CH2}}(z) = \frac{z^{-1/2}}{2}\left(X\left(z^{1/2}\right) + X\left(-z^{1/2}\right)\right) + z^{\frac{1}{2}}\varepsilon_{\mathrm{CH2}}(z)\left(1 - G(z)\right). \quad (11)$$

As depicted in Fig. 5(c), the output spectra of these two channels are composed of the channel input spectrum, $X_{\mathrm{CH1}}(z)$ or $X_{\mathrm{CH2}}(z)$, along with the shaped noise. Assuming ideal D/A conversion, the output of the interleaved DAC is represented by the summation of the two DSM outputs given in the following equation:

$$Y_{\mathrm{CH1}}(z) + Y_{\mathrm{CH2}}(z) = z^{-1/2}X\left(z^{1/2}\right) + \left(\varepsilon_{\mathrm{CH1}}(z) + z^{1/2}\varepsilon_{\mathrm{CH2}}(z)\right)\left(1 - G(z)\right). \quad (12)$$

Here, the desired signal and its even images add constructively, increasing their output power by 6 dB over that of a single channel, while the odd images are antiphase and are cancelled. Since the two error signals are uncorrelated, they do not cancel but add incoherently, increasing the noise power by 3 dB. The difference between the increase in signal power and noise density causes an increase of $0.5(P-1)$ bits in the resolution of the interleaved output [21]. To demonstrate the image cancelation and the increase in both the desired signal and noise power, an ideal second-order HP DSM and DAC are simulated and compared to an interleaved-by-two architecture in Fig. 6(a).

C. Nonideal Image Cancellation

Variations in signal amplitude or timing between the interleaved paths result in nonideal image suppression, as depicted in Fig. 5(d). This nonideality is quantified by the signal-to-image replica ratio (SIRR) expressed in (13). Based on the similarity observed in [31] between the interleaved-by-two architecture and an image reject mixer [32], (13) takes into account the error in timing δt between the 180° system clocks as well as the amplitude ratio γ between the two DAC outputs (ideally $\gamma = 1$). In addition to these errors, differences in the hold shaping between the signal and the image affect the SIRR. To account for this, the ratio in (14) is applied to (13) as a second additive term

$$\mathrm{SIRR} = 10 \cdot \log\left(\frac{\gamma^2 + 1 + 2\gamma\cos\left(\pi f_0 \delta t\right)}{\gamma^2 + 1 - 2\gamma\cos\left(\pi f_I \delta t\right)}\right) + 20 \cdot \log\left(\frac{f_I}{f_0}\right)\ [\mathrm{dB}] \quad (13)$$

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

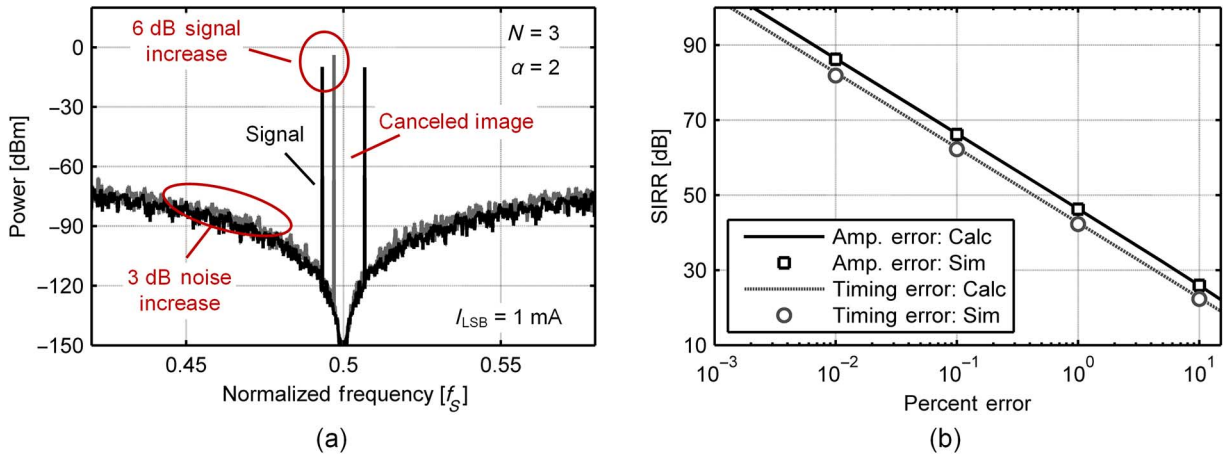

Fig. 6. Simulation of a second-order HP DSM and 3 bit DAC (1 mA I_{LSB}) showing (a) the comparison of a single DAC (black) to an interleaved-by-two architecture (gray) and (b) the calculated and simulated SIRR.

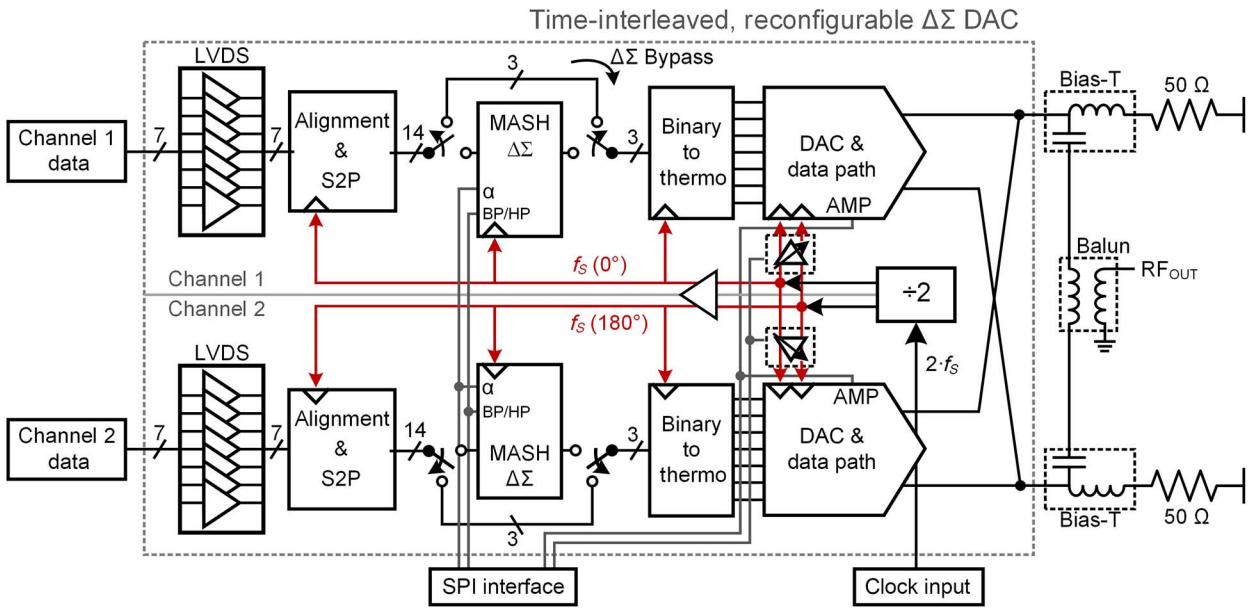

Fig. 7. Block diagram of the implemented DSM and DAC.

$$\frac{\operatorname{sinc}(f_0/f_S)}{\operatorname{sinc}(f_I/f_S)} = \frac{f_I \sin(\pi f_0/f_S)}{f_0 \sin(\pi f_I/f_S)} = \frac{f_I}{f_0}. \tag{14}$$

However, this term becomes negligible for HP modulation as f_0 and f_I are in the same passband ($f_0 \approx f_I$), and the second term approaches zero. Fig. 6(b) shows simulation results of the interleaved architecture with amplitude and timing errors injected into one of the interleaved channels. A close match is observed between analytical and simulated results, confirming the validity of (13).

III. Circuit Implementation

The block diagram of the ΔΣ DAC, shown in Fig. 7, comprises two parallel data paths, with each path aligned to separate 180° clocks derived from an off-chip 2X source. For each path, interleaved samples are received from an FPGA through seven LVDS channels parallelized into a 14 bit bus. Incoming data is offset off-chip to account for the pipelining of the DSM computation. A data path bypassing the DSM is also implemented to enable stand-alone DAC calibration and testing. After modulation, the 3 bit DSM outputs are thermometer encoded, retimed by clean clocks, and driven into the DAC current cells. To ensure accurate interleaving and linear DAC performance, fine amplitude and timing adjustments are also implemented via SPI registers.

A. Data Input

The ΔΣ function operates at the DAC's GS/s rate, requiring significant I/O bandwidth for each interleaved 14 bit data stream. To meet this requirement, low-power LVDS receivers are implemented on-chip to achieve a 4 Gb/s double-data rate input stream, enabling fourteen 2 Gb/s data input channels with seven receivers per DAC. In addition, three channels can be configured to bypass the DSM for stand-alone DAC testing. As shown in Fig. 8(a), the receiver is AC-coupled on-chip

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

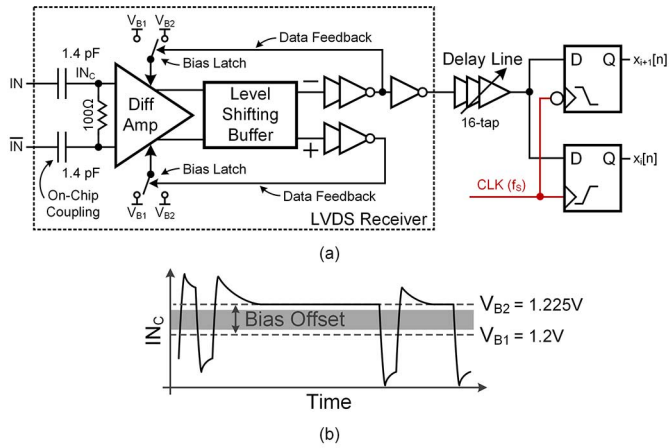

Fig. 8. (a) LVDS receiver and serial-to-parallel operation with (b) showing the latching of the coupled input.

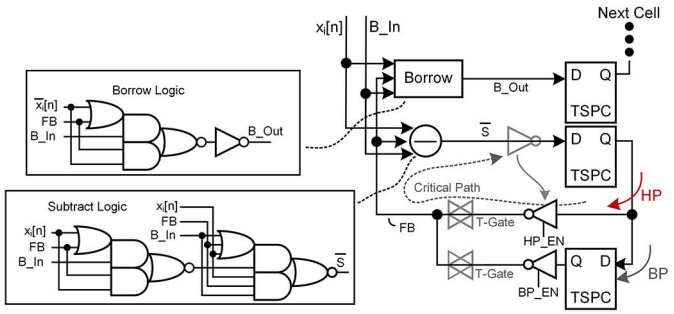

Fig. 9. 1 bit DSM cell showing the relocation of the $\overline{S}$ inversion.

with 1.4 pF capacitors, minimizing layout area. AC-coupled I/O usually requires encoded data to maintain DC balance, adding overhead to the high-speed data stream. Instead, the implemented receiver uses the coupling capacitor to create a return-to-zero pulse which removes baseline wander. These pulses are then latched by toggling the bias of the positive and negative amplifier inputs according to the previous bit [33]. As each pulse decays to the receiver bias voltage, the positive and negative legs of the amplifier remain offset, holding the new bit [Fig. 8(b)]. Following the receiver, incoming data is passed through a 16 tap adjustable delay line to compensate for off-chip clock-to-data skews of up to 1.2 ns. Once data is correctly aligned to the on-chip clock, the 4 Gb/s data from each channel is latched and separated into two 2 Gb/s streams via two flip-flops (FF) operating on opposite clock edges.

B. $\Delta\Sigma$ Bit Cell

As discussed in Section II-A, the 14 bit DSM is pipelined using 1 bit unit cells. This approach allows the DSM speed to increase up to the latency of the FB path. As shown in Fig. 9, this critical path consists of only the subtract logic and the HP/BP switches. For low latency, the subtraction is computed with an optimized 1 bit ripple carry add [34] with the borrow logic implemented in parallel. In the subtraction, the final inversion of $\overline{S}$ to S is relocated from directly after the function (gray) to after the delay FFs, allowing the BP and HP switches to be implemented with tristate inverters (black) instead of slower undriven transmission gates (gray). Minimum area and power true single phase clock (TSPC) FFs [35] are implemented, relying on the tristate inverters to drive the subtraction logic. This optimization reduces the FB latency by 40 ps in simulation, increasing the timing margin by 8% of the clock period at 2 GS/s.

C. DAC Core

The proposed 3 bit DAC core directly determines the SFDR and SNDR performance of the $\Delta\Sigma$ system, requiring a design that achieves much higher linearity than a 3 bit Nyquist DAC. As shown in Fig. 10, the core of each DAC comprises seven unary-weighted current switching cells. The unary architecture exhibits low data-dependent glitches at the DAC output and relaxes the constraints on current matching compared to the conventional binary and segmented schemes [36], [37]. The proposed design uses SiGe HBTs, mitigating nonlinearities caused by data-dependent impedance modulation [38]. Although SiGe HBTs are large, the DAC core comprises only seven unary cells allowing for a compact layout with reduced routing parasitic [39] and timing skew [40].

The current source in the DAC cell is implemented via CMOS transistors and placed outside the DAC cell array for compact interdigitation and optimized matching, as shown in Fig. 10. The output of each current source is routed to an individual cell, where it is cascoded with an HBT just before the data switches, providing high output impedance for the switched pair by shielding them from the interconnect capacitance. The data switches are implemented using HBTs to provide superior switching speed and output impedance as compared to those of their CMOS counterparts. Additionally, cascoded HBTs shield the data switches from the DAC output, further increasing the cell output impedance. A CMOS bleed current (35 μA) is added to each cascode to improve SFDR by keeping the cascode transistors ON, thereby reducing the data dependency of the cell output impedance and the settling time when the corresponding data switch is turned OFF [41].

To maximize the linearity and noise performance of the DAC current cell, any data-dependent timing effects on the data inputs to the cell must be minimized. While the impact of deterministic jitter has been analyzed in Nyquist DACs [42], to the authors' knowledge, no such analysis has been provided for $\Delta\Sigma$ DACs. Fig. 11(a) shows behavioral simulations of the DAC in the presence of deterministic jitter at the input of each current cell. A peak-to-peak deterministic jitter of just 1% of the clock period (5 ps at 2 GS/s) results in degradations in SFDR and SNR of nearly 20 and 6 dB, respectively. To minimize this effect, the data path, shown in Fig. 10, utilizes CML structures to retime the data and drive appropriate levels to the data switches in the current cell. Full-scale CMOS data from the thermometer encoder drives the first CML latch. While this stage removes much of the data-dependent jitter induced by the encoder and preceding circuitry, some remains (~130 fs of p-to-p jitter) due to the unbalanced differential input created by the inverter delay and due to the CMOS inputs overdriving the CML latch, pushing it out of saturation. The remaining jitter is nearly eliminated by a second CML latch that is driven by CML signals. The retiming latches are followed by two stages

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

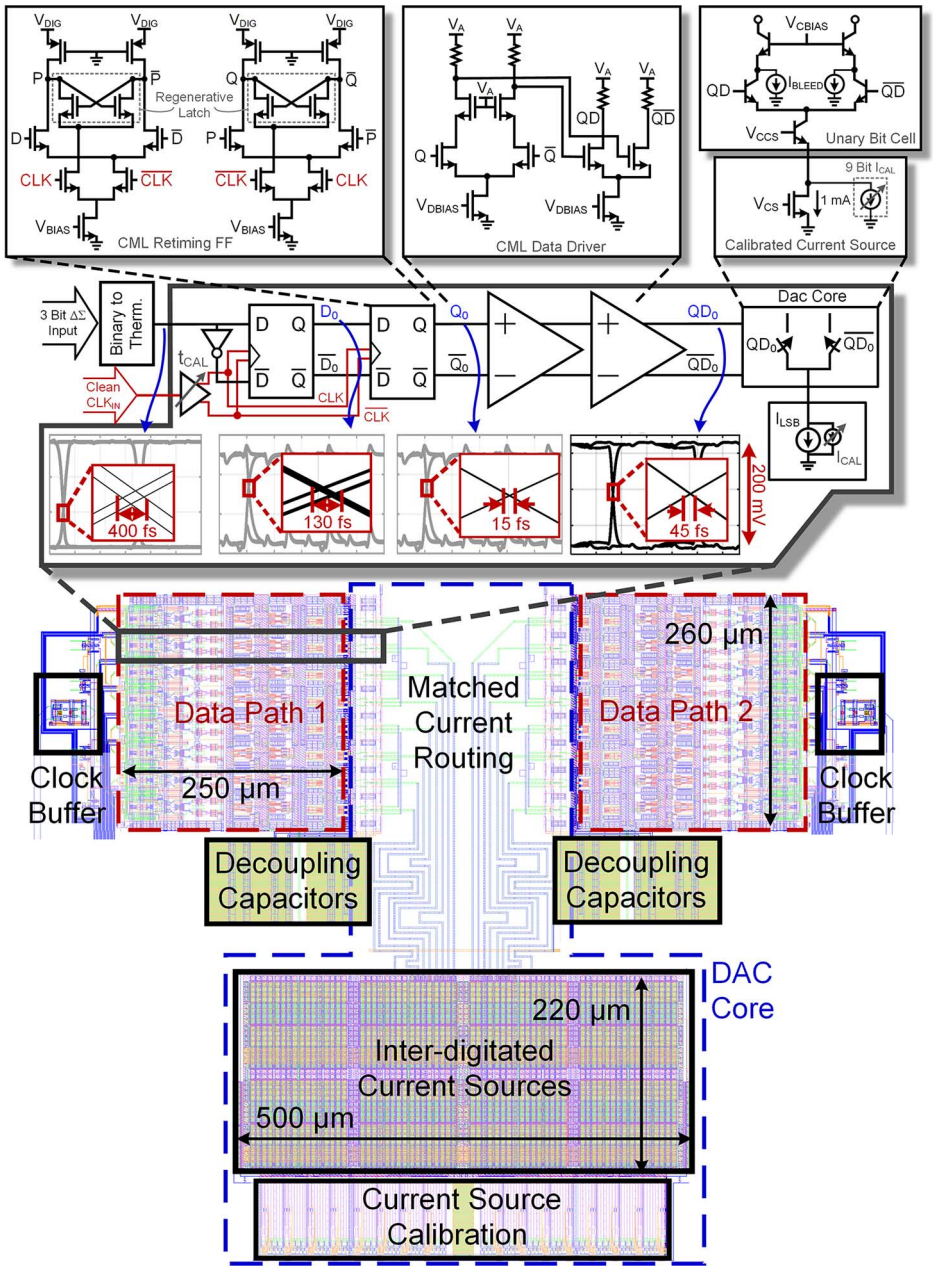

Fig. 10. Schematic and layout of the data path and interleaved DAC core.

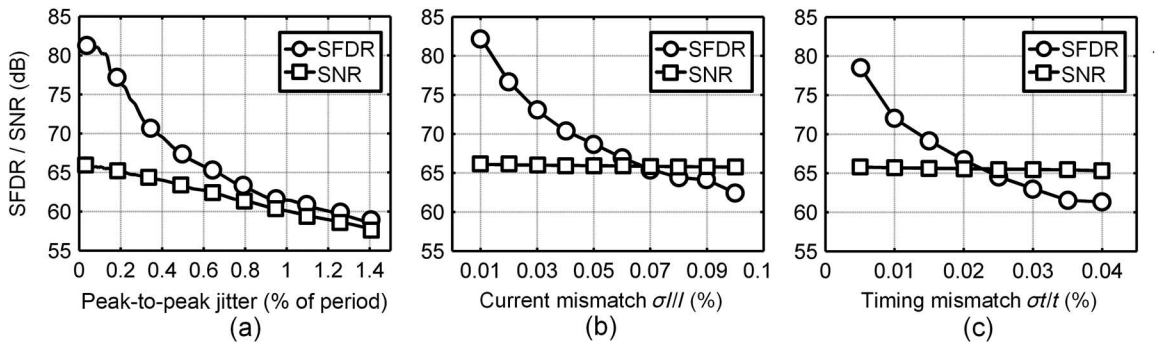

Fig. 11. SFDR and SNR performance across variations in (a) deterministic jitter, (b) static current mismatches, and (c) static timing mismatches.

of CML buffers. Although these buffers slightly increase the deterministic jitter because they are not clocked, they reduce the clock feedthrough from the latches and provide a voltage swing that is designed to minimize data-dependent jitter in the current cell switches [43]. Supply voltage induced deterministic jitter is mitigated by separating the power supply for the

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

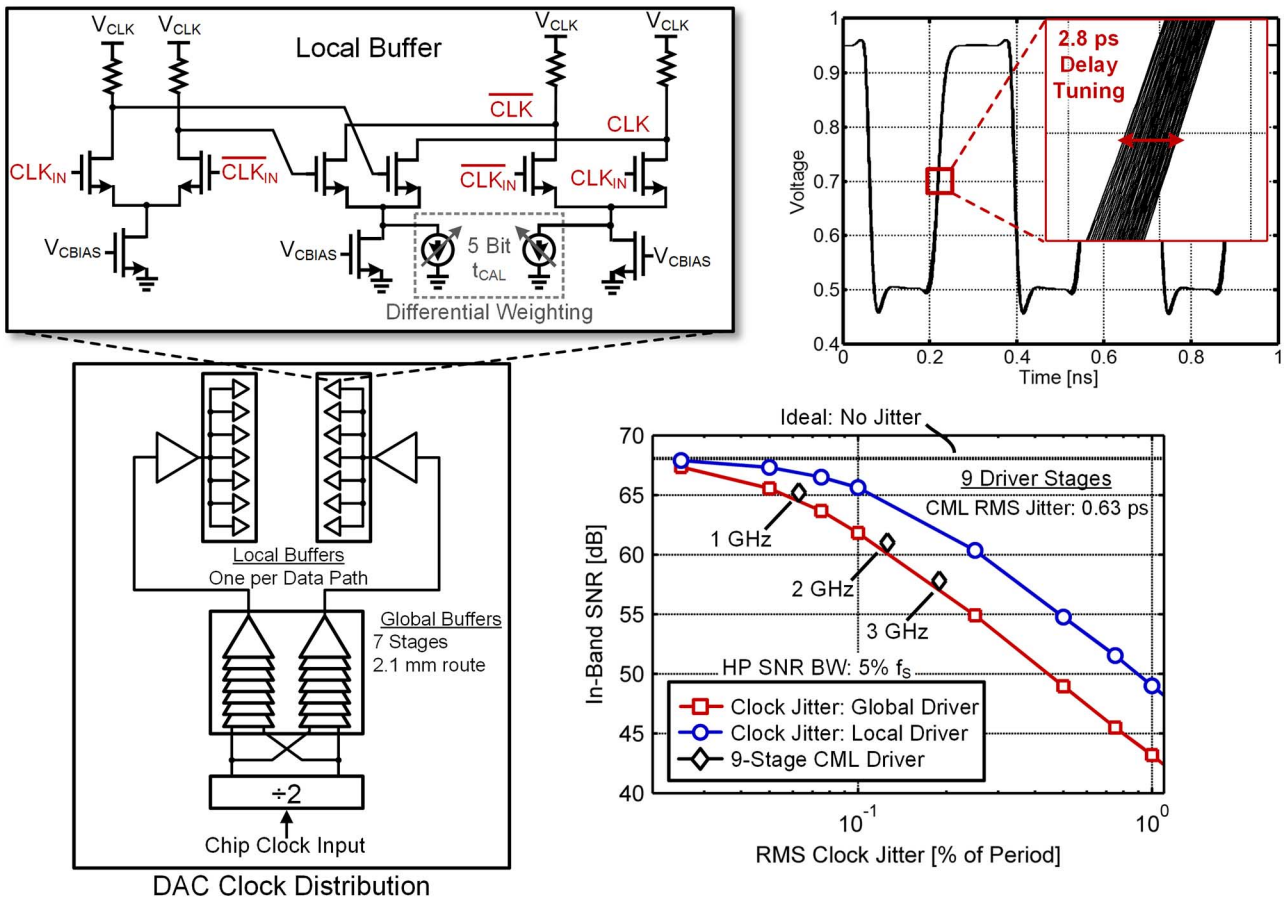

Fig. 12. Clock distribution scheme and simulation of SNR for both local and global drivers.

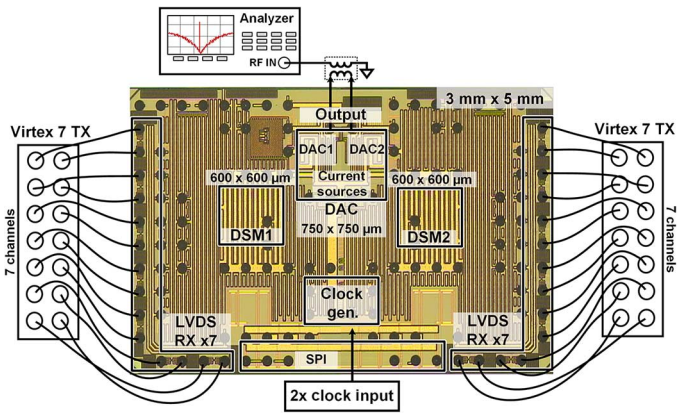

Fig. 13. Photograph of the $3\,\mathrm{mm} \times 5\,\mathrm{mm}$ test chip.

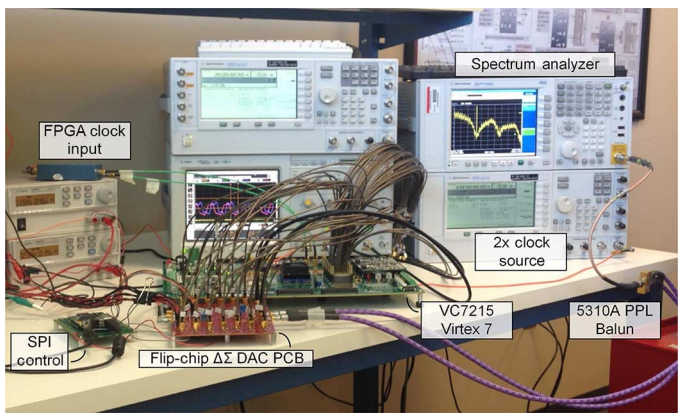

Fig. 14. Test setup of the interleaved $\Delta\Sigma$ DAC.

retiming data path and clock drivers from the rest of the digital circuitry. Fig. 10 shows the simulated eye diagram at the outputs of the second data driver in the data path. The peak-to-peak deterministic jitter is reduced to 45 fs (0.014%), resulting in a negligible degradation in SFDR and SNR.

D. DAC Amplitude and Timing Calibration

Even with the size and matching benefits of a low-bit $\Delta\Sigma$ DAC, the proposed multibit design ($N = 3$) still faces stringent requirements on linearity and timing to ensure that the rejected image and other spurious tones do not degrade the SNDR of the system. Static current mismatch within one DAC can manifest as spurious tones in the output while current mismatch between the interleaved DACs decreases the effectiveness of image cancellation, as described in (6). A Monte Carlo (MC) simulation performed on the interleaved $\Delta\Sigma$ DACs identifies the impact of static current mismatches, yielding the SFDR (including the replica image spur) given in Fig. 11(b). Each MC run includes

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

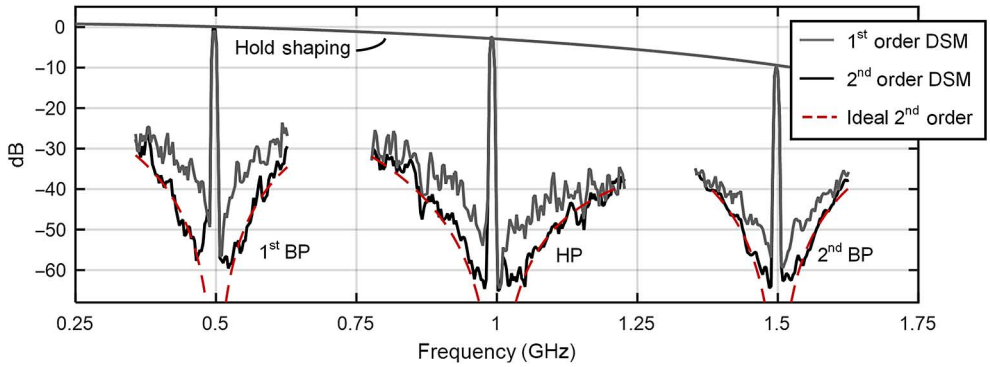

Fig. 15. Measured DAC output spectrum at 2 GS/s for first- and second-order BP and HP noise shaping with ideal second-order shaping shown.

1500 iterations, and the 97.7% yield line is plotted using a 95% confidence level. To ensure an SFDR above 70 dB, a mismatch tolerance of $\sigma_I/I_{\mathrm{LSB}} = 0.03\%$ is required. To achieve this in a reasonable area, the CMOS current source is designed for a 0.3% mismatch, and a 9 bit calibration DAC is used to fine tune the current of each cell. Similarly, static timing mismatches in the DACs can also degrade the SFDR and SIRR. Fig. 11(c) gives the MC results of DAC SFDR for various static timing mismatches between cells. As shown, a timing mismatch of 0.013% is required to achieve 70 dB of SFDR. To account for this possible mismatch, a 5 bit timing adjustment circuit is implemented via the interpolative clock buffer shown in Fig. 12. In this design, $\mathrm{CLK_{IN}}$ and $\overline{\mathrm{CLK}}_{\mathrm{IN}}$ are separately weighted by the current adjustment and then summed at the output node, allowing the design to shift the clock in $\sim$90 fs steps across a range of > 2.8 ps.

E. DAC Jitter

While static mismatches dramatically affect the DAC SFDR, they have less impact on in-band noise performance. This is highlighted in Fig. 11(b) and (c) where the ΔΣ DAC SNR is plotted with respect to MC mismatch for a 5% bandwidth ($0.05 \cdot f_S$). However, dynamic effects, such as clock jitter, significantly affect SNR performance. To demonstrate this, Fig. 12 plots the SNR for two cases: that of global clock jitter (all DAC cells experiencing the same jitter) and local clock jitter (each DAC cell has statistically independent jitter). For low RMS jitter, the SNR of both global and local clock jitters approach an ideal value set by the noise shaping of the DSM. As jitter increases, the effects of global jitter add coherently and degrade the SNR more severely than that of individual cell jitter, which adds incoherently. This difference is leveraged in the design of the CML clock buffer tree by locating all timing adjustment within each DAC cell, as shown in Fig. 12, minimizing its effect on global clock jitter. Additional improvements in SNR can be obtained by allocating more of the clock distribution to local clock buffers; however, this would significantly increase the power consumption of the chip and is thus avoided in this design. For the implemented 9 stage buffering, extracted simulation estimates a total RMS jitter of 0.63 ps, plotted in Fig. 12 for 1, 2, and 3 GHz operation.

IV. Measurement Results

The proposed ΔΣ DAC is fabricated in a C4-bumped 0.13 μm BiCMOS process and packaged flip-chip-on-board for testing. The 3 mm × 5 mm chip, pictured in Fig. 13, integrates fourteen LVDS receivers, the reconfigurable DSMs, the CML data path, and the interleaved 3 bit DAC core along with divide-by-two clock generation and digital SPI control. The test setup, shown in Fig. 14, utilizes a VC7215 Virtex 7 evaluation board to feed interleaved data samples into the DAC at double the on-chip data rate. The differential DAC output is taken from board mounted SMAs, converted to a single-ended output with a Picosecond Pulse Labs 5310A balun and measured using a spectrum analyzer.

In Fig. 15, the variable shaping of the on-chip DSM is demonstrated at a sample rate of 2 GS/s, showing first- and second-order shaping for the HP and both BP passbands. These outputs are attenuated by the sinc shaping of the DAC ZOH, resulting in a $\sim$10 dB attenuation of the second BP passband. Ideal second-order shaping highlights the in-band noise floor of the design which is limited by the jitter and nonlinearity of the DAC, folding noise back in-band. Fig. 16(a) shows a single tone output spectrum of the DAC at a sample rate of 2 GS/s and with second-order HP shaping. Since the design is implemented without reconstruction filtering, measurements are taken within the ΔΣ passband, a 100 MHz bandwidth (5% of f_S) in Fig. 16(a). The uncalibrated DAC exhibits an SIRR of 45.9 dB, with the image dominating the spurious-free dynamic range. To calibrate the DAC amplitude, the output power of each cell is measured off-chip and set to a common power reference while the timing of each cell is adjusted to minimize the system SIRR. After calibration, the DAC performance improves significantly, achieving an SFDR and SIRR of 76.2 dB, as well as an SNDR of 59.5 for a 0.997 GHz output. The SNDR performance correlates very well with the simulation results of Fig. 12, indicating that random jitter from the clock buffering is the dominating factor. Including 7 dB of measurement loss, an output power of -7.6 dBm is recorded, closely matching extracted simulation results. Within the same HP bandwidth, Fig. 16(b) shows a calibrated IM3 of -80.3 dBc from a two-tone test with 1 MHz spaced inputs. In Fig. 16(c) and (d), one- and two-tone tests are also shown for the second BP output. Within a 50 MHz bandwidth (2.5% of f_S), the calibrated DAC achieves an SFDR of 65.4 dB and in-band

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

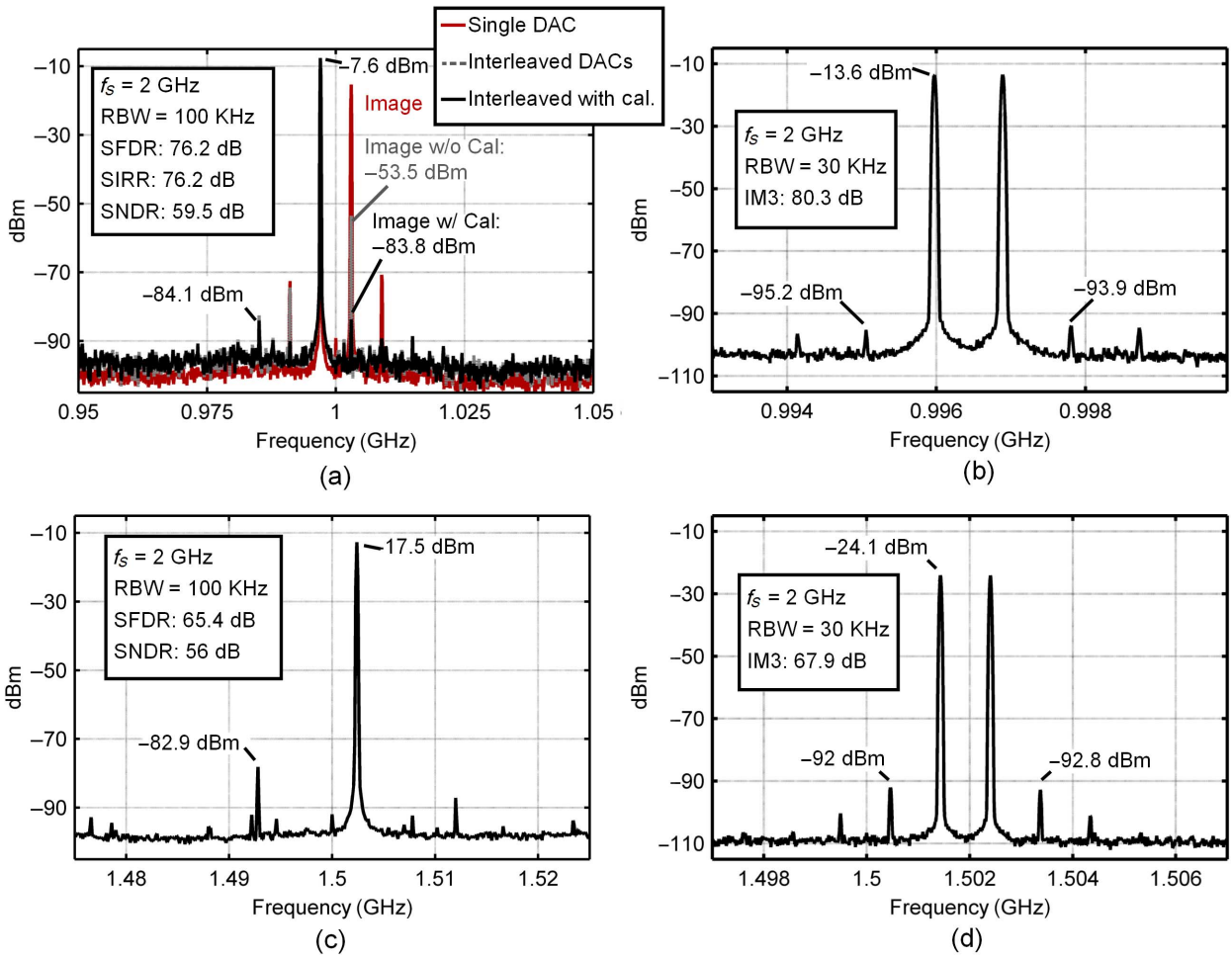

Fig. 16. Measured 100 MHz HP passband at 1.0 GHz showing (a) single- and (b) two-tone tests as well as the 50 MHz BP passband at 1.5 GHz with (c) single- and (d) two-tone tests. The results include a measurement loss of 7 dB.

SNDR of 56 dB while measuring an IM3 of −67.9 dBc. Note that the BP results are slightly degraded compared to the HP mode, due to the large ZOH attenuatation in the second Nyquist zone. In Fig. 17, a wideband plot of the second-order HP output is given. Over the 800 MHz bandwidth, the measured noise density is labeled at 100 MHz interverals and compares well to an ideal $\Delta\Sigma$ noise floor.

The performance of the DAC across sample rate for second-order HP modulation is shown in Fig. 18(a). Interleaving achieves a minimum SIRR of 73.5 dB due to accurate amplitude and timing calibration between each DAC. The SFDR performance remains above 65 dB up to an output frequency of 1.5 GHz. The IM3 is measured at a minimum of −80.2 dBc up to 1 GHz and increases to −67 dBc at 1.5 GHz. Fig. 18(b) shows the measured results of the BP modulation using the second passband, yielding an SFDR above 65 dB and IM3 better than −62 dBc across the frequency band.

In Fig. 19, the DAC sample rate is set to 3 GS/s, utilizing both the HP and BP output bands to synthesize 5 MHz WCDMA signals at 1.5 and 2.25 GHz, respectively. The DAC achieves an ACLR of −65.4 dBc in the HP mode and −59.3 dBc in the BP mode. Fig. 18(a) and (b) plots the DAC WCDMA ACLR performance across sample rate for a 5 MHz bandwidth in both

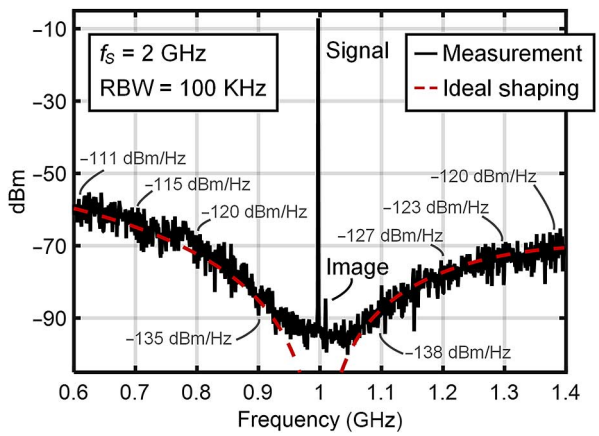

Fig. 17. Measured second-order HP output spectrum across an 800 MHz bandwidth at a sample rate of 2 GS/s. The noise density is labeled at 100 MHz steps, and ideal noise shaping is overlaid for reference.

the HP and BP passbands. In Fig. 18(b), the BP band is used at 2.6 GS/s to create a 1.95 GHz WCDMA output achieving an ACLR of −60.2 dBc. Fig. 20 shows the generation of a 20 MHz LTE signal at 1 GHz (HP, 2 GS/s) and 1.95 GHz (BP, 2.6 GS/s), yielding an ACLR of −66.4 and −59.2 dBc, respectively.

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

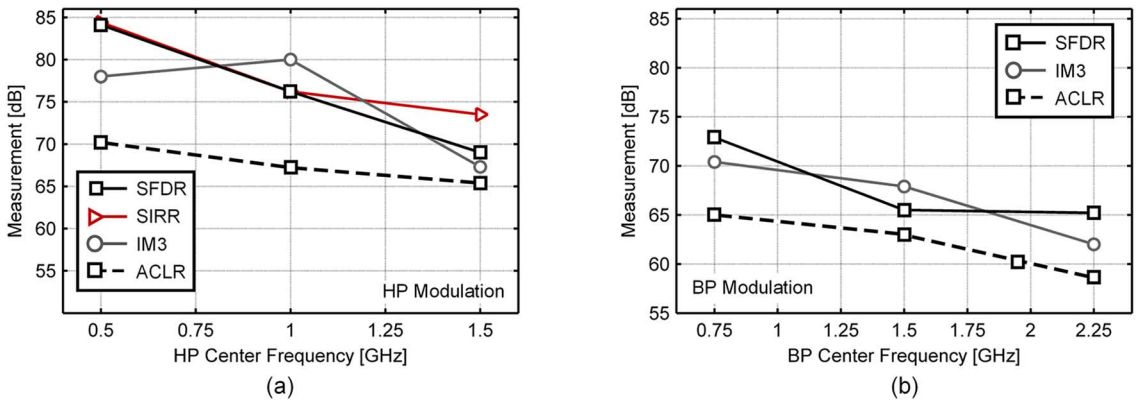

Fig. 18. DAC performance across varying passband frequencies for (a) HP mode and (b) BP mode.

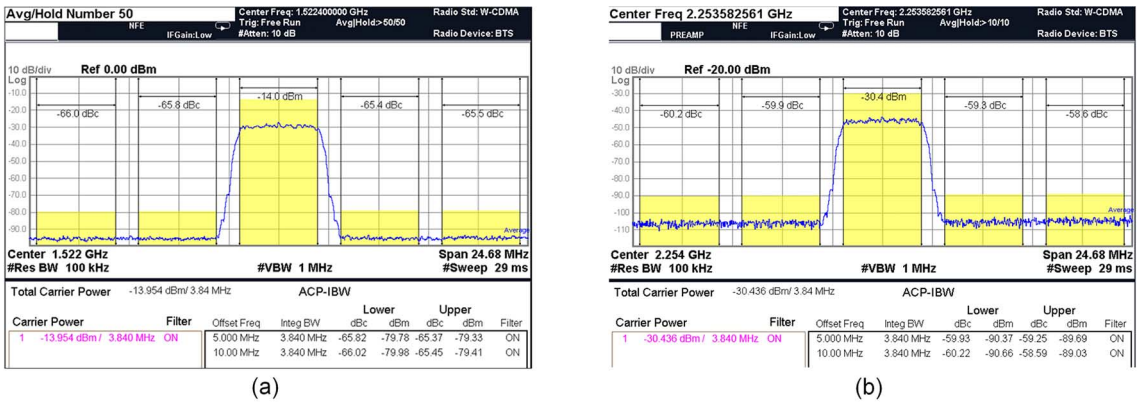

Fig. 19. ACLR of a 5 MHz WCDMA signal at 3 GS/s in the (a) 1.5 GHz HP band and (b) 2.25 GHz BP band.

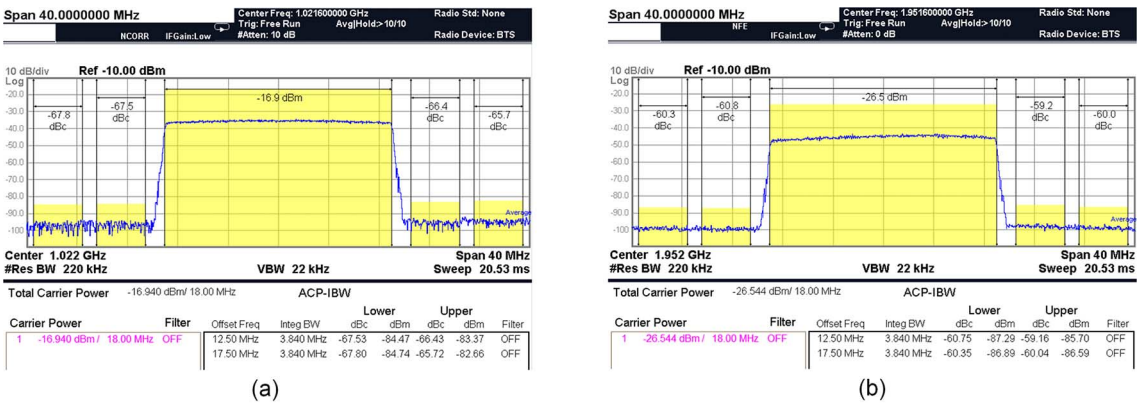

Fig. 20. ACLR of a 20 MHz LTE bandwidth in the (a) 1 GHz HP band and (b) 1.95 GHz BP band.

TABLE I
POWER CONSUMPTION AT 2 GS/S AND ACTIVE AREA BREAKDOWN OF CHIP BY FUNCTION

Block	Power at 2 GS/s (mW)	Area (mm^2)
DAC core (3.3 V)	53	0.255 mm^2
Retiming data path	174	0.130 mm^2
DSM (1.5 V)	109 (×2)	0.360 mm^2 (×2)
CML clocking (2.3 V)	342	–
LVDS receivers (1.8 V)	4 (×14)	0.0115 mm^2 (×14)
Total chip	843	15 mm^2

In Table I, the power consumptions of the primary functional blocks are given at 2 GS/s along with their respective layout areas. The 9 stage low-jitter CML buffers consume 342 mW with the layout distributed across chip while the two DSMs use a combined 218 mW. To meet the timing requirements of direct RF sampling, the DSM resolution and order were both pipelined, dramatically increasing power consumption. With technology scaling beyond 0.13 μm, the power of the DSMs and drivers is expected to drop considerably due to a lower supply voltage, reduced digital loading, and fewer pipelined stages. These expected improvements are highlighted by [23] and [24]

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

TABLE II
COMPARISON OF THE INTERLEAVED ΔΣ DAC WITH OTHER ΔΣ MIXING-DACS AND TRANSMITTERS

Ref.	Process Tech. [nm]	Arch.	ΔΣ Mod	Sample Rate (GS/s)	Output Freq. (GHz)	Output Power (dBm)	SFDR (dB)	IM3 (dBc)	SNDR (dB)	BW (MHz)	ACLR WCDMA /LTE (dBc)	Core Pwr. (mW)
[13]	180 CMOS	Mix. DAC	LP	0.514	0.942	–14.65	75	-70.8	53†	17.5	-/-	36
[14]	130 CMOS	Mix. DAC	LP	2.625	5.25	–8	52	–	49	200	-/-	10
[15]	250 CMOS	Mix. DAC	BP	0.25	1.062	–5.4	75	-64.7	72†	15	-/-	12.75
[20]	90 CMOS	Direct TX	LP	4.0	1.0	3.1	–	–	53.5	50	–53.6/-	71
			LP*	2.6	1.95	–8.6	–	–	46.5	30	–44.3/-	39
This work	130 SiGE BiCMOS	Direct TX	HP	2.0	1.0	–0.6‡	76.2	–80	59.5	100	–67.2/-66.4	53
				3.0	1.5	–5.5‡	69	–67.3	55.7	150	–65.4/-	
			BP*	2.0	1.5	–10.5‡	65.5	–67.9	56	50	–63.0/-	
				3.0	2.25	–16.6‡	65.2	–62	53.3	75	–59.3/-	

*Second Nyquist zone.
†SNR.
‡Measurement loss de-embedded (7 dB).

where 12 bit DSMs achieve 3.3 and 8 GS/s in 45 and 65 nm processes, consuming only 11 and 68 mW, respectively. Within the DAC, the low-distortion current cells consume 53 mW from a 3.3 V supply while the retiming path consumes 174 mW divided between a 1.5 V digital supply and a 2 V driver supply. The input LVDS consumes a total of 56 mW for all 14 input receivers.

Table II compares the interleaved ΔΣ DAC performance at 2 and 3 GS/s with other ΔΣ mixing-DACs and transmitters. Among the designs, the proposed architecture uniquely enables the use of HP ΔΣ modulation by suppressing the first DAC image below −76 dBc. For sample rates above 1 GS/s and bandwidths above 15 MHz, the proposed DAC exhbits the highest SFDR, IM3, and SNDR among previously reported ΔΣ DACs. Due to its excellent linearity, the highest WCDMA ACLR is achieved while first reporting an LTE ACLR of −66.4 dBc for a 1 GHz output.

V. CONCLUSION

An interleaved ΔΣ DAC is presented in this work, demonstrating reconfigurable RF synthesis via a high-speed low-resolution DAC fed with ΔΣ modulated data. Utilizing differential parallel data paths, the design cancels the first DAC image, leveraging the first and second Nyquist zones for RF output. The interleaved architecture facilitates the use of HP ΔΣ modulation by canceling the image replica that falls in-band, enabling the wide HP passband for RF output. The DAC can also be configured for BP modulation to enable signal generation in the first or second Nyquist zone. The implemented design utilizes per-cell amplitude and timing calibration to minimize mismatch, and leverages SiGe HBTs with CML drivers in the DAC data path to maximize linearity. The DAC is implemented in 0.13 μm SiGe technology and achieves an interleaved image cancelation above 76 dB with both BP and HP ΔΣ shaping. At a sample rate of 2 GS/s, the proposed design achieves an in-band SFDR of 76.2 dB, IM3 of −80 dBc, and SNDR of 59.5 dB over a 100 MHz bandwidth. The high spectral purity allows the DAC to generate WCDMA and LTE signals with an ACLR of −67.2 and −66.4 dBc, respectively, at 1 GHz. Compared with recently reported ΔΣ DACs, the results show the highest linearity performance when using sample rates greater than 1 GHz, and bandwidths greater than 15 MHz.

ACKNOWLEDGMENT

The authors would like to thank the Azimuth Industrial Company for their assistance with die attachment and PCB assembly.

REFERENCES

[1] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A multimode transmitter in 0.13 μm CMOS using direct-digital RF modulator," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.
[2] S. Balasubramanian *et al.*, "Ultimate transmission," *IEEE Microw. Mag.*, vol. 13, no. 1, pp. 64–82, Jan./Feb. 2012.
[3] P. Eloranta and P. Seppinen, "Direct-digital RF modulator IC in 0.13 μm CMOS for wide-band multi-radio applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 10, 2005, vol. 1, pp. 532–615.
[4] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A WCDMA transmitter in 0.13 μm CMOS using direct-digital RF modulator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 11–15, 2007, pp. 340–607.
[5] Z. Boos *et al.*, "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 20–24, 2011, pp. 376–378.

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

[6] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "9.6 A 5.3 GHz 16 b 1.75 GS/S wideband RF mixing-DAC achieving IMD<−82 dBc up to 1.9 GHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 22–26 2015, pp. 1–3.

[7] D. A. Mercer, "Low-power approaches to high-speed current-steering digital-to-analog converters in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1688–1698, Aug. 2007.

[8] W.-H. Tseng, C.-W. Fan, and J.-T. Wu, "A 12-bit 1.25-GS/s DAC in 90 nm CMOS with >70 dB SFDR up to 500 MHz," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2845–2856, Dec. 2011.

[9] H. Van de Vel *et al.*, "11.7 A 240 mW 16 b 3.2 GS/s DAC in 65 nm CMOS with <−80 dBc IM3 up to 600 MHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 9–13, 2014, pp. 206–207.

[10] W.-T. Lin, H.-Y. Huang, and T.-H. Kuo, "A 12-bit 40 nm DAC achieving SFDR > 70 dB at 1.6 GS/s and IMD <–61 dB at 2.8 GS/s with DEMDRZ technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 708–717, Mar. 2014.

[11] C.-H. Lin *et al.*, "A 12 bit 2.9 GS/s DAC with IM3 <−60 dBc beyond 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3285–3293, Dec. 2009.

[12] A. Bhide and A. Alvandpour, "An 11 GS/s 1.1 GHz bandwidth interleaved ΔΣ DAC for 60 GHz radio in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2306–2318, Oct. 2015.

[13] S. Luschas, R. Schreier, and H.-S. Lee, "Radio frequency digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, Sep. 2004.

[14] A. Jerng and C. G. Sodini, "A wideband ΔΣ digital-RF modulator for high data rate transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug. 2007.

[15] S. M. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A linear Σ-Δ digital IF to RF DAC transmitter with embedded mixer," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 5, pp. 1059–1068, May 2008.

[16] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, "A fully digital 65 nm CMOS transmitter for the 2.4-to-2.7 GHz WiFi/WiMAX bands using 5.4 GHz ΔΣ RF DACs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 3–7, 2008, pp. 360–619.

[17] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A wideband 2 × 13-bit all-digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 732–752, Apr. 2014.

[18] P. E. Paro Filho, M. Ingels, P. Wambacq, and J. Craninckx, "9.3 A transmitter with 10 b 128 MS/S incremental-charge-based DAC achieving –155 dBc/Hz out-of-band noise," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 22–26, 2015, pp. 1–3.

[19] J. Vankka, J. Sommarek, J. Ketola, I. Teikari, and K. A. I. Halonen, "A digital quadrature modulator with on-chip D/A converter," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1635–1642, Oct. 2003.

[20] A. Frappe, A. Flament, B. Stefanelli, A. Kaiser, and A. Cathelin, "An all-digital RF signal generator using high-speed ΔΣ modulators," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2722–2732, Oct. 2009.

[21] S. Balasubramanian *et al.*, "Systematic analysis of interleaved digital-to-analog converters," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 58, no. 12, pp. 882–886, Dec. 2011.

[22] J. J. McCue, B. Dupaix, L. Duncan, V. J. Patel, T. Quach, and W. Khali, "A time-interleaved multi-mode ΔΣ RF-DAC for direct digital-to-RF synthesis," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 17–19, 2015, pp. 103–106.

[23] P. Madoglio *et al.*, "A 2.5-GHz, 6.9-mW, 45-nm-LP CMOS, ΔΣ modulator based on standard cell design with time-interleaving," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1410–1420, Jul. 2010.

[24] A. Bhide, O. E. Najari, B. Mesgarzadeh, and A. Alvandpour, "An 8-GS/s 200-MHz bandwidth 68-mW ΔΣ DAC in 65-nm CMOS," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 60, no. 7, pp. 387–391, Jul. 2013.

[25] S. Su, T.-I. Tsai, P. K. Sharma, and M. S.-W. Chen, "A 12 bit 1 GS/s dual-rate hybrid DAC with an 8 GS/s unrolled pipeline delta-sigma modulator achieving >75 dB SFDR over the Nyquist band," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 896–907, Apr. 2015.

[26] P. Seddighrad, A. Ravi, M. Sajadieh, H. Lakdawala, and K. Soumyanath, "A 3.6 GHz, 16 mW ΣΔ DAC for a 802.11n/802.16e transmitter with 30 dB digital power control in 90 nm CMOS," in *Proc. 34th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 15–19, 2008, pp. 202–205.

[27] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2005. [Online]. Available: https://cds.cern.ch/record/733538

[28] S. Ralph and R. Farrell, "Using high pass sigma-delta modulation for class-s power amplifiers," in *Proc. 18th Eur. Conf. Circuit Theory Des. (ECCTD)*, Aug. 2007, pp. 707–710.

[29] J. Deveugele, P. Palmers, and M. S. J. Steyaert, "Parallel-path digital-to-analog converters for Nyquist signal generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1073–1082, Jul. 2004.

[30] A. Bhide, A. Ojani, and A. Alvandpour, "Effect of clock duty-cycle error on two-channel interleaved ΔΣ DACs," *IEEE Trans. Circuits Syst. II Exp. Briefs*, vol. 62, no. 7, pp. 646–650, Jul. 2015.

[31] A. K. Ong and B. A. Wooley, "A two-path bandpass ΣΔ modulator for digital IF extraction at 20 MHz," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1920–1934, Dec. 1997.

[32] J. W. Archer, J. Granlund, and R. E. Mauzy, "A broad-band VHF mixer exhibiting high image rejection over a multidecade baseband frequency range," *IEEE J. Solid-State Circuits*, vol. 16, no. 4, pp. 385–392, Aug. 1981.

[33] R. J. Drost, R. D. Hopkins, R. Ho, and I. E. Sutherland, "Proximity communication," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1529–1535, Sep. 2004.

[34] N. E. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed. Reading, MA, USA: Addison-Wesley, 2005, ch. 10, sec. 2, pp. 638–678.

[35] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, Feb. 1989.

[36] A. Van Den Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," in *Proc. 6th IEEE Int. Conf. Electron. Circuits Syst.*, 1999, vol. 3, pp. 1193–1196.

[37] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, Dec. 1998.

[38] S. Luschas and H. S. Lee, "Output impedance requirements for DACs," in *Proc. Int. Symp. Circuits Syst. (ISCAS'03)*, vol. 1, May 25–28, 2003, pp. I-861–I-864.

[39] G. Van Der Plas, J. Vandenbussche, W. Sansen, M. Steyaert, and G. Gielen, "A 14-bit intrinsic accuracy Q2 random walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1708–1718, Dec. 1999.

[40] B. Oyama, D. Ching, K. Thai, A. Gutierrez-Aitken, and V. Patel, "InP HBT/Si CMOS-based 13-b 1.33-Gsps digital-to-analog converter with >70-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2265–2272, Oct. 2013.

[41] C.-H. Lin *et al.*, "A 12 bit 2.9 GS/s DAC with IM3 <<−60 dBc beyond 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3285–3293, Dec. 2009.

[42] K. Doris, A. van Roermund, and D. Leenaerts, "A general analysis on the timing jitter in D/A converters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2002, vol. 1, pp. I-117–I-120.

[43] J. Bastos, A. Marques, M. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959–1969, Dec. 1998.

Jamin J. McCue (S'10–M'16) received the B.S.E.E. degree from Cedarville University, Cedarville, OH, USA, in 2009, and the M.S. and Ph.D. degrees from The Ohio State University, Columbus, OH, USA, in 2014 and 2015, respectively.

During his time at the ElectroScience Laboratory, The Ohio State University, his research included high-speed and interleaved D/A converters, low-power serial communications, and mm-wave IC design. He holds one patent and has authored/coauthored more than 10 conference and journal publications. He is currently with Northrop Grumman Mission Systems, Baltimore, MD, USA, where he is a Senior RF Engineer.

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply

Brian Dupaix (M'12) received the B.S. degree in electrical and computer engineering from Brigham Young University, Provo, UT, USA, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from The Ohio State University, Columbus, OH, USA, in 2009 and 2013, respectively.

In 2013, he joined the ElectroScience Laboratory (ESL), The Ohio State University, where he is currently a Research Scientist. During his time at ESL, he has worked on high-speed DACs, heterogeneous semiconductor power-amplifiers, wideband simultaneous-transmit-and-receive systems, and mixed-signal reliability analysis platforms. Prior to joining the ESL, he spent five years at Honeywell Air Transport Systems, Phoenix, AZ, USA, where he designed ASICs for flight and navigation computers for commercial aircraft, and four years at Intrinsix, Marlborough, MA, USA, where he generated IP blocks for extensible processors and system-on-chip ASICs for consumer electronics. He was also an Independent Design Consultant for eight years, working on trusted circuit analysis, wireless sensor networks, low power RADAR systems, RFID ASICs, and digital control of multichannel RF systems. He holds one patent. His research interests include direct digital-to-RF circuits, high-performance mixed signal circuits, heterogeneous semiconductor integrated circuits, and trusted electronic components.

Dr. Dupaix was the recipient of the Honeywell Technical Achievement Award in 2001 for his work on a cycle-accurate ASIC implementation of a full-custom microprocessor.

Lucas Duncan (M'08) received the B.S. and M.S. degrees in electrical and computer engineering from The Ohio State University, Columbus, OH, USA, in 2009 and 2012, respectively, where he is currently pursuing the Ph.D. degree.

His research interests include the design of analog, mixed-signal, and RF circuits.

Brandon Mathieu (S'16) received the B.S.E.C.E. (*magna cum laude*) and M.S. degrees from The Ohio State University, Columbus, OH, USA, in 2014 and 2015, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

He works closely with the Air Force Research Laboratory, Sensors Directorate, Wright Patterson AFB, OH, USA. His research interests include reconfigurable RF circuits and systems, mixed-signal design, and direct digital synthesis.

Mr. Mathieu received the DAGSI fellowship in 2014 and 2015.

Samantha McDonnell (S'10) received the B.S. and M.S. degrees in electrical engineering from The Ohio State University, Columbus, OH, USA, in 2008 and 2010, respectively, where she is currently pursuing the Ph.D. degree in electrical engineering.

She interned with the Air Force Research Laboratory, Dayton, OH, USA, in the summers of 2011–2014. Her research interests include calibration of high-speed digital-to-analog converters, time-based analog-to-digital converters, and delta-sigma modulators.

Ms. McDonnell received the SRC fellowship in 2008, DAGSI fellowship in 2010, and the four-year SMART fellowship in 2011.

Vipul J. Patel (S'97–M'13–SM'14) received the B.S. degree in electrical engineering and the M.S. degree in computer engineering from the University of Cincinnati, Cincinnati, OH, USA, in 2001 and 2006, respectively.

He was a Design and Process Engineer with the Maxim Integrated, Dallas, TX, USA, where he worked on CMOS timing circuit chipsets and submicron CMOS process development from 1998 to 2001. He is currently a Mixed-Signal Designer with the Sensors Directorate, Air Force Research Laboratory (AFRL), Wright-Patterson Air Force Base, Dayton, OH, USA. He is also an AF Technical Consultant and Point of Contact to the Defense Advanced Research Project Agency (DARPA), Washington, DC, USA. He has authored/coauthored more than 20 conference and refereed journal articles and 1 book chapter. His research interests include radio frequency and millimeter-wave integrated circuits and systems, high-performance clocking circuits and data converters, and reconfigurable radio hardware.

Tony Quach received the B.S.E.E. degree from Wright State University, Dayton, OH, USA, in 1988 and the M.S.E.E. degree from University of Dayton, Dayton, OH, USA, in 1994.

Since 1989, he has been involved with the research and development of solid-state microwave devices and integrated circuits at the Air Force Research Laboratory, Sensors Directorate, Wright Patterson AFB, OH, USA. He has led the research in the development of miniature digital receiver/exciter (MDREX) system on-a-chip (SOC) employing the advanced 130 nm silicon germanium (SiGe) BiCMOS technology. He is currently a Principal Researcher at AFRL engaging in the research and development of reconfigurable RF devices, components and systems for next generation phased-array applications. He has authored or coauthored more than 50 publications and holds 12 patents on microwave devices and circuits.

Waleed Khalil (SM'12) received the B.S.E.E. and M.S.E.E degrees from the University of Minnesota, Minneapolis, MN, USA, in 1992 and 1993, respectively, and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2008.

He is currently serving as an Associate Professor with the ECE Department and the ElectroScience Laboratory, The Ohio State University (OSU), Columbus, OH, USA. Prior to joining OSU, he spent 16 years at Intel Corporation, Chandler, AZ, USA, where he held various technical and leadership positions in Wireless and Wireline Communication Groups. While at Intel, he was appointed as the Lead Engineer at the Advanced Wireless Communications Group, where he played an instrumental role in the development of the industry's first analog front-end IC for third generation radios. He later co-founded a startup group to develop Intel's first RF front-end IC, as a Principle Leader of the radio transmitter chain. He has authored 12 issued and several other pending patents, over 70 journal and conference papers and 3 books/book chapters.

Dr. Khalil serves as an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and as a Steering and TPC Committee Member for the RFIC and CSIC Symposiums. He was the recipient of the Prestigious Intel Quality Award in 2005, during his work at Intel. His research group has received several paper awards, among them TSMC's Outstanding Research Award in 2010 and the Best Paper Award in the Wireless Innovation Forum and Phase Array Symposium in 2013.

Authorized licensed use limited to: NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS. Downloaded on January 07,2025 at 14:44:37 UTC from IEEE Xplore. Restrictions apply