A 0.13 µm CMOS 0.1-20 MHz Bandwidth 86-70 dB DR Multi-Mode DT $\Delta\Sigma$ ADC for IMT-Advanced

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***Abstract*— This paper presents a reconfigurable tri-level/multi-bit multi-mode $\Delta\Sigma$ modulator implemented in 0.13 µm CMOS. The modulator covers between 0.1 MHz and 20 MHz signal bandwidth which makes it suitable for cellular applications including 4G radio systems, also known as IMT-Advanced. With a maximum sampling rate of 400 MHz, the modulator achieves between 86 dB and 70 dB DR for 100 kHz and 20 MHz signal bandwidth, respectively, at a scalable power consumption between 2 mW and 34 mW from a 1.2 V supply, including the reference buffer.**

I. Introduction

Recent popularity of smart phones, netbooks, and other mobile broadband devices has vindicated 3G (WCDMA/HSPA) as an enabling technology and has given fresh impetus to its successor LTE, which many operators have started to deploy recently. Evolutions beyond LTE, notably IMT- and LTE-Advanced, are also being developed at standards bodies such as the International Telecommunication Union (ITU-R) and the 3rd Generation Partnership Project (3GPP), which provide roadmaps to 1 Gbps downlink data rate for stationary and 100 Mbps for mobile operation. The technology components defined by IMT-Advanced include extended spectrum flexibility to support scalable bandwidths between 5 MHz and 40 MHz [1], while LTE-Advanced even aims at bandwidths up to 100 MHz [2].

Scalable bandwidths and compatibility to legacy 3GPP standards such as WCDMA/HSPA and GSM/EDGE continue to be the strength of the family of standards. They are however contingent on highly integrated, multi-mode radios at low cost for their success. Availability of low power multi-mode ADCs for IMT- and LTE-Advanced bandwidths, for example, features prominently in the discussions of those standards today.

Above 20 MHz RF bandwidth (10 MHz bandwidth at baseband) and more than 10 bit resolution, there have not been many reports of ADCs at power consumption commensurate with cellular mobile terminals [3], [4], even for those optimized for a specific combination of sampling frequency and resolution [5], [6]. For multi-mode cellular ADCs the challenges are stiffer towards LTE and beyond, as the extremes of narrow-band highest resolution at very low power and broadband moderately high resolution low power further stretch the design to the limit. In this contribution we present such a GSM/EDGE-up-to-IMT-Advanced multi-mode $\Delta\Sigma$ ADC, that reaches 20 MHz signal bandwidth, which corresponds to 40 MHz bandwidth at RF, and 11 bit resolution at only 34 mW, occupying almost a quarter of the die-area compared to prior art [5].

II. System Considerations

While the bandwidths of such an ADC used in a wireless receiver are given by the standards it supports, the required resolution is determined by the required SNR for decoding, the peak-to-average ratio (PAR) of the modulated signal, residual blockers which has not been filtered by the baseband filter, and the margin between the receiver noise and the ADC noise floor [7]. The required SNR for decoding can be as high as 30 dB like in the case of EDGE, and the PAR is 0/3 dB for GSM/EDGE, respectively, and about 12 dB for CDMA and OFDM communication systems. The noise margin is chosen to be 12 dB, which is large enough to keep the degradation of the total receiver noise figure (NF) below 0.2 dB.

The amplitude of residual blockers depends on the amount of filtering provided by the receive chain, resulting in a trade-off between channel filtering and ADC resolution. Assuming a 3rd-order baseband filter for low EVM and about 50 dB programmable gain range in the receive chain, 13-14 bit ADC resolution is required for GSM/EDGE, 11-12 bit for WCDMA/HSPA and 10-11 bit for LTE, which already incorporates many of the features of IMT- and LTE-Advanced. The latter's high data rates in 20 MHz bandwidth may require a somewhat higher SNR for decoding than LTE, so that 11 bit resolution is anticipated.

III. $\Delta\Sigma$ Modulator Architecture

A. Multi-Mode $\Delta\Sigma$ Modulator

The discrete-time (DT) $\Delta\Sigma$ modulator lends itself well to a multi-mode ADC because its loop filter, hence signal bandwidth, scales with the sampling frequency. The sampling frequency is however a limiting factor when the desired signal bandwidth reaches 20 MHz as in the case of IMT-/LTE-Advanced, where it needs to be as high as 400 MHz just to achieve a modest OSR of 10, which in turn requires amplifiers with more than 2 GHz bandwidth. In addition to amplifier optimization for high speed, the $\Delta\Sigma$ modulator architecture plays the most crucial role in pushing the limit at the upper

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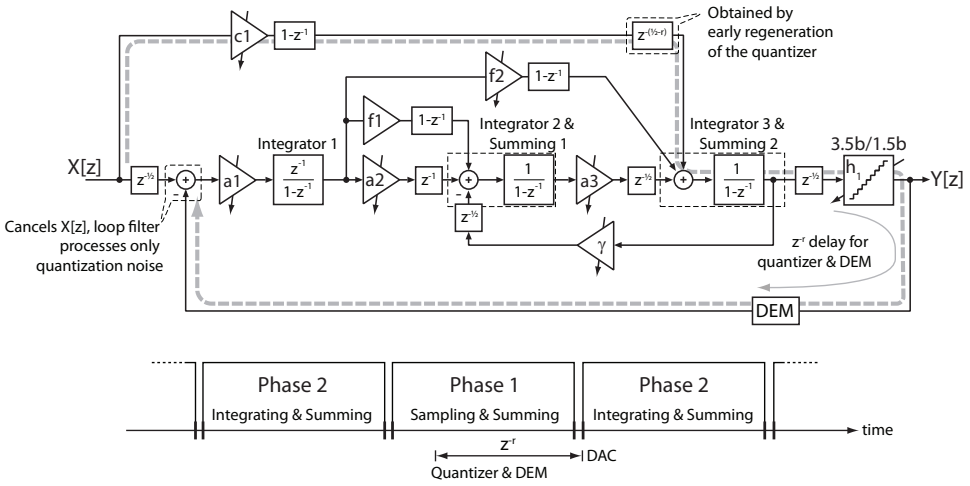

Fig. 1. Block and timing diagram of the $\Delta\Sigma$ modulator.

end of the signal bandwidth range (spanning a factor of 200), while keeping performance optimal for all legacy standards supported.

Figure 1 shows the single-loop, 3rd-order architecture adopted in this design, saving an amplifier, which is used for active summing of the feedforward paths, compared to our previous multi-mode modulator to allow more current into the remaining op-amps and doubling of the speed [4]. To cover a wide spread of bandwidth and resolution with a single topology is challenging as the thermal noise scales differently with the OSR than the modulator's quantization noise [5], and the latter should be kept 10-15 dB below the former for best power efficiency. This is achieved by making the number of quantization levels programmable in Fig. 1 to better adapt the modulator's noise-shaping property to the different modes. For those modes with high OSRs the tri-level quantizer is generally used, and 3.5 bit operation is introduced for modes with low OSRs. The loop filter transfer function is also made programmable according to the quantizer levels used, in order to optimize performance while maintaining stability. The transfer functions are designed to share as many filter coefficients as possible, and programmability is mainly realized by the switched-capacitor (SC) integrator feedback capacitors, as shown in Fig. 3. Note that only the single-ended version is shown in Fig. 3, although all of the circuits use differential signals. A programmable notch is further introduced in the noise transfer function (NTF) and placed at the edge of the signal band to optimize performance in each mode, as depicted in Fig. 2.

B. Loop Filter Implementation

A direct feedforward path, successfully deployed in our previous multi-mode modulator [4], helps to achieve low internal signal-swings and consequently low distortion by cancelling the signal component at the input of the first integrator. This however requires the round-trip delay via the forward path, quantizer, and DAC back to the first integrator of the loop (indicated by the dashed arrow in Fig. 1) to be less than half a clock cycle, which typically leaves only the gap between two clock phases (rather the non-overlap time) for the quantizer to regenerate, thus creating a speed bottleneck. The present design therefore imbeds the summing of the feedforward paths with the SC integrator outputs (Fig. 3) into the integrator stages, to allow the quantizer to regenerate a fractional phase (z^r) earlier than the full clock phase 2 required for the integrator's charge transfer. The resulting timing of the quantizer is illustrated in Fig. 1. Early regeneration of the quantizer relaxes the timing requirements of the quantizer and the dynamic element matching (DEM) logic for the faster LTE-Advanced mode. The introduction of z^r into the direct feedforward path of the modulator however modifies the signal transfer function (STF) to

$$\mathrm{STF} = 1 - \mathrm{NTF} \cdot \left(1 - z^{-r}\right). \tag{1}$$

The advance of quantizer regeneration (z^{-r} as marked in Fig. 1) is therefore chosen as short as the quantizer speed would allow to limit any peaking in the STF as a result of introducing z^r into the modulator loop. To ensure reliable timing over process and temperature variations the clock phases for the quantizer are generated by a digital DLL, as

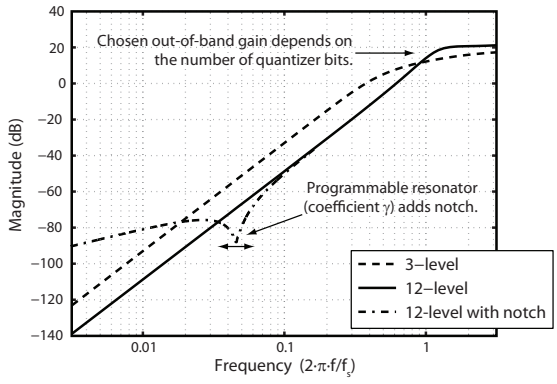

Fig. 2. NTF of the implemented $\Delta\Sigma$ modulator.

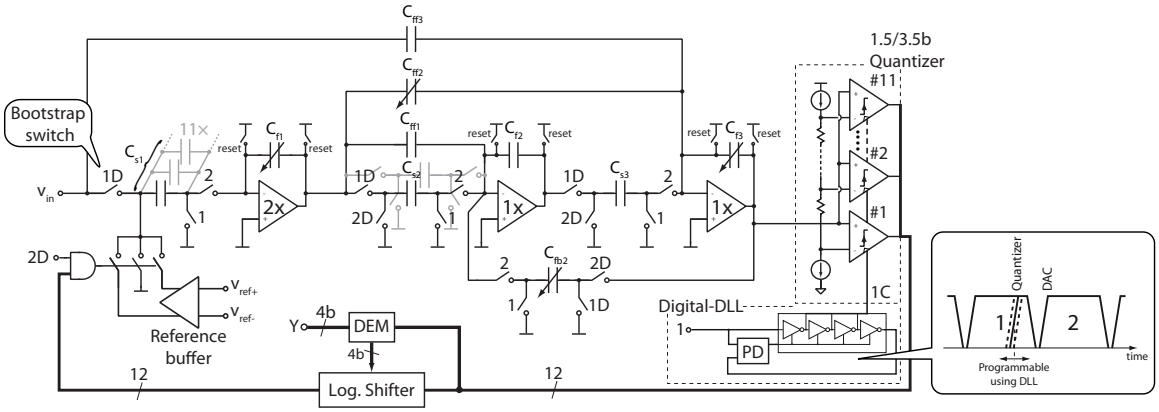

Fig. 3. Schematic diagram (single-ended version) and comparator timing.

shown in Fig. 3. The DLL is enabled at start-up only, and its digital implementation requires very little die-area and power consumption.

IV. Circuit Implementation

Due to the low internal signal-swings, power-efficient telescopic cascode amplifiers can be used even at 1.2 V supply voltage. In order to minimize distortion resulting from non-linear amplifier gain, regulated cascoding is incorporated in the amplifier. The amplifiers are designed to maximize speed in the IMT-/LTE-Advanced mode, but their bandwidth can be programmed via the bias current to reduce power consumption for modes with lower data rates.

Bootstrapping is used for the input sampling switches to maintain high linearity [8]. In the remaining integrator stages, transmission gates with NMOS and PMOS transistors, having their size optimized for linearity, are used. The switches connected to the amplifier inputs are simple NMOS transistors.

The quantizer is built up of eleven comparators, of which nine comparators are powered down for tri-level operation. The implemented comparators also feature programmable power consumption according to the selected mode. Each comparator consists of a differential difference amplifier (DDA) to perform comparison with the different voltage references, followed by a dynamic latch. Small input transistors are used to limit the loading of the comparators to the last integrator stage of the loop, and the resulting large comparator offsets are automatically trimmed with programmable current sources at start-up by digital calibration logic [6].

Also incorporated on-chip is a reference buffer for the voltage references of the DAC. A slow reference buffer approach is adopted where fast settling within less than 1.2 ns at low power consumption is achieved for the fast IMT-/LTE-Advanced mode by using a single external capacitor.

A serial peripheral interface (SPI) is incorporated on the chip for programming the ADC, and providing test functionality to the DLL and the digital calibration logic of the quantizer.

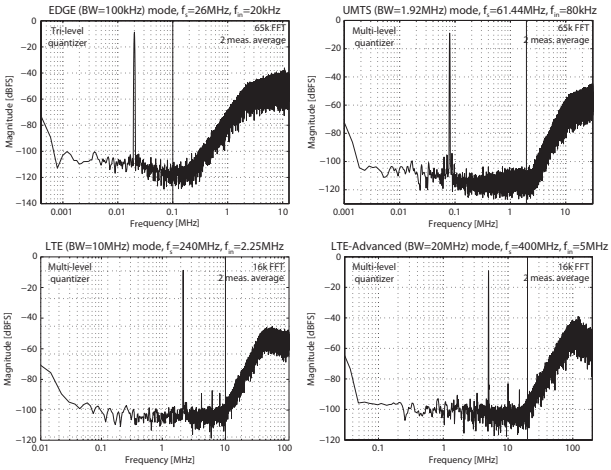

Fig. 4. Measured FFT output spectra at -6 dBFS.

V. Measurement Results

Implemented in a 0.13 µm CMOS technology the multi-mode $\Delta\Sigma$ modulator occupies 0.27 mm^2, excluding the SPI. Measurement results for EDGE-, UMTS-, and LTE-(Advanced)modes with (RF) channel bandwidths of 10/20/40 MHz, including the output spectra shown in Fig. 4, validate the modulator's flexibility, setting another benchmark in multi-mode performance. Note that the signal frequencies in Fig. 4 are dictated by external bandpass filters to remove the harmonics of the signal source. In Fig. 5 the measured SNDR is plotted versus the input signal for the various modes, where the dynamic range is 86 dB for EDGE, 77 dB for UMTS and 75/71/70 dB for LTE(-Advanced) with 10/20/40 MHz (RF) channel bandwidth, respectively. The achieved figure-of-merit (FOM) is 0.28 pJ/conv in UMTS-mode, one of the lowest reported for DT $\Delta\Sigma$ modulators. For the other modes, the FOM is still $\leq$0.9 pJ/conv, competitive compared to existing single-mode modulators despite being disadvantaged by multi-mode requirements. The overall circuit performance is summarized in Tab. I and the chip micrograph is shown in Fig. 6.

TABLE I

SUMMARY OF MEASURED PERFORMANCE.

Process	0.13 µm 1P6M CMOS, 1.2 V supply				
Core area	0.27 mm^2 (without SPI)				
Signal bandwidth	100 kHz – 20 MHz				
Sampling frequency	26 MHz – 400 MHz				
DR	70.4 dB – 86.8 dB				
Power consumption	2 mW – 34.7 mW (including the reference buffer)				
(Possible) Modes	**EDGE**	**UMTS**	**LTE(-Advanced)**		
Signal bandwidth	**100 kHz**	**1.92 MHz**	**5 MHz**	**10 MHz**	**20 MHz**
Sampling frequency	26 MHz	61.44 MHz	160 MHz	240 MHz	400 MHz
DR	86.8 dB	77.1 dB	75.4 dB	71.0 dB	70.4 dB
Peak SNR	85.3 dB	75.7 dB	72.2 dB	68.7 dB	66.9 dB
Peak SNDR	82.5 dB	75.2 dB	70.9 dB	66.0 dB	64.4 dB
Peak SFDR	100.9 dB	91.2 dB	91.2 dB	84.8 dB	83.9 dB
Power consumption	2 mW	5.2 mW	13.6 mW	20.2 mW	34.7 mW
FOM[1]	0.9 pJ/conv	0.28 pJ/conv	0.47 pJ/conv	0.6 pJ/conv	0.6 pJ/conv

[1] $\text{FOM} = \dfrac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{\frac{\text{SNDR}-1.76}{6.02}}}$

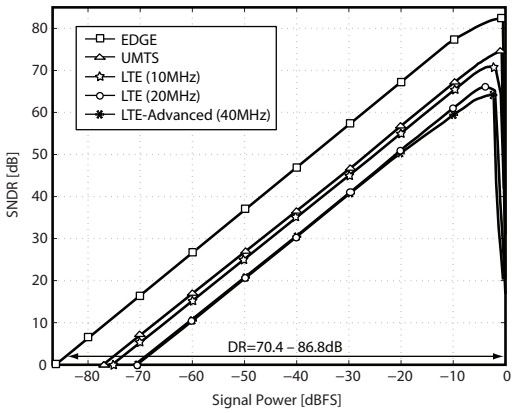

Fig. 5. Measured SNDR curves.

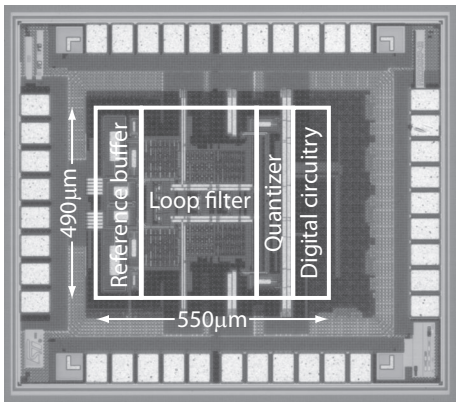

Fig. 6. Chip micrograph.

VI. CONCLUSION

A highly flexible multi-mode $\Delta\Sigma$ ADC has been presented that covers bandwidths between 100 kHz and 20 MHz which makes it suitable for GSM/EDGE-up-to-IMT-Advanced multi-standard scenarios. A loop filter topology has been proposed which imbeds the summing of the feedforward paths into the SC integrator stages to save power, reduce die-area, and increase the maximum sampling frequency. To achieve optimum performance in each mode the number of quantizer levels is programmable, resulting in low power consumption which is reflected in a FOM as low as 0.28 pJ/conv in UMTS mode, including an on-chip reference buffer. With a measured DR between 14.1 bit and 11.4 bit for GSM/EDGE and LTE-Advanced, respectively, and a SFDR over 100 dB in EDGE mode, the presented $\Delta\Sigma$ ADC achieves a high DR with excellent linearity which is in concurrence with the trend in multi-standard receiver design to increase the programmability by pushing more functionality into the digital domain.

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