A 69.8 dB SNDR 3rd-order Continuous Time Delta-Sigma Modulator with an Ultimate Low Power Tuning System for a Worldwide Digital TV-Receiver

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***Abstract*- This paper presents a 3rd-order continuous time delta-sigma modulator for a worldwide digital TV-receiver whose SNDR is 69.8 dB. An ultimate low power tuning system using RC-relaxation oscillator is developed in order to achieve high yield against PVT variations. A 3rd-order modulator with modified single opamp resonator contributes to cost reduction by realizing very compact circuit. The mechanism to occur 2nd-order harmonic distortion at current feedback DAC was analyzed and a reduction scheme of the distortion enabled the modulator to achieved FOM of 0.18 pJ/conv-step.**

I. Introduction

Recently, market of silicon TV-tuners is growing rapidly. Instead of an old type can-tuner, the silicon TV-tuner emerges at center stage, because the tuner can add TV function to many portable devices due to its very compactness and less power consumption.

In designing the TV-tuner circuits, analog-to-digital converter (ADC) is very important. The ADC with high SNDR can alleviate requirements to both filter and AGC before the ADC by using digital post filter to remove interference signals. A delta-sigma modulator is quite suitable for this application because the over sampling modulator is easy to realize high SNR as compared with other kinds of ADCs, such as pipeline-ADCs or successive approximation ADCs.

To reduce power consumption, the over sampling ratio of the modulator tends to be low. Thus the noise transfer function should have zeros in the signal band to enhance the SNR. We have already developed a 5th-order delta-sigma modulator which has enough bandwidth for TV-tuners[1]. However, the modulator has issues on circuit area and SNDR performances.

In this paper, we propose a very compact delta-sigma modulator with SNDR of 69.8 dB and bandwidth of 4 MHz. New type single opamp resonator has been developed for compact layout. In order to enhance SNDR, the mechanism of the 2nd-order harmonic distortion has been analyzed.

Although the order of the modulator is decreased from 5 to 3 for the compactness, the SNDR of the new modulator is superior to the previous version.

In addition, this paper describes the ultimate low power tuning system of the modulator, which uses an RC-relaxation oscillator. In a continuous time delta-sigma modulator, process variation degrades both SNR and stability. In order to overcome process variation, we have developed a new tuning system which uses an RC-relaxation oscillator[2] for tuning time constants of the modulator. The frequency to be calibrated is drastically reduced, because an RC filter is less sensitive to both temperature and supply voltage variations as compared with a Gm-C filter. In this paper, system overview is described in Section II. The design of the new single opamp resonator is detailed in Section III. A reduction scheme of the harmonic distortion is explained in Section IV. Measured circuit performances of the modulator are summarized in Section V. and conclusion is made in Section VI.

II. System Overview

Figure 1(a) shows the schematic of a 3rd-order delta-sigma modulator and Fig.1(b) shows that of an RC-relaxation oscillator with power averaging feedback (PAF), respectively.

A. RC-Relaxation Oscillator

We adopted the RC tuning to keep frequency response of the modulator constant because the RC time constant is more stable against disturbances as compared with the Gm-C constant and has less sensitivity to both temperature and supply voltage variations. Thus, RC tuning is needed only once before an operation of the modulator and zero power consumption can be realized at the ADC operation.

An oscillation frequency of the relaxation oscillator only depends on the RC time constant because of the power averaging feedback concept[2].

In Fig.1(b), the oscillation waveform under $R_1 >> R$ is

$$V_{osc1,2}(t) = V_{dd}\left(1 - e^{-\frac{1}{RC}t}\right). \quad (1)$$

PAF loop equalizes the averaged waveform with the reference generated by the resistive divider of V_{dd} like as

$$\frac{1}{T_{osc}}\int_0^T V_{osc1,2}(t)dt = V_{ref}\ . \quad (2)$$

Finally, we obtain the following simplified equation of

$$(1-\alpha)\left(T_{OSC}/RC\right) = 1 - e^{-\left(T_{OSC}/RC\right)}, \quad \text{where } \alpha = \frac{V_{ref}}{V_{dd}}\ . \quad (3)$$

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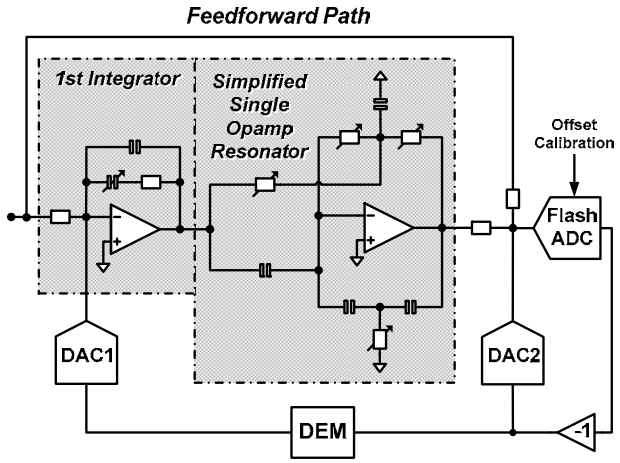
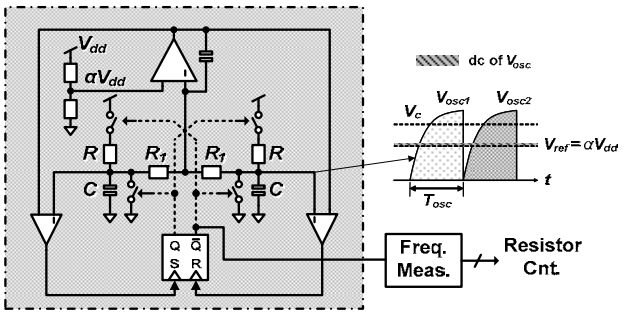


(a) Schematic of the 3rd-order modulator



(b) Schematic of the RC-relaxation oscillator with power averaging feedback

Fig.1 Circuit schematics of the modulator with tuning system

Equation(3) indicates that the oscillation period can be invariant against V_{dd}.

In this case the variation of the oscillation frequency is within ±1%. The oscillation frequency is measured using a counter driven by reference clocks and the RC time constants of the modulator are set according to the measurement result.

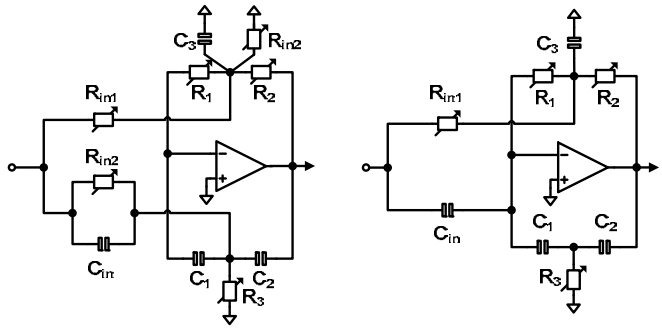
B. Modulator

The goal of this system is to put itself into a commercially-based TV-Receiver. Thus the system is required high reliability as well as low cost and low power operation. Third order modulator is adopted because feedback loop is more stable as compared with 5th-order modulator. In addition, both area reduction and lowering power consumption are expected.

In Fig.1(a), a 3rd-order modulator is composed of a 1st integrator and a 2nd resonator. The resonator needs only one opamp, thus it is called as "single opamp resonator"[1]. In this case, the resonator is modified so that the number of resistors is minimized in order to reduce circuit area and complexity

In order to achieve SNDR above 65dB, the loop gain has to be high so that the quantization noise is suppressed effectively. Thus, two stage opamps are adopted.

A three bit flash ADC with offset calibration and a dynamic element matching (DEM) technique are adopted for reducing harmonic distortion in output digital codes. The dominant mechanism to generate 2nd-order harmonic distortion is detailed in section IV.



(a) Conventional resonator (b) New simplified resonator

Fig.2 Comparison of resonators

III. Design of Simplified Resonator

We have devised a resonator for low power and small area. Figures 2(a) and (b) show the conventional[1] and the proposed resonators, respectively. The new resonator forms simplified architecture and the transfer function is calculated as the following equation.

$$V_{out} = -\frac{\left(\frac{s^2 C_{in} C_3}{C_1 C_2} + \frac{sC_{in}}{C_1 C_2 R_3} + \frac{1}{C_1 C_2 R_{in} R_1}\right)}{s^2 + \frac{1}{C_1 C_2 R_1 R_2}}. \quad (4)$$

The resonance condition is described as (5).

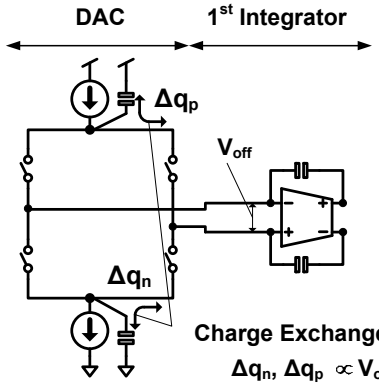
$$\begin{cases} C_3 = C_1 + C_2 \\ R_3 = \dfrac{1}{1/R_1 + 1/R_2 + 1/R_{in}} \end{cases}. \quad (5)$$

Although all terms of the transfer function are not independent one another, the proposed resonator has two benefits: resistive load of the first integrator is lighter than the previous version, and the number of resistors to be calibrated is decreased.

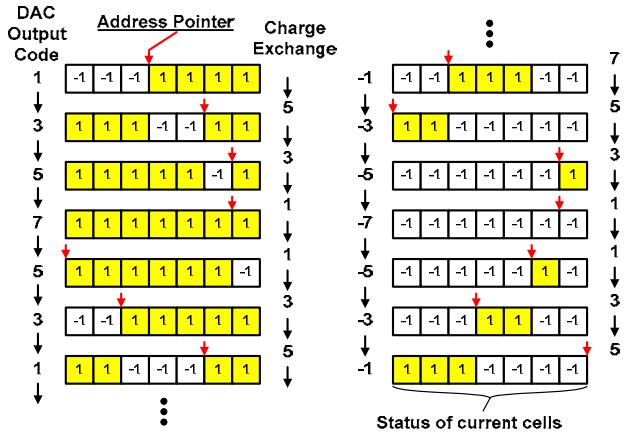
IV. Reduction of The Harmonic Distortion

In order to reduce the harmonic distortion, we have found out occasions of that. One reason is the unevenness of the quantization levels and the other is the offset of the 1st integrator.

The dominant source of the distortion is the interaction between the offset of the 1st integrator and parasitic capacitances of DAC current sources as shown in Fig.3(a). Figure 3(b) depicts the distortion mechanism. The numbers in the rectangles mean sign of the current cell. In this case we use 1st-order data weighted averaging as a DEM algorithm. Error charge is injected to the integrator at each switching of current cells. Thus the charge exchange of parasitic capacitances has a dependency on data patterns. In Fig.3(b), numbers at left side



(a) Occasions of the 2nd-order harmonic distortion



(b) 2nd-order harmonic distortion mechanism

Fig.3 Distortion mechanism of the integrator offset combined with DAC parasitic capacitances

of rectangles show DAC output codes and those at right side show amount of charge variation at each clock cycle. The variation of charge has two cycles within one cycle of DAC output. Thus the 2nd-order harmonic distortion is generated by interaction between the integrator offset and the parasitic

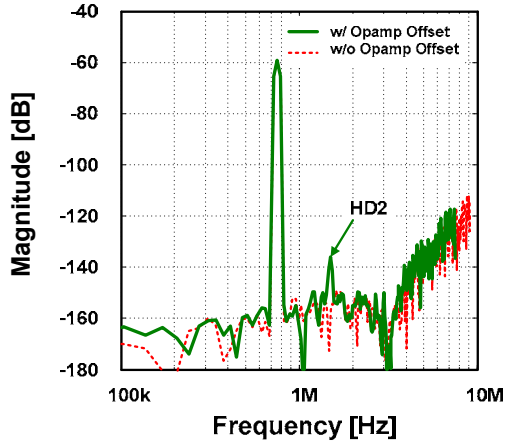


Fig.4 Simulation of 2nd-order harmonic distortion mechanism

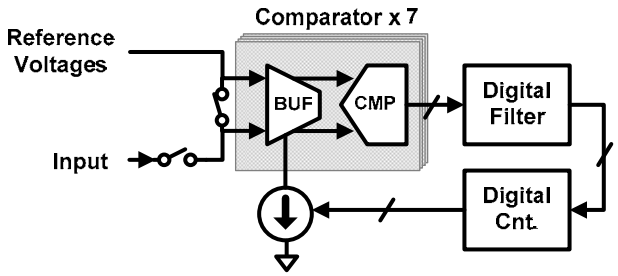


Fig.5 Block diagram of calibration circuit for comparator

capacitances.

The deduction is confirmed by the simulation results shown in Fig.4. The charge is proportional to the input offset voltage of the 1st integrator. Therefore, what we have to do for reducing the distortion is to make input transistors large so that the estimated offset voltage is within acceptable level.

The unevenness of the quantization level tends to cause larger harmonic distortion when we use lower order modulator. Thus the calibration scheme is needed in this case of using 3rd-order modulator.

Figure 5 shows the block diagram of a calibration circuit for comparator mismatch. In calibration mode, the inputs of the buffer are shorted and the offset current of the buffer is controlled so that the probability of "High" at the comparator output is close to 50%. The digital filter in the feedback path effectively removes the effect from noise generated by comparator.

V. Chip Fabrication And Measurement Results

The test chip was fabricated in a 65 nm RF-CMOS process.

Figure 6 shows the chip photograph of the 3rd-order modulator with tuning system. The modulator and tuning system areas are 325 μm × 270 μm and 150 μm × 220 μm, respectively.

Figure 7 shows the correlation between relaxation oscillator frequency and resonance frequency of the modulator. In Fig. 7 both axes show a percent deviation from the nominal value. The graph shows the very strong correlation, which means that we can control the frequency response of the modulator within 1% accuracy.

Figure 8 summarizes improvements of SNR by calibrations.

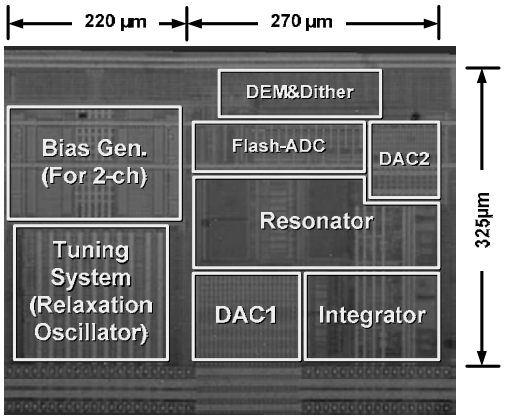


Fig.6 Microphotograph of the modulator with tuning system

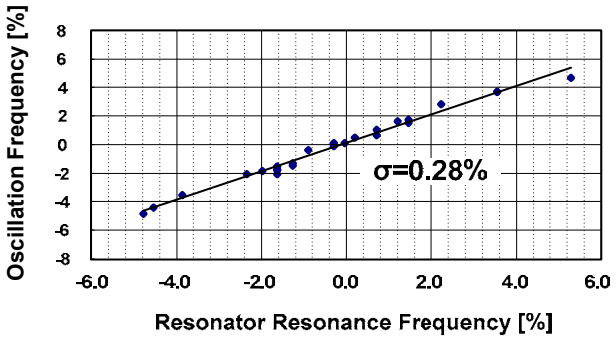


Fig.7 Correlation between oscillator frequency and resonator resonance frequency

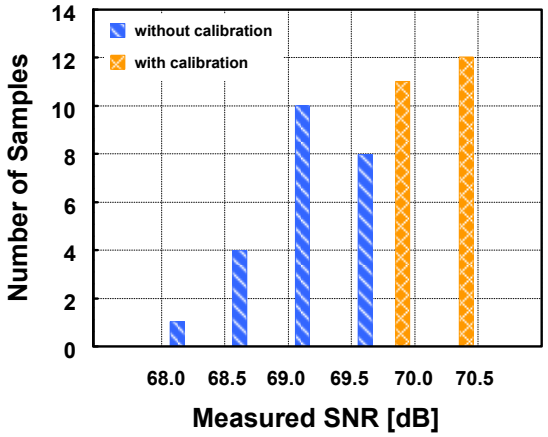


Fig.8 Improvement of SNR by calibrations

23 samples were measured and SNRs of all samples were improved beyond 69.5 dB by calibrations.

The FFT spectrum of the output digital code operating at 140 MHz is shown in Fig.9. The measured SNDR was reached to 69.8 dB due to reduction of the harmonic distortion. The total power consumption of the modulator core is 3.60 mW. The measured chip performances are summarized in Table I. Small chip size including tuning system and the efficient FOM of 0.18 pJ/conv-step were successfully achieved. Benchmark with other efficient modulators is done in Table II. Our modulator has the smallest chip size and enough efficiency.

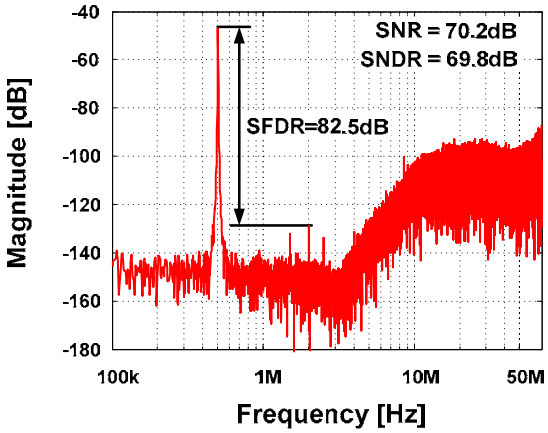


Fig.9 FFT spectrum of the modulator output

Table I Measured chip performance

ΔΣ Modulator Part		
Supply Voltage		0.95-1.25V
Sampling Freq.		140MHz
Signal B.W.		4MHz
SNDR		69.8dB
SNR		70.2dB
SFDR		82.5dB
Power Cons.	Analog	3.11mW
	Digital	0.49mW

ENOB	11.3bit
FOM	0.18pJ/conv.
Area	0.09mm^2
Relaxation Oscillator Part	
Oscillation Freq.	7MHz
Power cons.	100μW
Area	0.07mm^2
Osc. Freq. Sensetivity	<±1.0%

Table II Performance comparison with other efficient CT delta-sigma modulators

FOM [pJ/conv.]	SNDR [dB]	Power [mW]	BW [MHz]	Fs [MHz]	Supply [V]	Area [mm^2]	Reference
0.12	74	20	20	640	1.2	1.2	[3]G. Mitteregger
0.18	69.8	3.6	4	140	1.0	0.09(0.16*)	This work
0.22	72	28	20	420	1.2	1.0	[4]P. Malla
0.23	65	6.8	10	640	1.2	0.4	[5]P. Crombez
0.24	62.5	5.32	10	300	1.1	0.4	[1]K. Matsukawa
0.26	73	3.7	1.92	153.6	2.5	0.125	[6]B. Putter
0.26	71	3	2	104	1.5	0.3	[7]L. Dörrer

*Modulator&Tuning System

VI. Conclusion

In this paper, we have proposed a very compact 3rd-order delta-sigma modulator with ultimate low power tuning system. A new type single opamp resonator has been developed and the mechanism of 2nd-order harmonic distortion has been analyzed. The measurement results show that the proposed modulator has very small chip area and high efficiency. The modulator is very suitable for practical use.

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