# 28-nm FD-SOI CMOS Submilliwatt Ring Oscillator-Based Dual-Loop Integer-*N* PLL for 2.4-GHz Internet-of-Things Applications

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***Abstract*— This article presents a 2.4-GHz low-power compact integer-*N* ring oscillator-based phase-locked loop (PLL) for Internet of Things (IoT) applications. The proposed integer-*N* PLL is based on a dual loop Offset-PLL topology to achieve a fine frequency resolution similar to conventional fractional-*N* PLL. Not using a delta-sigma modulator (DSM) allows an expanded PLL bandwidth without deteriorating the overall noise performance. Implemented in 28 nm CMOS fully depleted silicon on insulator (FD-SOI) technology, the proposed architecture requires a 22-MHz internal reference frequency while achieving a 2-MHz frequency resolution and a 3-MHz PLL bandwidth. Measured prototypes perform −43.9 dBc reference spur, as an average value over all the bluetooth low energy (BLE) band and numerous tested dies, a jitter Figure-of-Merit of −229.6 dB for a power consumption of 0.87 mW and a core area of 0.0256 mm$^2$.**

***Index Terms*— Dual-loop phase-locked loop (PLL) architecture, Internet of Things (IoT), PLLs, ring oscillators (ROs), ultralow-power (ULP) frequency synthesizer.**

## I. Introduction

INTERNET of Things (IoT) frequency synthesizers face rigorous constraints in terms of power consumption to expand battery operating lifetime and compact integration to reduce the overall System on Chip (SoC) area. Ultralow-power (ULP) phase-locked-loop (PLL) architectures have been constantly challenged to fulfill the RF requirements defined in the IoT standards [1]–[3] while reaching the area and power consumption compromise. Compared with *LC* oscillators, ring oscillators (ROs) are found more suitable for IoT applications as they take benefit of their digital nature to follow the technology node scaling, their wide tuning range, and their multiphase capability. Representing the main drawback to tackle, recent studies [4], [5] aim to improve the RO phase noise to meet the IoT requirements.

Increasing the PLL bandwidth is another solution to improve the phase noise overall behavior [6]–[9]. Achieving both a fine frequency resolution and a wide PLL bandwidth, the common solution is to use a fractional-*N* PLL architecture [10]–[12]. Many recent works have significantly mitigated the quantization noise induced by the delta-sigma modulator (DSM) without sacrificing the PLL bandwidth. Noise filtering techniques are proposed as finite-impulse-response (FIR) [6] or space-time averaging (STA) [12] to improve the noise performance. Other approaches are focused on digital-to-analog converter (DAC) or digital-to-time converter (DTC) [8] to cancel the quantization errors. However, drawbacks such as the accuracy of the noise filtering technique or the robustness against the process, voltage, and temperature (PVT) variations for DTC techniques usually lead to higher power consumption, silicon area, and design complexity. Nevertheless, recent DTC architectures [13], [14] manage these drawbacks and achieve a submilliwatt solution, thereby enabling their use in IoT applications. Due to the PLL architecture features and the recent performance improvements, the fractional-*N* PLL remains the best solution to fulfill the needs of IoT applications.

The motivation of this article is to propose an integer-*N* PLL architecture for IoT, specifically bluetooth low energy (BLE). This standard requires a maximum spur of −20 dBm [2], a phase noise lower than −90 dBc/Hz at 1 MHz offset from the carrier [15], a rms jitter (omitting the spurs) lower than 4 ps integrated between 10 kHz and 100 MHz [16]. The proposed PLL shares the same properties as a fractional-*N* PLL in terms of fine frequency resolution and wide PLL bandwidth. The frequency resolution is here realized by the frequency difference between the comparison of two integer-*N* PLLs. The proposed PLL architecture presents an expanded PLL bandwidth to improve the output phase noise performance of simple RO architectures. Another type of compromise is reached between PLL bandwidth, frequency resolution, noise contribution, power consumption, and silicon area to fulfill ULP IoT applications.

As the two loops of the proposed PLL are combined in an offset-PLL (OPLL) topology [17], a new single sideband (SSB) mixer called down-conversion frequency mixer (DFM) is proposed. Entirely composed of digital blocks, the DFM does not require any extra passive filter to reject the unwanted mixing products. Moreover, the two integer-*N* loops are also mainly composed of digital building blocks to reduce the area and the power consumption thereby proposing

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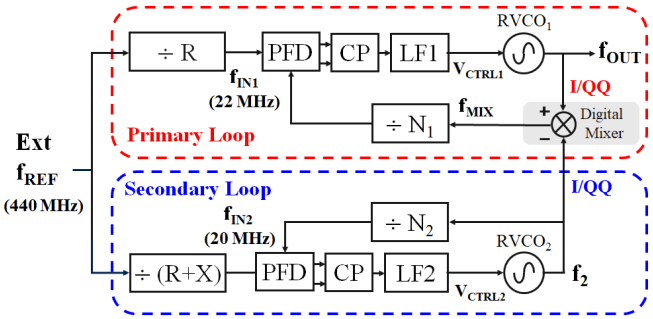


Fig. 1. Detailed block diagram of the proposed caliper PLL architecture.

a compact submilliwatt solution. Implemented in 28 nm fully depleted silicon on insulator (FD-SOI) CMOS process, the presented PLL is suitable for ULP IoT applications.

This article is organized as follows. Section II presents the proposed dual-loop integer-$N$ PLL architecture while Section III is focused on design implementation. Section IV gives measurement results and a comparison to the state-of-the-art. Finally, Section V concludes this article.

## II. Proposed PLL Architecture

### A. Caliper PLL Architecture

As part of the multiloop PLL architectures [17]–[19], the proposed frequency synthesizer is based on a dual-loop PLL topology as illustrated in Fig. 1. Each loop represents an integer-$N$ third-order charge-pump PLL. The external common reference frequency $f_{\text{REF}}$ is divided by two integer frequency dividers $R$ and $(R + X)$, respectively.

Thus, the primary loop runs at the internal frequency $f_{\text{IN1}} = f_{\text{REF}}/R$ to generate the output frequency $f_{\text{OUT}}$ while the secondary loop runs at the internal frequency $f_{\text{IN2}} = f_{\text{REF}}/(R+X)$ to produce its output frequency $f_2$. The internal frequency is defined as the phase-frequency detector (PFD) block comparison frequency. Hence, as being a reference frequency, this internal frequency will create spurs in the output spectrum. The two loops are combined into an OPLL topology. The output signals of frequency, respectively, $f_{\text{OUT}}$ and $f_2$ are mixed to recover the signal $f_{\text{MIX}}$ with a frequency of $f_{\text{OUT}} - f_2$. This signal $f_{\text{MIX}}$ is then propagated in the feedback path of the primary loop. Contrary to a classical OPLL, the phenomenon of injection pulling between the two oscillator frequencies is here avoided because the two internal frequencies $f_{\text{IN1}}$ and $f_{\text{IN2}}$ are already synchronized with the same reference frequency $f_{\text{REF}}$.

The interesting association of the OPLL topology and the dual loop architecture with a common reference frequency $f_{\text{REF}}$ provides the output frequency $f_{\text{OUT}}$ as a combination of the two internal frequencies $f_{\text{IN1}}$ and $f_{\text{IN2}}$ as

$$f_{\text{OUT}} = f_{\text{IN1}} \cdot N_1 + f_{\text{IN2}} \cdot N_2 = f_{\text{REF}} \cdot \left( \frac{N_1}{R} + \frac{N_2}{R+X} \right) \quad (1)$$

where $N_1$ and $N_2$ are, respectively, the integer values of the feedback loop dividers, and $R$ and $(R + X)$ are the integer values of input dividers as represented in Fig. 1.

Three achievable output frequency resolutions $\Delta f_{\text{OUT}}$ may be reached with the proposed PLL topology. Focusing on only the primary loop, an increment/decrement of the divide-by-$N_1$ feedback frequency divider while keeping constant the divide-by-$N_2$ feedback frequency divider, implies an output frequency resolution of $\Delta f_{\text{OUT}} = f_{\text{IN1}} = f_{\text{REF}}/R$. It represents the mode with the usual channel spacing of a classical integer- $N$ PLL.

Only regarding the secondary loop, an increment/decrement of the divide-by-$N_2$ feedback frequency divider while keeping constant the divide-by-$N_1$ feedback frequency divider, implies an output frequency resolution of $\Delta f_{\text{OUT}} = f_{\text{IN2}} = f_{\text{REF}}/(R + X)$. It represents here the mode with the usual output channel spacing of a classical OPLL.

Concerning the overall PLL architecture, another output frequency resolution $\Delta f_{\text{OUT}}$ is achievable. Both feedback frequency dividers ($N_1$ and $N_2$) can simultaneously be incremented and decremented while respecting the relation

$$\forall (N_1, N_2) \in \mathbb{N}^2, \quad N_1 + N_2 = k \in \mathbb{N} \quad (2)$$

where $k$ is a constant integer. Hence, each increment of $N_1$ implies a decrement of $N_2$. Thus, the output frequency resolution of the proposed PLL architecture is then achieved by the difference of the two internal frequencies as

$$\Delta f_{\text{OUT}} = f_{\text{IN1}} - f_{\text{IN2}} = f_{\text{REF}} \cdot \left( \frac{X}{R \cdot (R+X)} \right). \quad (3)$$

As the output frequency resolution $\Delta f_{\text{OUT}}$ is tuned using a frequency difference of the two internal frequencies $f_{\text{IN1}} = f_{\text{REF}}/R$ and $f_{\text{IN2}} = f_{\text{REF}}/(R + X)$, we propose the name of Caliper PLL for this topology. Compared with an integer-$N$ PLL with the same PLL bandwidth of a tenth of the internal frequency $f_{\text{IN1}}$, the proposed PLL achieves a frequency resolution $\Delta f_{\text{OUT}}$ $(R + X)/X$ times smaller. Thus, for the same $\Delta f_{\text{OUT}}$, the proposed PLL offers a larger PLL bandwidth than classical integer-$N$ PLL. The expanded PLL bandwidth is due to the "Caliper effect" of the proposed architecture, allowing to reduce the PLL settling time and to improve the voltage-controlled oscillator (VCO) phase noise behavior close to the carrier.

Let us now focus on the frequency plan allocation. Dedicated to IoT applications, the proposed PLL architecture targets an output frequency resolution $\Delta f_{\text{OUT}}$ of 2 MHz which suits the channel spacing of the BLE specifications (2.4–2.48 GHz) [2]. As expressed in (3), the 2-MHz frequency resolution is generated by choosing the loop internal frequencies of $f_{\text{IN1}} = 22$ MHz and $f_{\text{IN2}} = 20$ MHz, respectively. We have considered separately the stability of both the primary and secondary loops to settle the PLL bandwidth around a couple of MHz, ensuring the stability of the overall architecture.

As only ***integer*** frequency dividers are used in the proposed solution, the reference frequency would have a larger value than $f_{\text{IN1}}$ or $f_{\text{IN2}}$. The lowest common multiple of two adjacent integers is chosen which gets a reference frequency of $f_{\text{REF}} = 440$ MHz and input frequency *integer* division ratios of $R = 20$ and $(R + X) = 22$, respectively.

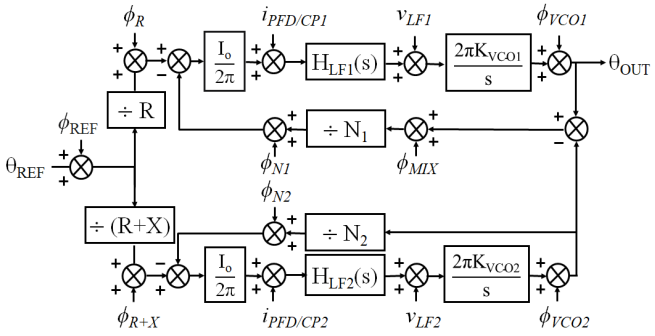


Fig. 2. Phase-domain noise model of the proposed caliper PLL.

The $f_{\mathrm{MIX}}$ frequency of the DFM output signal can be expressed as

$$f_{\mathrm{MIX}} = \frac{N_1 + N_2}{2} \cdot \Delta f_{\mathrm{OUT}} + \frac{N_1 - N_2}{2} \cdot (f_{\mathrm{IN1}} + f_{\mathrm{IN2}}) \quad (4)$$

where $\Delta f_{\mathrm{OUT}}$ is the frequency resolution equals to the frequency difference $f_{\mathrm{IN1}} - f_{\mathrm{IN2}}$. Thus, the $f_{\mathrm{MIX}}$ frequency contains the three frequencies $f_{\mathrm{IN1}} = 22$ MHz, $f_{\mathrm{IN2}} = 20$ MHz and $\Delta f_{\mathrm{OUT}} = f_{\mathrm{IN1}} - f_{\mathrm{IN2}} = 2$ MHz. These tones are translated into deterministic spurs in the output spectrum.

### *B. Design Considerations*

Illustrated in Fig. 2, a linear phase domain representation is established to determine the dominant noise sources in the proposed PLL architecture. The reference noise transfer function is representing by the closed-loop transfer function as

$$H_{\mathrm{CL}}(s) = \frac{\theta_{\mathrm{OUT}}}{\phi_{\mathrm{REF}}} = H_{\mathrm{CL1}}(s) \cdot \left(1 + \left(\frac{R}{N_1}\right) \cdot H_{\mathrm{CL2}}(s)\right) \quad (5)$$

where $H_{\mathrm{CL1}}(s)$ and $H_{\mathrm{CL2}}(s)$ are, respectively, the closed-loop transfer functions of the primary and the secondary loops. The phase noise model has determined that the out-of-band noise contributors are the two oscillator noise transfer functions of the primary and secondary loop are expressed, respectively, as

$$\frac{\theta_{\mathrm{OUT}}}{\phi_{\mathrm{VCO1}}} = \frac{1}{1 + H_{\mathrm{OL1}}(s)} \quad (6)$$

$$\frac{\theta_{\mathrm{OUT}}}{\phi_{\mathrm{VCO2}}} = \frac{R}{N_1} \cdot H_{\mathrm{CL1}}(s) \cdot \frac{1}{1 + H_{\mathrm{OL2}}(s)} \quad (7)$$

where $H_{\mathrm{OL1}}(s)$ and $H_{\mathrm{OL2}}(s)$ are, respectively, the open-loop transfer function of the primary and secondary loops. The oscillator noise transfer function of the secondary loop is filtered through the low pass function behavior of the primary loop. Thus, the out-of-band phase noise is mainly dominated by the primary loop oscillator noise. Thus, the proposed PLL architecture exploits all benefits of a wide PLL bandwidth to suppress the oscillator noise contribution.

### *C. Comparison of the Proposed PLL With Classical Integer-N and Fractional-N PLLs*

Represented in Table I, the proposed Caliper PLL characteristics are compared with the integer-*N* and fractional-*N* PLL architectures. The Caliper PLL architecture shares common practical features with classical fractional-*N* PLL such as a narrow frequency resolution $\Delta f_{\mathrm{OUT}}$ and a wide PLL bandwidth. At the same time, as an integer-*N* PLL, the out-of-band phase noise of the proposed solution is only composed of the oscillator phase noise. Thus, the Caliper PLL fully exploits the wide PLL bandwidth to improve the phase noise behavior close to the carrier without impacting the out-of-band phase noise performance. Considering the spurs performance, the dual loop PLL architecture of the proposed solution creates offset spurs as does a fractional-*N* PLL. Finally, the frequency resolution of the Caliper PLL is defined in (3) and discussed in Section II-A, by the reference frequency and the two input frequency dividers values.

TABLE I
PERFORMANCE COMPARISON

| | Integer-*N* PLL | Fractional-*N* PLL | Proposed PLL |
|---|---|---|---|
| For the same internal frequency $f_{IN}$ and same technology node | | | |
| Complexity | Single loop with integer divider | Single loop with fractional divider (DSM) | Dual loop with integer dividers |
| Internal frequency $f_{IN}$ | $f_{IN} = f_{REF}$ | $f_{IN} = f_{REF}$ | $f_{IN} = f_{REF}/R$ |
| $\Delta f_{OUT}$ | $\Delta f_{OUT} = f_{IN}$ | $\Delta f_{OUT} < f_{IN}$ | $\Delta f_{OUT} < f_{IN}$ |
| PLL BW | $f_{BW} < \Delta f_{OUT}$ | $f_{BW} > \Delta f_{OUT}$ | $f_{BW} > \Delta f_{OUT}$ |
| Out-of-band phase noise | RO phase noise | DSM phase noise | RO phase noise |
| Spurious | Reference spurs | Reference and fractional spurs | Reference and offset spurs |

The proposed topology requires a larger reference frequency than classical crystal referenced PLL. However, recent studies have shown outstanding results in line with existing industrial standards, while using other types of external resonators such as bulk acoustic wave (BAW) devices with reference frequencies around hundreds of megahertz or even higher [20], [21]. Fractional-*N* PLL can also take advantage of high reference frequency to produce a wide bandwidth and a fine frequency resolution using noise shaping techniques. However, the power consumption of the DSM is proportional to its clock frequency. Considering a given power consumption, a DSM-based PLL will have comparable performance with the proposed solution, while it would need a high value of its internal clock. Targeting a submilliwatt power consumption and a reduced silicon area suitable for IoT applications, the Caliper PLL proposes an alternative PLL architecture showing performance between the integer-*N* and fractional-*N* PLLs.

For direct synthesizer modulation, for instance, the frequency shift keying (FSK) generation, the fractional-*N* PLL is certainly a suited candidate. When considering the proposed topology, the frequency shift must be added to $f_{\mathrm{REF}}$ through another loop, nevertheless, the two loops keep an integer-*N* architecture. The integration of such Caliper PLL in a BLE transmitter will require a careful overall SoC frequency planning and certainly some filtering regarding the generated spurs, while the use with respect to a receiver is much more straightforward.

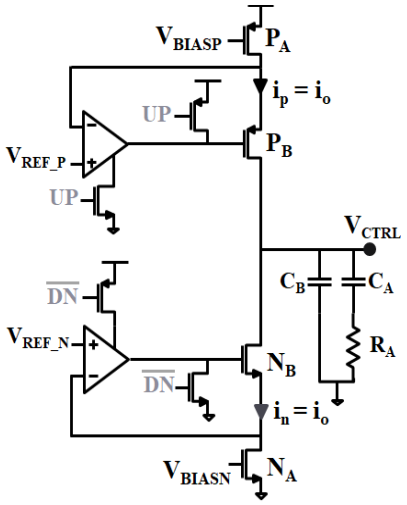


Fig. 3. Proposed CMOS bootstrapped charge-pump architecture.

## III. Design of Caliper PLL Architecture

### A. Bootstrapped Charge Pump

The proposed CMOS bootstrapped charge pump is illustrated in Fig. 3. The $N_A$ and $N_B$ nMOS transistors with the associated operational amplifier compose the nMOS bootstrapped current source. For instance, the current $i_N$ is set by the transistor $N_A$. The $V_{DS}$ voltage of the current source $N_A$ is compared by the OpAmp with the reference voltage $V_{REF-N}$.

Each OpAmp is composed of a single-ended differential pair with active load. The OpAmp output voltage acts as a control loop of the $N_B$ transistor biasing to regulate the $i_N$ current under variation of the $V_{CTRL}$ voltage. As depicted in Fig. 3, a similar structure is implemented on the pMOS side following the same principle. The designed charge pump generates a current of 10 $\mu$A.

Thus, the bootstrapped current source principle ensures a constant current control throughout all the $V_{CTRL}$ possible swing by reducing the channel length modulation phenomenon. For instance, results from postlayout simulation for $V_{CTRL} = 0.5$ V gave $i_N = 10.35$ $\mu$A and $|i_P| = 10.21$ $\mu$A. As the reference spur performance is linked to the current difference $|i_N - |i_P||$ [22], the proposed principle performs a constant reference spur performance over all the output PLL frequency range.

Represented in Fig. 3, the same second-order low pass filter topology is implemented in both the primary and secondary loop. For both filters, same capacitance values of $C_A = 4$ pF and $C_B = 320$ fF were used while resistor values were fixed with $R_{A1} = 114$ k$\Omega$ and $R_{A2} = 165$ k$\Omega$ for the primary and secondary loop filter, respectively. The two digital signals UP and $\overline{DN}$ are coming from a positive-edge triggered tri-states comparator PFD. UP and $\overline{DN}$ signals control the charge pump by shorting both the output and the current source of each OpAmp. The $V_{CTRL}$ amplitude is bounded by the two respective $V_{DS}$ voltages of the $N_A$ and $P_A$ transistors. Thus, the $N_A$ and $P_A$ transistors are biased in linear mode to maximize the achievable amplitude swing for $V_{CTRL}$. Although it reduces the output resistance of the current sources, the bootstrapped principle permits to have a 1-V low voltage charge pump.

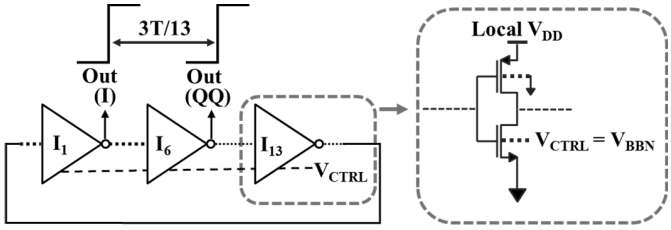


Fig. 4. $N = 13$ single-ended CMOS inverter-based RO topology.

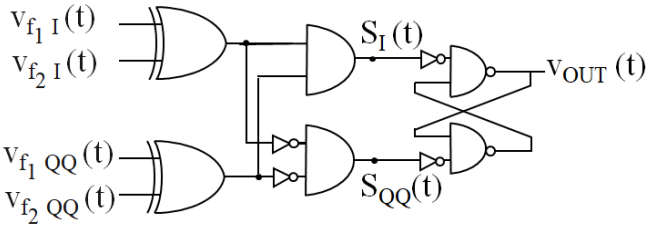


Fig. 5. Detailed representation of the proposed digital DFM.

### B. Ring Oscillator

As illustrated in Fig. 4, both loops of the proposed PLL contain the same single-ended inverter-based RO architecture. Each RO is composed of $N = 13$ delay cells implemented with classic CMOS inverters. The RO generates quasi-quadrature outputs ($I$ and $QQ$) represented by a relative delay of $3T_{OSC}/13 = 0.23T_{OSC}$ where $T_{OSC}$ represents the period of oscillation. Fine-tuning is applied within the loop to reduce the VCO noise sensibility and improve the PLL stability. The RO fine frequency tuning is controlled by body-biasing the transistors' back gate [23], [24]. The oscillator gain $K_{VCO}$ is 250 MHz/V. In steady-state, the body-biasing control voltage range of $RVCO_1$ is comprised between 0.5 and 0.8 V to cover the BLE bands (2.4–2.48 GHz). In contrast, $RVCO_2$ has to cover from 0.8 to 1.0 GHz to provide all the BLE channels. Consequently, the $K_{VCO}$ of $RVCO_2$ has been set to 250 MHz/V as well to provide a small margin. Using only the nMOS low-VT (LVT) body-biasing enables to directly use the filter voltage output as RO control voltage without extra biasing circuit to achieve minimal power consumption. Thus, the body biasing feature, unique to FD-SOI technology, enables this new frequency tuning knob over this very simple, compact, power-efficient, and robust RO topology [25].

### C. Digital DFM

In OPLL architectures [26], the frequency $f_{MIX} = f_1 - f_2$ is recovered from all the mixing products by using a highly selective filter thereby contributing significantly to the total PLL area. Based on a fully digital architecture, the proposed DFM produces the $f_{MIX}$ frequency as a SSB mixer by rejecting the other mixing products without using typical filters [27]. The SSB mixer theory normally, requires quadrature inputs (I/Q), usually produced by additional circuits based on fully differential oscillators [4] or polyphase filters [28].

As illustrated in Fig. 5, we propose a DFM that uses only the quasi-quadrature inputs ($I$ and $QQ$) from the two ROs ($v_{f1}(t)$ and $v_{f2}(t)$) with, respectively, $f_1$ and $f_2$ frequencies. For instance, the quasi-quadrature digital signals from the $RVCO_1$

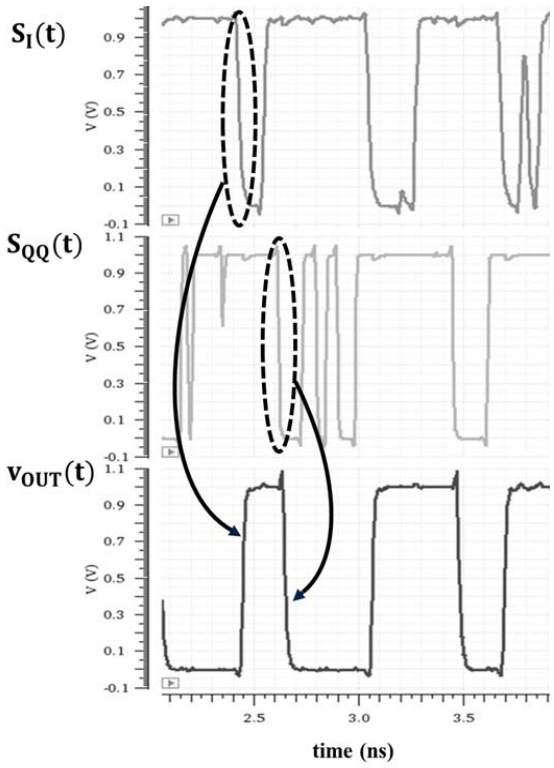


Fig. 6. Transient simulation of the proposed DFM architecture.

can be expressed at the first-order approximation ($n = 0$) as

$$v_{f_1 I}(t) = A \cdot \sum_{i=0}^{n} \frac{\cos((2i+1)\omega_1 t)}{2i+1} = A \cdot \cos(\omega_1 t) \tag{8}$$

$$v_{f_1 QQ}(t) = A \cdot \sum_{i=0}^{n} \frac{\cos((2i+1)\omega_1 t + \theta)}{2i+1} = A \cdot \cos(\omega_1 t + \theta) \tag{9}$$

where $\theta$ represents the quasi-quadrature phase delay close to $\pi/2$. The quasi-quadrature inputs from the $RVCO_2$ share the same expressions with a $\omega_2$ frequency.

The four input signals are mixed by the digital paths to create the two intermediate signals $S_I(t)$ and $S_{QQ}(t)$. In the first order, $S_I(t)$ and $S_{QQ}(t)$ signals have the same expression

$$\begin{aligned} &S_I(t) \\ &= S_{QQ}(t) = v_{f_1 I}(t) \cdot v_{f_2 I}(t) + v_{f_1 QQ}(t) \cdot v_{f_2 QQ}(t) \\ &= A^2 \cos((\omega_1 - \omega_2)t) + A^2 \cos(\theta) \cos((\omega_1 + \omega_2)t + \theta). \end{aligned} \tag{10}$$

For $\theta$ close to $\pi/2$, the frequency of the two signals $S_I(t)$ and $S_{QQ}(t)$ is approximated by the frequency $f_1 - f_2$. Illustrated in Fig. 6, the digital output signal $v_{OUT}(t)$ is generated by the RS latch. The falling edge of $S_I(t)$ acts as a positioning signal and the next falling edge of $S_{QQ}(t)$ acts as a reset signal. Based on a similar approach concerning the digital sampling [29], the RS latch acts as a digital sampler to enforce the $f_1 - f_2$ frequency component.

Due to the quasi-quadrature relation between the DFM inputs, the output signal $v_{OUT}(t)$ presents an instantaneous frequency that fluctuates around the average frequency $f_1 - f_2$.

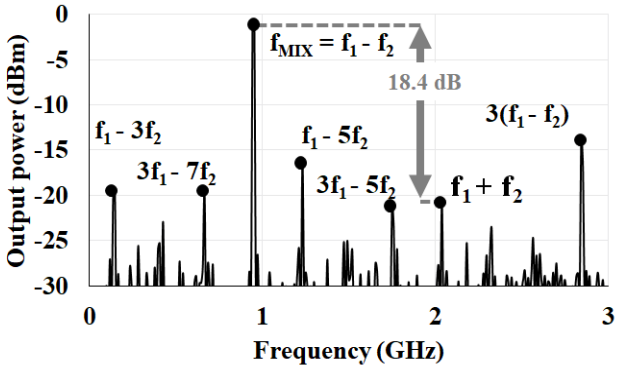


Fig. 7. Measured DFM output spectrum for $f_{OUT} = 1.496$ GHz and $f_2 = 546$ MHz.

The digital mixer is still compliant with the PLL because of the frequency divider architecture. Indeed, the four frequency dividers ($N_1$, $N_2$, $R$, and $(R+X)$) of the Caliper PLL contains the same integer-$N$ frequency divider architecture based on an edge-counter. The edge counter is implemented through a set of D-flip-flops that successively count the number of rising edges. When the binary value of the rising edges reaches the respective programmable value, a logic path resets the counter and outputs a pulse to the PFD. The edge counter permits to filter the phase variation of signal $v_{OUT}(t)$ by computing the average frequency over $N$ periods, the frequency divider acts as another selective filter while the PLL loop ensures the PLL locking on the $f_1 - f_2$ frequency.

A prototype was implemented in 28-nm FD-SOI CMOS technology to validate the original features of the DFM. Thus, the DFM prototype is measured with quasi-quadrature inputs from the RO topology presented before, with, respectively, $f_1 = 1496$ MHz and $f_2 = 546$ MHz frequencies. The output spectrum is represented in Fig. 7 where the dominant difference frequency $f_1 - f_2$ presents a significant amplitude to be retrieved from the other mixing products.

Using the amplitudes of $S_I(t)$ and $S_{QQ}(t)$ signals in (9), the power difference between the $f_1 - f_2$ and $f_1 + f_2$ tones is calculated by

$$P_{f_1 - f_2} - P_{f_1 + f_2} = 10 \log\left(\left(\frac{A^2}{A^2 \cdot \cos(\theta)}\right)^2\right) \tag{11}$$

$$P_{f_1 - f_2} - P_{f_1 + f_2} = 10 \cdot \log\left(\frac{1}{\cos^2(\theta)}\right) = 18.4 \text{ dB} \tag{12}$$

where $\theta = (6\pi/13)$ is the radian value of the quasi-quadrature relation. This value has been verified through measurement as highlighted in Fig. 7. It confirms that the first-order approximation is sufficient to validate the digital mixer operation. As input signals are square wave signals, mixing products are created between the harmonic frequencies of $f_1$ and $f_2$. Represented in Fig. 7, the measured frequency of each tone matches the expected parasitic frequency. Exact amplitude of the other parasitic spurs should be calculated with the complete mathematical formulas taking into consideration the $\sin(x)/x$ amplitude functions. However, these spurs are considered negligible as their amplitude is lower than the one of the third harmonic $3(f_1 - f_2)$, which is at $-10$ dB from the carrier.

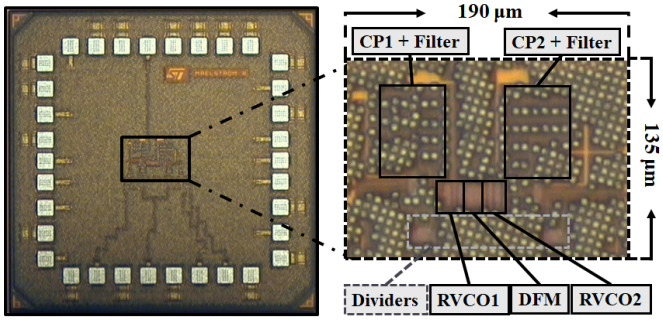


Fig. 8. Die photography of the proposed PLL.

This criterion permits to avoid the use of another filter around $f_{\text{MIX}}$ once implemented inside the proposed PLL architecture.

Thus, the proposed DFM is a fully digital down-converter mixer that generates only the difference frequency $f_{\text{MIX}} = f_1 - f_2$ without the use of a passive filter. Its capability to perform with quasi-quadrature inputs reduces its impact on terms of area and power consumption once implemented inside the Caliper PLL.

## IV. Measurement Results

The prototype of the proposed Caliper PLL has been fabricated in the 28-nm FD-SOI CMOS technology from STMicroelectronics. The die photography is shown in Fig. 8, the active area occupies 0.0256 mm$^2$ including the bias voltage decoupling capacitors. The two passive loop filters constitute 17% of the total area.

The total measured power consumption is 870 $\mu$W under a 1-V voltage supply. The two ROs consume, respectively, 350 $\mu$W for RVCO$_1$ and 170 $\mu$W for RVCO$_2$. The digital parts consume 320 $\mu$W including the four frequency dividers, the down-converter frequency mixer, and the two PFDs. Finally, each charge pump consumes 15 $\mu$W.

The prototype PLL locks on a frequency range from 2.28 to 2.5 GHz with a common 440 MHz reference frequency provided by an Agilent E4400B external signal generator. To cover the whole synthesizer frequency range, the secondary PLL varies from 800 MHz to 1 GHz. Fig. 9 illustrates the output spectrum for a 2.420-GHz output frequency obtained by the feedback divider values of $N_1 = 70$ and $N_2 = 44$.

The measured reference spur is $-43.9$ dBc at 22 MHz offset from the carrier corresponding to the internal frequency $f_{\text{IN1}}$ of the primary loop. A small PLL bandwidth is usually used to improve the spurs performance [30]. As the Caliper PLL, targets a large PLL bandwidth, it explains the quite high reference spurs performance. Due to the OPLL topology of the proposed Caliper PLL, other spurs from the combination of the two internal frequencies $f_{\text{IN1}}$ and $f_{\text{IN2}}$ appear in the output spectrum [26].

Thereby, Fig. 9 shows a measured spur of $-65$ dBc at 20 MHz from the carrier which corresponds to the internal frequency $f_{\text{IN2}}$ of the secondary loop. A spur at 2 MHz from the carrier is measured at $-30.75$ dBc. PLL nonidealities are generally caused within the PFD/CP or dividers circuits. Reducing these nonidealities through calibration loops or any compensation circuitry would reduce the levels of these spurs at the cost of increased power consumption and silicon footprint. The in-band spurs are also impacted by the inaccuracy of the quasi-quadrature relation within the digital mixer. Using an exact quadrature relation produced by quadrature oscillators [4] or polyphase filters [28] would also reduce these in-band spur levels at the same cost of an increased power consumption and area. Over all the BLE channels, the measured spurs at 2 MHz from the carrier shows a $\pm 5$ dB variation around the $-30.75$ dBc value. This variation is also explained by the inaccuracy of the quasi-quadrature relation and by the unequal efficiency of the filtering function provided by the loop filters over the PLL frequency range. Extracted from BLE requirements [2], the maximum spur in adjacent channel (at 2 MHz offset) is $-20$ dBm. Consequently, the proposed synthesizer is compliant with BLE requirements, so no action was made to further reduce these spurs.

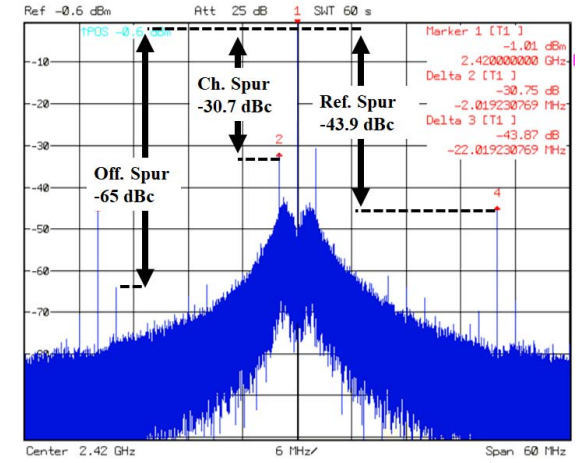


Fig. 9. Measured frequency spectrum at a 2.420-GHz output frequency (caliper PLL mode).

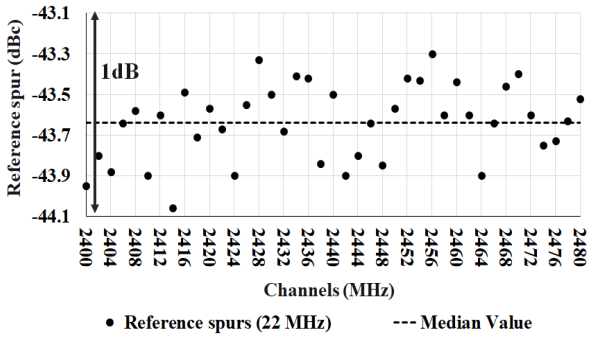


Fig. 10. Measured reference spurs performance (at the offset frequency $f_{\text{IN1}}$, internal frequency of the primary loop in Fig. 1) over all the BLE channels.

Fig. 10 represents the measured reference spurs performance at 22 MHz offset from the carrier for all BLE channels. The measured frequency resolution of 2 MHz settles the proof of concept of the proposed architecture. Measured from the same chip, the reference spurs show only a 0.76-dB variation around the median value of $-43.63$ dBc. Thus, it confirms that the bootstrapped principle achieves a constant reference spurs performance over the PLL frequency range.

Fig. 11 illustrates the measured reference spurs at 22 MHz offset from the 2.438-GHz carrier for ten different random dies

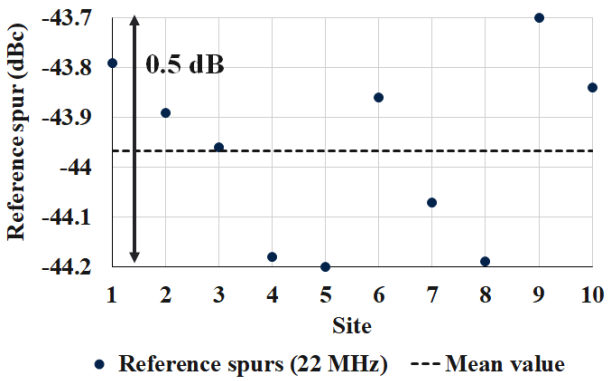


Fig. 11. Measured reference spur performance at a 2.438-GHz output frequency for ten different tested chips (at the offset frequency $f_{IN1}$, internal frequency of the primary loop in Fig. 1).

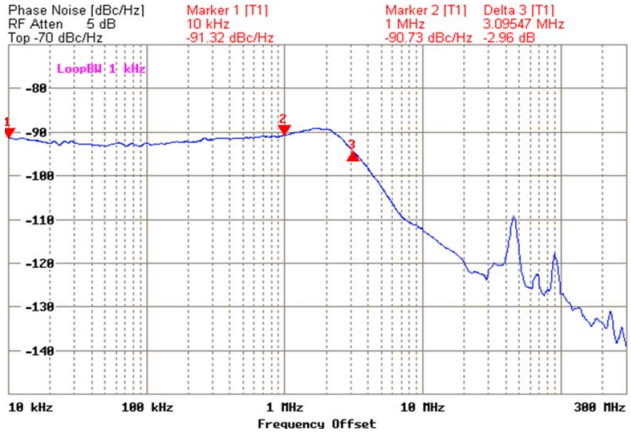


Fig. 12. Measured output phase noise for a 2.438-GHz output frequency.

from the same wafer. All the measured dies achieve a low variability around a mean reference spurs value of −43.96 dBc.

Thus, the proposed PLL shows a reproducible and robust reference spur performance.

Fig. 12 plots the measured output phase noise for a 2.438-GHz output frequency obtained by the divider values of $N_1 = 69$ and $N_2 = 46$. The Caliper PLL shows a 3-dB-bandwidth of 3 MHz for a frequency resolution of 2 MHz. Measured in-band phase noise of −91 dBc/Hz is achieved. The 350-$\mu$W locked RO achieves a −90.7 dBc/Hz phase noise at 1 MHz offset from the carrier and an out-of-band phase noise of −112 dBc/Hz at 10 MHz offset from the carrier. The reported phase noise measurement is omitting the spurs. Thus, a measured 3.58 ps rms jitter is achieved by integrating the phase noise from 10 kHz to 100 MHz. The out-of-band portion shows around 50 MHz offset the presence of external disturbances corresponding to the measurement environment.

Fig. 13 illustrates the phase noise model of the proposed Caliper PLL, the model represents the main phase noise contributions with the overall simulated phase noise of the proposed PLL. As the phase noise model is based on uncorrelated noise sources, small differences between the simulated and the measured phase noises are noticed. However, the phase noise model shows good agreements with the measurement

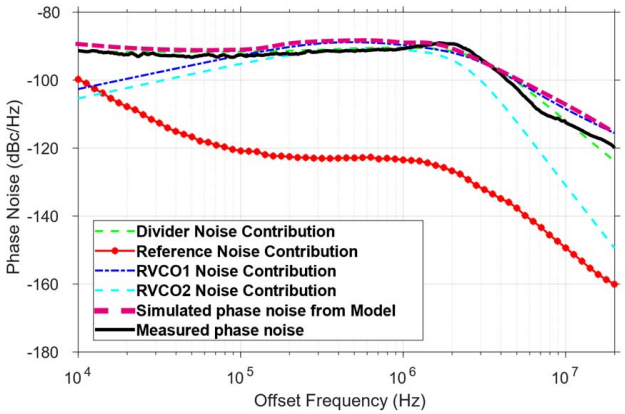


Fig. 13. Phase noise model of the proposed PLL representing the five main noise contributions (noise from both dividers, both oscillators, and the reference) compared with the measured output phase noise.

results. As expected from the noise transfer function study, the out-of-band noise is dominated by $RVCO_1$. $RVCO_2$ noise is less significant due to additional filtering at high offset frequencies. Thus, the phase noise model confirms that the internal frequency divider noise imposes the in-band noise level around −91 dBc/Hz and then degrades the phase noise and jitter performances of the prototype PLL.

The performance of the Caliper PLL is summarized and compared with the state-of-the-art for IoT applications in Table II. Two metrics are introduced to compare different frequency synthesis architectures, which target a large panel of output frequencies and are implemented in a large span of CMOS technology nodes. The power spending per frequency is defined as the ratio between the power consumption in milliwatt and the PLL output frequency in GHz. It represents how much power the PLL has to burn to generate the output frequency. A normalized area parameter is defined as well, the ratio between the active area in millimeter square and the technology node in $nm^2$. Considering the technology scalability, this parameter draws a fair comparison between PLL architectures over several technology nodes.

The presented PLL implementation exhibits system-level performance in line with the best-in-class state-of-the-art. The phase noise performance of −90.7 dBc at 1 MHz offset from the carrier meets the BLE requirements. From a measured rms jitter performance of 3.58 ps integrated between 10 kHz and 100 MHz, the Caliper PLL achieves a jitter figure-of-merit (FoM jitter) of −229.6 dB in line with the State-of-the-Art Ring fractional-*N* PLL architectures.

This demonstrates that the proposed PLL architecture is suitable for BLE applications. The proposed dual-loop architecture obtains the second-best absolute area among planar CMOS technologies. The Caliper PLL achieves the best power spending per frequency and the second lowest power consumption among the reported RO-based PLLs. Moreover, the proposed solution gets close to the power spending per frequency of *LC*-based PLL.

As the proposed PLL architecture, each reported RO-based fractional-*N* PLL architecture uses a wideband PLL bandwidth to increase the RO phase noise filtering, hence, improving their RF performance (e.g., rms jitter and phase noise).

TABLE II
COMPARISON WITH STATE-OF-THE-ART FRACTIONAL-*N* PLL

| | **This work** | **JSSC 16 [8]** | **JSSC 18 [6]** | **JSSC 20 [12]** | **RFIC 18 [7]** | **ISSCC 20 [16]** | **TCAS-I 21 [14]** | **JSSC 19 [31]** | **ISSCC 20 [32]** | **JSSC 19 [15]** | **ISSCC 17 [9]** | **JSSC 19 [13]** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PLL Architecture | Ring integer-*N* | Ring fractional-*N* | | | | | | | | | LC fractional-*N* | |
| | Dual Loop | Multi-modulus divider | ΔΣ noise reduction | ΔΣ noise reduction | Injection-locked | MDLL | MDLL | MDLL | ADPLL | ADPLL | Divider-less | DPLL FLL |
| Technology | 28nm FDSOI CMOS | 65nm CMOS | 45nm CMOS | 40nm CMOS | 40nm CMOS | 22nm FinFET | 65nm CMOS | 65nm CMOS | 65nm CMOS | 40nm CMOS | 40nm CMOS | 65nm CMOS |
| Frequency Range (GHz) | 2.28-2.5 | 2.0-5.5 | 2.31-3.05 | 1.67-3.12 | 1.8-2.7 | 1.2-3.8 | 0.6-1.6 | 1.65-3.05 | 4.5-6.0 | 0.5-0.8 | 1.8-2.5 | 2.1-3.1 |
| Output Frequency [a] (GHz) | 2.438 | 2.5 | 2.42 | 2.76 | 2.432 | 2.4175 | 1.0 | 3.05 | 5.5 | 0.6 | 2.433 | 2.404 |
| Ref Frequency (MHz) | 440 | 50 | 22.6 | 50 | 64 | 40 | 100 | 100 | 100 | 37.5 | 32 | 10 |
| Internal Frequency (MHz) | 22[b] | 50 | 22.6 | 50 | 64 | 40 | 100 | 100 | 100 | 37.5 | 32 | 10 |
| Freq resolution (MHz) | 2 | 0.196 | N.A. | N.A | 0.016 | N.A. | 0.781 | 1.96 | 0.0031 | 0.0021 | 0.016 | 0.001 |
| Ref Spur (dBc) | -44 | -44 | -60 | -67.2 | -43.6 | -50 | -64.5 | -54.5 | N.A. | -55 | -62 | N.A. |
| Frac Spur (dBc) | -30.7 | -41.6 | -41 | -47.2 | -45.8 | -46.5 | -59.6 | -54.8 | -58 | -42.3 | -56 | -52 |
| RMS Jitter (ps) | 3.58 | 3.6 | 1.5 | 2.26 | 1.6 | 4.04 | 0.7 | 0.376 | 0.648 | 10 | 1.98 | 2.8 |
| Integ. range (Hz) | 10k – 100M | 10k – 100M | 10k – 50M | 1k – 100M | 10k – 10M | 10k – 100M | 10k-40M | 30k-30M | 1k-30M | 20k-100M | 10k – 10M | 1k-40M |
| Phase noise[c] (dBc/Hz) | −90.7 | −91.5 | −104 | −100 | −108.4 | −97.2 | −125.4 | −117.4 | -110.1 | -95 | −103 | -105 |
| Supply voltage (V) | 1 | 0.7 | 1 | 1.1 | 1 | 1.1 | 1.2 | 1.2 | N.A. | 0.9 | 1 | 1 |
| Power consumption (mW) | 0.87 | 1.35 | 10 | 4.85 | 1.3 | 1.81 | 1.85 | 3.35 | 9.88 | 0.253 | 0.67 | 0.265 |
| FOM Jitter [d] (dB) | -229.6 | -227.6 | -226.5 | -226.1 | -234.7 | -225.8 | -240.4 | -239.2 | -233.8 | -208.5 | -236.0 | -236.8 |
| Area ($mm^2$) | 0.0256 | 0.084 | 0.096 | 0.086 | 0.13 | 0.0052 | 0.126 | 0.0275 | 0.108 | 0.0166 | 0.18 | 0.25 |
| ***Normalized Area [e] ($10^6$)*** | ***32.65*** | ***19.88*** | ***47.41*** | ***53.75*** | ***81.25*** | ***10.74*** | ***29.82*** | ***6.51*** | ***25.56*** | ***10.37*** | ***112.50*** | ***59.17*** |
| ***Power spending per frequency [f] (mW/GHz)*** | ***0.35*** | ***0.54*** | ***4.13*** | ***1.75*** | ***0.53*** | ***0.75*** | ***1.85*** | ***1.10*** | ***1.80*** | ***0.42*** | ***0.27*** | ***0.11*** |

[a] All measured data is considered for the given output frequency
[b] Fabricated from a common reference at 440 MHz divided into a 22 MHz for the primary loop and 20 MHz for the secondary loop.
[c] Measured at 1 MHz offset frequency from the carrier.
[d] FOM Jitter = 20 log(RMS Jitter/1 s)+10 log(Power/1 mW).
[e] Normalized Area = Area ($mm^2$) / Technology node$^2$ ($nm^2$).
[f] Power spending per frequency = Power consumption (mW) / Output frequency (GHz)

Focusing on the DSM-based PLLs [6], [8], [12], either a DTC [8], a FIR method [6], or STA method [12] is used to cancel the DSM quantization noise without impacting the PLL bandwidth. In all-digital PLL (ADPLL) architecture [32], the time-invariant probability modulator (TIPM) method is used to reduce the DSM noise before it interacts with the DTC nonlinearity. Thus, these PLL architectures are using noise filtering techniques to reduce the DSM noise and achieve high RF performance. Only the ADPLL [15] achieves the minimum RF performance to fulfill BLE requirements for a wideband time-to-digital converter (TDC)-based ADPLL with a lower RO frequency combined with an edge-combiner to generate the 2.4-GHz signal.

Multiplied delay-locked loops (MDLLs) [14], [16], [31] and injection-locked PLLs (IL-PLLs) [7] suppress the jitter accumulation in the PLL by performing a periodic realignment of RO edges to a cleaner reference signal edge. Thus, these PLL architectures achieve high RF performance at the cost of calibration loops to compensate their system nonlinearities (e.g., static-phase-offset (SPO) calibration and two-path

injection technique in [7] or DTC nonlinearity calibration loops [14] such as DTC gain correction loop [16] or DTC range reduction technique [31]).

All the techniques described above increase nevertheless the power consumption of their respective PLL architecture. The power spending per frequency metric highlights the tradeoff between the RF performance and the power consumption which is crucial for IoT applications. The proposed solution has managed this tradeoff by fulfilling the BLE requirements while presenting the smallest power spending per frequency among RO-based PLLs.

For a given power consumption, the *LC*-based PLLs [6], [13] present higher intrinsic RF performance than their RO-based PLL counterparts. As their power consumption is mainly used for biasing purposes, techniques such as phase dithering DTC [6] or switching feedback method [13] enable the *LC*-based PLL to improve their RF performance for minimum power consumption. The *LC*-based PLLs represent the virtuous goals in terms of electrical circuit performance, thus the price to pay being their large area.

Furthermore, all the techniques described above increase the area of their respective PLL architecture. Here comes the discussion related to the normalized circuit area. As reported, the noise filtering techniques of DSM-based PLLs [6], [12] or calibration loops for IL-PLL [7] rise their respective normalized area. Thus, the proposed solution has managed the tradeoff between the RF performance and the area as its normalized area is in line with ADPLL architecture [15], [32] and close to fully synthesizable PLLs [14], [16]. Nevertheless, in a future implementation, the proposed solution can perform an even smaller normalized area by replacing the two analog passive loop filters with digital loop filters [8], [31].

## V. Conclusion

This article presents a novel ULP 2.4 GHz IoT PLL architecture which enables a narrow frequency resolution combined with a wide PLL bandwidth. Based on a dual loop integer-*N* OPLL topology, the proposed PLL architecture provides a behavior similar to conventional fractional-*N* PLL, while having a simplified circuit complexity. Indeed, the frequency resolution is produced by the dual-loop architectural nature of the proposed PLL. The power consumption and the core area are reduced by introducing innovative digital building block solutions.

Implemented in a 28-nm FD-SOI CMOS technology, the proposed PLL architecture is in line with the stringent industrial specifications for BLE IoT applications for BLE applications. Several circuit-level innovations within the PLL enable accurate and robust ULP operation. The proposed digital DFM does not require any extra selective passive filter. It operates with single-ended oscillators implying a reduced power consumption. It requires only quasi-quadrature inputs from the ROs which further reduces the overall power consumption. As the spur performance is the main drawback in OPLL architecture, a robust bootstrapped charge-pump implementation is also presented, enabling a constant reference spur performance over all PLL channels. Finally, the two ROs are implemented with simple single-ended body-bias controlled CMOS inverters. The FD-SOI technology specificities permit to enable interesting frequency tuning range optimization, which at the end of the day has direct impacts in terms of power consumption, design complexity and finally die area.

The proposed Caliper PLL compares positively with a large sampling of the state-of-the-art upon two normalizing parameters: power spending per frequency and normalized area.

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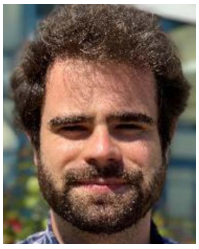

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Dr. Deval was the General Chair of the 2010 RFIC Symposium in Anaheim, CA, USA, the 2012 ESSCIRC-ESSDERC conferences in Bordeaux, France, and is the 2022 LASCAS Symposium in Puerto Varas, Chile.