A Compact Low-Voltage Segmented D/A Converter with Adjustable Gamma Coefficient for AMOLED Displays

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***Abstract*—A compact low-voltage segmented digital to analog (D/A) converter with adjustable gamma correction coefficient is proposed for source drivers of active matrix organic light-emitting diode (AMOLED) displays. The shared resistor-string is separated into several segments. The switching networks for each segmentation could be realized using low-voltage or medium-voltage transistors. The outputs of the segmented DACs are added up by an analog adder to obtain the final DAC value. Compared to the conventional resistor string DAC (R-DAC) with high-voltage transistors, the proposed D/A converter features the layout area reduction by 84.7%, due to the elimination of high-voltage transistors. The proposed segmented DAC is implemented in an industrial 0.25-μm CMOS technology. The measurement results show that the differential and integral nonlinearity of the proposed D/A converter are 0.21 LSB and 1.31 LSB, respectively, which are significantly lower compared to the previously published high resolution DACs. The deviation of output voltages is also reduced by up to 2.9x compared to the previously published high resolution DACs.**

Keywords—DAC, resistor string, gamma coefficient, low-voltage transistor.

I. INTRODUCTION

In recent years, the active matrix organic light-emitting diode (AMOLED) displays have attracted widespread attentions, due to the advantages of high contrast ratio, wide viewing angle, and fast response time [1] – [3]. High performance source driver plays an important role for the mass production of AMOLED displays. Typical source drivers of AMOLED displays include shift register, data latch, D/A converter (DAC), and output buffer [4]. Due to the increase of display resolution, source driver occupies large layout area. Design of compact DAC is critical to reduce the layout areas of source drivers [5].

Resistor string DAC (R-DAC) is widely used in display source driver due to the merit of good gray-level uniformity among different channels, as the resistor string can be shared by all the channels to generate the reference voltages. However, the required resistors and switching transistors increase exponentially with higher display resolution. As shown in Fig. 1, the numbers of resistors and switching transistors for an N-bit conventional R-DAC are 2^N and 2^{N+1}, respectively. For the conventional driving circuit with an 8-bit resolution, the layout area of switching transistors and routing wires would exceed 60% of the whole source driver chip [5].

H. U. Post [6] and C. W. Lu [7] proposed a DAC structure with two-stage resistor strings to reduce the layout area. All the channels share the main resistor string. Each channel owns a separate fine resistor string. The fine resistor string chooses two adjacent voltages from the first stage as reference voltages to generate required voltages for the second stage. For an N-bit (= m+n bit) DAC with two-stage resistor strings, the numbers of resistors and switching transistors are 2^m+2^n and $2^{m+1}+2^n$, respectively, which could reduce the layout area to certain extent. However, the circuit is complicated due to the insertion of fine resistor strings. If the required output voltage increases, the supply voltage also needs to be increased. Furthermore, due to the increase of the operating voltage, the switching network of the conventional DAC circuit must be implemented using high-voltage transistors, which occupy significantly larger layout area than low-voltage and medium-voltage transistors. For example, Seol [2], [9] adopted the 18 V high-voltage transistors and 6 V medium-voltage transistors in a 0.18-μm CMOS technology to fulfil the 12-bit and 10-bit resistor string-buffer combined DAC, respectively. The layout areas are 3954×38 μm^2 and 528×27 μm^2 for the two DACs, respectively. Therefore, the DAC structure with two stages is not suitable for compact DAC for AMOLED displays.

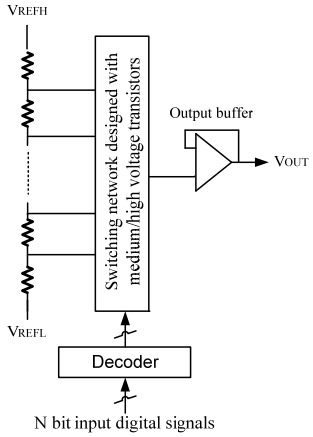

Fig. 1. The structure for a conventional N-bit R-DAC.

In this paper, targeting high-voltage outputs, a low-voltage segmented R-DAC with adjustable gamma coefficient is proposed to reduce the layout area. The shared resistor string is separated into several segments. The output voltage ranges of each segment are ensured to be the same and maintained low-voltages. The switching networks could be therefore designed with low-voltage or medium-voltage transistors. The outputs of each segment are added up by an analog adder to obtain the final high-voltage output. The feasibility of the proposed DAC circuit is well proved by simulation and measurement results using an industrial 0.25-μm CMOS technology. The layout area of the proposed DAC designed with medium-voltage transistors is reduced by 84.7% compared to the design using high-voltage transistors. The differential and integral nonlinearity as well as the deviation of output voltages of the proposed D/A converter are all reduced significantly compared to the previously published high resolution DACs.

This paper is organized as follows. The overall architecture of the source driver of AMOLED displays is presented in Section II. The principle of the proposed DAC is described in Section III. The measurement results of the proposed DAC ciruict are presented in Section IV. The paper is concluded in Section V.

II. ARCHITECTURE OF THE AMOLED DRIVING CHIP

The overall architecture of the AMOLED display driving circuit is shown in Fig. 2. The row driver and source driver provide gate and source signals for the pixel arrays, respectively. The timing controller provides timing signals for the row and source drivers. The reference voltage/current generator provides reference voltages and currents for adders, buffers, and current detections. DAC1, i.e. the display DAC, provides display data for the pixel arrays. DAC2, i.e. the compensation DAC, provides

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compensation information of mobility and threshold voltages for the driving transistors in the pixel arrays. A switching transistor N_T and a feedback line are added on the basis of the traditional 2T1C pixel circuit for current detection. The current flowing through OLED is detected and compared to the standard reference current by the current detections through N_T and feedback lines. The comparison results are stored in external memories and then fed back to the digital circuits to adjust the input digital signals of DAC1. The output voltages of the display and compensation DACs are added to achieve display data with compensation information through an analog adder.

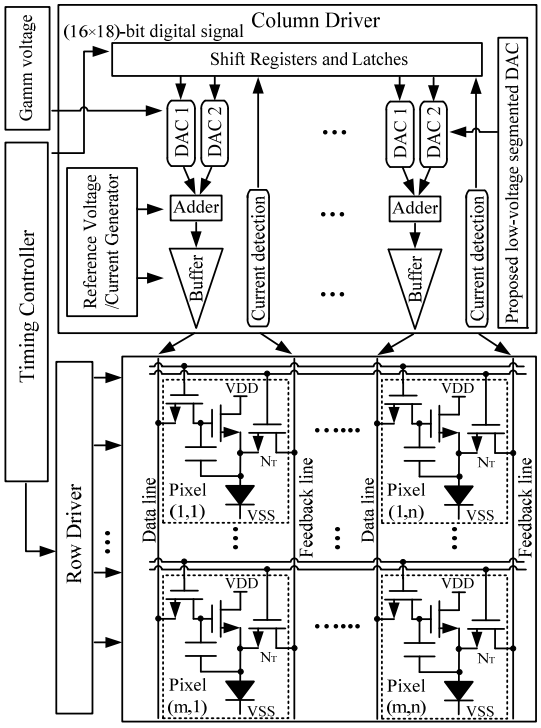

Fig. 2. The architecture of an AMOLED display panel.

III. The Proposed Low-Voltage Segmented DAC

The proposed low-voltage segmented DAC is introduced in this section. The structures of the proposed segmented R-DAC with adjustable gamma coefficient and the analog adder are shown in Fig. 3. According to the required range of output voltages, we could separate the shared global resistor string of the proposed D/A converter into M (M is an integer equal to or greater than one) segments in special gray levels. In the analog adder, the transistors marked with red dashed ellipses are high-voltage transistors, while the other transistors are all low-voltage or medium-voltage transistors.

Compared with the two-stage R-DAC proposed by H. U. Post [6] and C. W. Lu [7], the proposed DAC in this paper enables all DAC channels in the source driver chip to share the global resistor string. Each channel does not need a separate resistor string, which could decrease the complexity of the entire layout. Furthermore, when the required output voltages increase, we could separate the shared global resistor string of the proposed DAC into M segments in special gray levels. The output voltage ranges of each segment are ensured to be the same and maintained low-voltage, according to the supply voltage of switching transistors. Therefore, only low-voltage or medium-voltage transistors are required to design the switching network. The output voltages of M segments can obtain high output voltage through an adder, the principle of which is shown in Fig. 4.

Apart from the panel's brightness, the visual effect of AMOLED displays also depends on the contrast with the background [3], [11], [14]. To achieve better visual effect, therefore, it's necessary to apply gamma voltages in special gray levels to realize gamma correction. To achieve adjustable gamma coefficient of the OLED voltage-gray curves, transistors with equal resistance are used in the resistor string. We could change the gamma voltages applied in special gray levels to realize different output voltages, thereby achieving voltage-gray curves with different gamma coefficients. The output voltage range of each segment is therefore the same for the proposed low-voltage DAC with M segments while the number of gray levels does not need to be the same.

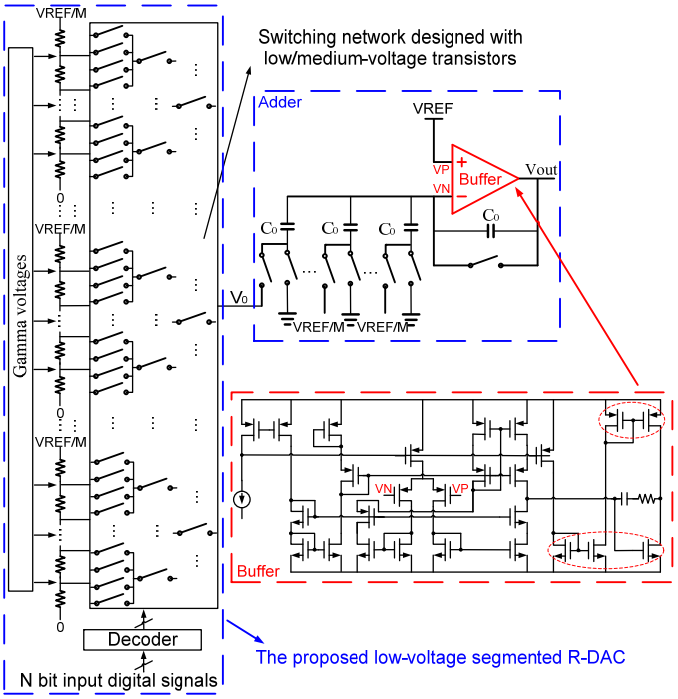

Fig. 3. The proposed N-bit low-voltage segmented R-DAC with the output analog adder.

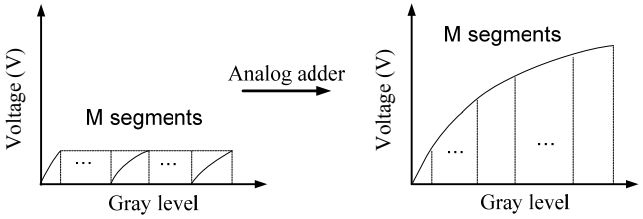

Fig. 4. The principle for the low output voltages of M segments of the proposed R-DAC to realize high output voltage through an analog adder.

IV. Test Results for The Proposed DAC

The proposed low-voltage segmented R-DAC is implemented in an industrial 0.25-μm CMOS technology. We separate the 8-bit resistor string into two segments to verify the feasibility of the proposed DAC. The source driver chip consists of 18 DAC channels. For the DAC module testing, the 8-bit input digital signals varies from 0000 0000 to 1111 1111.

According to the luminance-voltage test results of OLED, we could calculate gamma voltages of different voltage-gray curves and apply to special gray levels in the resistor string to obtain the needed curve. In this paper, the gamma coefficient is 2.2. On the basis of the simulation results, we separate the resistor string into two segments at the gray level of 80 to ensure that the output voltage ranges of the two segments are the same.

A. Test results

The measurement results for the proposed 8-bit R-DAC in the source driver chip are shown in Fig. 5. The proposed structure is separated into two segments: the first segment with gray levels of 0-80 and the second segment with gray levels of 81-255. The output voltage ranges for the two segments are both 0.5-2.5 V. The output voltage curve for the two segments added by the adder is shown in Fig. 5a. The percent error of the output

voltage added by an adder with the segmented DAC is lower than ±1.2% compared to the unsegmented DAC, which is shown in Fig. 5b. The error caused by addition could be further reduced by external compensation algorithm. The comparison between the simulation and measurement results for the proposed 8-bit DAC without gamma voltages is shown in Fig. 6. The output voltage ranges for the two linear segments are both 0.5-2.5 V. We could calculate the parameters which characterize the DAC performance, according to the simulation and measurement results with the proposed 8-bit linear DAC.

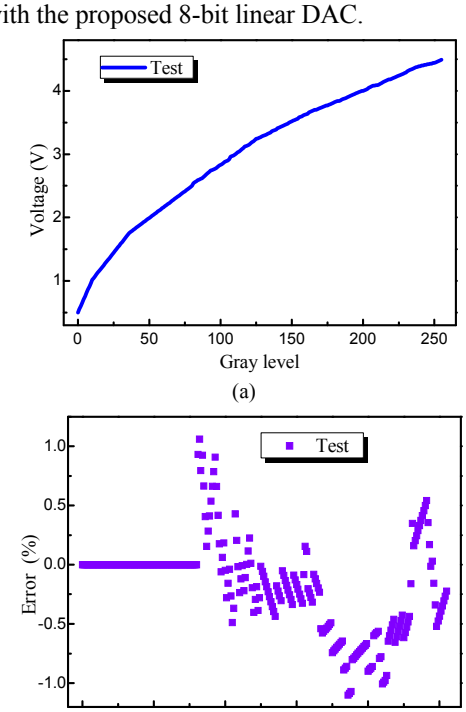

Fig. 5. The (a) measured output voltage curve and (b) percent error added by an adder for the proposed DAC.

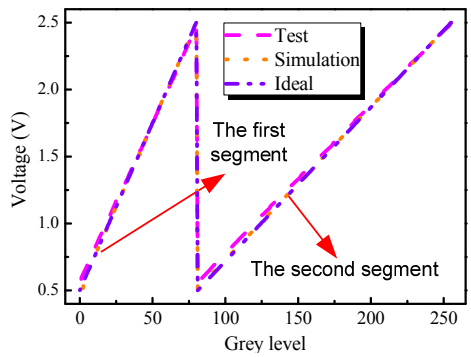

Fig. 6. The comparison results for the proposed DAC without gamma voltages.

B. Parameters for the proposed DAC

1) Setup time and conversion speed

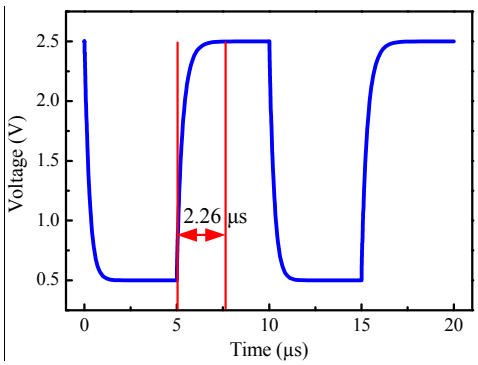

Fig. 7. The measured transient response of the proposed DAC.

Setup time refers to the required time for the output analog voltage to achieve stability (±0.5 LSB), when the input digital signals change. Conversion speed is characterized by measuring the transient response of the DAC circuit. As shown in Fig. 7, the output voltage of the proposed DAC needs 2.26 µs to be stable, when the 8-bit input digital signals change from 0000 0000 to 1111 1111. The output terminal of the DAC circuit is loaded with R_L of 100 kΩ and C_L of 10.5 pF. Therefore, the conversion speed for the proposed DAC is 0.88 V/µs. From the conversion speed, we can see the changing speed of the output voltages varying with the 8-bit input digital signals for the proposed DAC. With the same loading, the measured setup time with the proposed DAC is reduced by 3x compared to the resistor-current combined DAC [3], where the measured setup time is 6.8 µs.

2) Differential and integral nonlinearity

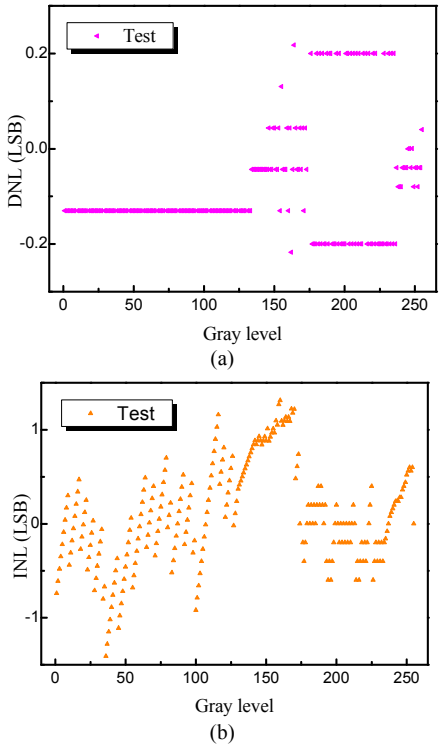

Fig. 8. The measured (a) DNL and (b) INL values for the proposed DAC.

The existence of non-ideal effect in circuits would lead to certain deviation between actual and ideal output values. The test results of differential nonlinearity (DNL) and integral nonlinearity (INL) for the proposed 8-bit segmented lineal DAC are shown in Figs. 8a and 8b, respectively. The ranges for the DNL and INL are -0.21 ~ 0.21 LSB and -1.28 ~ 1.31 LSB, respectively. Y. J. Jeon [5] and C. W. Lu [8] both had proposed R-DAC structures, the DNL and INL values of which are (0.37 LSB, 1.71 LSB) and (3.83 LSB, 3.83 LSB), respectively. Compared to these two R-DACs, the non-ideal effect and difference between the actual and ideal output voltages are smaller with the proposed low-voltage segmented R-DAC.

3) Deviation for the output voltage

The uniformity of DAC channels in the source driver chip could be characterized by measuring the deviation of output voltages (DVO) between different channels [5]-[9]. We obtain the DVO values by measuring the output voltages of the 1st, 6th, 12th, and 18th channels according to 256 gray levels as shown in Fig. 9. The maximum DVO values of the 1st, 6th, 12th, and 18th DAC channels are 9.3 mV, 8.6 mV, 8.5 mV and 7.5 mV, respectively. The inter-channel deviation is mainly related to the global resistor string variations caused by process and the voltage offset of output buffers. Compared to the DVO values of 22 mV and 15.9 mV for the 10-bit two-stage R-DAC [7] and

resistor-buffer combined DAC [10], the DVO value is reduced by up to 2.9x and 2.1x, respectively, with the proposed DAC. Therefore, the proposed low-voltage segmented R-DAC is able to improve the output voltage uniformity of different DAC channels in the source driver chip, which would increase the display uniformity and achieve better display effect.

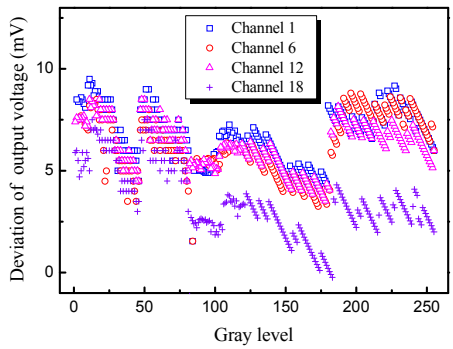

Fig. 9. The measured DVO values for different DAC channels.

4) Layout for the proposed DAC

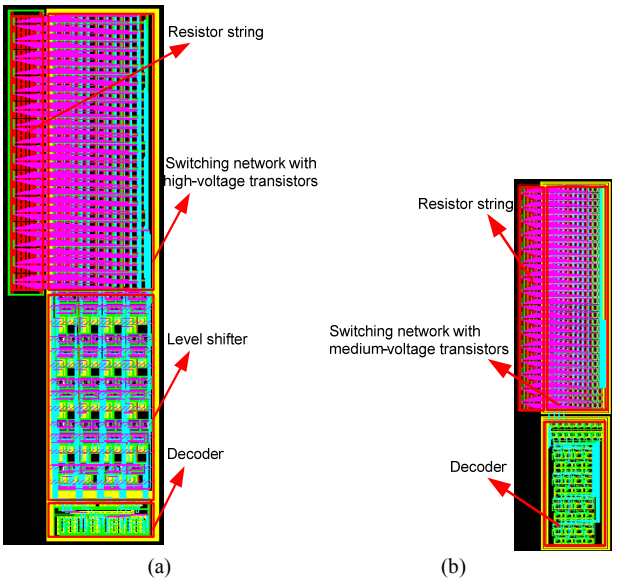

Fig. 10. Layout for the proposed DAC designed with (a) high-voltage transistors and (b) medium-voltage transistors.

The switching networks designed with high-voltage and medium-voltage transistors for the proposed DAC are shown in Figs. 10a and 10b, respectively. The layout area for the whole design is 179.14×1177.47 μm^2, if we adopt high-voltage transistors to design the switching network of the proposed DAC in each channel. Alternatively, the proposed design with medium-voltage transistors has a layout area of 56.92×565.27 μm^2, which achieves an area reduction of 84.7%. Therefore, compared to the traditional R-DAC designed with high-voltage transistors, the proposed DAC designed with medium-voltage transistors could reduce the layout area significantly.

The micrograph for the proposed 8-bit two-segmented R-DAC with 18 channels in the source driver chip is shown in Fig. 11. For the test of the source driver chip, the required digital signals are generated by Verilog HDL codes, which are downloaded to the FPGA test board through the input PADs of the chip on the PCB board.

A comprehensive comparison between the proposed R-DAC and other high-resolution DACs in the literature are summarized in Table I. The proposed DAC exhibits good performance in terms of nonlinearity and uniformity.

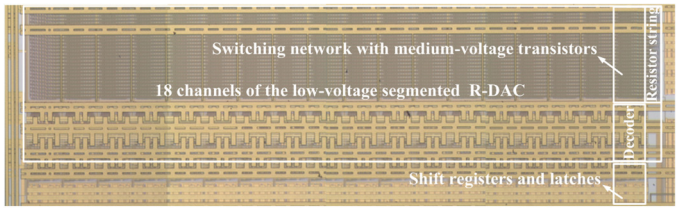

Fig. 11. The micrograph of 18 channels for the proposed DAC that is fabricated in an industrial 0.25-μm CMOS technology.

V. Conclusions

We propose a compact low-voltage segmented R-DAC with adjustable gamma coefficients, which could be applied in the source driver of AMOLED displays. The shared resistor string is separated into several segments. The high-voltage output is achieved through an analog adder. The switching network therefore could be designed with medium-voltage transistors while the output voltages of each segment maintain low values. The proposed segmented DAC therefore has a layout area reduction by 84.7% compared to the traditional R-DAC. The proposed DAC is fabricated in an industrial 0.25-μm CMOS technology. The measurement results show that the percent error for the output voltage added by the analog adder is smaller than ±1.2%. Furthermore, the measured differential and integral nonlinearity are 0.21 LSB and 1.31 LSB, respectively, which are significantly lower compared to the previously published high resolution DACs. The deviation of output voltages is also reduced by up to 2.9x compared to the previously published high resolution DACs. The proposed low-voltage segmented R-DAC is therefore promising for high-end AMOLED displays.

Acknowledgement

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Table I. Comparison Between the Proposed DAC and the Related Works in the Literature.

Parameters	Traditional	[3] JDT	[5] JSSC	[7] JSSC	[8] JSSC	[9] JDT	[10] JSSC	[13] TCAS-I	[14] TCSVT	[15] TCAS-I	This paper
CMOS process / μm	0.25	0.35	0.1	0.35	0.35	0.18	0.35	0.35	0.35	0.35	0.25
Supply voltage / V	5, 10	3.3/5	1.5/5	5	5	1.8, 18	5	5	5	3.3	5
High voltage transistors	yes	no	no	no	no	yes	no	no	no	no	no
Resolution / bit	8	8	10	10	10	12	9	8	10	12	8
Channels	18	240	240	15	4	640	20	30	-	60	18
DNL / LSB	-	0.4	0.37	1.37	3.83	0.26	0.44	0.35	1.3	0.49	0.21
INL / LSB	-	0.43	1.71	1.45	3.84	0.54	0.58	0.34	2.13	1.51	1.31
DVO / mV	-	42	6.35	22	7.0	7.42	15.9	13.2	4.9	9.3	7.3
Area of one channel / μm^2	210683	-	6622	9660	63000	150252	13200	40960	52670	46500	32165

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