A Digital Intensive Fractional-N PLL and All-Digital Self-Calibration Schemes

Ping-Ying Wang, Jing-Hong Conan Zhan, Hsiang-Hui Chang, *Student Member, IEEE*, and Hsiu-Ming Sherman Chang

***Abstract*—A digital intensive PLL featuring a digital filter in parallel with an analog feed-forward path and a digital controlled oscillator (DCO) is presented. Digital loop filter replaces analog passive filter to reduce chip area and associated gate-leakage in advanced process. It also allows the PLL loop gain and DCO gain to be digitally calibrated to within 100 ppm within 50 μs. Such fine frequency resolution enables the PLL to accurately compensate for the loop parameter variation due to process, voltage and temperature (PVT). The analog feed-forward path is insensitive to quantization error of fractional-N divider and DCO nonlinearity. Direct modulating the DCO frequency and phase through the analog feed-forward path, and compensating the modulating signal digitally for the DCO gain variation are demonstrated. At 3.6 GHz all fractional spurs are under −75 dBc. The phase noise at 400 kHz and 3 MHz are −115.6 dBc/Hz and −134.9 dBc/Hz, respectively. The chip is fabricated in a 0.13 μm CMOS process, and occupies an active area of 0.85 mm^2 and draws 40 mA from a 1.5 V supply including all auxiliary circuitry.**

***Index Terms*—All-digital PLL, analog feed-forward path, digital controlled oscillator, digital intensive, direct frequency modulator, fractional-N, loop gain calibration.**

I. Introduction

DIGITAL intensive RF design is of great research interest recently: RF circuit requirements could be relaxed because the possibility of digitally repairing RF impairments; and designs could migrate to different technology node or foundry relatively more effortlessly. One example application is the direct-frequency-modulated (DFM) PLL [1], [2], where the base band signal is pre-emphasized digitally to compensate for PLL low-pass response [1]. The PLL loop bandwidth can therefore be optimized for noise filtering while high data rate modulation is still possible. However, mismatch between PLL loop bandwidth and the digital pre-emphasis filter will result in significant transmission signal quality degradation. Precise control for loop parameters such as VCO gain and loop gain and improving robustness against PVT are keys for mass production of these DFM PLLs.

All-digital PLLs (ADPLLs) [2]–[7] are one candidate architecture for DFM PLLs: digital loop filters can be precisely controlled and reduces area gate-leakage current in advanced process; and real-time digital calibration can compensate for PVT variation. However, these ADPLLs still suffers from the limitations described below.

First, in high-order delta-sigma modulated fractional-N ADPLLs, nonlinearity of the loop would introduce fractional spurs. Time-to-digital converter (TDC) quantization error, nonlinearity, meta-stability, and the DCO nonlinearity all contribute to loop nonlinearity. The choice of bandwidth for such PLLs involves a more demanding tradeoff between fractional spur/quantization noise and DCO noise when compared to a conventional charge pump PLLs. Furthermore, the spurs caused by nonlinearity cannot be eliminated by a digital loop filter, because there is still finite truncation error of the digital loop filter limited by the DCO.

Second, there is another difficulty in designing a large dynamic range, fine resolution TDC with minimum area overhead. A ring TDC [3], [4] could significantly reduce the required area, but it is more prone to supply noise because jitter accumulate through the ring. The inverter-based TDC also induces large transient current [4], and an additional dedicated power pin with a heavy external cap is usually necessary [4].

Third, even if the above mentioned problems are solved, the loop gain of the ADPLL depends on TDC resolution and DCO gain, unfortunately both are PVT sensitive parameters. The argument that ADPLLs are more robust than their traditional analog counter part is therefore not all valid.

Finally, although the TDC only uses digital logic, the high resolution, critical timing matching, and tight parasitic capacitance requirements usually do not allow such blocks to be synthesized from hardware description languages. Significant custom design efforts are still required, which would be comparable to designing a traditional analog PLL.

This paper presents a digital-intensive fractional-N PLL [8], [9] to address the aforementioned problems except that the design is still full custom. The noisy TDC is replaced by an analog feed-forward path which eliminates the noise and fractional spur, has good PSRR, and produces lower transient current noise. The integral path maintains benefits of using digital filters. The synthesizer is insensitive to nonlinearity and quantization error of DCO, relaxing the DCO design requirements compared to conventional ADPLLs. Loop gain and DCO gain can be digitally calibrated to within 100 ppm. All loop parameters are represented by digital codes, therefore the PLL can be precisely compensated in real-time, regardless of PVT variations. Such compensation is important for DFM PLLs. Since the loop and DCO gain represented by the digital codes

Manuscript received December 01, 2008; revised March 05, 2009. Current version published July 22, 2009.

P.-Y. Wang, J.-H. Zhan, and H.-H. Chang are with the RF Division, MediaTek Inc., Hsin-Chu, Taiwan (e-mail: py.wang@mediatek.com).

H.-M. Chang is with the Department of Electrical Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106-9560 USA.

Digital Object Identifier 10.1109/JSSC.2009.2022304

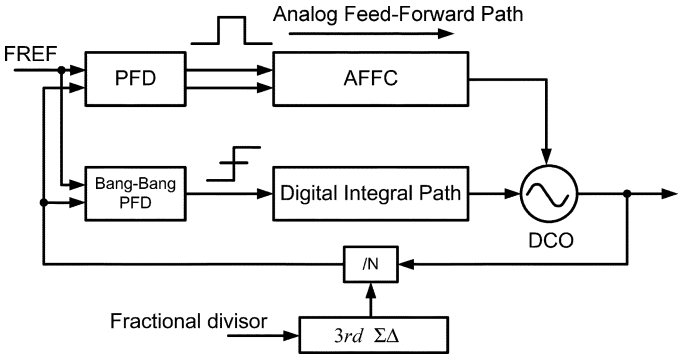


Fig. 1. The block diagram of the digital intensive PLL.

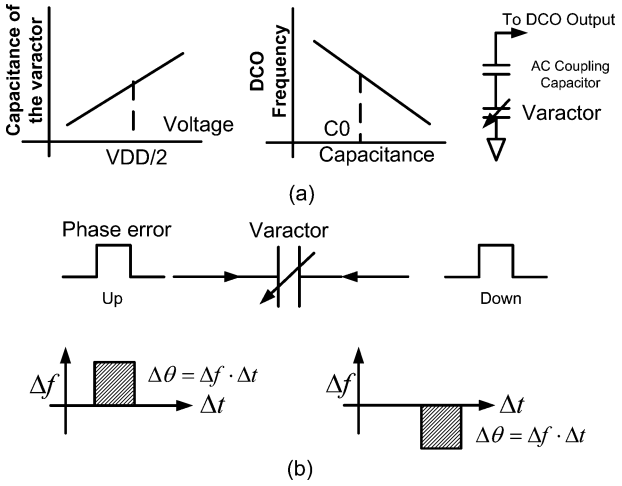


Fig. 2. (a) Operation principle of AFFC: Frequency change is inversely proportional to the capacitance change to the first order approximation. (b) Operation principle of AFFC: Frequency change is linearly proportional to the phase error.

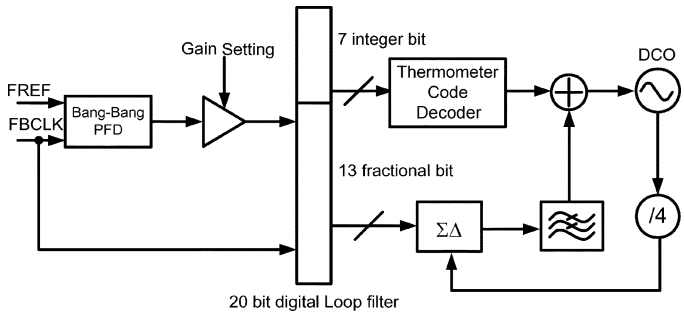


Fig. 3. The block diagram of the digital integral path.

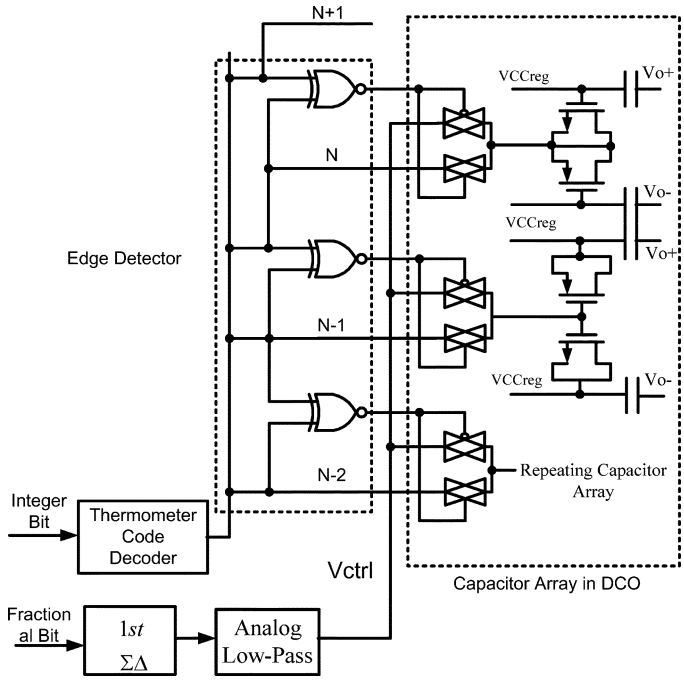


Fig. 4. The block diagram of the interface between the digital loop filter and DCO.

through the proposed self-calibration are dependent on PVT, the history of the PVT variation can be recorded by storing the digital codes in memory.

This paper is organized as follows. In Section II, the proposed digital intensive PLL architecture is presented and its loop dynamic is analyzed. Details of individual sub-blocks are shown in Section III. The calibration algorithms are described in Section IV. In Section V, DFM is demonstrated using the proposed digital intensive PLL architecture. Experimental results are provided in Section VI, followed by conclusions in Section VII.

II. Proposed Digital Intensive PLL Architecture

The block diagram of the proposed synthesizer is shown in Fig. 1. In the integral path, the frequency of the reference clock is sampled by a bang-bang PFD and is integrated digitally. The proportional path consists of a conventional PFD and an analog feed-forward circuits (AFFC). The AFFC corrects phase in the time domain using output generated from a conventional PFD, where the relation among frequency, capacitance and control voltage is shown in Fig. 2(a). The correction of phase is linearly proportional to the phase error because the frequency/phase change of the DCO is linearly proportional to change of the capacitance, as shown in Fig. 2(b). TDC is replaced by the combination of analog feed-forward circuit and the bang-bang operation, which produces much less switching noise than TDC.

The detailed digital integral path circuit is shown in Fig. 3. It has a 4-bit gain control, a 20-bit digital loop filter to replace the large zero capacitor in a conventional analog PLL, a 13-bit first order delta-sigma modulator (SDM) following by a third order analog low-pass filter, an edge detector and a 7-bit thermometer code decoder. 5 Hz effective frequency resolution is achieved by 900 MHz first order SDM to dither the fractional capacitor which has the same capacitance as the integer bit has. The shaping noise of the first order SDM is filtered by the third order analog low-pass filter [10]. The tracking bit frequency monotonicity is maintained as explained below. Every capacitor is thermometer-coded, and can be switched to be either fractional bit or integer bit. The capacitor representing an integer bit or a fractional bit is determined by the edge detector in Fig. 4. Note that there will be only one fractional capacitor in the whole tracking capacitor array. Since these capacitors are thermometer-coded, and the way the DCO has the folded frequency transfer curve, the tank capacitance vs. fractional control voltage

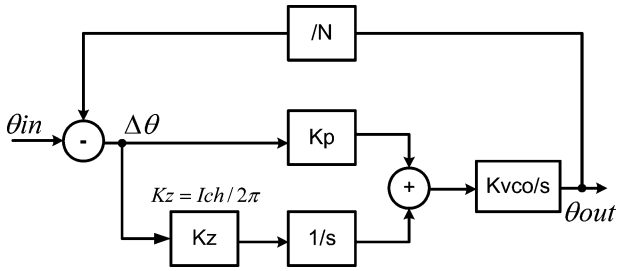


Fig. 5. Linear model of the conventional dual path PLL.

is always continuous. The bang-bang operation also limits that only one unit capacitor in the DCO is switched when an update is necessary to compensate for phase error. Switching noise is therefore reduced.

In the next paragraph, comparison between a dual-path PLL [11]–[13] and our design will show that in the proposed architecture, the loop bandwidth is determined by the gain in the analog feed-forward path, and the gain variation induced by bang-bang operation in the integral path has no impact on loop bandwidth.

The linear model for the PLL with a dual path loop filter is shown in Fig. 5. The open loop gain of the PLL is

$$H_{con}(s) = \left(K_p + \frac{K_z}{s \cdot C}\right) \cdot \frac{K_{vco}}{N \cdot s}. \tag{1}$$

The coefficient for the $1/\mathrm{s}^2$ term represents the gain of the integral path:

$$\frac{Ich \cdot Kvco}{2\pi N \cdot C}. \tag{2}$$

This expression shows that the gain of the integral path is constant and inversely proportional to the capacitance of the loop filter in a conventional charge pump-based PLL. For the typical case where the DCO operating at 3.588 GHz, the gain of the integral path is about 10^{10} while the gain of the VCO is 10 MHz/V, the charge pump current, Ich, is 600 μA, divisor, N, is 138 and the capacitance, C, is 600 pf in typical case.

In our design, the integral path circuits track the frequency of the reference clock in the digital domain. The gain of the integral path is no longer linearly proportional to the phase error. Instead, the gain of the integral path is constant for arbitrary phase error. The coefficient now becomes phase-error-dependent:

$$\frac{\Delta f}{2\pi \cdot \Delta te \cdot N} \tag{3}$$

where Δf (5 Hz in this design) is the step size of the frequency correction and Δte is the timing error produced by the PFD. Since a third order MESH 1-1-1 SDM is used in the fractional divider, the phase error is dominated by the dithering noise of the SDM ranging from -3 Tvco to 4 Tvco. Accordingly, the gain of the integral path varies from $10^6 \sim 10^7$, which is $1/10^3 \sim 1/10^4$ compared to conventional charge pump PLL described in (2). The equivalent capacitance represented by the digital loop filter is therefore $10^3 \sim 10^4$ times that of the conventional analog loop filter, which is up to uF order.

Large capacitance leads to a high damping factor and reduces jitter peaking. This is a type I loop filter characteristic. As a result, the loop bandwidth is only affected by the AFFC with the linear phase correction [14]:

$$\omega_{-3\ \mathrm{dB}} = K_p \cdot K_{vco}/2\pi N. \tag{4}$$

Validation of the above analysis will be supported by measurements in Section VI.

III. Detailed Building Blocks of the Proposed PLL Circuit

A. DCO

Fig. 6 shows the simplified schematic of the LC-DCO [15]. The supply is regulated by an on-chip low-drop-out (LDO) regulator to generate the required voltage for the DCO. Switchable resistors set the current consumption and oscillation amplitude of the DCO, improves common mode rejection, and reduces the effect of noise and spurs generated from DCO ground. The capacitive tanks are comprised of a PVT tank for process/voltage/temperature variation compensation; an acquisition tank (ACQ) for fast frequency acquisition; and a tracking (TRK) tank which has low gain when the PLL operates in lock mode. The PVT, ACQ and TRK tanks provide roughly 7 MHz, 200 kHz and 20 kHz per unit step, and each of them is controlled by a 7-bit control word to cover the required frequency range of 3.2 GHz to 4.0 GHz. Among the three tanks, the PVT tank has the highest gain. Therefore metal-insulator-metal (MIM) capacitors instead of MOSFET based capacitors are chosen to reduce supply pushing. To reduce the amount of redundant capacitance, this tank is binary-code controlled; but the layout is unit-cell-based to improve frequency monotonicity. The NFET switches are sized to provide low on resistance $(\mathrm{r_{ds}})$ when the MiM cap is switched into the tank. The PFET switches are minimum sized to have high on resistance $(\mathrm{r_{ds}})$ when the MiM cap is switched out of the tank. PFET switches prevent the drain terminal from floating when the MiM cap is disconnected from the tank. The acquisition and tracking tanks use MOSFET for their much finer frequency step and much smaller area. These two tanks are thermometer coded for better matching, which also improves frequency monotonicity. For the tracking tank, it is further split into even and odd tanks, as illustrated in Fig. 6. Only one capacitor in the 128 capacitor array of the tracking bit is selected to be sigma-delta modulated. The rest of the tracking bits are controlled digitally to add or remove capacitance from the tank. The matching requirement among each tracking bit is thus relaxed. Only frequency monotonicity is important. Complex dynamic element matching mechanism is not necessary. Slight gain variation for different tracking bit can be digitally calibrated and compensated. The voltage-to-frequency transfer curve of the proposed tracking tank is folded and avoids frequency discontinuity when compared to traditional designs, as illustrated in Fig. 7. The folded transfer curve results from the opposite polarity of the even and odd tracking bits. Assume the current tracking tank selects the M-th sub-band, and the target frequency is within the $\mathrm{M}+1$-th sub-band. For the proposed tracking tanks design, the sigma-delta modulated voltage will approach zero first, the tracking bit control toggles digitally

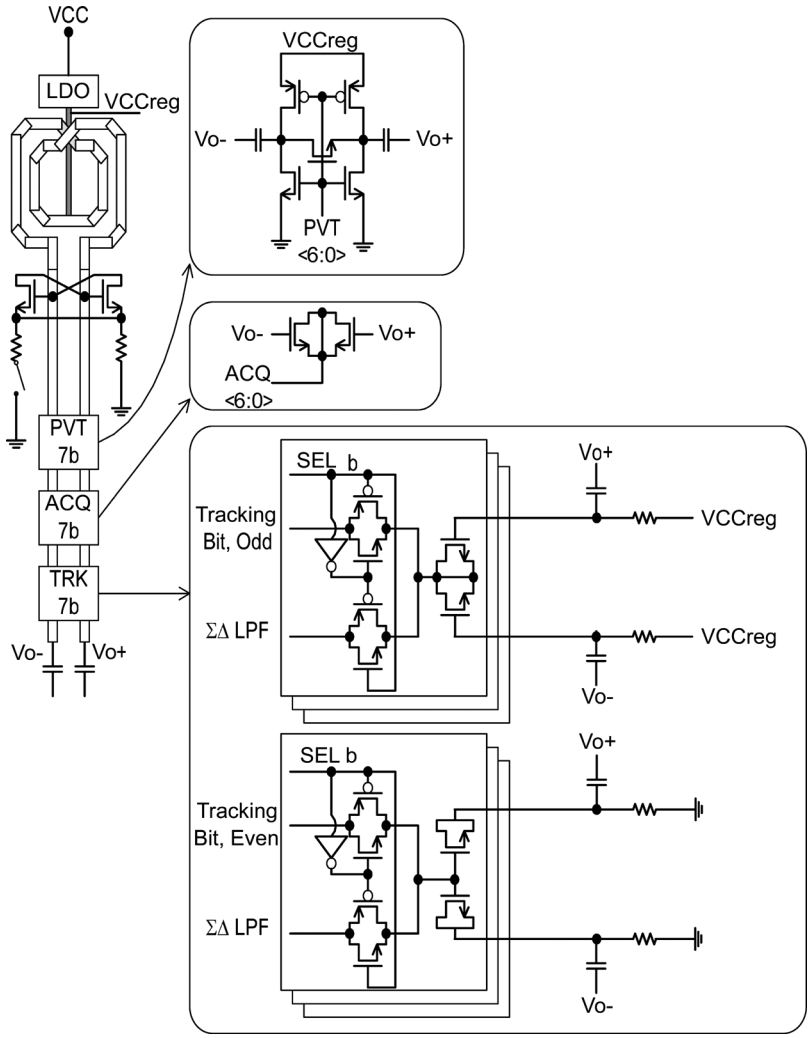


Fig. 6. Detailed schematic of the DCO.

from M to $\mathrm{M}+1$, and the sigma-delta modulated voltage then charges to the desired value. If a conventionally designed tank is used, the control voltage also approaches zero first, but when the tracking bit toggle to $\mathrm{M}+1$, there is a significant frequency discontinuity, because the sigma-delta modulated voltage cannot suddenly be charged to the new target value. This discontinuity will cause undesired spurs and may even lead to temporary out of lock. The two frequency tracking processes are highlighted in Fig. 7. Fig. 8 shows an example simulation of the transfer-curve of three consecutive tracking bits. It can be clearly observed that the frequency transfer-curve is folded.

B. Analog Feed-Forward Circuits

Shown in Fig. 9 are several topologies which could implement the desired analog feed-forward function. The simplest is the voltage mode AFFC where a varactor is connected directly to the output of a conventional PFD as shown in Fig. 9(a). The phase error output of a conventional PFD controls the phase of the DCO by changing the capacitance of the varactor. The correction of the phase is linearly proportional to the phase error. It is the simplest and produces the least noise. However, the loop gain is low and is limited by the supply voltage of PFD. A current mode AFFC, as shown in Fig. 9(b) where its common mode is biased at VDD/2 by a resistive voltage divider, is preferred over the voltage mode AFFC in Fig. 9(a), because it provides higher gain and beter PSRR with differential implementation. A low-pass filter (LPF) filters out transient ripples. Pseudo-differential implementation shown in Fig. 9(c) was chosen to further reduce area, which requires only half the size of the LPF. The output node of the AFFC $\mathrm{Vo}+$ and $\mathrm{Vo}-$ in Fig. 9(c) are connected to the same nodes of the DCO in Fig. 6.

The gain of AFFC is proportional to the voltage coefficient of the varactor at common mode voltage (VDD/2). In a conventional analog PLL, the VCO gain will depends on loop filter voltage variation due to PVT and residual frequency error after sub-band calibration. In contrast, this design is insensitive to such factors.

C. Bang-Bang PFD

The implementation of the bang-bang PFD is shown in Fig. 10. It consists of two latches with cross-coupled path. The circuit topology is symmetric to minimize the mismatch between reference and feedback path. When the reference

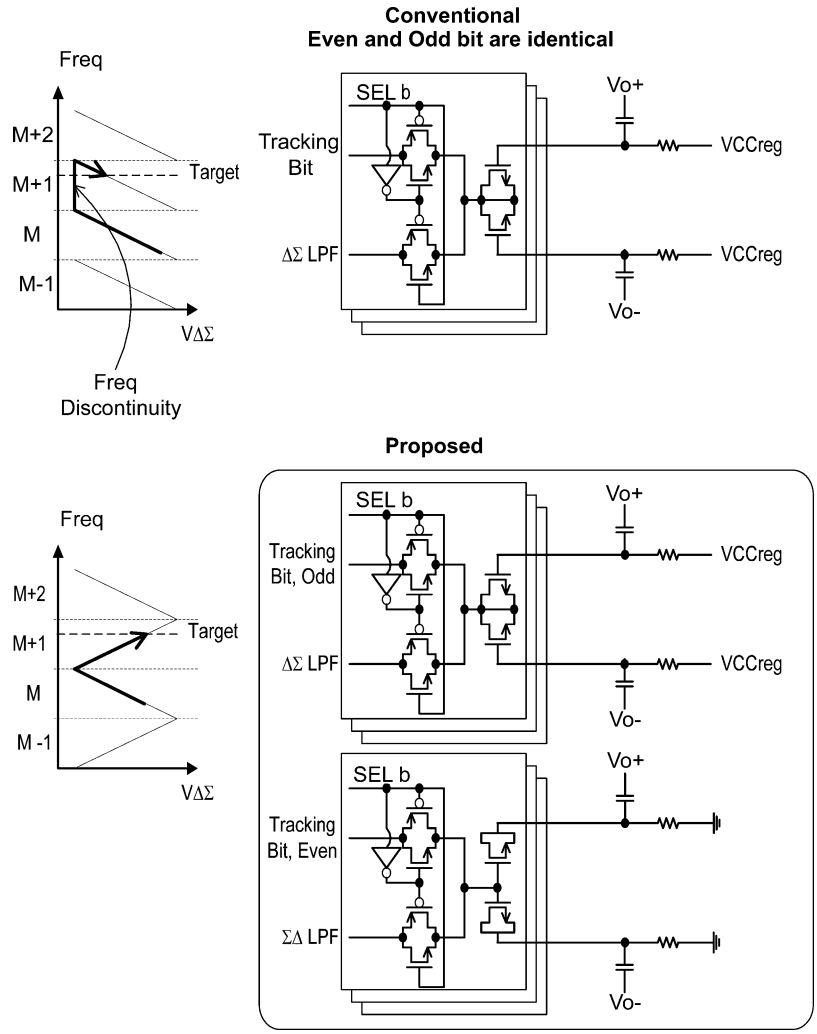


Fig. 7. Conventional and proposed tracking bank.

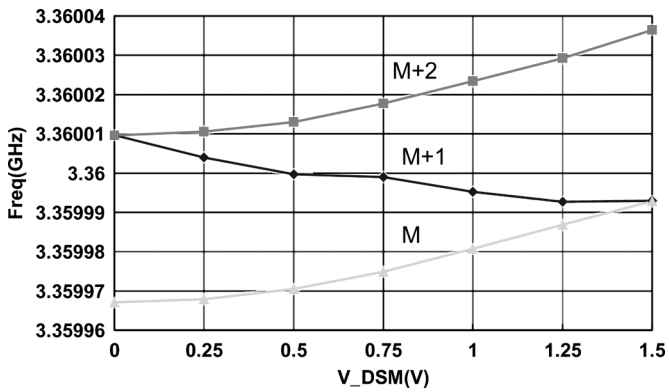


Fig. 8. Simulated tracking bit transfer-curve. Exact values of $\mathrm{TRK}\langle 6:0\rangle$ are arbitrarily chosen for demonstration purpose.

clock is lead, the output voltage of the reference path is rising first so the transistor M4 in the feedback path is disabled and M3 is turned on to pull down the output of the feedback path. Finally, the output voltage of the lead signal is changed to logic high while the output voltage of the Lag signal keeps the ground level. Accordingly, the sign of the phase difference is distinguished.

The devices mismatch and noise between two paths will result in static phase error and meta-stability. Monte Carlo simulation shows that the static phase error is 5 ps in the worst condition which the largest mismatch threshold voltage is 10 mV. By using Monte Carlo simulation with transient noise, three sigma of the meta-stability is below 1 ps. The jitter induced by the meta-stability is under the phase noise contributed by the analog feed-forward path, which will be supported by the measurement results in Section VI.

When the phase difference between reference and feedback clock is equal to the opposite static phase error in the bang-bang PFD, the bang-bang PFD will produce lead and lag signal with the same probability so that the digital loop filter for frequency tracking will converge to the steady state. Accordingly, the steady state of the loop is that the phase difference between reference clock and feedback clock is equal to the opposite static phase error in the bang-bang PFD. The frequency error induced by the static phase error in the bang-bang PFD will be compensated for by the analog feed-forward path through adjusting the

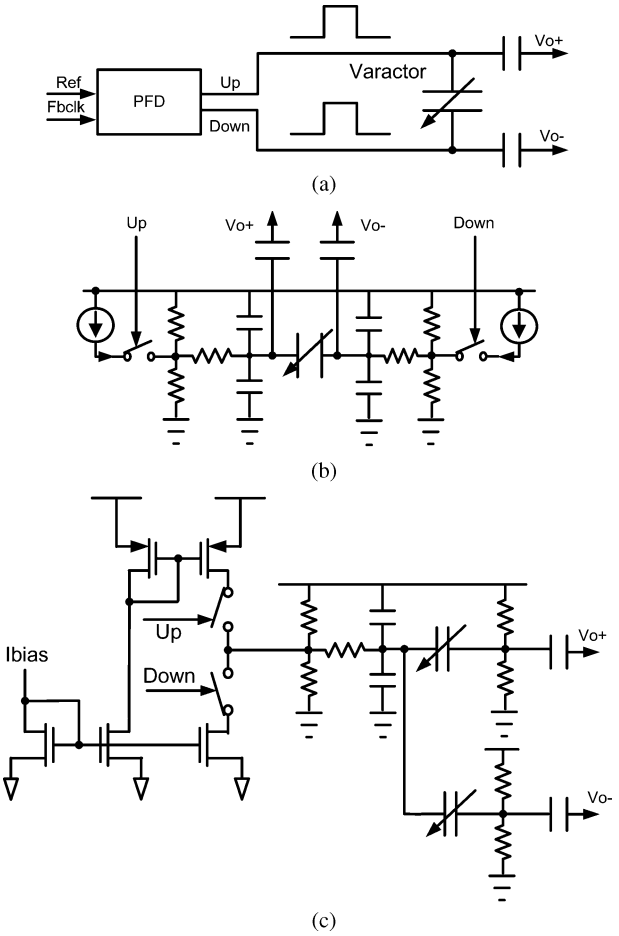


Fig. 9. (a) Voltage mode AFFC. (b) Differential current mode AFFC. (c) Pseudo-differential current mode AFFC.

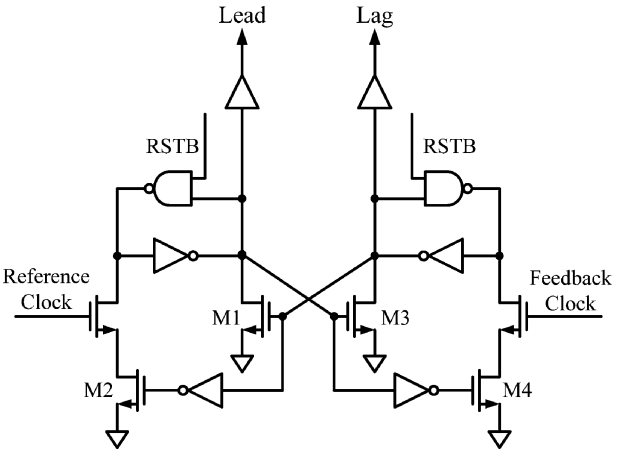


Fig. 10. Schematic of the bang-bang PFD.

control voltage in AFFC because opposite static phase error exists between the reference and feedback clock.

The induced frequency offset in the analog feed-forward path to compensate the frequency error induced by the static phase error in the bang-bang PFD is calculated as

$$\Delta t \cdot Ichp \cdot R \cdot K_{vco}/Tref \tag{5}$$

where Δt is the static phase error which is 5 ps, $Ichp$ is the charge pump current in the AFFC, which is 600 μA, R is the resistance of the loop filter which is 10 kΩ, VCO gain is 10 MHz/V and $Tref$ is the period of the reference clock, which is 38.4 ns in this design. The induced frequency offset is about 7 kHz.

However, the frequency offset induced by the bang-bang PFD have no impact on the accuracy of the calibration proposed in the following section because 1) it has been compensated for by the analog feed-forward path as mentioned above and the output of the DCO has no offset for the target frequency, and 2) the different loop configurations used in the self-calibration take the same PFD in the analog feed-forward path and bang-bang PFD, thus the offset is cancelled.

IV. Self-Calibration Scheme

The most attractive feature of the design is that the critical analog design parameters including loop gain and DCO gain can be calibrated digitally so the history of the loop/DCO gain variation with PVT can be represented by digital codes which can be recorded by memory and gain variation can be compensated in the digital domain. The principle of the calibration is that the static phase error of the type I loop is the function of the frequency error induced by a frequency step, which can be measured by the bang-bang PFD.

The digital calibration circuitry could be fully synthesized and does not require custom designed high-speed logics as in the cases of TDC [4] or high-speed ADCs. The calibration circuitry settles to 100 ppm within 50 μs, therefore real-time calibration to track PVT variation for burst mode communication is possible. For reference, GSM/GPRS/EDGE/BT has 200 $\sim$ 300 usec blank time before transmitting data. The principle of the calibration is based on switching loop dynamic between type I and type II PLL as explained below.

The difference between type I and type II PLL is that type II PLL has a capacitor integrating phase errors to track reference frequency drift so that there is no static phase error between reference clock and feed-back clock from divider output [16]. Equivalently, if the integration capacitor is removed, the type II PLL cannot track such input frequency drift; its dynamic becomes type I. For type I PLL, the mentioned frequency drift results in a static error which the loop will try to compensate for. By measuring this error, the frequency drift is known and could be calibrated.

The proposed self-calibration is to measure the static phase error by adjusting the fractional divisor of the divider in the feedback path to compensate for the static phase error until the static phase error is eliminated. As a result, the fractional divisor adjusted is equal to the frequency drift which is the frequency of the input clock multiplied by fractional divisor. Since the divisor is represented digitally and the fractional divider and the bang-bang PFD is embedded in the PLL, the calibration is all digital without extra full custom design circuit.

A. DCO Gain Calibration

Fig. 11 shows the digital self-calibration loop to calibrate DCO gain. Since a separated proportional and integral loop filter is used, the PLL can be switched between type I and type II

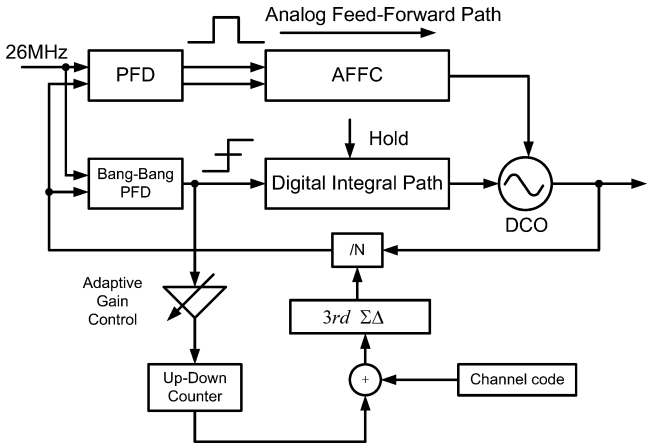


Fig. 11. Block diagram of the all-digital DCO gain calibration.

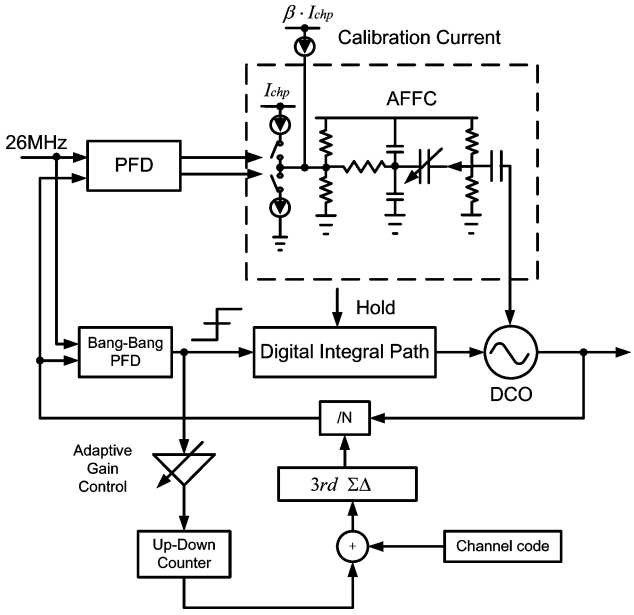


Fig. 12. Block diagram of the loop gain calibration in the analog feed-forward path.

by holding digital loop filter. When the calibration starts, the digital loop filter is held and the PLL becomes type I when the fractional divisor is $N.F1$. Meanwhile, the DCO control code is added code ΔC. After the closed loop settles, the type I PLL will generate a static phase error to compensate for the frequency difference between the reference frequency and the divided output frequency, so the bang-bang PFD will tilt toward either a phase lead or lag. The digital output of the bang-bang PFD is amplified by an adaptive gain circuit and then accumulated in an up-down counter. The result of the up-down counter is added with fractional divider's channel code so the divider ratio can be adjusted according to the direction of the phase lead/lag. When the static phase error is close to zero, the bang-bang PFD will indicate equal opportunity of phase lead or lag and the divisor of divider will converge. The converged divisor with fractional code is recorded as $N.F2$. As a result, the DCO gain $\Delta f/\Delta C$ is equal to $Fref*(N.F2-N.F1)/\Delta C$ which is calculated all digitally.

The resolution of the calibration is determined by the resolution of the frequency step of the PLL, which is $\Delta f = 1/2\hat{}23 * Fref$. With a 26 MHz reference frequency, the finest resolution is 3.099 Hz. However, there is a tradeoff between the calibration resolution and the time needed for the convergence. To speed up the calibration process while getting the finest resolution, an adaptive gain circuit is applied.

B. Loop Gain Calibration

Fig. 12 shows the functional diagram for the proposed calibration technique. When a current mirrored from the charge pump current with a ratio of β is injected into a resistor, the capacitance changes due to the voltage drop $\beta * \mathrm{Ichp} * \mathrm{R}$ in the proportional path, inducing a frequency offset is. At the same time, the loop is switched to type I loop by digitally holding the digital loop filter. The self-calibration method mentioned in DCO gain calibration can be applied to find the frequency offset digitally so the loop gain can be calculated as describe below.

The loop gain in the AFFC is defined as the frequency variation of the DCO divided by the voltage variation in the varactor which is $\Delta\mathrm{f}/(\beta\mathrm{Ichp}*\mathrm{R})$ multiplied by charge pump current and resistor in the loop filter, and the -3 dB frequency according to (4) is

$$\omega - 3\,\mathrm{dB} = \Delta f/\beta \cdot 2\pi N \tag{6}$$

where Δf is the frequency variation when the current is injected into the resistor. Since β is well defined by device geometry ratio, (6) shows the -3 dB frequency only depends on Δf, which can be self-calibrated as already described above.

It should be emphasized that in this architecture, an extensive sets of analog design parameter can be digitally monitored and calibrated, e.g., DCO's frequency pushing and charge pump current mismatch in the AFFC.

V. Digital Intensive RF Example: All-Digital Modulator

The block diagram of the modulator is shown in Fig. 13. During modulation, the modulation data is simultaneously sent to the fractional-N divider and the DCO.

The modulation signal passes through the fractional-N divider path, which has low-pass characteristic of the PLL transfer function. With a 26 MHz reference, the 23-bit third-order SDM provides a 3 Hz frequency resolution. On the other hand, the modulation signal passes through the DCO, which has the high-pass characteristic DCO noise transfer function. The modulation output is the sum of the modulation signal from the two modulation paths. With proper high-pass and low-pass combination, the baseband data could have an all-pass transfer function [17]. The PLL loop bandwidth then can be optimized solely for noise performance. At any given time, low error modulation could be guaranteed if the modulation frequency from the fractional-N divider path, $\Delta N.f/2\hat{}23 * Fref$, equals the modulation frequency from the digital integral path,

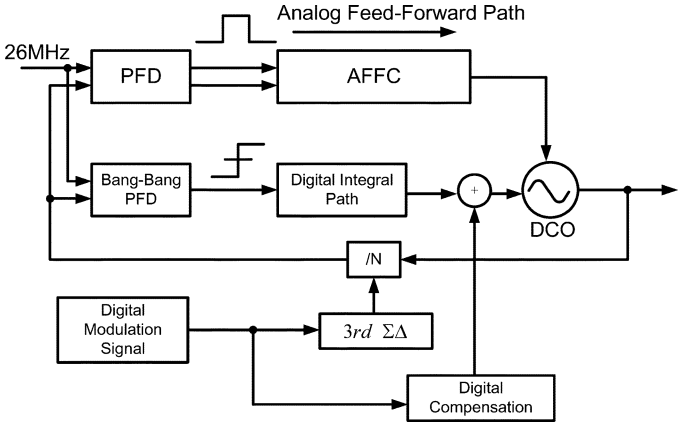


Fig. 13. The block diagram of the direct digital frequency modulator.

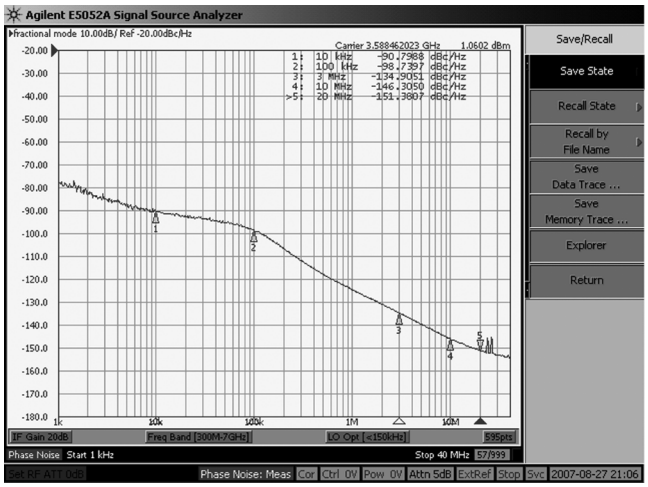


Fig. 14. The measured phase noise.

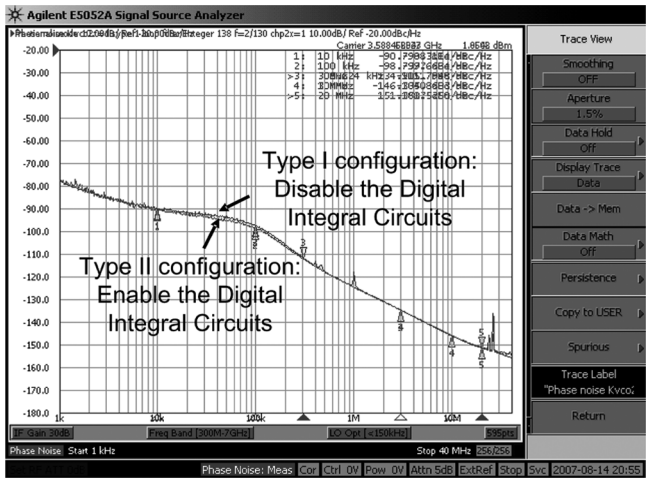


Fig. 15. Comparison of measured phase noise between type I and our proposed design.

$\alpha * (\Delta f/\Delta C)$, where α is the control code of the desired frequency and *DCO gain* $(\Delta f/\Delta C)$ is the frequency of the DCO unit control code. If *DCO gain* is known, the modulation code for the DCO can be easily computed digitally. However, the modulation frequency usually spans over several integer codes and each code may have different DCO gain due to minimum device size MOSFETs used in the tracking bit, which will be more prone to process variations. Additionally, *DCO gain* $(\Delta f/\Delta C)$ also varies with supply and temperature variations. Therefore, *DCO gain* $(\Delta f/\Delta C)$ should be calibrated both during startup and in real-time operation when channel switches. During startup, the relative frequency gain of each integer code should be calibrated. During channel switching, calibration should also be performed to observe absolute frequency gain due to temperature and supply variation. The relative frequency of the integer codes are obtained and normalized in a digital compensation circuit to obtain α which would eventually be used to directly modulate the DCO. A low error rate DFM PLL is thus possible through the combination of digital calibration and compensation.

VI. Measurement Results

Fig. 14 shows measured phase noise at 3.6 GHz using a 26 MHz reference clock when the fractional spurs are programmed to occur at harmonics of 400 kHz, which is the worst case for GSM. No spur is observed and therefore the fractional spur is at least below the measured phase noise level of -75 dBc.

Fig. 15 shows the measured phase noise has low jitter peaking as a type-I PLL. The curve labeled "type I loop filter" is obtained by disabling the digital integral path. No phase noise difference was observed when the digital integration path is enabled or disabled. This shows the integral path contribute negligible jitter peaking due to heavily damped loop, which is usually achievable using large capacitors if implemented purely through analog approach. Moreover, the two curves overlap, which indicates the digital integral path does not contribute dithering jitter. These observation validates the analysis in Section III.

The overlapped curves clearly show the type I loop PLL response, as predicted in Section III. The static phase error is zero because the measured output of the bang-bang PFD shows equal possibility for phase lead/lag. Low jitter peaking and zero static phase error make the presented architecture a suitable candidate for not only wireless communications, but also wired line applications such as SONET [18].

Fig. 16 is the comparison of measured phase noise between the proposed design and the TDC based ADPLL [4], which the TDC resolution is 25 ps. The in-band noise of our design is 10 dB lower than that of the TDC based ADPLL [4]. It gives the evidence that the digital integral path in our design contributes much less quantization error.

The measured output frequency as a plot of time during the calibration of a 30 kHz/bit integer code is shown in Fig. 17. The adaptive gain block decreases the gain by half when every 64 phase lead and lag transitions is counted. The calibration converges within 35 μs after the calibration starts. Note that the output frequency may still toggles around the optimum value since the bang-bang PFD will always indicate either a phase lead or lag after calibration completes. Thus, the last 16 samples at 50 μs are averaged to obtain the optimum frequency offset for a given injected code. The calibration error is within 3 Hz, or 100 ppm for a 30 kHz/bit integer code. This calibration proce-

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

		This Work	JSSC 06' pp. 1160 [19]	ISSCC 08' pp. 340 [5]
Process		0.13um CMOS	90nm CMOS	0.13um CMOS
Area (mm^2)		0.85	~0.85	0.95
Voltage (V)		1.5	1.4	1.5
Current (mA)	DCO core	20	18	**NA**
	Whole PLL	40	**NA**	26
Frequency (GHz)		3.2 - 4	3.2 - 4	3.6
Phase Noise (dBc/Hz) (referred to GSM band)	At 400kHz offset	-127.6	-123.5	-120.9
	At 3MHz offset	-148	-149	-144.9
	At 20MHz offset	163.3	-167	-162.2
Reference Freq	MHz	26	26	40
Reference Spur	dBc	-86	**NA**	-65
Frac Spur (worst case)	dBc	<-75	**NA**	<-64

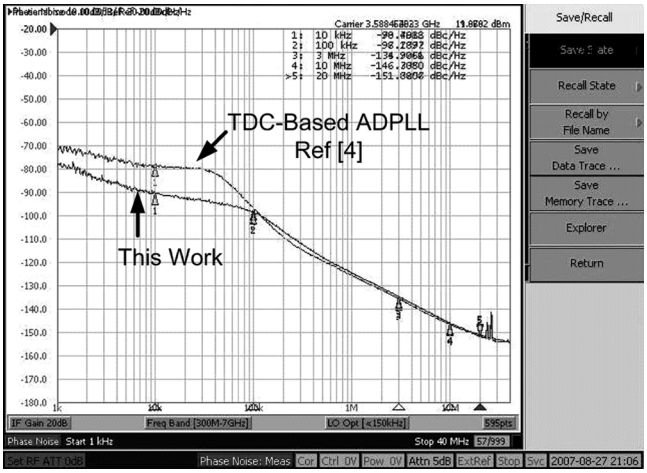


Fig. 16. Comparison of measured phase noise between the proposed design and TDC based ADPLL.

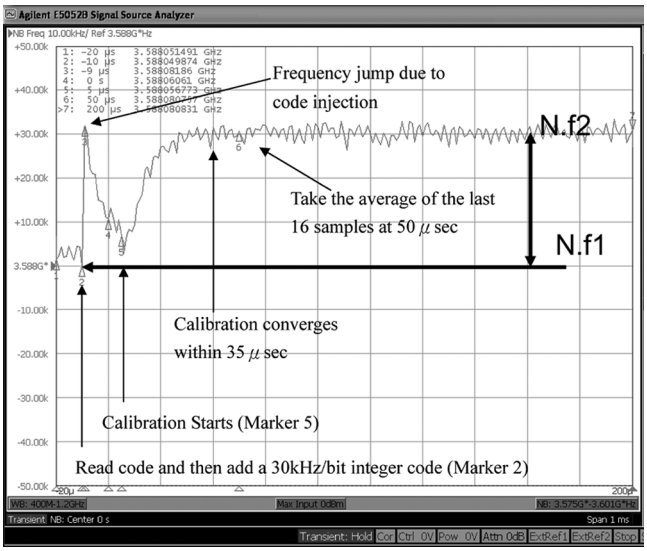


Fig. 17. Measurement result of calibrating for one integer code (30 kHz/bit) of the digital integral path.

dure is applied to every integer code during the system startup to obtain the relative frequency offset of each integer code.

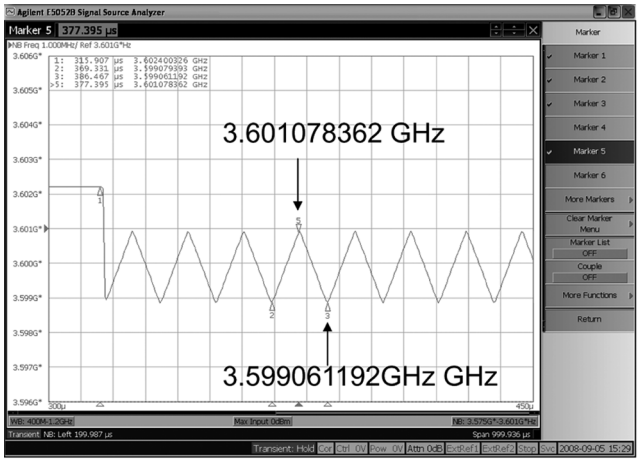


Fig. 18. Measurement result of modulation with a 60 kHz sawtooth with a signal range of 2 MHz.

Fig. 18 is the modulated output when a 60 kHz saw-wave with 2 M frequency range was sent to the presented PLL which has 40 kHz PLL loop bandwidth. The output frequency still resembles the input modulation data profile, which demonstrates our design approach breaks the tradeoff between modulation rate and PLL loop bandwidth. The measured maximum output frequency is 2.017 MHz, which has 1% compared to the 2 MHz modulation input data.

The die photo is shown in Fig. 19. This chip is implemented in 0.13 μm CMOS process. It occupies an active area of 850 μm $\times$ 1000 μm excluding regulator, and draws 40 mA from the regulated supply of 1.5 V. Key performance parameters are summarized in Table I.

VII. CONCLUSION

Digital intensive RF design could relax RF circuit requirements because the possibility of digitally repairing RF impairments; and designs could migrate to different technology node or foundry relatively more effortlessly. The key for such designs is the ability to measure RF impairments and stores the results digitally. In this paper, a digital intensive PLL whose loop parameters can be accurately measured and represented digitally

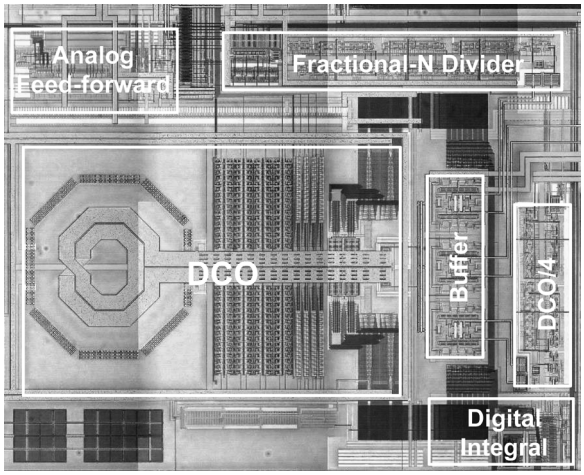


Fig. 19. Die micrograph of the chip in 0.13 μm CMOS (active area: 0.85 mm^2).

is presented. The architecture features separated integral path and proportional path, and a transfer curve folded DCO. The integral path is all digital and shares the benefits of ADPLLs. The transfer curve folded DCO provides all-digital control interface, which allows the PLL to be directly modulated by high data rate baseband signals. Pre-compensation of the baseband signal is possible for the proposed architecture. Synthesizer mode and modulator mode are both demonstrated in a 0.13 μm test chip. The chip occupies 0.85 mm^2 and draws 40 mA from a 1.5 V supply, including all auxiliary circuitry such as regulators and 3-wire control logics.

ACKNOWLEDGMENT

The author would like to thank all MediaTek RF division colleagues for the support and useful discussions, especially Mr. Lin-We Ke and Mr. Rickey Yu.

REFERENCES

[1] M. H. Perrott, T. L. Tewksbury, and C. G. Sodini, "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2048–2060, Dec. 1997.

[2] B. Neurauter, G. Marzinger, A. Schwarz, and R. Vuketich, "GSM 900/DCS 1800 fractional-N modulator with two-point-modulation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2002, vol. 1, pp. 425–428.

[3] R. B. Staszewski *et al.*, "All-digital PLL and GSM/EDGE transmitter in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 316–317.

[4] H.-H. Chang, P.-Y. Wang, J.-H. Zhan, and B.-Y. Hesieh, "A fractional spur free all-digital PLL with loop gain calibration and phase noise cancellation for GSM/GPRS/EDGE," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 200–201.

[5] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6 GHz digital sigma-delta fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 340–341.

[6] C.-W. Wu, E. Temporiti, D. Baldi, and F. Svelto, "A 3 GHz fractional-N all-digital PLL with precise time-to-digital converter calibration and mismatch correction," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 344–345.

[7] J. Zhuang, Q. Du, and T. Kwasniewski, "A 4 GHz low complexity ADPLL-based frequency synthesizer in 90 nm CMOS," in *Proc. IEEE CICC*, Feb. 2007, pp. 543–546.

[8] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N synthesizer," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[9] P.-Y. Wang, J.-H. C. Zhan, and H.-H. Chang, "An analog enhanced all digital RF fractional-N PLL with self-calibrated capability," in *Proc. IEEE CICC*, Sep. 2008, pp. 749–752.

[10] P.-Y. Wang, H.-H. Chang, and J.-H. C. Zhan, "A fractional spur reduction technique for RF TDC-based all digital PLLs," in *Proc. ESSCIRC*, Sep. 2008, pp. 422–425.

[11] P.-Y. Wang, S.-P. Chen, and P. Chen, "Timing orthogonal capacitance multiplication technique for PLL," in *VLSI Circuits Symp. Dig.*, Jun. 2007, pp. 162–163.

[12] V. Kratyuk, P. K. Hanumolu, K. Mayaram, and U. Moon, "A 0.6 GHz to 2 GHz digital PLL with wide tracking range," in *Proc. IEEE CICC*, Sep. 2008, pp. 305–308.

[13] K.-H. Chao, P.-Y. Wang, and T.-H. Hsu, "0.0234 mm^2/1 mW DCO based clock/data recovery for Gbit/s applications," in *VLSI Circuits Symp. Dig.*, Jun. 2007, pp. 132–133.

[14] J. Encinas, *Phase Locked Loops*. New York: Springer, 1993, p. 83.

[15] J.-H. C. Zhan, H.-H. Chang, and P.-Y. Wang, "A transfer-curve-folded DCO in 0.13 μm CMOS," in *IEEE RFIC Dig.*, Jun. 2008, pp. 391–394.

[16] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice Hall, pp. 257–268.

[17] P.-Y. Wang and H.-M. Chang, "A charge pump based direct frequency modulator," in *Proc. IEEE ISCAS*, May 2008, pp. 1962–1965.

[18] M.-H. Perrott *et al.*, "A 2.5 Gb/s mulit-rate 0.25 μm CMOS CDR utilizing a hybrid analog/digital loop filter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 328–329.

[19] C.-M. Hung, R. B. Staszewski, N. Barton, M.-C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.

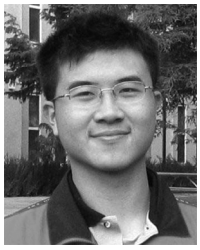
Ping-Ying Wang was born in Keelung, Taiwan, in 1969. He received the M.S. degree in physics science from National Taiwan University, Taipei, Taiwan, in 1994. His M. S. thesis focused on finite-size effect of Landau diamagnetism.

From 1996 to 1999, he was a process technology development engineer with Macronix Semiconductor Inc., where he invented the double exposure method for 0.18 and 0.13 μm lithograph in Mask ROM production line. He joined Etron and Realtek semiconductor, Hsinchu, Taiwan, in 1999 and 2001, respectively, where he developed all-digital line lock loop for LCD controller and digital spread-spectrum clock for chipsets of personal computers. In 2003, he joined Mediatek, Hsinchu, Taiwan, where he developed all-digital clock data recovery for Blu-ray and optical storages, design automation for PLL, digital controlled oscillator based CDR for high speed serial link, and capacitance multiplication technique for analog PLLs. Currently, he is the Senior Manager of the RF division, focusing on digitized RF transmitter for cellular phone.

Jing-Hong Conan Zhan received the B.S. and M.S. degrees in electrical engineering from Tsing-Hua University, Hsinchu, Taiwan, in 1996 and 1997, respectively. His M.S. thesis focused on side-polished fiber fabrication and theoretical analysis. After completing compulsory services in the Taiwanese Army as a second lieutenant from 1997 to 1999, he joined MediaTek, Hsinchu, Taiwan, as a logic design engineer until 2001. He developed the data path and spindle motor control circuitry for MediaTek's optical storage products. He then pursued the Ph.D. degree in electrical engineering and computer science at Cornell University, Ithaca, NY, focusing on VCO and high-speed clock and data recovery circuit design using BiCMOS and CMOS. He received the Ph.D. degree in 2004 and joined Intel Communication Circuit Lab in Hillsboro, OR, as a RF circuit designer. His research focused on fabricating low-cost radios on CMOS technologies for microprocessors production. In 2006, he joined MediaTek RF division where he worked on tuner front-end design. He co-developed an all-digital PLL for wireless applications. His recent interest is on millimeter wave circuit design.

Hsiang-Hui Chang (S'01) was born in Taipei, Taiwan, on February 4, 1975. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, in 1999, 2001, and 2004, respectively.

He is currently with Mediatek Inc., Hsinchu, Taiwan, working on wireless communication products. His research interests are digital-enhanced PLLs, RF system architecture design, DLLs, and high-speed interfaces for gigabit transceivers.



Hsiu-Ming Sherman Chang received the B.Eng. degree in electrical and electronics engineering (industrial education) from National Taiwan Normal University in 2002. He received the M.S. degree in electrical engineering from Stanford University in 2006. He joined the SoC Design and Test Lab at the University of California, Santa Barbara, in 2006 where he is currently pursuing the Ph.D. degree in electrical and computer engineering under the supervision of Prof. Kwang-Ting (Tim) Cheng. He interned in the RF Division at MediaTek, Inc. during summers 2007 and 2008. His current research interests include design and test of mixed-signal and radio-frequency circuitry.