An Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC With Code-Counter-Based Offset Calibration

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***Abstract*— This article presents an inherent gain error-tolerant noise-shaping (NS) successive approximation register (SAR)-assisted pipelined analog-to-digital converter (ADC). The architecture is hybrid with a pure passive-feedforward (FF) NS SAR ADC in the first stage of the pipeline, realizing an N-0 (2-0) multistage NS sigma–delta (MASH). The Nth order from the first stage shapes not only the quantization error and comparator noise but also the interstage gain and nonlinearity error, which greatly relaxes the gain accuracy constraint in the conventional pipelined architecture. In addition to gain, a code-counter-based (CCB) background offset calibration is introduced to mitigate the interstage offset with low cost. The prototype further adopts partial interleaving in the first stage for high speed while sharing the integration capacitors in the feed-forward (FF) structure for a compact area. The 2-0 MASH runs at 400 MS/s and achieves 25-MHz bandwidth with 8 × OSR, consuming 1.26-mW power from a 1-V supply. Within a gain error range of −16% to +12%, the SNDR of the ADC deviates less than 3 dB from the nominal 75-dB SNDR. Fabricated in a 28-nm CMOS process, it exhibits a 178-dB Schreier figure of merit (FoM_S).**

***Index Terms*— Amplifier linearity enhancement, analog-to-digital converter (ADC), background offset calibration, DWA, digital reconstruction filter, energy and area efficient, inherent gain error tolerant, inter-stage gain error, noise shaping (NS), oversampling, partial interleaving, pipelined successive approximation (SAR), quantization leakage error.**

I. Introduction

With a continuous trend of deep-submicrometer technology scaling, successive approximation register analog-to-digital converters (SAR ADCs) [1], [2] and noise-shaping (NS) SAR ADCs [3]–[6] became more attractive for a high-resolution and energy efficiency scenario [7]. However, their inartificial serial conversion scheme and comparator noise introduce a major bottleneck on their speed and resolution, respectively. By breaking the conversion in two steps with a pipeline scheme [8], [9], it can enhance the speed and relax the comparator noise either through the inter-stage redundancy or gain. While further adopting the NS technique [10], [11], the critical comparator noise can be further suppressed. Although the residue amplifier (RA) in these architectures enables pipeline and/or NS, its gain accuracy and linearity are crucial and often need conscious design.

To ensure a stable gain over process–voltage–temperature (PVT) variations, the classic solution adopts a closed-loop structure with a high-gain amplifier. However, it is not friendly to the technology scaling due to the shrunken intrinsic gain of the device. The multistage amplifier, correlated double sampling (CDS) [12], [13], and correlated level shifting (CLS) [14] can enhance the gain, but at the cost of either poor stability or extra operation phase and hardware overhead. More recent solutions are the digital amplifier [15] and the closed-loop dynamic amplifier [16], but the former technique calls for a low noise comparator. The latter has a limited speed for stability consideration. Besides, digital calibration [11], [17]–[19] can also tackle such gain error. Nevertheless, they inevitably induce substantial hardware costs and potential convergence issues.

Rather than the circuit or calibration approach, the inter-stage gain error can be suppressed by the gain error shaping (GES) [20]. Similar to the NS concept, the second-stage residue is fed back to the first and second stages with opposite polarity. In this way, the gain error is high-pass shaped. Furthermore, the digital error feedback (DEF) [21] can also shape the truncation error due to the only partial residue feedback from the second stage, achieving an outstanding GES ability. However, such a technique not only increases the in-band quantization but also worsens the linearity of the amplifier with a positive gain error, which eventually harms the overall ADC performance. Last but not least, its hardware cost is considerable, which complicates the design.

In this work, a multistage noise-shaping (MASH) N-0 structure realized by an NS SAR-assisted pipeline architecture is introduced [22], which has an inherent gain error

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tolerance ability. An Nth order NS SAR ADC in the first stage shapes the quantization error and comparator noise in all stages, together with the inter-stage gain error, gain nonlinearity, and partial noise from the RA, thus relaxing the comparator and RA design. The error and noise suppression abilities rise with NS order and this architecture provides a solution to tackle all the abovementioned nonidealities as a bundle rather than separated solutions in the conventional pipeline-SAR ADCs. The first-stage NS-SAR, designed with a second-order fully passive feedforward (FF) structure, ensures a sufficient gain error suppression and robust noise transfer function (NTF). With an accurate passive integration, the proposed MASH 2-0 sigma–delta modulator (SDM) avoids any NTF calibration or tuning. A 6-b coarse NS-SAR ADC and partial interleaving is adopted to speed up the first-stage conversion. The 4-b DWA addresses the DAC mismatch during the idle time when performing the decision transfer from the coarse ADC to the fine DAC. A gain-boosted dynamic amplifier is adopted as the RA and a CCB background offset calibration method is introduced to remove the inter-stage offset error. Fabricated in a 28-nm CMOS process, the ADC prototype runs at 400 MHz with 25-MHz bandwidth (BW) and 75-dB SNDR, consuming a total of 1.26-mW power from a 1-V supply. It delivers a 178-dB Schreier figure of merit (FoM) and demonstrates a -16% to $+12\%$ 3-dB-SNDR gain error tolerance ability at OSR $= 8$.

This article provides the details of the analysis and implementation of the proposed inter-stage GES SAR-assisted pipeline structure. This article is organized as follows. Section II presents the analysis of the proposed MASH N-0 structure. The overall MASH 2-0 architecture is discussed in Section III. Section IV explains and analyzes the CCB background offset calibration method and circuit implementation details. Section V exhibits the measurement results of the ADC followed by the conclusions drawn in Section VI.

II. NS, SAR, and Pipeline Hybrid MASH

Combining the merits of the SAR and $\Delta\Sigma$ ADC, the NS-SAR ADC can achieve high resolution with low power by effectively suppressing the comparator noise. Passive [23] or active [24] integrator can be adopted to realize the NS, while the former solution suffers from a mild NTF. The latter NTF is sensitive to the gain of the additional amplifier. While further incorporating with the pipeline in [10] and [11], the reutilization of the amplifier can lead to a sharp NTF with the full resolution residue of the ADC fed back to the second stage only, which enables a high-speed operation. Since the NS happens in the second stage, such MASH 0-N architecture calls for an accurate inter-stage gain as in conventional two-step ADCs to avoid noise leakage. In this design, we move the NS to the first stage (MASH N-0) for better inter-stage gain error immunity than its MASH 0-N counterparts.

A. MASH 0-N SAR-Assisted NS Pipelined ADC

Fig. 1(a) shows the architecture block diagram of the MASH 0-N SAR-assisted NS pipelined ADC. It consists of a pure

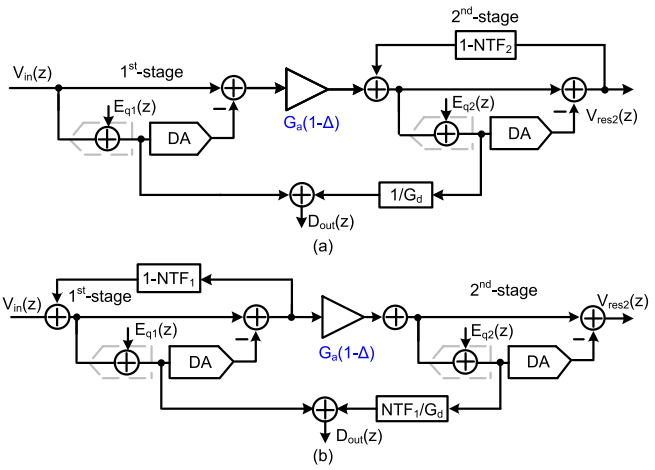


Fig. 1. (a) MASH 0-N SAR-assisted pipelined ADC. (b) MASH N-0 SAR-assisted pipelined ADC.

SAR ADC in the first stage and an NS-SAR ADC in the second stage. The NS-SAR can be realized based on the error feedback (EF) [24] or FF [23] structure, while here, we particularly show and analyze the EF structure for simplicity. The overall transfer function of the ADC can be expressed as

$$D_{\text{out}}(\text{z}) = V_{\text{in}}(\text{z}) + \frac{1}{G_{\text{d}}}(G_{\text{d}} - G_{\text{a}}(1-\Delta))E_{\text{q1}}(\text{z}) + \frac{\text{NTF(z)}}{G_{\text{d}}}E_{\text{q2}}(\text{z}) \quad (1)$$

where $E_{\text{q1}}(\text{z})$ and $E_{\text{q2}}(\text{z})$ are the quantization noise from the first and second stages, respectively, $V_{\text{in}}(\text{z})$ and $D_{\text{out}}(\text{z})$ are the input signal and output of the ADC, respectively, G_{d} is the digital gain in the noise cancellation filter, and $G_{\text{a}}(1-\Delta)$ is the gain of the amplifier with Δ its gain error. NTF(z) is the noise transfer function of the ADC. Due to the pipeline architecture, $E_{\text{q1}}(\text{z})$ is completely canceled (if $\Delta = 0$) and $E_{\text{q2}}(\text{z})$ is attenuated by the inter-stage gain G_{a}. The NTF further shapes $E_{\text{q2}}(\text{z})$ from the EF structure, thus greatly relaxing the accuracy requirement of the second stage. However, it can be observed from (1) that the NTF does not affect the inter-stage error since it only happens in the second stage after the amplification, implying that this MASH 0-N architecture has a similar level of sensitivity and no improvement when compared with the conventional SAR-assisted pipelined architecture [10]. Such error, also known as the noise leakage in the MASH SDM, can be significant and hinders the benefits originated from the NS-SAR.

B. Proposed MASH N-0 NS-SAR-Assisted Pipelined ADC

Fig. 1(b) shows the concept of the proposed MASH N-0 NS-SAR-assisted pipeline architecture with the NS-SAR placed in the first stage. The output can be derived as

$$D_{\text{out}}(\text{z}) = V_{\text{in}}(\text{z}) + \frac{\text{NTF(z)}}{G_{\text{d}}}(G_{\text{d}} - G_{\text{a}}(1-\Delta))E_{\text{q1}}(\text{z}) + \frac{\text{NTF(z)}}{G_{\text{d}}}E_{\text{q2}}(\text{z}). \quad (2)$$

Similar to the previously introduced MASH 0-N SDM, $E_{\text{q2}}(\text{z})$ can be shaped by the NTF and further suppressed by

the gain. However, differently, $E_{q1}(z)$ now also experiences the NTF through the NS in the first stage. While without gain error ($\Delta = 0$), such a feature is not important because $E_{q1}(z)$ is completely canceled anyway. On the other hand, such shaped $E_{q1}(z)$ enables a better inter-stage gain error immunity, which equivalently imposes a smaller noise leakage in the MASH architecture. Even though the comparator noise of the first stage is canceled, the proposed MASH N-0 structure maintains the merit of NS-SAR ADC, which can shape the quantization noise and comparator noise of the second stage.

The GES method [21] mitigates the gain error by feeding back the output codes of the second stage through a digital GES transfer function (H_{GES}) to the first stage. The second-to-first stage's feedback has opposite polarity and ideal gain ratio, adopting the capacitive DAC as a reference to effectively shape the gain error into high frequency. However, the left-hand pole of the transfer function for the quantization leakage, the second-stage quantization, and truncation errors move to the right when there is a positive gain error, forming positive feedback and thus leading to an undesirable large swing at the first-stage GES residue, while in the proposed architecture, the shaped $E_{q1}(z)$ enables a good noise leakage immunity, and therefore, the gain error can be shaped by the NTF without the swing issue.

C. Inter-Stage Gain and Nonlinearity Error Shaping

Based on (2) for the proposed MASH N-0 architecture, it can be noted that the inter-stage gain error can be shaped by the NTF. Indeed, not only the first-order error but also the high-order nonlinearity error of the amplifier can be suppressed. To illustrate this capability, this section compares the proposed structure with the MASH 0-N based on the behavioral simulation results. Figs. 2 and 3 show the performance comparisons of the mentioned two structures with sole gain error and sole nonlinearity error, which is expressed as total harmonic distortion (THD) of the amplifier in dBc. Considering the gain and nonlinearity error of the amplifier, the output voltage of the amplifier V_{AMPOUT} is modeled as

$$V_{AMPOUT} = -E_{q1}(z)G_a(1-\Delta) - \alpha_i G_a\left(-E_{q1}(z)\right)^i (i \geq 2) \quad (3)$$

where G_a is the ideal gain of the amplifier, Δ is the gain error, and α_i is the coefficient of the ith order nonlinearity of the amplifier. For simplicity, we only include the third-order nonlinearity. It can be seen from (3) that high-order nonlinearities undergo the digital reconstruction filter with NTF, which is similar to the gain error Δ. The two architectures have the same number of resolutions in the first and second stages, as well as an identical NTF but realized in different stages. The number of bit resolutions is 6 in both stages and one-bit redundancy is adopted, and the NTF is $(1 - 0.5z^{-1})^N$ in the behavioral model, aligned with the implementation of this design.

There is a degradation of the SQNR in both architectures in the presence of the inter-stage gain and nonlinearity error, but the performance of the MASH 0-N drops steeper than its MASH N-0 counterpart with the same amount of gain or nonlinearity error. In the MASH 0-N architecture with moderate

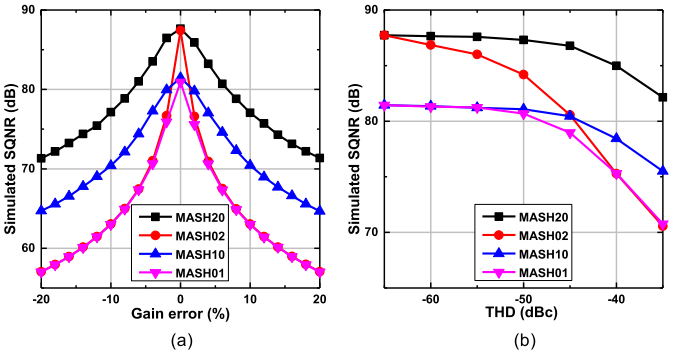


Fig. 2. Comparison between the MASH 0-N and the MASH N-0. (a) Simulated SQNR varies with gain error. (b) Simulated SQNR varies with THD of the amplifier.

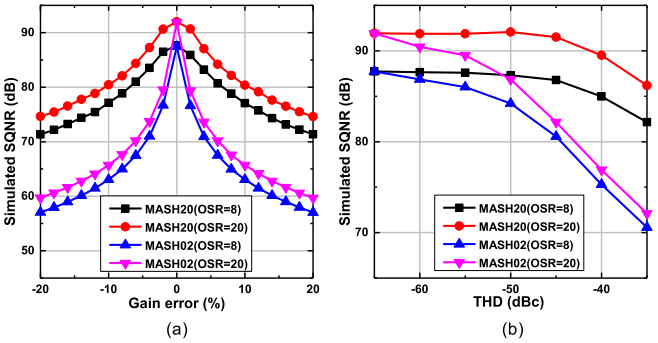


Fig. 3. Comparison between the MASH 0-N and the MASH N-0 with different OSRs. (a) Simulated SQNR varies with gain error. (b) Simulated SQNR varies with THD of the amplifier.

gain error, the SQNR is limited by the noise leakage instead of $E_{q2}(z)$, and therefore, increasing the order in the second stage [Fig. 2(a)] does not imply any benefit. These results also match the previous analysis and the derived transfer function (1). A similar phenomenon can be observed in Fig. 2(b) for the nonlinearity error. With the MASH N-0 structure, the achieved SQNR is significantly better than MASH 0-N under the same amount of gain error and THD, demonstrating a better immunity. Besides, by increasing the NS order in the first stage, such immunity can be further improved, enabling a better performance target. With larger OSR, the achieved SQNR of the MASH N-0 can improve even more without affecting the gain and nonlinearity error shaping ability. For example, the achieved SQNR is 92 dB when OSR = 20, which is 5 dB better than OSR = 8 with $N = 2$, while the SQNR of the MASH 0-N still experiences a small improvement, because certain significant harmonics caused by the gain and nonlinearity error become out-band with larger OSR. The expected THD of the designed amplifier is at worst -45 dBc based on simulation results, which leads to an SQNR drop of 1 and 7.2 dB in the MASH 2-0 and the MASH 0-2 structure, respectively, with OSR = 8. The proposed architecture retains $\sim$14 dB better SQNR with $\pm$20% gain error comparing with the MASH 0-2 counterpart.

It should be noted that the same gain error sensitivity can be achieved by increasing the number of bits resolution in the first stage. However, this increases the burden of the first-stage ADC design and associated calibration as well as limits the

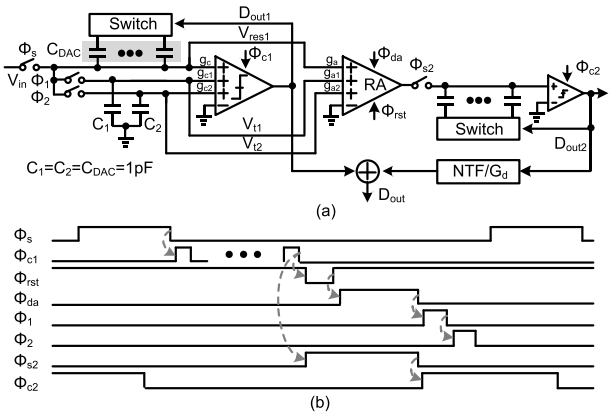


Fig. 4. Proposed CIFF MASH 2-0 SAR-assisted pipeline. (a) Simplified schematic. (b) Timing diagram.

ADC implementation choice. For example, an extra 2-bit resolution is necessary to reach a similar gain sensitivity as the proposed design, which consumes considerably larger power as it becomes noise-limited. Besides, the error correction range drops, thus calling for a greater calibration effort and a lower error first-stage ADC. Finally, with more bits in the first stage, the inter-stage gain has to be increased to maintain the size of the second-stage DAC. Otherwise, more attenuation capacitance is necessary, thus increasing the total capacitance of the second-stage DAC. The proposed architecture can improve the gain error tolerance ability by increasing the LF's order instead of the quantization bits, which provides another option to resolve the inter-stage gain and nonlinearity error.

III. Overall MASH 2-0 Architecture

To realize the NS in the first stage, both EF and CIFF can be considered. The EF structure often calls for an amplifier with accurate gain to construct the sharp NTF [24], leading to extra noise and requiring calibration. In the proposed work, a fully passive CIFF NS structure is used in the first stage to implement a stable NTF.

A. Proposed MASH 2-0 NS-SAR-Assisted Pipelined ADC

The proposed MASH 2-0 NS-SAR-assisted pipelined ADC with simplified schematic and timing diagram is shown in Fig. 4. The second-order NS-SAR ADC in the first stage is realized based on a passive CIFF filter [23], while the second stage is a pure SAR ADC. The NTF in (2) of the first stage is $(1 - 0.5z^{-1})^2$ as two integration capacitors, C_1 and C_2, are equal to the main DAC capacitor. Its operation procedure can be described as follows. Initially, the DAC capacitor samples the input voltage (V_{in}) during Φ_{S}. Then, the NS-SAR ADC of the first stage converts 6 b with the three-input comparator where the ratio of the input pairs (g_{c}, g_{c1}, and g_{c2}) is 1:1:2. After the sampling and conversion phases, the first-stage residue (V_{res1}) and the voltage on two integration capacitors (V_{int1} and V_{int2}) are summed, subsequently amplified by a three-input dynamic amplifier where the ratio among the input pairs is the same as the three-input comparator. Eventually, considering the FF path summation, the amplifier and the comparator (equivalently at their inputs) undertake

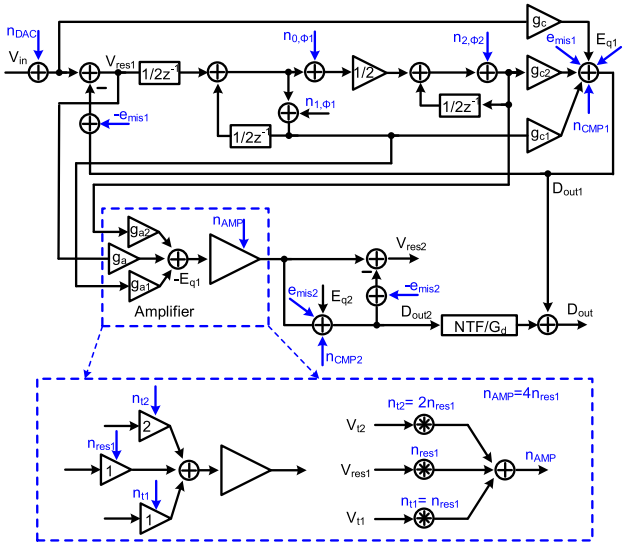


Fig. 5. Noise and mismatch analysis of the MASH 2-0 structure.

$-E_{\text{q1}}$ during the amplification phase Φ_{da}. With $-E_{\text{q1}}$ handed over to the second stage, it maintains the NS ability for the quantization error and comparator noise. After the amplification, V_{res1} on C_{DAC1} is charge-shared with two integration capacitors (C_1 and C_2) sequentially during Φ_1 and Φ_2, leading to a second-order passive integration. Simultaneously, the second-stage SAR ADC attains the remaining 6-b resolution. After all, the output of the second stage (D_{out2}) passes through the digital reconstruction filter (NTF/G_{d}) and then sums with the first-stage output (D_{out1}), thus removing the quantization noise in the first stage at the final output (D_{out}).

B. Source of Nonidealities

Fig. 5 shows the major sources of nonideality in the proposed MASH 2-0 SAR-assisted pipeline ADC. n_{DAC} is mainly from the kT/C noise, while $n_{0,\Phi1}$, $n_{1,\Phi1}$, and $n_{2,\Phi2}$ are the noises from the two passive integration phases Φ_1 and Φ_2[23]. $n_{\text{AMP}}$is the total input-referred noise of the amplifier. E_{q1}, e_{mis1}, and n_{CMP1} are the quantization noise, mismatch error in the capacitance DAC array, and comparator noise of the first stage, respectively, while E_{q2}, e_{mis2}, and n_{CMP2} are the corresponding impairments of the second stage (same as above). The overall transfer function, including these nonidealities, is

$$\begin{aligned} D_{\text{out}} = {} & V_{\text{in}} + e_{\text{mis1}} + n_{\text{DAC}} + n_{0,\phi1}\left(1 - 1/2z^{-1}\right) + n_{1,\phi1} \\ & + 2n_{2,\phi2}\left(1 - 1/2z^{-1}\right) + \text{NTF} \cdot n_{\text{CMP1}} + \text{NTF} \\ & \cdot n_{\text{AMP}} + \frac{\text{NTF}}{G}\left(E_{\text{q2}} + e_{\text{mis2}} + n_{\text{CMP2}}\right). \end{aligned} \tag{4}$$

Then, e_{mis1}, n_{DAC}, and $n_{1,\Phi1}$ cannot be shaped, while $n_{0,\Phi1}$ and $n_{2,\Phi2}$ are first-order shaped. With sufficiently large sampling and integration capacitors, n_{DAC}, $n_{0,\Phi1}$, $n_{1,\Phi1}$, and $n_{2,\Phi2}$ can be well suppressed, and e_{mis1} is addressed by the 4-b DWA in this design (detailed later). Both n_{CMP1} and E_{q1} are shaped by the NTF, while n_{CMP1} can be further covered by the redundancy between stages and E_{q1} is canceled by the reconstruction filter (without gain error). E_{q2}, e_{mis2}, and n_{CMP2}

are shaped by the NTF and also suppressed by the inter-stage gain G.

Since the amplification indeed is split into three paths, their noises are listed individually. n_{AMP} can be divided into three-input-referred noises n_{res1}, n_{t1}, and n_{t2}, which connect to the signal path V_{res1}, V_{t1}, and V_{t2} (Fig. 4), respectively. n_{AMP} is the lump sum of all the above noises. It can be noticed from (4) that they are all second-order shaped by the NTF. Nevertheless, the multiple input pairs worsen the noise comparing with single pair at the same power budget [23]. The total noise is increased by 4× because of the two additional added paths. Fortunately, the noise is attenuated by ∼4× due to the NTF with OSR = 8. Its net in-band noise is almost the same as in the case of one-pair device. Eventually, an overall small n_{AMP} is ensured by budgeting a sufficiently long integration time in the proposed design.

C. MASH Noise Cancellation

The noise leakage issue in the MASH architecture due to the nonideal first-stage NTF is carefully studied. The NTF in this design is determined by the ratios of the capacitors (DAC array capacitor and two integration capacitors) and the ratio between input pairs of the comparator and amplifier. As the DAC and integration capacitors are implemented with the same type of capacitors (MoM), they are assumed to be well matched in the following analysis with $C_1 = C_2 = C_{\mathrm{DAC}}$. Besides, the noise leakage due to the inter-stage gain error is well analyzed in Section II, and therefore, we set $G_{\mathrm{d}} = G_{\mathrm{a}} = 1$ to simplify the analysis and focus on the discussion of the NTF mismatch. The noise transfer function of the first stage of the MASH SDM is detailed as

$$\mathrm{NTF}_1(\mathrm{z}) = \frac{\left(1-0.5\mathrm{z}^{-1}\right)^2}{1+(0.5g_{\mathrm{c1}}+0.25g_{\mathrm{c2}}-1)\mathrm{z}^{-1}+(0.25-0.25g_{\mathrm{c1}})\mathrm{z}^{-2}} \tag{5}$$

where g_{c1} and g_{c2} are the gain ratio of the input pairs of the comparator normalized to g_{c}. Besides, as the first-stage residue of this MASH SDM is constructed by a three-input amplifier, the output voltage of the amplifier $V_{\mathrm{amplifier}}$ is modeled as

$$V_{\mathrm{amplifier}} = -\mathrm{NTF}_1(\mathrm{z})E_{\mathrm{q1}}(\mathrm{z}) \times \frac{1+(0.5g_{\mathrm{a1}}+0.25g_{\mathrm{a2}}-1)\mathrm{z}^{-1}+(0.25-0.25g_{\mathrm{a1}})\mathrm{z}^{-2}}{(1-0.5\mathrm{z}^{-1})^2} \tag{6}$$

where g_{a1} and g_{a2} are the gain ratio of the input pairs of the amplifier normalized to g_{a}. In the ideal case, where $g_{\mathrm{c1}} = g_{\mathrm{a1}} = 1$ and $g_{\mathrm{c2}} = g_{\mathrm{a2}} = 2$, the transfer function of the digital reconstruction filter is

$$\mathrm{NTF}_{\mathrm{d}}(\mathrm{z}) = \left(1-0.5\mathrm{z}^{-1}\right)^2. \tag{7}$$

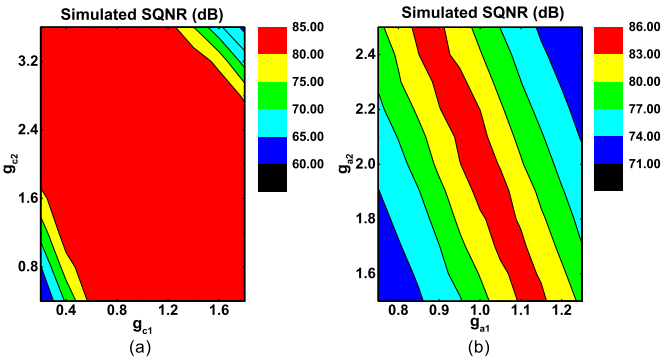


Fig. 6. Simulated SQNR varies with (a) extra comparator ratio and (b) extra amplifier ratio.

Then, the complete output of this MASH SDM will be (8), as shown at the bottom of the page.

It can be noticed that $E_{\mathrm{q1}}(\mathrm{z})$ is completely canceled in the ideal case. Under PVT and mismatch variations, the zeros of the NTF_1 are robust as they are set by the capacitor ratio, while the pole locations can drift due to the mismatch among g_{c1} and g_{c2}, but they are not crucial in the cancellation process. Besides, the cancellation procedure is affected by the mismatch between g_{a1} and g_{a2}. Fortunately, their variations can be relaxed by the robust NTF_1. It is worth noting that the ratio between g_{c1}, g_{c2}, g_{a1}, and g_{a2} is in the first-order set by the width of the same type of transistors, and therefore, they are relatively insensitive to PVT variations.

Only the absolute variation of the amplifier gain (Figs. 2 and 3) is a direct cause of the inter-stage gain error. The variations of g_{a1} and g_{a2} associated with g_{a} mainly affect the transmission of $-E_{\mathrm{q1}}(\mathrm{z})$ to the second stage and therefore potentially causes noise leakage. Since the ratio among g_{a}, g_{a1}, and g_{a2} are realized by the same type of transistor in different sizes, they experience similar variations over PVT. On the other hand, the relative value between g_{a}, g_{a1}, and g_{a2} can be affected by the mismatch, altering the NTF and affecting the gain error tolerance ability. To demonstrate the sensitivity, a behavioral simulation is performed based on the proposed ADC structure. The SQNR with g_{c1}, g_{c2}, g_{a1}, and g_{a2} variations is shown in Fig. 6. Furthermore, the proposed ADC is more sensitive to the input pair mismatch of the amplifier than the comparator as the perfect cancellation relies on g_{a1} and g_{a2}, which is consistent with (8). To have good matching, the inputs of the amplifier are sufficiently large with sizes 16 μm/0.05 μm, 16 μm/0.05 μm, and 32 μm/0.05 μm. Fig. 7 shows their variations with a 100-run Monte Carlo simulation, and such large size ensures small enough standard variations. The 3σ coefficient variations of g_{a1} and g_{a2} are ±8.4% and ±12%, leading to the worst SQNR of 77 dB.

$$D_{\mathrm{out}}(\mathrm{z}) = V_{\mathrm{in}}(\mathrm{z}) + \mathrm{NTF}_{\mathrm{d}}(\mathrm{z})E_{\mathrm{q2}}(\mathrm{z}) + E_{\mathrm{q1}}(\mathrm{z})\mathrm{NTF}_1(\mathrm{z}) \times \left(1 - \frac{1+(0.5g_{\mathrm{a1}}+0.25g_{\mathrm{a2}}-1)\mathrm{z}^{-1}+(0.25-0.25g_{\mathrm{a1}})\mathrm{z}^{-2}}{\left(1-0.5\mathrm{z}^{-1}\right)^2}\mathrm{NTF}_{\mathrm{d}}(\mathrm{z})\right). \tag{8}$$

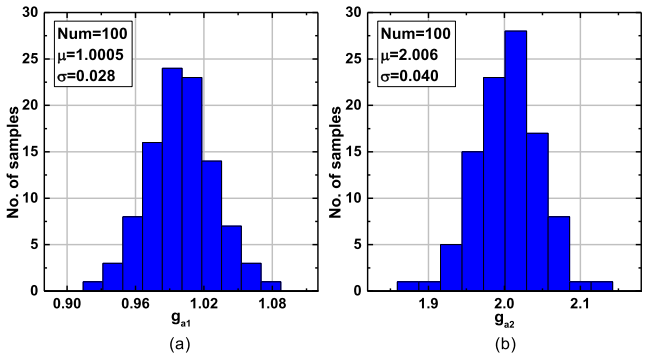


Fig. 7. Monte-Carlo simulation results of (a) g_{a1} and (b) g_{a2}.

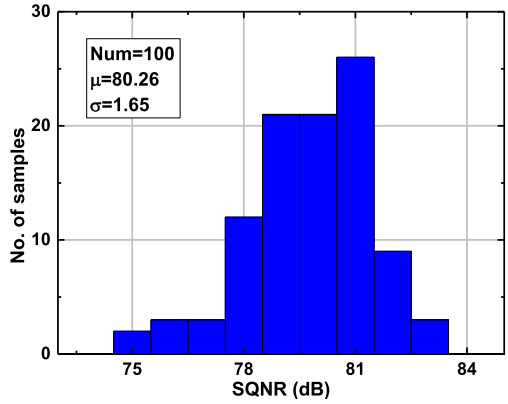


Fig. 8. Post-layout ADC simulation results with multiple-input first-stage comparator and amplifier mismatch.

Fig. 8 shows a 100-run post-layout Monte Carlo simulation, which illustrates the SQNR variations due to the mismatch of the input pairs of the comparator and the amplifier. The mean and standard deviation values of the SQNR are 80.26 dB and 1.25, respectively, leaving enough margin for an overall 75-dB SNDR target.

IV. CC-Based Offset Calibration and Circuit Implementation

A. CCB Inter-Stage Offset Calibration

A code-counter-based offset calibration is presented to address the inter-stage offset error, which relies on the characteristic of the symmetrical output code distribution from the second stage. With a 6-b quantization in the first stage, the code distribution of the second stage should be Gaussian and centered at mid code when there is no inter-stage offset error (Fig. 9) [25]. On the other hand, with a large positive or negative inter-stage offset, the symmetry of the code distribution varies and one of the intervals experiences significantly less code count. Even with a large inter-stage gain error, such characteristic still enables an inter-stage offset calibration based on the symmetry of the second-stage output code distribution. While monitoring the entire output interval can be costly, we only inspect the distribution on the boundary codes of the second stage. Fig. 10 shows the logic flowchart of the CCB offset calibration. It monitors the second-stage output to obtain a calibration decision, which controls the offset of the first-stage comparator through analog feedback. When D_{out2} are equal to all "1", it triggers an up-down counter to count

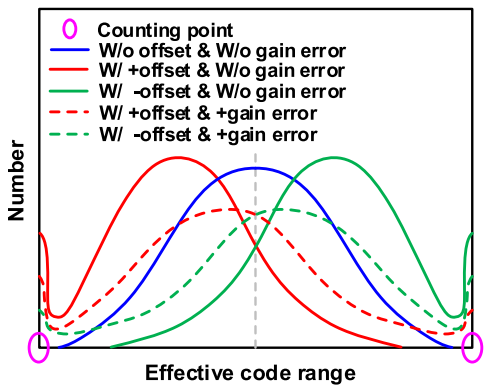


Fig. 9. Code distribution in the second stage varies with offset and positive gain error.

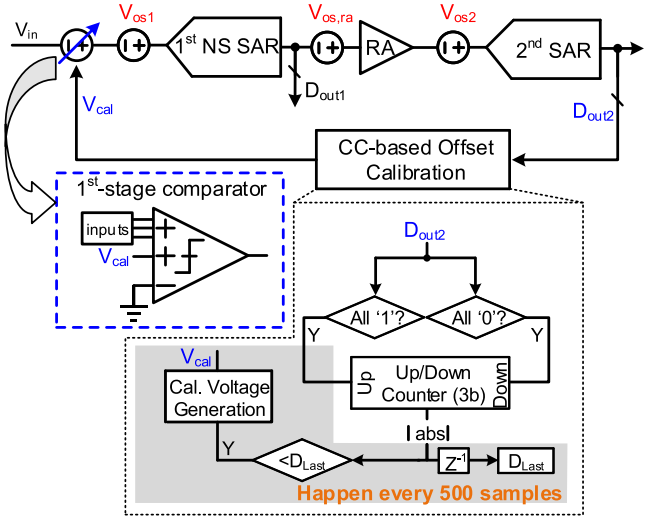


Fig. 10. Proposed CCB method.

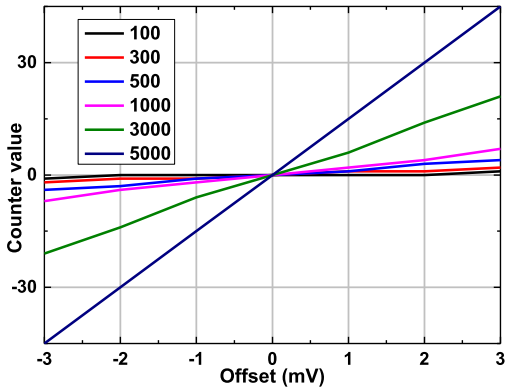


Fig. 11. Counter value varies with counter sample.

up and vice versa to count down when equals to all "0". After certain samples, the counter output should be close to zero if the offset is small, while if the counter has a positive count, it implies a negative offset among stages and vice versa for the positive offset with a negative count.

In this design, the most critical condition for offset detection is that only a small amount of code touches the boundary of the second stage. Fig. 11 shows the code count of different offsets with various samples and an 8.14 mV_{rms} input-referred

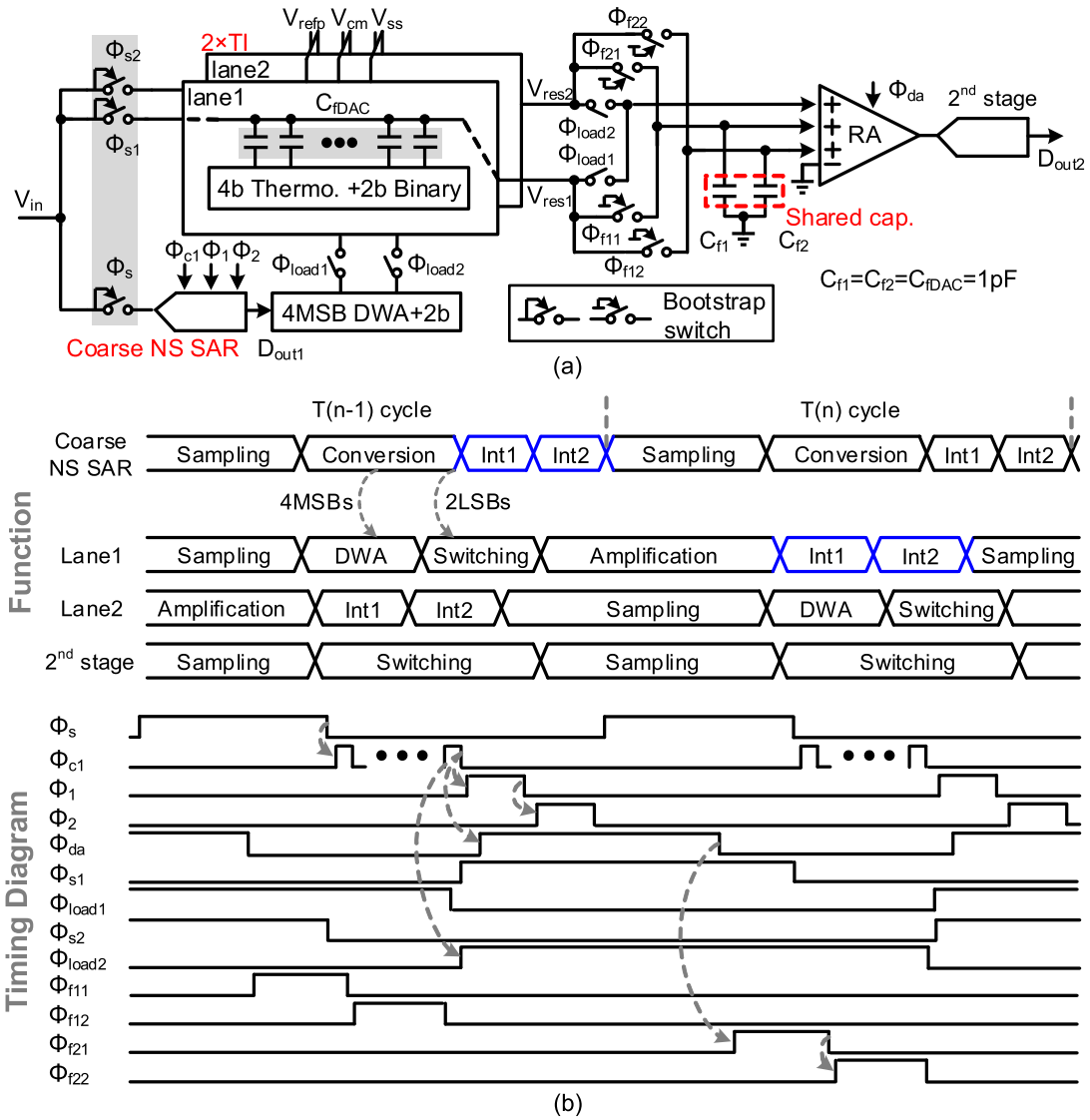


Fig. 12. Proposed MASH 2-0 ADC. (a) Overall schematic. (b) Operation procedure and timing diagram.

noise from the first-stage comparator. A 2-mV offset can be detected with 500 samples, which ensures a less than 1-dB variation on the overall SQNR due to the inter-stage offset. With an increased number of samples, the counter value can detect a smaller offset difference. However, it consumes considerable time and hardware. In order to balance the convergence speed and calibration accuracy (within 2-mV error), the number of counting samples is set as 500. The offset adjustment only happens when the counter value of the current 500 samples is (in absolute) less than the previous one. The offset compensation is done in the analog domain at the first-stage comparator through an additional input pair. Since the counter is counting toward zero during the calibration, the depth of the counter can be short as 3 bit in this design. In the current prototype, the calibration logic is off-chip, while the offset tuning is on-chip. Only a 3-b counter, 3-b storage, a subtractor, and an arbiter are needed for the CCB calibration logics. As this calibration relies on the Gaussian output distributions of the second-stage output, it shares a similar input condition limitation as to the variance-based calibration method [25]. A busy and large input signal is needed. The input signal should be larger than several LSBs of the ADC to show a spread code distribution in the second stage. Besides, the frequency of the input signal should not be an integer multiple of the sampling frequency of each channel. Otherwise, each channel converts the same sampled signal each time and the code range in the second stage will stay in a small output code range. The size of the extra offset calibration pair of the comparator is 1/4 size of the input pair connected to the DAC, and it can cover a ±25.8-mV offset voltage range.

B. Implementation Details

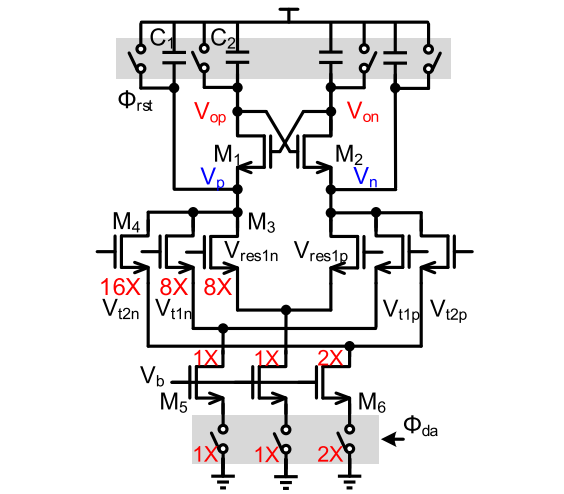
The schematic of the proposed MASH 2-0 SAR-assisted pipeline ADC is shown in Fig. 12(a). It consists of a 6-b coarse NS SAR ADC, bootstrapped sampling switches, gate-voltage-boosting integration switches, a two-way-interleaved front end, a 4-b DWA logic, channel selection switches, two integration capacitors, a gain-boosted dynamic amplifier, and a 6-b SAR ADC in the second stage. With 6-b first stage

and one-bit redundancy in the second stage, the redundancy range is ±7.5 mV. The coarse NS-SAR ADC is also in the CIFF structure, matching the fully passive CIFF operation of the main DACs. It works at full speed with its decisions transferred to the time-interleaving fine DACs, which speeds up the conversion. The two-way interleaved front end enables a long tracking time and enhances the overall ADC speed. The two fine DACs work in an interleaving fashion and generate the first-stage residue alternatively for the pipeline operation. The integration capacitors (C_{f1}, C_{f2}) between two lanes of the CIFF structure are shared to save substantial area with a low noise target in this design. A 4-b DWA logic is used to first-order shape the DAC mismatch error. Gate-voltage-boosting switches are used to shorten the required time for the charge-sharing operation between the DACs and the integration capacitors.

The operation procedure of the ADC is shown in Fig. 12(b). First, the coarse NS-SAR ADC and one of the fine DAC lanes, for example, Lane1, sample the input V_{in} at the same time during Φ_s and Φ_{s1}. Then, the coarse ADC resolves four MSBs and Lane1 adopts this 4 b through DWA logic, while at the same time, the coarse ADC converts the rest two LSBs. In such a way, the DWA is conducted without consuming any extra phases. The two LSBs' decisions are passed to the fine DAC Lane1 to generate the residue; meanwhile, the coarse ADC starts the integrating procedure on its coarse integration capacitors. Next, the residue of the first stage on Lane1 together with the voltages on two fine integration capacitors (C_{f1} and C_{f2}) is amplified by the dynamic amplifier to the second stage and the residue then is charge-shared with two integration capacitors sequentially. Concurrently, the second stage resolves the amplified signal from the first stage. The integration procedure of the coarse ADC and the fine DAC lane is separated and the capacitors in the coarse ADC are far smaller than the capacitors in the fine DAC lane. The integration time of the coarse and fine ADC is 200 and 300 ps, respectively. The amplification time of the RA is 1.5 ns. The total capacitors of the coarse and fine DAC are 64 fF and 1 pF, respectively. Each of the two integration capacitors, C_{f1} and C_{f2}, has the same value as the main capacitor DAC. The three inputs are designed with a gain ratio of 1:1:2, forming an NTF of $(1–0.5z^{-1})^2$.

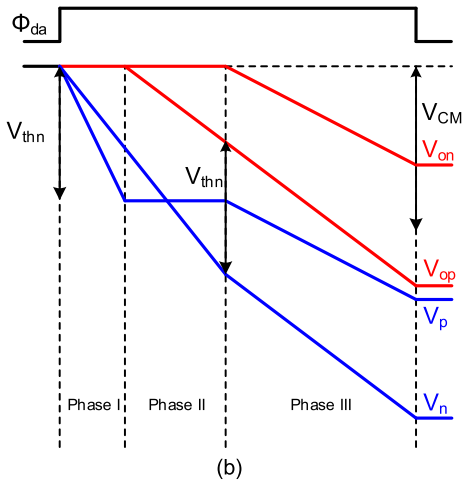
C. Time-Interleaving Associated Errors

The mismatches between channels include offset, gain, and sampling skew [11]. With two-way interleaving in this design, the tones caused by the offset mismatch are at $F_s/2$ and its multiples, where F_s is the sampling rate of the ADC. With an OSR higher than 8, those tones are outside the band of interest and are not a concern. The gain mismatch between channels mainly caused by the DAC mismatch is often small and has a negligible impact on the ADC performance with the designed resolution [11]. The signal-dependent tones caused by the clock skew are at $F_s/2 \pm F_{in}$, where F_{in} is the input signal frequency and its error amplitude increases along with higher F_{in}. To maintain an SFDR > 85 dB at the highest F_{in} of interest, the clock skew should be less than 0.52 ps, which is ensured by a careful layout. Another concern is



Transistor	M1	M3	M4	M5	M6
Size [um]	8/0.03	16/0.05	32/0.05	9.6/0.03	19.2/0.03

(a)



(b)

Fig. 13. Proposed amplifier. (a) Schematic with transistor sizes. (b) Working phases.

the mismatch between the coarse and fine DACs, while the redundancy among stages can correct such error. In this design, we have carefully matched the sampling time constant of the coarse and fine S&H circuits as well as the top-plate parasitic capacitance in the coarse and fine DACs, reducing their occupied correction range.

D. Three Inputs Gain-Boosted Dynamic Amplifier

One challenge of this architecture is implementing a relatively high inter-stage gain in the FF paths handover. While an inter-stage gain of 8× in the V_{res}-path is designed to provide enough noise suppression for the second-stage comparator, it requires a gain of 16× in the V_{t2}-path for a proper NTF. The circuit schematic of the proposed amplifier, the sizes of its transistors, and its signal behavior are given in Fig. 13 [26]. The main difference between this dynamic amplifier and the traditional one [26] is the added cross-coupling cascode pair and the extra integration capacitor C_1. Its operation can be separated into three procedures. In phase I, the cross-coupling cascode pair (M_1 and M_2) is switched OFF and the integration procedure happens on C_1. Then, the voltage of C_1 drops and

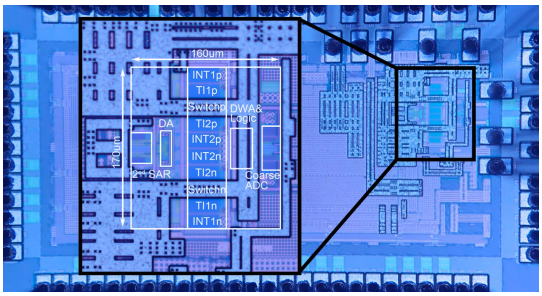


Fig. 14. Die photograph.

one of these two transistors (M_1 or M_2) switches ON. Phase II starts at this point and ends when the other cascode transistor turns on. Then, the integration procedure of C_2 happens in phase III. The integration ends when the common-mode detector detects the output common mode passed the desired reference voltage. The dynamic amplifier is then disconnected from the ground and completes the amplification. Based on the abovementioned operation, the gain of the dynamic amplifier can be derived as

$$G = \frac{g_m}{I_D}\left(\frac{C_2 + C_1}{C_2 - C_1}(V_{DD} - V_{CM}) + \frac{C_1}{C_2 - C_1}V_{thn}\right). \quad (9)$$

V_{CM} is the common-mode voltage and V_{thn} is the threshold of the cross-coupling transistors. Noted that (9) is only valid under the assumption that capacitor C_1 (76 fF in this design) is much smaller than the loading capacitor C_2 (242 fF). If C_1 is large, then phase I occupies a long integration period and affects the gain-boosted phases. It retains a similar noise performance as the conventional dynamic amplifier, whereas the extra noise induced by additional input pairs is suppressed through budgeting a longer integration time. The controlling switches and the current sources are also designed with the same ratio as the inputs to have better matching. Miyahara *et al.* [27] used a voltage-to-time amplifier with positive feedback as pre-amp of the comparator, thus only having a small load. The added cross-coupled positive feedback pair only boosts up the gain, while it does not involve in multiple phase integration. However, the proposed amplifier uses a fully positive feedback pair of cross-coupling cascode transistors to obtain an enhanced gain at high speed. What is more, due to the extra inserted integration capacitors and the two-phase integration procedure, the gain is determined by the ratio of integration capacitors and it is more stable than [27], while the linearity of the amplifier can be ensured by the nonlinearity shaping of the MASH 2-0 structure and proper sizing.

V. Measurement Results

Fabricated in 28-nm CMOS technology, the ADC occupies an area of 0.027 mm^2, as shown in the die photograph from Fig. 14. Fig. 15 shows the measured ADC's output spectrum with and without DWA. The input frequency is 2.04 MHz where more than nine harmonics are included. As a consequence of the inter-stage gain and nonlinearity error shaping ability, the proposed ADC achieves a peak SFDR and SNDR of 92.1 and 75 dB, respectively. To demonstrate the

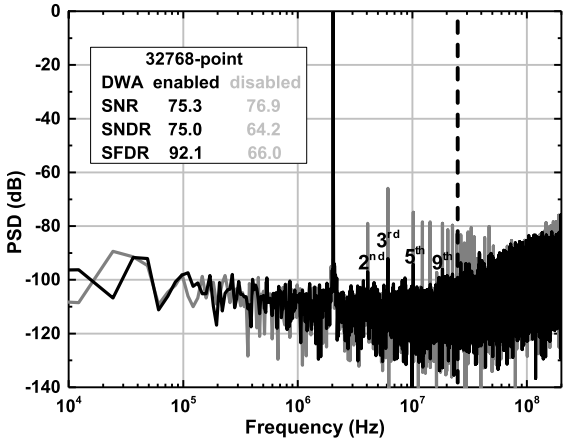


Fig. 15. Measured spectrum.

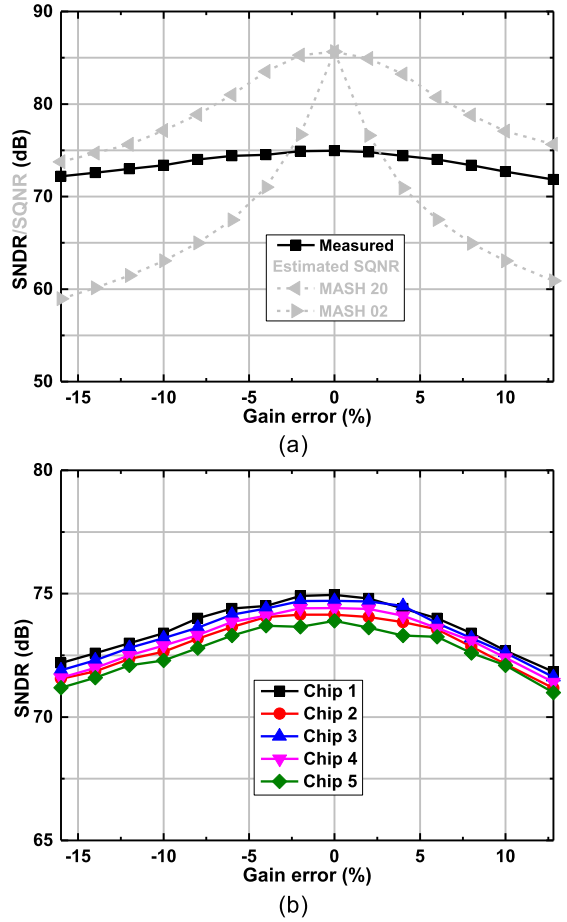


Fig. 16. Measured SNDR versus gain error (a) compared with estimated SQNR of MASH 2-0 and MASH 0-2 and (b) with five chips.

tolerant range, a wide range of gain error is introduced by adjusting the reference voltage of the second-stage SAR ADC. The reference voltage of the second-stage ADC is brought off-chip for measurement purposes. The measured SNDRs versus gain error are reported in Fig. 16(a), where the deviation is within 3 dB with the gain error between -16% and $+12\%$ at OSR $= 8$. The corresponding SQNRs are also included, which is calculated based on the assumption that the SNR limited by other errors, including the noise from the comparator, amplifier

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	Gregoire ISSCC2008 [14]	Yoshioka ISSCC2017 [15]	Song JSSC2020 [10]	Hsu JSSC2020 [20]	Song JSSC2021 [11]	Hsu JSSC2020 [21]	Wang JSSC2020 [28]	This work		
Process [nm]	180	28	65	40	28	40	28	28		
Architecture	Pipeline ADC	Pipeline SAR	0-1 MASH	Pipeline SAR	Pipeline NS SAR	Pipeline SAR	Pipeline SAR	2-0 MASH		
Inter-stage gain-error suppression scheme	Closed-loop SAR	Digital Amplifier	Closed-loop Opamp	2nd-order GES	Foreground Calibration	2nd-order GES+DEF	WACLS	Inherent Architecture		
Inter-stage offset suppression scheme	N/A	Digital Amplifier	Foreground Calibration	N/A	Background Calibration	N/A	Auto Zeroing	Code-counting-based Background Calibration		
DAC mismatch calibration	N/A	N/A	Foreground Off-chip Calibration	Foreground Off-chip Calibration	3b DWA	Foreground Off-chip Calibration	RS	4b DWA		
Supply [V]	1.2	0.7	1.0	1.0	1.0	1.0	1.1	1.0		
Fs [MHz]	20.2	160	200	100	600	100	100	400		
Power [mW]	7.5	1.9	4.5	1.54	2.56	1.38	0.7	1.26		
Area [mm^2]	2.3	0.097	0.014	0.061	0.016	0.054	0.018	0.027		
OSR	1	1	8	4	7.5	8	1	8	10	20
-3dB SNDR gain [%]	N/A	N/A	N/A	<-5 to N/A*	N/A	<-25 to N/A*	N/A	-16~ +12	-17~ +13	-19~ +14
BW [MHz]	10.1	80	12.5	12.5	40	6.25	50	25	20	10
SNDR [dB]	65	61.1	77.1	75.8	75.2	77.1	71.7	75	76.2	79.5
FoM_S [dB]**	156.3	167.3	171.5	174.9	177.1	173.7	180.2	178	178.2	178.5
FoM_W [fJ/conv.-step]***	255.5	12.8	30.8	12.2	6.8	18.9	2.2	5.5	6	8.5

*Does not provide the positive gain error data. *FoM_S=SNDR+10$\log_{10}$(BW/Power). ***FoM_W=Power/(2×BW×$2^{(SNDR-1.76)/6.02}$).

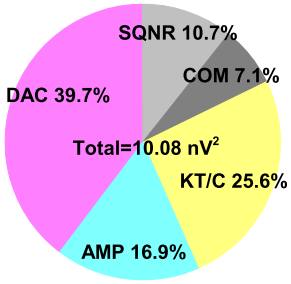


Fig. 17. Noises and DAC mismatch breakdown.

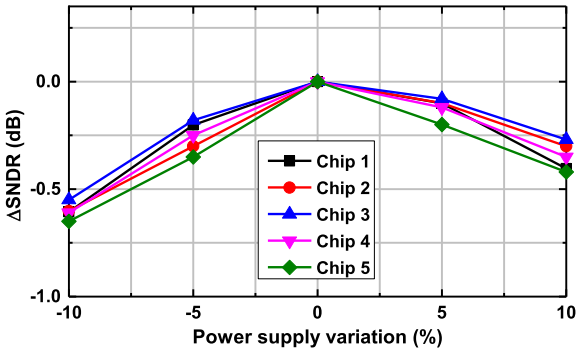


Fig. 18. Measured SNDR variations versus power supply with five chips.

and kT/C, and the DAC mismatch, is 76 dB estimated from the post-layout simulation and the measurement results. The SQNRs in Fig. 16(a) (from measurement) and Fig. 2 (behavior model) under gain variation have a good agreement with only less than 2% error. We also provide measurement results from

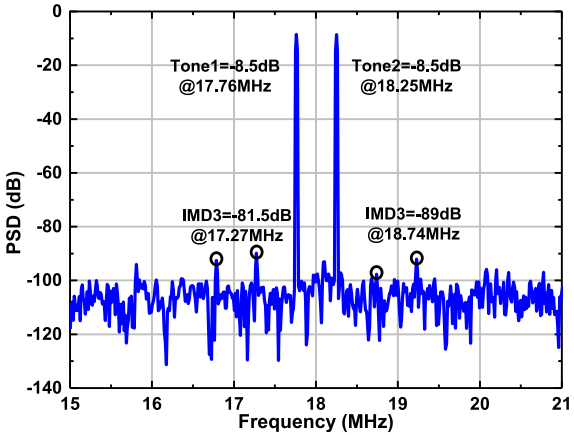


Fig. 19. Two-tone spectrum.

multiple samples in Fig. 16(b), which confirms the robustness of the designed NTF. All the samples maintain an SNDR higher than 70 dB and a similar gain error-tolerant range. It is worth highlighting that the SNDR drops steeper with a positive gain variation due to the second stage's saturation. The measured SNR is 75.3 dB for sample number 1 and the estimated contribution from the SQNR, the comparator noise, the kT/C noise, the amplifier noise, and the shaped DAC mismatch are 10.7%, 7.1%, 25.6%, 16.9%, and 39.7%, respectively, based on the simulation and measurement results, as shown in Fig. 17. According to the simulation, the gain of the dynamic amplifier varies $-14.6\% \sim 12.1\%$, $-4.1\% \sim 5.5\%$, and $16.9\% \sim -25\%$ under process, $\pm 10\%$

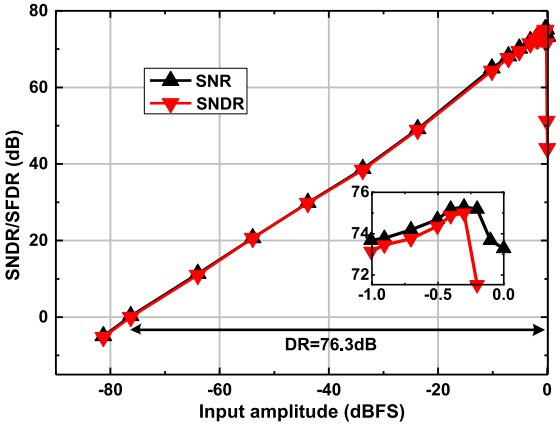


Fig. 20. Dynamic range.

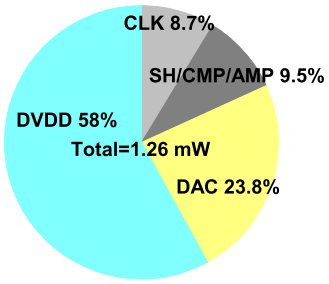


Fig. 21. Power consumption breakdown.

supply, and 0 °C–80 °C temperature variations. Five samples have been measured and their SNDR variations across ±10% supply voltages are given in Fig. 18. The largest SNDR drop is 0.65 dB, which agrees with the analysis in Section II. The two-tone spectrum with −8.5 dBFS is given in Fig. 19 and the IMD3 is −81.5 dB. Fig. 20 shows the SNR and SNDR with the DWA on versus different input amplitudes, where the dynamic range is 76.3 dB. The prototype ADC runs at 400 MHz and consumes 1.26-mW power. Fig. 21 details the power breakdown, where the digital circuits consume the major portion. Table I compares the proposed design with the state of the art in similar specifications. Unlike the GES [21] scheme, the proposed design can handle both positive and negative gain errors with small hardware overhead while still keeping a relatively high-speed operation. Reference [28] achieves a good energy efficiency without calibration. However, our SNDR is ∼4 and ∼8 dB better with OSR = 8 and OSR = 20, respectively. The prototype avoids off-chip DAC calibration and is within a −16% to +12% gain error tolerable range with OSR = 8. The proposed design exhibits a larger gain error tolerance range with a larger OSR, while the SNDR is mainly limited by other noises and nonlinearities, which cannot be shaped by the NTF. FoM_W and FoM_S of 5.5 fJ/conv.-step and 178 dB are obtained, showing that this design can maintain a good power efficiency with an additional gain error tolerance ability.

VI. Conclusion

This article presents an architectural approach (MASH N-0) inherently shaping the quantization error, comparator noise, RA gain error, and RA noise together, omitting any additional hardware. The nonlinearity of the RA is also noise-shaped, achieving good SFDR performance as well. A code-counter-based method is proposed to calibrate the inter-stage amplifier offset in the background. With the coarse NS SAR ADC, the partial-interleaving first stage, and the 4-b DWA, the prototype runs in 400 MHz and it is free from the off-chip DAC calibration. The prototype exhibits 75 dB SNDR and 25-MHz BW with background offset calibration. The resultant FoM_S is 178 dB with a gain error tolerable range of −16% to +12% in the 3-dB SNDR-deviation with OSR = 8.

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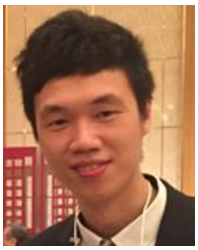

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