A 10-Bit 200-kS/s 1.76-μW SAR ADC With Hybrid CAP-MOS DAC for Energy-Limited Applications

Hongshuai Zhang, *Student Member, IEEE*, Hong Zhang, *Member, IEEE*, Yan Song, *Student Member, IEEE*, and Ruizhi Zhang

***Abstract*— This paper presents a low-power and area efficient 10-bit successive approximation register (SAR) analog-to-digital (ADC) with a hybrid capacitive-MOS consisting of a 7-bit MSB capacitive DAC (CDAC) and a 3-bit LSB MOS DAC (MDAC), which consumes less power and much smaller chip area than a pure CDAC. Instead of using a string of eight MOS transistors to control one unit capacitor, the 3-bit LSB MDAC is realized by a MOS string with four native MOS transistors to control two unit capacitors, which allows higher voltage drop and more reliable operation for each unit MOS. The overall energy consumption of the proposed CAP-MOS DAC is reduced by 56.2% compared to a Vcm-based 10-bit pure CDAC with the same unit capacitance. Under the sampling rate of 200 kS/s, the prototype 10-bit SAR ADC implemented in a 0.18-μm CMOS technology achieves a signal-to-noise-and-distortion ratio / spurious-free dynamic range of 56.91 /68.56 dB at 99-kHz input under a 0.6-V power-supply, while consumes 1.76 μW at 200 kS/s for a figure of merit of 15.38 fJ/step. The peak DNL and INL are +0.27/−0.21 LSB and +0.43/−0.45 LSB, respectively. The ADC occupies a small active area of 0.097 mm^2.**

***Index Terms*— Analog to digital converter, energy efficient, mismatch, noise, area efficient, low voltage, hybrid, CAP-MOS, successive approximation register.**

I. Introduction

ANALOG-TO-DIGITAL (ADC) converter is an essential block to digitize the analog signals in energy-limited applications such as sensing networks and implantable biomedical devices [1]–[16]. In such systems, the sensed signals are usually processed by ADCs with moderate resolution (8-12 bits) and sampling rate (1-1000 kS/s). The demands of small chip area and high energy efficiency are of great importance for these applications. Taking a cardiac pacemaker for example, it is expected to operate as long as 10 years without charging the battery, and the system's volume should also be as small as possible because it is implanted in a patient's body [13], [17]. Among others, the successive approximation register (SAR) ADC is a preferred architecture for these energy- and area-limited applications because of its digital-like structure, which usually shows smaller chip area and higher power efficiency than other topologies, especially in advanced CMOS processes.

The digital-to-analog converter (DAC) in a SAR ADC usually consumes a large portion of the total energy and chip area among all the circuit blocks. In past years, several innovative switching strategies have been proposed to reduce both the DAC switching energy and the total capacitance in the capacitive DAC (CDAC), including the energy saving [12], charge average switching (CAS) [11], charge recycling with LSB-down [7], monotonic [18], merge-and-split (MS) [8], bidirectional single-side (BSS) [19], Vcm-based [20], higher-side-reset-and-set (HSRS) [21] and one-side switching instead (OSSI) + higher bit switching instead (HBSI) [22], which reduce the switching energy by 69%, 75%, 77%, 81%, 83%, 86%, 88%, 92% and 97%, respectively, compared with the conventional approach. Most of the above schemes also achieve 50% reduction in the total capacitance except for the BSS method and OSSI + HBSI method, which can reduce the total capacitance by 75% compared to the conventional switching scheme. However, the OSSI + HBSI method requires the voltage reference V_{CM} to provide extra energy, which increases the overall energy consumption and design complexity of the reference circuit. Additionally, some methods have been proposed to reduce the energy consumption of SAR ADCs for signals with specific characteristics. In [23], a bypass window is used to select switching sequences to skip several conversion steps when the signal is within a predefined small window, resulting in significant reduction in power consumption for the ADC. The incremental converting algorithm in [5] is proposed for low frequency signals with small magnitude, which achieves a maximum reduction of 43% in the power consumption at the expense of larger circuit area and higher design complexity to realize the control scheme.

In addition to the improvements made for the switching scheme of pure CDACs, hybrid capacitive-resistive (CAP-RES) DAC, which can reduce the total capacitance and also the switching energy of the CDAC significantly, has been proved to be an effective way for SAR ADCs to achieve 10-bit

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H.-S. Zhang, H. Zhang, and R. Zhang are with the School of Electronic and Information Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: hongzhang@xjtu.edu.cn; zhanghongshuai@stu.xjtu.edu.cn).

Y. Song is with the State Key Laboratory of Analog and Mixed Signal VLSI, DECE/FST, University of Macau, Macau 999078, China.

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or even higher resolutions [24]–[26]. However, the resistive DAC (RDAC) usually consumes relatively large static current and considerable chip area under low power requirement.

This work presents a 10-bit SAR ADC structure with a hybrid CAP-MOS DAC consisting of a 7-bit MSB CDAC and a 3-bit LSB MDAC [27]. Thorough analysis from aspects of energy consumption, mismatch, area and noise is carried out, showing that the proposed CAP-MOS DAC structure consumes lower overall energy and smaller chip area than the hybrid CAP-RES DAC and pure CDAC with the same resolution and unit-capacitance. For a 10-bit resolution, the overall energy consumption of the proposed CAP-MOS DAC is reduced by 56.2% compared to the Vcm-based pure CDAC [20]. For the circuit implementation, instead of using a string of 8 MOS transistors to control one unit capacitor, the 3-bit LSB MDAC is realized by a MOS string with 4 native MOS transistors to control 2 unit capacitors, which allows higher voltage drop and more reliable operation for each unit MOS transistor.

The remainder of this paper is organized as follows. Section II gives the analysis of energy consumption, linearity and noise for hybrid CAP-MOS DAC with comparison to hybrid CAP-RES DAC and pure CDAC, and the ADC's architecture and circuit implementation are discussed in Section III. Section IV presents the measurement results of the ADC followed by conclusions drawn in Section V.

II. Design Considerations for Hybrid CAP-MOS DAC

In a high-resolution SAR ADC with pure CDAC, the ratio between the MSB and LSB capacitor of the binary DAC capacitor array is usually too large to ensure the linearity and precision performance considering the mismatch. Additionally, with given unit capacitance, the total capacitance of a pure CDAC would be too large, resulting in large chip area and high energy consumption. Hybrid CAP-RES DAC is an effective way to achieve higher resolution by reducing the total capacitance and the energy consumption in the DAC. However, under the requirement of ultra-low power consumption, the resistor array may consume large silicon area. Compared to conventional hybrid CAP-RES DAC, the MDAC in the proposed hybrid CAP-MOS DAC has an advantage of lower static current than a RDAC when driving the same capacitance under given settling requirement. Moreover, the MDAC usually consumes much smaller silicon area than a RDAC when the static current is in the sub-μA range.

The structure of the CAP-MOS DAC is given in this chapter followed by detailed analysis of the relationship between bit partition and energy consumption, linearity and noise performance, with comparison to the hybrid CAP-RES DAC counterpart.

A. Proposed CAP-MOS DAC Structure

The conceptual structure of the proposed CAP-MOS DAC for an N-bit SAR ADC is given in Fig. 1, which consists of a K-bit CDAC and an M-bit MDAC ($N = K + M$). The CDAC consists of K-1 binary weighted capacitors and operates with

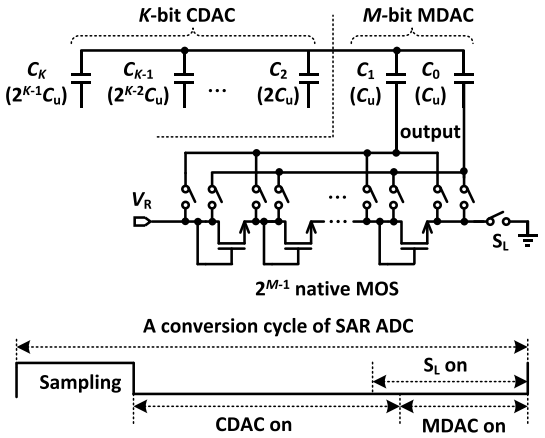

Fig. 1. Conceptual structure of the proposed hybrid CAP-MOS DAC.

the Vcm-based switching scheme [20]. Instead of using a string of 2^M MOS transistors to control one unit capacitor, the M-bit LSB MDAC is realized by a MOS string with 2^{M-1} MOS transistors to control 2 unit capacitors, which allows higher voltage drop and more reliable operation for each unit MOS. The structure reduces the amount of unit capacitor by a factor of 2^{M-1} compared to an N-bit Vcm-based pure CDAC, implying that much energy consumption and silicon area are expected to be saved.

As Fig. 1 shows, the CDAC is in operation at first to solve the K-bit MSBs in a SAR ADC conversion cycle. Then, the MDAC is turned on to solve the M-bit LSBs. As in [24], a switch SL is used to turn off the MDAC when it is not in operation to save power further.

B. Energy Consumption Analysis

The switching energy of the differential K-bit Vcm-based CDAC in Fig. 1 can be obtained as

$$E_{\mathrm{CDAC}} = \sum_{i=1}^{N-M-1} 2^{N-M-2i-1}(2^i - 1)C_{\mathrm{u}}V_{\mathrm{R}}^2 \tag{1}$$

On the other hand, the static energy consumed by the MDAC depends on the static current flowing through the MOS string. In order for low-voltage operation, native MOS transistors with near-zero threshold voltage are chosen for the MOS string, which are available in most mixed-signal CMOS technologies.

The drain current of a diode-connected MOS can be expressed as

$$I_{\mathrm{D}} = \frac{1}{2}\frac{W}{L}K'(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \tag{2}$$

where V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, W/L represents the aspect ratio of the MOS, $K'(= \mu_{\mathrm{n}}C_{\mathrm{ox}})$ is the transconductance coefficient, μ_{n} is the carrier mobility, and C_{ox} is the gate-oxide capacitance. Fig. 2 plots the simulated I/V curve of a native MOS with $W/L = 1\mu\mathrm{m}/10\mu\mathrm{m}$ in the used technology, which shows a threshold voltage of about -4mV. Ideally, each MOS in the MDAC string has a voltage drop of $V_{\mathrm{GS}} = V_{\mathrm{R}}/2^{M-1}$ in steady state.

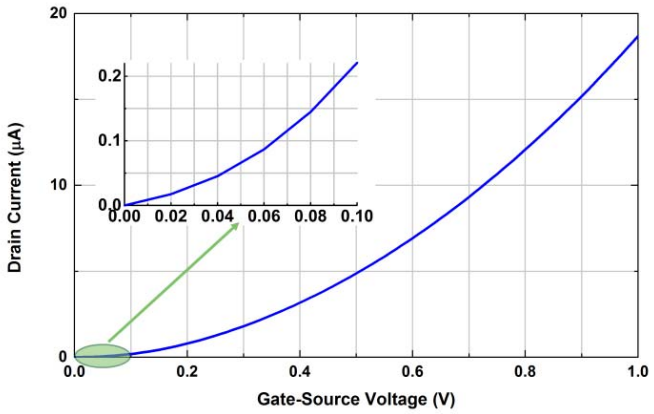

Fig. 2. Simulated I/V curve of a diode-connected native MOS ($W/L = 1/10\ \mu$m).

As the V_{TH} of a native MOS is around zero, the average static power can be written approximately as

$$P_{MDAC} \approx \eta V_R \cdot \frac{1}{2}\frac{W}{L}K'\left(\frac{V_R}{2^{M-1}}\right)^2 \tag{3}$$

where η is the duty cycle that the resistive string is on in a period of the sampling clock, T_{CKS}. Assuming the period of the internal clock period for SAR operation is T_{CKC}, then $T_{CKS} = (M + K + D_S)T_{CKC}$, where D_S is the number of internal clock cycles needed for sampling of the input signal. Therefore, the coefficient η in (3) can be written approximately as

$$\eta \approx (M + D_R)/(N + D_S) \tag{4}$$

where D_R is the number of additional clock cycles for the resistive string to be turned on before the MDAC's operation.

Obviously, the minimum value of W/L in (3) needs to be determined according to the settling requirement of the DAC's output voltage. Because the MDAC shows a nonlinear settling process, the small-signal of the unit MOS in steady state is used for approximation. The small-signal resistance of the diode-connected unit MOS can be written as

$$r_u = \frac{1}{g_m} = \frac{2^{M-1}}{(W/L)K'V_R} \tag{5}$$

where g_m is the transconductance of the unit MOS in saturation region. The maximum output resistance is $2^{M-3}R_u$ for the MDAC when its output is $V_R/2$, and the overall capacitance seen by the string is approximately $2C_u$. Then the worst-case time constant is about $2^{M-2}C_uR_u$. Assuming that the voltage of the MDAC needs to settle to its final value with a precision of $0.5V_R/2^M$ in $T_{CKC}/2$, the MOS parameters can be derived as

$$\left(K'\frac{W}{L}\frac{V_R}{2^{M-1}}\right)_{min} = \frac{2^{M-1}\ln(2^{M+1})C_u}{T_{CKC}} \tag{6}$$

Substituting (6) into (3) and considering $T_{CKS} = (N + D_S)T_{CKC}$, the static energy consumed by the MOS string in a period of T_{CKS} can be calculated in terms of ${V_R}^2C_u$:

$$E_{MDAC,st\text{-}ideal} \approx T_{CKS}P_{MDAC} = \frac{1}{2}\eta(N + D_S)\ln(2^{M+1}){V_R}^2C_u \tag{7}$$

In order to show the advantage of MDAC over the conventional RDAC, the ideal energy consumption of the RDAC can also be calculated in terms of ${V_R}^2C_u$ under given settling requirement. If the unit MOS in the MOS string in Fig. 1 is replaced by an unit resistor with value of R_u, the ideal energy consumption of the RDAC in a period of T_{CKS} can be obtained using a similar deriving procedure from (3) to (7):

$$E_{RDAC,st\text{-}ideal} \approx \eta(N + D_S)\ln(2^{M+1}){V_R}^2C_u \tag{8}$$

Comparing (7) and (8), the energy consumption of the proposed MDAC is only half of that for a RDAC under the same DAC architecture and settling requirement.

The result in (7) is obtained with the small-signal resistance of the MOS in steady state, meaning that even smaller W/L can be used for the unit MOS because the MOS string can provide larger charge/discharge current in the settling process than that implied by the linear small-signal resistance R_u given by (5). However, when considering process variations, the value of W/L should be enlarged correspondingly to ensure the required settling behavior under all operation conditions. In this work, Monte-Carlo simulation result shows that process variations can be accommodated safely if the aspect ratio (also DC current) of each MOS is increased by a factor of 3 from the value defined by (6). Neglecting the dynamic energy in the MDAC for a fully differential implementation, the overall average energy consumption of the hybrid CAP-MOS DAC can be estimated as

$$E_{C\_M} \approx E_{CDAC} + 6E_{MDAC,st\text{-}ideal} \tag{9}$$

Similarly, considering equal margin for process variation, the average energy for a hybrid CAP-RES DAC is

$$E_{C\_R} \approx E_{CDAC} + 6E_{RDAC,st\text{-}ideal} \tag{10}$$

According to (9) and (10), Fig. 3 plots the total average energy dissipation of the hybrid DAC for different partitioning schemes in 10-bit and 12-bit SAR ADCs, respectively ($D_R = 1$, $D_S = 3$). It can be seen that the hybrid CAP-MOS DAC consumes smaller total DAC energy compared to the hybrid CAP-RES DAC for both the 10-bit and 12-bit ADCs. The optimum bit partitions of the hybrid CAP-MOS DAC are at $K = 6$ and $K = 7$ for the 10-bit and 12-bit SAR ADCs, respectively, while the optimum bit partition points of the hybrid CAP-RES DAC are at $K = 7$ and $K = 8$ for the 10-bit and 12-bit SAR ADCs, respectively.

Obviously, at the optimum bit partition point, both hybrid DAC structures consume much smaller energy than the pure CDAC (the cases of $K = 10$ and $K = 12$ for the 10-bit and 12-bit SAR ADCs, respectively) with the same unit capacitance.

C. Linearity Analysis

As in conventional SAR ADCs, the value of C_u and the size of the unit MOS cannot be too small because both the mismatch in the capacitors of the CDAC and the mismatch in the MDAC can lead to degradation in the static linearity

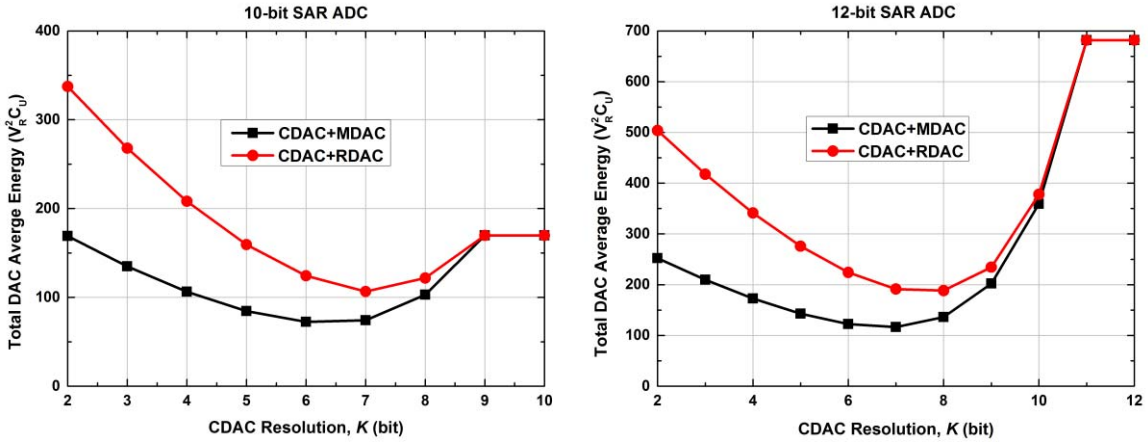

Fig. 3. Total DAC average energy dissipation of the hybrid CAP-RES and CAP-MOS DACs for 10-bit and 12-bit SAR ADCs ($D_R = 1$, $D_S = 3$).

performance. In the MDAC, mismatches in each MOS will cause a ΔV_{GS} in its V_{GS} [28],

$$V_{GS} + \Delta V_{GS} = (V_{TH} + \Delta V_{TH}) + \frac{\sqrt{2I_D}}{\sqrt{(W/L + \Delta_{W/L})(K' + \Delta K')}} \quad (11)$$

where ΔV_{TH}, $\Delta_{W/L}$ and $\Delta K'$ are the mismatch errors in V_{TH}, W/L and K', respectively. These three error terms are known to be Gaussian variables with zero means and standard deviations of σ_{VTH}, $\sigma_{W/L}$ and $\sigma_{K'}$, respectively:

$$\sigma_{VTH} = \frac{A_{VTH}}{\sqrt{WL}}; \quad \frac{\sigma_{W/L}}{W/L} = \frac{A_{W/L}}{\sqrt{1/W^2 + 1/L^2}}; \quad \frac{\sigma_{K'}}{K'} = \frac{A_{K'}}{\sqrt{WL}} \quad (12)$$

where A_{VTH}, $A_{W/L}$ and $A_{K'}$ are process parameters. Therefore, ΔV_{GS} can be assumed as a Gaussian random variable with zero mean and standard deviation of $\sigma_{\Delta VGS}$. As the MDAC is an unit-element array, its DNL is almost code-independent, and is determined only by ΔV_{GS} of each unit MOS. On the other hand, it can be assumed that the unit capacitor C_u has an error term of ε_u, which is a Gaussian random variable with zero mean and standard deviation of σ_u. If the capacitors in the CDAC array ($C_2 \sim C_K$ in Fig.1) are realized with parallel connected unit capacitors, their error terms ($\varepsilon_2 \sim \varepsilon_K$) can be thought as independent variables with variance of

$$E(\varepsilon_i^2) = 2^{i-1}\sigma_u^2 \quad (13)$$

For the proposed DAC, the worst DNL occurs at the mid code transition (from $011\cdots1$ to $100\cdots0$). The difference between the error voltages at these two steps can be derived as

$$\Delta V_{err,max} \approx \frac{2\Delta V_{GS}C_u + \left(\varepsilon_K - \sum_{i=2}^{K-1}\varepsilon_i\right)V_R}{2^K C_u} \quad (14)$$

The mismatch error in C_1 and C_0 are neglected in (14) for simplicity, which has negligible contribution to the voltage error. The variance of (14) can be calculated as

$$E\left(\Delta V_{err,max}^2\right) \approx \frac{4\sigma_{\Delta VGS}^2 C_u^2 + 2^K\sigma_u^2 V_R^2}{2^{2K}C_u^2} \quad (15)$$

Then, the DNL's standard deviation can be calculated as

$$\sigma_{DNL,max} = \frac{\sqrt{E\left(\Delta V_{err,max}^2\right)}}{V_R/2^{N-1}} \approx \sqrt{\frac{2^{2N}\sigma_{\Delta VGS}^2}{2^{2K}V_R^2} + \frac{2^{2N+K-2}}{2^{2K}}\frac{\sigma_u^2}{C_u^2}} \quad (16)$$

Considering $N = M + K$, and the nominal value of $V_{GS} = V_R/2^{M-1}$, (16) can be rearranged as

$$\sigma_{DNL,max} \approx \sqrt{\left(2\frac{\sigma_{\Delta VGS}}{V_{GS}}\right)^2 + 2^M 2^{N-2}\left(\frac{\sigma_u}{C_u}\right)^2} \quad (17)$$

Similarly, if the unit resistor R_u in a hybrid CAP-RES DAC has an error term of ε_r, which is also a Gaussian random variable with zero mean and standard deviation of σ_r. Then the maximum error voltage and the DNL's standard deviation of the hybrid CAP-RES DAC can be obtained as

$$\Delta V_{err,max\_CAP\text{-}RES} \approx \frac{2\left(\frac{\sigma_r}{R_u}\frac{V_R}{2^{M-1}}\right)C_u + \left(\varepsilon_K - \sum_{i=2}^{K-1}\varepsilon_i\right)V_R}{2^K C_u} \quad (18)$$

$$\sigma_{DNL,max\_CAP\text{-}RES} \approx \sqrt{\left(2\frac{\sigma_r}{R_u}\right)^2 + 2^M 2^{N-2}\left(\frac{\sigma_u}{C_u}\right)^2} \quad (19)$$

To compare the component mismatch's effects on the 2 hybrid DAC structures, behavioral simulation has been performed for a 10-bit and a 12-bit SAR ADC in Matlab assuming $\sigma_r/R_u = 1\%$, $\sigma_u/C_u = 1\%$ and $W/L = 4.5\mu m/10\mu m$. The process parameters are $A_{VTH} = 3.65\ mV \cdot \mu m$, $A_{W/L} = 0.02\ \mu m$ and $A_{K'} = 0.0056\ \mu m$ for the used technology. At a given bit partition point, the expected ENOB is obtained as the average ENOB from a 1000-run Monte-Carlo simulation of the ADCs with above mismatch parameters for a sinusoid input signal. Fig. 4 plots the simulated expected ENOB of the 10-bit and 12-bit SAR ADCs with different hybrid DAC structures. For a 10-bit ADC, the hybrid CAP-RES and CAP-MOS structures achieve almost the same expected ENOB for bit partition schemes of $K \geq 5$. Additionally, the ENOB at the bit partition of $K = 7$ is about 9.71 bit for both hybrid structures, which is only 0.19 bit less than the pure CDAC case ($K = 10$).

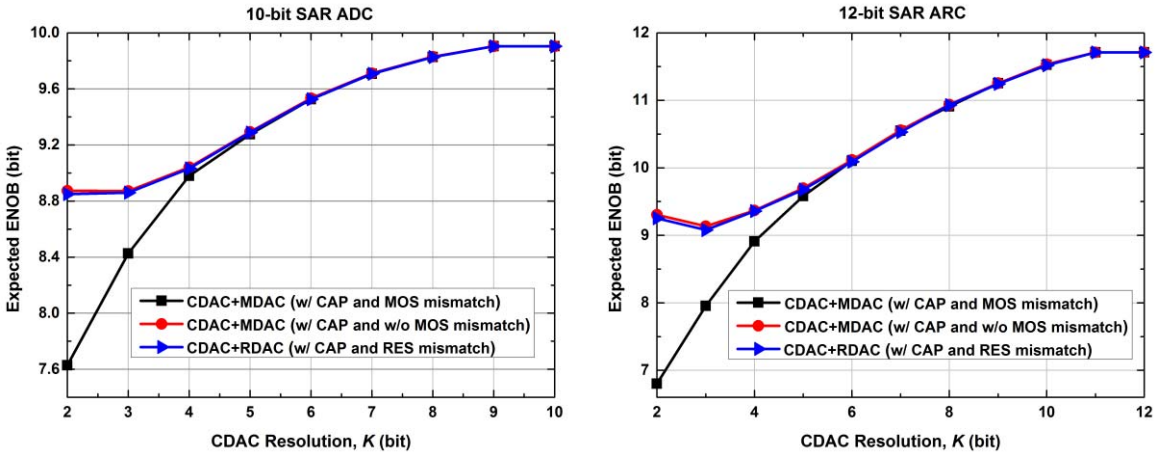

Fig. 4. Simulated expected ENOB for a 10-bit and a 12-bit SAR ADC with different hybrid DAC structures considering device mismatches ($\sigma_u/C_u = 1\%$, $\sigma_R/R_u = 1\%$, $W/L = 4.5\mu$m/10μm, $A_{VTH} = 3.65$ mV $\cdot\ \mu$m, $A_{W/L} = 0.02\mu$m, and $A_{K'} = 0.0056\ \mu$m).

On the other hand, for the 12-bit ADC with the same mismatch parameters, both hybrid structures can achieve ENOBs larger than 11 bit only if $K \geq 9$.

The simulation results also show that the expected ENOBs are mainly determined by the capacitor's mismatch if K is large enough, which is consistent with above theoretical derivation.

D. Noise Analysis

Because the total capacitance involved in the sampling process depends on the exact hybrid DAC structure, the noise performance may vary with the exact bit partition scheme. The kT/C noise due to sampling for the CDAC depends on the total sampling capacitor C_s as follows [29]:

$$C_s = 2^K C_u \tag{20}$$

$$P_{ns\_CDAC} = \frac{2kT}{C_s} = \frac{kT}{2^{K-1}C_u} \tag{21}$$

where P_{ns_CDAC} is the effective differential noise power due to sampling.

For the MOS string in the MDAC, it can be verified that the noise density at the middle point of the MOS string can be thought as the noise density contributed by a single transistor [30]:

$$\overline{V_n^2} = \frac{4kT\gamma}{g_m} + \frac{K_f}{C_{ox}WL}\frac{1}{f} \tag{22}$$

where γ is the noise coefficient, k is the Boltzmann constant, T is the absolute temperature, K_f is the process-dependent constant for flicker noise, and f is frequency. Assuming that the area of the transistor gate in the MDAC is relatively large, the flicker noise is neglected to simplify the analysis. Then the total effective differential noise power of the MDAC is

$$P_{ns\_MDAC} = \frac{2kT\gamma}{C_{eq}} \tag{23}$$

where C_{eq} is the equivalent capacitance seen by the MDAC

$$C_{eq} = \frac{2^K - 2}{2^{K-1}}C_u \tag{24}$$

When considering the noise contribution from the MDAC to the sampling node in the hybrid CAP-MOS DAC structure, the noise voltage of the MOS string will be attenuated by a factor H:

$$H = \frac{1}{2^{K-1}} \tag{25}$$

From (21) to (25), the total noise power for the hybrid CAP-MOS DAC can be obtained as

$$P_{ns\_CAP\text{-}MOS} = \frac{kT}{2^{K-1}C_u} + \frac{kT\gamma}{(2^{2K-2} - 2^{K-1})C_u} \tag{26}$$

Similarly, the total noise power for the hybrid CAP-RES DAC is

$$P_{ns\_CAP\text{-}RES} = \frac{kT}{2^{K-1}C_u} + \frac{kT}{(2^{2K-2} - 2^{K-1})C_u} \tag{27}$$

Comparing (26) and (27), the noise power of the hybrid CAP-MOS DAC is a little smaller than the hybrid CAP-RES DAC assuming $\gamma = 2/3$. Considering only the noise contribution, Fig. 5 shows the simulated expected ENOB of the 10-bit and the 12-bit SAR ADC for different hybrid DAC structures. In the simulation, the unit capacitor is 4.84fF which is consistent with the matching condition of $\sigma_u/C_u = 1\%$ for the technology used. It can be seen that the thermal noise's effect can be neglected safely if $K \geq 6$ for the 10-bit ADC ($K \geq 7$ for the 12-bit ADC), which verifies that the noise is indeed dominated by the CDAC.

III. ADC Architecture and Circuit Implementation

To verify the effectiveness of the proposed approach, a fully differential 10-bit, 200-kS/s SAR ADC with hybrid CAP-MOS DAC is designed in a 0.18-μm CMOS technology for biomedical devices and sensing systems. Both the power supply and voltage reference for the ADC core are selected as 0.6 V to reduce power dissipation.

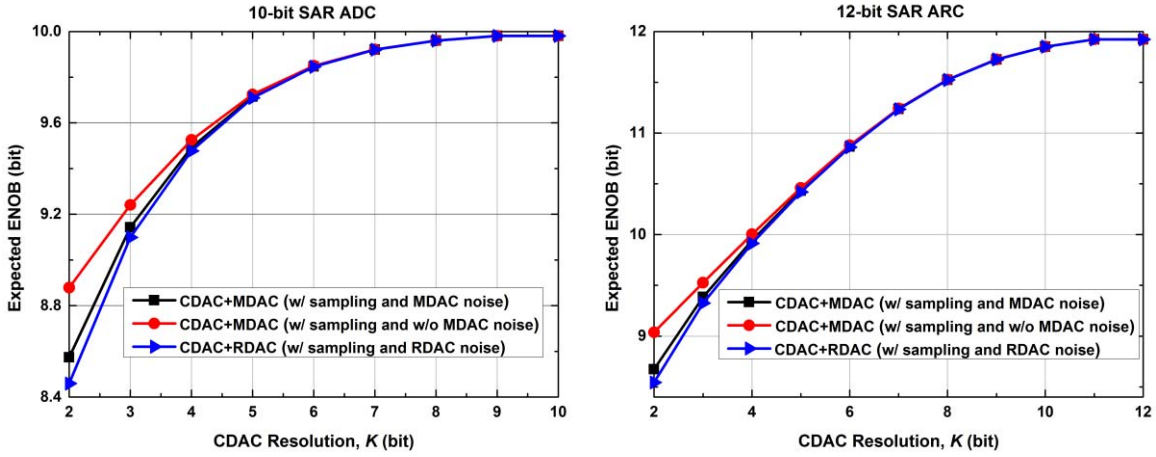

Fig. 5. Simulated expected ENOB for a 10-bit and a 12-bit SAR ADC with different hybrid structures considering noise ($C_u = 4.84$fF, $V_{FS,diff} = 1.2$V).

A. ADC Architecture

Base on above analysis, for a given unit capacitance, a larger K means better noise and linearity performances. From these two aspects, a pure CDAC ($K = 10$) is the best choice. However, when considering the DAC's energy consumption (Fig. 3), the optimum bit partition occurs at $K = 6$ ($M = 4$) while the energy consumption for $K = 7$ ($M = 3$) is only a little bit larger than that for $K = 6$. From the view of circuit implementation, the voltage drop of each MOS transistor for $K = 7$ is twice of that for $K = 6$, meaning that more reliable operation can be obtained for the MOS string in the case of $K = 7$. From Fig. 4 and Fig. 5, this choice can ensure an expected ENOB larger than 9.5 bit considering device mismatch and thermal noise. Therefore, the bit partition of $K = 7$ ($M = 3$) is chosen for this design, which can save about $95{V_R}^2C_u$ in average energy saving compared with the 10-bit pure CDAC case ($K = 10$), showing that the proposed hybrid structure is efficient in energy consumption.

From the aspect of power consumption, the unit capacitance should be minimized to reduce the energy consumed by the DAC [29], [31]. However, as analyzed above, the size of the unit capacitance influences the ADC's linearity performance directly. According to (17) and 3-σ principle ($\sigma_{DNL} < (1/6)$ LSB), the minimum σ_u/C_u is calculated to be 0.37% for $N = 10$ and $M = 3$. This value is more conservative than that used in the behavioral simulation, which will lead to larger energy consumption. However, this tighter matching requirement can ensure the required yield for mass production. For the metal-insulator-metal (MIM) capacitor with a nominal density of 2.071fF/μm^2 in the used technology, C_u is calculated to be at least 30.4 fF according to method in [7]. However, the minimum available capacitor in the technology is 62.2 fF (5 μm$\times$5 μm). Therefore, by connecting two smallest MIM capacitors in series, C_u is realized as 31.1 fF for better matching. The resulted single-side input capacitance is about 3.98 pF, which is large enough to ensuer the DAC's noise performance.

Fig. 6 plots the simulated root-mean- square (RMS) of DNL and INL in 10000-run Monte-Carlo simulation for a 10-bit SAR ADC with the proposed hybrid scheme CAP-MOS DAC ($K = 7$, $M = 3$). The maximum DNL and INL are both 0.323 LSB. Therefore, the selection of the unit capacitance can ensure the linearity requirement for the ADC. Additionally, Fig. 4 also shows that the matching requirement for the MDAC can be looser than that for the CDAC.

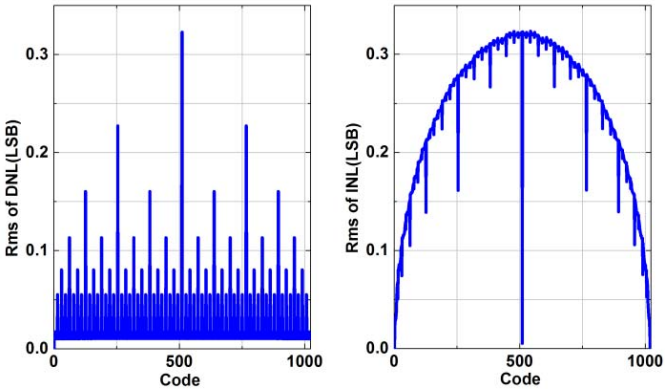

Fig. 6. The standard deviations of DNL and INL obtained in 10000-run Monte Carlo behavioral simulations, with Gaussian errors in the unit capacitor ($\sigma_u/C_u = 1\%$, $W/L = 4.5\mu$m/10μm, $A_{VTH} = 3.65$ mV $\cdot\ \mu$m, $A_{W/L} = 0.02\mu$m, and $A_{K'} = 0.0056\ \mu$m).

Furthermore, to show the advantage of the proposed CAP-MOS DAC's smaller silicon area, Table I roughly compares this area to that of the hybrid CAP-RES DAC and the pure CDAC. The unit capacitance is the same for the three DAC structures, while the hybrid CAP-RES and the hybrid CAP-MOS DAC have the same bit partition scheme ($K = 7$ and $M = 3$). The unit resistor for the hybrid CAP-RES DAC is calculated according to the settling requirement similar with (6), and poly resistors with 1-KΩ sheet resistance and 1-μm width are used to estimate the area. The unit MOS in the MDAC has a size of $W = 0.46\mu$m and $L = 10\mu$m. Table I shows that the hybrid CAP-MOS DAC saves 85.3% and 40.1% DAC areas compared with the pure CDAC and the hybrid CAP-RES DAC, respectively.

Fig. 7 shows the architecture of the proposed fully differential SAR ADC. The 7-bit MSB CDAC consists of 6 pairs of binary capacitors ($C_7 \sim C_2$), while the 3-bit LSB MDAC is realized by a MOS string with 4 equal-sized MOS transistors to control the two unit capacitors (C_1 and C_0). Other necessary

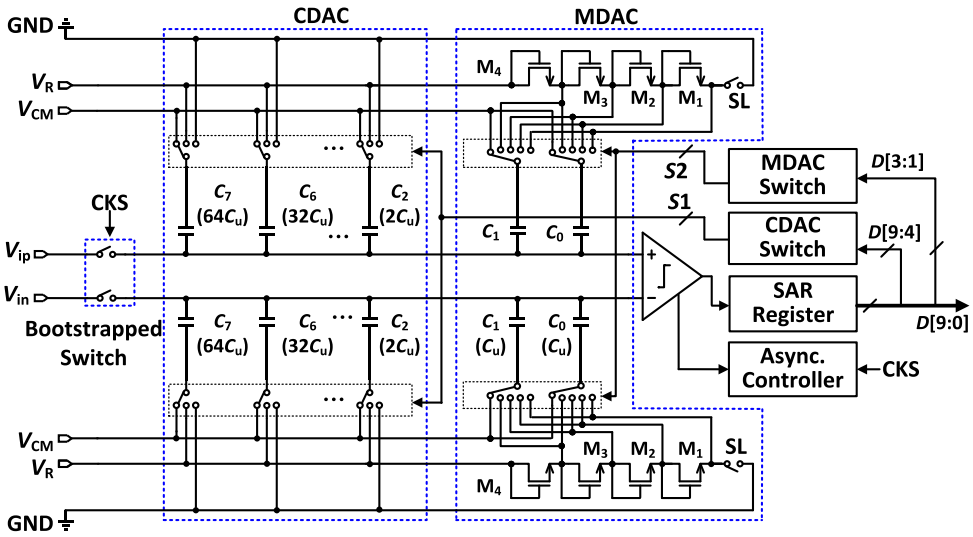

Fig. 7. Architecture of the proposed ADC.

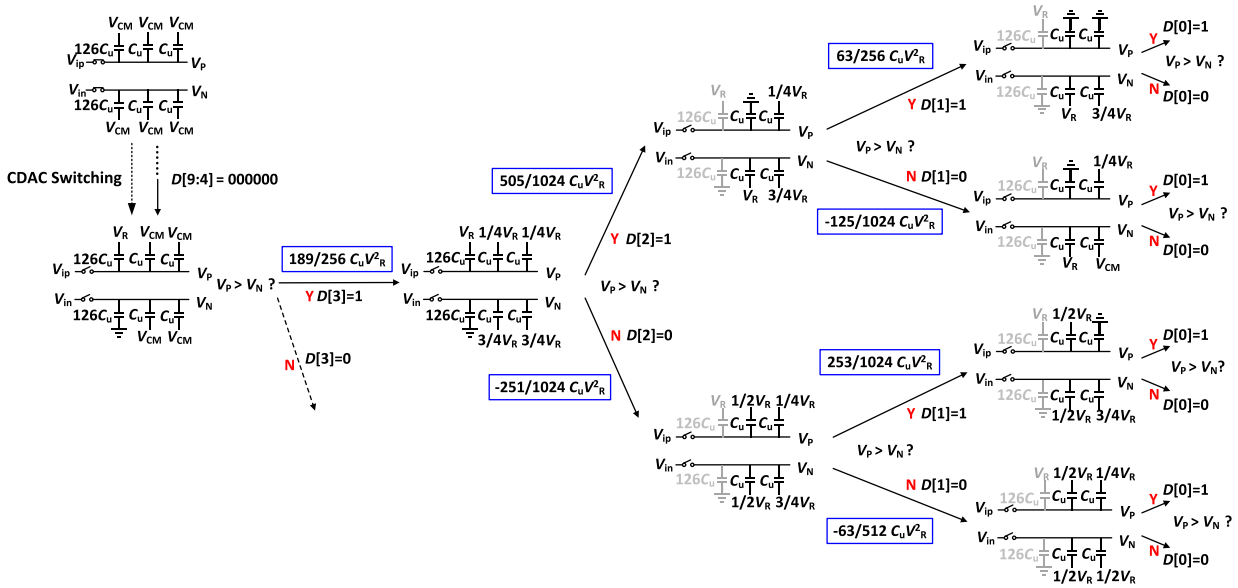

Fig. 8. Detailed switching procedure and switching energy of the MOS DAC for an example case of $D[9:4] = 000000$ (only half is shown for simplicity).

TABLE I

COMPARISON OF ESTIMATED DAC AREA FOR DIFFERENT DAC STRUCTURES

A 10-bit SAR ADC	Pure CDAC*	CAP-RES DAC*$^{\&}$	CAP-MOS DAC*$^{\#}$
Area of Cap.(μm^2)	25600	3200	3200
Area of Res.(μm^2)	--	3100.8	--
Area of MOS.(μm^2)	--	--	571.8
DAC area.(μm^2)	25600	6300.8	3771.8

*$V_R = 0.6$V, $T_{CKS} = 5\mu$s, $T_{CKC} = 0.38\mu$s, $C_u = 62.2$fF
$^{\$}K = 7$, $M = 3$
$^{\&}R_u = 280$ KΩ (poly resistors with 1-KΩ sheet resistance and 1-μm width)
$^{\#}$Unit MOS: $W = 0.46\mu$m; $L = 10\mu$m

blocks include a pair of bootstrapped switch, a comparator, an asynchronous controller, a SAR register and two switch signal generators for the CDAC and the MDAC, respectively.

B. Hybrid DAC Switching Procedure

When the main clock CKS is high, the input signal is sampled onto the top plates of the capacitors, while the bottom plates of all capacitors are initialized by V_{CM}. After that, the CDAC operates with the Vcm-based switching scheme to solve the 7-bit MSBs, $D[9:3]$, in which $D[9]$ is solved directly after the sampling phase. After the CDAC's operation, the bottom plates of C_1 and C_0 are charged by the MDAC in three sequential steps to solve the 3 LSBs. The detailed switching procedure for the MDAC is shown in Fig. 8 (only half is shown for simplicity). The first two steps operate in a fully differential way to keep the CM level for the comparator as V_{CM}. As shown in Fig. 8, single-side switching is adopted in the last step, in which only one MOS string changes its output to lower values, while the other keeps its output unchanged. In this way, only 4 MOS instead of 8 are needed for each

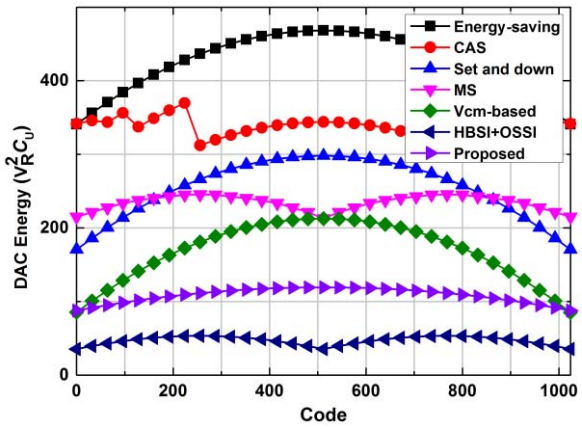

Fig. 9. Energy consumption varies with code for different switching schemes.

string to generate a differential step of $V_R/4$. The cost is that the CM level decreases by $V_R/1024$, which is negligible to the operation of the comparator.

From Fig. 8, the average dynamic energy consumption of the MDAC can be derived as

$$E_{\mathrm{MDAC,dy}} = (-11 \times 2^{-N-1} + 7/16) C_u {V_R}^2 \tag{28}$$

Adding $E_{\mathrm{MDAC,dy}}$ into (9), the total energy consumption is

$$E_{\mathrm{tot,pro}} \approx E_{\mathrm{CDAC}} + 6E_{\mathrm{MDAC,st\text{-}ideal}} + E_{\mathrm{MDAC,dy}} \tag{29}$$

For $\eta = 0.3$, $K = 7$ and $M = 3$, the first, second, and third terms in (29) are calculated as 41.67, 32.44, and 0.43 $C_u {V_R}^2$, respectively, amounting to a total average energy consumption of 74.54 $C_u {V_R}^2$, which is reduced by 56.2% compared to that of the Vcm-based scheme (170.2 $C_u {V_R}^2$) [20]. Fig. 9 plots the total energy consumption of the proposed hybrid DAC as a function of the output code, with comparison to other well-known switching schemes for 10-bit pure CDAC ADCs. It shows that the proposed hybrid CAP-MOS DAC consumes less DAC energy than most of the DACs except for the DAC with the HBSI and OSSI method. The OSSI and HBSI method achieves very low switching energy with an optimized switching scheme for a pure CDAC. The proposed hybrid DAC structure reduces the overall SAR ADC capacitance, which is helpful to reduce the active area and energy consumption. It shows higher energy consumption than the OSSI and HBSI method because its CDAC employs a Vcm-based switching scheme. If other more optimized switching strategies, such as the OSSI and HBSI method, are used for the CDAC in the proposed hybrid structure, even lower energy consumption can be expected.

C. Circuit Implementation

The W/L of each MOS in the MDAC is designed as 0.46μm/10μm, which is about 3-times larger than that required by (6) to accommodate possible process variations. The DC current in each string is about 205 nA. To compensate voltage errors caused by body effect, the width of each MOS is adjusted slightly according to detailed simulation, as given in Table II. The total gate area of all the MOS transistors

TABLE II
WIDTH ADJUSTMENT FOR BODY-EFFECT COMPENSATION
(UNIT: μM, $L = 10\ \mu$M)

	M_1	M_2	M_3	M_4
W	0.425	0.455	0.485	0.525

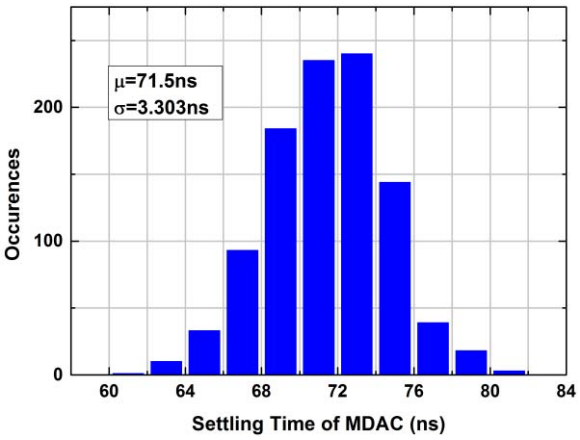

Fig. 10. Monte-Carlo simulation results of 1000 runs for the settling time of the MDAC under process variations.

in the 2 MOS strings is 37.8 μm^2, which is less than the sum of 2 unit capacitors' area. As the amount of capacitors is reduced by a factor of 4 compared to a 10-bit pure Vcm-based CDAC and the area consumed by the MDAC is quite small, the proposed ADC is indeed area efficient.

Monte-Carlo simulation with 1000 runs has been performed to verify that the settling time of the MDAC fulfills the requirement under process variations, with simulation results given in Fig. 10. As can be seen, as the W/L value is enlarged by 3 times from the ideal value, even the worst-case settling time is less than $T_{\mathrm{CKC}}/4$ (96 ns).

Another Monte-Carlo simulation with 300 runs has also been conducted to obtain the distribution of V_{GS} for each MOS in the MDAC, with the worst-case distribution given in Fig. 11, showing a standard deviation of 1.132mV. According to (17), because $\sigma_{\Delta \mathrm{VGS}}/V_{\mathrm{GS}}$ is only 0.7%, it would cause negligible influence on the ADC's static linearity.

The logic circuit structure including the asynchronous controller, SAR register and switch signal generators for the CDAC and MDAC is given in Fig. 12(a), with timing diagram given in Fig. 12(b). The structure of the asynchronous controller is similar with that in [5], which generates the clock signals CK9 to CK0 for the SAR registers and the switch signal generators. The main clock signal, CKS is provided externally with a duty cycle of about 20%, while the Valid signal is generated by the comparator indicating that the comparison results is ready for processing. At the rising edges of CK9 to CK0, the SAR registers sample the comparison result, COMP, sequentially to generate the digital output D[9:0]. With D[9:4], and CK9 to CK4, the CDAC switch signal generator generates the control signals for the CDAC switches according to the Vcm-based switching scheme. On the other hand, with

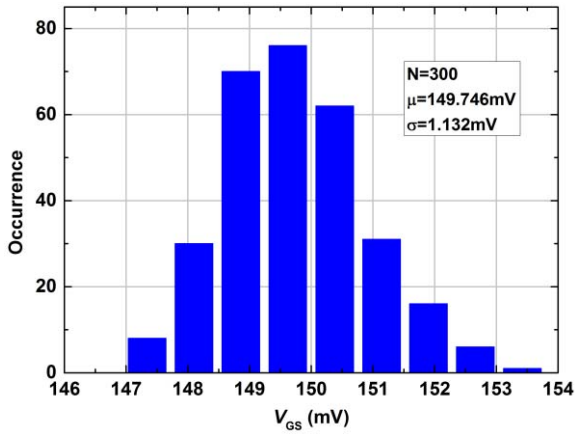

Fig. 11. Worst-case distribution of V_{GS} for the 4 MOS transistors of MDAC obtained from 300-run Monte Carlo simulation.

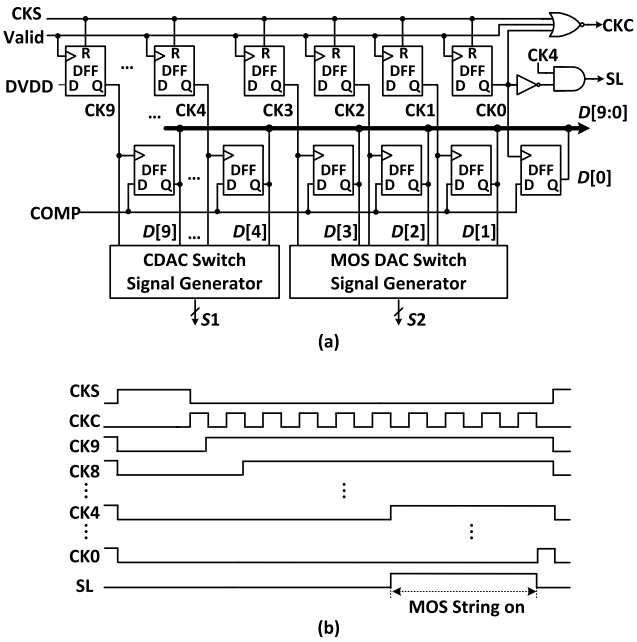

Fig. 12. Logic circuits in the proposed ADC. (a) Structure. (b) Timing diagram.

D[3:1] and CK3 to CK1, the MDAC switch signal generator selects the MDAC's output according to the proposed switching procedure. All the 10-bit conversion results are sampled to output at the rising edge of CK0.

As can be seen, the switch signal for the MOS string, SL, is generated by CK4 and CK0, which turns on the MOS string one cycle before the MDAC's operation. This ensures enough time for the MDAC to be ready before operation. The total on-time of the MOS string is about 30% of one CKS cycle.

The dynamic comparator with self-down control logic in [5] is employed in this paper, as shown in Fig. 13. When CKC is low, V_{op} and V_{on} are set to VDD. The rising edge of CKC triggers the comparison of the two input voltages. The regeneration of the latch forces one output to high and the other to low according to the difference between the

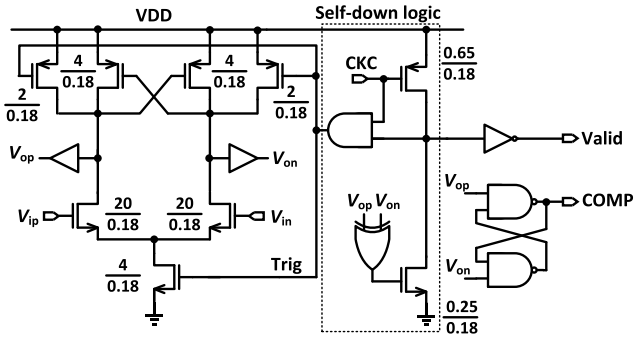

Fig. 13. Dynamic comparator with self-down logic.

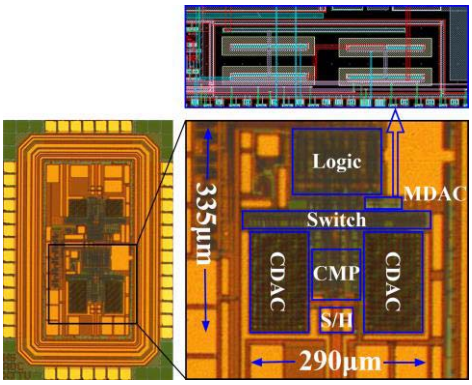

Fig. 14. Chip micrograph.

two inputs. Then, the Valid signal is pulled high to enable the asynchronous clock signal, and the RS latch holds the results for sampling until the next comparison. The self-down logic is used to generate the Trig signal which turns off the comparator before the falling edge of CKC comes. Therefore, unnecessary power consumption of the comparator can be avoided. Monte-Carlo simulation results show a 3-σ offset of 9.4 mV for the comparator, decreasing the SNR by 0.068dB. This fixed offset doesn't influence the linearity of the ADC.

IV. Measurement Results

The proposed ADC is implemented in a 1P6M 0.18-μm CMOS process with a small active area of 0.097 mm^2, as shown in Fig. 14. The MDAC occupies only very small area compared to other circuit blocks. A 0.6-V supply voltage is provided externally for measurement of the chip. The reference voltage is also set to 0.6-V to enable rail-to-rail sampling, resulting in an ideal full-scale input range of $1.2V_{p-p}$. The maximum sampling rate is 200 kS/s.

Fig. 15 plots the measured DNL and INL of the proposed DAC at sampling rate of 200 kS/s, showing peak DNL and INL of $+0.27/-0$. 21 LSB and $+0.43/-0.45$ LSB, respectively. The measured FFT spectrum for a 99-kHz sinusoid input under 200-kS/s sampling rate is given in Fig. 16. The calculated signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 56.91 dB and 68.56 dB, respectively. Fig. 17 shows the measured SFDR and SNDR versus the input frequency at 200-kS/s sampling rate and 0.6-V supply voltage. At a low input frequency, the measured SNDR

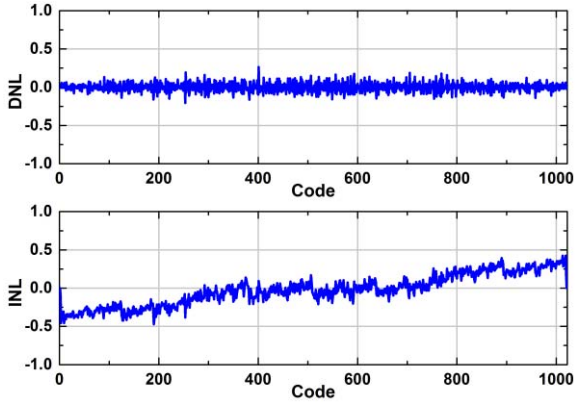

Fig. 15. Measured DNL and INL at 200 kS/s.

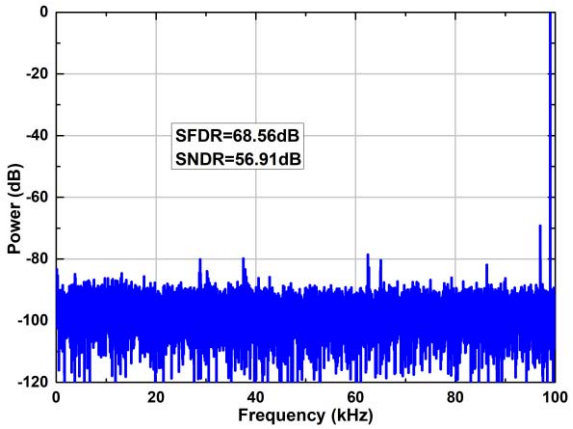

Fig. 16. Measured spectrum for a 99-kHz sinusoid input at 200-kS/s sampling rate.

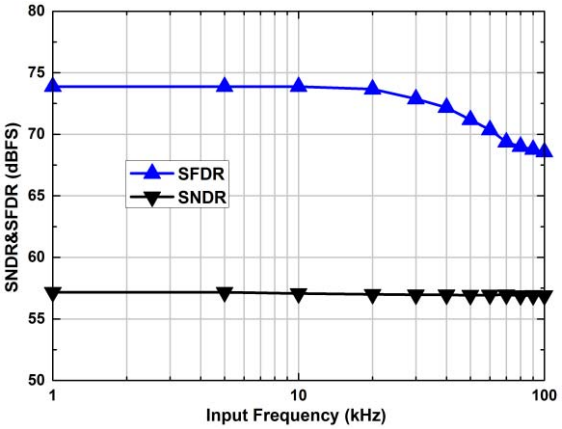

Fig. 17. Dynamic performance versus input frequency at 200kS/s.

and SFDR have higher values of 57.16 dB and 73.87 dB, respectively.

Fig. 18 plots the measured power consumption versus the input frequency with sampling rate of 200kS/s. The power consumption increases slightly with the input frequency. With a 10-kHz sinusoid input at a sampling rate of 200 kS/s, the power consumption of ADC is 1.76 μW. The power consumption breakdown is given in Fig. 19, showing that the

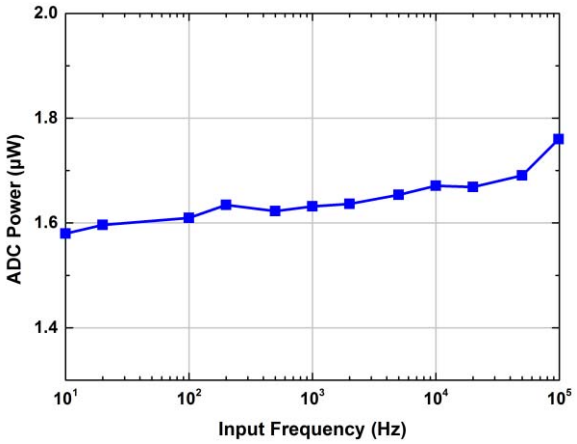

Fig. 18. ADC power consumption versus input frequency at 200 kS/s with 0.6-V supply.

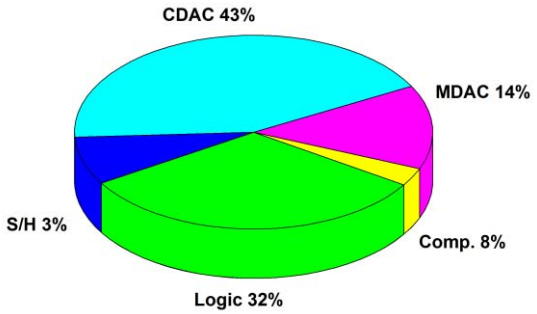

Fig. 19. Power consumption breakdown.

CDAC, MDAC, control logic, comparator and the bootstrapped sampler account for 43%, 14%, 32%, 8%, and 3% of the total power consumption, respectively.

The figure of merit (FoM) is calculated with the popular definition of

$$\text{FoM} = \frac{\text{power}}{2^{\text{ENOB}} \cdot f_{\text{sample}}} \tag{30}$$

From (29), a FoM of 15.38 fJ/conv.-step is obtained for the proposed ADC. Fig. 20 shows the dynamic range of the measured ADC. Fig. 21 plots the conversion energy of recent reported ADCs as a function of the SNDR [32], showing that the proposed work achieves good energy efficiency compared with other similar works.

The performance of the proposed ADC is summarized in Table III with comparison to other prior arts of low-power SAR ADCs. The FoM of the proposed ADC is better than those in [5]–[7], [19], and [34], mainly owing to the optimized hybrid CAP-MOS DAC. Besides, the proposed work achieves better linearity performance in terms of DNL than most of the works in Table III except for [33]. Moreover, thanks to the hybrid CAP-MOS DAC architecture, the proposed ADC consumes smaller chip area than most of the ADCs in Table III except for the ADC with more advanced technologies in [6] and [14].

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	TCAS-I'16 [5]	TCAS-I'15 [6]	TCAS-I'15 [7]	JSSC'17 [14]	ESSCIRC' 16 [19]	ISSCC'14 [33]	ISSCC'11 [34]	**This work**
Tech. (nm)	180	130	130	65	180	180	65	180
Supply Voltage (V)	0.6	0.8	1/0.5	0.7	1	1	0.55	0.6
Resolution (bits)	10	10	10	11	11	10	10	10
Sample rate (kS/s)	200	1000	1100	100	1000	450	20	200
Unit Cap. (fF)	28	80	30	2	2	72	65	31.1
Input Cap. (pF)	14	---	6.9	1.06	1.04	2.3	2.08	3.98
DNL (LSB)	0.29	0.56	0.8	1.04	0.85	0.1	0.58	0.27
INL (LSB)	0.8	0.61	1.6	1.57	0.91	0.2	0.57	0. 45
SFDR (dB) @Nyq.	72.3	---	60.8	67	63.4	80.8	68.8	68.56
SNDR (dB) @Nyq.	57.9	54.5	54.6	64.5	76.6	60.4	55	56.91
ENOB (bits) @Nyq.	9.3	8.8	8.8	10.5	10.3	9.82	8.84	9.16
Power (μW)	2.01	1.76	15.6	0.6	24	3.7~13	0.206	1.76
FoM (fJ/conv.-step)	15.51	20	31.8	4.5	19.9	9.1~35	22.4	15.38
Active area (mm^2)	0.154	0.056	0.87	0.03	0.1	0.12	0.212	0.097

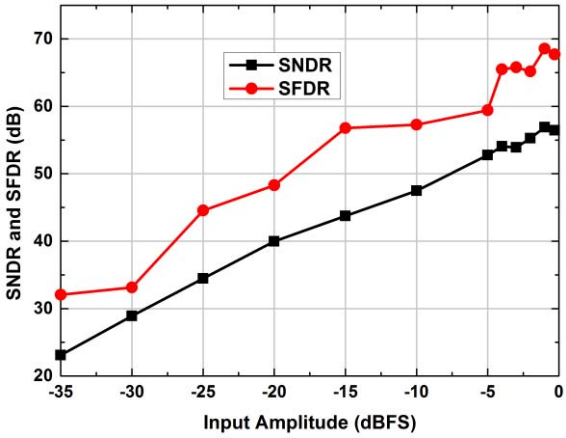

Fig. 20. Measured SNDR and SFDR varying with input amplitude.

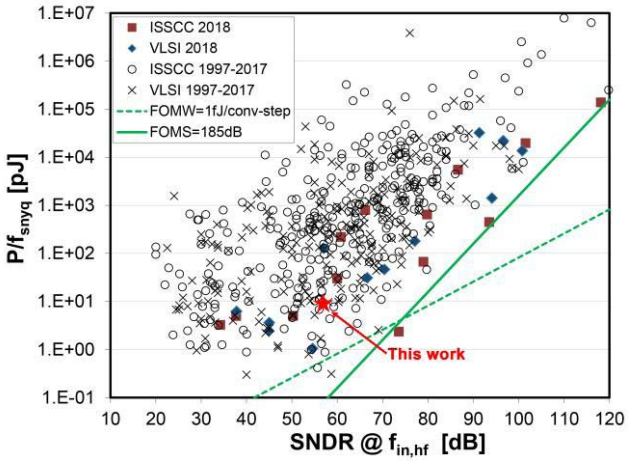

Fig. 21. ADC conversion energy (reported at the ISSCC and VLSI Symposium) as a function of SNDR.

V. CONCLUSION

A fully differential 0.6-V, 200-kS/s 10-bit SAR ADC with a hybrid CAP-MOS DAC has been presented in this work, which reduces both power consumption and the chip area compared with a pure 10-bit CDAC. The 3-bit MDAC is realized by a MOS string with 4 native MOS to control 2 unit capacitors, which allows larger voltage drop on each unit MOS and more reliable operation for MDAC. The prototype 10-bit SAR ADC is implemented in a 0.18-μm CMOS technology, showing an SNDR/SFDR of 56.91 dB/68.56 dB at 99-kHz input under a 0.6-V power-supply, while consuming 1.76 μW at 200 kS/s for a FoM of 15.38 fJ/conv.-step. The proposed ADC is suitable for energy limited applications such as implantable bio-medical devices and sensing systems.

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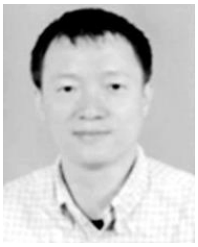
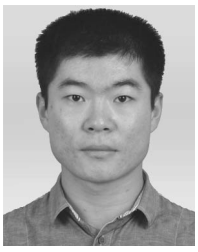
Hongshuai Zhang received the B.S. degree in microelectronics engineering from Xi'an Jiaotong University, Xi'an, China, where he is currently pursuing the M.S. degree in microelectronics.

His research interest includes mixed-signal integrated circuits design, especially in SAR and delta-sigma ADC. He was a Visiting Student with National Chiao Tung University, Taiwan, in 2014. He has received the 2015 and 2017 First Prize in the IC design Contest held by the Beijing Electronics Association, China.



Hong Zhang (M'14) received the B.S. degree in electronic engineering from the Xi'an University of Technology in 2000 and the Ph.D. degree in electronic engineering from Xi'an Jiaotong University, Xi'an, China, in 2008.

In 2009, he was a Visiting Scholar with KU Leuven and IMEC, Belgium. From 2016 to 2017, he was a Visiting Professor with the Department of the Electrical and Computer Engineering, University of Toronto. Since 2008, he has been with the Department of Microelectronics, Xi'an Jiaotong University, where he is currently an Associate Professor. His research interests include high speed ADC and low power biomedical IC design.



Yan Song (S'17) received the B.Sc. and Ph.D. degrees in microelectronics from Xi'an Jiaotong University, Xi'an, China, in 2011 and 2018, respectively.

From 2015 to 2016, he was a Visiting Student with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, where he is currently a Research Assistant with the State Key Laboratory of Analog and Mixed-signal VLSI. His research interests include the low-voltage low-power SAR ADCs, high-resolution wide-bandwidth SAR ADCs, and pipelined-SAR ADCs.

Ruizhi Zhang received the B.S., M.S., and Ph.D. degrees from the Department of Electronic Engineering, Xi'an Jiaotong University, China, in 1982, 1987, and 1995, respectively.

From 1982 to 1984, he was with the Semiconductor Research Center, Ministry of Electronic Industry, China, where he was involved in the design and fabrication of MOSFET. Since 1988, he has been with the Department of Microelectronics, Xi'an Jiaotong University, where he is currently a Professor. His current research focuses on the design of low-power analog CMOS IC. He was also a recipient of several awards from the Ministry of Science and Technology and the Ministry of Education, China, from 1996 to 2005. He has served as the Chair of the Department of Microelectronics, Xi'an Jiaotong University, from 2000 to 2015.