A Subpicosecond Jitter PLL for Clock Generation in 0.12-μm Digital CMOS

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***Abstract*—A fully integrated subpicosecond jitter phase-locked loop (PLL)-based frequency synthesizer in a standard digital 0.12-μm CMOS technology with 1.5-V supply is presented. Two differentially tuned *LC*-VCOs are implemented to support different standards for serial data transmission. A fully differential charge pump and an active loop filter are used for reduction of charge-pump current mismatch. Operating with a 311-MHz reference clock, the PLL achieves typically 860-fs integrated jitter, and a phase noise of −115 dBc/Hz at 1-MHz offset, on a 2.488-GHz output. The power consumption is 35 mW, and the area is 0.7 mm^2.**

***Index Terms*—Clock generation, frequency synthesizer, jitter, *LC*-VCO, phase-locked loop (PLL), phase noise, wideband PLL.**

I. Introduction

A CLOCK with very low integrated jitter is a prerequisite for high-speed transceiver circuits or sampling applications using high-performance analog-to-digital (ADCs) or digital-to-analog converters (DACs). In this brief, we present the concept and design of a subpicosecond jitter phase-locked loop (PLL) for clock generation. We focus on the most important design issues relevant for optimum jitter performance. High-level phase-noise model simulations reveal the main contributors to output clock jitter. A test chip was fabricated and measurement results are presented.

II. Concept and Implementation

Fig. 1 shows the block diagram of the test chip implementation. The module is a classical integer-N charge-pump PLL topology and is fully integrated. To minimize supply and substrate noise injection, all clock and analog signal paths are differential, although drawn single-ended in the block diagram for simplicity. The input clock is designed to operate at 311 or 622 MHz. For the latter frequency, a 2:1 input divider can be used to get a fixed phase detector frequency of 311 MHz. The input frequency is chosen as high as possible to allow the use of very high PLL bandwidths, resulting in minimum jitter for low-noise input clock sources. The bandwidth is selectable by trimming the charge-pump current and loop filter resistor. The PLL output clock can be selected by a current mode logic (CML) multiplexer, choosing either the 2.488 or the 3.11 GHz voltage-controlled oscillator (VCO) or the bypass clock. A final CML buffer provides the chip-internal clock output. After the first 2:1 CML divider stage of the feedback clock path, a second half-rate clock output is provided. To close the feedback path, two additional CML-type dual-modulus dividers (DMD) are inserted, each providing two possible division rates of 4 or 5, with bypass option for the second divider. The second DMD enables production test with lower reference clock frequency.

The basic structure for all CML blocks is an nMOS differential pair with resistive load. The CML dividers have been designed for a nominal output voltage swing of 300-mV peak to peak. The current consumption of the first 2:1 CML prescaler is 600 μA, plus 600 μA for a buffer driving the following stages. A CML test multiplexer with simple current steering pseudo-emitter-coupled logic (PECL) output structure using external pull-up resistors is implemented. Such a differential low-swing interface is essential for enabling low-jitter high-frequency measurements. Bias currents are derived from a bandgap voltage reference circuit. The poly resistor in the bandgap used to generate the reference current is of the same type as the CML load resistors, therefore canceling first-order deviations in CML signal swing over process and temperature.

The phase/frequency detector (PFD) uses the three-state output architecture [1]. In order to reduce noise coupling on the Up and Down output pulses, a fully differential topology has been chosen. The Up and Down signals are rail to rail in order to drive the charge pump fully into ON or OFF state, avoiding leakage currents in the switches.

Particular attention was paid to the charge pump (CHP). Indeed, mismatch errors of the Up and Down current pulses at the output of the charge pump lead to unwanted spurious tones at the output clock of the synthesizer. The differential CHP architecture (Fig. 2) is made out of two identical units, each of which is connected to one of the loop filter (LF) inputs (*Lfp, Lfn*).

A nonoptimum biasing of the input nodes of the loop filter causes current mismatches between Up and Down currents in one unit, due to the finite output resistance of the current sources P3 and N3. A similar CHP structure was shown in [2], where it was combined with a passive loop filter. In our design, we combine the differential CHP with an active loop filter as proposed in [3]. In this way, we assure that the two differential input voltages of the loop filter (*Lfp, Lfn*) keep very close together and close to the common-mode voltage *Lfcm*, independent of the differential output voltage of the loop filter. The voltage *Lfcm* is set equal to a reference voltage *Ref* by a control loop, comprising amplifier A1 and transistors P3. Any mismatch between the currents of P3 and N3 in one unit would cause the voltage of *Lfcm* to drift from the reference value *Ref*. As this is prevented by the control loop, an excellent match of the Up and Down currents is achieved. The reference voltage *Ref* has to be chosen taking care of the correct operation of the active loop filter and of the current sources in the charge pump.

The LF resistor adding the zero in the transfer function has been made programmable from 8 to 48 kΩ by bypassing portions of the resistor with transmission gates, thus allowing changes in the PLL bandwidth. To ensure stability, the unity

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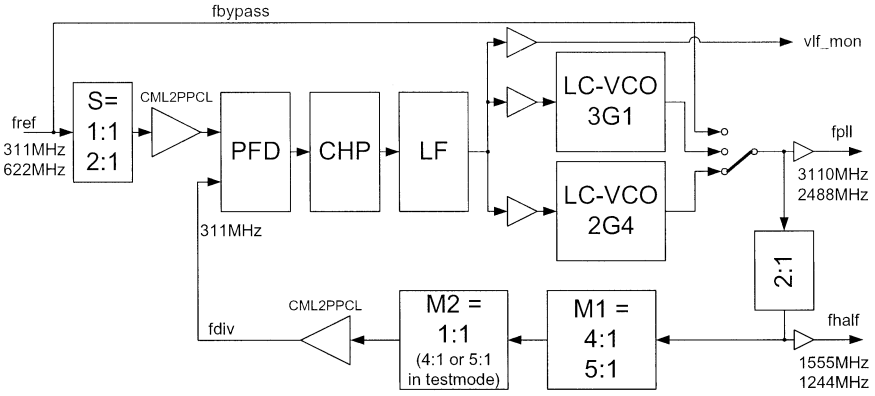

Fig. 1. PLL block diagram.

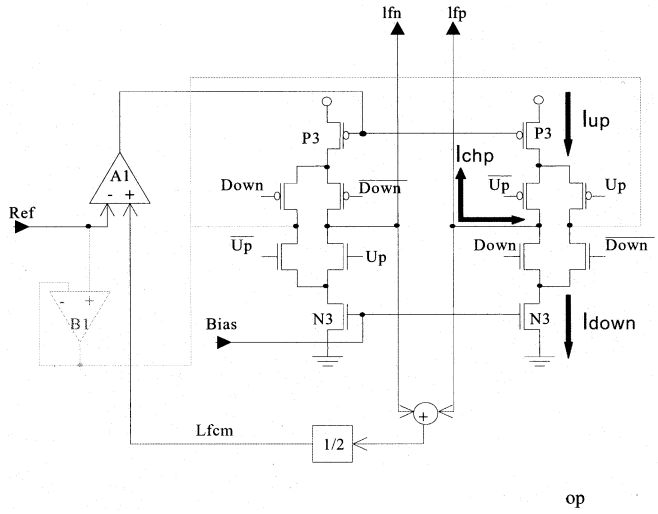

Fig. 2. Charge pump with common-mode control loop.

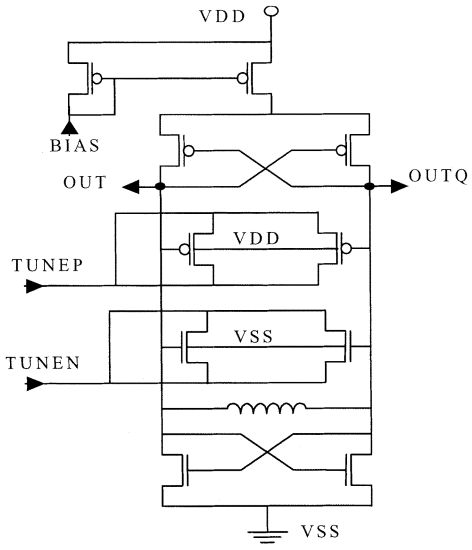

Fig. 3. Differentially tuned *LC*-VCO structure.

gain frequency F_u of the operational amplifier must be somewhat greater than the bandwidth of the PLL. In this PLL, the F_u was designed to be 100 MHz nominal. Due to the relatively small LF capacitance of 13 pF, the loop filter noise (in combination with charge-pump noise) is the dominating noise source for large loop bandwidth, as can be seen later in the phase-noise simulations.

For its good characteristics with respect to low phase noise and power, an *LC*-VCO (see Fig. 3) was chosen as the core oscillator [5]. This PLL will be able to provide either 2.488 or 3.11 GHz output frequency. Using a single VCO, this would require a center frequency of 2.8 GHz and a frequency range of at minimum 22%, in a practical implementation even more to account for process, voltage, and temperature (PVT) variations. Such a large tuning range is hard to achieve for *LC*-VCOs. Therefore, and to allow dedicated phase-noise optimization for each target frequency, a dual-VCO topology was chosen, at the cost of additional silicon area (0.1 mm^2 for one *LC*-VCO). To avoid unwanted cross coupling between the VCOs, only one VCO is active at one time. The inductance of the integrated coils is equal to 5.6 and 3.97 nH for the 2.488 and the 3.11 GHz VCOs, respectively. The quality factor (Q) of the *LC* tanks is dominated by the Q factor of the inductors. A characterization of the coils with S parameters results in a maximum Q3 dB of 8. Each of the VCOs has a current consumption of 3 mA. The VCO varactor represents quite a large capacitive load to the output of the loop filter. Since two VCOs are used in this design, the capacitive load is even doubled when compared to a single-VCO PLL design. Therefore, a buffer is inserted to avoid a disturbing parasitic pole in the transfer function and to damp the kickback from the VCOs to the loop filter. As can be seen in Fig. 1, a separate buffer is used to monitor the loop filter voltages without fringing the performance on the noise-sensitive VCO input nodes. The VCO input buffer is realized with simple source followers, using a pMOS and a nMOS follower for the positive and negative signal path, respectively.

III. Phase Noise and Jitter Simulations

Fig. 4 shows the simulated phase-noise performance of the PLL using an s domain Matlab model. It can be seen that in the case of a bandwidth programmed to maximum (15 MHz), the noise is not dominated by the VCO. This changes when the PLL is programmed to a lower bandwidth. Then, the VCO noise gives major contributions at a PLL corner frequency below 2 MHz. From the phase-noise simulation, the accumulated jitter graph [5] can be calculated and, furthermore, the

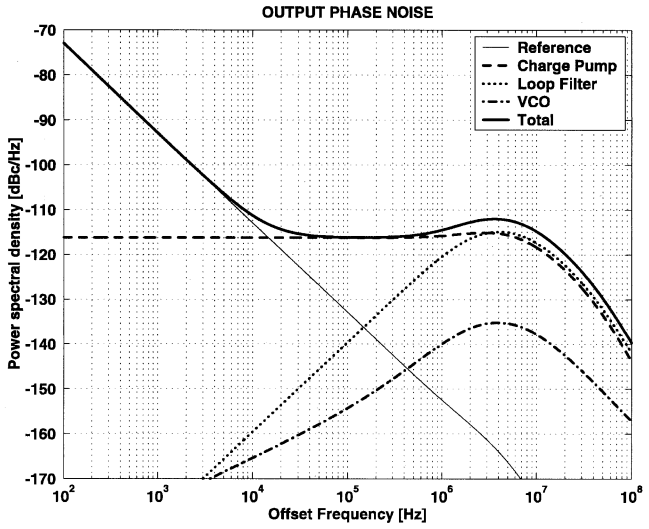

Fig. 4. Simulated phase noise performance over frequency offset. $f_{\mathrm{PLL}} = 2.488$ GHz.

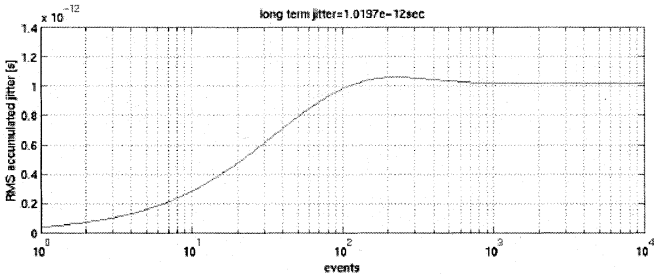

Fig. 5. Simulated accumulated jitter. $f_{\mathrm{PLL}} = 2.488$ GHz.

long-term jitter, which is $\sqrt{2}$ times the integrated jitter [6]. This simulation result is shown in Fig. 5 for typical conditions. Long-term jitter yields 1.02-ps rms, integrated jitter 721-fs rms.

IV. Measurement Results

A test chip was fabricated in a 0.12-μm CMOS technology, using standard digital devices only (regular VT MOS, polysilicon resistors, sandwich capacitors). Fig. 6 shows a layout plot of the PLL module, which occupies an area of 0.7 mm^2. Fig. 7 shows, in the upper graph, the phase-noise performance on the 2.488-GHz clock at the PECL outputs. For comparison, the lower graph shows the phase noise of the input reference clock of 311 MHz, which is derived from a low-noise sine-wave generator and a transformer to get a differential input clock. The output clock is made single-ended by using another transformer and then fed to the spectrum analyzer. The PLL phase noise is -115 dBc/Hz at 1-MHz offset from carrier. The integrated jitter over the measured band (100 Hz–100 MHz) is 860 fs for typical conditions. Over temperature (-25° to $+125^\circ$) and supply variation ($\pm 10\%$), this value varies from 633 fs to 1.36 ps for one sample. There is very good match between simulations and measurement. In the 2.488-GHz graph, one can see that for low offsets up to 2 kHz the noise is equal to the upconverted input noise ($20\log_{10}(8) = 18$ dB higher). In midrange, the phase noise gets flat, thus showing the in-band PLL phase-noise performance. The PLL bandwidth can be identified around 15 MHz. On the 311-MHz clock, the noise floor of the used PSA E4440A spectrum analyzer limits the measured noise from 2 kHz upward. So the real phase-noise performance of the input clock for higher offsets is better than the measured graph. The only spurious seen in a peak spectrum plot during locked condition is at 311-MHz offset with -65 dBc from the 2.488-GHz carrier. A summary of the PLL performance is shown in Table I.

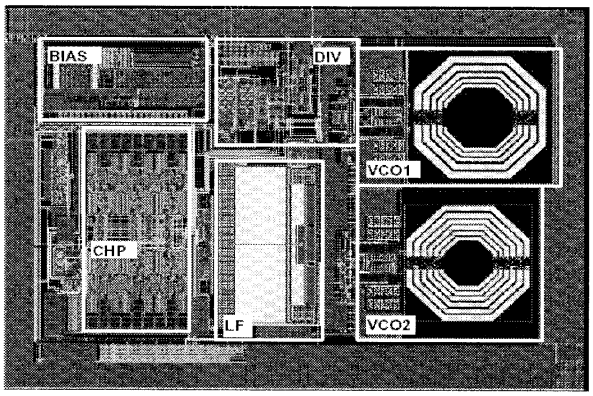

Fig. 6. Layout plot.

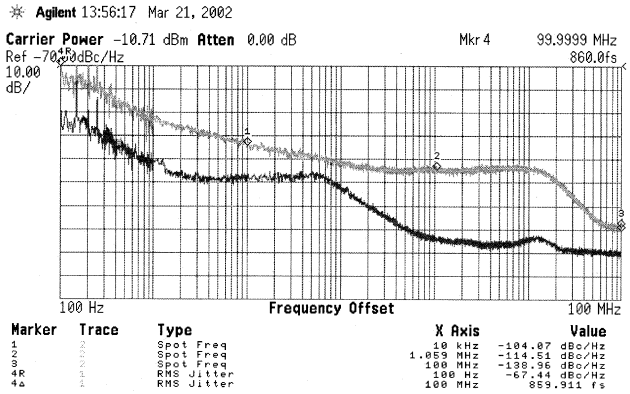

Fig. 7. Phase noise performance. Upper graph: 2.488 GHz; lower graph: 311 MHz input reference.

TABLE I
PLL Performance Summary

LC VCO frequency:	2.488GHz	3.11GHz
Loop divider:	8	10
Phase noise @1MHz offset:	-115dBc/Hz	-113dBc/Hz
RMS Integrated jitter (100Hz-100MHz) (-25 to 125°C, ±10% supply):	typ. 860fsec, 633fsec to 1.36psec w.c.	
Spurious performance	< -65dBc	
PLL Bandwidth	1-15MHz programmable	
LC-VCO tuning range:	±10%	
Input frequency:	311MHz	
Supply Voltage:	1.3 to 1.7V	
Module Area (without pads):	0.7mm²	
LC-VCO Power:	4.5mW	
Total Power:	35mW (45mW including PECL off-chip driver)	

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