A Slew-Rate Controlled Output Driver Using PLL as Compensation Circuit

Soon-Kyun Shin, Seok-Min Jung, Jin-Ho Seo, *Member, IEEE*, Myeong-Lyong Ko, and Jae-Whui Kim

***Abstract*—A slew-rate controlled output driver adopting the delay compensation method has been implemented using 0.18-μm CMOS process for storage device interface. A phase-locked loop (PLL) is used to generate compensation current and constant delay time. The compensation current reduces the slew-rate variation over process, voltage, and temperature variation of the output driver. The constant delay time, which is generated by the replica of the voltage-controlled oscillator in the PLL, reduces the slew-rate variation over load capacitance variation. Such an output driver has 25% less variation at slew rate than that of the conventional output driver. The proposed output driver is able to meet UDMA100 interface that specifies load capacitance ranging from 15 to 40 pF and slew rate from 0.4 to 1.0 V/ns.**

***Index Terms*—CMOS, output driver, phase-locked loop (PLL), process, voltage, and temperature (PVT) compensation, slew-rate control, voltage-controlled oscillator (VCO).**

I. Introduction

THE speed of modern storage interfaces has rapidly increased up to 100 MB/s. With this increased speed, the vulnerability of the original ATA cabling scheme has become apparent on desktop systems. Ringing caused by improper termination, crosstalk between signals, and bus timing on the bus are elements that must be considered by the system manufacturers, chipset designers, and disk-drive manufacturers. UDMA100 is the specification of ATA/ATAPI-6, which specifies the interface between storage device and PC [1]. The ATA specification has changed from UDMA33, UDMA66, to UDMA100 using 16-bit data lines. Each of the specifications is shown in Table I. With increasing data rate and signal frequency, crosstalk of transmission lines has emerged. The problem can be solved by means of a new cable and the lowered slew rate that reduces noise but is unable to go lower than a certain value because of timing margin. During the change from UDMA33 to UDMA66, the cable is changed from 40 to 80 conductors that have additional ground lines. It reduces crosstalk and increases signal integrity. UDMA100 slew-rate specification is tighter than UDMA66 over a wide range of load conditions. UDMA100 interface uses the same cable as UDMA66, but the specification of the load range is changed from 40 pF to 15 $\sim$ 40 pF and that of the slew rate is changed from maximum 1.25 V/ns to 0.4 $\sim$ 1.0 V/ns, respectively.

TABLE I
SLEW-RATE SPECIFICATION OF ATA INTERFACE

ATA MODE	Signal frequency	Slew rate Specification
UDMA33	8.25 MHz	Min tr, tf 5ns
UDMA66	16.5 MHz	Max. 1.25[V/ns]
UDMA100	25 MHz	0.4 ~ 1.0 [V/ns]

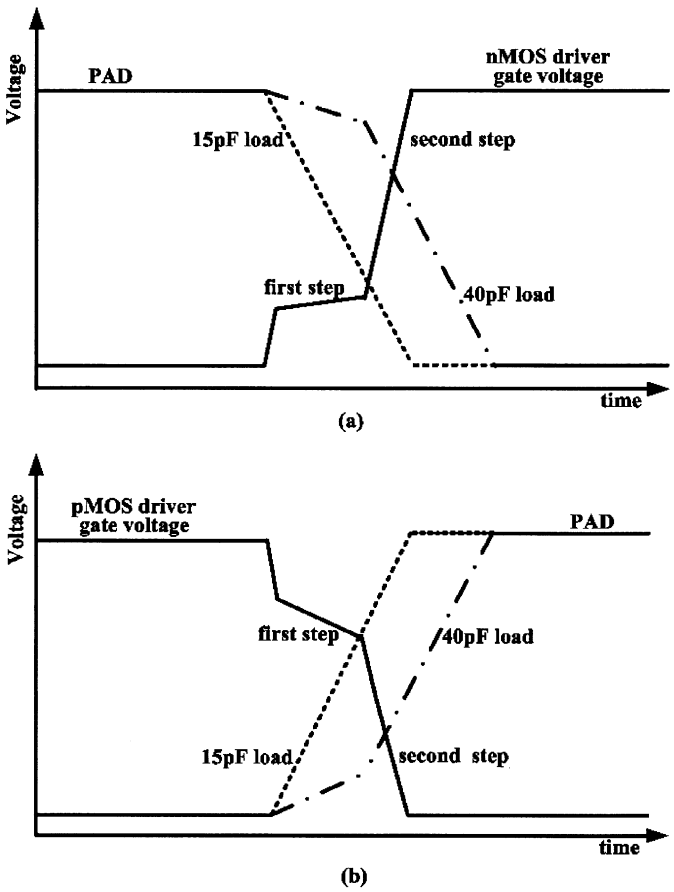

Fig. 1. Simplified PAD waveforms and gate voltage. (a) When PAD falls. (b) When PAD rises.

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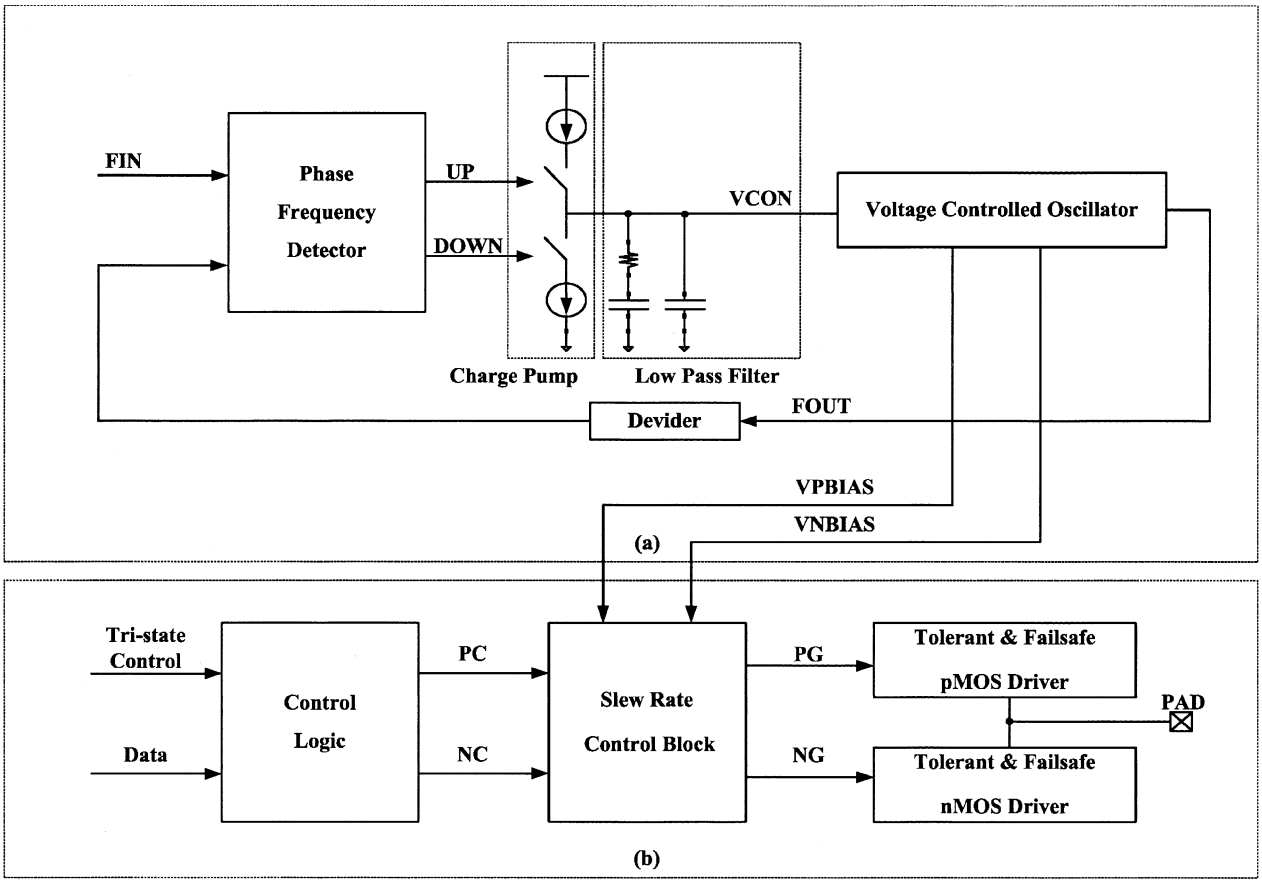

Fig. 2. Simplified block diagram of new output driver. (a) PLL. (b) Output driver.

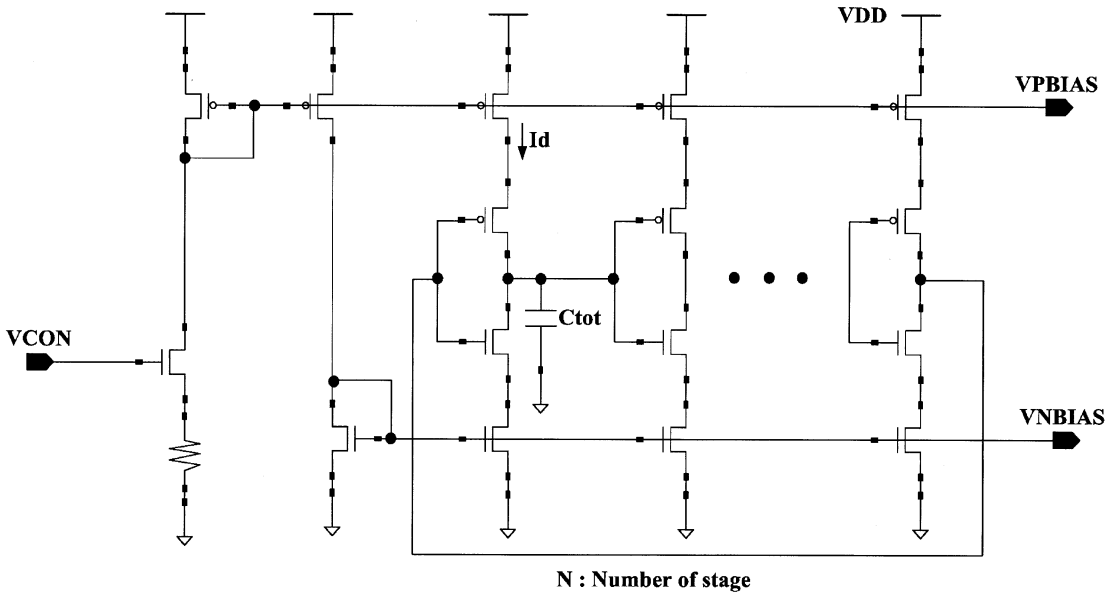

Fig. 3. VCO.

That means the maximum load is 2.67 times larger than its minimum while the slew-rate maximum is 2.5 times larger than its minimum. The conventional output driver is unavailable because the characteristic of slew rate changes in proportion to the load capacitance. To meet this specification, two compensation circuits for load capacitance and process, voltage, and temperature (PVT) variation are required.

Various compensation architectures have been previously reported for PVT variation [2]–[8], and most of them use external resistors to generate a bias current. Feedback architecture has

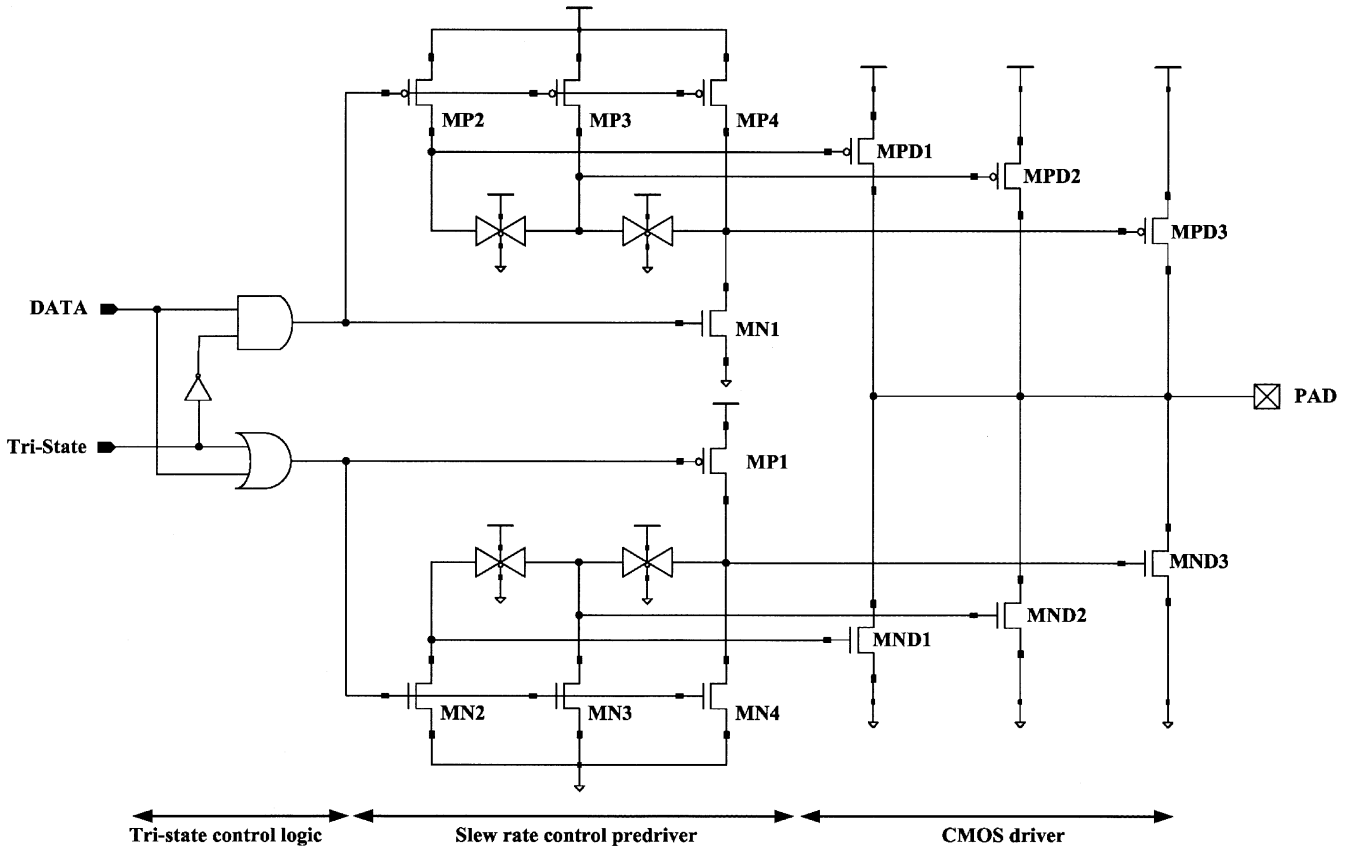

Fig. 4. Schematic of conventional slew-rate controlled output driver.

been used for a wide range of load capacitance variation [9], but it is useless in such a fast slew rate.

Accordingly, it is suggested in this paper that a slew-rate controlled output driver is desirable in that it has more tolerance to PVT and load variation than the conventional output drivers.

II. Circuit Design

The important design of UDMA100 I/O is the slew-rate control of output driver. An output driver that does not adopt a compensation circuit is unable to satisfy the UDMA100 slew-rate specification because of the large variation of slew rate over the variation of PVT and load capacitance.

A compensation circuit using a phase-locked loop (PLL) is adopted to generate constant delay and compensation current over the PVT variation. The circuit controls the gate voltage of output CMOS driver by increasing or decreasing the voltage slope in two steps, which results in small slew-rate variation over wide load variation. Fig. 1 shows the concept in detail. If the load capacitance is small, the transition of the output driver is already completed before the gate control voltage goes to second slope. So the second voltage slope of the gate does not affect the slew rate. If the load capacitance is large, the first voltage slope of the gate is too low to meet the slew-rate specification. Because of that, the second voltage slope of gate is able to increase the slew rate after a delay time from the first voltage slope of the gate. The interval time can be estimated through the transition time simulation of the first voltage slope over PVT variation.

A. Compensation Current and Constant Delay Generation Using PLL

Since the delay time of the conventional delay circuit varies too much over PVT corners to meet the UDMA100 slew-rate specification, a PLL is adopted to generate the constant delay time over PVT corners. A characteristic of PLLs is the constant clock frequency over PVT corners when the PLL is locked. Constant clock frequency means that the period of the clock is constant, in other words, constant delay time at each inverter stage of the voltage-controlled oscillator (VCO). The VCON control voltage of the VCO, shown in Fig. 3, generates the bias voltage in the VCO block to make a certain frequency. The bias voltage is used as compensation voltage of slew rate in the output driver. In Fig. 2, it is shown that the PLL provides the output driver with bias voltage for compensation. The voltage of VPBIAS and VNBIAS that come from the VCO is supplied to the slew-rate control block in the output driver.

The VCO's oscillation frequency is

$$f_{\rm osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_d}{NC_{\rm tot}V_{DD}} \tag{1}$$

where t_1 and t_2 are charge and discharge time, respectively, N is the number of delay stages, $C_{\rm tot}$ is the total capacitance at each stage, I_d is bias current, and V_{DD} is supply voltage [10]. If V_{DD} is constant and the PLL is locked, I_d is a constant current over process and temperature corners.

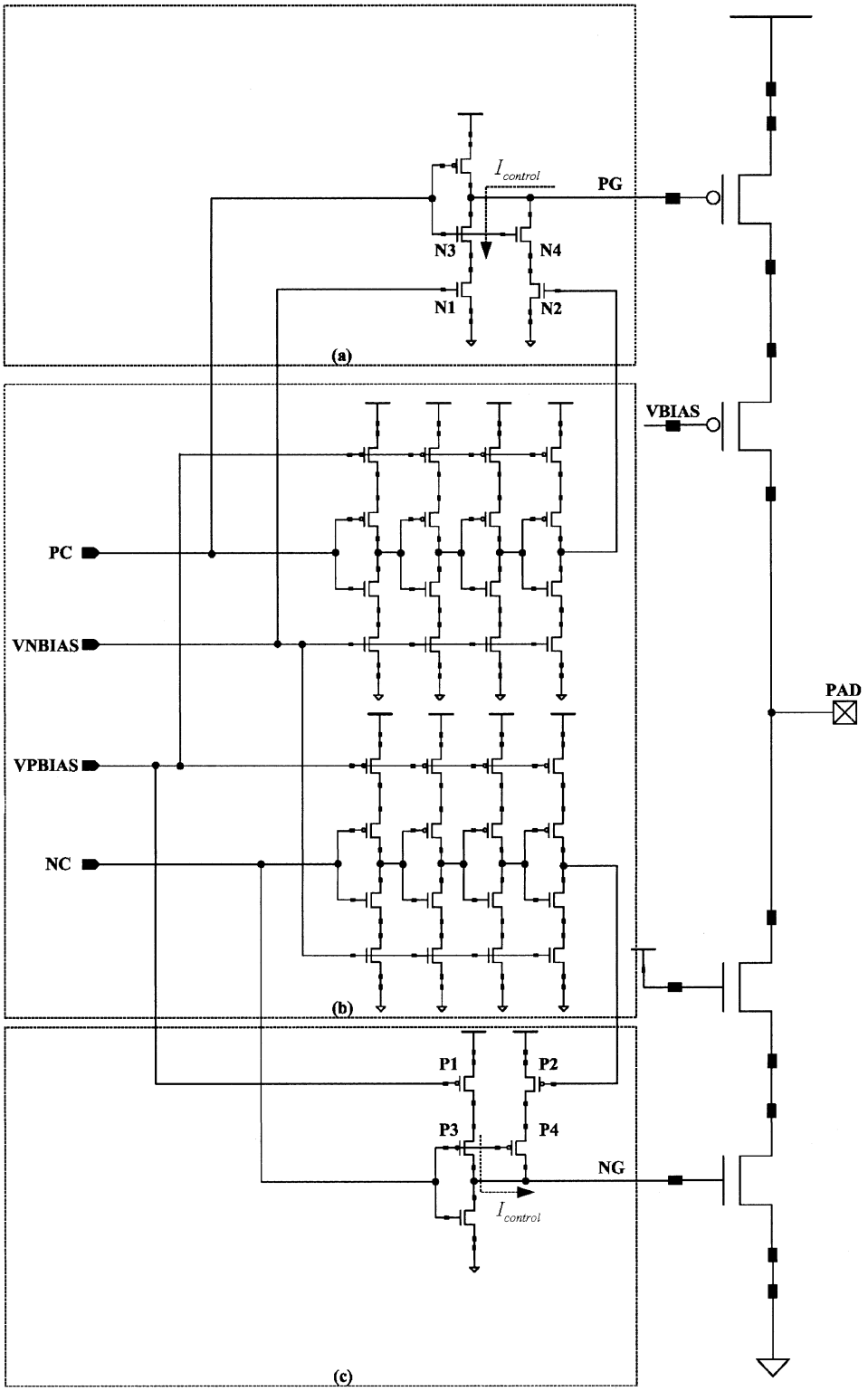

Fig. 5. Simplified schematic of slew-rate control block. (a) PMOS driver gate voltage control block. (b) Delay block (replica of VCO). (c) NMOS driver gate voltage control block.

Regardless of all variation of PVT, the PLL is locked after a certain time and the frequency of the VCO is constant. So the delay stage of VCO produces constant delay time. The output driver uses the replica at the delay stage of VCO as shown in Fig. 4. After the PLL is locked, bias voltages of VCO (VPBIAS and VNBIAS) are generated, and the slew-rate control block of the output driver utilizes the voltage. Then, the input frequency of the PLL (FIN) must have a constant frequency regardless of any clock used in the whole chip. In this paper, 100 MHz was used as FIN while PLL consisted of FOUT so as to generate 30 MHz.

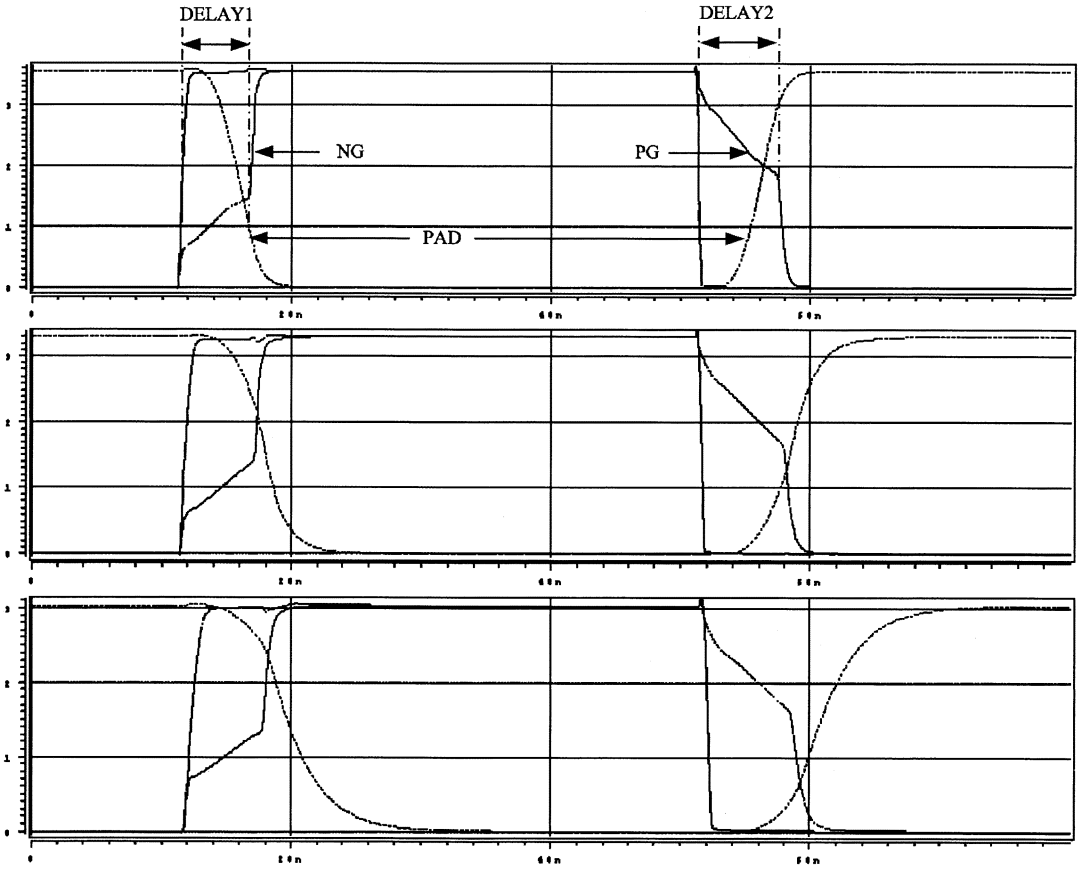

Fig. 6. Corner simulation results. (a) Process fast, $V_{DD} = 3.564$ V, temperature $-40\,^{\circ}$C, load 15 pF. (b) Process typical, $V_{DD} = 3.3$ V, temperature $25\,^{\circ}$C, load 27 pF. (c) Process slow, $V_{DD} = 3.036$ V, temperature $125\,^{\circ}$C, load 40 pF.

B. Slew-Rate Control Block in Output Driver

Fig. 4 shows the conventional slew-rate controlled output driver. MND1, MND2, MND3, MPD1, MPD2, and MPD3 of the CMOS drivers were divided into three pieces for simultaneous switching output (SSO) noise reduction and slew-rate control. MP2, MP3, MP4, MN2, MN3, and MN4 were used to turn off the CMOS drivers quickly while the transmission gate was used as a resistive element to turn each individual CMOS driver on separately. MP1 and MN1 were used to control the CMOS driver to turn it on [2].

A major difference between such a proposed slew-rate controlled output driver and the conventional output driver is that the former uses a compensation circuit so as to make a small slew-rate variation against PVT and load variation.

Fig. 2 shows the proposed output driver that consists of control logic block, slew-rate control block, and the output of pMOS and nMOS with tolerant and fail-safe function. The control logic block has the function that controls tri-state. The slew-rate control block controls the gate voltage of the CMOS driver using the compensation voltage of VPBIAS and VNBIAS that come from the PLL. Fig. 5 shows the slew-rate control block and the CMOS driver. In detail, the PC and NC go to the same logic level when the output driver transmits the data signal. If the output driver is in tri-state mode, the PC is high and NC is low state. The delay block generates constant delay time over PVT corners when the PLL is locked because the MOS size and structure is the replica of the VCO. P1 and N1 have the same length and bias voltage of the VCO's bias MOS. The only difference is the width. Therefore, it operates as a current mirror.

The current equation in the output driver when the PLL is locked is

$$I_{\text{control}} = K \times I_d = K\frac{NC_{\text{tot}}V_{DD}}{f_{\text{osc}}} \tag{2}$$

where K is the ratio factor of the current mirror, N is the number of inverter stages, C_{tot} is the total capacitance of the inverter stage, V_{DD} is the power supply voltage, and f_{osc} is the frequency when the PLL is locked.

The dominant factor of I_{control} is V_{DD}. The variation of process and temperature does not change the current because K and C_{tot} are physical factors, and f_{osc} is a constant value when the PLL is locked. The current issues the constant current source that generates the waveforms, which are DELAY1 and DELAY2 at the first voltage slope of NG and PG in Fig. 6. The first voltage slope can satisfy the slew-rate specification in the 15-pF load condition and the second voltage slope can meet the 40-pF load condition. The start time of the second voltage slope can be determined through transition time simulation over PVT corner in the 15-pF load condition.

When output PAD falls down, both PC and NC also go down and NG rises. At this time, PG rises rapidly to turn the pMOS driver off, and P1 connected by NC supplies the constant current to NG. So NG rises with constant slope. After NC goes down, P2 is turned on in a certain delay time by the delay block. P2 determines the second rising slope.

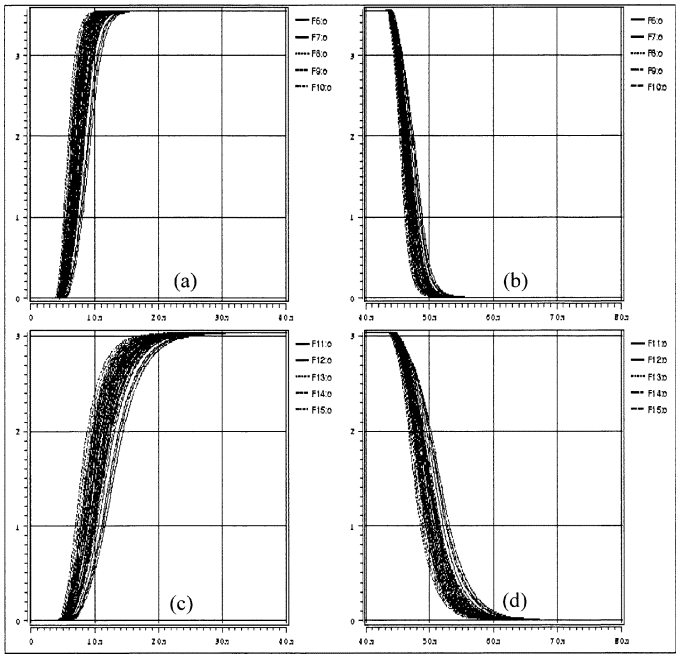

Fig. 7. Conventional output driver simulation results. (a), (b) Process slow, typical, fast, $V_{DD} = 3.564$ V, temperature $-40\,^{\circ}$C$\sim$125 $^{\circ}$C, load 15 pF. (c), (d) Process slow, typical, fast, $V_{DD} = 3.036$ V, temperature $-40\,^{\circ}$C$\sim$125 $^{\circ}$C, load 40 pF.

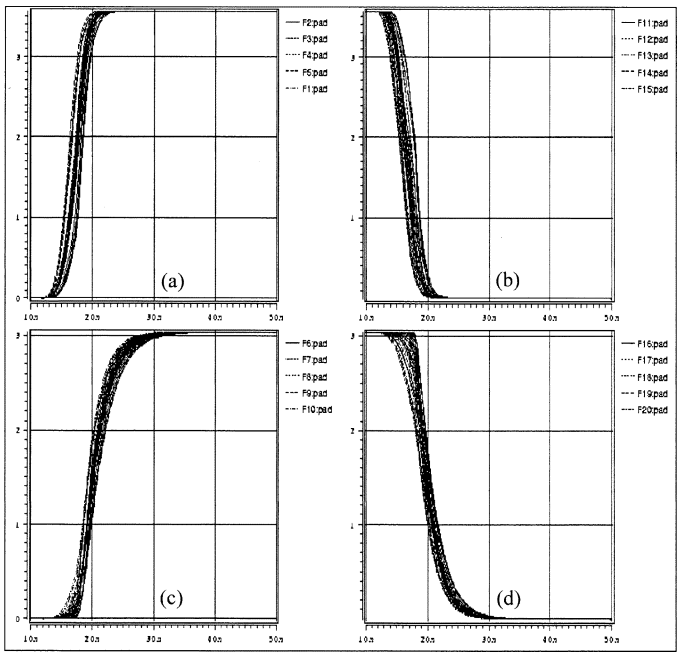

Fig. 8. Proposed output driver simulation results. (a),(b) Process slow, typical, fast, $V_{DD} = 3.564$ V, temperature $-40\,^{\circ}$C$\sim$125 $^{\circ}$C, load 15 pF. (c),(d) Process slow, typical, fast, $V_{DD} = 3.036$ V, temperature $-40\,^{\circ}$C$\sim$125 $^{\circ}$C, load 40 pF.

It can be explained in a similar manner when output PAD rises. Both PC and NC go up and PG goes down. At this time, NG falls down rapidly to turn the nMOS driver off, and N1 connected by PC supplies the constant current to PG. So PG falls down with constant slope. After PC rises, N2 is turned on in a certain delay time by the delay block. N2 determines the second falling slope. P3, P4, N3, and N4 are just used as switches.

TABLE II
SIMULATION RESULTS OF SLEW RATE

Slew rate	Simulation results [V/ns]
UDMA100 Specification	0.4 ~ 1.0
Conventional output driver	0.305 ~ 1.216
Proposed output driver	0.403 ~ 0.986

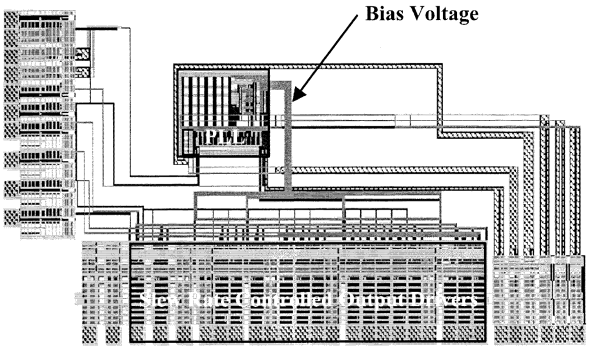

Fig. 9. Layout of test chip.

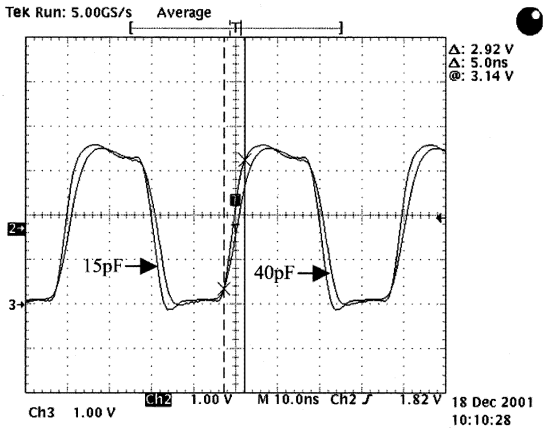

Fig. 10. Measured results of test chip.

III. SIMULATION AND MEASUREMENT RESULTS

HSPICE simulation is carried out using 0.18-μm CMOS SPICE model parameter. Fig. 6 shows the simulation results of slew rate under conditions that are fast, typical, and slow in PVT corner. The delay time of DELAY1 and DELAY2 are constant in spite of PVT variation. Fig. 7 is the simulation result of the conventional output driver and Fig. 8 is that of the proposed new output driver. Compared with Fig. 7, the slew-rate variation in Fig. 8 is smaller than that in Fig. 7. As Table II shows, the new output driver has 23% less variation at minimum slew rate and 25% less variation at maximum slew rate than that of the conventional output driver.

The test chip was implemented in a 0.18-μm one-poly six-metal CMOS technology. The PLL and the output driver were integrated completely, as shown in Fig. 9. Silicon area was 70×401 μm^2 in the output driver and $421 \times 317 \mu$m^2 in the PLL. Fig. 10 shows measured waveforms in the load conditions of 15 and 40 pF. The measured results over all PVT corners meet the UDMA100 specifications.

IV. Conclusion

In this paper, a slew-rate controlled output driver was implemented using a PLL as the bias voltage generation block in 0.18-μm CMOS technology. A constant delay and compensation current over PVT corner were generated by the PLL and used in output driver to minimize the slew-rate variation. The slew-rate variation of the output driver is 25% less than that of the conventional output driver. The proposed output driver is able to meet the UDMA100 specification which specifies the slew rate ranging from 0.4 to 1.0 V/ns at load capacitance range of 15$\sim$ 40 pF.

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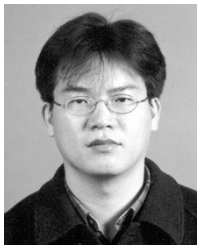

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