An 85 dB DR 4 MHz BW Pipelined Noise-Shaping SAR ADC With 1-2 MASH Structure

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***Abstract*— A pipelined noise-shaping successive approximation register (NS-SAR) ADC with 1-2 multistage noise-shaping (MASH) structure is presented. Two-stage pipelined structure consisting of 5 bit NS-SAR and 4 bit NS-SAR quantizers enables 3rd-order noise-shaping. A single operational transconductance amplifier (OTA) is shared by an integrator for noise-shaping and a residue amplifier for pipelining to maximize the power efficiency. The measured dynamic range (DR) is 84.6 dB when the sampling rate is 83.3 MS/s, bandwidth is 4 MHz, and power consumption is 3.5 mW showing Schreier figure-of-merit ($FoM_{S,DR}$) of 175.2 dB. The proposed ADC structure greatly relaxes design requirement of each SAR quantizer and can achieve high resolution and wide bandwidth with good power efficiency.**

***Index Terms*— $\Delta\Sigma$ analog-to-digital converter (ADC), data converter, multistage noise-shaping (MASH), noise-shaping successive approximation register (NS-SAR) ADC, pipelined SAR ADC.**

I. Introduction

INTERNET of things or narrow-band wireless communication applications require high-performance analog-to-digital converters (ADCs) with bandwidth of at least several MHz, high resolution above 13 bits, and wide dynamic range (DR) above 80 dB. One of promising candidates satisfying those requirements is a $\Delta\Sigma$-ADC, which is widely used in high-resolution applications [1]–[3]. A $\Delta\Sigma$-ADC often adopts high-order noise transfer function (NTF) combined with a low-bit quantizer to avoid complex digital-to-analog converter (DAC) calibration, and the high resolution is achieved by fast sampling rate and high oversampling ratio (OSR). However, this method requires a loop filter consisting of several operational transconductance amplifiers (OTAs) that inevitably lead to high power consumption. To mitigate the power issue, various hybrid ADCs based on a $\Delta\Sigma$-ADC have been introduced. Jiang *et al.* [4] apply time-interleaving extrapolation scheme to a conventional $\Delta\Sigma$-ADC so that the sampling rate becomes quadrupled while making the loop filter requirements relaxed. Although this approach not only reduces the duplicated hardware cost but also achieves higher resolution with a lower-order loop filter, at least two power-hungry OTAs are still necessary for its implementation. Ragab and Sun [5] and Sanyal and Sun [6] minimize the number of OTAs in a $\Delta\Sigma$-ADC effectively by replacing a conventional quantizer with a voltage-controlled oscillator (VCO). The VCO performs both signal integration and quantization, so the 1st-order noise-shaping is acquired at no cost alleviating the loop filter requirement. However, the use of a VCO often limits the achievable ADC resolution due to its nonlinearity [7].

A noise-shaping successive approximation register (NS-SAR) ADC is another hybrid version based on a $\Delta\Sigma$-ADC that significantly mitigates the trade-off between energy efficiency and resolution [8]–[14]. A NS-SAR ADC uses an SAR quantizer that can easily perform multi-bit quantization with low hardware cost and very high energy efficiency compared with a flash quantizer which is often used in conventional $\Delta\Sigma$-ADCs. Therefore, a NS-SAR ADC might not require a power-hungry higher-order loop filter, and even a passive loop filter can be enough if the target resolution is moderately high.

Fig. 1(a) compares the performance of state-of-the-art $\Delta\Sigma$-ADCs and NS-SAR ADCs with >MHz bandwidth. It is observed that NS-SAR ADCs show a better energy efficiency versus SNDR than $\Delta\Sigma$-ADCs. Regardless of the good energy efficiency, most NS-SAR ADCs have not provided high resolution over 80 dB for >MHz bandwidth as shown in Fig. 1(b). This limitation is mainly related to conventional methods of improving the resolution of NS-SAR ADCs, which are categorized by: 1) increase of SAR quantizer resolution and 2) increase of the loop filter order for high-order NTF. The first method lowers the total amount of quantization noise uniformly over the whole frequency region. The inband noise can decrease by 6 dB for every quantization bit number increase. However, the comparator noise should be suppressed together to take the advantage of the increased bit number, and the ADC conversion speed and power consumption become dominated by the comparator if a fine SAR quantizer is to be used. Therefore, most NS-SAR ADCs limit the SAR quantizer resolution below 10 bits [8]–[14] considering power

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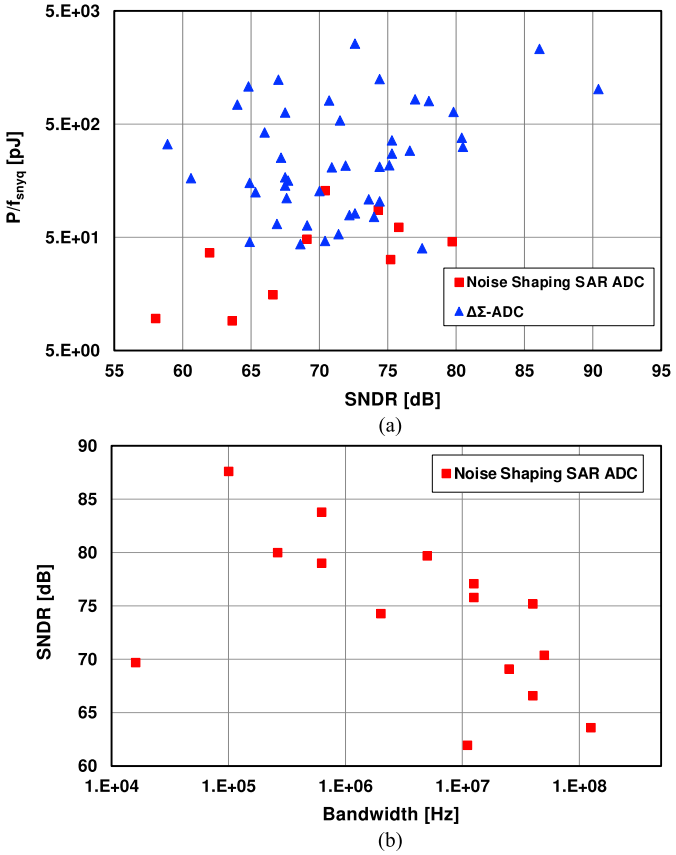

Fig. 1. (a) Energy efficiency (P/fsnyq) versus signal-to-noise-and-distortion-ratio (SNDR) comparison of ΔΣ-ADCs and NS-SAR ADCs with MHz bandwidth and (b) SNDR versus bandwidth for NS-SAR ADCs with MHz bandwidth from 2012 to 2020 ISSCC & VLSI.

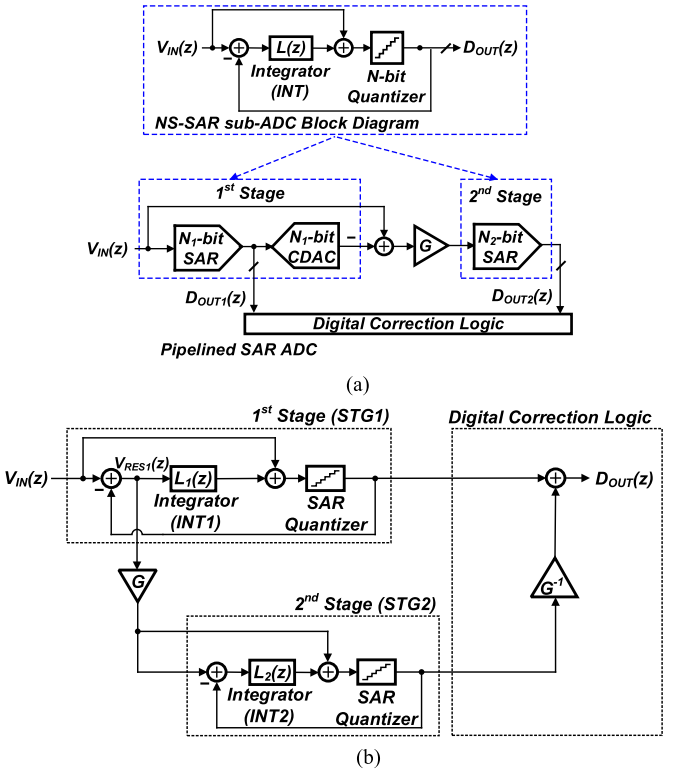

Fig. 2. (a) Concept of pipelined NS-SAR ADC and (b) its block diagram.

and bandwidth. The second method effectively improves the resolution by suppressing the inband noise further, but the loop filter latency for processing residue signal would increase significantly. This not only affects stability but also leads to a lower bandwidth which is often limited to ~kHz [12]–[14].

To overcome the trade-off between accuracy, speed and energy efficiency, a NS-SAR ADC can be combined with a pipelined ADC for a hybrid structure. Song *et al.* [15]–[17] use a NS-SAR quantizer in the second stage of a pipelined SAR ADC and a 0-1 multistage noise-shaping (MASH) structure is configured. However, the NS-SAR quantizer is applied only to the second stage and the maximum achievable resolution is still limited. To improve the accuracy further for a given bandwidth, we propose a 1-2 MASH pipelined NS-SAR ADC [18] that applies a NS-SAR quantizer to all stages and has the following advantages: 1) immunity to comparator noise and speed enhancement due to pipelined SAR structure; 2) high-order NTF and high stability achieved by MASH structure; and 3) fast residue signal processing by parallel operation. To minimize the power consumption, we also propose a way to acquire the 3rd-order NTF only with a single OTA. Our proposed ADC shows an 84.6 dB DR and a competitive FoM_{DR} of 175.2 dB for 4 MHz bandwidth, and the power consumption is 3.5 mW.

The rest of this article is organized as follows. Section II describes the proposed ADC architecture, and Section III discusses on design considerations for the key building blocks. Section IV explains details of the circuit implementation and operation timing. Then, Section V reports the measurement results, and Section VI makes conclusion.

II. Concept of Pipelined Noise-Shaping SAR ADC

In this section, we introduce the proposed ADC structure and show a way to optimize it for better power efficiency.

A. Pipelining of NS-SAR ADCs

Fig. 2(a) shows our initial concept of the pipelined noise-shaping SAR ADC that simply replaces SAR quantizers in a conventional pipelined SAR ADC with NS-SAR quantizers. The resulting structure in Fig. 2(b) will have the final digital output and NTF of each stage that are expressed as

$$D_{\text{OUT}}(z) = V_{\text{IN}}(z) + \frac{1}{G}\cdot\text{NTF}_{\text{STG2}}(z)\cdot Q_2(z) \quad (1)$$

$$\text{NTF}_{\text{STG\#}}(z) = \frac{1}{1+L_{\#}(z)} \quad (2)$$

where $L_{\#}(z)$ is the integrator transfer function of each stage, G is the inter-stage gain, and Q_2 is quantization noise from the second stage (STG2). The signal transfer function remains as unity, and only the quantization noise from STG2 appears at the final output since the first stage (STG1) quantization noise is canceled out by digital correction logic. At this time, Q_2 is not only shaped by $\text{NTF}_{\text{STG2}}(z)$ but also suppressed by the inter-stage gain G with the help of pipelining, and a sufficiently high resolution is achievable. However, the NTF generated by the first stage ($\text{NTF}_{\text{STG1}}(z)$) does not contribute to the overall NTF even though STG1 uses a NS-SAR quantizer

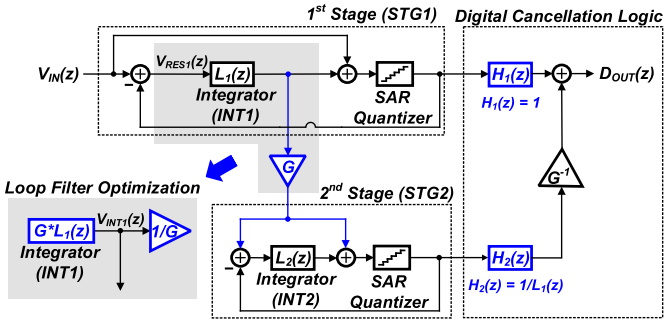

Fig. 3. Optimization of pipelined NS-SAR ADC structure to achieve 1-2 MASH structure with single amplifier.

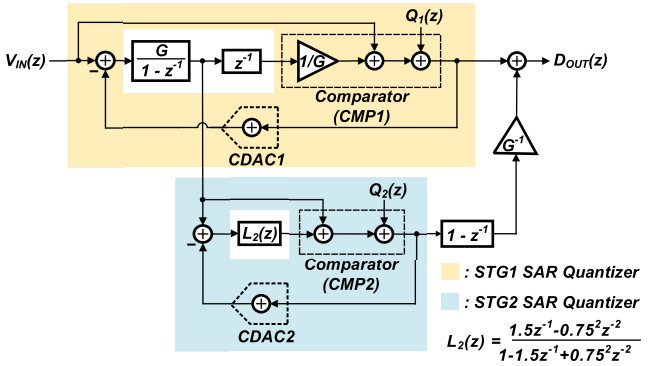

Fig. 4. Block diagram of proposed pipelined NS-SAR ADC with 3rd-order noise-shaping.

instead of an SAR quantizer. Much higher resolution could be achieved if the NTF of STG1 is reflected in the final NTF, and this means that a coarser quantizer and a lower OSR would be enough to achieve a given target resolution and bandwidth while significantly reducing the power consumption.

B. MASH Structure for High-Order NTF

We modify the scheme in Fig. 2 so that the NTF of STG1 contributes to the overall NTF. In STG1, the integrator output instead of the residue signal (V_{RES1}) is transferred to STG2 as shown in Fig. 3. By applying an appropriate digital cancellation filter to the digital output of each stage, we can get the final digital output that is expressed as

$$D_{\mathrm{OUT}}(z) = V_{\mathrm{IN}}(z) + \frac{1}{G} \cdot \frac{1}{L_1(z)} \cdot \mathrm{NTF}_{\mathrm{STG2}}(z) \cdot Q_2(z) \quad (3)$$

where $1/L_1(z)$ can be approximated to $\mathrm{NTF}_{\mathrm{STG1}}(z)$ which is equal to $1/(1 + L_1(z))$ as long as $L_1(z)$ is sufficiently large in the signal band. So, the final NTF can be expressed as $1/G \cdot \mathrm{NTF}_{\mathrm{STG1}}(z) \cdot \mathrm{NTF}_{\mathrm{STG2}}(z)$. The modified structure is similar to the MASH structure of $\Delta\Sigma$-ADCs, but it is slightly different in that the inter-stage gain shows in the final NTF. The quantization noise is not only attenuated by both NTFs but also suppressed by the inter-stage gain, so a higher resolution than that from the architecture in Fig. 2 is achievable.

C. Loop Filter Implementation

Signal integration and amplification are necessary in the proposed structure, so their implementation could be critical for energy efficiency and noise performance. At least one amplifier is essential to get inter-stage gain for pipelining, and the residue signal needs to be integrated with a minimum number of additional amplifiers to avoid significant power increase. A passive integrator based on charge sharing is a good option considering only the power consumption, but it suffers from integration loss and makes it difficult for a NS-SAR ADC to obtain high resolution. A multi-input comparator with a large comparator gain might be able to compensate the integration loss. However, the comparator gain needs to be high enough to acquire the desired NTF and the high gain multi-input comparator design bottlenecks the performance of a conventional NS-SAR ADC with a passive integrator. Therefore, recent NS-SAR ADCs [9], [19] has preferred to use passive integrators in combination with active ones for optimized power efficiency and resolution, and we will take a similar approach for the same purpose.

If STG1 in Fig. 3 uses a passive integrator, the inter-stage gain needs to be quite large to recover the attenuation of the first integrator output for the target resolution, which increases the OTA requirement accordingly. To avoid both signal attenuation and use of an additional OTA, the integrator of STG1 (INT1) can be combined with the inter-stage gain amplifier to share the OTA as shown in Fig. 3. The unity-gain bandwidth of the OTA for the integrator that results from the sharing above should increase by G due to the decreased feedback factor. However, the integrator drives a very small capacitor in STG2 as will be described in Section III-C, so the total load capacitance of the OTA will decrease by a similar factor due to the reduced feedback capacitor. Therefore, sharing of the OTA can save power and hardware costs. Furthermore, amplification and integration of the residue signal happen simultaneously, and the sampling rate can also be improved. Now, INT1 will have additional gain of G, which would change the original loop transfer function of STG1 and saturate the quantizer input. To recover the original target transfer function and avoid signal saturation, V_{INT1}, which represents the integrator output of the modified structure, is attenuated at the quantizer input, which can be implemented by using a multi-input comparator with the inverse of the inter-stage gain.

By contrast, STG2 focuses mainly on power efficiency and is implemented with a passive integrator that further shapes the quantization error. A 2nd-order passive integrator is used to maximize the resolution, and it barely affects the overall conversion speed and power consumption due to the intrinsic nature of the second stage. The SAR conversion in STG2 can run faster than that in STG1, so STG2 has enough time for the 2nd-order passive noise-shaping without affecting the overall conversion speed while increasing the noise-shaping order of STG1 would significantly slow down the conversion speed and require additional OTA. Therefore, the proposed ADC can achieve the target resolution easily by the final 3rd-order NTF without additional power-hungry amplifiers.

Fig. 4 shows the final block diagram considering the hardware implementation. The SAR quantizer consists of a capacitive DAC (CDAC) and a multi-input comparator. The transfer function of each integrator is also presented, and the

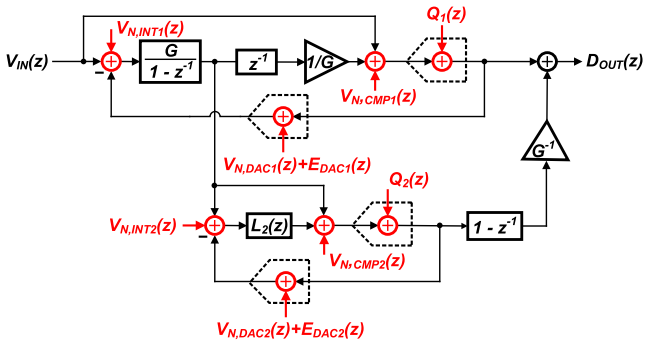

Fig. 5. Noise and nonlinearity sources for proposed ADC.

resulting digital output is expressed as

$$D_{\mathrm{OUT}}(z) = V_{\mathrm{IN}}(z) + \frac{1}{G}\cdot\left(1-z^{-1}\right)\cdot\left(1-0.75z^{-1}\right)^2\cdot Q_2(z) \quad (4)$$

and the quantization noise is shaped by 3rd-order as expected.

D. Analysis of Noise Performance

Besides the high-order noise-shaping, the proposed ADC has an advantage of low noise contribution from its building blocks. Fig. 5 shows every noise source in the proposed ADC and the final digital output including noise is expressed as

$$\begin{aligned} D_{\mathrm{OUT}}(z) &= V_{\mathrm{IN}}(z) + V_{N,\mathrm{DAC1}}(z) + E_{\mathrm{DAC1}}(z) + V_{N,\mathrm{INT1}}(z) \\ &\quad +\mathrm{NTF}_1(z)\cdot\left(E_{\mathrm{DAC2}}(z) + V_{N,\mathrm{DAC2}}(z) + V_{N,\mathrm{INT2}}(z)\right) \\ &\quad +\mathrm{NTF}_2(z)\cdot\left(V_{N,\mathrm{CMP2}}(z) + Q_2(z)\right) \end{aligned} \quad (5)$$

where

$$\mathrm{NTF}_1(z) = \frac{1.5}{G}\cdot z^{-1}\cdot\left(1-z^{-1}\right)\cdot\left(1-0.375z^{-1}\right)$$
$$\mathrm{NTF}_2(z) = \frac{1}{G}\cdot\left(1-z^{-1}\right)\cdot\left(1-0.75z^{-1}\right)^2$$

and $V_{N,\mathrm{DAC\#}}$, $E_{\mathrm{DAC\#}}$, $V_{N,\mathrm{INT\#}}$, and $V_{N,\mathrm{CMP\#}}$ represent thermal noise from CDAC, CDAC mismatch error, thermal noise from integrator, and comparator in each stage, respectively. For STG1, noise and error from CDAC, and input referred integrator noise appear directly at the final output while quantization noise and comparator noise are completely canceled out by a digital cancellation filter. For STG2, the CDAC noise and error, and input referred integrator noise are reduced by $1.5/G$ and noise-shaped unlike in STG1. NTF_1 of (5) has two zeros of 1 and 0.375, so it shows weak 2nd-order noise-shaping. The comparator noise and quantization noise are also attenuated by $1/G$ and noise-shaped by 3rd-order. In summary, most noises except for those from CDAC1 and INT1 are suppressed substantially due to the pipelined structure as well as noise-shaping SAR quantizers.

Note that noise from STG2 is highly suppressed, and thus, the design complexity and requirement for STG2 become much relaxed compared with conventional two-stage pipelined SAR ADCs or 0-1 MASH structured ADCs. Also, the CDAC2 size can be greatly scaled down regardless of its mismatch thanks to the 2nd-order noise-shaping. Finally, the comparator also benefits from the structure and a very coarsely designed multi-input comparator can be used in STG2 not affecting the overall performance.

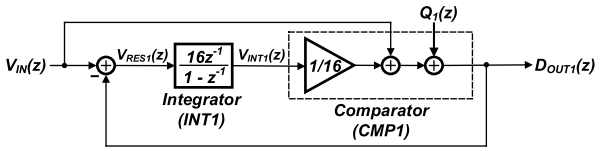

Fig. 6. Block diagram of 1st-order NS-SAR quantizer for STG1.

III. Design Consideration

This section describes how to determine the number of quantization bits in each stage and the inter-stage gain. Also, we discuss the design parameters of each integrator and issues related to its implementation.

A. Quantization Bit Number and Inter-Stage Gain

In addition to noise-shaping, there are two more factors in (4) affecting the resolution; the quantization noise Q_2 from STG2 and the inter-stage gain G. Finer quantizer of STG2 reduces Q_2 and can easily enhance the ADC resolution by itself. Also, a larger G will attenuate the output noise linearly so is also helpful for achieving high resolution. However, thanks to the high-order noise-shaping, fine quantization in STG2 and large inter-stage gain are not essential in our work for the target resolution. Rather, the quantization noise Q_1 from STG1 which does not appear in (4) could be more critical due to noise leakage effect caused by mismatch between digital and analog filters in MASH structures [5], [7], [15]. Q_1 would not be completely canceled out and transferred to the final output if $G\cdot L_1(z)$ in STG1 varies and does not match to $G^{-1}\cdot H_2(z)$ for digital cancellation logic in Fig. 3. This leads to increase in the noise floor and limits the maximum achievable resolution regardless of quantization bit number of STG2 or inter-stage gain. The noise leakage is mostly related to the nonideality of INT1 but the use of a finer quantizer for STG1 can alleviate the leakage effect to some extent by decreasing the absolute amount of Q_1. Even though a finer quantizer for STG1 can make the design of a perfect integrator unnecessary, too fine quantizer burdens the hardware implementation and makes the pipelined structure less advantageous. Therefore, the quantization bit number B_1 for STG1 is chosen to be 5 in this work considering the trade-off between leaked noise and hardware complexity. Accordingly, the inter-stage gain is set to 16 ($=2^{(B_1-1)}$) guaranteeing enough margin for the input overloading of STG2. A 4 bit quantizer is chosen in STG2, and these parameters give 94 dB signal-to-quantization-noise ratio (SQNR) for OSR of 10, which does not include the noise leakage effect. The exact noise leakage effect on the proposed ADC performance will be discussed in Section III-B.

B. First Stage Noise-Shaping SAR ADC Design

Fig. 6 illustrates the block diagram of a NS-SAR ADC for STG1. The integrator can be implemented as in Fig. 7 providing the inter-stage gain. Nonideality of the integrator is the

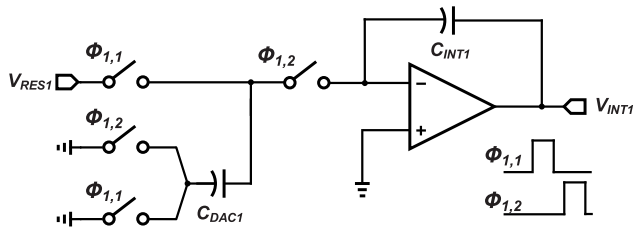

Fig. 7. Active integrator for STG1 based on switched-capacitor circuit.

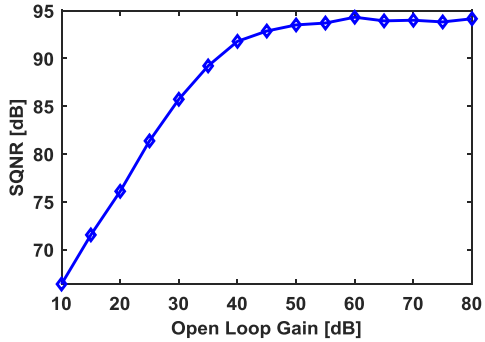

Fig. 8. Maximum achievable SQNR of proposed ADC versus open loop gain of amplifier for INT1.

most critical for the ADC performance since the other blocks are mostly involved in coarse SAR conversion. The integrator transfer function could vary substantially depending on finite open-loop gain (A_{OL}) of the amplifier, A_{OL} variation due to PVT variation and mismatch between the total capacitance of CDAC1 (C_{DAC1}) and integration capacitance (C_{INT1}) shown in Fig. 7. Our work is aimed at high resolution, so the capacitors are sized quite large to suppress kT/C noise. Thus, the capacitor mismatch is negligible and barely contributes to the integrator performance. On the other hand, A_{OL} could have a quite large effect on the integrator transfer function that is expressed as

$$L_1(z) = G \cdot \frac{\lambda}{1 - pz^{-1}} \tag{6}$$

where

$$\lambda = \frac{1}{1 + (1+G)/A_{\mathrm{OL}}}$$
$$p = \frac{1 + 1/A_{\mathrm{OL}}}{1 + (1+G)/A_{\mathrm{OL}}}$$
$$G = \frac{C_{\mathrm{DAC1}}}{C_{\mathrm{INT1}}}$$

G, λ, and p represent the desired inter-stage gain, inter-stage dc gain loss, and integration loss, respectively. λ and p are ideally unity assuming A_{OL} is infinite. However, finite A_{OL} generates nonunity λ and p, which causes mismatch between analog and digital filters as mentioned previously. The resulting noise leakage problem could be addressed by compensating $H_2(z)$ in the digital cancellation filter according to the change in $L_1(z)$ if all the parameters are well known. As shown in Fig. 8, a >84 dB SQNR can be still achieved even with the low A_{OL} of 30 dB. However, A_{OL} varies due to PVT variation, and the noise leakage is not perfectly canceled out and still affects the resolution. This phenomenon that often occurs in a pipelined

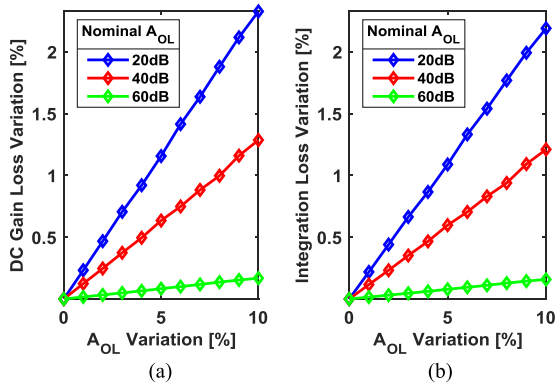

Fig. 9. (a) DC gain loss variation and (b) integration loss variation of INT1 versus open-loop gain variation for different nominal open-loop gains of amplifier in INT1.

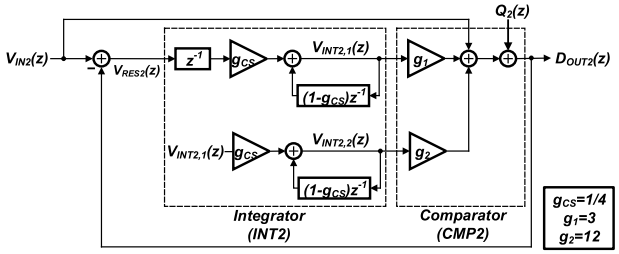

Fig. 10. Block diagram of 2nd-order NS-SAR quantizer for STG2.

structure becomes severe when the quantization in the first stage is coarser, and the signal-dependent noise leakage would cause high in-band spurs. The variation of λ and p over PVT becomes greater for lower A_{OL} as in Fig. 9(a) and (b), which makes the noise leakage compensation difficult and can significantly lower the yield. Thanks to the loop filter in STG1, Q_1 is dithered and looks similar to a white noise regardless of the coarse quantization. This helps to suppress the signal-dependent spurs and mitigate the noise leakage effect. Therefore, a lower open-loop gain, compared to those used in other pipelined structures without noise-shaping in the first stage, can be used in our work. The required minimum open-loop gain can be determined by Monte–Carlo SPICE simulation, and an A_{OL} over 52 dB is enough to meet the target SNR of >80 dB for 6σ variation when the standard gain deviation σ is assumed to be 10% with a quite large margin.

The comparator gain variation is another consideration. A multi-input comparator is adopted to sum the input signal with the integrator output V_{INT1} with the weight of 16:1. The attenuation of V_{INT1} can be easily implemented by the input device width ratio of a multi-input comparator. The input device mismatch, common-mode voltage difference, and large comparator input signal due to 5 bit quantization might change the pole location in the NTF of STG1, but it barely affects the loop stability since the nominal loop gain of STG1 is unity and has quite large margin for stability.

C. Second Stage Noise-Shaping SAR ADC Design

The NS-SAR ADC for STG2 with a passive integrator adopts the architecture similar to [20] shown in Fig. 10.

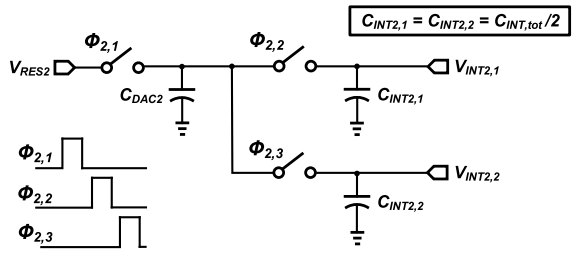

Fig. 11. 2nd-order passive integrator for STG2 based on charge sharing.

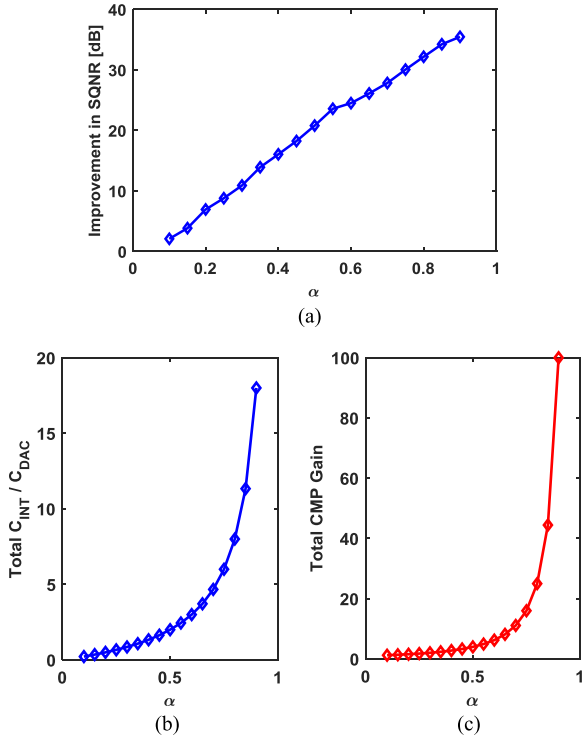

Fig. 12. (a) Improvement in SQNR of proposed ADC. (b) Required integration capacitance over CDAC capacitance. (c) Required comparator gain versus charge sharing integration gain ($=\alpha$).

Fig. 11 shows the integrator block diagram where residue signal gain (g_{CS}) is expressed as $C_{DAC2}/(C_{DAC2}+C_{INT2,\#})$ and integration gain ($\alpha = 1-g_{CS}$) is expressed as $C_{INT2,\#}/(C_{DAC2}+C_{INT2,\#})$. Typical fully passive 2nd-order NS-SAR ADCs [11], [20], [21] using the integrator above give NTF expressed as $(1-\alpha z^{-1})^2$. α is desired to be close to unity for sharp NTF as in Fig. 12(a); however, this not only requires large $C_{INT2,\#}$ but also needs high comparator gain compensating for the residue signal attenuated by low g_{CS}, as shown in Fig. 12(b) and (c). Furthermore, the noise of a multi-input comparator grows fast as the gain increases, and the comparator power consumption would soar to keep the comparator noise smaller than the LSB size regardless of noise-shaping.

On the other hand, our NS-SAR ADC for STG2 is free from the trade-off between NTF performance, capacitor size, and comparator power since it is located at the second stage. CDAC2 can be made tiny since its thermal noise and mismatch has little effect on SNDR as shown in (5). Thus, having $C_{INT,tot}$ that is multiple times C_{DAC2} is allowed, which suppresses integration loss without area penalty. Also, the 4 bit coarse quantization of STG2 relaxes the design requirement of the comparator, so the comparator gain barely affects the noise performance or power consumption. As a result, in STG2, the total integration capacitance is set to $6C_{DAC2}$ ($C_{INT2,1} = C_{INT2,2} = 3C_{DAC2}$) and the multi-input comparator is designed to have a gain ratio of 1:3:12, which provides α of 0.75 satisfying the target resolution by the plot in Fig. 12(a).

In contrast to STG1, the comparator in STG2 uses the gain much greater than unity, which can cause a stability issue, and this will be discussed in Section IV.

IV. Circuit Implementation

Circuit implementation and timing diagram of the proposed ADC are shown in Fig. 13. Both stages adopt merged capacitor switching scheme for better energy efficiency, and CDACs and switches are configured accordingly. The single-ended total capacitance C_{DAC1} is chosen to be 2.5 pF for the performance not to be limited by kT/C noise, and the integration capacitor is set to 156 fF (=unit capacitance C_1) for amplification by 16. The capacitor mismatch is calibrated off-chip to achieve high SFDR. On the other hand, CDAC2 can be made tiny as mentioned previously and a 20 fF unit capacitor (C_2) is used. Thanks to the small capacitance C_{DAC2}, the integration capacitor can have a reasonable size of 480 fF ($=24C_2$). The mismatch for CDAC2 is not calibrated since it is shaped and suppressed by the pipelined loop filter. Also, digital cancellation filter is implemented off-chip. The coefficients of λ and p shown in Fig. 13 are determined by (6).

The proposed ADC operates as: the sample-and-hold (S/H) phase $\Phi_{S/H1}$ is followed by 5 bit conversion phase Φ_{CONV1} in STG1 where asynchronous SAR logic is used for faster conversion. After Φ_{CONV1}, the resulting SAR residue signal is integrated and amplified (Φ_{INT1}), and at the same time the S/H phase $\Phi_{S/H2}$ of STG2 starts. Then, STG1 repeats the same cycle from S/H while STG2 starts 4 bit asynchronous SAR conversion (Φ_{CONV2}) followed by two-step charge sharing (Φ_{INT2}) for 2nd-order noise-shaping. The digital output of each stage produces the final output after digital cancellation filtering. The conversion period is 12 ns, and it consists of $\Phi_{S/H1} = 2$ ns, $\Phi_{CONV1} = 3.3$ ns and $\Phi_{INT1} = 6.6$ ns.

A two-input comparator in Fig. 14 is used in STG1 to process the output of INT1. We employ a double differential version of the strong-arm latched comparator for low kickback noise, power efficiency, and simple dynamic structure. The STG2 comparator has the same structure but has one more input pair and the input devices are sized 1:3:12 for residue signal path gain as in Fig. 15. As mentioned, a large comparator gain can affect the loop stability due to mismatch. The loop stability of STG2 is verified by 500-run Monte–Carlo SPICE simulation. Fig. 16 shows the resulting NTF pole-zero plot when x3 and x12 gains vary by the input device mismatch and common mode voltage difference, and it is observed that our system is robust since poles remain in the unit circle regardless of the tiny size of the input devices and other variations.

The OTA design can be critical both for sampling rate and resolution. A wide-BW OTA is necessary in our work to shorten the integration phase Φ_{INT1} that takes a substantial part of the pipelined phase. In addition to that, high dc-gain and wide output swing are also required to minimize distortion

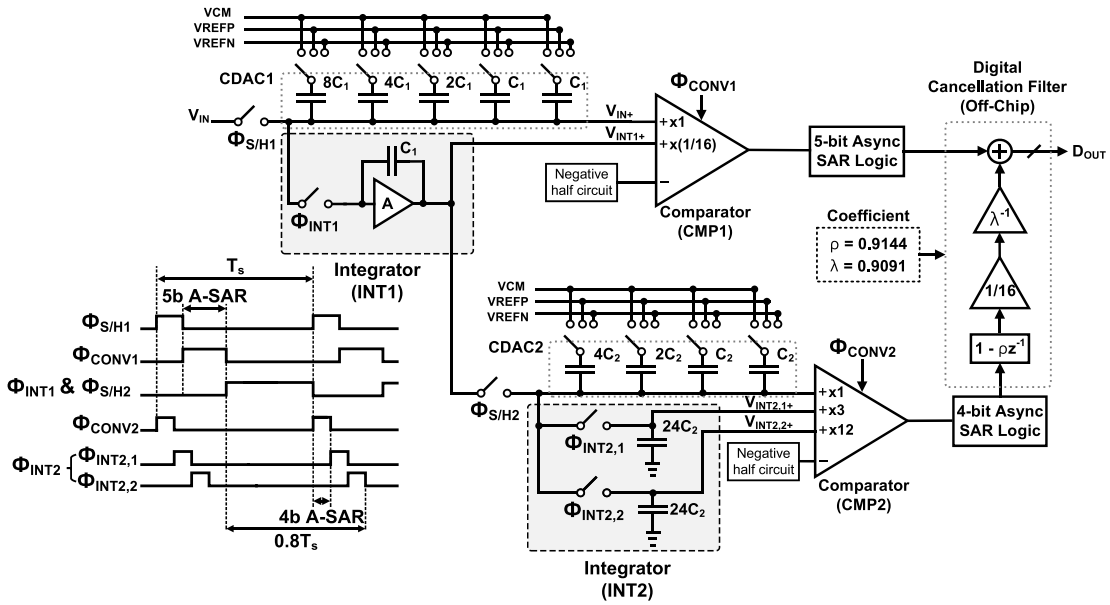

Fig. 13. Implementation of proposed pipelined NS-SAR ADC with 1-2 MASH structure.

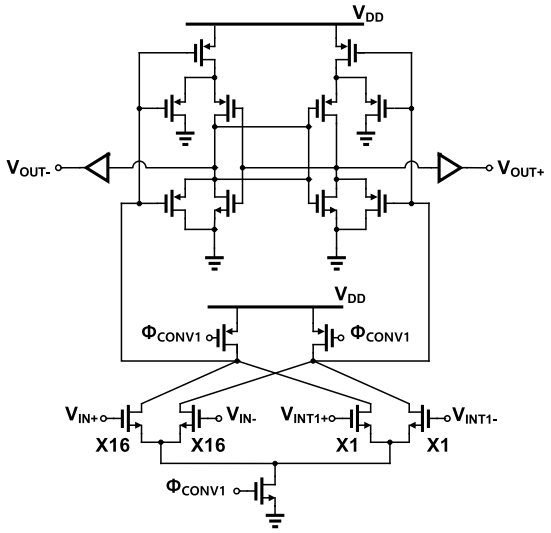

Fig. 14. Comparator in STG1 (CMP1) with two-inputs for summing input signal and INT1 output signal.

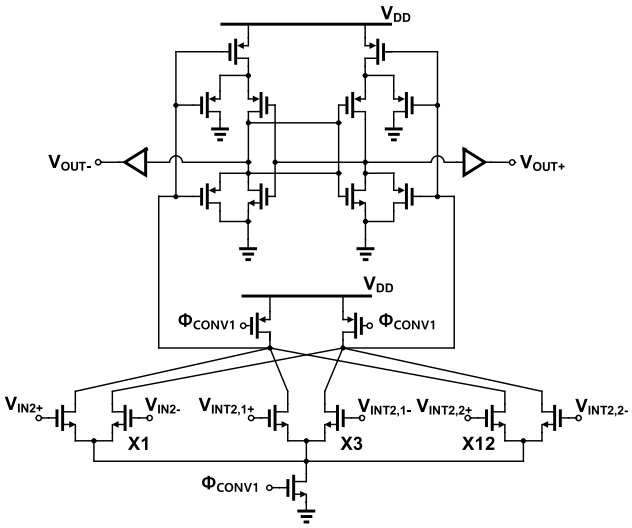

Fig. 15. Comparator in STG2 (CMP2) with three-inputs for summing input signal and two INT2 output signals.

and noise leakage that varies due to PVT. To meet those requirements, we adopt a two-stage feedforward compensated OTA shown in Fig. 17. M_{1-6} provide a slow path with high dc gain, and M_{7-8} create a high frequency feedforward path stabilizing the OTA. Each stage has its own CMFB that enables high CMRR. The open-loop gain variation σ of the OTA over PVT is simulated to be less than 5% ($=1\sigma$, so a 45 dB dc gain which is lower than the requirement in Fig. 9(a) and (b) is used while guaranteeing the target resolution. The unity-gain bandwidth is set to 2.3 GHz so that the settling error does not impair the overall resolution. The OTA consumes a power of 2.51 mW for 1.2 V supply voltage.

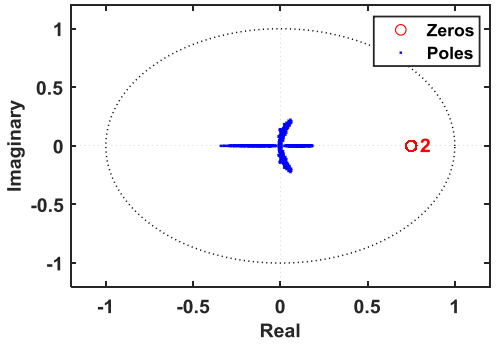

Fig. 16. Pole-zero scatter plot for NTF of STG2 according to comparator (CMP2) gain variation.

V. Measurement Result

The ADC prototype is fabricated in 65 nm CMOS process and occupies an active area of 390 × 290 μm^2 shown in Fig. 18. Fig. 19 shows the ADC measurement setup with off-chip digital cancellation filter and CDAC calibration. The digital output signals come from both STG1 and STG2, and

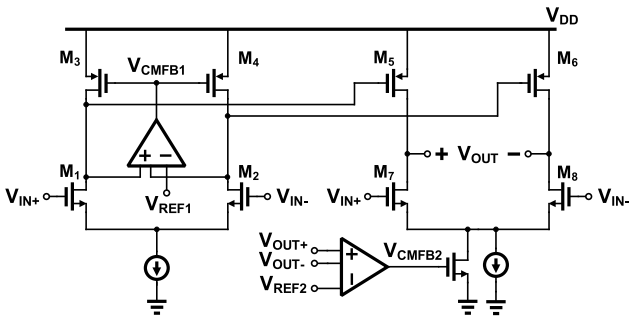

Fig. 17. Two-stage feedforward compensated OTA.

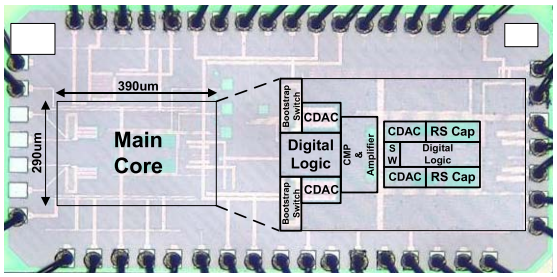

Fig. 18. Die photograph.

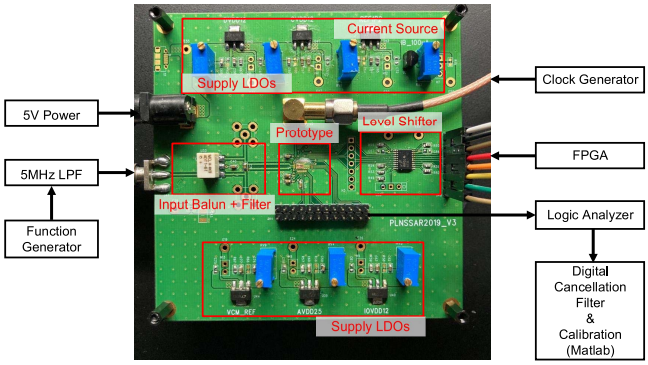

Fig. 19. ADC measurement setup.

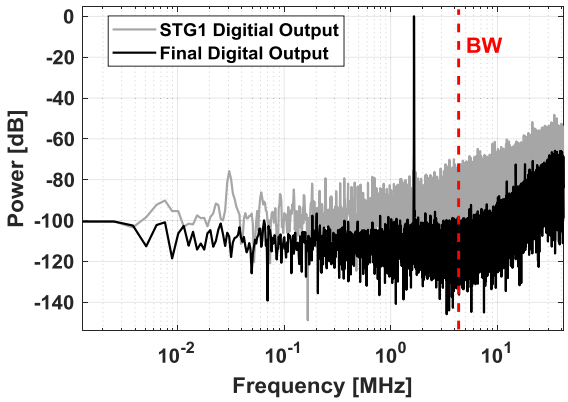

Fig. 20. Power spectral density of first stage and final digital outputs at 1.7 MHz input tone with CDAC mismatch calibration ON.

they are processed by digital cancellation filter in MATLAB to provide the final digital output. Fig. 20 shows the power spectral density of the STG1 output and the final output (65k FFT). The peak SNDR/SFDR of them are measured to be 55.8 dB/69.5 dB and 77.1 dB/92.3 dB, respectively, when a 1.65 MHz input tone at −1.1 dBFS is applied and

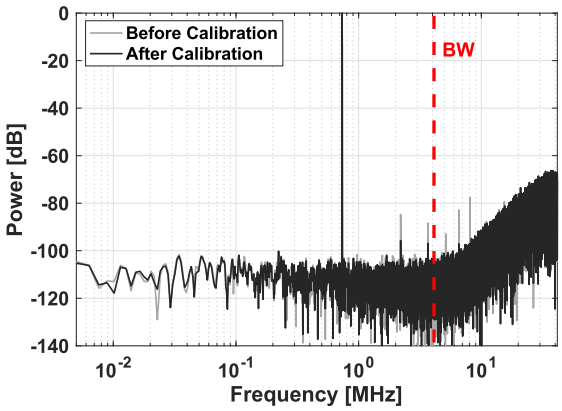

Fig. 21. Power spectral density of final digital output at 733 kHz input tone with CDAC1 mismatch calibration OFF (gray) and ON (black).

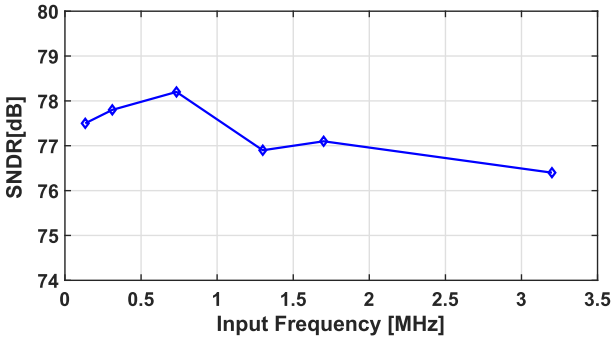

Fig. 22. Measured SNDR across different input frequencies.

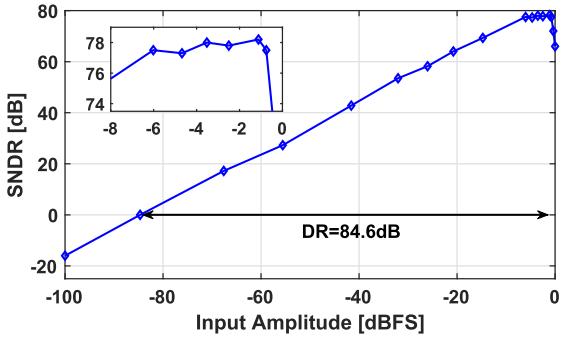

Fig. 23. Measured SNDR across different amplitude with input tone at 733 kHz.

the bandwidth is 4.1 MHz (sampling rate = 83.3 MS/s, OSR = 10). The measured power spectral density with a 773 kHz input tone is also shown in Fig. 21. The measured SNDR/SFDR improves from 76.7 dB/84 dB to 78.1 dB/95 dB. It also compares the results when CDAC1 mismatch calibration is ON/OFF. As mentioned in Section IV, only the CDAC1 mismatch error is calibrated and performed off the chip with cvx toolbox [22] by finding each capacitor size for which SNDR is optimized.

Fig. 22 plots the measured SNDR across different input frequencies and the SNDR variation is below 2 dB. Fig. 23 plots the measured SNDR across different input amplitudes and our prototype achieves DR of 84.5 dB. The SNDR starts to be saturated as the input level increases above −6 dBFS where the in-band noise floor also increases. This limits the peak SNDR and is estimated to be caused by measurement environment and wire-bonds. For the input level below −6 dBFS,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-ART NS-SAR ADCS

	Hsu [23] JSSC 2020	Liu [19] ISSCC 2017	Liu [20] JSSC 2019	Song [15] JSSC 2020	Song [16] JSSC 2021	Hsu [17] JSSC 2021	Lyu [24] VLSI 2020	**This Work*** **
Architecture	Pipelined SAR	NS-SAR	CT-ΔΣ + NS-SAR	Pipelined NS-SAR (0-1 MASH)	Pipelined NS-SAR (0-1 MASH)	Pipelined NS-SAR (0-1 MASH)	Pipelined NS-SAR (0-1 MASH)	**Pipelined NS-SAR (1-2 MASH)**
Technology [nm]	40	28	40	65	28	40	28	**65**
Fs [MS/s]	100	132	500	200	600	100	1000	**83.3**
BW [MHz]	12.5	5	12.5	12.5	40	6.25	125	**4.1**
OSR	4	13.2	20	8	7.5	8	4	**10**
Area [mm^2]	0.061	0.0049	0.029	0.014	0.016	0.054	0.018	**0.113**
Resolution [bits]	12	10	4	10	10	11	8	**8**
SNDR [dB]	75.8	79.74	70.4	77.1	75.2	77.1	63.58	**78.2**
DR [dB]	76.8	81.8	73	78.5	76.6	78.2	N/A	**84.6**
Power [mW]	1.54	0.46	1.16	4.5	2.56	1.38	2.3	**3.5**
FoM$_{S,DR}$* [dB]	175.9	182.2	170.7	172.9	178.5	174.6	N/A	**175.2**
FoM$_{S,SNDR}$ [dB]**	174.9	180.1	173.3	171.5	177.1	173.7	170.9	**168.8**

$FoM_{S,DR} = DR + 10*log10(BW/Power)$
**$FoM_{S,SNDR} = SNDR + 10*log10(BW/Power)$*
****off-chip digital cancellation filter*

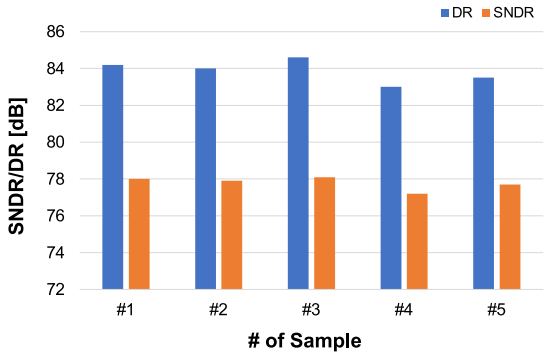

Fig. 24. Measured DR/SNDR of 5 samples.

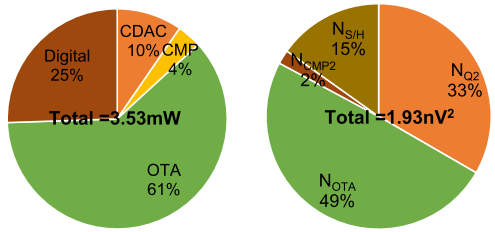

Fig. 25. Pie chart of power consumption and noise budget.

our prototype shows better SNDR than 0-1 MASH NS-SAR ADCs [15]–[17] and provides higher DR, which demonstrates the effectiveness of the proposed architecture. The measured DR and SNDR show small variation for different samples and are less than 2 dB as in Fig. 24.

Fig. 25 shows the details of power consumption and total noise budget by blocks. The total power consumption is measured to be 3.53 mW when a supply voltage of 1.2 V is applied and on-chip regulators and output driving buffers are not included. The power consumption of STG2 is less than 1/4 of that of STG1 (excluding the OTA power) thanks to the pipelined noise-shaping structure. The total noise budget considering OSR of 10 is 1.93 nV^2. The comparator noise barely affects the overall SNR as expected, while the OTA dominates the overall noise performance since its noise is not shaped as the input sampling noise. Therefore, the total power consumption is also dominated by the OTA as in Fig. 25.

Table. I summarizes the performance of our prototype and compares it with state-of-the-art NS-SAR ADCs. The proposed ADC achieves high DR regardless of 9 bits quantization (1 bit redundancy) providing several MHz BW. Also, it shows good power efficiency of 175.2 dB FoM$_{S,DR}$ and 168.8 dB FoM$_{S,SNDR}$ despite the use of a class-A type two-stage OTA.

VI. CONCLUSION

This work demonstrates a pipelined NS-SAR ADC with 1-2 MASH structure achieving both high resolution and wide bandwidth. The pipelined structure enhances conversion speed, and the use of a coarse quantizer in each stage relaxes noise requirements compared with prior works. The proposed ADC structure shows 3rd-order noise-shaping providing DR over 80 dB without stability issue with the help of MASH structure, and it requires only one OTA for its implementation. The use of a single OTA greatly increases power efficiency together with the pipelined structure. Therefore, the proposed ADC structure can be advantageous in applications demanding low power and wide bandwidth as well as high accuracy.

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