An 80-dB DR, 7.2-MHz Bandwidth Single Opamp Biquad Based CT $\Delta\Sigma$ Modulator Dissipating 13.7-mW

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***Abstract*—A novel low power compact loop filter using a single amplifier biquad (SAB) network is presented for continuous-time (CT) delta-sigma ($\Delta\Sigma$) modulators. This new technique reduces power consumption and die area by minimizing the number of active elements and simplifying the modulator topology. The new SAB network has a transfer function (TF) zero, which implements a local feedforward (FF) path in system-level diagram. By having a local FF branch embedded in the SAB network, the FF branches to the summing block in the SAB based feedforward modulator topology is reduced to half the number of FF branches in the conventional topology. Consequently, the SAB based modulator utilizes a switch-capacitor (SC) adder replacing the commonly used CT adder and the sample & hold blocks in the conventional architecture. The SAB based loop filter with reduced FF branches simplifies the design and implementation of the high-order continuous-time $\Delta\Sigma$ modulator. The proposed loop filter is a general filter, which can be used for both high and low oversampling ratios (OSRs). A 4th-order low pass continuous-time $\Delta\Sigma$ modulator is designed and implemented in 130 nm process to confirm the effectiveness of the proposed techniques. Within a 7.2 MHz signal bandwidth, the measured dynamic range and SFDR of this prototype IC are 80 dB and 83.1 dB, respectively, and the total power consumption of 13.7 mW.**

***Index Terms*—ADC, analog-to-digital converter, biquad filter, continuous-time, $\Delta\Sigma$ modulator, oversampling ratio, single opamp based filter.**

I. Introduction

FUTURE wireless communication products require high-performance analog-to-digital converters (ADCs) that have wide signal bandwidths up to several megahertz and resolutions of more than 10 bits. However, the reduction in supply voltage that accompanies reduced transistor dimensions makes it difficult to realize high performance analog circuits. With the reduction in supply voltage, the dynamic range is also reduced. To keep the same performance, either the architecture must be changed or the thermal noise of the analog components must be reduced, which in turn will normally increase the power dissipation. Discrete-time (DT) modulators with 4 MHz bandwidth and resolutions of 11 bits have been reported [1]–[3]. Compared with DT converters, CT converters have the advantages of lower power consumption and inherent anti-aliasing filtering. Additionally, they do not suffer from noise aliasing because of the continuous-time loop filter. Moreover, the absence of stringent settling requirements enables CT converters to digitize signals up to several hundred MHz [4], which is still not possible for their DT counterparts. All these advantages result in an extended battery life and reduced system complexity, which are especially important for portable wireless devices.

Recent CT modulators have achieved bandwidths of 10 MHz in 0.18-μm CMOS technology [5]–[7] and 15 MHz [8]–[10] and 20 MHz [11]–[13] in 0.13-μm CMOS technology, all with a resolution of 10 bits or more. These results suggest that CT implementations are capable of operating at signal bandwidths difficult to achieve with DT designs while still maintaining high resolution.

This paper describes the architecture design and circuit realization of an area and power efficient biquad filter-based CT $\Delta\Sigma$ modulator with an increased stability range implemented in 0.13-μm CMOS technology. A novel single amplifier biquad (SAB) network is developed to be utilized in the proposed modulator topology, which can be used in either high or low OSR applications. In other words, both zero-optimized and non-zero-optimized modulator noise transfer functions (NTFs) can be realized with the proposed network. Using a SAB network decreases the power consumption and die area of the CT $\Delta\Sigma$ modulator by reducing the number of active blocks and FF branches in the modulator. Because of the reduced number of FF branches to the summing block, an SC adder is used as a summing block in the modulator instead of a CT adder and sample-hold block.

The rest of the paper is organized as follows: Section II of this paper presents details of the general architecture of the SAB based modulators including the proposed SAB based CT ADC. The system level design and analysis of the wideband, high-resolution 4th-order CT A/D modulator is described in Section III. Section IV covers the design details of the analog and digital blocks of the modulator. Section V presents the measured performance of the prototype. The paper concludes in Section VI.

II. General Architecture of the SAB Based CT ADC

Fig. 1 shows a general Nth-order feedforward CT $\Delta\Sigma$ ADC which has the most suitable configuration of the loop filter for

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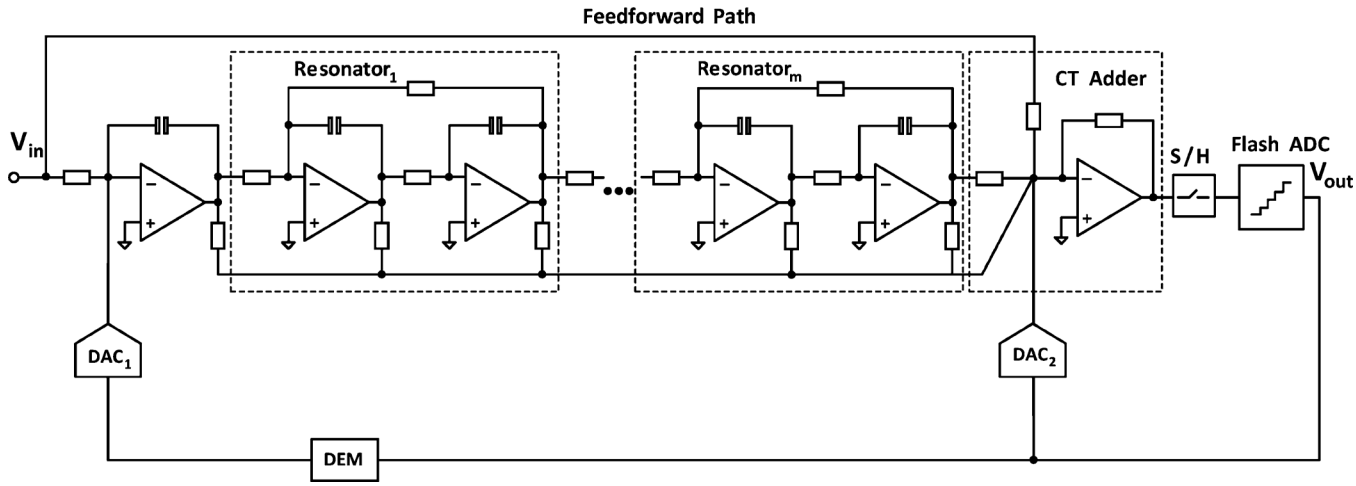

Fig. 1. General block diagram of a conventional Nth-order CT $\Delta\Sigma$ modulator.

low power operation [14]. The loop filter has N active integrators and N feed forward branches going to the adder block. The modulator utilizes a flash-ADC as a multi-bit quantizer and dynamic element matching (DEM) to reduce the nonlinearity of DAC_1. The zero order feedback path to the input of the quantizer is required to improve the modulator stability and compensate excess loop delay introduced by the circuit delays from the output of the sampler block to the output of the DAC [15]. In this paper, we use a 4th-order noise transfer function with at least one pair of in-band zeros and a multi-bit quantizer to realize a modulator with over 12 bit accuracy and a bandwidth higher than 5 MHz. Increasing the modulator order requires more operational amplifiers (opamps) that increase the overall power consumption. Therefore, reducing the number of opamps in high order modulators greatly decreases the power consumption, loop phase delay, and modulator total die area.

Before introducing the proposed SAB network and other techniques used in the CT modulator, recently published SAB network power saving techniques for CT $\Delta\Sigma$ ADC are explained in detail. Advantages and disadvantages of these methods are described and a new network, which overcomes the limitations of existing techniques, is proposed in Section II.B.

A. Conventional SAB Power Saving Techniques for CT $\Delta\Sigma$ Modulators

The loop filter is the main block of a CT $\Delta\Sigma$ modulator. It dissipates a significant amount of the total energy and occupies a major portion of the modulator die area. It has a continuous-time TF with large gain within the signal band, which helps to attenuate out-of-band signals. There are two types of commonly used continuous-time active integrators to realize a loop filter: R-C integrators and Gm-C integrators. Active-RC based loop filters have the widest dynamic range, but they consume more power due to the larger number of active blocks. On the other hand, passive networks do not consume power, but they introduce an attenuation factor for the in-band signals, which amplifies the internal electronic noise, and non-idealities of the loop filter blocks referred to the modulator input [16]. As an alternative, SAB networks which are a combination of active and passive filters and use just one operational amplifier instead of two

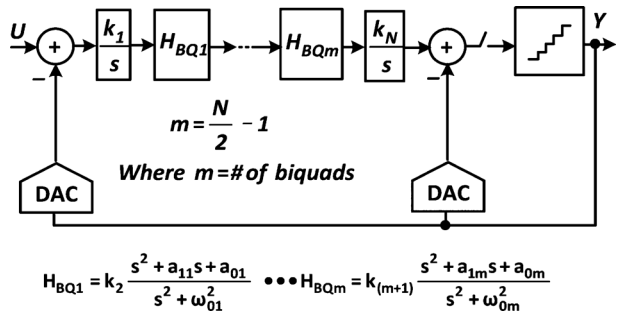

Fig. 2. Nth-order CT $\Delta\Sigma$ modulator topology with cascaded biquad stages.

can be used in the modulator loop filter to reduce the power consumption. SAB-based loop filters have all the benefits of both active and passive filters.

Fig. 2 depicts an Nth-order CT $\Delta\Sigma$ modulator architecture with m cascaded biquad networks in the loop filter (the last integrator is removed if N is odd). References [17], [18] have developed CT modulators with cascaded biquad filters. A single amplifier resonator (SAR) network shown in Fig. 3 is introduced for a 5th-order CT $\Delta\Sigma$ modulator [17]. This second-order network uses one active block rather than two resulting in power and area savings. The transfer function for this biquad does not include a first-order Laplace term in the denominator.

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{\frac{\mathrm{C_{in}}}{\mathrm{C_2}}\mathrm{s}^2 + \frac{1}{\mathrm{C_2R_{in2}}}\mathrm{s} + \frac{1}{\mathrm{C_1C_2R_1R_{in1}}}}{\mathrm{s}^2 + \frac{1}{\mathrm{C_1C_2R_1R_2}}} \tag{1}$$

Thus, the network has a resonating transfer function, which can be utilized to implement a zero optimized noise transfer function. On the other hand, the SAR network in [17] has a third-order transfer function which reduces to second-order for $\mathrm{R_3'}\|\mathrm{R_{in2}} = \mathrm{R_1}\|\mathrm{R_2}\|\mathrm{R_{in2}}\|\mathrm{R_{in1}}$ and $\mathrm{C_3} = \mathrm{C_1} + \mathrm{C_2} + \mathrm{C_{in}}$. Satisfying these assumptions is difficult when the network resistor and capacitor values change with process and temperature variations. As a result, the modulator will not have the desired NTF, which can consequently result in modulator instability.

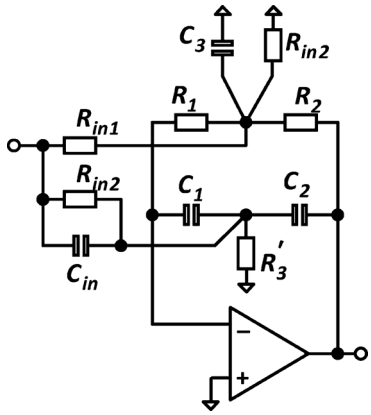

Fig. 3. Single Amplifier Resonator developed by [17].

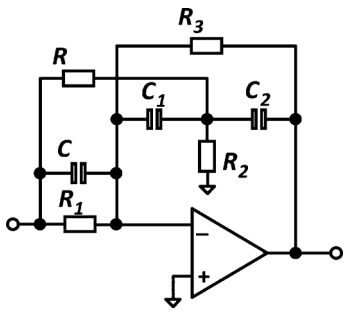

Fig. 4. Single Amplifier Biquad developed by [18].

Another disadvantage of this SAB network is that it cannot be used in the ADC front-end to reduce the power consumption of the most power hungry part of the ADC. Since the input signal is not applied to the virtual ground of the operational amplifier in this structure, the front-end DAC signal cannot be subtracted from the input signal. An alternative biquad network is shown in Fig. 4, and used in the fifth-order CT ΔΣ modulator of [18]. This SAB network has a *true* second-order TF and a reduced number of passive components compared to [17].

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{\mathrm{s}^2 + \frac{1}{\mathrm{C_1}}\left(\frac{2}{\mathrm{R_1}} + \frac{3}{2\mathrm{R}} + \frac{1}{2\mathrm{R_2}}\right)\mathrm{s} + \frac{1}{\mathrm{C_1C_2R_1}}\left(\frac{1}{\mathrm{R_2}} + \frac{1}{\mathrm{R}}\right)}{\mathrm{s}^2 + \frac{2}{\mathrm{C_1R_3}}\mathrm{s} + \frac{1}{\mathrm{C_1C_2R_3}}\left(\frac{1}{\mathrm{R_2}} + \frac{1}{\mathrm{R}}\right)} \tag{2}$$

Unlike the biquad in [17], this SAB network includes a first-order Laplace term in the denominator. This term creates a leakage effect in the modulator final performance by shifting the NTF optimized zeros from the imaginary axes to the left half plane. Fortunately this undesired effect can be attenuated by choosing a relatively high value for $\mathrm{R_3}$.

The other advantage of this network is that it can be utilized in the ADC front-end because the input signal is applied to the operational amplifier virtual ground. Finally, when either of these biquad techniques [17], [18] are incorporated into the loop filter of a CT ΔΣ modulator, they require high gain bandwidth (GBW) amplifiers. The high GBW amplifiers reduce the accumulated delay in the loop filter from the ADC front-end to the input of the quantizer block that can cause modulator instability.

B. The Proposed Stability Improved Topology

Fig. 5 shows the proposed biquad based CT ΔΣ modulator. In this topology, FF branches from the output of the biquad networks to the adder block increase the stability range of the modulator. This is due to the reduced delay introduced by the finite GBW of the loop filter active blocks. This modulator architecture uses an active adder block instead of a passive one used in [17]. The main drawbacks of a passive adder are that it introduces a gain attenuation, which needs to be compensated by boosting the loop filter gain. This gain attenuation introduced by the passive adder can also amplify the input referred non-ideal effects coming from the quantizer block. In addition, the lumped capacitive loading from the comparator units of the multi-bit quantizer introduces an extra pole at the summing node if no isolating sample and hold block is used. The additional pole reduces the modulator stability range. The quantizer loading effect can also be an issue for a modulator with a Gm-R active adder without a sample and hold block. For high performance modulators with very low OSR, using a sample and hold block isolates the quantizer loading effect and also avoids the slew-dependent errors in the quantizer [15], [20]. While this architecture decreases the number of feedforward branches from N to N/2, the feedback factor of the active adder block is enhanced compared to an Nth-order conventional CT ΔΣ modulator (Fig. 1). Consequently, an SC adder block can be utilized instead of the commonly used CT adder and sample-and-hold blocks. In this way, the SC adder acts as both the summing and the sampler block. Additionally, using a switched-capacitor DAC can reduce the power and area of the second DAC. Fig. 6 depicts the improved SAB network and it has all the advantages of the network introduced in [18] with transfer function of:

$$\begin{aligned}\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} &= -\frac{1}{\mathrm{C_1C_2R_1}} \cdot \frac{(\mathrm{C_1}+\mathrm{C_2})\mathrm{s} + \left(\frac{1}{\mathrm{R_2}} + \frac{1}{\mathrm{R_4}}\right)}{\mathrm{s}^2 + \frac{1}{\mathrm{C_1C_2R_3}}\left(\frac{1}{\mathrm{R_2}} + \frac{1}{\mathrm{R_4}}\right)} \\ &= \mathrm{k_{SAB}} \cdot \frac{\mathrm{s} + \mathrm{z_0}}{\mathrm{s}^2 + \omega_0^2}\end{aligned} \tag{3}$$

The positive feedback path introduced by $\mathrm{R_4}$ removes the first-order Laplace term from the denominator when:

$$\mathrm{R_3C_1} = \mathrm{R_4}\left(\mathrm{C_1} + \mathrm{C_2}\right) \tag{4}$$

and

$$\omega_0 = \frac{1}{\sqrt{\mathrm{C_1C_2R_3}(\mathrm{R_2} \| \mathrm{R_4})}}, \quad \mathrm{k_{SAB}} = -\frac{1}{\mathrm{R_1}(\mathrm{C_1} \| \mathrm{C_2})} \tag{5}$$

Eliminating the first-order Laplace term in the SAB transfer function shifts the complex-conjugate poles of the SAB TF from the LHP to the imaginary axes resulting in a perfect pair of optimized zeros in the modulator NTF. Satisfying (4) to eliminate the first-order Laplace term relies on matching the ratio of the capacitors and the ratio of the resistors rather than the absolute

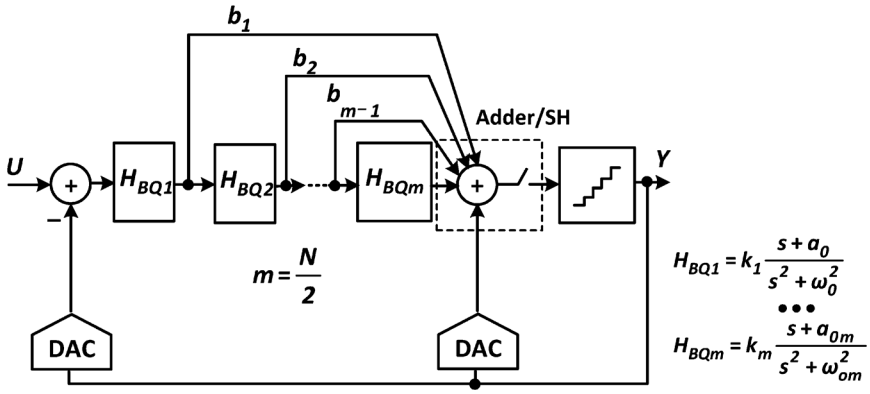

Fig. 5. Stability improved biquad based CT $\Delta\Sigma$ modulator architecture.

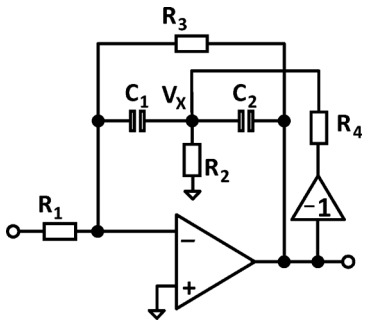

Fig. 6. Proposed single amplifier biquad network.

values of the components. These ratios of capacitors and resistors can be matched to within 0.1% and 1%, respectively, with proper sizing. Meanwhile, the resistor and capacitor process and temperature variations that change the resonant frequency and the SAB block's gain can be calibrated using tuning blocks such as tunable bank of capacitors. The effect of the finite gain in the SAB network is illustrated in (6). To remove the first-order Laplace term in this case, R_4 can be calculated from:

$$\mathrm{R_3C_1} = \mathrm{R_4(C_1 + C_2)} + \frac{\mathrm{R_3C_1}\left(1+\frac{\mathrm{R_4}}{\mathrm{R_2}}\right) + \mathrm{R_4(C_1+C_2)}\left(1+\frac{\mathrm{R_3}}{\mathrm{R_1}}\right)}{\mathrm{A}} \quad (7)$$

The resonant frequency and the gain factor of the SAB filter with the finite gain effect are:

$$\omega_{0,\mathrm{A}} = \omega_0\sqrt{\left(1+\frac{\mathrm{R_3}}{\mathrm{R_1(1+A)}}\right)}, \quad \mathrm{k_{SAB,A}} = \frac{\mathrm{k_{SAB,A}}}{\left(1+\frac{1}{\mathrm{A}}\right)} \quad (8)$$

The SAB TF poles can be shifted further to the RHP to provide a margin for the other non-ideal effects such as component mismatch. Since the SAB network is used in the loop filter of the modulator with an overall negative feedback, the local positive feedback in the network cannot cause any instability.

Another benefit of the proposed SAB network is that $\mathrm{R_2}$ improves the phase margin of the operational amplifier embedded in the SAB network and, together with $\mathrm{R_4}$, it can be used as the common-mode detector for the opamp in the differential topology.

To compare the implementation of the proposed SAB filter with the conventional active-RC resonator, Fig. 7 depicts the equivalent system level diagram of the SAB network and circuit level diagram of the two amplifier based resonator. Considering the SAB filter as a standalone block, the equivalent two amplifier based resonator needs to have an extra summing block to implement the local FF path. The input-output TFs of the two-amplifier based resonators along with their resonant frequency and gain factors, respectively are:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = -\frac{1}{\mathrm{C_1C_2R_1}}\cdot\frac{\mathrm{C_2s}+\frac{1}{\mathrm{R_2}}}{\mathrm{s}^2+\frac{1}{\mathrm{C_1C_2R_2R_3}}} = \mathrm{k_{SAB}}\cdot\frac{\mathrm{s}+\mathrm{z_0}}{\mathrm{s}^2+\omega_0^2} \quad (9)$$

$$\omega_0 = \frac{1}{\sqrt{\mathrm{C_1C_2R_3R_2}}}, \quad \mathrm{k_{SAB}} = -\frac{1}{\mathrm{R_1C_1}} \quad (10)$$

Without considering the adder block in the two amplifier based resonator, the SAB network implements the same TF with the same number of passive components but with one less amplifier. If the proposed SAB filter is used as the loop filter

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} = \frac{-\frac{1}{\mathrm{R_1}}\left[(\mathrm{C_1+C_2})\mathrm{s}+\left(\frac{1}{\mathrm{R_2}}+\frac{1}{\mathrm{R_4}}\right)\right]}{\mathrm{C_1C_2}\left(1+\frac{1}{\mathrm{A}}\right)\mathrm{s}^2+\left\{\frac{\mathrm{C_1}\left(\frac{1}{\mathrm{R_2}}+\frac{1}{\mathrm{R_4}}\right)+(\mathrm{C_1+C_2})\left(\frac{1}{\mathrm{R_1}}+\frac{1}{\mathrm{R_3}}\right)}{\mathrm{A}}+\frac{(\mathrm{C_1+C_2})}{\mathrm{R_3}}-\frac{\mathrm{C_1}}{\mathrm{R_4}}\right\}\mathrm{s}+\left\{\left(\frac{1}{\mathrm{R_3}}+\frac{\left(\frac{1}{\mathrm{R_1}}+\frac{1}{\mathrm{R_3}}\right)}{\mathrm{A}}\right)\left(\frac{1}{\mathrm{R_2}}+\frac{1}{\mathrm{R_4}}\right)\right\}} \quad (6)$$

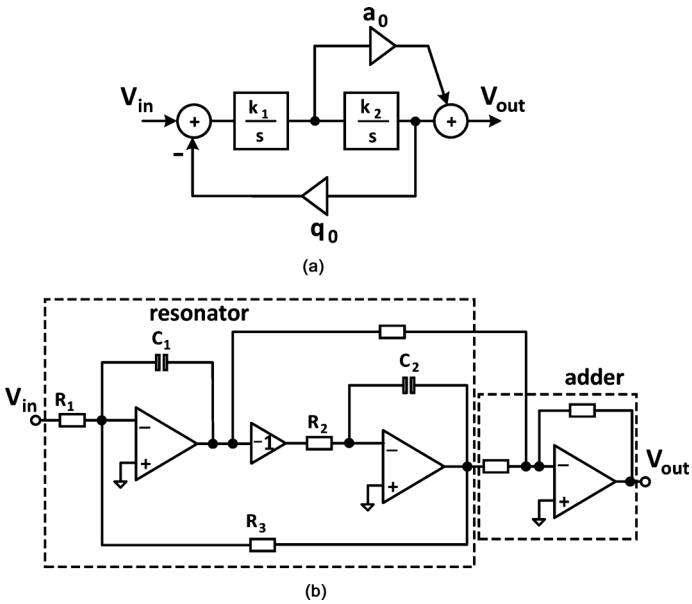

Fig. 7. (a) Equivalent system-level diagram of the proposed SAB network (b) equivalent two amplifier based resonator filter topology.

TABLE I
MODULATOR NOISE BUDGETING

Noise Source	Noise Budget (%)	SNR (dB)
Quantization Noise	8	89.2
Thermal Noise	25	84.3
Clock Jitter	35	82.8
Quantizer Error	7	89.8
DAC Mismatch	15	86.5
Other Noise Sources	10	88.3

in a second-order FF modulator topology, it does not require a summing block unlike the conventional two-amplifier based second-order loop filter topology.

III. SYNTHESIS OF THE PROPOSED 4TH-ORDER SAB BASED CT ΔΣ

The target specification for the proposed SAB based CT modulator in this paper is defined to be 13 bits with an input signal bandwidth of 10 MHz. The modulator maximum power dissipation is designed for less than 15 mW. All the noise sources of a CT modulator such as quantization noise of the inner flash-ADC, thermal noise of all circuit components, clock jitter, DAC unit mismatches, and the quantizer imperfections are accounted for in the noise budget as summarized in Table I. As shown, thermal noise and clock jitter are the two dominant noise sources in the CT modulator design. The clock jitter noise budget is determined by the phase noise of the off-chip clock source.

A. Modulator Gain Coefficient Scaling Techniques

Based on extensive simulations in MATLAB, a fourth-order, 4-bit (16 output levels) topology is chosen. The nominal clock frequency for the design is chosen to be 250 MHz for a 10 MHz input signal bandwidth. Taking only quantization noise into account, the ideal peak SNR is about 90 dB. Fig. 8(a) depicts the system level block diagram of the 4th-order CT modulator using the biquad networks and feedforward branches. In this architecture, the modulator NTF has one pair of non-optimized zeros and another pair of optimized zeros introduced by the first and the second biquad filters, respectively. The modulator architecture utilizes a feedforward path from the modulator input to the adder block implementing the low-distortion architecture. The low-distortion architecture bypasses the input signal term from the loop filter and directly applies it to the summing block. Low distortion topology removes the input signal term from the loop filter relaxing the loop filter design requirements and also makes $\mathrm{STF} = 1$ in the bandwidth. As demonstrated in Fig. 8(b), two different system level scaling techniques are utilized in the proposed modulator topology to optimize the design and relax the modulator complexity. The first scaling technique introduces $\mathrm{G}_1(>1)$ in front of the flash-ADC block and consequently reduces the gain factors in SAB_1, DAC_2 and the direct feedforward path by G_1. This decreases the output swing and GBW requirements of the operational amplifier in SAB_1 [19]. However, decreasing the gain of SAB_1 has a trade-off with either increased resistor or capacitor values used in the first biquad network as illustrated in (3). The second scaling approach is accomplished by amplifying the signal at the input of the quantizer by $\mathrm{G}_2(>1)$ and putting $1/\mathrm{G}_2$ gain attenuation through all the feedforward branches connected to the adder block. This method boosts the adder block's feedback factor to reduce both the power consumption and the capacitor area in the summing block. Another advantage of the second scaling technique is that a larger amplitude input signal can be applied to the modulator front-end to enhance the ADC dynamic range. To implement the gain factor of $\mathrm{G}_1 \cdot \mathrm{G}_2$ after the adder block, the most power efficient way is shrinking the flash-ADC reference voltages by $1/(\mathrm{G}_1 \cdot \mathrm{G}_2)$. Consequently, scaling down the quantizer reference increases the complexity in the design of the quantizer comparators. So, the optimum value of $\mathrm{G}_1 \cdot \mathrm{G}_2$ is chosen as a trade off

TABLE II
MODULATOR GAIN COEFFICIENTS

Gain	Value
a_1	3
a_2	0.63
a_3	0.63
k_1	2.36
k_2	0.32
h_1	1
h_2	2
b_0	0.32
c_0	0.45
G_1	2
G_2	1.5
ω_p	0.21

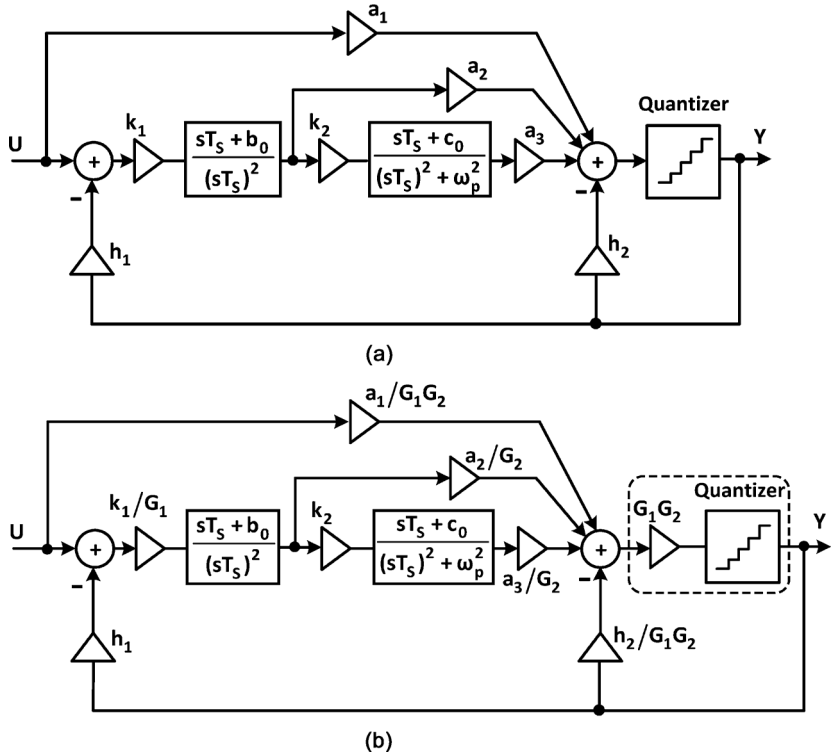

Fig. 8. Proposed 4th-order SAB based CT modulator architecture (a) without gain scaling (b) with gain scaling techniques.

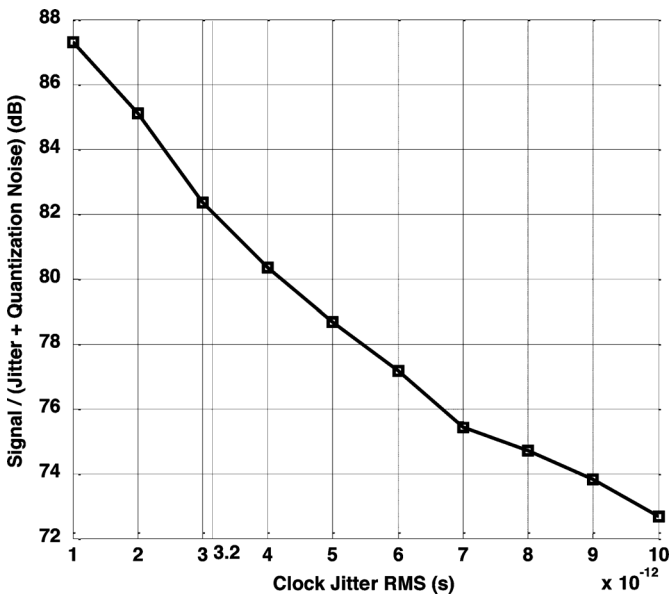

Fig. 9. SNR vs. sensitivity to clock jitter.

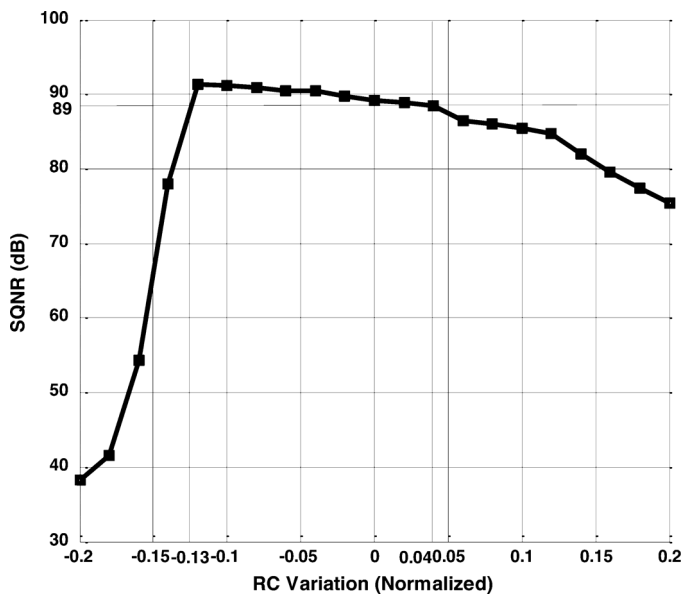

Fig. 10. SNR (-1.5 dBFS input) vs. the normalized time constant.

for which SAB_1 and the adder blocks have relaxed opamp requirements and comparators do not have increased circuit complexity. Table II shows all the gain coefficients of the proposed modulator for optimum gain scaling.

B. Clock Jitter Sensitivity

The clock jitter is one of the design challenges for a CT modulator and also a dominant factor in the design of the front-order DAC block. That is because the non-idealities of the front-end DAC such as clock jitter are not attenuated by the order of the modulator. This is unlike the jitter noise introduced in the SC adder and the second DAC, which will be shaped by the modulator loop filter. Jitter sensitivity of a CT A/D modulator is also determined by the front-end DAC pulse choice. In this design, a non-return-to-zero (NRZ) DAC pulse shape is chosen mainly for its low sensitivity to clock jitter. An approximate equation, which expresses the signal-to-jitter noise ratio of a CT $\Delta\Sigma$ modulator, is:

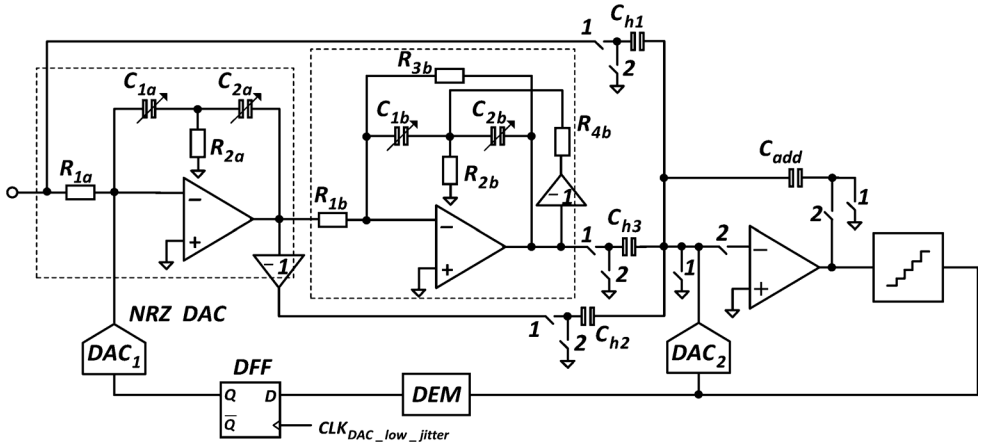

Fig. 11. Block diagram of the proposed 4th-order ΔΣ ADC.

$$\mathrm{SNR_{jitter}} = \frac{\mathrm{P_s}}{\mathrm{P_{jitter}}} = \frac{\mathrm{A}^2/2}{\sigma^2 \mathrm{e_{NRZ}/OSR}} = \frac{\mathrm{OSR}\cdot \mathrm{A}^2}{2\sigma^2_{\Delta \mathrm{y,NRZ}} \left(\frac{\sigma_{\Delta \mathrm{t}}}{\mathrm{T}}\right)^2} \tag{11}$$

where A is the sinusoidal input signal amplitude, OSR is the oversampling ratio, T is the sampling clock period, $\sigma_{\Delta \mathrm{t}}$ is the clock jitter standard deviation, and $\sigma_{\Delta \mathrm{y,NRZ}}$ is the standard deviation of the adjacent modulator output difference [20].

The NRZ DAC pulse will result in reduction of the jitter sensitivity because of the lower value of $\sigma_{\Delta \mathrm{y,NRZ}}$. Fig. 9 shows the simulated SNDR for -1.5 dBFS input for different clock jitter rms values. It should be noted that the simulations include both the quantization noise and the jitter noise. To ensure that the total power of the quantization noise and the jitter noise is 82 dB below the input signal power, the clock jitter rms value must be less than 3.2 ps, placing a very stringent requirement on the clock signal generator.

C. Loop Filter Coefficient Variations

One of the major disadvantages of CT modulators is the large time constant variations compared to DT modulators and thus careful examination at the system level is needed. A worse case simulation is shown in Figs. 10 where the RC time constants in the two SAB networks are assumed to vary by the same percentage.

As shown in Fig. 10, when the time constants, i.e., the products of resistors and capacitors, become smaller than their nominal values, the integrator gains increase and the SNR improves. However, when the time constants decrease by more than -13% of their nominal values, the SNR decreases and the modulator becomes unstable due to excessive loop gain. On the other hand, if the time constants are larger than their nominal values, the loop gain decreases so that the noise shaping is less efficient; as a result, SNDR drops gradually. From Fig. 10, we see that for time constants in the range of -13% and 4%, the modulator can achieve more than 89 dB SNDR for -1.5 dBFS input. To extend the tolerable time constant variation, the loop filter coefficients are centered at -8% of the nominal time constant. By doing this, the time constants can vary by almost $\pm 8\%$ without significantly degrading SNR. As a result, some non-ideal effects such as component mismatch and temperature or changing the modulator gain factors can be tolerable if they are well limited to this range. Since it is not uncommon for the RC time constants to vary by $\pm 25\%$, on-chip tuning is incorporated.

IV. Circuit Realization of the Proposed CT ΔΣ ADC

Fig. 11 illustrates the configuration of the proposed fourth-order CT ΔΣ ADC. Single-opamp biquad filters are embedded for low power operation. The circuit implementation details of all the important building blocks of the modulator are discussed next.

A. Loop Filter

The fourth-order loop filter of this design is implemented with a single-stage, dual-loop CIFF (Chain of Integrators with Feed-Forward branches) architecture, as shown in Fig. 11. The loop filter consists of two SAB networks to implement the modulator NTF. The first SAB $(\mathrm{SAB_1})$ realizes the non-optimized zeros of NTF and the second SAB network resonates at the frequency of the NTF optimized zeros.$\mathrm{SAB_1}$ is located at the ADC front-end; hence, it has less resistors compared to $\mathrm{SAB_2}$, and it results in lower input referred thermal noise. In Fig. 6, the thermal noise introduced by $\mathrm{R_2}$ and $\mathrm{R_4}$ is attenuated by first-order noise shaping since the signal TF from the input to$\mathrm{V_X}$ has a first-order integration factor. Consequently, the main thermal noise contributors are $\mathrm{R_1}$ and $\mathrm{R_3}$. The total input referred thermal noise PSD coming from these two resistors is:

$$\mathrm{V^2_{n,total,in}(f)} \approx \mathrm{V^2_{n,R_1}} + \mathrm{V^2_{n,R_3}} = 4\mathrm{KTR_1}\left(1 + \frac{\mathrm{R_1}}{\mathrm{R_3}}\right)\Delta \mathrm{f} \tag{12}$$

This illustrates that placing $\mathrm{SAB_1}$ at the ADC front-end will reduce the total input referred thermal noise PSD. Fig. 12 depicts the magnitude and the phase response of the loop filter considering the finite gain and bandwidth effects of two SAB amplifiers. As shown in Fig. 12, the peaking close to the signal bandwidth is created by the $\mathrm{SAB_2}$ resonating poles while the other magnitude peaking at the lower frequency is caused by the opamp finite gain effect in $\mathrm{SAB_1}$. This desirable effect automatically moves the non-optimized NTF zeros from the origin on the unit circle in the z-domain. Finite gain effects in the $\mathrm{SAB_1}$ signal TF are:

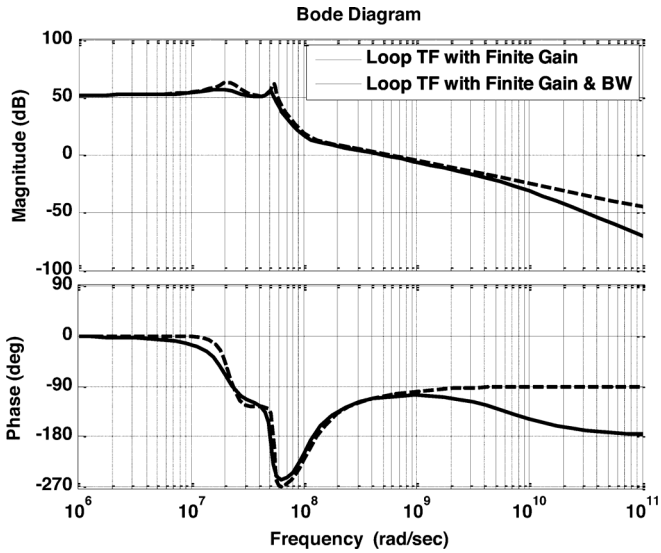

Fig. 12. Frequency response of the SAB base loop filter.

$$\frac{V_{out}}{V_{in}} = \frac{-\frac{1}{R_1}\left[(C_1+C_2)s+\frac{1}{R_2}\right]}{C_1C_2\left(1+\frac{1}{A}\right)s^2+\left\{\frac{C_1}{R_2A}+\frac{(C_1+C_2)}{R_1A}\right\}s+\frac{1}{R_1R_2A}} \quad (13)$$

This shows how the finite gain transfers the TF poles originally located at DC to a pair of complex poles.

Fig. 13 depicts the effect of the SAB_1 finite gain on the loop filter bode plot and also its pole-zero location. By decreasing the finite gain of SAB_1 from 60 dB to 40 dB, its TF poles are moved towards the RHP and also exhibit higher resonant frequencies.

Unlike the DT A/D modulator where the loop coefficients are determined by capacitor ratios and can be as accurate as 0.1%, the loop coefficients in CT A/D modulators are determined by products of resistor and capacitor values which can vary by as much as 25% in today's CMOS processes. In this design, integration capacitors in all integrators are realized by an adjustable capacitor array as shown in Fig. 14 [15]. The capacitors in the arrays are binary-weighted except the "always-in-use" capacitors. This sizing method provides constant tuning steps with the least number of capacitors. The 5-bit digital control codes are fed externally to choose which capacitors to use.

The value of C_P and C_U are chosen such that $(C_P + 8C_U)$ equals the nominal value of the integration capacitor. The ratio between C_P and C_U is chosen to be 24, thus, the tuning range and tuning accuracy are 2.3 and 3.1%, respectively which are shown in (14) and (15). This is enough to meet the requirements for the gain coefficient variation according to simulation results shown in Fig. 9.

$$(\text{Tuning Range})\ m = \frac{C_{MAX}}{C_{MIN}} = \frac{C_p + 31C_U}{C_p} = 2.3 \quad (14)$$

$$(\text{Tuning Accuracy})\ P = \frac{C_U}{C_P + 8C_U} = 3.1\% \quad (15)$$

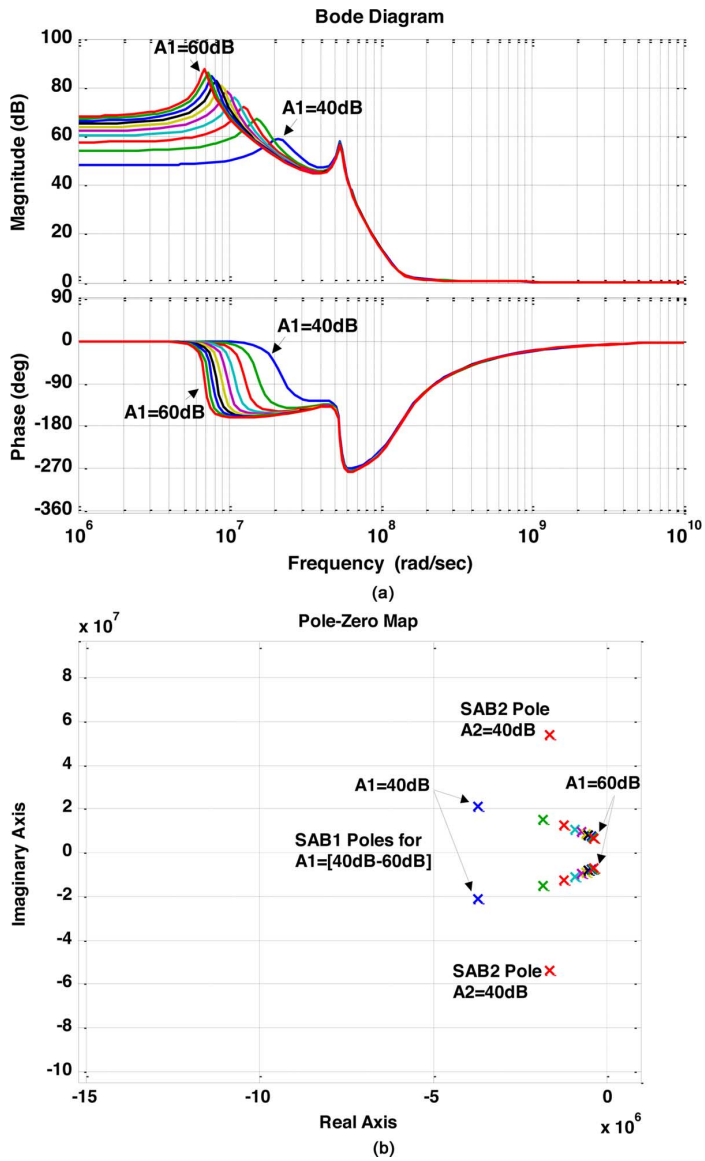

Fig. 13. (a) Bode plot and (b) pole-zero location of the modulator loop filter for different SAB_1 finite gain values.

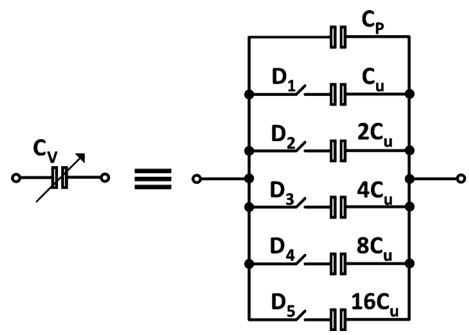

Fig. 14. Tunable capacitor array.

The nominal capacitor value is not centered at the mid tuning range since it is $C_P + 8C_U = 32C_U$. In the process used for this design, 3-sigma process variations of the utilized capacitors and resistors for the properly sized components are less than 10% and 15%, respectively. So, the lower range of the tuning block covers the total RC product variations of +25% at the slow case,

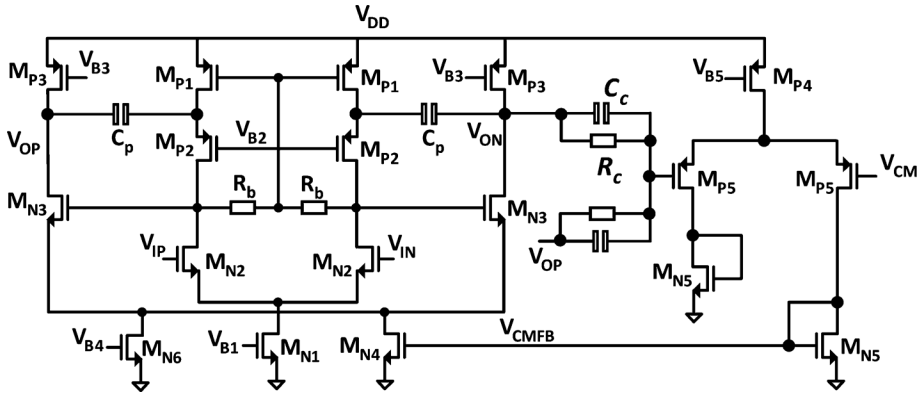

Fig. 15. Two-stage amplifier with cascode compensation utilized in SAB_1 network.

TABLE III
SPECIFICATION TABLE OF THE AMPLIFIERS

Amplifier	Type	Gain(dB)	Gain BW (Hz)	Cap Load (pF)	Current (mA)
1st SAB	Two-Stage	50	$3.5xf_{CK}$	3.5	4.5
2nd SAB	Telescopic	35	$1.5xf_{CK}$	1.2	1.3
Adder	Telescopic	50	$2.5xf_{CK}$	1	1.4

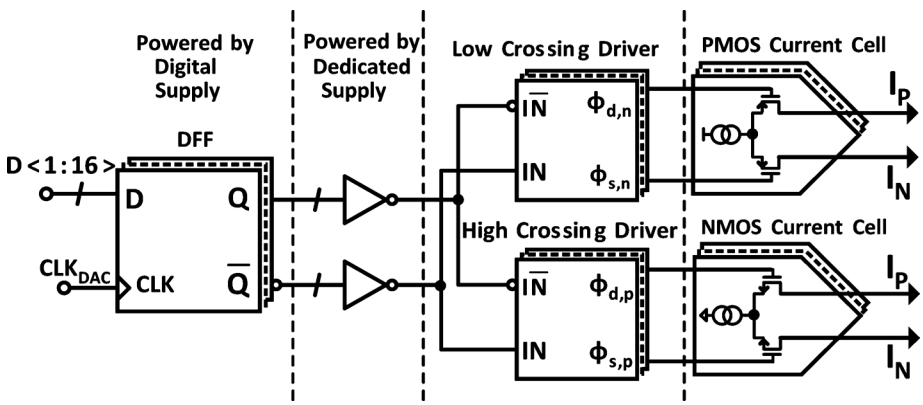

Fig. 16. Front-end feedback DAC block of the CT ΔΣ ADC.

but the higher range covers up to -72% of time constant variations. Since the RC product variations at the fast case will not be more that -25% of its nominal value, the rest of the tuning range on the higher side $(-72\% + 25\% = -47\%)$ is left as a margin for the modulator to be able to operate at lower clock rates (as low as 140 MHz).

Input resistors of the first SAB network play a critical role in defining the total input-referred thermal noise of the modulator. Therefore by choosing a smaller resistance, larger capacitors are required in the front-end SAB filter. To achieve sufficient resistive and capacitive load drivability with higher voltage swing, a two-stage amplifier topology is employed in SAB_1. The amplifier schematic is shown in Fig. 15. The first stage of the amplifier is a telescopic circuit, providing most of the DC gain. The second stage is a simple 5-transistor amplifier with an nMOS input differential pair instead of a common-source pair with pMOS loads. This will make the biasing of the second stage almost independent from the first stage. The second stage has minimal voltage gain, but can drive the resistive load from

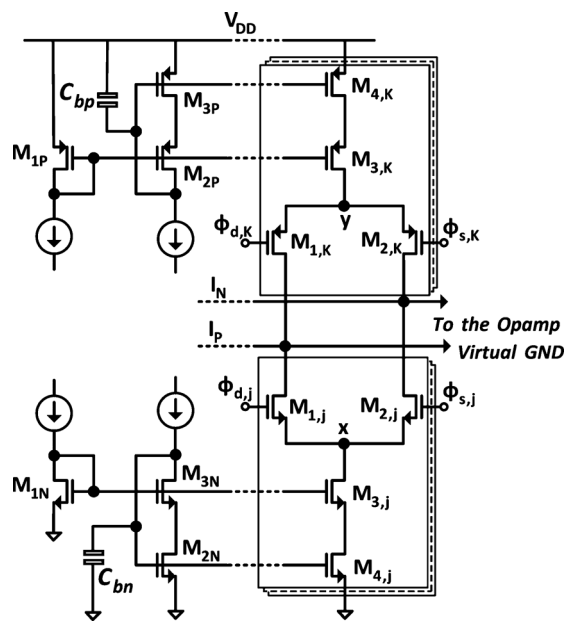

Fig. 17. P-type and n-type full-bridge current steering DAC.

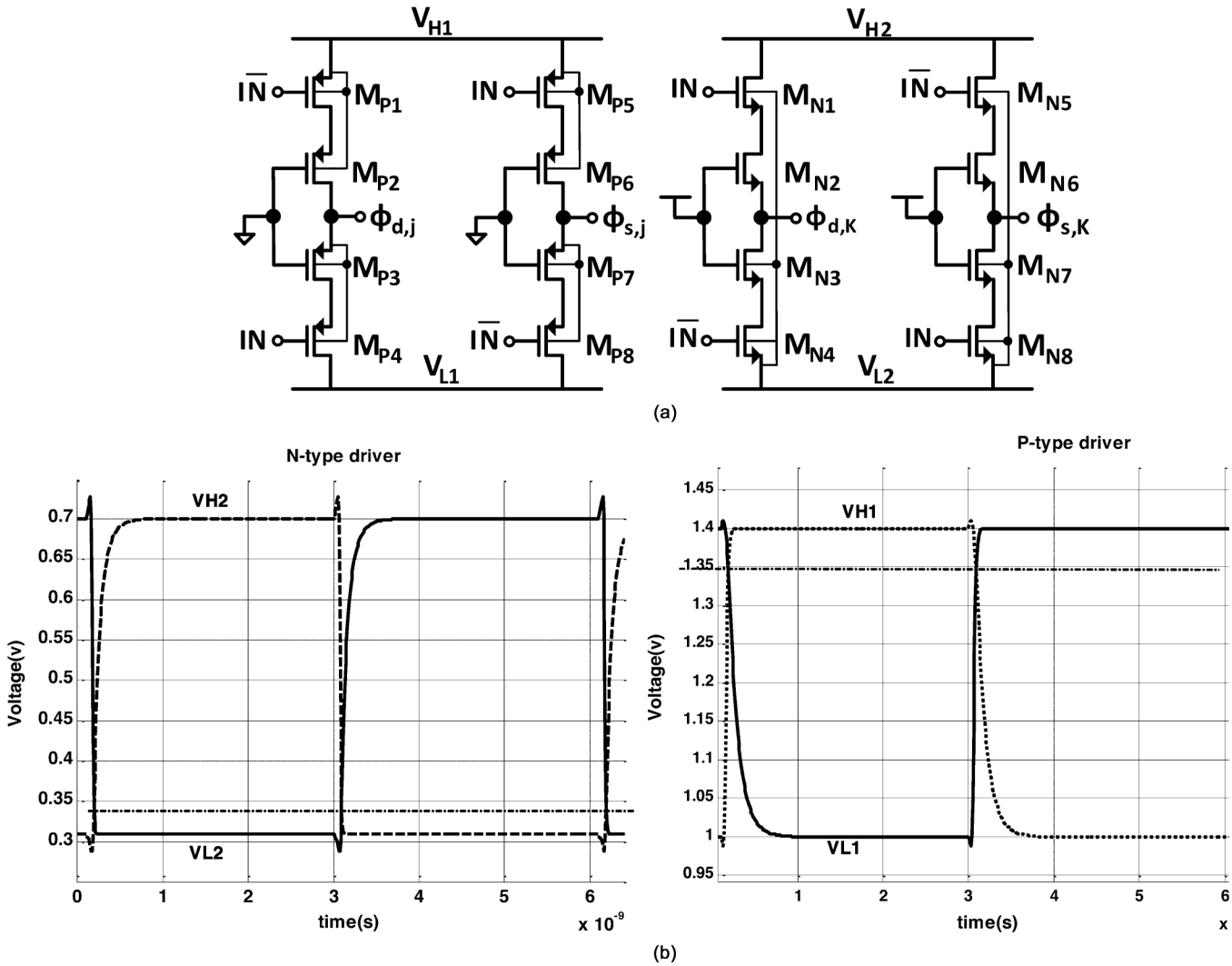

Fig. 18. (a) Circuit diagram and (b) timing diagram of the low-swing high-crossing p-type and low-swing low-crossing n-type voltage limiters.

$\mathrm{SAB_2}$, common-mode sensing resistors and the amplifier load. The CT integrator amplifier employs cascode-compensation instead of the miller-compensation because it reuses the first stage to realize the compensation resistor without consuming extra power and area. The output common-mode (CM) voltage is then sensed by resistor $\mathrm{R_c}$. With the common-mode feedback circuit, the integrator output common-mode voltage is set to a reference voltage $\mathrm{V_{CM}}$. The capacitor $\mathrm{C_c}$ in parallel with $\mathrm{R_c}$ is used to improve the amplifier phase margin by putting a left-half-plane (LHP) zero in the amplifier TF. For the first stage of the amplifier, the resistor $\mathrm{R_b}$ acts as the common-mode detector, which feeds back the sensed CM voltage directly to transistor $\mathrm{M_{P1}}$. A simple single-stage telescopic amplifier is used in the second SAB filter and the summing block. While these two blocks have lower swing requirements due to the low distortion architecture and reduced resistive and capacitive loads, because of the noise scaling in the loop filter, there is no need for the two-stage amplifier. The performance specifications of the CT amplifiers are summarized in Table III. For a nominal sampling frequency of 250 MHz, the CT SAB amplifier unity-gain frequencies are relatively low.

B. Feedback DAC

The CT switched-current-source DAC outputs drive the virtual ground nodes of the CT integrators. Each DAC unit element comprises three separate circuits: a retiming DFF, low-swing high-crossing pMOS and low-swing low-crossing nMOS drivers, and n-type and p-type switched-current sources as shown in Fig. 16.

Fig. 17 depicts the circuit diagram of the current feedback DAC and its biasing circuit. Capacitors $\mathrm{C_{bp}}$ and $\mathrm{C_{bn}}$ are used to filter out the noise from the reference current biasing circuits. There are 16 identical unit-cells for the $\mathrm{I_{DAC}}$. In each unit cell, the cascode transistor is used to increase the output resistance of the current mirror. The current source devices $\mathrm{M_{4,j}}$ and $\mathrm{M_{4,k}}$ are sized to achieve approximately 0.1% matching (10-bit accuracy) according to (16) where $\mathrm{A_\beta}$ and $\mathrm{A_{VTH}}$ are process dependent coefficients.

$$\mathrm{W \cdot L} > \frac{\mathrm{A^2} + \dfrac{4\mathrm{A_{VTH}^2}}{\left(\mathrm{V_{GS}} - \mathrm{V_{TH}}\right)^2}}{\left(\dfrac{\sigma_\mathrm{I}}{\mathrm{I}}\right)^2} \tag{16}$$

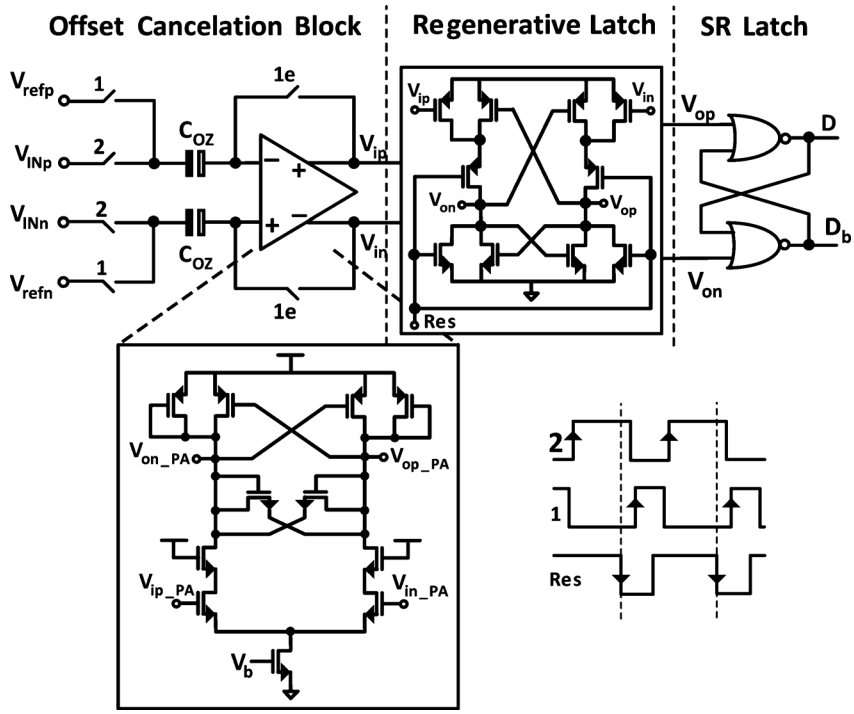

Fig. 19. Circuit diagram of the comparator including its timing diagram.

However, a DEM block is used to improve the initial matching accuracy of the first DAC block from 10-bit to around 14-bit by averaging and first-order shaping the DAC unit mismatches. The DEM block improves the $\mathrm{I_{DAC}}$ linearity by only 4-bit since the design has low OSR. One of the DAC design issues to address is the glitch generated when $\mathrm{M_{1,2,j}}$ or $\mathrm{M_{1,2,k}}$ are turned off. This glitch can cause a long settling time of the output current. The delay and the shape deviation from its ideal output current will change the transfer function of the DAC. As a consequence, the modulator performance may be degraded. Full pMOS low-swing, high-crossing and full nMOS low-swing, low-crossing generators are used in this modulator to convert full-swing and middle-crossing to low-swing, high-crossing digital signals for the n-type switching current source, and low-swing, low-crossing digital signal for the p-type switching current source as shown in Fig. 18(a) [15], [23]. A low-swing digital input can reduce clock feed-through and high crossing and low crossing can prevent the n-type and p-type current switches, respectively, from turning off simultaneously to minimize glitch energy. Fig. 18(b) depicts the timing diagram of the low-swing high-crossing p-type and low-swing low-crossing n-type voltage limiters. In these voltage limiter blocks, the relative sizes of the transistors in the stacks determine the crossing point and rising and falling time of the outputs.

The second DAC is implemented using a SC scheme since the adder block is also SC. The matching requirement on this DAC is more relaxed since its non-linearity will be 4th-order shaped. Thus, the unit capacitor used in SC DAC is the smallest metal-to-metal capacitor available in the process to save power and area. In the SC adder, the FF branch and the feedback DAC coefficients are well define by the ratio of the capacitors, which reduces the input signal leakage into the loop filter and also keeps STF close to the desired one. SC DAC uses analog supply and also ground as its voltage references, which are provided off-chip.

C. Modulator Front-End Device Noise Analysis

The device noise at the modulator front-end limits the noise performance of the modulator. There are three sources of noise at the front-end; 1) noise of the input resistors, 2) noise of the telescopic opamp, 3) noise of the current-steering $\mathrm{DAC_1}$. The input referred thermal noise coming from each of three noise sources is illustrated in (17), (18), and (19). In (18), there are assumptions that both n-type and p-type current DACs have the same full-scale current values ($\mathrm{I_{DAC,P}} = \mathrm{I_{DAC,N}}$) and the same over-drive voltage ($\mathrm{V_{OD,P}} = \mathrm{V_{OD,N}}$) for the tail current main device, $\mathrm{M_{4,j}}$ and $\mathrm{M_{4,k}}$. In the input referred thermal noise of the $\mathrm{SAB_1}$ amplifier in (19), it is considered that the noise from the amplifier second stage is attenuated by its first stage gain and also it is assumed that the signal BW is smaller than the unity gain BW of the $\mathrm{SAB_1}$ network.

$$\mathrm{V_{n,Rin}^2} = 8\mathrm{KTR_{in}BW} \tag{17}$$

$$\mathrm{V_{n,DAC}^2} = 8\mathrm{KTR_{in}^2}\gamma\left(\frac{\mathrm{I_{DAC,P}}}{\mathrm{V_{OD,P}}} + \frac{\mathrm{I_{DAC,N}}}{\mathrm{V_{OD,N}}}\right) \times \mathrm{BW} \xrightarrow{(\mathrm{I_{DAC,P}}=\mathrm{I_{DAC,N}})\&(\mathrm{V_{OD,P}}=\mathrm{V_{OD,N}})} \tag{18}$$

$$\mathrm{V_{n,DAC}^2} = 8\mathrm{KTR_{in}^2}\gamma\left(2\cdot\frac{\mathrm{I_{DAC}}}{\mathrm{V_{OD,DAC}}}\right)\mathrm{BW}$$

$$\mathrm{V_{n,OP1}^2} = 8\mathrm{KT}\gamma\left(\frac{1}{\mathrm{g_{m,N2}}} + \frac{\mathrm{g_{m,P1}}}{\mathrm{g_{m,N2}^2}}\right)\mathrm{BW} \tag{19}$$

where K represents the Boltzmann constant, T represents absolute temperature, γ is the MOS noise factor, and BW is the signal bandwidth. In this design, $\mathrm{I_{DAC}} = 1$ mA, $\mathrm{V_{OD,DAC}} = 0.32$ V, $\mathrm{R_{in}} = 680\ \Omega$, $\mathrm{BW} = 10$ MHz, and $\mathrm{g_{m,N2}} = 11\ \mathrm{m}\mho \approx \mathrm{g_{m,P1}}$;

TABLE IV
SUMMARY OF MEASUREMENT RESULTS

Supply Variations	±10% (VDDA=1.2V, VDDD=1.4V)	
Temp. Variations	± 25°C around room temp.	
Sampling Frequency	185MHz	185MHz
Signal BW (MHz)	7.2	10
Fin (MHz)	1	1
SFDR (dB)	83.1	82.4
SNDR (dB)	76.9	71.9
SNR(dB)	78.2	73.4
FOM (pJ/conv.)	0.168	0.21
Input Range (Diff)	2.8 Vp-p	2.8 Vp-p
Power (mW)	11.4(A),2.3(D)	11.4(A),2.3 (D)

substituting these quantities into (20), we obtain an SNR of 90 dB which is almost 6 db below the designated thermal noise budget. This provides enough margins for the second SAB noise (which will be second-order noise shaped by referring to the ADC front-end) and all other non-ideal effects. Simulation in Spectre shows that the input referred in-band device noise due to SAB_1 (including its resistors and the opamp) and DAC_1 is 1.1 nV^2.

$$\mathrm{SNR} = \frac{\mathrm{P_{in}}}{\mathrm{P_n}} = \frac{(2 \cdot \mathrm{R_{in}} \mathrm{I_{DAC}})^2}{2\mathrm{V}^2_{\mathrm{n,total}}} \tag{20}$$

D. Quantizer

The quantizer in the prototype is a 4-bit flash ADC. It comprises 16 differential comparators, with the 16 reference voltages derived from a resistor ladder between the positive and negative reference voltages. The resistor values in the ladder were chosen small enough to ensure settling to within a few mV at the 250 MHz sampling rate. Because the output range of the adder circuit is only one third of the full-scale input range, the reference voltages to the quantizer only span 1/3 of the input full-scale range, that is, $\mathrm{V_{REFP}} = 940$ mV and $\mathrm{V_{REFN}} = 460$ mV. Notice that the resolution of the quantizer is 5.5 bits relative to the modulator's full-scale input range. The comparator circuit used in the 4-bit quantizer, shown in Fig. 19, is based on a regenerative latch [20], [24]. The comparator has a pre-amplifier stage to reduce kick-back noise. In addition, a switched capacitor input offset cancelation technique is adopted to suppress offset from both the pre-amplifier and latch stages. The pre-amplifier is a low gain single-stage amplifier with gain of 15. The two nMOS transistors acting as a limiter in the pre-amplifier can constrain the swing of the pre-amplifier for faster speed. The capacitance of $\mathrm{C_{OZ}}$ must be chosen carefully because this capacitor and its parasitics contribute to the load seen by the sampling and summing circuit. Also, the time constant of this capacitor with the resistive ladder resistance defines the settling time of the offset sampling cycle in the comparator. The regenerative latch outputs are pulled down to zero when the reset signal is high to eliminate the memory effect. When reset goes low, the regenerative latch amplifies the difference at its input to full scale. For a typical 0.13 μm CMOS technology and $\mathrm{C_{OZ}} = 100$ fF, simulations with the sampling circuit show that the overall input-referred offset of the comparator in the worst case is less than a quarter LSB.

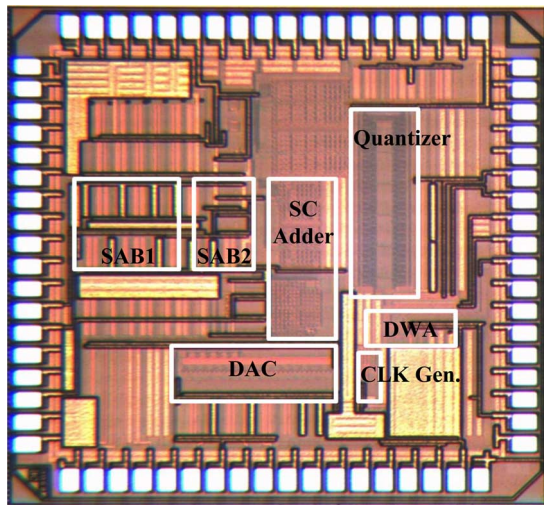

Fig. 20. Chip die microphotograph.

V. MEASUREMENT RESULTS

The proposed CT ADC was fabricated in a 130 nm eight-metal CMOS process. The die microphotograph of the chip is shown in Fig. 20. The ADC active area is 1 mm × 1.3 mm. Minimizing the coupling between digital and analog blocks and reducing offset and parasitic capacitors and resistors are the major considerations for the floor plan. Several commonly used layout techniques were employed, such as common-centroid layout for capacitors and resistors, inter-digitations for transistors, guard rings and shielding. A deep n-well was inserted in DAC_1 between the array of digital control logic and current cells to further reduce the noise coupling. Large decoupling capacitors have been used for supply lines and critical analog DC biasing lines. While all the non-idealities of DAC_1 such as unit cell mismatches will degrade the modulator performance, to decrease the gradient effect all the unit cells have been divided into two portions to be positioned in the common-centroid configuration, which eliminates x-axis and y-axis gradient effects. Fig. 21 illustrates the basic idea of this technique. Two test boards were designed. One board houses the prototype chip, signal generation, and low jitter clock generation circuitry. On the other board are supply voltage generation circuitry, and DC biasing circuitry. The two boards communicate through board-to-board connectors.

Figs. 22 illustrates the measured spectrum (32k FFT) of the modulator output. The input signal and the clock frequency are 1 MHz sine wave with -1.5 dBFS amplitude, and 185 MHz, respectively. The modulator was designed to operate at 250 MHz clock frequency with 10 MHz signal BW but the best performance of the chip prototype was achieved by running the modulator at lower clock frequency (185 MHz). A pulse generator provides the clock signal and its RMS jitter is less than 2.5 ps. The measured peak SNR, peak SNDR and peak spurious-free dynamic range (SFDR) were 78.2 dB, 76.9 dB and 83.1 dB in a 7.2 MHz bandwidth with DEM, respectively. For the 10 MHz signal bandwidth, the measured peak SNR, SNDR, and SFDR were 73.4 dB, 71.9 dB and 82.4 dB. There is no performance degradation having ±10% supply voltage variations

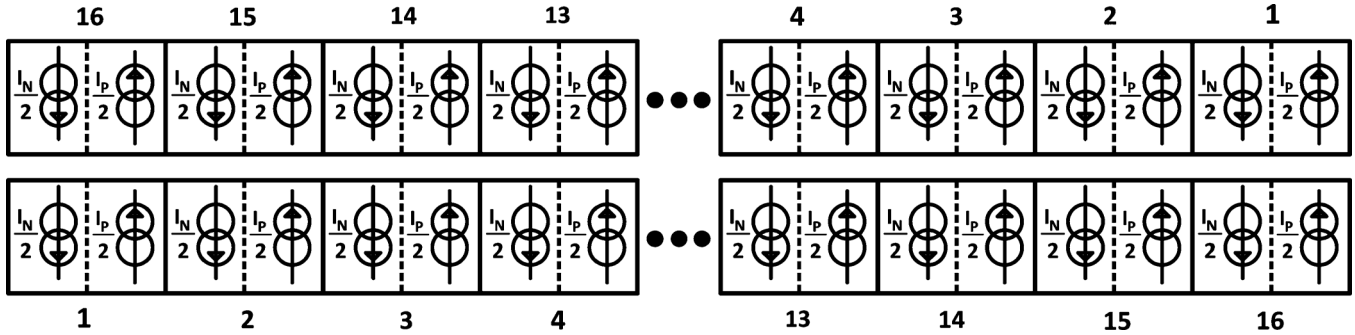

Fig. 21. Common centroid current steering DAC layout.

TABLE V
PERFORMANCE COMPARISON

Reference	Type	Process [μm]	FOM [pJ/conv. Step]
[5] P. Crombez	CT	0.09	0.24
[6] L. Breems	CT-DT	0.18	5.3
[7] R. Schoofs	CT	0.18	0.23
[8] A. Giandomenico	CT	0.13	2.3
[9] K. Reddy	CT	0.18	0.37
[10] E. Prefasi	CT	0.13	0.48
[11] M. Park	CT	0.13	0.33
[12] M. Straayer	CT	0.13	2.07
[13] G. Mitteregger	CT	0.13	0.12
[15] S. Yan	CT	0.5	2.5
[16] T. Song	CT	0.25	0.57
[17] K. Matsukawa	CT	0.13	0.24
[19] S. D. Kulchycki	CT-DT	0.18	2.3
[20] Z. Li	CT	0.25	1.2
[21] P. Malla	DT	0.07	0.27
[22] V. Dhanasekaran	CT	0.065	0.34
[25] E. Prefasi	CT	0.065	0.17
[26] J. G. Kauffman	CT	0.09	0.14
This Work	CT	0.13	0.16

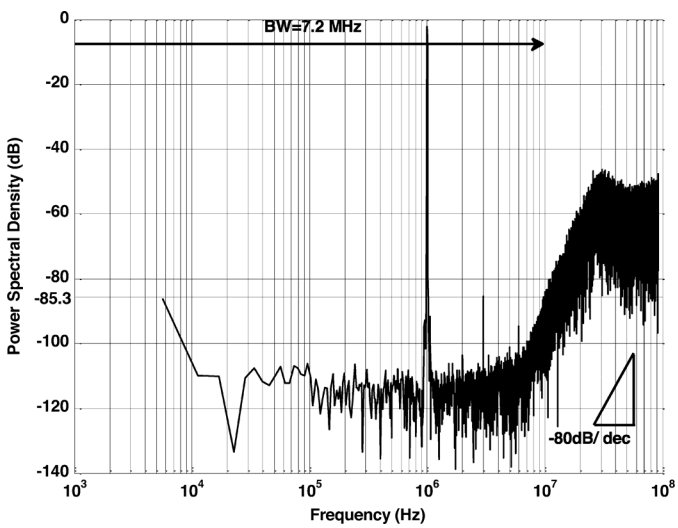

Fig. 22. Measured FFT spectrum.

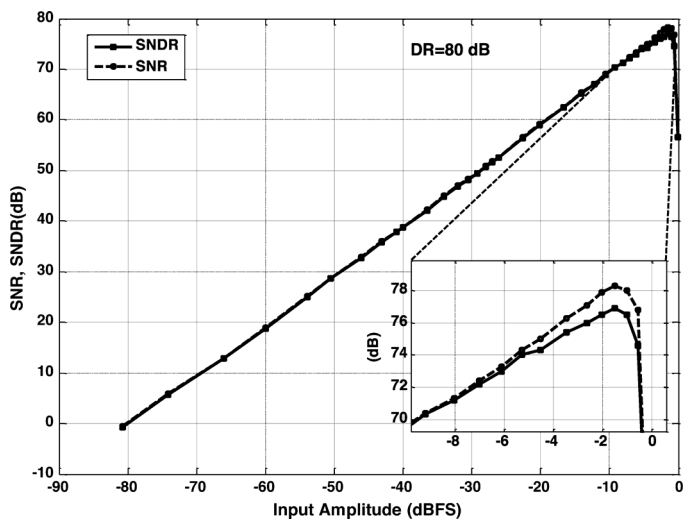

Fig. 23. Measured SNDR, SNR versus input amplitude.

(analog and digital supply voltages are 1.2 V and 1.4 V, respectively) and $\pm 25^{\circ}$C temperature variations around the room temperature. The third-order harmonic distortion (HDs) degrades SNDR, and the noise floor is determined by the thermal noise. Amplitude of the third-order harmonic is around -85.3 dB. It does not change with the input signal frequency revealing that it is coming from the ADC front-end since it does not get noise shaped. Post lay-out simulation indicates that the source of the

3rd-order harmonic is the ADC front-end and specifically it comes from the routing mismatch of the 16-DAC unit elements. The SNDR and SNR plots for varying input signal amplitudes are shown in Figs. 23 for 185 MHz sampling rate and input clock frequency of 1 MHz. The measurement results summarized in Table IV demonstrate the effectiveness of this modulator.

VI. Conclusion

A new power efficient, compact SAB based CT $\Delta\Sigma$ modulator was presented. The proposed modulator utilizes a new SAB network, which reduces the power consumption and die area by reducing the number of active blocks.

Additionally, because the new technique also decreases the feed forward branches to the adder block in the modulator, a switch-capacitor (SC) adder replaces the CT adder and sample and hold blocks used in the conventional architecture. These two techniques make the design and implementation of the high-order continuous-time modulator easier. A 4th-order low pass CT $\Delta\Sigma$ modulator was designed and implemented in 130 nm process to confirm the effectiveness of the proposed techniques. The modulator has achieved SNR, SNDR, and DR of 78.2 dB, 76.8 dB and 80 dB, respectively in a bandwidth of 7.2 MHz, and a FOM of 0.168 pJ/conv.

Table V summarizes a comparison of this design to the recently published works [5]–[12] and [13]–[22]. In this comparison, the FOM is defined as the following (21). Our ADC is ranked as second position.

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2 \cdot \mathrm{Bndwidth} \cdot 2^{\mathrm{ENOB}}}. \tag{21}$$

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