An *I/Q*-Channel Time-Interleaved Bandpass Sigma–Delta Modulator for a Low-IF Receiver

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***Abstract*—This brief proposes a multiplexing scheme to realize an *I/Q*-channel time-interleaved (TI) bandpass sigma–delta modulator that shares operational transconductance amplifiers to minimize power consumption and silicon area for a low-intermediate-frequency (IF) wireless receiver. The test chip was fabricated for a 10.7-MHz IF system with a 0.35-μm CMOS process. The measured peak signal-to-noise distortion ratio for a 200-kHz bandwidth is approximately 73 dB. The power consumption of the fabricated chip is 61 mW with a 3.3-V supply, and the silicon area is 1.78 mm^2. The measured channel crosstalk is about -48 dB.**

***Index Terms*—Bandpass sigma–delta modulator (BPSDM), *I/Q* channel, low-intermediate-frequency (IF) receiver, time interleaved.**

I. Introduction

In WIRELESS communication systems, several receiver topologies have been utilized, such as a heterodyne receiver, a zero-intermediate-frequency (IF) receiver, and a low-IF receiver. Among these topologies, the heterodyne receiver provides the best performance but requires analog blocks that consume considerable power [1]. Recently, the zero-IF receiver provides an efficient design in terms of cost, size, and power. However, it suffers from significant performance degradation due to dc offset and $1/f$ noise [2], [3]. The low-IF receiver is one of the best candidates to overcome the problems in zero-IF receivers [4].

The block diagram of a low-IF receiver can be presented as shown in Fig. 1 [5]. The received radio frequency signal is converted into low-IF in-phase/quadrature-phase (*I/Q*) signals, and then the image signal is suppressed with a complex polyphase bandpass filter. After the complex bandpass filter, the analog I and Q IF signals are converted into digital signals, and the second downconversion to the baseband is performed in the digital domain.

In the low-IF receiver, the analog-to-digital conversion can be performed by two Nyquist analog-to-digital converters (ADCs), by two low-pass sigma–delta ADCs, or by a quadrature bandpass sigma–delta ADC [6]. While the performance requirement for an ADC is relieved as moving to a lower IF frequency, the requirement for an image rejection filter is stricter. Therefore, the choice of the IF frequency is dependent on the tradeoff between image rejection and analog-to-digital conversion.

The bandpass sigma–delta modulator (BPSDM) is classified into continuous-time BPSDMs and discrete-time BPSDMs. The continuous-time BPSDM uses continuous-time noise-shaping filter for high-speed operation with lower power consumption

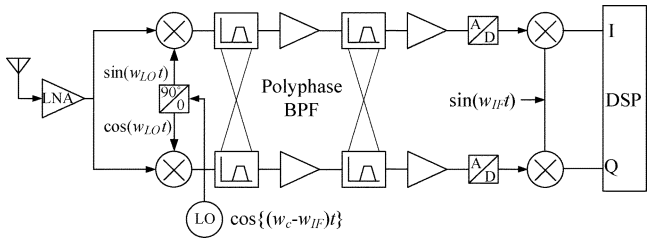

Fig. 1. Block diagram of a low-IF receiver.

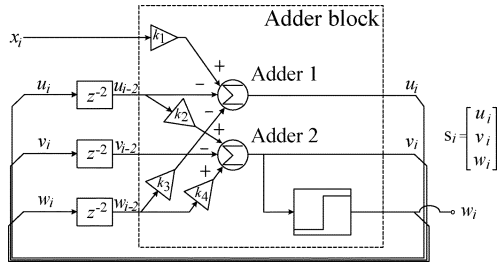

Fig. 2. Modified BPSDM architecture [9].

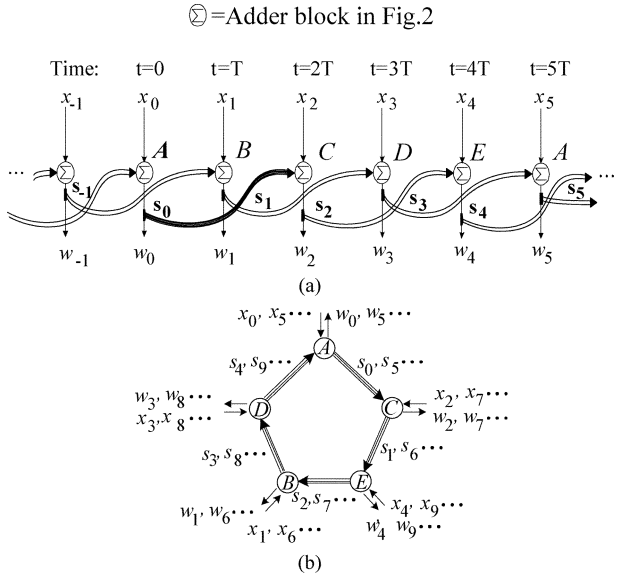

Fig. 3. Architecture of five-stage TI BPSDM. (a) Time unfolded diagram of Fig. 2. (b) Adder-reuse scheme.

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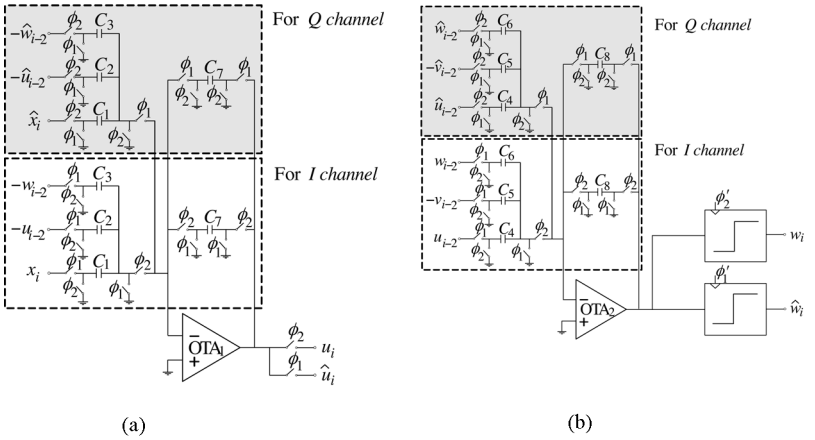

Fig. 4. Simplified circuit diagram of the adder stage for the *I/Q* channel TI BPSDM. (a) Adder 1. (b) Adder 2.

[7]. This approach requires a tuning scheme to set the resonance frequency of the noise-shaping filter to the desired IF frequency. In contrast, discrete-time BPSDMs can be a good candidate. However, the choice of IF frequency is limited due to the slew-rate (SR) limitation of the switched-capacitor (SC) circuits [8]. To overcome this SR limit, a time-interleaved (TI) BPSDM has been introduced in [9].

This brief proposes a multiplexing scheme that realizes an *I/Q*-channel TI BPSDM which reduces power consumption by sharing operational transconductance amplifiers (OTAs) for two modulators. Section II introduces the TI BPSDM, and Section III proposes the *I/Q*-channel TI BPSDM architecture. Section IV shows simulation results. Section V presents the experimental results from the fabricated chip. The conclusion is provided in Section VI.

II. TI BPSDM

The conventional fourth-order BPSDM can be modified to a structure as shown in Fig. 2 by a simple rearrangement of state variable [9]. Then, the state variable $\boldsymbol{s} = [u, v, w]^{\mathrm{T}}$ can be expressed with an iterative equation as follows:

$$\boldsymbol{s_i} = \boldsymbol{A}\boldsymbol{s_{i-2}} + x_i. \tag{1}$$

Here, x_i is the current input and $\boldsymbol{A}$ represents a 3×3 matrix that represents the coefficient $k_1 \sim k_4$ in Fig. 2.

The structure shown in Fig. 2 can be unfolded along time, as shown in Fig. 3(a). Here, T is the sampling period, and the adder block represents the circuits enclosed by the dotted box in Fig. 2. Fig. 3(a) shows that one adder block should hold the result until two clock periods later. Once the adder block C retrieves the signal from the adder block A (bold line in Fig. 3), the adder block A may be reused to perform the addition at 5T. This adder-reuse scheme forms a loop that consists of five adders, as shown in Fig. 3(b). The major advantage of the TI BPSDM is the relaxed SR requirement of the OTA by 1/5. A more detailed explanation about TI BPSDM can be found in [9].

III. Proposed *I/Q*-Channel TI BPSDM

The adder block shown in Fig. 2 can be implemented with SC circuits as shown in Fig. 4. In Fig. 4, for the I channel, all SC

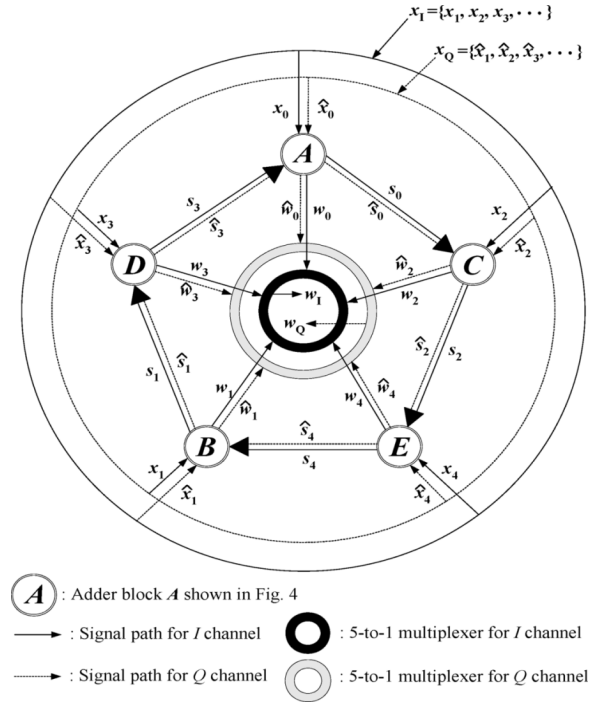

Fig. 5. *I/Q*-channel signal path of the proposed architecture.

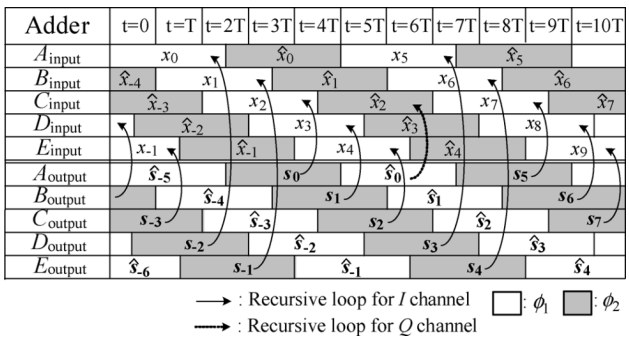

Fig. 6. Input/output signals of adder stages for *I/Q* channels.

circuits sample the input signals at ϕ_1 and transfer the charge to the feedback capacitors $C_{7,8}$ at ϕ_2. The OTAs are completely idle during the ϕ_1 phase. Therefore, the OTAs can be reused to process another channel during the ϕ_1 phase. In other words, the

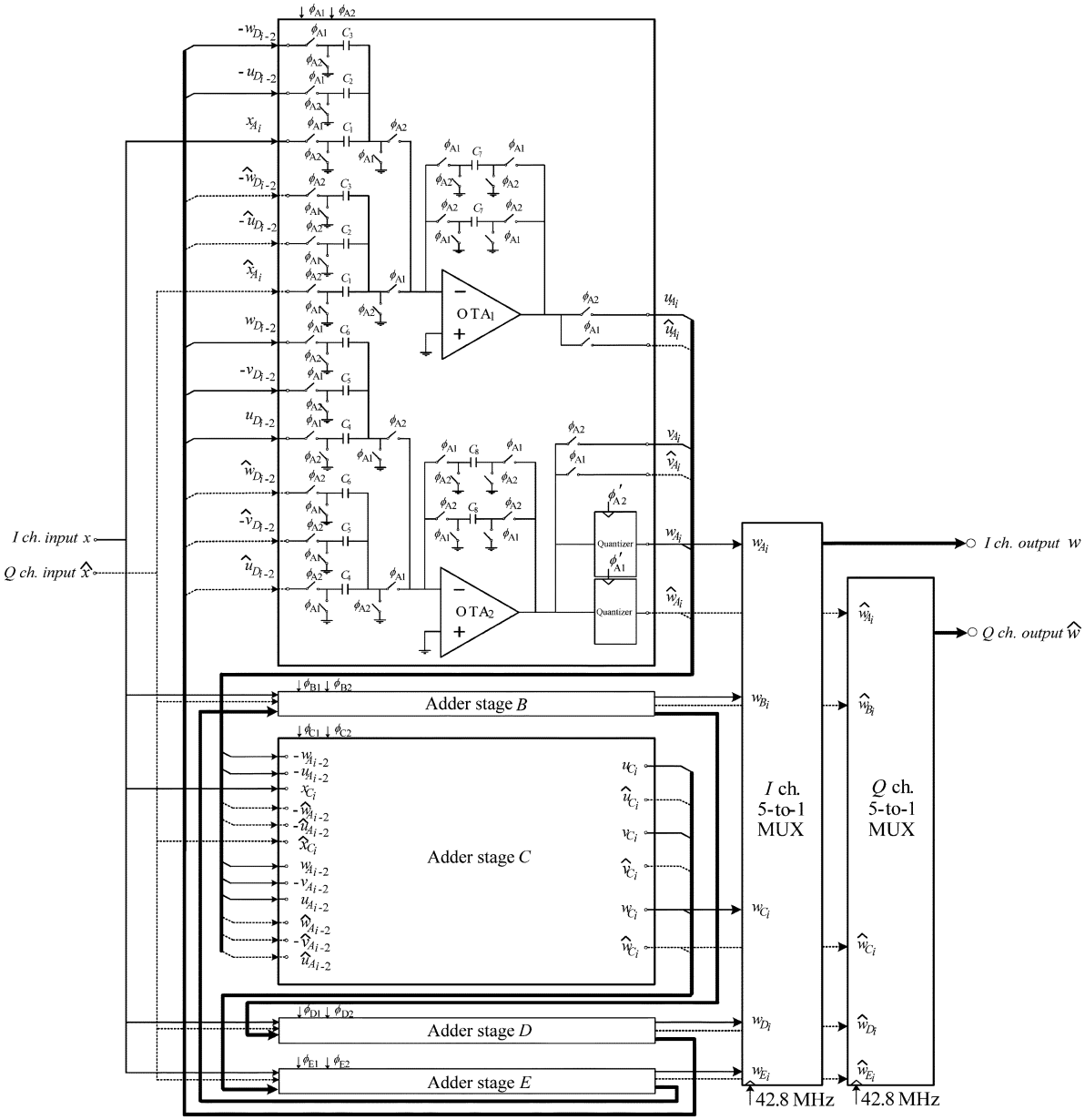

Fig. 7. Proposed *I/Q*-channel TI BPSDM architecture (circuit diagram in each adder block is simplified to a single-ended circuit).

input signals of the I channel are sampled at ϕ_1 and transferred to the feedback capacitors at ϕ_2, while the input signals of the Q channel are sampled at ϕ_2 and transferred to the feedback capacitor at ϕ_1. Two feedback capacitors are reset alternatively. The signals with hats ($\hat{\boldsymbol{x}}$, $\hat{\boldsymbol{u}}$, $\hat{\boldsymbol{v}}$, and $\hat{\boldsymbol{w}}$) represent signals for the Q channel while the others represent signals for the I channel. Here, ϕ_1' and ϕ_2' are the delayed versions of ϕ_1 and ϕ_2 clocks, respectively.

Fig. 5 shows the architecture of the proposed *I/Q*-channel TI BPSDM, which combines the five-stage TI BPSDM and the multiplexing scheme explained in Fig. 4. In Fig. 5, the adder A receives the input signal of the I channel $\boldsymbol{x}_0$ during the ϕ_{1A} phase, and the output $\mathbf{s}_0$ is taken by the adder C at the ϕ_{1C} phase. The output signal $\boldsymbol{w}_0$ is sent to the multiplexer of the I channel during ϕ_{2A}. Here, ϕ_{1A} and ϕ_{2A} are internal clock phases ϕ_1 and ϕ_2 for the adder A, respectively. In contrast to I channel, the adder A receives the input signal of the Q channel at the ϕ_{2A} phase. All clock phases for the Q channel signal are opposite of the clock phases for the I channel. In Fig. 5, the solid lines represent signal paths for the I channel and the dotted lines represent signal paths for the Q channel.

Fig. 6 shows the input and the output of each adder stage along time. Here, the white part and the gray part represent the ϕ_1 phase and the ϕ_2 phase of each adder stage, respectively. The arrow lines represent the signals from an adder stage to the other. Only I-channel signals are shown in Fig. 6 for simplicity. For the Q channel, the adder output at ϕ_1 (the white part in output section) is fed to the corresponding adder input at ϕ_2 (the gray part in the input section). For example, $\hat{\boldsymbol{s}}_0$ from the output of the adder A is fed to the input of the adder C and summed with

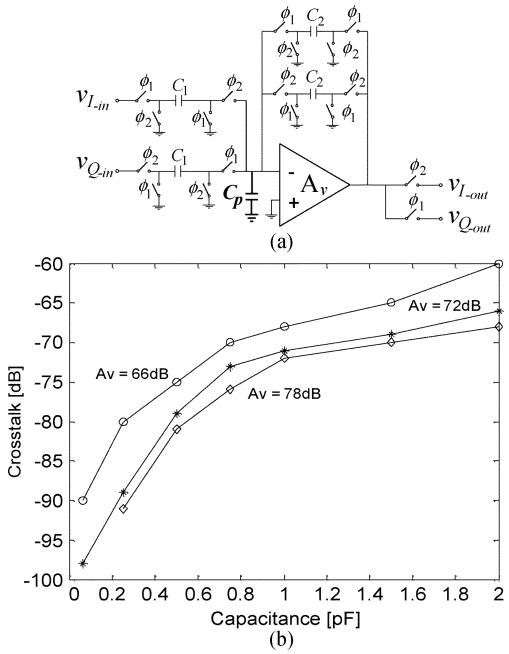

Fig. 8. Simulation results of the adder circuit with parasitic capacitance and finite OTA gain for crosstalk effects. (a) Circuit diagram. (b) Crosstalk effect.

$\hat{\boldsymbol{x}}_2$. Based on Figs. 5 and 6, the *I/Q*-channel TI BPSDM can be implemented with five adder stages which form recursive loops, as shown in Fig. 7.

In Fig. 7, the output of each stage is fed to the input of the adder block of the stage that comes after the next stage. For the I channel, the input signal x is distributed to each stage ($x_{A\mathrm{i}}$, $x_{B\mathrm{i}}$, $x_{C\mathrm{i}}$, $x_{D\mathrm{i}}$, and $x_{E\mathrm{i}}$) and sampled with five-phase sampling clocks (ϕ_{A1}, ϕ_{B1}, ϕ_{C1}, ϕ_{D1}, and ϕ_{E1}) of each stage. Outputs from each stage are selected at the end of ϕ_2 for the I channel and at the end of ϕ_1 for the Q channel in a sequence of $A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow A$.

IV. Simulation Results

The proposed *I/Q*-channel TI BPSDM has been designed for a 10.7-MHz IF system using a 0.35-μm CMOS process. The input frequency is 10.7 MHz, and the clock frequency is 8.56 MHz, while the effective sampling frequency is 42.8 MHz for both channels. A fully differential folded-cascode OTA [10] is designed with open loop gain of 69 dB, gain–bandwidth product of 316 MHz, phase margin of 57°, and SR of 175 $\mathrm{V}/\mu\mathrm{s}$ with a 1.25-pF load capacitor. The capacitor values in the SC adder are 0.25 pF for $C_{1,3,4,6}$ and 0.5 pF for $C_{2,5,7,8}$.

Since two channels share one OTA, there exists inter-channel crosstalk [11]. The major source of the crosstalk is residual charge stored in the input parasitic capacitance of the OTA, as shown in Fig. 8(a). Considering parasitic capacitance C_p and the finite OTA gain A_v, the crosstalk in an adder stage can be obtained as follows:

$$v_{\mathrm{out}}|_{\mathrm{Ich}} = \frac{C_1}{C_2(1-1/A_v)} v_{\mathrm{in}}|_{\mathrm{Ich}} + \frac{C_p}{C_2(1-A_v)} v_{\mathrm{out}}|_{\mathrm{Qch}}. \quad (2)$$

Fig. 8(b) shows the simulated crosstalk of one adder stage. The crosstalk increases as the parasitic capacitance increases. The crosstalk effect of the parasitic capacitance is decreased as the OTA gain increases.

The other major source of the crosstalk is the nonideality of the common-mode feedback (CMFB) circuits. The CMFB samples the output common-mode signal at ϕ_1 and then feeds it back at ϕ_2. Therefore, the common-mode voltages for each channel are not equal. Moreover, the mismatch in the common-mode detector makes it sample some portion of the differential signal, and it is fed to other channel. The simulated crosstalk due to CMFB without mismatch was 10 dB.

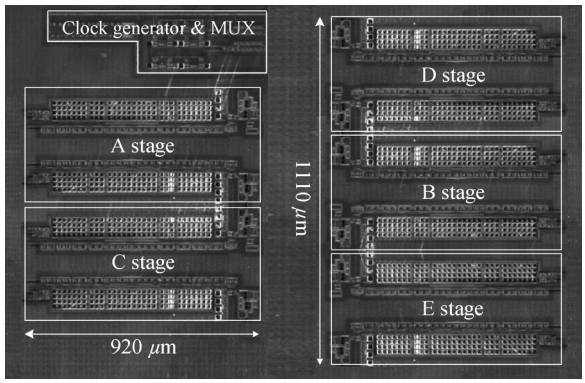

Fig. 9. Microphotograph of the fabricated chip.

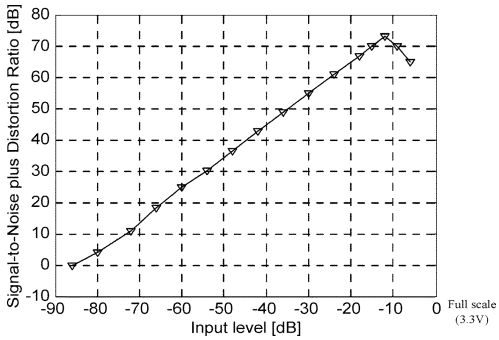

Fig. 10. Input level versus SNDR from the fabricated chip.

V. Experimental Results

The test chip was fabricated with a 0.35-μm CMOS process. Fig. 9 shows the microphotograph of the fabricated chip. In Fig. 9, five stages are placed in the sequence of $A \rightarrow C \rightarrow E \rightarrow B \rightarrow D$. These sequences make the architecture to be performed with the condition of minimum paths for *I/Q*-channel signals of all stage. The total silicon area is 1.78 mm^2.

Fig. 10 shows the measured signal-to-noise distortion ratio (SNDR) with respect to input signal magnitude, and the peak SNDR is 73 dB. Fig. 11 shows the measured I-channel output spectrum when a 10.7-MHz signal is applied for the I channel while a 10.9-MHz signal of same magnitude is applied to the Q channel. The 10.9-MHz signal appears in the output of I channel due to crosstalk. The measured inter-channel crosstalk is -48 dB.

Table I summarizes the performance of the proposed *I/Q*–channel five-stage TI BPSDM along with the ones of the

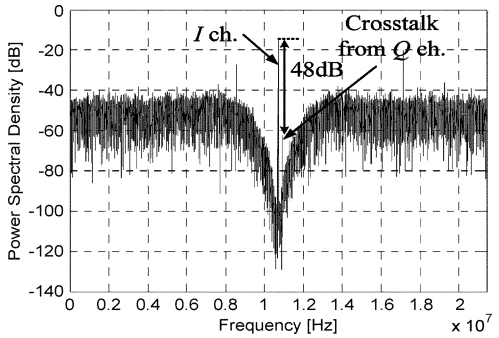

Fig. 11. Measured I-channel output spectrum with crosstalk effect (for $v_{\rm in} = 0.8\ {\rm V}_{p-p}$, $f_{\rm in\_I} = 10.7$ MHz, $f_{\rm in\_Q} = 10.9$ MHz, $f_s = 42.8$ MHz, and $f_{\rm clk} = 8.56$ MHz).

TABLE I
COMPARISON AMONG THE PROPOSED *I/Q*-CHANNEL TI BPSDM AND OTHER BPSDMS

Design	This work	[13]	[14]	[15]
Technology	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.25 μm CMOS
Number of channel	2	1	1	1
Input frequency	10.7 MHz	10.7 MHz	10.7 MHz	10.7 MHz
Effective sampling frequency	42.8 MHz	42.8 MHz	42.8 MHz	42.8 MHz
Clock frequency	8.56 MHz	21.4 MHz	42.8 MHz	7.13 MHz
Signal bandwidth	200 kHz	200 kHz	200 kHz	200 kHz
Order	4	2	6	4
Peak SNDR	73 dB	42.3 dB	61 dB	59.5 dB
Core area	1.78 mm^2	1.3 mm^2	1 mm^2	2.91 mm^2
Power supply	3.3 V	1 V	3.3 V	1 V
Power consumption	61 mW*	12 mW	76 mW	8.45 mW
FOM	141	114	125	133

* includes the clock generator

other reported BPSDMs. It provides the figure-of-merit (FOM) that is defined as follows [12]:

$$\text{FOM} = \text{DR}_{\text{dB}} + 10\log\left(\frac{\text{BW}}{P}\right). \tag{3}$$

Here, DR_{dB}, BW, and P represent the dynamic range, signal bandwidth, and the power consumption per channel, respectively. Although the proposed *I/Q*-channel TI BPSDM occupies a larger area than a conventional BPSDM does, it is smaller than the area for two conventional modulators in [13]–[15].

VI. CONCLUSION

This brief proposed a multiplexing scheme to implement the *I/Q*-channel TI BPSDM as an extension of the five-stage TI BPSDM for a low-IF receiver. The experimental results show 73-dB peak SNDR and −48 dB inter-channel crosstalk. The proposed architecture occupies smaller area and consumes lower power than two conventional modulators. The crosstalk can be improved further with increased OTA gain and reduced input parasitic capacitance.

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