A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With >70 dB SFDR up to 500 MHz

Wei-Hsin Tseng, Chi-Wei Fan, and Jieh-Tsorng Wu, *Senior Member, IEEE*

***Abstract*—A current-steering digital-to-analog converter (DAC) was fabricated using a 90 nm CMOS technology. Its dynamic performance is enhanced by adopting a digital random return-to-zero (DRRZ) operation and a compact current cell design. The DRRZ also facilitates a current-cell background calibration technique that ensures the DAC static linearity. The measured differential nonlinearity (DNL) is 0.5 LSB and the integral nonlinearity (INL) is 1.2 LSB. At 1.25 GS/s sampling rate, the DAC achieves a spurious-free dynamic range (SFDR) better than 70 dB up to 500 MHz input frequency. The DAC occupies an active area of 1100 × 750 μm^2. It consumes a total of 128 mW from a 1.2 V and a 2.5 V supply.**

***Index Terms*—Background calibration, current-steering, D/A converters, digital random return-to-zero (DRRZ), digital-analog conversion, digital-to-analog converter (DAC), return-to-zero (RZ).**

I. Introduction

THE current-steering digital-to-analog converts (DACs) can achieve high sampling rate, and thus are commonly used in generating high-frequency signals [1]–[8]. Fig. 1 shows a generic current-steering DAC. It consists of M equally-weighted current cells. Each current cell contains a current source of I_u output current, a MOSFET pair functioning as a current switch, and a digital latch controlled by a clock CK. The complementary outputs of the latch control the current switch, directing the I_u current to either the R_L load at V_{o1} or the one at V_{o2}. A decoder converts the DAC digital input $D_i[k]$ into M thermometer-code signals $B_j[k]$, where $1 \le j \le M$. We define the $B_j[k]$ signal as a binary value of either $+1$ or -1. Fig. 1 illustrates the DAC differential non-return-to-zero (NRZ) output waveform $V_o = V_{o1} - V_{o2}$. The V_o has a step size of $2I_uR_L$ and a voltage range between $+MI_uR_L$ and $-MI_uR_L$.

The DAC static linearity, specified as differential nonlinearity (DNL) and integral nonlinearity (INL), is mainly determined by the matching of I_u among different current cells and the output resistances of the I_u current sources. The cascode technique is usually used to increase the output resistance of a current source. The dimension of the transistors in the current sources must be large enough to ensure good I_u matching [9]. There are techniques that can relax the device matching requirements, including calibration [10]–[15] and the dynamic element matching [16].

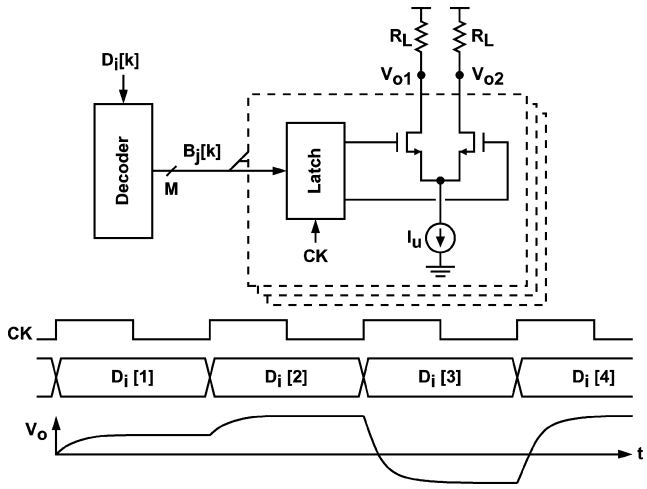

Fig. 1. Current-steering DAC.

Besides static linearity, dynamic performance is also crucial for a high-speed DAC. The DAC dynamic performance is manifested as spurious-free dynamic range (SFDR) degradation shown in the output spectrum of V_o when the $D_i[k]$ input is a single-tone sinewave. As for a DAC with poor dynamic performance, its SFDR decreases rapidly with increasing input frequency. The DAC dynamic performance is related to the switching operation of the internal current switches. It induces the code-dependent switch transient (CDST) effect [17]–[19] and the code-dependent loading variation (CDLV) effect [7], [8], [20], [21].

This paper describes a 12-bit 1.25-GS/s current-steering DAC [22]. We employ the digital random return-to-zero (DRRZ) technique [23] to mitigate the CDST effect and relax the matching requirement for current switches. The DRRZ operation also enables a current-cell background calibration. The calibration relaxes the device matching requirements for the I_u current sources, allowing a more compact design of the current cells. The compact current cell design directly reduces the CDLV effect. The DAC was fabricated using a standard 90 nm CMOS technology. At 1.25 GS/s sampling rate, this DAC chip achieves a SFDR better than 70 dB up to 500 MHz input frequency.

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W.-H. Tseng was with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, and is now with Mediatek Inc., Hsin-Chu, 30078, Taiwan (e-mail: buz.ee91g@nctu.edu.tw).

C.-W. Fan was with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, and is now with Mediatek Inc., Hsin-Chu 30078, Taiwan.

J.-T. Wu is with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu 300, Taiwan.

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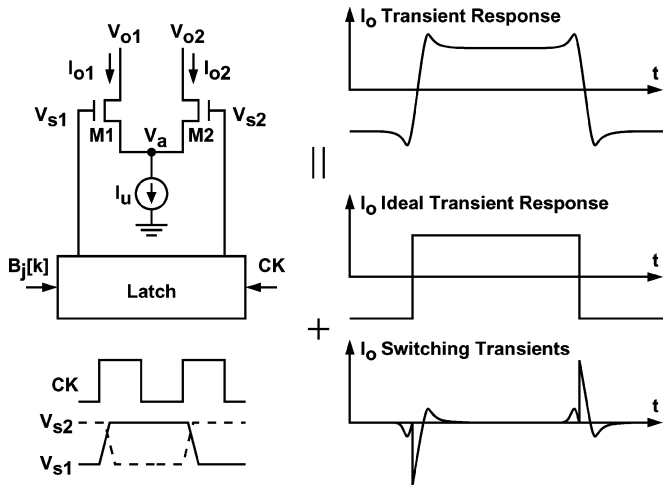

Fig. 2. Code-dependent switching transient (CDST).

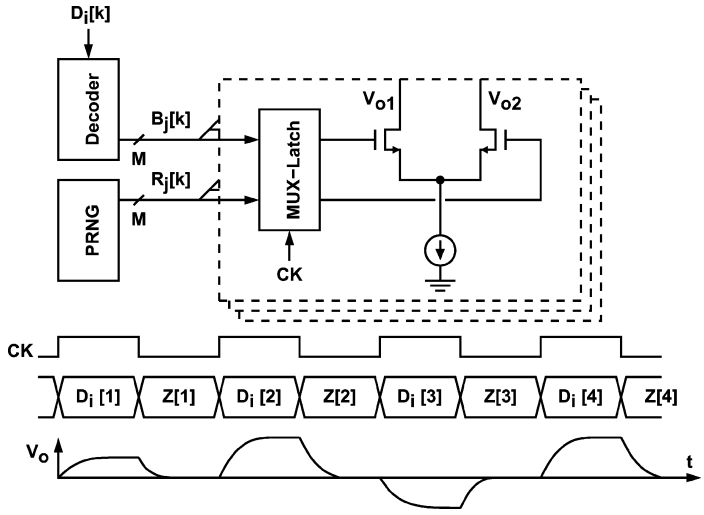

Fig. 3. Digital random return-to-zero (DRRZ) operation.

The rest of this paper is organized as follows. Section II discusses the design considerations for the DAC. Section III describes the DAC architecture and the current cell design. Section IV introduces the proposed current-cell background calibration and its related circuits. Section V shows the experimental results. Section VI draws conclusions. The Appendix analyzes the calibration operation under a finite DAC output-port bandwidth.

II. Design Considerations

Consider the DAC shown in Fig. 1. Its static linearity, as manifested by DNL and INL, is determined by the matching of the I_u current sources among the current cells. Its dynamic performance, as manifested by SFDR versus input frequency, is degraded by the CDST and CDLV effects. In the following subsections, CDST and CDLV are explained. Techniques to mitigate their effects are proposed.

A. Code-Dependent Switching Transient (CDST)

Fig. 2 shows the operation of a single current cell. The current cell contains a current source I_u and a MOSFET current switch M1–M2. Upon the rising edge of clock CK, the binary input $B_j[k]$ is loaded into the latch. Its two complementary outputs, V_{s1} and V_{s2}, drive the current switch, directing the I_u current to either output node V_{o1} or output node V_{o2}. Fig. 2 also shows the transient response of the differential output current $I_o = I_{o1} - I_{o2}$. The output current I_o is a combination of an ideal transient response and switching transients. Switching transients occur only when $B_j[k]$ varies. There are several sources for switching transients [17], including switch feedthrough through the current switch, timing skew of CK, finite rise/fall time of V_{s1} and V_{s2}, and voltage fluctuation at the common-source node V_a.

Current cells exhibit mismatches in switching transients due to 1) device variations in both the current switch and the latch; 2) CK timing skew mismatches among current cells. The I_o switching transients from all current cells are summed up at the DAC V_o port. Depending on the $D_i[k]$ sequence, the summation of the switching transient mismatches becomes a nonlinear term, resulting in harmonic distortions. This is called the code-dependent switching transient (CDST) effect.

To reduce the switching transient mismatch, the V_{s1} and V_{s2} waveforms must be carefully designed. Adding a cascode stage to the current switch is also a common practice to reduce the feedthrough of V_{s1} and V_{s2} to the outputs. Matching among current switches, latches, and CK routes must be considered in the design. Voltage return-to-zero (RZ) techniques [12], [14], [17], [24] or current RZ techniques [4], [5], [16], [25] can hide the switching transients from the DAC output; thus, lessen the CDST effect. Modifying the current-cell switching operation can also mitigate the CDST effect. These techniques decouple the sequence of the switching transients from the input sequence. The switching transients then appear as noise instead of distortions at the DAC output [16], or they become out-of-band signals [2], [26]. Another technique is dynamic-mismatch mapping [27] which optimizes the cell-selecting sequence to minimize the CDST effect without increasing the random noises.

This work employs the digital random return-to-zero (DRRZ) technique [23] to eliminate the CDST effect. The DRRZ randomizes the switching transient sequence by forcing a RZ operation. Fig. 3 shows its operation. When CK is high, the DAC is in the data phase. The DAC decodes the digital input $D_i[k]$, sets up its internal current switches through $B_j[k] \in \{-1, +1\}$, and generates an analog output V_o corresponding to $D_i[k]$. When CK is low, the DAC is in the $Z[k]$ zero phase, in which the DAC arranges its internal current switches in such a way that the output $V_o = 0$. When the DAC is in $Z[k]$ phase, the output current of each current cell is dictated by a binary signal $R_j[k] \in \{-1, +1\}$. A pseudo random number generator (PRNG) generates $R_j[k]$ such that $\sum_{j=1}^{M} R_j[k] = 0$. Due to the insertion of the $Z[k]$ zero phases, the switching transients no longer have $D_i[k]$ dependency, and they no longer induce harmonic distortion [23].

Comparing to other techniques, the overhead of the DRRZ is entirely in the digital domain. The DRRZ arranges the DAC current cells such that the total DAC output current is zero during the $Z[k]$ phases. It does not demand the DAC output voltage V_o returning to zero in every $Z[k]$ phase. The DRRZ randomizes the operations of current switches regardless of V_o. The

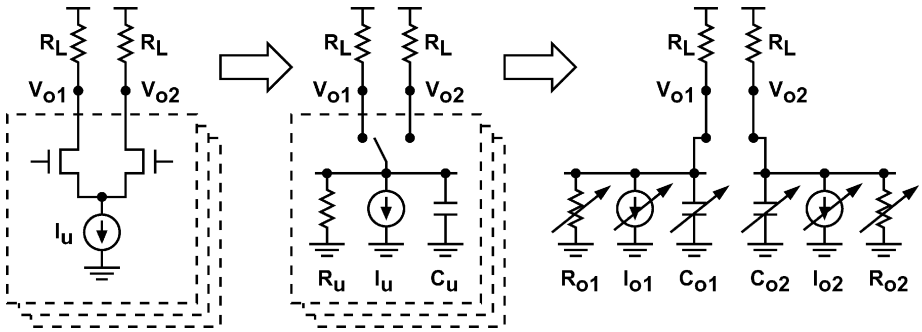

Fig. 4. Code-dependent loading variation (CDLV).

switching transients are not hidden from the output. The resulting sequence of switching transient mismatches appear as random noise instead of distortion at the DAC output.

B. Code-Dependent Loading Variation (CDLV)

Fig. 4 shows another source of harmonic distortion. Each current cell is modeled as an ideal switch on top of an ideal current source I_u in parallel with a resistor R_u and a capacitor C_u. The resistor R_u and capacitor C_u represent the resistance and capacitance variations by looking into one of the current cell output terminal while the current switch switches from one position to the other. Both R_u and C_u are connected to either the V_{o1} node or the V_{o2} node, depending on the state of the switch. As a result, the total loadings for output nodes V_{o1} and V_{o2} vary with digital input $D_i[k]$. This code-dependent loading variation (CDLV) effect introduces harmonic distortion in the differential output $V_o = V_{o1} - V_{o2}$. When $D_i[k]$ is a sinewave, the third-order harmonic distortion caused by the CDLV effect is [7], [8], [20], [21]

$$\mathrm{HD3} = \left[\frac{M}{4} \cdot \frac{R_{L.d}}{|Z_u|}\right]^2 \tag{1}$$

where M is the total number of current cells, $R_{L,d} = 2R_L$ is the differential resistance of the DAC output loads, and Z_u is the output impedance of a single current cell, where $1/Z_u = 1/R_u + j\omega C_u$.

Increasing R_u and reducing C_u can mitigate the CDLV effect. Adding cascode stage to a current source increases R_u. In most high-speed designs, the CDLV effect at high frequencies is dominated by C_u. The C_u capacitance is determined by the device dimensions of the current switch and the current source, while the device dimensions are governed by the matching requirements. The CDLV effect can be mitigated by adding a cascode stage to the current switch in each current cell [3], [7], [28]. Adding constant bias currents to the cascode stage can further reduce the code-dependent effect [7].

For this work, instead of adding additional cascode stages, we simply use smaller devices for both the current sources and the current switches to reduce C_u. Smaller devices lead to larger mismatches. However, due to the use of DRRZ, the matching requirement for the current switches is relaxed. The mismatches among the current sources are corrected by the current-cell background calibration described in Section IV.

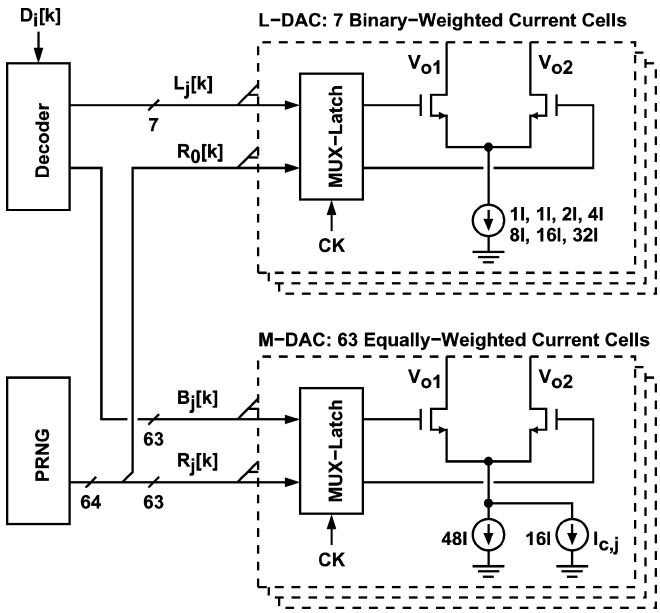

Fig. 5. Segmented 12-bit DAC.

III. DAC Architecture

Fig. 5 shows the 12-bit DAC architecture. The DAC is segmented into a 6-bit equally-weighted MSB DAC (M-DAC) and a 6-bit binary-weighted LSB DAC (L-DAC). The differential output currents from both the M-DAC and the L-DAC are tied together and connected to two external resistive loads R_{L1} and R_{L2} to produce the differential output voltage $V_o = V_{o1} - V_{o2}$. The M-DAC comprises 63 identical current cells. Each current cell is designed to output a nominal current of $64I$, where I is the DAC unit current. The L-DAC comprises 7 current cells which output a current of $1I$, $1I$, $2I$, $4I$, $8I$, $16I$, and $32I$ respectively. There are two $1I$ current cells in the L-DAC so that a differential output of zero can be realized. In our design, $I = 4\ \mu$A. If $R_{L1} = R_{L2} = R_L = 25\ \Omega$, and then V_o has a voltage range of $0.8V_{pp}$.

The DAC employs the DRRZ operation described in Section II-A. As shown in Fig. 5, each current cell contains a multiplexing latch (MUX-Latch). When CK is high, the DAC is in the data phase. The jth M-DAC current cell selects the $B_j[k] \in \{-1, +1\}$ control signal from the D_i decoder, and the jth L-DAC current cell selects the $L_j[k] \in \{-1, +1\}$ control signal. The combination of the equally-weighted $B_j[k]$ and

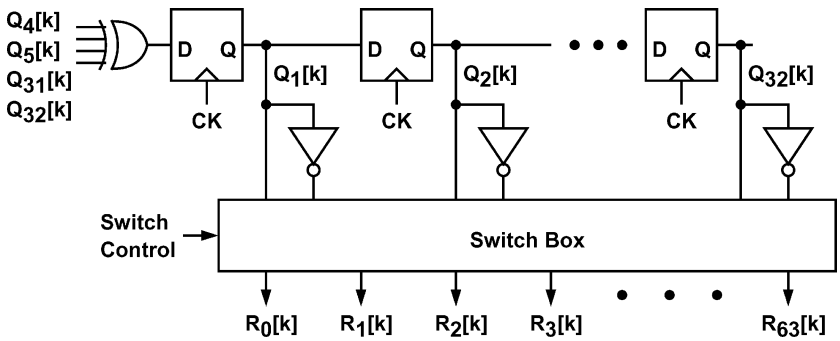

Fig. 6. Pseudo random number generator (PRNG).

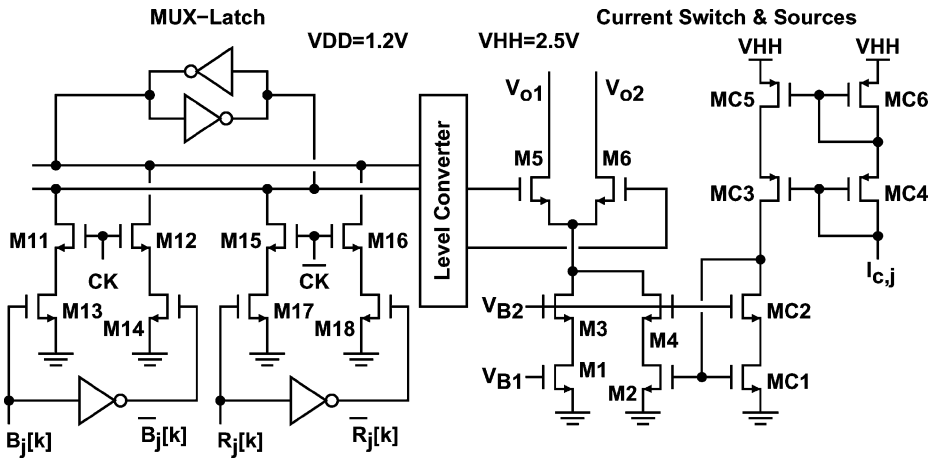

Fig. 7. Schematic of the jth M-DAC current cell.

binary-weighted $L_j[k]$ reflects the value of $D_i[k]$. When CK is low, the DAC is in the $Z[k]$ zero phase. The jth M-DAC current cell selects the $R_j[k] \in \{-1, +1\}$ control signal from a pseudo-random number generator (PRNG). The entire L-DAC is treated as a single MSB current cell. Its current cells select the same $R_0[k]$ control signal. Since $\sum_{j=0}^{63} R_j[k] = 0$, the DAC differential output current is zero during the zero phase.

Fig. 6 shows the PRNG schematic. It is a 32-bit linear feedback shift register. The 32 outputs from the register, $Q_j[k]$ where $j = 1, \ldots, 32$, and their complementary outputs, $\overline{Q}_j[k]$, form the 64 $R_j[k]$ control signals, such that $\sum_{j=0}^{63} R_j[k] = 0$. The switch box shown in Fig. 6 is used to rearrange the connections from $Q_j[k]$ and $\overline{Q}_j[k]$ to $R_j[k]$. The rearrangement is required by the background calibration described in Section IV.

As shown in Fig. 5, there are two separate current sources in each M-DAC current cell. One current source provides an output current of $48I$. The current may vary due to device mismatches. The other current source provides an output current of $I_{c,j}$. The calibration described in Section IV adjusts $I_{c,j}$ so that the total output current of a M-DAC current cell is $64I$.

Fig. 7 shows the circuit schematic of the jth current cell in the M-DAC. MOSFETs M11–M18 and four inverters form a level-sensitive MUX-Latch. When CK is high, the $B_j[k]$ input is loaded into the latch. When CK is low, the $R_j[k]$ input is loaded into the latch. The MUX-Latch is operated under a 1.2 V supply. MOSFETs M5 and M6 together function as a current switch. MOSFETs M1 and M3 form a cascode current source with a fixed current of $48I$. MOSFETs M2 and M4 form another cascode current source whose output current is mirrored from the $I_{c,j}$ current input. Both current sources are operated under a 2.5 V supply. M1–M6 are MOSFETs with thick gate oxide. Device dimensions are listed in Table I. Current mirrors MC1–MC6 are also thick-gate MOSFETs. The level converter shown in Fig. 7 converts the MUX-Latch complementary outputs of 1.2 V swing into signals of 2.5 V swing to drive the M5–M6 current switch. Each signal path in the level converter is a cascade of three inverters. The supply voltage for the last inverter is 2.5 V.

TABLE I
DIMENSIONS OF MOSFETS IN THE M-DAC

	M1	M2	M3	M4	M5	M6
W (μm)	48	16	38.4	12.8	12	12
L (μm)	1	1	0.4	0.4	0.34	0.34

Fig. 8 shows the M-DAC current cell layout. The dimension is $80 \times 15\ \mu\text{m}^2$. From post-layout simulations, we obtain $R_u = 19\ \text{M}\Omega$ and $C_u = 6.3$ fF. Note that M5 and M6 of the current switch are biased in the saturation region when they are turned on. From (1) with $M = 64$ and $R_{L,d} = 50\ \Omega$, the HD3 due to the CDLV effect is less than -70 dB if the input frequency is lower than 560 MHz.

Consider only the M1 and M2 current sources of the current cell shown in Fig. 7. Its total output current I_u exhibits a standard deviation of $\sigma(I_u) = 2.56I$ due to device variation, where I is the LSB current of the DAC. To achieve 12-bit resolution

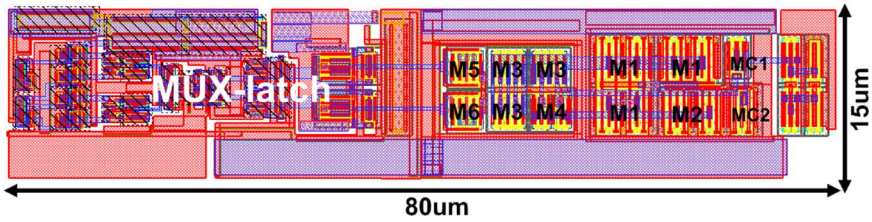

Fig. 8. M-DAC current cell layout.

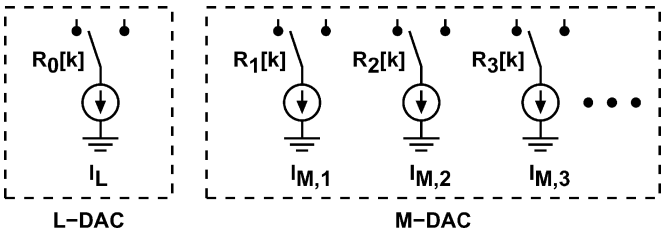

Fig. 9. Zero-phase current-mismatch modulation.

and an INL less than 0.5 LSB, $\sigma(I_u) < 0.125I$ is required. The calibration described in the next section is used to meet the requirement.

IV. Current-Cell Background Calibration

The output current variation of the M-DAC current cell shown in Fig. 7 with the device dimensions listed in Table I does not meet the resolution requirement due to the device variation. In this work, we use background calibration to correct the current variation.

Fig. 9 shows the proposed calibration principle. The total L-DAC current is I_L. There are 63 M-DAC current cells whose currents are $I_{M,1}$ to $I_{M,63}$, respectively. The calibration chooses I_L as a reference and adjusts $I_{M,j}$ to make $I_{M,j} = I_L$, where $j = 1, \ldots, 63$. The M-DAC and the L-DAC execute the regular DRRZ operation described in Section II-A. During the $Z[k]$ zero phase, all M-DAC current cells and the L-DAC are controlled by $R_j[k]$ from the PRNG. The output current of the entire L-DAC is $R_0[k] \times I_L$. The output current of the jth M-DAC current cell is $R_j[k] \times I_{M,j}$. When the jth M-DAC current cell is under calibration, the switch box shown in Fig. 6 rearranges its zero-phase control such that

$$R_j[k] = \overline{R}_0[k]. \tag{2}$$

The DAC total output current in the $Z[k]$ zero phase can be expressed as

$$I_o[k] = R_0[k] \times (I_L - I_{M,j}) + \sum_{i=1, i\neq j}^{63} R_i[k] \times I_{M,i}. \tag{3}$$

The current mismatch $\Delta I_j = I_L - I_{M,j}$ is modulated by $R_0[k]$. The calibration can extract ΔI_j from $I_o[k]$ by using $R_0[k]$ correlation. Once ΔI_j is acquired, it is used to correct $I_{M,j}$. The goal is to make ΔI_j approach zero. The calibration proceeds sequentially. It calibrates all 63 M-DAC one cell at time.

Fig. 10 shows the block diagram of the entire DAC, including its calibration signal path. The differential output currents from both M-DAC and L-DAC are tied together and connected to R_{L1} and R_{L2} to generate the differential output voltage $V_o = V_{o1} - V_{o2}$. When the jth M-DAC current cell is under calibration, the modulated current mismatch $R_0[k] \times \Delta I_j$ is embedded in V_o during the $Z[k]$ zero phase. The DAC output V_o is sampled and processed by a chopper followed by a low-pass filter (LPF) to extract ΔI_j, yielding $V_m = V_{m1} - V_{m2}$. The V_m voltage is digitalized by an incremental delta-sigma modulator (DSM) [29]. The resulting digital code is used to adjust the jth calibration DAC (C-DAC). Its output current $I_{c,j}$ adjusts the jth current cell in the M-DAC, $I_{M,j}$, to make ΔI_j approach zero.

Fig. 11 illustrates various signal waveforms in the calibration signal path. When CK is low, the DAC output voltage V_o during the zero phase is sampled, yielding $V_z = V_{z1} - V_{z2}$. And when CK is high, $V_z = 0$. Voltage V_z is correlated with $R_0[k]$ by a chopper. The output of the chopper can be expressed as $V_p = V_z \times R_0[k]$. A LPF produces the averaged value of V_p, yielding $V_m = 0.5\Delta I_j \times R_L$. A continuous-time DSM is used to digitize V_m. The DSM operates at 1/16 of the CK frequency. It produces an one-bit digital stream $D_s \in \{-1, +1\}$. The decimation filter (DF) following the DSM is an accumulator that dumps its content every 2^{18} D_s samples. The DF output D_m is a digital representation of V_m. The digital code D_m is then scaled into D_a. The value of D_a is $\{0, \pm1, \pm2, \pm4\}$. Fig. 12 shows the D_m-to-D_a mapping function. The D_a is added to the content of the jth accumulator (ACC). There are 63 ACCs. Their outputs, $D_{c,j}$, control 63 calibration DACs (C-DACs) respectively. Each C-DAC is a 7-bit current-steering DAC with a resolution of $I/8$. For the jth C-DAC, its output is $I_{c,j} = D_{c,j} \times I/8$. The current $I_{c,j}$ adjusts the output of the jth M-DAC current cell, $I_{M,j}$.

Fig. 13 shows the schematic of the calibration analog signal path. MOSFETs M1–M4 form the V_o sampler. When CK is high, the V_{z1} and V_{z2} nodes are connected to a common-mode voltage, V_{CM}. MOSFETs M5–M8 form the V_z chopper. The RC pairs, R_{F1}–C_{F1} and R_{F2}–C_{F2}, are the LPFs with a bandwidth of 26.5 kHz. The LPF output, V_m, is converted to current by a transconductor $G_m = 825\ \mu\text{A/V}$, and then integrated by the following DSM. Both the transconductor and the opamp are simple folded-cascode opamps. The DSM is operated at a clock frequency of 78.125 MHz. The internal feedback in the DSM is a one-bit current-steering DAC with an output current of $I_s = 40\ \mu$A. The DSM can resolve a current mismatch ΔI_j as large as $\pm I_s/(R_L G_m) = \pm 242I$. A ΔI_j of $1I$ corresponds to a $D_m = 15$.

The calibration path shown in Fig. 13 includes a transconductor G_m and an opamp. They exhibit offsets due to device mismatches, which introduce errors in the DSM measurements. Assume the 1st M-DAC current cell is under calibration. During

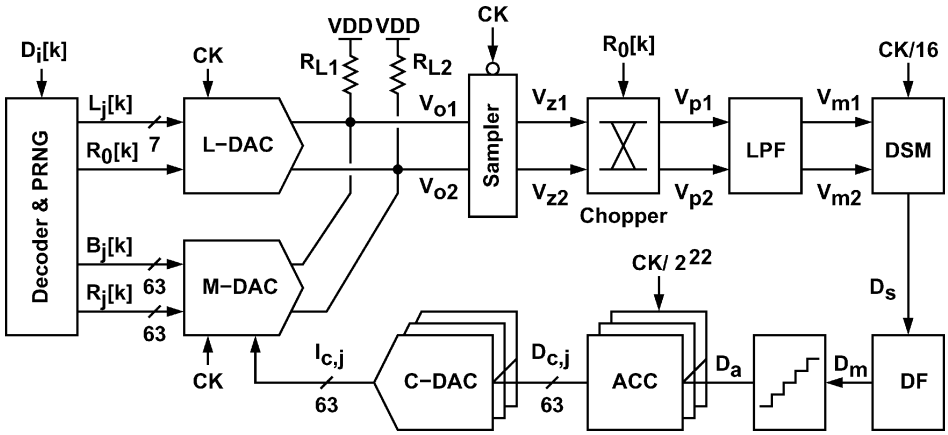

Fig. 10. DAC block diagram.

the $Z[k]$ zero phase, I_L is modulated by $R_0[k]$ and $I_{M,1}$ is modulated by $\overline{R}_0[k]$. Neglecting the DSM conversion gain, the corresponding digital output D_m can be expressed as

$$D_{m1} = +I_L - I_{M,1} + \text{Offset}. \tag{4}$$

The offset must be removed from the measurement data. To find the offset, an additional calibration measurement is performed at the beginning of each calibration cycle. During the $Z[k]$ zero phase of this measurement, I_L is modulated by $\overline{R}_0[k]$ and $I_{M,1}$ is modulated by $R_0[k]$. The resulting digital output D_m can be expressed as

$$D_{m2} = -I_L + I_{M,1} + \text{Offset}. \tag{5}$$

Thus, the offset is obtained by applying $(D_{m1} + D_{m2})/2$. This acquired offset is subtracted from the subsequent measurement data. Every calibration cycle includes one offset measurement and 63 mismatch measurements. The acquired offset is updated in every calibration cycle.

As shown in Fig. 11, due to the finite bandwidth of the V_o port, the sampled signal V_z contains the return-to-zero tails of V_o. They are scrambled by $R_0[k]$ and suppressed by the following LPF and DF. The effects of finite output-port bandwidth on the calibration are analyzed in the Appendix. The return-to-zero tails are treated as noise that induce calibration errors. The calibration errors can be reduced by increasing the DF down-sampling ratio. For this design, 2^{18} consecutive D_s data are accumulated for every D_m. This DF down-sampling ratio allows an output-port bandwidth as low as 100 MHz.

With a DF down-sampling ratio of 2^{18}, one calibration measurement takes 3.34 msec. Since one calibration cycle requires 64 measurements, it takes 214 msec to complete one calibration cycle. During power up, it takes 9 calibration cycles or 1.93 sec for the calibration to converge if the initial M-DAC current cell mismatches are as large as $4.5I$. After that, the calibration only needs to track the environmental variations, such as supply voltage and temperature variations. Although not implemented in this design, the calibration time for the initial power up can be reduced by setting input $D_i[k] = 0$. And then the DF down-sampling ratio can be reduced.

V. Experimental Results

The DAC was fabricated using a standard 90 nm CMOS technology. All functional blocks shown in Fig. 10 are integrated, except the V_o resistive loads R_{L1} and R_{L2}. Fig. 14 shows the chip photograph. The DAC core area is 1100×750 μm^2. The chip also includes a direct digital frequency synthesizer (DDFS) to generate digital inputs for DAC dynamic testing. The synthesizer also generates ramp waveforms for DNL and INL measurements.

The measured DNL and INL before calibration is shown in Fig. 15. In our design, the device dimensions and bias conditions for the L-DAC current cells are different from those for the M-DAC current cells. In addition, this DAC floor plan does not employ common-centroid scheme to reduce the gradient effects. As a result, the raw DNL and INL are poor. The DNL is $+4.5/-0.5$ LSB and the INL is $+10.2/-7.1$ LSB. Fig. 15 shows the measured DNL and INL after current-cell calibration. The DNL is improved up to $+0.47/-0.51$ LSB and the INL is improved up to $+1.0/-1.2$ LSB.

Fig. 17 shows the measured DAC full-scale transient response. The 10%-to-90% rising time is 0.5 nsec, which corresponds to an output-port bandwidth of 700 MHz. This bandwidth does not hinder the DRRZ and the current-cell calibration.

The DAC output spectra are measured during the single-tone tests. The DAC is operated at 1.25 GS/s sampling rate. Fig. 18 shows the output spectrum when the input frequency is 40 MHz. The DAC is calibrated, and the DRRZ is turned off. The SFDR is 73.3 dB. At low input frequency, the CDST effect is low. The SFDR is dictated by the DAC static linearity. In this design, the static linearity is achieved by calibration. Fig. 19 shows the DAC output spectrum with the input frequency increased to 477 MHz. The SFDR is degraded to 58.8 dB by the CDST effect. Fig. 20 shows the DAC output spectrum with the DRRZ enabled. The SFDR recovers to 73.6 dB. The DRRZ mitigates the CDST effect.

Our DAC is designed to operate with each of its outputs connected to a 25 Ω resistive load. However, in the above output spectrum measurements, a spectrum analyzer (SA) is connected to the DAC via a transformer, similar to the output-port configuration of [16]. In this setup, each of the two DAC output

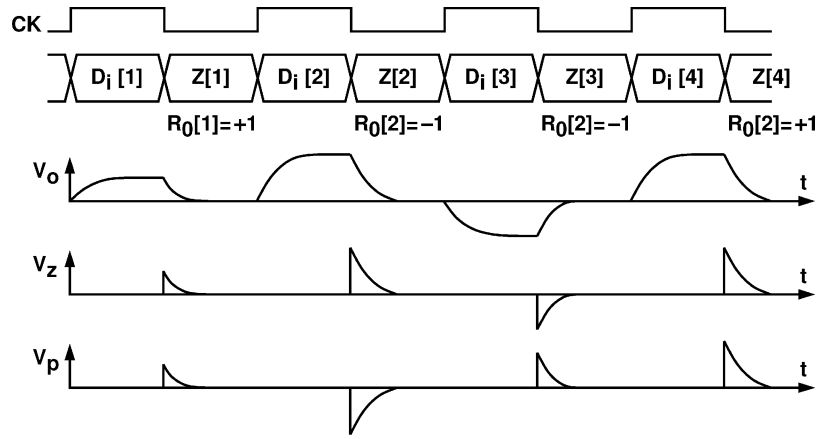

Fig. 11. Various waveforms in calibration signal path.

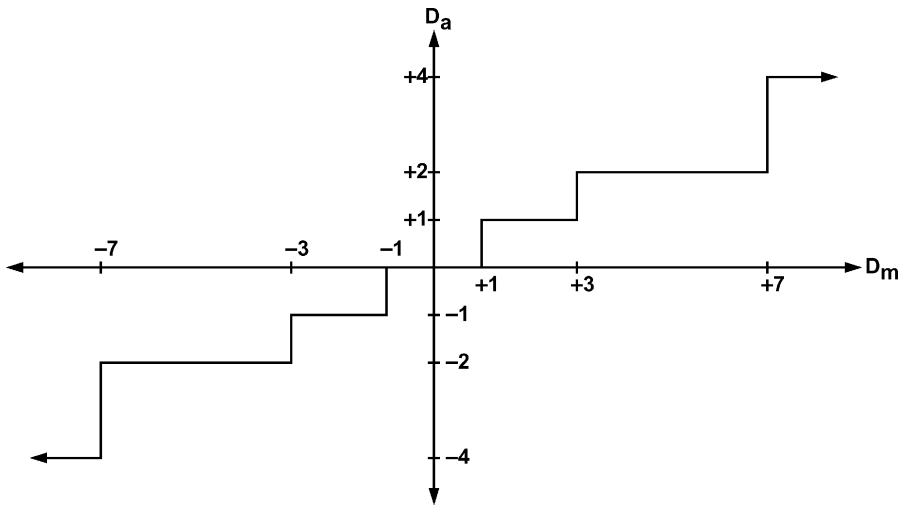

Fig. 12. D_m-to-D_a mapping function.

terminals is connected to a 25 Ω resistor. The other end of the resistor is connected to the $V_{HH} = 2.5$ V supply. The SA adds an additional 50 Ω load connected to the DAC differential output. The DAC can deliver a full-range current of 16 mA to either of its output terminals. In the non-return-to-zero (NRZ) configuration, the DAC can generate a low-frequency full-range sinewave of −4 dBm power to the SA, as shown Fig. 18. In the DRRZ configuration, the DAC can only generate a sinewave of −10 dBm to the SA. However, the sinc droop of a DRRZ DAC is less severe than that of a NRZ DAC [17]. In Figs. 19 and 20, the input frequency is 477 MHz, the resulting signal power is −8.5 dBm for the NRZ DAC and −12.5 dBm for the DRRZ DAC. The power loss due to the NRZ sinc droop is 2.2 dB, and the loss due to the RZ sinc droop is 0.5 dB. The loss due to the 700 MHz output-port bandwidth is 1.6 dB.

Several sources contribute to the random noise at DAC output. They are estimated as follows. 1) The total quantization noise power is $\overline{I_{n1}^2} = I^2/12$. Assume the signal bandwidth is 625 MHz. The current power density is $\overline{I_{n1}^2}/\Delta f = 2.13 \times 10^{-21}$ A^2/Hz. The corresponding noise spectral density (NSD) received by the SA is $\mathrm{NSD}_1 = -166$ dBm/Hz. 2) The current sources in the DAC exhibit device thermal noise. From simulation, the total DAC output current thermal noise density is $\overline{I_{n2}^2}/\Delta f = 2.05 \times 10^{-21}$ A^2/Hz. The corresponding NSD received by the SA is $\mathrm{NSD}_2 = -172$ dBm/Hz. 3) Comparing Figs. 19 and 18, the power increase in the harmonics is $\Delta P_{st} = 10^{-7}$ mW as input frequency is increased. Assume ΔP_{st} is induced entirely by the CDST effect, and it is spread from 0 Hz to $f_s/2$ by the DRRZ. The resulting NSD is $\mathrm{NSD}_3 = \Delta P_{st}/(f_s/2) = -158$ dBm/Hz. The SA in our measurement setup has a noise floor of −140 dBm/Hz by itself. As detailed in the Appendix, once settled, the current-cell calibration in our design does not introduce noise to the DAC output.

Fig. 21 shows the measured SFDR versus input frequency. If the DAC is not calibrated, the SFDR exhibits no significant change when varying the input frequency. The DAC static linearity dominates the SFDR performance. Once the DAC is calibrated, and if the DRRZ is turned off, the CDST effect is the main source of SFDR degradation. When the DAC is calibrated and the DRRZ is turned on, the SFDR is better than 70 dB for input frequencies up to 500 MHz. Also shown in Fig. 21 is the CDLV effect calculated with (1). In this design, the CDLV effect becomes relevant only when the input frequency is higher than 550 MHz.

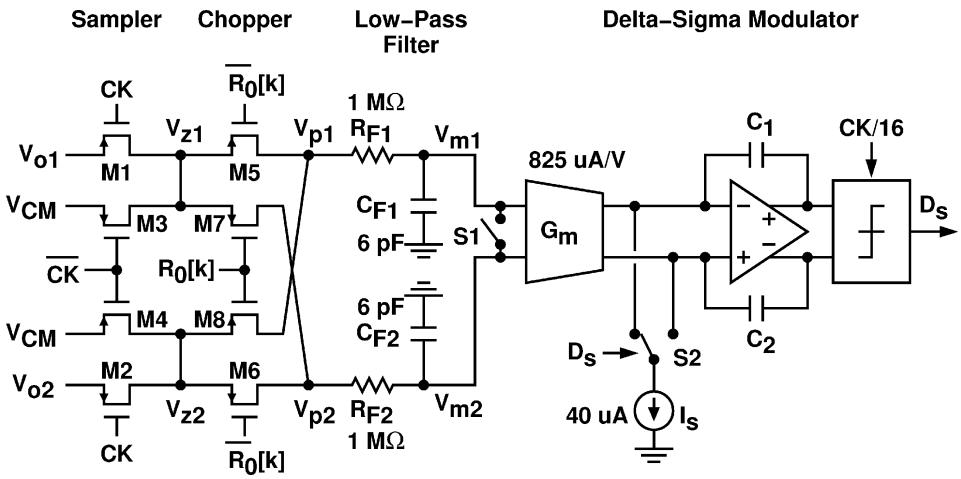

Fig. 13. Schematic of the calibration analog signal path.

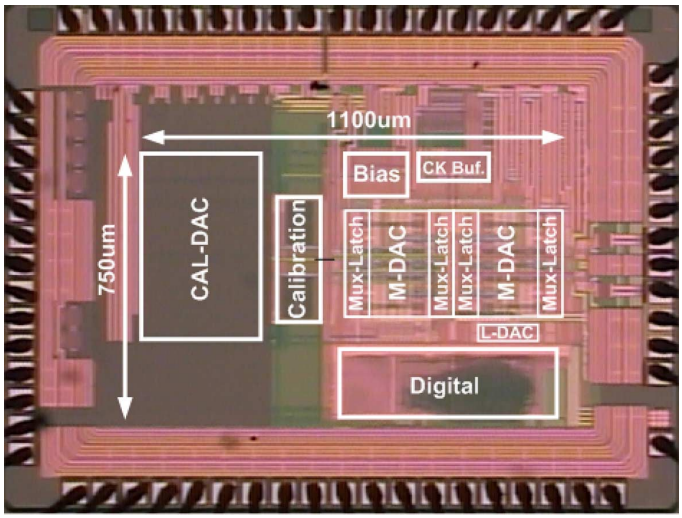

Fig. 14. Microphotograph of the DAC.

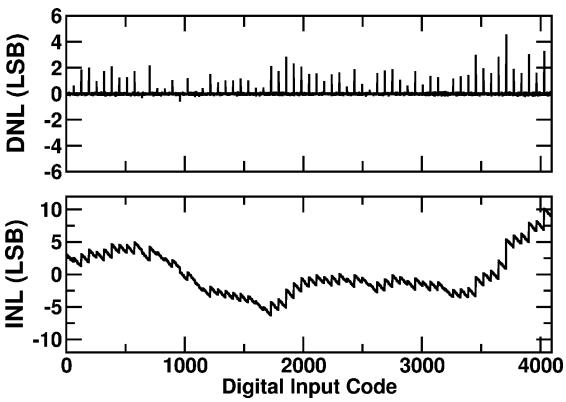

Fig. 15. Measured DNL and INL before current-cell calibration.

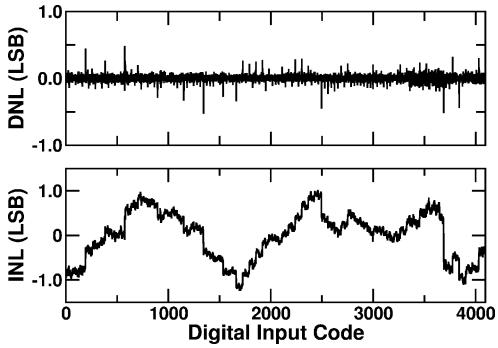

Fig. 16. Measured DNL and INL after current-cell calibration.

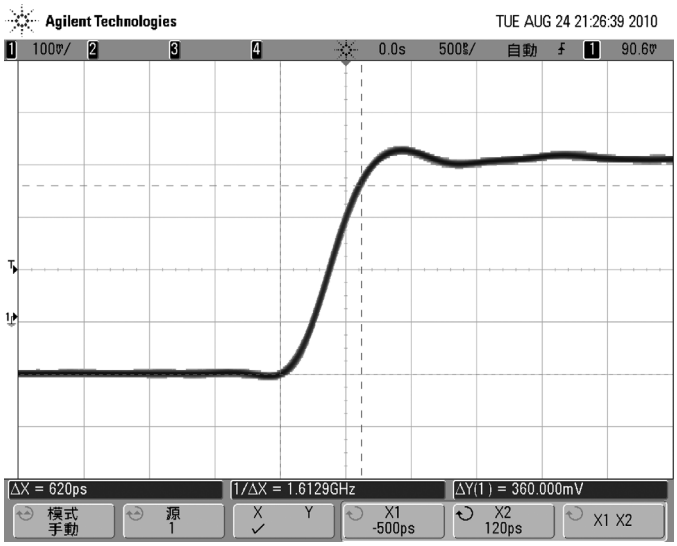

Fig. 17. Measured DAC full-scale transient response.

Fig. 22 compares the SFDR performance of several high-speed DACs of which the sampling rate is higher than 0.5 GS/s and the resolution is better than 12 bits. Table II lists their specifications. In Table II, f_s is the sampling rate, I_L is the maximum output current, $P_{\rm Load}$ is the low-frequency sinewave power delivered to the DAC output load, $\rm SFDR_{LF}$ is the SFDR at low input frequency, and $\rm SFDR_{f_s/2}$ is the SFDR at $f_s/2$ input frequency. The figure of merit (FOM) is defined as

$$\rm FOM = \frac{2^{ENOB_{LF}} \times 2^{ENOB_{f_s/2}} \times f_s}{P_{Total} - P_{Load}} \qquad (6)$$

where $\rm ENOB_{LF} = (SFDR_{LF} - 1.76)/6.02$ and $\rm ENOB_{f_s/2} = (SFDR_{f_s/2} - 1.76)/6.02$. There are various FOM definitions

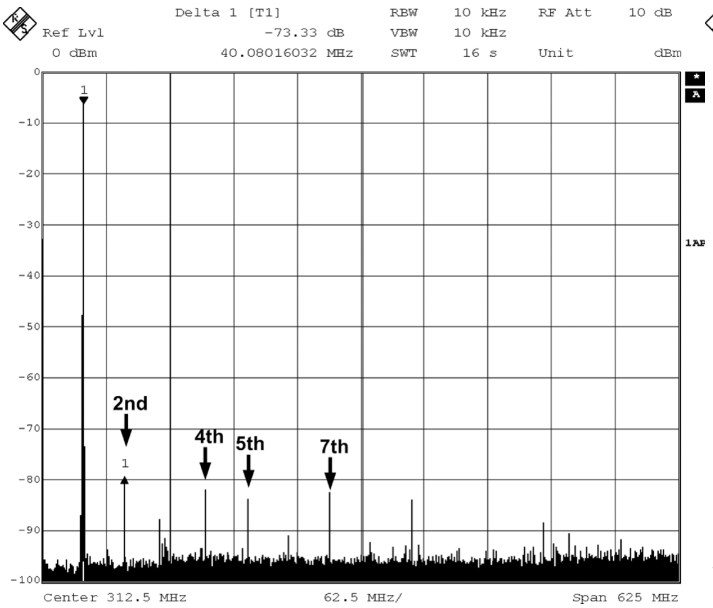

Fig. 18. Measured DAC output spectrum after calibration but without DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 40 MHz.

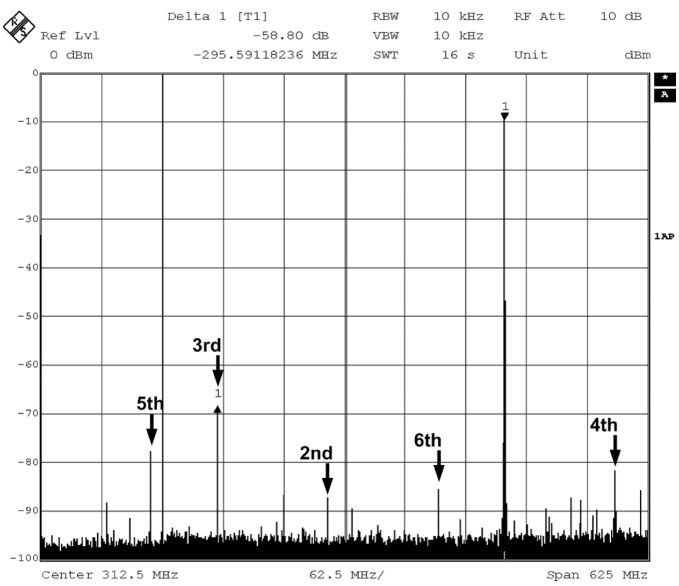

Fig. 19. Measured DAC output spectrum after calibration but without DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 477 MHz.

for DAC comparison [8]. None of the existing definitions is universally endorsed. The FOM of (6), first defined in [30], includes the DAC dynamic performance at high input frequency.

VI. Conclusion

The static linearity of a current-steering DAC is governed by the matching of its internal current sources. Its dynamic performance is degraded by both the code-dependent switching transient (CDST) effect and the code-dependent loading variation (CDLV) effect. The random return-to-zero (DRRZ) operation can eliminate the CDST effect. Adopting a compact current cell design can mitigate the CDLV effect. The DRRZ also facilitates a current-cell background calibration scheme that can correct the mismatches among DAC internal current sources due to device variations. We designed a CMOS 12-bit 1.25-GS/s current-steering DAC to demonstrate the above design techniques. As a result, the DAC achieves a SFDR better than 70 dB up to 500 MHz input frequency.

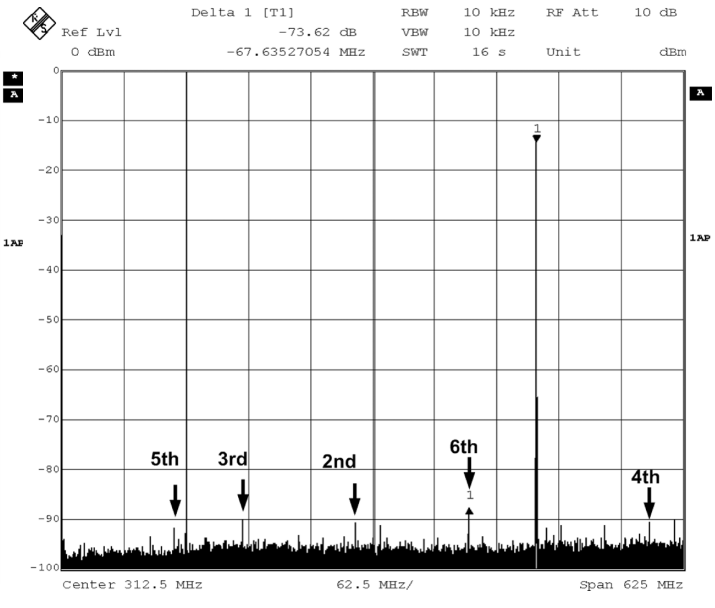

Fig. 20. Measured DAC output spectrum after calibration and with DRRZ. Sampling rate is 1.25 GS/s. Input frequency is 477 MHz.

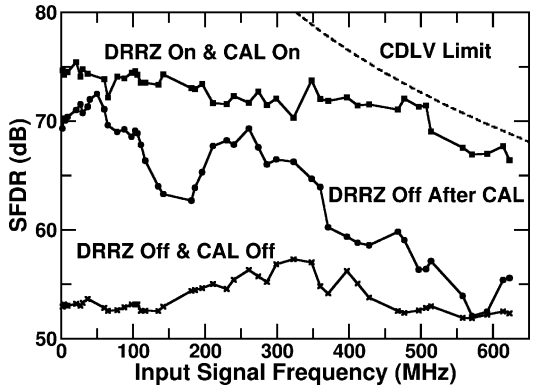

Fig. 21. Measured SFDR versus input frequencies.

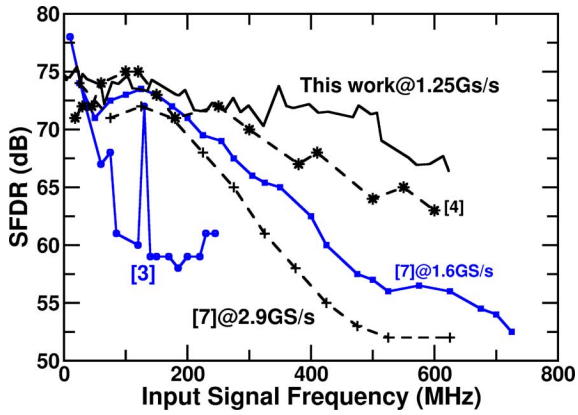

Fig. 22. SFDR performance comparison.

TABLE II
COMPARISON OF PUBLISHED HIGH-SPEED DACS

	This Work	[3]	[4]	[7]
Technology (nm)	90	180	350	65
Core Area (mm^2)	0.825	1.13	30.6	0.31
Supply (V)	1.2/2.5	1.8	3.3	1.0/2.5
P_{Total} (mW)	128	216	6000	188
Resolution (Bits)	12	12	15	12
f_s (GS/s)	1.25	0.5	1.2	2.9
I_L (mA)	16	15	N/A	50
P_{Load} (dBm)	−7	+1.5	0	+9
SFDR_{LF} (dB)	75	78	75	74
$\text{SFDR}_{f_s/2}$ (dB)	66	62	63	52
FOM (10^4 × GHz/mW)	7.36	1.55	0.11	2.24

The technology used in [4] is BiCMOS.

APPENDIX
CALIBRATION UNDER FINITE OUTPUT-PORT BANDWIDTH

Consider the current-cell background calibration scheme shown in Fig. 10 and the related waveforms shown in Fig. 11. Let two capacitors C_{L1} and C_{L2} be in parallel with the two output resistors R_{L1} and R_{L2} respectively, resulting in a finite output-port bandwidth of $1/(2\pi\tau_L)$, where $\tau_L = R_L C_L$, $R_L = R_{L1} = R_{L2}$, and $C_L = C_{L1} = C_{L2}$. The differential DAC output V_o is tracked in every $Z[k]$ zero phase, yielding V_z. Assume the DAC is switched from the $D_i[k]$ data phase to the $Z[k]$ zero phase when $t = 0$. Then, $V_z(t)$ for $t > 0$ can be expressed as

$$V_z(t) = V_z[k]\left(1 - e^{-t/\tau_L}\right) + V_o(0)e^{-t/\tau_L} \tag{7}$$

where $V_z[k] \approx 0$ is the steady-state V_o value in the $Z[k]$ zero phase and $V_o(0)$ is the V_o value at $t = 0$. In (7), $V_z[k]$ contains the current mismatch information ΔI_j, while $V_o(0)e^{-t/\tau_L}$ is the calibration noise to be suppressed by the calibration. If the output-port bandwidth is reduced by increasing τ_L, the mismatch information embedded in V_z is decreased and the calibration noise is increased.

As shown in Figs. 10 and 11, the V_z pulses are modulated by the $R_0[k]$ chopper, yielding V_p. Let $T_s = 0.8$ nsec be the DAC sampling interval and $T_z = T_s/2$ be the zero-phase interval with 50% duty cycle. The average of V_p is the desired mismatched information, which can be expressed as

$$V_m = \eta_m \times \Delta I_j R_L \tag{8}$$

where

$$\eta_m = \frac{1}{T_s}\int_0^{T_z}\left(1 - e^{-t/\tau_L}\right)dt = \frac{1}{2} + \frac{\tau_L}{T_s}\left(e^{-T_z/\tau_L} - 1\right) \tag{9}$$

is the calibration conversion gain for the mismatch $\Delta I_j R_L$. If the output-port bandwidth is 700 MHz, then $\tau_L = 0.23$ nsec and $\eta_m = 0.263$.

Fig. 23 shows the worst-case calibration noise, in which V_z are pulses to approximate the $V_o(0)e^{-t/\tau_L}$ term in (7). Let $V_o(0) = (1/2)2^{12}IR_L$ in every zero phase as the worst-case scenario. The pulse magnitude V_{zs} illustrated in Fig. 23 is found by equating the pulse power to the averaged power of $V_o(0)e^{-t/\tau_L}$. We have

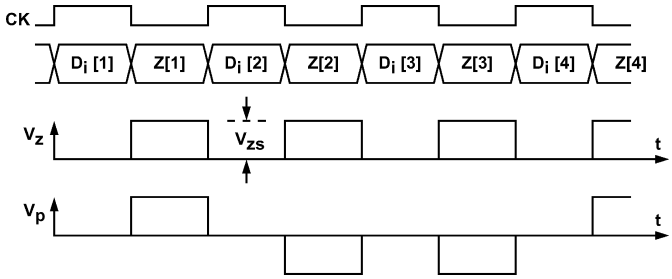

Fig. 23. Worst-case calibration noise.

$$V_{zs} = \eta_n \times 2^{11} I R_L \tag{10}$$

where

$$\eta_n^2 = \frac{1}{T_z}\int_0^{T_z}\left(e^{-t/\tau_L}\right)^2 dt = \frac{\tau_L}{T_s}\left(1 - e^{-T_s/\tau_L}\right). \tag{11}$$

If $\tau_L = 0.23$ nsec, then $\eta_n = 0.53$.

The V_z pulses are randomized by the $R_0[k]$ sequence, yielding the V_p pulses. The power spectral density of V_p, denoted as $S_p(f)$, can be found in [31]. As shown in Fig. 10, the V_p pulses are filtered by a low-pass filter (LPF) with a bandwidth $f_{\text{LP}} = 26.5$ kHz. The residual power of the calibration noise at the LPF output can be found as

$$P_{mc} = \int_0^{\infty} S_p(f)|H(jf)|^2 df \approx 2^6(\eta_n I R_L)^2 \tag{12}$$

where $H(jf) = 1/(1 + jf/f_{\text{LP}})$ is the LPF transfer function. This P_{mc} is further reduced by the decimation filter (DF) shown in Fig. 10. Let N_{ds} be the DF down-sampling ratio. To make the measurement perturbation caused by the calibration noise less than the DAC resolution, I, we want

$$4 \times \sqrt{\frac{P_{mc}}{N_{ds}}} < \eta_m \times I R_L. \tag{13}$$

Thus, the requirement for N_{ds} is

$$N_{ds} > 2^{10} \times \left(\frac{\eta_n}{\eta_m}\right)^2. \tag{14}$$

If the output-port bandwidth is 700 MHz and $\tau_L = 0.23$ nsec, then the calibration requires a DF down-sampling ratio $N_{ds} > 2^{12}$. In our design, $N_{ds} = 2^{18}$. Thus, the calibration can still function under $\tau_L = 1.6$ nsec, i.e., an output-port bandwidth as low as 100 MHz.

The calibration noise yields a variation in the DF output, denoted as D_m in Fig. 10. From (12), with $N_{ds} = 2^{18}$, the variance of D_m can be found as $\sigma(D_m) = (G_m/I_s)\sqrt{P_{mc}/N_{ds}} = 1.7 \times 10^{-5}$. As shown in Fig. 10, $G_m = 825\ \mu\text{A/V}$ is the transconductance converting V_m to current and $I_s = 40\ \mu\text{A}$ is the DSM internal feedback current. Due to the use of the

D_m-to-D_a mapping shown in Fig. 12, the resulting D_a is always 0 once the calibration settles. Thus, the calibration does not introduce noise at the DAC output.

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Wei-Hsin Tseng received the B.S. degree in electrical engineering from National Cheng-Kung University (NCKU), Tainan, Taiwan, in 2002. From 2002 to 2011, he pursued the M.S. and Ph.D. degrees in electronics engineering at National Chiao-Tung University (NCTU), Hsinchu, Taiwan. He received the Ph.D. degree in 2011.

Since 2010, he has been working at MediaTek Inc. where he is responsible for the design of analog and mixed-signal ICs. His current research interest is high-speed high-resolution data converters.

Chi-Wei Fan was born in Hsin-Chu, Taiwan. He received the B.S degree in electrical engineering from the National Central University, Chung Li, Taiwan, in 2000. From 2001 to 2010, he worked toward the Ph.D. degree in electronics engineering at National Chiao-Tung University, Hsin-Chu.

His research interests are mixed-signal, high-speed, and high-resolution integrated circuits. Since 2010, he has been working at MediaTek Inc. where he is engaged in the design of analog and mixed-signal ICs.

Jieh-Tsorng Wu (SM'06) was born in Taipei, Taiwan. He received the B.S. degree in electronics engineering from National Chiao Tung University, Taiwan, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1988, respectively.

From 1980 to 1982 he served in the Chinese Army as a Radar Technical Officer. From 1982 to 1988, at Stanford University, he focused his research on high-speed analog-to-digital conversion in CMOS VLSI. From 1988 to 1992 he was a Member of Technical Staff at Hewlett-Packard Microwave Semiconductor Division in San Jose, CA, and was responsible for several linear and digital gigahertz IC designs. Since 1992, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, where he is now a Professor. His current research interests are high-performance mixed-signal integrated circuits.

Dr. Wu is a member of Phi Tau Phi. He has served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.