Current-Steering Digital-to-Analog Converter With a High-PSRR Current Switch

Ippei Akita, *Member, IEEE*, Tetsuro Itakura, *Member, IEEE*, and Kei Shiraishi

***Abstract*—A power-supply noise (PSN) reduction method for a fully differential current-steering digital-to-analog converter is presented. The method employs a proposed auxiliary path in each current switch and makes PSN-induced currents common-mode ones at the positive and negative outputs, resulting in the differential output with PSN suppressed. The proposed switch also has the capability to cancel out glitch. The simulation results show that the influence due to PSN is effectively reduced and the spurious-free dynamic range is improved.**

***Index Terms*—Current steering, digital-to-analog converter (DAC), glitch, power-supply rejection, substrate noise.**

I. Introduction

THE DEMAND for high-speed, high-resolution, and low-cost CMOS digital-to-analog converters (DACs) is increasing for several system large-scale integration (LSI) technologies, such as transmitters of portable wireless systems [1]–[4]. For these applications, a current-steering topology has been often utilized because of high-speed and low power consumption.

A high power-supply rejection ratio (PSRR) is required in a current-steering DAC because a DAC is generally implemented with a large digital circuit on the same chip when an upsampler and an interpolation filter (IPF) are used in front of the DAC. The use of an upsampler and an IPF lowers the cost of an analog reconstruction filter (RCF) following a DAC in a scaled CMOS process [2]–[5]. Power-supply noise (PSN) comes from the digital circuit through the common substrate and degrades the spurious-free dynamic range (SFDR) at the DAC's output. In this implementation, since PSN includes the frequency components of clock in the digital circuit, the SFDR deteriorates within the Nyquist frequency of a DAC.

The SFDR is also degraded by a glitch that is mainly due to three causes, namely, data skew between current switches, signal feedthrough, and channel charge injection at the switches. Although techniques related with dynamic element matching [6], [7] are suitable for suppressing spurious due to the skew, a novel approach is needed for reducing the SFDR induced by the feedthrough, the charge injection, and PSN.

This brief presents a current-steering DAC with a current switch that makes PSN-induced currents equal at each of the differential terminals of the DAC to cancel out the common-mode PSN-induced currents. The proposed method can also suppress a glitch current that is mainly induced by the signal feedthrough and channel charge injection.

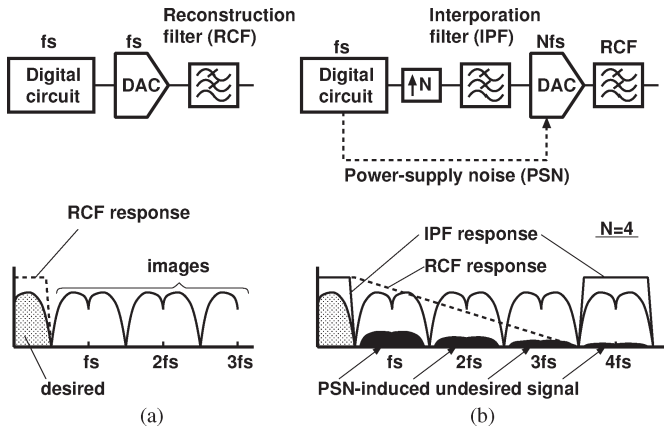

Fig. 1. Output stages. (a) Traditional DAC and RCF chain. (b) DAC–RCF chain with an upsampler and an IPF to simplify the RCF.

II. PSN Issue in a DAC With Interpolation

Adopting an interpolation technique prior to a DAC is an attractive approach to lowering the cost of an RCF implemented in a scaled CMOS process. A traditional output stage consists of a digital circuit, a DAC, and an RCF, as shown in Fig. 1(a). The digital circuit and the DAC operate at the same clock frequency f_s. Since a steep roll-off is required for the RCF to suppress the images of the DAC's desired signal, the order of the RCF is apt to be large, resulting in a high cost. On the other hand, locating an upsampler and an IPF in front of the DAC, the closest image to the desired signal can be suppressed by the IPF. Fig. 1(b) shows this configuration with upsampling rate N of 4. Although the RCF is still needed to eliminate the images around the integer multiple of $4f_s$, the filter order can be considerably reduced. This method is specifically effective in a scaled CMOS process because the digital filter IPF can be implemented in a smaller area.

In this configuration, however, an issue exists: The DAC is influenced by PSN that comes from the digital circuit through the common substrate. The amount of substrate noise is mainly determined by the dynamic switching current of the digital circuit and the impedance of substrate, coupling capacitor, and bonding wires. Even if the power-supply lines of the digital and the analog part on the chip are separated, the analog supply is affected through the substrate and the junction capacitor.

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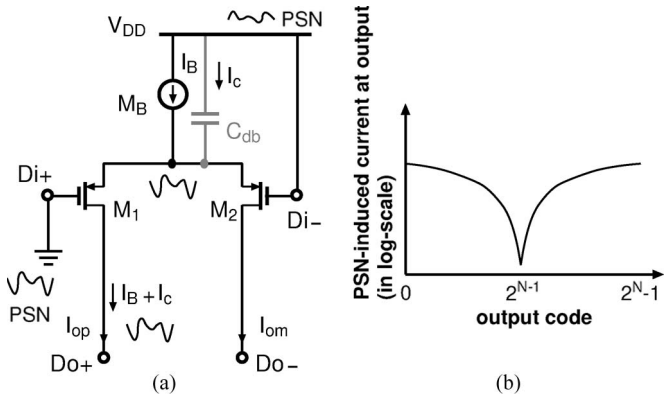

Fig. 2. PSN effect on the current switch of a DAC. (a) Current switch and influence of PSN and (b) its dependence for the output code.

The waveforms of the analog ground and the power-supply voltage have the opposite phase due to a configuration of decoupling capacitors and inductors of bonding wires. Note that the frequency component of the PSN-induced undesired signal mainly includes f_s rather than Nf_s, as shown in Fig. 1(b), because most of the digital circuit operates at f_s [8]. In this case, the RCF has to eliminate the influence, resulting in the increase in complexity for the RCF.

The mechanism of the PSN effect at the DAC's output is shown in Fig. 2(a). In this figure, a conventional current switch is considered when M_1 and M_2 are assumed to be on and off, respectively. In this case, M_1 and bias current source I_B, which is usually realized by p-channel MOSFET M_B, act as a source follower. An ac I_C flows through drain-to-bulk capacitor C_{db} of M_B because PSN of ground directly appears at the common-source node of M_1 and M_2, as shown in Fig. 2(a). Positive output current $I_{\rm op}$ is equal to $I_C + I_B$, which corresponds to differential output current $I_{\rm op} - I_{\rm om}$ because a negative one, i.e., $I_{\rm om}$, is zero. This means that the output of a conventional current switch is strongly influenced by PSN. Note that, although there are source-to-bulk capacitors C_{sb} of switch MOSFETs in parallel with the drain-to-bulk capacitors, the capacitance of C_{sb} is much smaller than that of C_{db} and can be merged with C_{db}. Therefore, the source-to-bulk capacitors are omitted here.

The PSRR of a current-steering DAC depends on the output code, as shown in Fig. 2(b). When the middle code is output, the PSN-induced current from the power-supply and ground lines almost disappears at the differential output of the DAC because the noise currents are common-mode ones. By contrast, in the case of an output of a maximum or a minimum code, the noise is steered into either a positive or a negative output terminal. In this case, the noise is no longer a common-mode current at the output, resulting in spurious. Therefore, the high PSRR of a DAC in such a system LSI is required.

III. Current Switch With a Proposed Auxiliary Path

A. PSN Reduction

In order to suppress the influence of PSN at the output of the DAC, a novel current switch is proposed, as shown in Fig. 3.

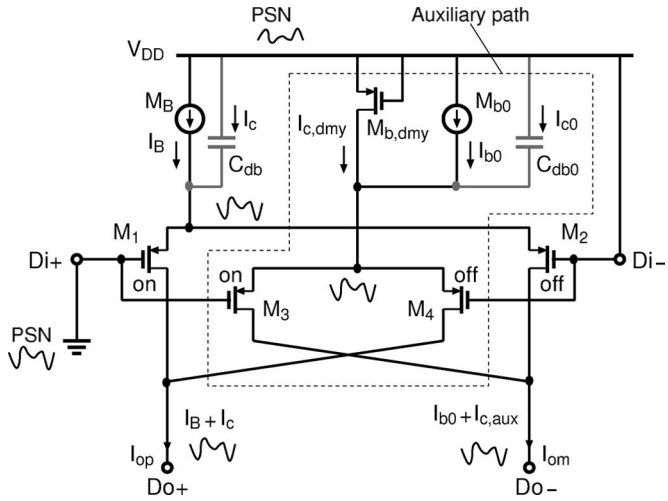

Fig. 3. Current switch with the proposed auxiliary path (including parasitic capacitors and an explanatory drawing for PSN reduction).

The switch has an auxiliary path that makes a PSN-induced current a common-mode one. The auxiliary path consists of current switches M_3 and M_4, current source M_{b0}, and dummy MOSFET $M_{b,\rm dmy}$. Current source M_{b0} is biased to flow dc I_{b0}. The output terminals of the additional current switch are cross coupled with those of the main switch consisting of M_1 and M_2. Capacitor C_{db0} is a drain-to-bulk one of M_{b0}, and its ac is I_{c0}. Since the gate terminal of dummy transistor $M_{b,\rm dmy}$ is connected to its source one, the dc does not flow. On the other hand, an ac due to the drain-to-bulk capacitor is defined as $I_{c,\rm dmy}$.

First, it is assumed that input D_{i+} is connected to ground, and another D_{i-} connected to supply voltage V_{DD} without PSN is considered. In this case, differential output current $I_{\rm op} - I_{\rm om}$ is equal to $I_B - I_{b0}$, where the current in the main path is larger than that in the auxiliary path, i.e., $I_B > I_{b0}$. Next, it is assumed that the power-supply and ground voltage have PSN in opposite phase, as shown in Fig. 3. In this case, M_3 and I_{b0} in the auxiliary path act as a source follower, as well as M_1 and I_B. In the main path, PSN-induced current I_c is generated in the same manner as that in Fig. 2 and flows into terminal D_{o+}. On the other hand, another PSN-induced current $I_{c,\rm aux}$ also arises in the auxiliary path and appears with I_{b0} at terminal D_{o-}. Therefore, if $I_c = I_{c,\rm aux}$, the noise currents are common-mode ones, and thus, the differential output current becomes $I_B - I_{b0}$ that no longer includes the PSN-induced current. Note that the value of current I_{b0} in the auxiliary path is set to a value larger than the peak of PSN-induced current $I_{c,\rm aux}$. In the situation shown in Fig. 3, since I_{b0} becomes a bias current of M_3 to flow I_{c0} into D_{o-}, lack of I_{b0} results in weak PSN-reduction capability. Increasing I_{b0} lowers the dynamic range and if differential output $I_B - I_{b0}$ is smaller than a specified least significant bit (LSB) value, I_B should be increased.

The proposed technique can be also adopted in a cascoded current source. In this case, although the drain-to-source voltage of a current source transistor is constant, a PSN-induced current flows through C_{db} of a cascode transistor.

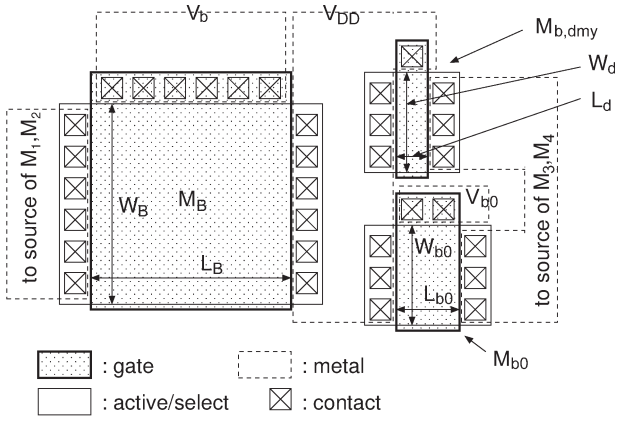

Fig. 4. Layout example of a current source and an auxiliary path.

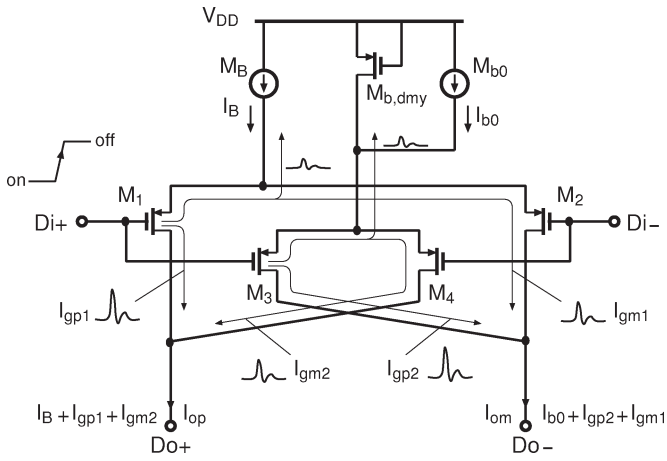

Fig. 5. Glitch behavior in the proposed current switch at update transition.

A magnitude of current $I_{c,\mathrm{aux}}$ is determined by total parasitic capacitance between the power supply and the common-source node of M_3 and M_4. In Fig. 3, C_{db0} of M_{b0} might correspond to the capacitance. However, since $I_B > I_{b0}$ as described above, the gate size of current source M_{b0} is different from that of M_B, and thus, $C_{db} \neq C_{db0}$. This means that $I_c \neq I_{c0}$. To avoid this current difference, dummy transistor $M_{b,\mathrm{dmy}}$ is added in the proposed auxiliary path. The dummy transistor also has a drain-to-bulk capacitor, and its ac $I_{c,\mathrm{dmy}}$ flows into terminal D_{o-} along with I_{c0}. If $I_c = I_{c0} + I_{c,\mathrm{dmy}} = I_{c,\mathrm{aux}}$, the PSN-induced current can be suppressed by the differential configuration. Fig. 4 shows the layout example of the main current source and auxiliary one with a dummy MOSFET. In order to adjust $I_{c0} + I_{c,\mathrm{dmy}}$ to I_c, the gate width relation between these transistors should satisfy

$$W_B = W_{b0} + W_d \tag{1}$$

because the drain-to-bulk capacitance is almost determined by the diffusion area of their drain terminals, where W_B, W_{b0}, and W_d are the gate width of M_B, M_{b0}, and $M_{b,\mathrm{dmy}}$, respectively.

Adopting a voltage regulator for the supply voltage of a DAC is one of the solutions to suppress PSN. In this case, a higher supply voltage for the regulator is required, and a loss due to a voltage drop of the regulator becomes relatively large. Furthermore, a large capacitor at the output of the regulator is also needed, which is usually an external component. These requirements could lead to more complexity and increase power consumption compared with the proposed method.

B. Glitch Reduction

The proposed auxiliary path can suppress not only the PSN-induced current but also glitch, which arises from channel charge injection and the signal feedthrough at the instance of changing the state of the current switch.

Fig. 5 illustrates the glitch behavior in the proposed current switch. A transition in which the state of M_1 and M_3 changes from ground to supply voltage is considered, as shown in Fig. 5. First, channel capacitors of M_1 and M_3 in a saturation region are charged when these switches are ON-state. Letting these switches off rapidly, channel capacitors are discharged, and their charges are injected toward output terminals D_{o+} and D_{o-} [9]. These charges emerge from its source and drain terminals as a pulse current (glitch), namely, I_{gp1} and I_{gm1}, where the M_1-induced glitch is only considered for ease of explanation. The amplitude of glitches at the output terminals becomes different because of an impedance difference between the source and drain terminals of M_1. Although I_{gp1} directly flows to D_{o+}, I_{gm1} does to D_{o-} through M_2 and a parasitic capacitor at the common-source node of the main switches. This different impedance of the paths makes the amplitude of I_{gm1} smaller than that of I_{gp1}. On the other hand, M_3-induced glitches I_{gp2} and I_{gm2} appear at outputs D_{o-} and D_{o+} in the same manner as M_1. As a result, output currents I_{op} and I_{om} are equal to $I_B + I_{\mathrm{gp1}} + I_{\mathrm{gm2}}$ and $I_{b0} + I_{\mathrm{gp2}} + I_{\mathrm{gm1}}$, respectively. If the gate sizes of all the switches are the same, $I_{\mathrm{gp1}} \approx I_{\mathrm{gp2}}$ and $I_{\mathrm{gm1}} \approx I_{\mathrm{gm2}}$ can be realized because the impedance of two common-source nodes and each channel capacitance have almost the same value. Therefore, since these glitch currents are common-mode ones at the output terminals, differential output current $I_{\mathrm{op}} - I_{\mathrm{om}}$ becomes $I_B - I_{b0}$, which does not have a glitch due to channel charge injection. An effect due to the signal feedthrough can be also canceled out in the same manner as channel charge injection.

In a conventional current switch, the cross point of the differential digital input signal has been a concern with regard to the change in the common-source node voltage [10]. This change results in unbalanced glitch currents between the differential outputs. Since the adjustment of the cross point is realized by properly sizing latches in front of the current switch, the accuracy of the cross-point decision depends on a variation of transistors in latches. Consequently, the variation results in a glitch. By contrast, the amount of the glitch in the proposed current switch is independent of the cross point. Even if unbalanced glitch currents appear at the output in the main path, the auxiliary path also generates the same glitch currents and feeds them to the opposite output terminal. Therefore, the glitch always becomes common mode and can be suppressed. Note that the common-mode rejection ratio (CMRR) of the circuit is important because PSN and glitch-cancellation capability directly depends on the CMRR.

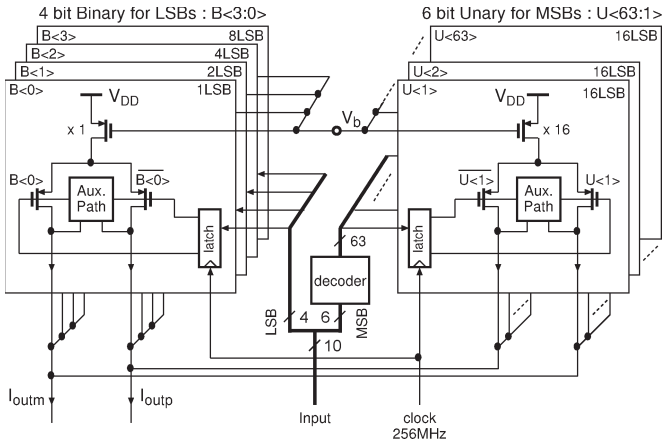

Fig. 6. DAC with the proposed current switch.

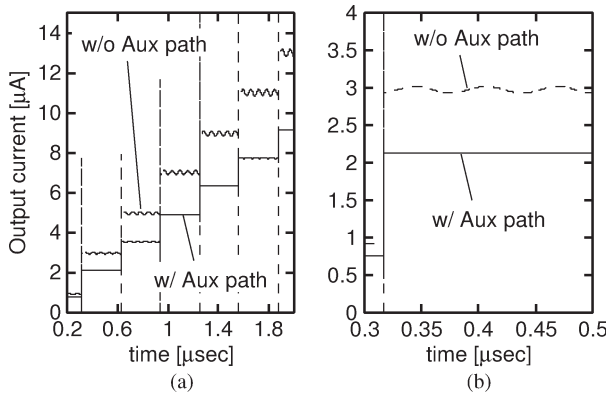

Fig. 7. Simulated output waveforms. (a) Applying a ramped input code and (b) its expanded one.

IV. Simulation Results

A 10-bit current-steering DAC shown in Fig. 6 is designed to verify the effectiveness of the proposed current switch. The DAC consists of current sources, switches, latches, and a decoder. The DAC is a segment type and has 6-bit unary cells and 4-bit binary ones. The number of bits for unary and binary is determined by a balance between the device size of the current sources and a required static characteristic. In this design, a requirement of both the differential and the integral nonlinearity is set to ± 0.2 LSB, and the number of bits for unary and binary becomes 6 and 4 bits, respectively [11]. A 0.13-μm CMOS process is assumed, and the device size of the current source satisfies (1). The total active area of the designed DAC is 1.3 times larger than that of the conventional DAC. The following results are provided by prelayout simulations.

The output waveforms of the conventional and proposed current switches are shown in Fig. 7(a), where 16-MHz PSNs from a digital circuit are assumed: a 16-MHz 20-mV sinusoidal wave (SW) is applied to ground and a 10-mV SW in opposite phase to the power supply. The input data are a ramp waveform, as shown in Fig. 7(a), and its expanded waveform at around 0.4 μs is depicted in Fig. 7(b). The differential output current of the DAC with the auxiliary path is smaller than that without the path because of the subtraction of I_{b0} at the proposed current switch. In this design, the currents of 1 LSB for the main and

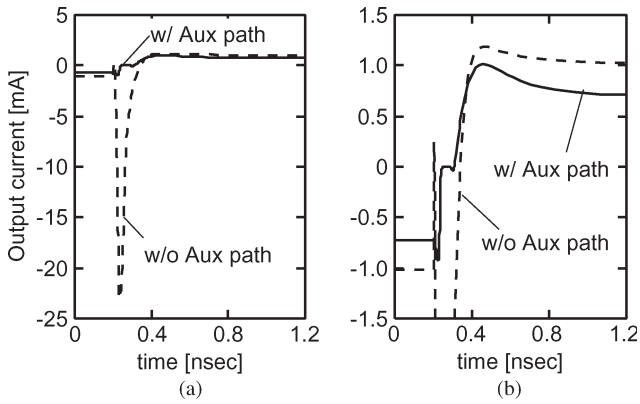

Fig. 8. Simulated output waveforms. (a) Full-scale switching and (b) its expanded one.

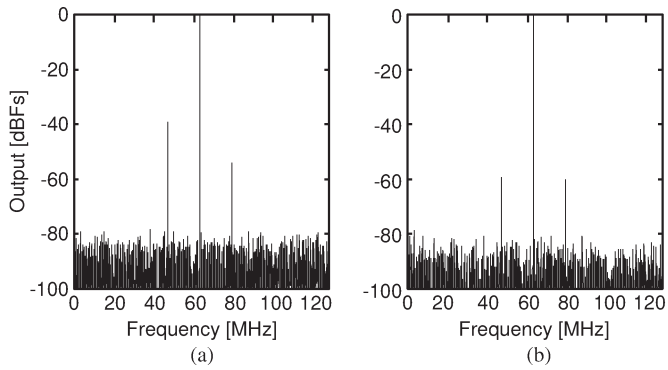

Fig. 9. Output spectrum with PSN for $f_{\rm in} = 62.875$ MHz and $f_s = 256$ MHz. (a) Without and (b) with an auxiliary path.

auxiliary paths are set to 1 and 0.3 μA, respectively. Therefore, the increase rate of the consumed current compared with the conventional DAC is about 1.3. From this result, the output of the DAC with the proposed auxiliary path does not suffer from the PSN-induced current. Step responses of the DACs are shown in Fig. 8, where full-scale swing input is applied, changing the input code from 0 to 1023. As shown in the result, the peak of the glitch exceeds 20 mA at the DAC with the conventional current switch. On the other hand, the proposed one can suppress the glitch current.

Fig. 9 shows the output power spectrum of the current-steering DACs with and without the auxiliary path in current switches. Since the 16-MHz PSN is assumed, two spurious appear on both sides of the fundamental signal at a 16-MHz interval because they are modulated. In this simulation, a parallel digital signal processing or a digital intermediate frequency transmitter architecture [4], [5] is assumed, and thus, the frequency of the input signal is set to around 60 MHz, which is higher than the Nyquist frequency of the digital clock of 16 MHz. The results show that the SFDR using the proposed current switch is improved by about 20 dB. This improvement of dynamic characteristic is also confirmed in the comparison in Fig. 10, which shows the simulated SFDR and signal-to-noise-plus-distortion ratio (SNDR) excluding thermal noise.

The proposed current switch has extra devices, such as a dummy transistor, an additional current source, and switches in an auxiliary path. Therefore, it is more sensitive to process

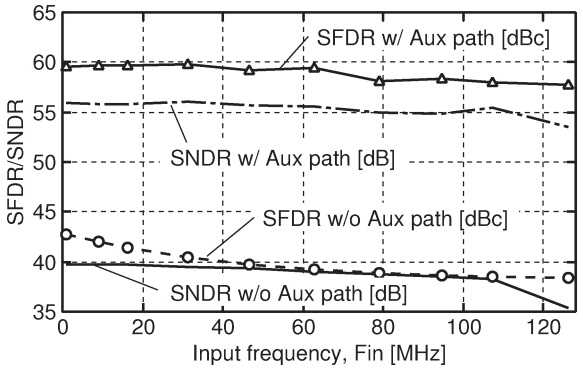

Fig. 10. Simulation result of the SFDR and SNDR as a function of input frequency.

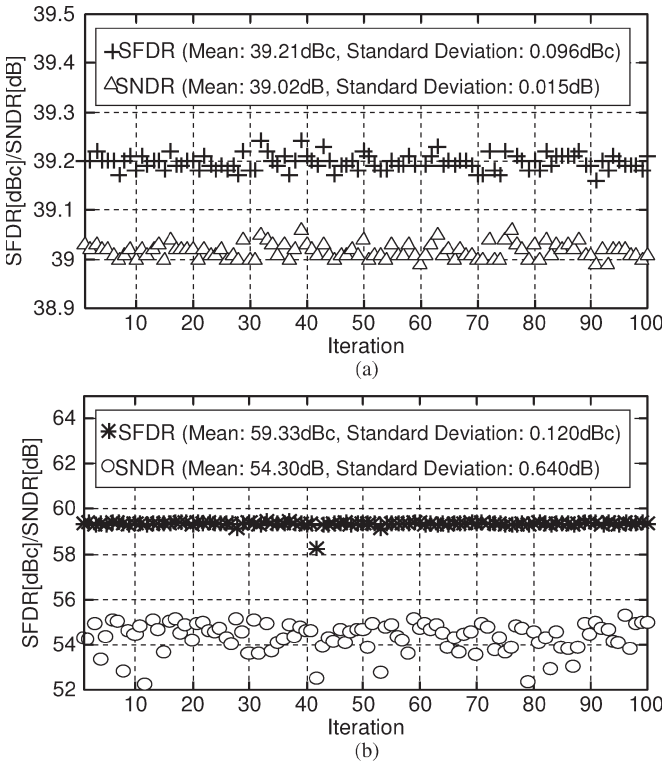

Fig. 11. Monte Carlo simulation. SFDR and SNDR results under 100 iterations. (a) Without and (b) with an auxiliary path, where $f_{\rm in} = 62.875$ MHz and $f_s = 256$ MHz.

variation, as shown in Fig. 11, which shows Monte Carlo simulations with a threshold voltage varied under 100 iterations. However, the standard deviation is still small compared with SFDR and SNDR improvements.

PSN-reduction capability has a frequency characteristic. The frequency bandwidth from ground to the common-source nodes of the two switch pairs is different because their bias currents are different, i.e., $I_B > I_{b0}$. In this case, PSN at the common-source node of M_3 and M_4 is smaller than that of M_1 and M_2 as PSN frequency $f_{\rm ck}$ becomes higher. This is confirmed by the result shown in Fig. 12, which is the simulated power-supply rejection characteristic as a function of PSN frequency $f_{\rm ck}$. Note that the amplitude of the output signal becomes small although the SFDR becomes larger at high PSN frequency $f_{\rm ck}$ as I_{b0} is

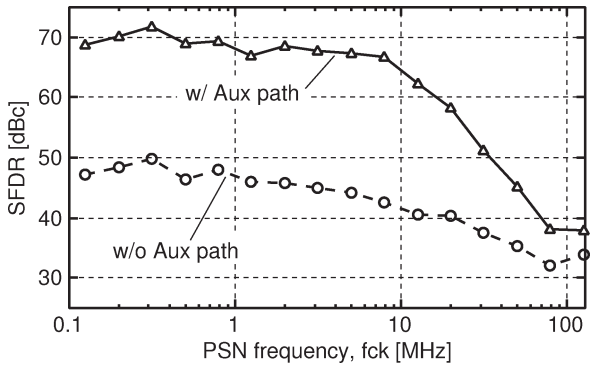

Fig. 12. SFDR versus PSN frequency $f_{\rm ck}$.

set to a larger value. Although there is a tradeoff between the bandwidth and the power consumption, the proposed technique is suitable for applications with a few megahertz baseband and an interpolation.

V. Conclusion

This brief has presented a high-PSRR current switch for DACs in system LSI technologies. The current switch includes the proposed auxiliary path that generates the PSN-induced current and glitch, one like the main path, in order to make these currents common-mode ones. These common-mode noise currents can be suppressed at the differential output. The simulation results show the effectiveness of the current switch in terms of SFDR improvement.

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