A 10-bit Resistor-Floating-Resistor-String DAC (RFR-DAC) for High Color-Depth LCD Driver ICs

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***Abstract*—This work proposes a novel resistor-floating-resistor-string digital-to-analog converter (RFR-DAC) architecture with a 10-bit resolution for liquid crystal display (LCD) driver applications. The proposed architecture improves the linearity of DAC, unifies its channel performance, and achieves a 10-bit resolution with a compact die size smaller than those of the state-of-the-art 10-bit DACs. The proposed RFR-DAC combines a 6-bit RDAC and a 4-bit FR-DAC (floating-resistor-string DAC) to offer unique two-voltage-selection and one-voltage-selection schemes without the need of unity-gain buffers to isolate parallel-connected resistor strings. A stacked floating class-AB control is also devised to bias the last output buffer stage. The 10-bit RFR-DAC prototypes are implemented using 0.35-µm/0.5-µm CMOS technology with the worst DNL/INL = 0.11/0.92 LSB via a two-voltage-selection scheme; and 1.37/1.45 LSB via a one-voltage-selection scheme.**

***Index Terms*—Buffer amplifier, column driver, DAC, digital-to-analog converter, LCD, LCD driver, liquid crystal display, RDAC.**

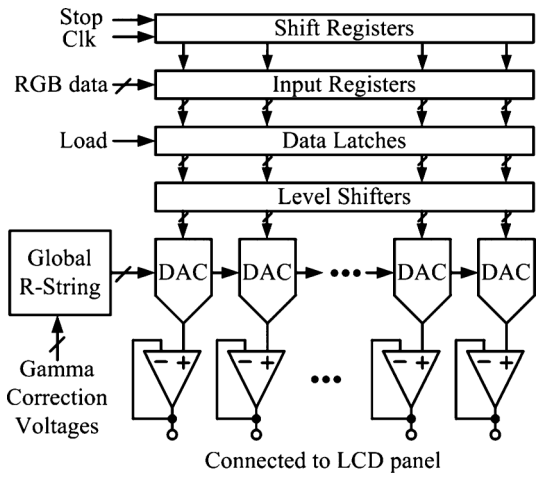

Fig. 1. Column driver architecture.

I. Introduction

RECENT advancements in liquid crystal display (LCD) panels for multimedia and medical systems demands higher definition and higher color depth. An LCD module often includes several column drivers and gate drivers. Within the column driver, it contains shift registers, input registers, data latches, level shifters, DACs and output buffers, as shown in Fig. 1 [1], [2]. Among these components, DACs and output buffers determine the speed, resolution, voltage swing, and power dissipation of a column driver. Additionally, DACs often occupy an extensive part of silicon area in column drivers because each driver chip contains hundreds of DACs and output buffer amplifiers. It would greatly advance the state-of-the-art, if we can substantially reduce the area and static power consumption of the DAC and associated buffer amplifiers. The uniformity among various drivers is also critical, since an LCD panel requires several column drivers. Linearity, however, tends to be less critical than non-uniformities among off-chip drivers for LCD driving purpose [3]. Those output buffers should provide a nearly rail-to-rail voltage driving capability that can accomplish higher gray levels. Also, the settling time must be less than the horizontal scanning time. For UXGA $(1600 \times \mathrm{RGB} \times 1200)$ and XGA $(1024 \times \mathrm{RGB} \times 768)$ displays with 60 Hz frame rate, the horizontal scanning times should not exceed 13.9 μs and 21.7 μs, respectively.

Achieving a higher color depth in LCD drivers requires a higher DAC resolution [4], [5]. Also, because of stringent display uniformity requirements, a resistor-string DAC (RDAC) is predominantly used in LCD column drivers. However, the area of RDAC and its related routing lines is excessively large for a high-resolution data converter, rendering it impractical for using conventional column driver ICs in high color depth displays [6].

To avoid the aforementioned issues, several DAC architectures have been developed for LCD driver applications, including a CDAC [7], [8], an embedded DAC [9], [10], and DACs with current modulation/interpolation [11]–[13]. However, the CDAC architecture suffers from a long D/A conversion time. The embedded DAC architecture requires several input transistors with long widths and lengths for accurate matching, subsequently resulting in large area overhead for high-bit interpolation.

RDAC has guaranteed monotonicity and is applicable for converters with 10-bit resolution. However, for high-resolution applications, the switch components of a voltage selector grow exponentially with the number of bits, leading to a larger RC delay at the output and a prohibitively large area of switch components and the metal routing lines. Several modifications were proposed to obtain high-resolution data conversion and/or high-

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speed switching. Resistor-resistor-string DACs (RRDACs) utilizing two cascaded resistor strings have been developed [14]. By operating as a coarse divider, the first resistor string provides a few equal voltage segments between two reference voltages. A voltage selector chooses two adjacent voltages and, then, sends them to the second resistor string for further fine voltage division. Additionally, an intermeshed resistor reference ladder network was proposed for use in an analog-to-digital converter (ADC) [15]. This intermeshed ladder-design layout uses separate polysilicon and diffused resistors for coarse and fine sections to increase the switching speed. Another study also developed folded resistor string DACs and dual-ladder resistor string DACs to enhance the conversion linearity by minimizing the gradient effects of polysilicon resistors [16], [17]. A mixed-signal, piece-wise linear calibration scheme was also developed to improve the linearity of resistor string DACs [18]. The calibration uses a single insertion during the final test. This scheme eliminates the need for an exotic thin-film process, expensive laser trimming setup and costly wafer probing.

Among the above modifications of RDACs, RRDACs are the most area-effective and thus the most promising alternative for LCD column driver applications [19]. The coarse resistor string used for the global resistor string provides a few reference voltages for all channel drivers. Each channel driver contains a fine resistor string for fine voltage division. However, this cascaded resistor string configuration is limited by the loading of the coarse resistor string from the fine resistor strings, subsequently affecting the segment voltage levels of the coarse resistor string. Although the problem with loading by the fine voltage dividers can be avoided by using two intermediate unity-gain buffers in each channel driver, doing so often causes offset errors to LCD driver outputs, leading to display non-uniformity. Moreover, each output channel requires two additional buffers with increased power consumption.

To alleviate the above problems, this work presents a novel RFR-DAC architecture, capable of simultaneously achieving high linearity, high uniformity and 10-bit resolution at a size smaller than that of a conventional 8-bit RDAC [20]. Two prototype RFR-DACs are also implemented with two different voltage selection schemes. Furthermore, a class-AB buffer amplifier with a stacked floating class-AB control is developed for LCD drivers.

The rest of this paper is organized as follows. Section II introduces proposed RFR-DACs with either two-voltage-selection or one-voltage-selection floating-resistor string(s). The voltage selector, compensation current source, and class-AB buffer amplifier are also described. Section III summaries test results and Section IV concludes the work.

II. Proposed RFR-DACs

The conventional RRDAC cascades two RDACs and uses the resistor string of the first RDAC to bear the loading from the second. To minimize such a loading burden, the proposed RFR-DAC is constructed by connecting an RDAC and a floating-resistor-string DAC (FR-DAC) in a series manner. Consequently, FR-DAC adds only an insignificant loading to the resistor string of the first-stage RDAC. Moreover, two FR-DACs are implemented for the second-stage DAC of RFR-DAC. Fig. 2(a) shows the FR-DAC based on a two-voltage-selection scheme. The floating-resistor string contains m resistors connected in a series with a compensation current source as well as a compensation current sink. The compensation current source and sink have the same amount of current. The current source injects a current into the top end of the resistor string, and the current sink draws the same amount of current from its bottom end. Because the two compensation currents are equal to each other, the resistor string shows a high output impedance at any node in the resistor string. The resistor string thus equivalently floats between the compensation current source and sink. When the floating-resistor string

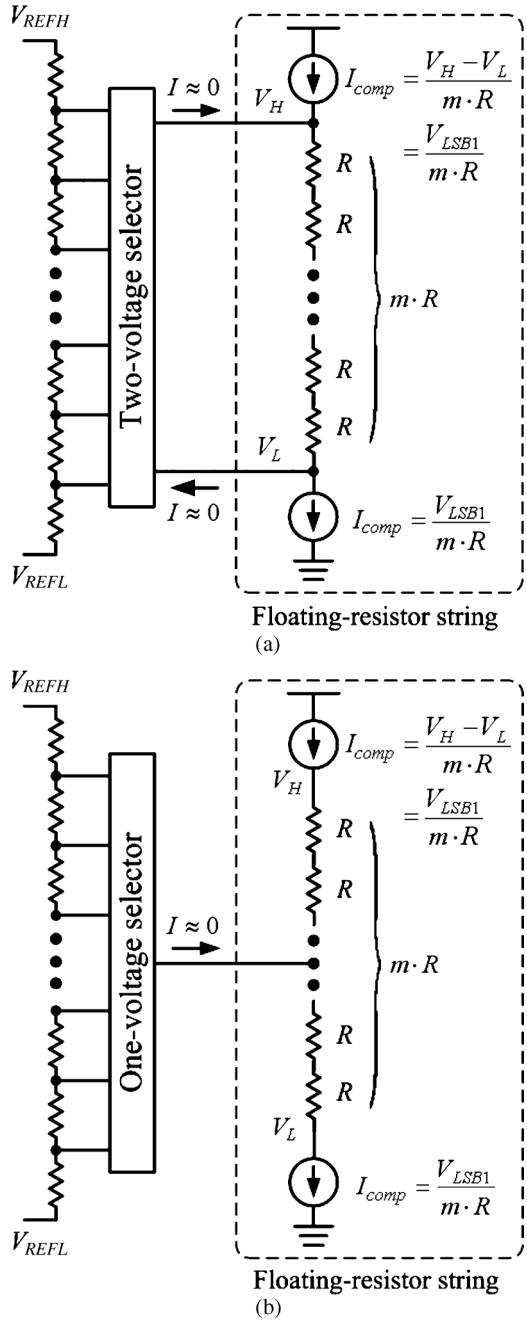

Fig. 2. Floating-resistor-string DAC with (a) two-voltage-selection scheme and (b) one-voltage-selection scheme.

is using in RFR-DAC, the voltage difference between the top and bottom ends of the floating-resistor string equals one LSB voltage of the first-stage RDAC. Therefore, the compensation current is

$$I_{comp} = \frac{V_{LSB1}}{m \cdot R} \tag{1}$$

where V_{LSB1} denotes one LSB voltage of the first-stage RDAC. The voltage selector chooses two adjacent resistor string node voltages from the first-stage resistor string and, then, connects them to the top and bottom ends of the floating-resistor string. Because the voltage difference between the top and bottom ends of the floating-resistor string equals one LSB voltage of the first-stage RDAC, little current flows between the first-stage resistor string and the floating-resistor string. Hence, the loading effect on the first-stage RDAC from the floating-resistor string is insignificant. Because the floating-resistor string exhibits a high output impedance at any node in the resistor string, the voltage-selection scheme may become a one-voltage-selection scheme, as shown in Fig. 2(b). The voltage selector chooses one voltage from the first-stage resistor string and, then, connects it to one point of the floating-resistor string. Owing to high output impedance of the floating-resistor string, the first-stage resistor string suffers insignificant loading from its second-stage counterpart.

However, the finite output resistances of the compensation current source and sink vary with the selected voltages (V_i and V_{i+1}). A situation in which the selected voltages are close to VDD/GND implies that output resistance of the compensation current source/sink is reduced, subsequently increasing the loading burden on the first-stage resistor string. Currents then flow between the first-stage resistor string and the floating-resistor string. Fig. 3(a) shows the simplified FR-DAC based on a two-voltage-selection scheme with finite output resistances of the compensation current source and sink for analyzing the loading effect, where R_1 denotes the segment resistance of the first-stage resistor string and R_S represents the switch on-resistance between the input and output of the voltage selector. The first-stage resistor string contains M resistors connected in a series. Also, R_{outp} and R_{outn} refer the output resistances of the compensation current source and sink, respectively. The voltage selector chooses two adjacent voltages (V_i and V_{i+1}) from the first-stage resistor string and, then, connects them to the top and bottom ends of the floating-resistor string. When the selected voltages are close to VDD, the output resistance of the compensation current source becomes smaller. The compensation current source then supplies a lower current; in addition, two currents (I_{S1} and I_{S2}) flow from the first-stage resistor string to the floating-resistor string. Using the superposition theorem allows us to obtain the voltages V_i and V_{i+1} in terms of V_{REFH}, V_{REFL}, I_{S1}, and I_{S2}. The difference voltage between V_i and V_{i+1} can be expressed as

$$\begin{aligned} V_{i+1} - V_i &= \frac{(V_{\mathrm{REFH}} - V_{\mathrm{REFL}})}{M} \\ &\quad + \frac{I_{S2} \cdot i \cdot (M-i) - I_{S1} \cdot (i+1) \cdot (M-i-1)}{M} R_1 \\ &\cong \frac{(V_{\mathrm{REFH}} - V_{\mathrm{REFL}})}{M} + \frac{\Delta I_S \cdot i \cdot (M-i)}{M} R_1 \end{aligned} \tag{2}$$

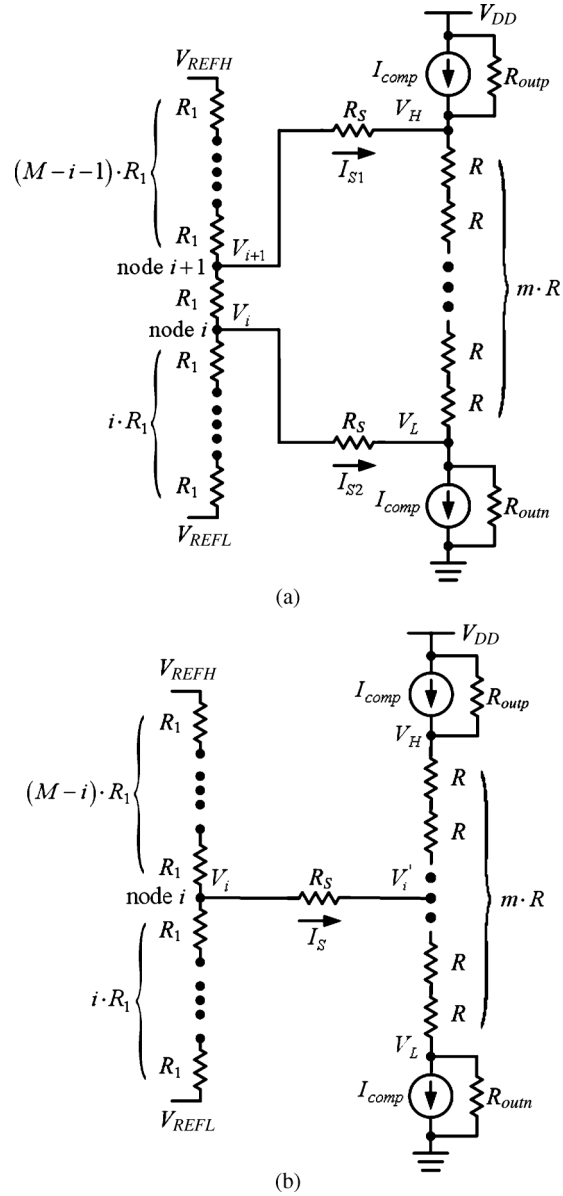

Fig. 3. Simplified FR-DACs based on (a) a two-voltage-selection scheme and (b) a one-voltage-selection scheme for analyzing the loading effect.

where ΔI_S denotes the current difference between I_{S2} and I_{S1}. The voltage difference between the top and bottom ends of the floating resistor string is then obtained as

$$\begin{aligned} V_H - V_L &= (V_{i+1} - V_i) - I_{S1} R_S + I_{S2} R_S \\ &\cong \frac{(V_{\mathrm{REFH}} - V_{\mathrm{REFL}})}{M} + \frac{\Delta I_S \cdot i \cdot (M-i)}{M} R_1 \\ &\quad + \Delta I_S R_S. \end{aligned} \tag{3}$$

The second and third terms of the right-hand side of (3) are the error voltages due to the loading effect to the first-stage resistor string. Because these error voltages are proportional to the current difference between I_{S1} and I_{S2}, they are cancelled in a first order. Hence, the error voltages due to the finite output resistance of the compensation current source/sink are rather small.

A similar analysis can be performed for the one-voltage-selection scheme FR-DAC. Fig. 3(b) illustrates the simplified

FR-DAC based on a one-voltage-selection scheme for analyzing the loading effect. The voltage selector chooses one voltage (V_i) from the first-stage resistor string and, then, connects it to one point of the floating-resistor string. A situation in which the selected voltage is close to VDD implies that a current (I_S) flows from the first-stage resistor string to the floating-resistor string. The voltage at the connected point of the floating resistor string is obtained as

$$V_i' = \frac{i \cdot (V_{\mathrm{REFH}} - V_{\mathrm{REFL}})}{M} + V_{\mathrm{REFL}} - I_S \frac{i \cdot (M-i) \cdot R_1}{M} - I_S R_S. \tag{4}$$

The third and fourth terms of the right-hand side of (4) are the error voltages, which vary with the selected node of the first-stage resistor string. When one of the tail ends of the first-stage resistor string is connected to the floating resistor string, the first-stage resistor string burdens the heaviest loading. Hence, the maximal error voltage is

$$\begin{aligned} V_{err,\max.} &= V_i'\big|_{i=1 \text{ or } M-1} \\ &= I_S \left[\frac{(M-1)R_1}{M} + R_S \right] \\ &\cong I_S(R_1 + R_S). \end{aligned} \tag{5}$$

The error voltage should be smaller than $0.5V_{LSB}$. Because current I_S is due to the finite output resistance of the compensation current source, the minimal requirement for the output resistance $(R_{out,\min.})$ of the compensation current source can be estimated as

$$\begin{aligned} R_{out,\min.} &= \frac{V_{LSB}}{I_S} \\ &= \frac{V_{LSB}}{\frac{0.5V_{LSB}}{(R_1+R_S)}} \\ &= 2(R_1 + R_S). \end{aligned} \tag{6}$$

In this work, a resistance of 380 Ω was used for R_1. The switch on-resistance between the input and output of the voltage selector is approximately 10.8 KΩ. Hence a minimal value of 23 KΩ is required for the output resistance of the compensation current source and sink. For a general design, a larger value of the output resistance must be achieved because the error is not only due to the finite output resistance of the compensation current source and sink.

Comparing the error voltages between these two FR-DACs reveals that the two-voltage-selection FR-DAC has a better linearity than one-voltage-selection FR-DAC. The deviation voltage outputs (DVOs) of the two-voltage-selection FR-DACs are then expected to have smaller values than those of the one-voltage-selection FR-DACs when these two FR-DACs are used in LCD column driver ICs.

A. RFR-DAC With a Two-Voltage-Selection Floating-Resistor String

Fig. 4 shows the proposed 10-bit RFR-DAC in which a 6-bit RDAC and a 4-bit two-voltage-selection FR-DAC are combined without the need of unity-gain buffers to isolate parallel-connected resistor strings. In a column driver chip, a 6-bit global resistor string $(64R_1)$ is used. Each output channel has a

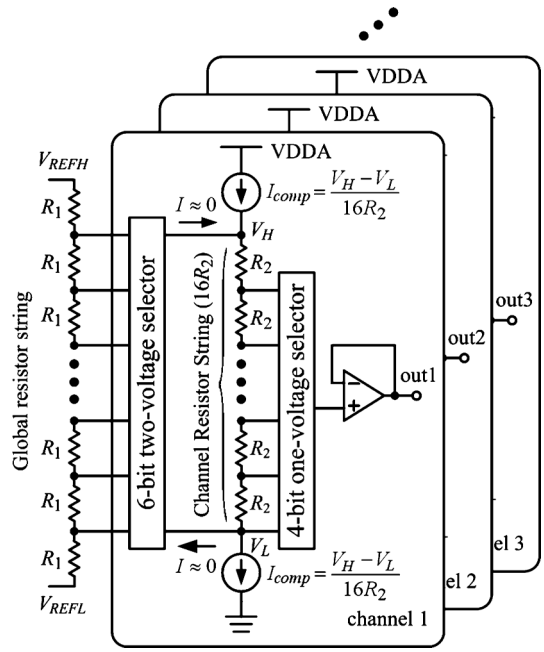

Fig. 4. Architecture of 10-bit RFR-DAC with two-voltage-selection scheme.

6-bit two-voltage selector, 4-bit channel floating-resistor string $(16R_2)$, 4-bit one-voltage selector, and output buffer. Based on higher 6-bit data signals, the 6-bit voltage selector chooses two adjacent node voltages (V_H and V_L) from the global resistor string and, then, connects them to the 4-bit channel floating-resistor string. For lower 4-bit data signals, the 4-bit channel floating-resistor string divides the output voltage into 16 levels between V_H and V_L. The 4-bit voltage selector further chooses a voltage from the channel floating-resistor string and, then, connects it to the output buffer. The current flowing in the channel floating-resistor string is $(V_H - V_L)/16R_2$. To minimize the loading effect, the compensation current source (sink) with the same value of $(V_H - V_L)/16R_2$ is injected into (drawn from) the top (bottom) ends of the channel floating-resistor string simultaneously. Thus, only a negligible static current flows between the global and channel resistor strings. Consequently, the reference voltages of the global resistor string remain intact.

B. RFR-DAC With a One-Voltage-Selection Floating-Resistor String

The RFR-DAC with a one-voltage-selection floating-resistor string possesses an identical architecture as that of RFR-DAC with a two-voltage-selection floating-resistor string except for the connection between the global resistor string and the channel floating-resistor string. Fig. 5 shows the proposed 10-bit RFR-DAC with a one-voltage-selection floating-resistor string. Each output channel has a 6-bit one-voltage selector, 4-bit channel floating-resistor string $(16R_2)$, 4-bit one-voltage selector, and output buffer. Because the channel floating-resistor string conveys a high output impedance at any node of the resistor string, the output of 6-bit voltage selector can be connected to any node of the floating-resistor string without significantly burdening the global resistor string. The operation resembles that of the RFR-DAC with a two-voltage-selection

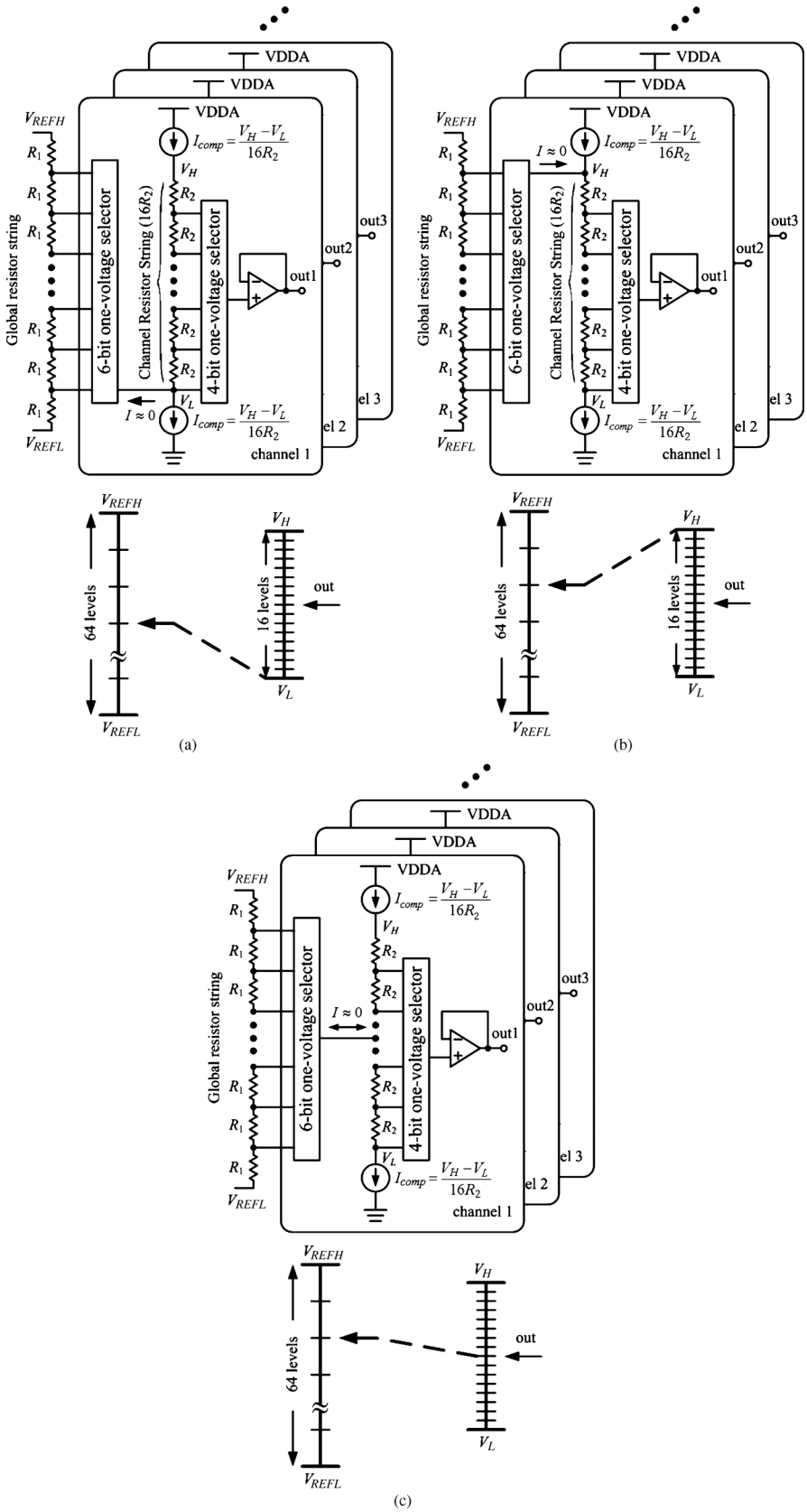

Fig. 5. Architecture of proposed 10-bit RFR-DAC with a one-voltage-selection floating-resistor string. (a) Channel floating-resistor string generates 16 voltage levels above the selected voltage (V_L). (b) Channel floating-resistor string generates 16 voltage levels below the selected voltage (V_H). (c) Channel floating-resistor string generates 16 voltage levels around the selected voltage.

floating-resistor string. Fig. 5(a) reveals that the 6-bit voltage selector chooses one voltage (V_L) from the global resistor string and, then, connects it to the bottom end of the 4-bit channel floating-resistor string. The channel floating-resistor

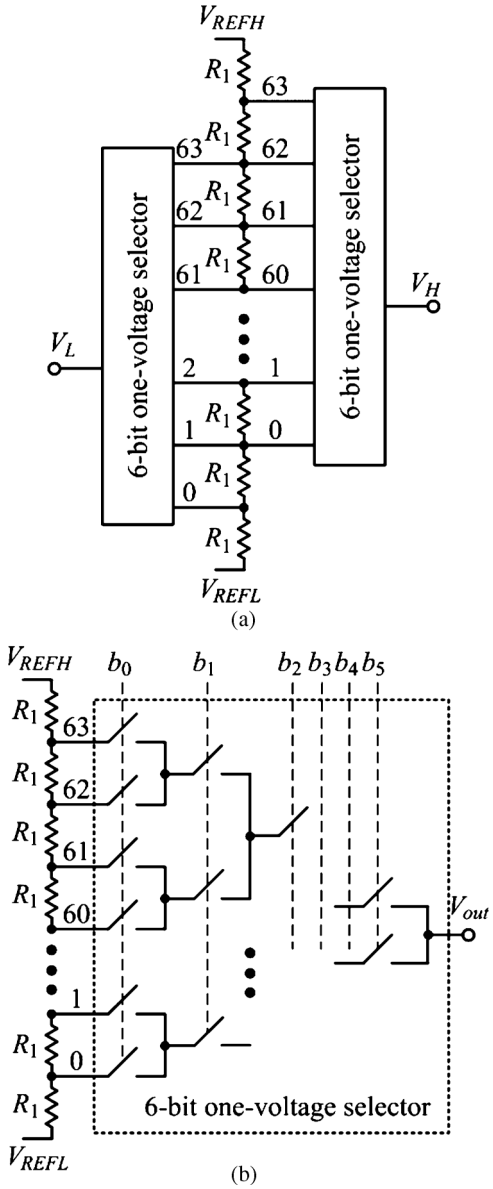

Fig. 6. (a) Two-voltage selector. (b) One-voltage selector.

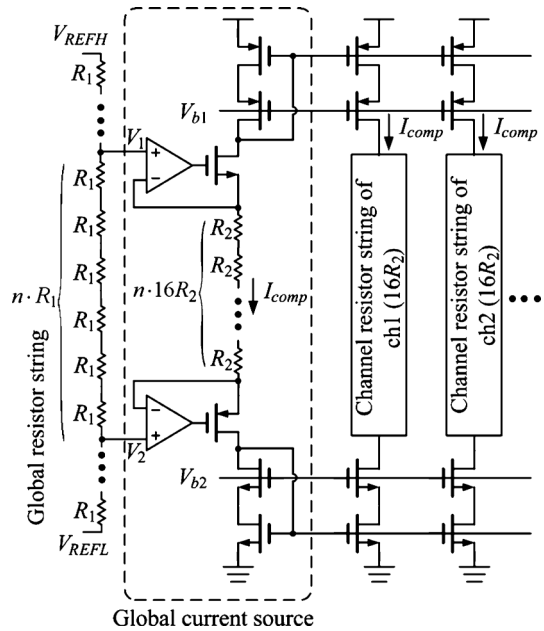

Fig. 7. Schematic of global compensation current source.

string generates 16 voltage levels above the selected voltage (V_L). Similarly, the channel floating-resistor string generates 16 voltage levels below the selected voltage by connecting the selected voltage (V_H) to the top end of the channel floating-resistor string, as shown in Fig. 5(b). Moreover, the selected voltage can be connected to any node of the channel floating-resistor string, as shown in Fig. 5(c).

C. Voltage Selectors

The RFR-DAC with a two-voltage-selection floating-resistor string requires a two-voltage selector to choose two adjacent node voltages from the global resistor string. Fig. 6(a) shows such a selector consisting of two sets of 6-bit one-voltage selector, mutually with a one-bit offset. One set outputs V_H, whereas the other outputs V_L. However, the RFR-DAC with a one-voltage-selection floating-resistor string requires only one selector to choose a voltage from the global resistor string. Fig. 6(b) shows such a selector consisting of only one set of 6-bit switch array and occupying a smaller die area than its two-voltage-selection counterpart. The switch matrix is connected in a treelike manner, eliminating the need for a digital decoder. Notably, for a 6-bit resolution, 126 switch components are required.

D. Compensation Current Source

Compensation currents of all channels for a column driver are mirrored from a global compensation current source to reduce the area and power overhead. This global compensation current source senses a voltage difference between two nodes from the middle of the global resistor string and, correspondingly, produces the proper compensation current, as shown in Fig. 7. Because the sensed voltage difference is $n \cdot (V_H - V_L)$, and the total value of the resistor string in the global compensation current source is n times that in the channel resistor string, the compensation current is therefore set to

$$I_{comp} = \frac{n \cdot (V_H - V_L)}{n \cdot 16R_2} = \frac{V_H - V_L}{16R_2}. \tag{7}$$

E. Output Buffer

A two-stage class-AB operational amplifier (op-amp) is cascaded through a unity-gain buffer to drive highly capacitive column lines. Fig. 8 schematically depicts the proposed buffer amplifier, which is constructed by a rail-to-rail input differential amplifier (M1–M10), pair of stacked floating class-AB controls (M11–M18), and output stage (M19–M20). The stacked floating class-AB control, as modified from a floating class-AB control [21], [22], designates the quiescent current of the output transistors precisely, rendering it insensitive to the supply voltage. The stacked diode-connected transistors (Mb1–Mb2 and Mb3–Mb4) in the global bias circuit are used to bias the gates of the stacked floating class-AB control transistors (M11, M15 and M13, M17, respectively). The floating class-AB con-

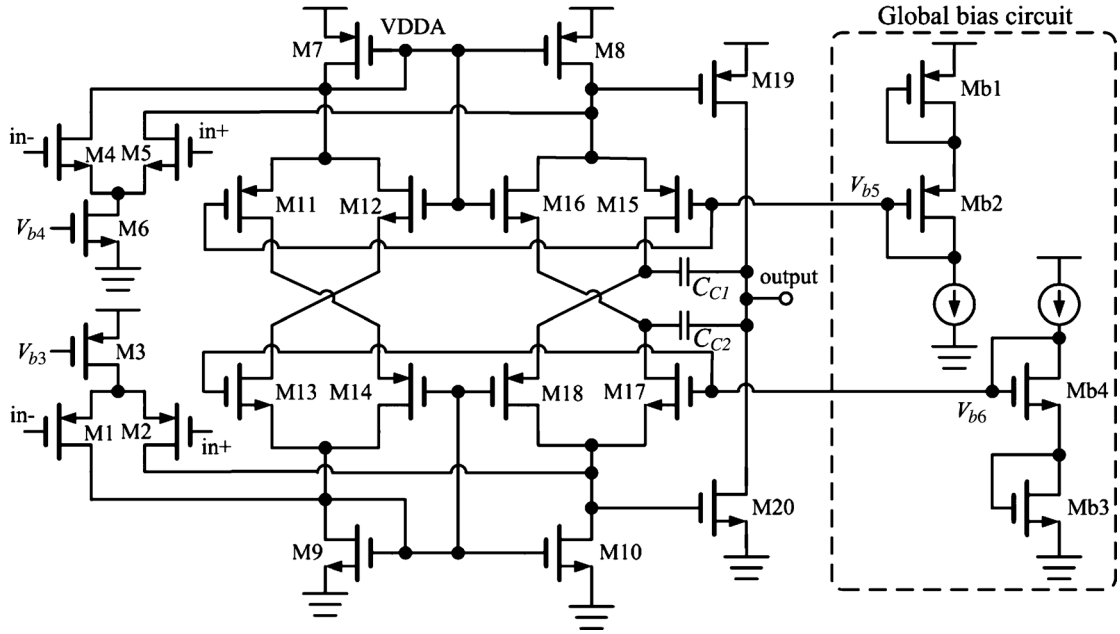

Fig. 8. Schematic of proposed buffer amplifier.

trol transistors, stacked diode-connected transistors, and output transistors set up two translinear loops (M15, M19, Mb1, Mb2, and M17, M20, Mb3, Mb4), which determine the quiescent current at the output stage.

This sub-section is intended to discuss the required DC open-loop gain, bandwidth, phase margin, slew rate, and power consumption of the op-amp used in LCD drivers. For an N bit resolution, the minimum required DC open-loop gain, A_{OLDC}, can be estimated as [23]

$$A_{OLDC} \geq 2^{N+1}. \tag{8}$$

A 10-bit DAC would require op-amp's DC open-loop gain greater than 66 dB and in the meantime, the op-amp may largely limit the speed of an RDAC. For a large-signal step response, settling time is the sum of the slew-rate limiting settling time and the small-signal settling time [24]. Small-signal settling time is related to the op-amp gain-bandwidth (f_u) and phase margin. If the phase margin is assumed to be 90°, the op-amp output response is an RC-like settling response shape. Then, for an N bit resolution, the minimal gain-bandwidth of the unity-gain buffer amplifier required for a specific settling time t_s can be estimated by [23]

$$f_u \geq \frac{\ln 2^{N+1}}{2\pi \cdot t_s}. \tag{9}$$

If 1 μs is assigned to the minimal small-signal settling time, the gain-bandwidth of the buffer amplifier used in a 10-bit DAC will exceed 1.2 MHz. If the op-amp phase margin is 70°, the step response shows a moderate amount of ringing. Decreasing the phase margin will cause increase of the peak amplitude of the ringing and lengthens the small-signal settling time.

The slew-rate limiting settling time can be approximated by dividing the bias current of differential pairs over the compensation capacitance value. To achieve a larger slew rate, the compensation capacitance value has to be smaller. However, a tradeoff need to be be made between the slew rate and phase margin if a lower compensation capacitance value is desired. Increasing the differential pair's bias current may raise the slew rate but at the expense of excessive power consumption.

Some buffer amplifiers adopt the output node as a dominant pole to achieve sufficient stability without a Miller capacitance [25]–[27]. However, charge conservation technology is commonly used in LCD drivers to reduce power consumption by decreasing the average voltage swing [28], [29]. Refreshing voltage level of data lines consists of three phases. First, all data lines are isolated from the buffer outputs. The data lines are then shorted to an external capacitor. During the final phase, all data lines are connected to corresponding buffer amplifiers, which continue to drive data lines to their final values. Since buffer amplifiers based on the charge conservation technology are configured and unloaded in the first and second phases, these amplifiers require Miller compensation to achieve better stability [30], [31]. Furthermore, the Miller compensation scheme lowers the required capacitor value and reduces the required bias current for a specific slew rate. However, a two-stage op-amp incorporating Miller compensation contains a right-half-plane zero, which arises from the feed-forward path formed by the compensation capacitor. To overcome this problem, this work implements the stacked floating class-AB control in a series with the compensation capacitor to isolate the feed-forward path from the output of the first stage to the output of the second stage. The compensation capacitors offer the feedback current from the output to inputs of the second stage through common-gate amplifiers, M16 and M18. Despite the feed-forward paths exist through M15 and M17, transistor sizes can be adjusted properly to eliminate the right half plane zero. The Appendix provides details of the stability analysis.

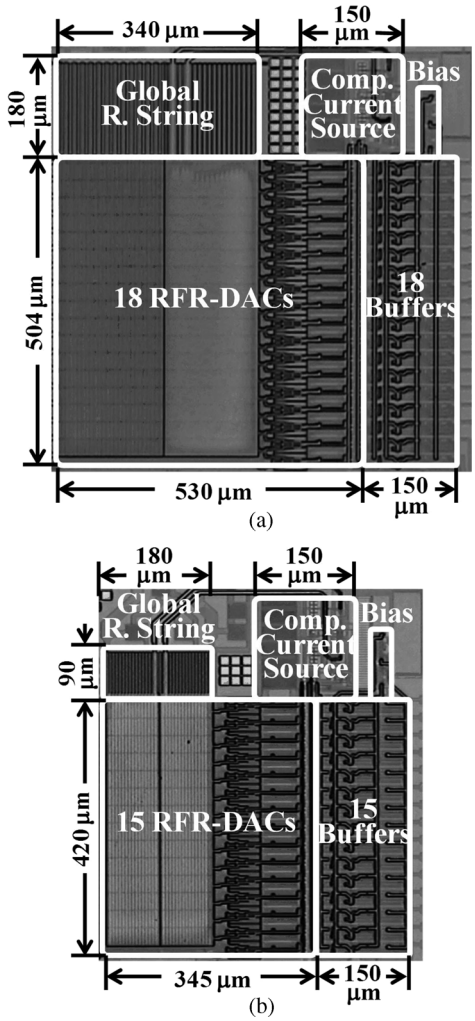

Fig. 9. Die photographs for (a) 18 channel RFR-DACs with two-voltage-selection scheme and 18 buffers, and (b) 15 channel RFR-DACs with one-voltage-selection scheme and 15 buffers.

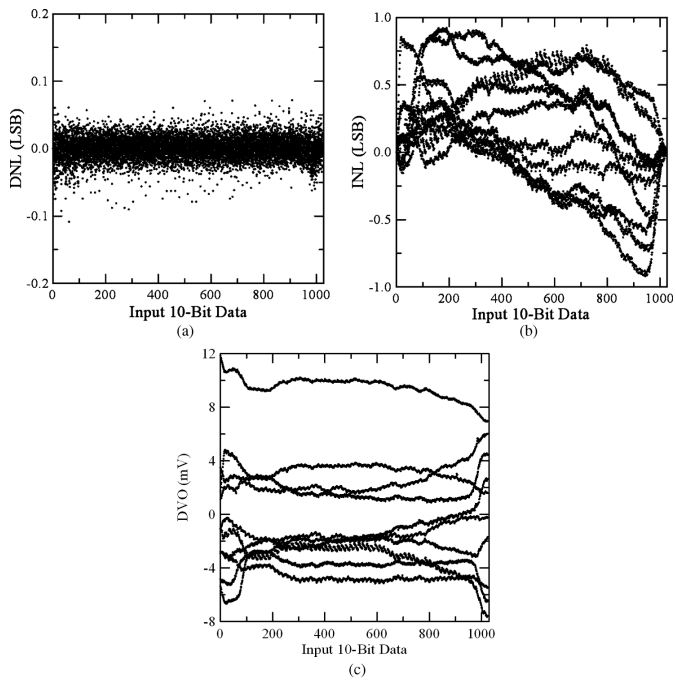

Fig. 10. Measured (a) DNL, (b) INL, and (c) DVO in terms of a linear 10-bit grayscale for RGB-separate gamma on 10 different chips for the two-voltage-selection RFR-DAC.

III. Experimental Results

By using 0.35-μm/0.5-μm two-poly-four-metal (2P4M) CMOS technology, this work fabricated two prototypes to validate the performance of the 10-bit RFR-DAC with either a one- or two-voltage-selection floating-resistor string. Although the process variation of poly resistors is smaller than that of diffusion resistors, the latter possess a larger sheet resistance value. For the 0.35-μm/0.5-μm 2P4M CMOS technology, the sheet resistances of the poly 1 and p+ diffusion are 8 $\Omega/\square$ and 150 $\Omega/\square$, respectively. In this work, better linearity is achieved by using poly 1 as the global resistor string. The p+ diffusion resistor is used for the channel resistor string to conserve the channel area. Fig. 9(a) and (b) shows the die photographs with sizes of 530 μm $\times$ 504 μm and 150 μm $\times$ 504 μm for 18 channel RFR-DACs with two-voltage-selection floating-resistor string and 18 buffers, respectively, and of 345 μm $\times$ 420 μm and 150 μm $\times$ 420 μm for 15 channel RFR-DACs with one-voltage-selection floating-resistor string and 15 buffers, respectively. The test pattern was applied concurrently to all channel inputs. Fig. 10(a), (b), and (c) shows the measured DNL, INL, and DVO in terms of a linear 10-bit grayscale for RGB-separate gamma on 10 different chips for the two-voltage-selection RFR-DAC. The worst DNL and INL are measured as 0.11 LSB and 0.92 LSB, respectively (1 LSB = 4.4 mV). DVO is also tested according to 1024 grayscales on 10 chips. Without applying any off-chip trimming, the maximum inter-chip DVO is 19.5 mV. Every DVO curve shows a larger deviation at the both ends of the digital code. This is due to finite output resistances of the compensation current source and sink. The INL curves show the similar behavior with systematic bends detected at both ends. Fig. 11 shows the measured output waveform with a 30 KΩ-resistance and 30 pF-capacitance load, as the digital data change from "000_{16}" to "$3FF_{16}$". Settling time within 0.2% of the final voltage is 4 μs. Fig. 12(a), (b), and (c) shows the measured DNL, INL, and DVO from 10 chips for the 10-bit RFR-DAC with a one-voltage-selection scheme. The worst DNL, INL, and DVO are 1.37 LSB, 1.45 LSB, and 22 mV, respectively. The two-voltage-selection scheme RFR-DAC has a better linearity, which corresponds with the theoretical analysis results of (3) and (4).

Since we use pass transistor logic circuits as voltage selectors, only the compensation source/sink and buffer amplifiers of channel drivers consume quiescent currents. As a result, 10-bit RFR-DAC channel drivers with one- or two-voltage-selection floating-resistor strings consume quiescent currents of 1.2 μA, and 1.18 μA, respectively. The DAC die area is compared with those of the state-of-the-art circuits by generating the layouts using standard 90-nm CMOS technology for the proposed RFR-DACs. The p+ poly resistor without salicide is used for the channel resistor string. Its sheet resistance is 402.1 $\Omega/\square$. Fig. 13 shows the areas of the proposed 10-bit RFR-DACs with (a) 0.35-μm/0.5-μm and (b) 90-nm

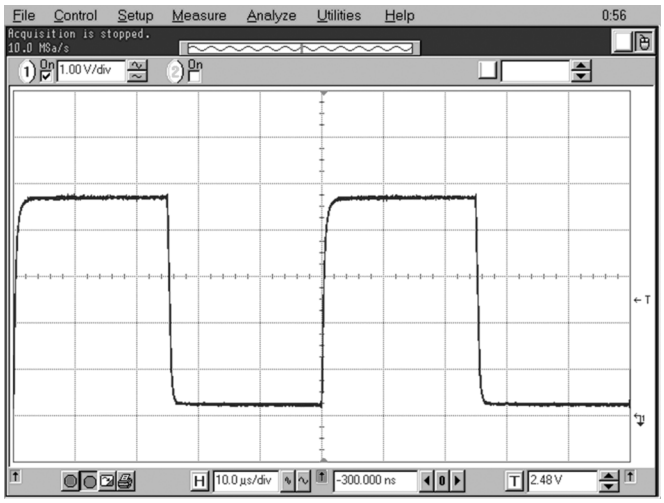

Fig. 11 Measured output waveform with a 30 $\mathrm{K}\Omega$-resistance and 30 pF-capacitance load when the digital data change from "000_{16}" to "$3\mathrm{FF}_{16}$".

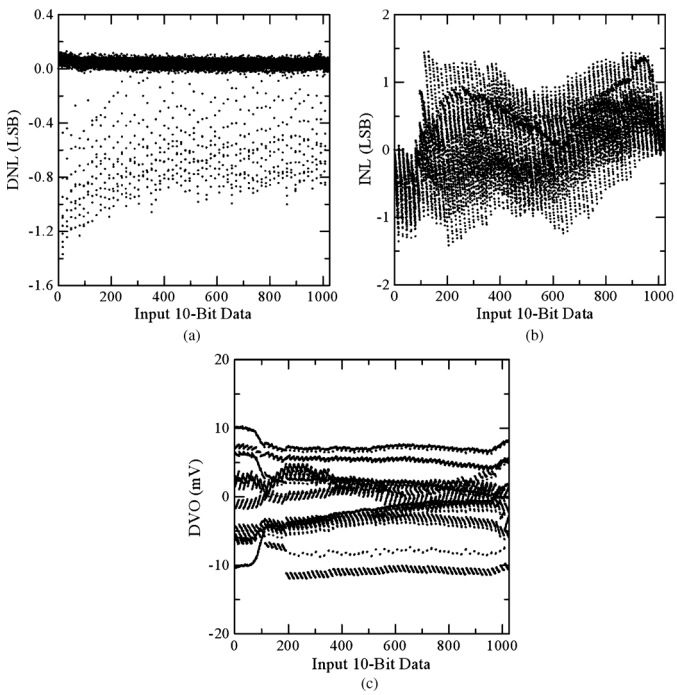

Fig. 12. Measured (a) DNL, (b) INL, and (c) DVO from 10 chips for the 10-bit RFR-DAC with a one-voltage-selection scheme.

CMOS technologies. Because of the smaller required minimal width and spacing of metal and poly, as well as smaller device sizes with advanced technologies, the areas of the proposed circuits implemented with 90-nm technology are much more compact than those of the same circuits implemented with 0.35-μm/0.5-μm technology. By using 0.35-μm/0.5-μm 2P4M CMOS technology the area is 680 μm $\times$ 28 μm for an RFR-DAC with a two-voltage-selection floating-resistor string and an output buffer, and of 495 μm $\times$ 28 μm for RFR-DAC with one-voltage-selection floating-resistor string and one buffer. The areas of two RFR-DACs are significantly reduced to 185.5 μm $\times$ 12.2 μm and 164.5 μm $\times$ 12.2 μm, respectively, with 90-nm CMOS technology. Table I shows the simulated

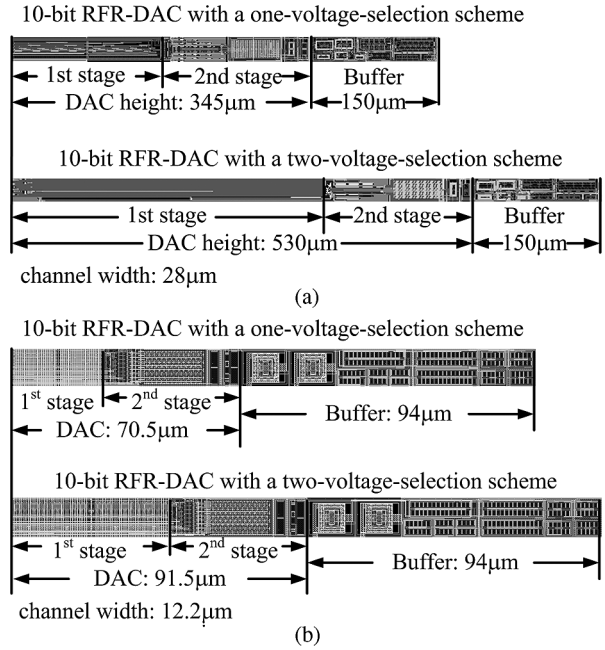

Fig. 13. Areas of the proposed 10-bit RFR-DACs with (a) 0.35-μm/0.5-μm and (b) 90-nm CMOS technologies.

TABLE I
SIMULATED PERFORMANCE OF THE TWO 10-BIT RFR-DACS WITH 90-nm CMOS TECHNOLOGY

	* RFR-DAC-I	**RFR-DAC-II
Technology	90 nm CMOS (1P9M)	90 nm CMOS (1P9M)
Gray scale	10 bit	10 bit
Output range	0.2V to 4.7V	0.2V to 4.7V
DNL/INL	0.033/0.064 LSB	0.217/0.31 LSB
Static current	1.21µA/channel	1.21 µA/channel
One10-bit DAC area	91.5×12.2 µm^2	70.5×12.2 µm^2
Output buffer area	94×12.2 µm^2	94×12.2 µm^2

* RFR-DAC with two-voltage-selection scheme.

** RFR-DAC with one-voltage-selection scheme.

performance of the two 10-bit RFR-DACs with 90-nm CMOS technology. Table II summarizes the performance of the 10-bit RFR-DAC in comparison with the state-of-the-art circuits. The proposed two-voltage-selection RFR-DAC has the lowest DNL value, and its area with 90-nm technology is smaller than those of the state-of-the-art DACs. Although two-voltage-selection RFR-DAC demonstrates better linearity, its area is inevitably larger than that of the one-voltage-selection RFR-DAC.

IV. CONCLUSIONS

This work presents a novel prototype of a 10-bit RFR-DAC with either one- or two-voltage-selection schemes to improve the linearity and uniformity of the channel performance, and maintain a 10-bit resolution at a size smaller than those of the state-of-the-art 10-bit DACs. This work also realizes a rail-to-rail class-AB operational amplifier with a stacked floating class-AB control for LCD driver ICs. RFR-DACs implemented in a 0.35-μm/0.5-μm CMOS technology displays the worst DNL = 0.11 LSB and INL = 0.92 LSB, respectively,

TABLE II
PERFORMANCE SUMMARY

	[12]	[13]	* RFR-DAC-I	**RFR-DAC-II
Technology	0.1μm CMOS (1P5M)	0.1μm CMOS (1P5M)	0.35 μm/0.5 μm CMOS (2P4M)	0.35 μm/0.5 μm CMOS (2P4M)
Gray scale	10 bit	10 bit	10 bit	10 bit
Output range	0V to 5V	0.25V to 4.75V	0.2V to 4.7V	0.2V to 4.7V
DNL/INL	0.37/1.71 LSB	0.4/0.7 LSB	0.11/0.92 LSB	1.37/1.45 LSB
Max. DVO	6.35 mV	20 mV	19.5 mV	22 mV
Static current	1.2μA/channel	1μA/buffer	1.18μA/channel	1.2 μA/channel
One10-bit DAC area	206×14 μm^2	195x14 μm^2	530×28 μm^2 (0.35 μm/0.5 μm tech.) 91.5×12.2 μm^2 (90 nm tech.)	345×28 μm^2 (0.35 μm/0.5 μm tech.) 70.5×12.2 μm^2 (90 nm tech.)
Output buffer area	127×14 μm^2	125x14 μm^2	150×28 μm^2 (0.35 μm/0.5 μm tech.) 94×12.2 μm^2 (90 nm tech.)	150×28 μm^2 (0.35 μm/0.5 μm tech.) 94×12.2 μm^2 (90 nm tech.)

* RFR-DAC with two-voltage-selection scheme.

** RFR-DAC with one-voltage-selection scheme.

from a two-voltage-selection scheme and DNL = 1.37 LSB and INL = 1.45 LSB, respectively, from a one-voltage-selection scheme. The proposed two-voltage-selection RFR-DAC has the lowest DNL value and its area with 90-nm technology is smaller than those of the state-of-the-art circuits. With the settling time of 4 μs within 0.2% of the final voltage, the proposed RFR-DAC is highly promising for both small- and large-size high color-depth LCD applications.

APPENDIX

This appendix describes the stability analysis for the proposed class-AB amplifier. Fig. 14 shows a simplified small-signal equivalent circuit for the buffer amplifier by reducing the differential injection scheme (M1–M6) to be single-sided and neglecting the channel length modulation of M15–M18. Where R_{O1} and R_{O2} refer to the output resistance of the first and second stages, respectively; G_{m1} represents the transconductance of differential pairs; g_{m16}, g_{m17}, g_{m18}, and g_{m20} are transconductance of M16, M17, M18, and M20, respectively; C_{O2} denotes the parasitic capacitance at the output node of the second stage; C_{C1} and C_{C2} refer to the Miller compensation capacitors; and R_L and C_L denote the resistive and capacitive loads, respectively. By assuming that $C_{C1} = C_{C2} = C_C$, the open-loop transfer function, v_{out}/v_{id}, can be obtained from Fig. 14, that is,

$$\frac{v_{out}}{v_{id}} = \frac{A_0\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \quad (10)$$

where

$$A_0 = G_{m1}g_{m20}R_{O1}R_{O2} \quad (11)$$

$$\omega_{z1} \cong \frac{1}{C_L R_L} \quad (12)$$

$$\omega_{z2} \cong \frac{g_{m16}g_{m18}g_{m20}}{C_C(g_{m20}-g_{m17})(g_{m18}+g_{m16})} \cong \frac{g_{m16}g_{m20}}{2C_C(g_{m20}-g_{m17})} \quad (13)$$

$$\omega_{z3} \cong \frac{(g_{m20}-g_{m17})(g_{m16}+g_{m18})}{C_C(g_{m20}-g_{m18})} \cong \frac{g_{m16}+g_{m18}}{C_C} \quad (14)$$

$$\omega_{p1} \cong \frac{1}{2C_C g_{m20}R_{O1}R_{O2}+C_L R_{O2}} \quad (15)$$

$$\omega_{p2} \cong \frac{(2C_C g_{m20}+C_L/R_{O1})g_{m16}g_{m18}}{C_C C_L g_{m17}(g_{m16}+g_{m18})} \cong \frac{1}{2C_C R_{O1}} \quad (16)$$

$$\omega_{p3} \cong \frac{g_{m17}(g_{m16}+g_{m18})}{C_C(g_{m17}+g_{m18}g_{m20}R_L)} \cong \frac{g_{m16}+g_{m18}}{C_C} \quad (17)$$

$$\omega_{p4} \cong \frac{g_{m17}+g_{m18}g_{m20}R_L}{C_{O2}g_{m17}R_L} \cong \frac{1}{C_{O2}R_L}. \quad (18)$$

The unity-gain frequency can be approximately expressed as

$$\omega_t \cong A_0\omega_{p1} \cong \frac{G_{m1}}{2C_C}. \quad (19)$$

A negative term, $-g_{m17}$, can be found in the denominator of the expression for ω_{z2}, which is owing to that M17 conducts a feed-forward path from the input of the second stage to the output through C_{C2}. If the transconductance of M20 exceeds that of M17, then the zero is moved into the left-half plane to cancel out the first non-dominant pole, ω_{p2}. Additionally, ω_{z3}

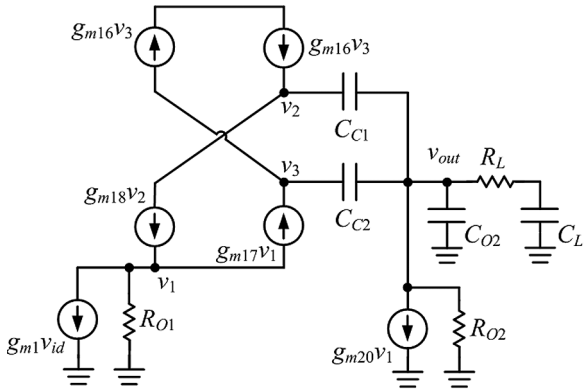

Fig. 14. Simplified small-signal equivalent circuit of proposed buffer amplifier.

compensates for the second non-dominant pole, ω_{p3}. The third non-dominant pole is far away from the unity gain frequency, thus affecting the phase margin negligibly.

When the amplifier is operated without a load, the open-loop transfer function becomes

$$\frac{v_{out}}{v_{id}} = \frac{A_0\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \tag{20}$$

where

$$\omega_{z1} \cong \frac{g_{m16}g_{m20}}{2C_C(g_{m20}-g_{m17})} \tag{21}$$

$$\omega_{z2} \cong \frac{g_{m16}+g_{m18}}{C_C} \tag{22}$$

$$\omega_{p1} \cong \frac{1}{2C_C g_{m20} R_{O1} R_{O2}} \tag{23}$$

$$\omega_{p2} \cong \frac{2g_{m16}}{C_C} \tag{24}$$

$$\omega_{p3} \cong \frac{g_{m18}g_{m20}}{C_{O2}g_{m17}}. \tag{25}$$

The compensation scheme of the load-less amplifier can be similar to that of amplifiers with either a resistive or capacitive load. The first zero, ω_{z1}, can compensate for the first non-dominant pole, ω_{p2}, if the transconductance of M20 exceeds that of M17. The second non-dominant pole, ω_{p3}, located far from the unity-gain frequency, only slightly affect the phase margin. Consequently, the proposed amplifier can be used for LCD driver ICs with the charge conservation technique. To demonstrate the stability of the amplifier, the open-loop response of the amplifier was simulated by using 90-nm CMOS parameters. The device sizes used in the amplifier are shown in Table III. Fig. 15 shows the simulated open-loop responses of the amplifier (a) with a 30 KΩ-resistance and 30 pF-capacitance load and (b) without a load. The DC voltage gain is 92 dB, and the unity-gain frequencies are 1.5 MHz and 11.7 MHz, respectively, with a 30 KΩ-resistance and 30 pF-capacitance load and without a load. These data correspond with the minimal required values in 10-bit DACs. Their phase margins are 94° and 89°, respectively. Consequently, the proposed amplifier can be used for LCD driver ICs with the charge conservation technique.

TABLE III
DEVICE SIZES USED IN THE AMPLIFIER

M1	$\frac{1.5\mu\times12}{1\mu}$	M7	$\frac{1.5\mu\times12}{1\mu}$	M13	$\frac{1.5\mu}{1\mu}$	M19	$\frac{2\mu\times8}{0.8\mu}$
M2	$\frac{1.5\mu\times12}{1\mu}$	M8	$\frac{1.5\mu\times12}{1\mu}$	M14	$\frac{1.5\mu\times3}{1\mu}$	M20	$\frac{2\mu\times3}{0.8\mu}$
M3	$\frac{1.5\mu\times6}{1\mu}$	M9	$\frac{1.5\mu\times4}{1\mu}$	M15	$\frac{1.5\mu\times3}{1\mu}$	C_{C1}	0.08 pF
M4	$\frac{1.5\mu\times12}{1\mu}$	M10	$\frac{1.5\mu\times4}{1\mu}$	M16	$\frac{1.5\mu}{1\mu}$	C_{C2}	0.08 pF
M5	$\frac{1.5\mu\times12}{1\mu}$	M11	$\frac{1.5\mu\times3}{1\mu}$	M17	$\frac{1.5\mu}{1\mu}$		
M6	$\frac{1.5\mu\times2}{1\mu}$	M12	$\frac{1.5\mu}{1\mu}$	M18	$\frac{1.5\mu\times3}{1\mu}$		

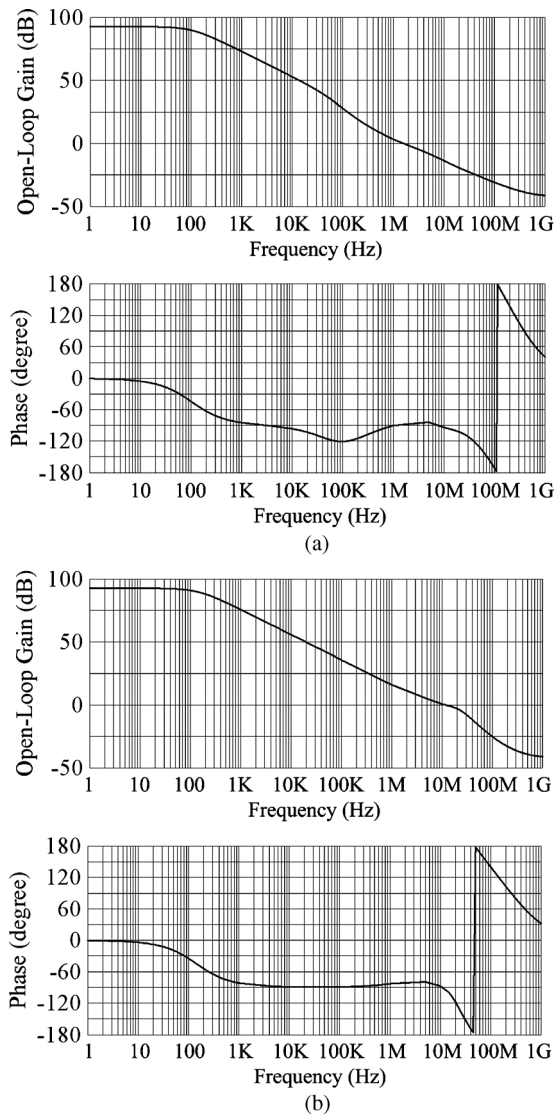

Fig. 15. Simulated open-loop responses of the amplifier (a) with a 30 KΩ-resistance and 30 pF-capacitance load and (b) without a load.

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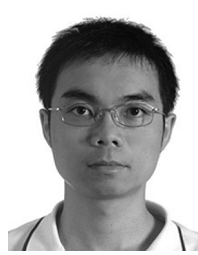
His research interests include LCD driver design and RFIC design.



Ching-Min Hsiao was born in Taiwan on March 22, 1977. He received the B.S. degree in electronic engineering from Feng Chia University, Taichung, in 2000 and the M.S. degree in electrical engineering from National Chi Nan University, Puli, Nan-Tou, Taiwan, in 2004, where he is currently pursuing the Ph.D. degree in electrical engineering.

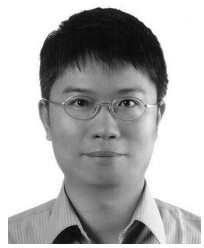
His research interests focus on LCD driver design.

Mau-Chung Frank Chang (M'79–SM'94–F'96) is the Department Chairman and the Wintek Chair Professor of Electrical Engineering at the University of California at Los Angeles (UCLA).

Before joining UCLA, he was the Assistant Director of the High Speed Electronics Laboratory at Rockwell Science Center (1983–1997). In this tenure, he developed and transferred GaAs HBT/BiFET IC technologies from the research laboratory to production (now Skyworks). This has grown into multi-billion dollar businesses and dominated cell phone power amplifier markets for the last two decades (currently exceeding one billion units/year).

Throughout his career, his research has primarily focused on the development of high-speed semiconductor devices and integrated circuits for RF & mixed-signal communication, radar and imaging system applications. He was the PI at Rockwell in leading DARPA's multi-Gb/s ADC/DAC development for direct conversion transceiver (DCT) and digital radar receivers (DRR). He invented multiband, reconfigurable RF-Interconnects, based on FDMA multiple access algorithms, for inter-CMP-core and inter-CPU/Memory communications. He also pioneered the development of 60 GHz radio transceiver front-end based on transformer-folded-cascode (Origami) high-linearity circuit topology; and the low phase noise CMOS VCO (F.O.M. < -200 dBc/Hz) with Digitally Controlled on-chip Artificial Dielectric (DiCAD). He also first demonstrated CMOS oscillators in Terahertz frequency range (1.3 THz) and demonstrated the first CMOS active imager at the sub-mm-Wave spectra (180–500 GHz) based on a Time-Encoded Digital Regenerative Receiver and 3-dimensional SAR radar with <1 cm resolution at 144 GHz.

Dr. Chang is a member of the US National Academy of Engineering and an IEEE Fellow, and was elected to Taiwan's Academia Sinica in 2012. He received the IEEE David Sarnoff Award in 2006 for developing and commercializing HBT power amplifiers for modern wireless communication systems.



Yo-Sheng Lin (M'02–SM'06) was born in Puli, Taiwan, on October 10, 1969. He received the Ph.D. in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1997. His Ph.D. thesis was on the fabrication and study of GaInP-InGaAs-GaAs doped-channel field-effect-transistors and their applications to monolithic microwave integrated circuits.

He joined Taiwan Semiconductor Manufacturing Company in 1997 as a Principal Engineer for 0.35/0.32 μm DRAM and 0.25 μm embedded DRAM technology development in the Integration Department of Fab-IV. Since 2000, he has been responsible for 0.18/0.15/0.13 μm CMOS low-power device technology development in the Department of Device Technology and Modeling, R&D, and was promoted to Technical Manager in 2001. In August 2001, he joined the department of Electrical Engineering, National Chi Nan University (NCNU), where he was promoted to an Associate Professor in August 2003, and a full Professor in August 2006. He was a recipient of the Excellent Research Award from NCNU in 2006, a recipient of the Outstanding Young EE Engineer Award from Chinese Institute of Electrical Engineering in 2007, and a recipient of the Excellent Teaching Award from NCNU in 2011. From June to September, 2004, he was a visiting researcher at the High-Speed Electronics Research Department, Bell Laboratories, Lucent Technologies, Murray Hill, NJ. From February 2007 to January 2008, he was appointed as Visiting Professor at the Department of Electrical Engineering, Stanford University, Stanford, CA. His current research interests are in the areas of RFID reader/tag chip design, and ultra-wideband circuits and systems in both microwave and millimeter wave bands.