A 64-fJ/Conv.-Step Continuous-Time ΣΔ Modulator in 40-nm CMOS Using Asynchronous SAR Quantizer and Digital ΔΣ Truncator

Hung-Chieh Tsai, Chi-Lun Lo, Chen-Yen Ho, *Member, IEEE*, and Yu-Hsin Lin

***Abstract*—A third-order single-loop continuous-time sigma-delta modulator (CTSDM) with 6-bit asynchronous successive approximation register (ASAR) quantizer and digital ΔΣ truncator for WCDMA/GSM/EDGE cellular systems is presented. The proposed ASAR-based quantizer reduces the area and power of the modulator dramatically by utilizing the digital truncation technique. By using the 6-bit ASAR quantizer, the sampling frequency is lowered, which reduces the design efforts not only in system level but also in the modulator. In addition, the ac-coupled push–pull stage is employed to improve the high-frequency driving capability of the first integrator. Sampling at 65 MHz, the modulator achieves 83.4 dB dynamic range (DR) and 80/79.6 dB peak SNR/SNDR with 1.92 MHz bandwidth in WCDMA mode. In GSM/EDGE mode, the DR is 96.2 dB. Fabricated in 40-nm CMOS, the modulator occupies 0.051 mm^2 and consumes 1.91 mW from a 1.2-V supply. A 64fJ/conv.-step figure of merit is achieved.**

***Index Terms*—AC-coupled push-pull, asynchronous successive approximation register (ASAR), continuous-time sigma–delta modulator (CTSDM), digital ΔΣ truncator, dynamic element matching (DEM), EDGE, GSM, low sampling frequency, WCDMA.**

I. Introduction

THE integration level of handset solution becomes higher, and the system-on-chip (SoC) solution is more and more popular. High-performance and low-power downlink analog-to-digital converters (ADCs) are always demanded to relax the front-end filtering and pushes the design penalty to the digital circuitry which scales well with process. Multistandard capability is popular in downlink ADC [1]–[3], and Fig. 1 shows an example of the multistandard receiver for WCDMA/GSM/EDGE cellular systems. The separated front-ends support all modes and frequency bands with different local oscillation (LO) frequencies. Moreover, the receiver only uses one I/Q transimpedance amplifier (TIA), channel filter, and ADC. The TIA translates the current from mixer to voltage and the channel selection filter provides sufficient attenuation to avoid overloading the ADC. The dynamic range (DR) of the downlink ADC is determined by the equivalent front-end noise at ADC input, the SNR requirements under the given modulation scheme, peak-to-average ratio (PAR), the reserved DR for adjacent channels, blockers and fading channels, and some margins for gain error and dc offset. The channel selection filter and ADC must be optimized simultaneously because there is a design tradeoff among the filter order number, cutoff frequency, and ADC DR in terms of the reserved DR. Therefore, a high-DR and high-performance ADC is always demanded to relax the requirements of channel selection filter. CTSDM is appropriated for high DR applications and provides inherent anti-aliasing to relax the front-end filtering prior to the downlink ADC. In addition, CTSDM achieves better power efficiency [4]–[8] than the discrete-time (DT) counterparts [9], [10]. Although CTSDM suffers SNR degradation by process variation, this can be alleviated by RC calibration mechanism.

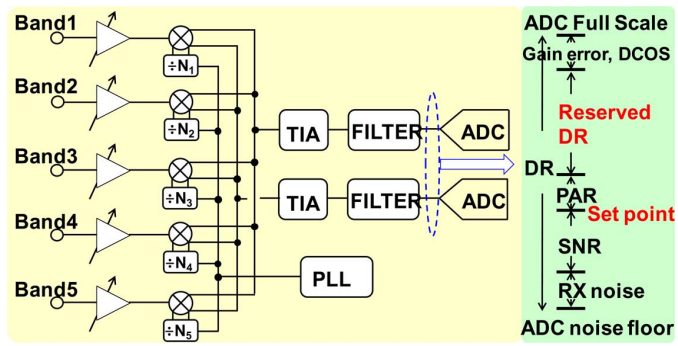

Fig. 1. Block diagram of the WCDMA/GSM/EDGE receiver and the DR budget for the ADC.

Low oversampling ratio (OSR) and multibit [11] CTSDMs serve as a good candidate to provide power-efficient data conversion because of the reduced quantization error, better stability for large-signal, low op-amp current in slewing, and relaxed jitter requirement. Low sampling rate reduces both the system-level design effort and the circuit-level design complexity of the modulator. High-order or high-resolution quantizers can be used to achieve high signal-to-quantization-ratio (SQNR) with low OSR. However, high-order modulator suffers from the stability issue, and it is sometimes complicated to recover from the overload state to normal state when large blockers or adjacent channels apply before automatic gain control (AGC) starting working. Alternatively, a high-resolution quantizer with low OSR can provide more stable modulator but the resolution is limited to four or five because of the design complexity.

The flash ADC-based quantizer is popular in CTSDM. However, it is not power-efficient if the bit number is larger than

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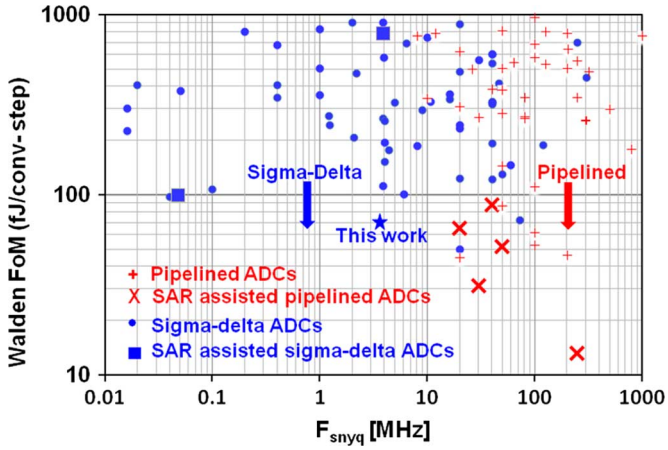

Fig. 2. Walden FOM versus Nyquist bandwidth for pipelined and sigma-delta ADCs.

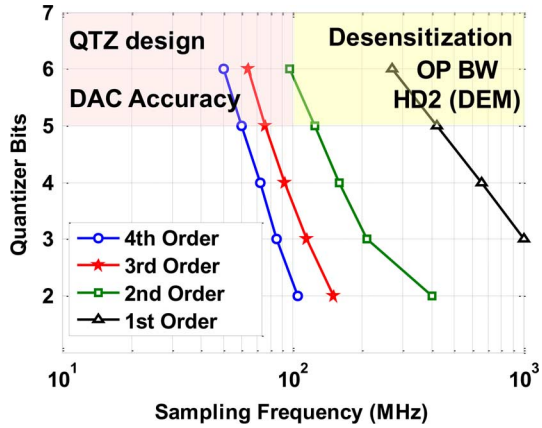

Fig. 3. System-level design considerations to achieve 90-dB SQNR.

five because the number of comparator grows exponentially. Recently, successive approximation register (SAR) ADCs are becoming more and more popular for low power consumption. SAR ADCs, which operate with only one comparator, achieve lower power and higher efficiency than other types of ADCs. While the low-power characteristic of SAR ADCs is attractive, the large number of decision cycles to finish one conversion is a fundamental drawback for high-speed operation. Nowadays, highly digitized architecture of the asynchronous SAR (ASAR) ADCs push the operation speed from several MHz to GHz due to the advanced process technology and circuit techniques [12], [13]. Moderate resolution (6–8-bits) ASAR ADCs have advantages of small analog complexity and the conversion rate can be improved to several hundred picoseconds by an advanced process. These power-efficient ASAR ADCs have been leveraged to the pipelined ADCs by replacing sub-ADCs and back-end stages successfully [14], [15].

Fig. 2 shows a plot of Walden figure of merit (FOM) versus nyquist bandwidth of the state-of-the-art CTSDMs and pipelined ADCs for the power efficiency less than 1 pJ/conv.-step [16]. Pipelined ADCs based on the SAR architecture have achieved the signal bandwidths of up to 50 MHz with 55–65 dB DR with excellent power efficiency. As it can be seen, the SAR-assisted pipelined ADCs have pushed the energy efficiency down to below 100 fJ/conv.-step compared with the conventional architecture. However, only few CTSDMs have adopted this technique in the past ten years. A 5-bit ASAR-based quantizer [17] has been utilized to achieve 100 fJ/conv.-step with DTSDM for audio application in a 65-nm CMOS process. Only a few CTSDMs adopt an SAR-assisted technique to achieve low-power and high-performance modulator in wireless application. The SAR-assisted technique in CTSDM [18] performs only 788 fJ/conv.-step because of the synchronous operation of quantizer and high sampling frequency with first-order modulator loop. High sampling frequency does not lead to low-power operation in CTSDM. This work utilizes an ASAR-assisted quantizer with digital $\Delta\Sigma$ truncation technique in a power-efficient way to reduce the sampling frequency and still achieve high DR modulator.

In this paper, an ASAR-based quantizer is proposed in 65-MHz CTSDM to achieve 64 fJ/conv.-step in 1.92-MHz bandwidth. [19] Section II introduces the behavior-level evaluations and circuit architecture considerations to achieve a power-efficient modulator. Section III discusses the implementation details, and Section IV describes the modulator's measurement setup and measurement results. Finally, Section V concludes the presented work.

II. Behavior and Circuit Architecture Evaluations

A. Behavior-Level Design Considerations

From system-level evaluation, the DR requirements for WCDMA (1.92 MHz) should be higher than 80 dB to meet the adjacent channel selecting requirement. In order to save chip area, we do not scale the *RC* value in GSM/EDGE mode because the resistor/capacitor areas are determined by the application bandwidth (BW) and sampling frequency. Instead, the DR requirement in GSM/EDGE mode is determined by integrating the narrow noise BW (100 kHz). The DR for GSM/EDGE mode becomes higher than $80 + 10 * \log(1.92/0.1) = 92.8$ dB. To achieve a DR higher than 80 dB in 1.92-MHz BW, 90-dB SQNR is used for behavior simulation. Fig. 3 illustrates the relation among loop filter, sampling frequency, and quantizer resolution in CTSDM with 6-dB maximum noise-transfer function (NTF) out-of-band gain. Although the in-band quantization noise can be suppressed by using aggressive NTF gain, 6 dB is chosen for at least 2-bit quantization, different order and different sampling frequency comparisons without causing overload at -2 dBFS input power. A low-order modulator loop means that a high sampling frequency or high-resolution quantizer is essential to achieve the high DR requirement.

B. Circuit-Level Design Considerations

For high sampling frequency, high-frequency coupling from a downlink ADC can be categorized into the conductive, the capacitive, and the magnetic couplings [20]. These factors may cause desensitization of front-end circuit. In general, conductive and capacitive couplings can be prevented by inserting the low-pass filter and ground shielding, and the magnetic coupling can be eliminated by careful top arrangement. The harmonic energy of the unwanted coupling signal source from ADC to the receiver front-end is proportional to the sampling clock frequency. The attentuation capability by a passive low-pass filter must be

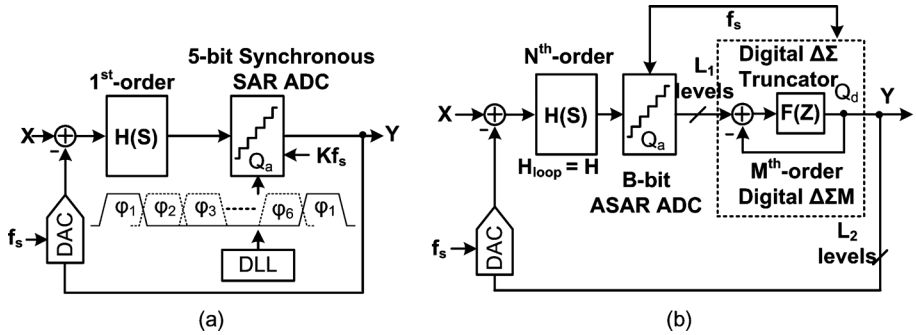

Fig. 4. (a) Synchronous SAR-based CTSDM architecture. (b) Proposed ASAR-based CTSDM architecture with digital ΔΣ truncator.

increased according to the stringent desensitization specification for high-performance SoC. For the CTSDM, a high sampling frequency means that a high operational-amplifier (op-amp) BW is inevitable to reduce the phase shift by loop filter. For the current DAC linearity perspective, the dynamic element matching (DEM)-based current DAC suffers from the second-harmonic [8] distortion especially for high sampling frequency, which will be discussed later.

For the same SQNR, the sampling frequency of CTSDM can be reduced by using a multibit quantizer or a high-order loop filter. A high-order loop filter requires more coefficients to stabilize the modulator, thus increasing the design complexity. SAR-based quantizer can be utilized to replace the power-hungry flash ADC, especially for the resolution larger than 5 bit. In this work, the ASAR-based quantizer is adopted, and the latency of this architecture can be easily implemented in a 40-nm CMOS process.

C. SAR-Based Quantizer

The SAR-based quantizer in CTSDM was first published in [18]. As shown in Fig. 4(a), a first-order 5-bit synchronous SAR quantizer is employed to realize a 62-dB DR in 1.92-MHz BW. However, due to synchronous control manner, a delay-locked loop (DLL) for multiphase timing of the quantizer is required, which is not favorable in a low-cost and low-power SoC application. Furthermore, the first-order loop filter cannot provide the sufficient loop gain to suppress the quantization noise and nonlinearity of the quantizer especially for high DR application. To avoid using a high-frequency DLL, an ASAR-based quantizer is employed in this work. It is obvious that the design effort of feedback loop grows proportionally with the quantizer bit number. The routing complexity, DAC area, and matching requirement cause design challenges if we use a 6-bit ASAR quantizer. As shown in Fig. 4(b), the ASAR-based quantizer incorporated with a digital ΔΣ truncator is proposed to mitigate the problems mentioned before. The quantization error is denoted by Q_a and truncation error is Q_d. By reducing the quantizer output level L_1 to a smaller level L_2 with extra ΔΣ shaping technique, a power-efficient and high-performance downlink ADC can be realized by leveraging ASAR ADC. The transfer function according to the linear model with the loop gain H is derived as follows:

$$Y = X + \frac{1}{H}Q_a + \frac{1}{H}(1 - Z^{-1})^M Q_d \tag{1}$$

where M represents the order of digital the ΔΣ truncator. The truncation error Q_d is shaped not only by the digital ΔΣ loop but also by the original loop gain H if we take the output after truncation as the final output. The error feedback digital ΔΣ truncator is utilized to reduce the delay between the quantizer output and DAC input.

D. Proposed Modulator

For the top-level clock planning, the available clock is 2080 MHz/N, where N is the integer number of power of 2. From behavior simulation, 32.5-MHz 6-bit $(N = 64)$ need higher order (> 6) to meet 90-dB SQNR in 1.92-MHz BW. In addition, high sampling frequency requires a high BW op-amp to reduce the loop filter delay for stability issue. Therefore, 65-MHz $(N = 32)$ third-order 6-bit is chosen to save quantizer and op-amp powers. Fig. 5 shows the block diagram of the proposed third-order single-loop with 6-bit ASAR-based quantizer and digital ΔΣ truncator. To reduce its power consumption, the loop filter employs a feed-forward topology instead of feedback one because more DACs are required in feedback topology. Directly feed-forward from input X to quantizer input is not adopted in this work because there is no anti-aliasing in the loop filter and the kick-back noise from the quantizer may interfere with the previous stage. The feed-forward coefficient a_{f1} and a_{f2} realize the second- and first-order loop filter parameters, respectively, and coefficient $a_{\rm res}$ forms the resonator for optimized SQNR. The notch frequency can be individually determined by the equation shown below once K_2 and K_3 are found in coefficient synthesis as follows:

$$f_{\rm notch} = \frac{\sqrt{K_2 K_3 a_{\rm res}}}{Ts}. \tag{2}$$

The excess loop delay (ELD) compensation is realized by K_{f2} with three-quarter cycle delay to quantizer input.

E. Error Feedback Digital ΔΣ Truncator

A first-order error feedback ΔΣ truncator shown in Fig. 6 is used to implement the F(Z) in Fig. 5. By feeding the LSB with one cycle delay to the quantizer output Y_1, the truncation error Q_d can be first-order shaped. The transfer function can be written as

$$Y = Y_1 + (1 - Z^{-1})Q_d. \tag{3}$$

In Fig. 7, the numerical SQNR and DR evaluation is analyzed by using the same quantizer levels L_1 equal to 64 but different

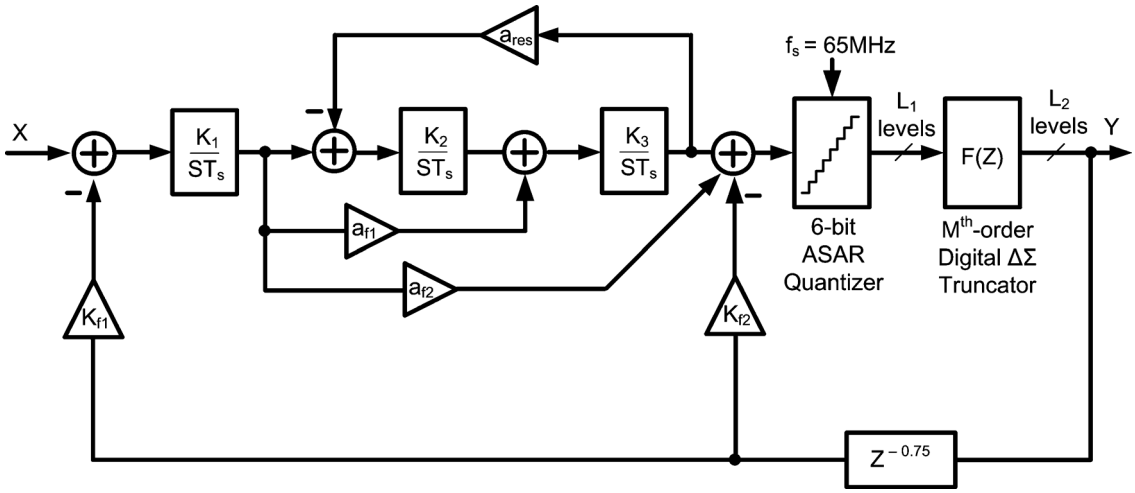

Fig. 5. Proposed single-loop feedforward CTSDM.

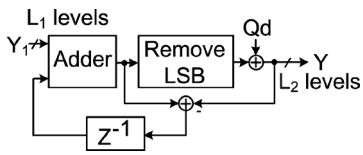

Fig. 6. Schematic of the first-order error feedback digital $\Delta\Sigma$ truncator.

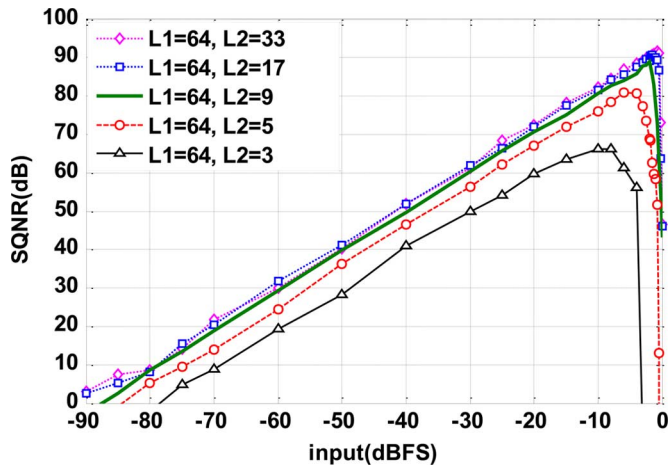

Fig. 7. Numerical simulation results with the same L_1 but different L_2.

levels after truncation, denoted by L_2, from 33 to three levels. The truncation error begins to dominate the modulator performance as the output is truncated to less than five levels. Since the extra truncation noise is shaped to the high-frequency band, the large input signal power (input power > -10 dBFS) with large truncation noise exceeds the reference level at the quantizer input easily and cause overload of the modulator. Therefore, the performance drops obviously for large input signal with L_2 is less than five levels. In this work, the output levels L_2 after truncation is selected to be nine for area and performance considerations. The compared spectra among the third-order, $L_1 = 64$, with and without truncating to nine levels, and the fourth-order nine levels without truncation is shown in Fig. 8. For the proposed third-order loop filter, $L_1 = 64$ with $\Delta\Sigma$ truncation to $L_2 = 9$, and it shows only 2-dB SQNR degradation compared with the same order loop filter without $\Delta\Sigma$ truncation. The relatively high in-band noise of fourth-order nine levels is due to larger quantization noise. The extra out-of-band noise between the third- and fourth-order filters without truncation is due to the additionally shaped truncation noise. With $\Delta\Sigma$ truncation, the equivalent out-of-band gain gets higher so some margins must be reserved for original maximum NTF out-of-band gain for stability consideration. This extra noise can be easily addressed by the back-end decimation filter.

III. Circuit-Level Implementation

A. CTSDM Schematic

Fig. 9 shows the schematic of the modulator. All of the integrators are implemented as active-*RC* integrators since these show better linearity performance than Gm-C ones. To compensate the *RC* variation, all capacitors have 4-bit networks to cover the process variation with $\pm 30\%$ covering range. The *RC* calibration mechanism is shared with top calibration circuit to reduce the complexity in SoC. The value of input resistor R_1 is determined by the noise requirement and capacitor C_1 is determined by the coefficient scaling in contrast to the feed-forward architecture with transconductance amplifiers [21], which is realized by the capacitive summation at the virtual ground node of the last integrator and no power is consumed. Additionally, the feed-forward coefficient is inherently linear regardless of signal swing. The first-order loop filter coefficient a_{f2} in Fig. 5 is realized by the capacitive ratio of C_{f2}/C_3 to save an additional summing amplifier.

Because the most critical first-order loop parameter is determined by the first integrator and the ratio of C_{f2}/C_3, the gain-bandwidth (GBW) requirement for the first op-amp is the most stringent. The susceptibility of the delay to CTSDM due to finite GBW in the first integrator can be eliminated by the excess loop delay compensation path from the final output to the quantizer input. The GBW of the first integrator is mainly determined by the noise performance although 1.5 fs is already sufficient for stability issue in behavior simulation. The GBW

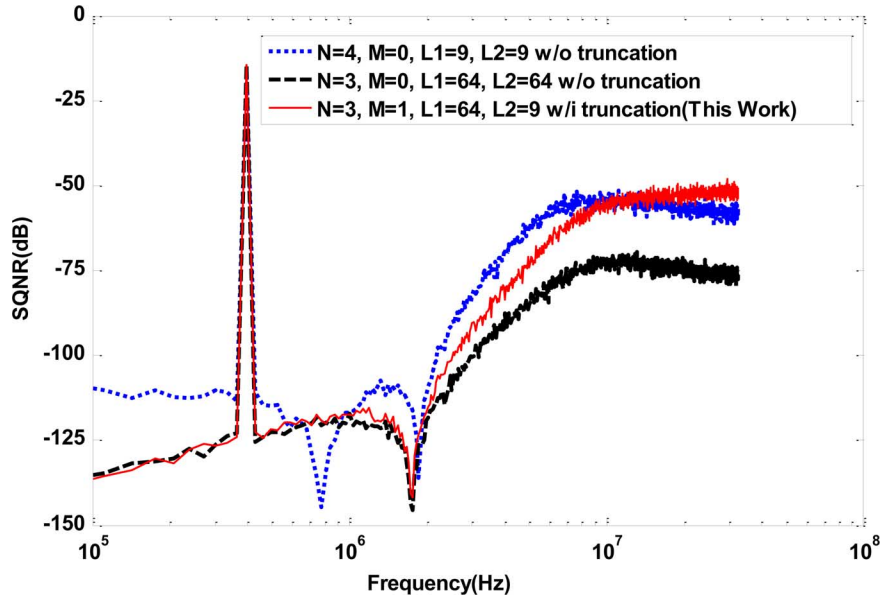

Fig. 8. Compared spectrum of the proposed architecture.

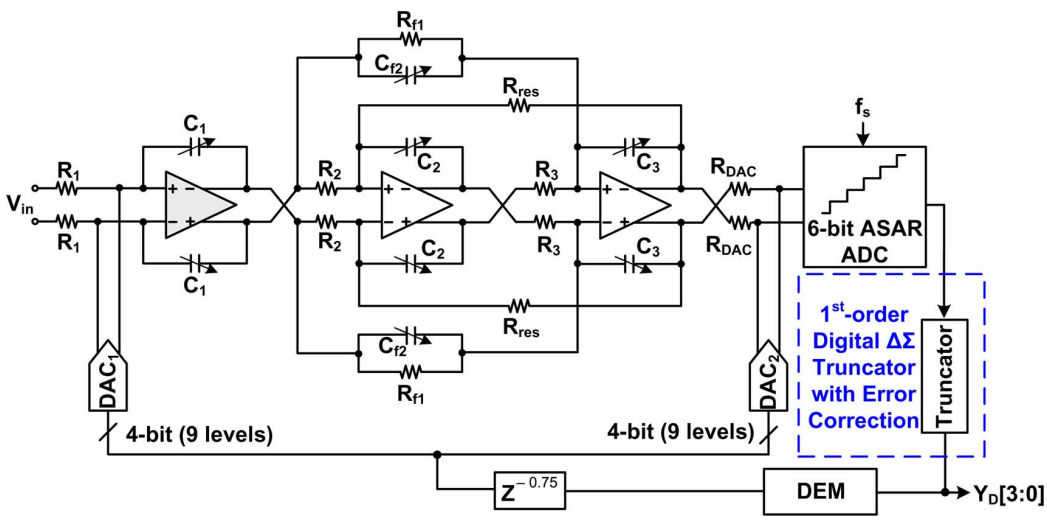

Fig. 9. Implementation for third-order CTSDM with first-order digital ΔΣ truncator.

requirements for integrators 2 and 3 are not critical, and the currents are scaled down to save power consumption. Extra effort for the last integrator is the driving capability of quantizer input sampling network. The GBW for the first, second, and third integrators are roughly 2.5, 1, and 1.5 fs, respectively.

Clocking at 65 MHz, the digital error correction logics are merged to digital ΔΣ truncator to reduce the ELD. The ELD compensation is realized by introducing a three-quarter cycle delay to the quantizer input with the passive summation through R_{DAC} [22]. Although an extra pole is formed by R_{DAC} and equivalent capacitance at quantizer input, which causes an extra delay of the loop filter, this problem can be ignored thanks to the low sampling frequency. A low-latency DEM [23] is utilized to reduce the delay between the truncator output and the DAC input. Both DAC1 and DAC2 are current-steering NRZ DACs with nine levels.

B. Amplifier Design

The op-amp used in the first integrator is shown in Fig. 10. A Miller-compensated, two-stage op-amp with output rail-to-rail driving capability is adopted. In general, a switched-capacitor-based level shifter in the output stage is adopted for better driving capability. However, this technique is not feasible in CTSDM due to the switch-less characteristic. By feed-forwarding the first stage output in the high-pass manner to the second-stage PMOS M_5 and M_6, the slew rate can be enhanced by the push–pull behavior of the output stage. The corner of this high-pass path BW is around 10 MHz because only high-frequency performance is concerned. Furthermore, the output parasitic pole under output loading C_{load} can be pushed to higher frequency as

$$\frac{(g_{m5}+g_{m7})}{C_{\mathrm{load}}}. \tag{4}$$

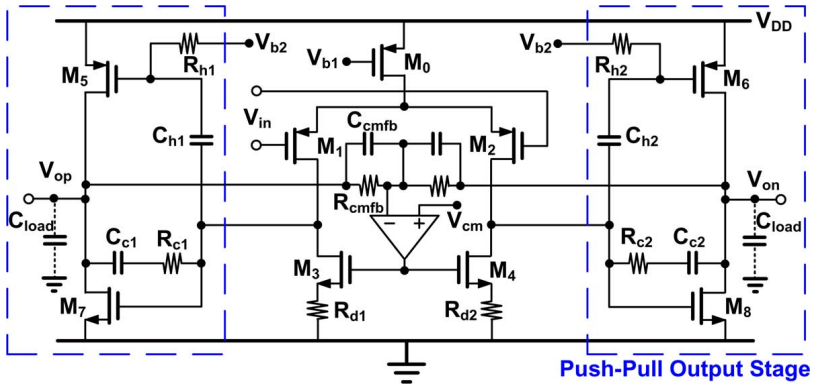

Fig. 10. Schematic of the op-amp with ac-coupled push–pull driving stage.

A small current can be used to achieve the same integrator loop stability and save the power dissipation. The source degeneration resistors R_{d1} and R_{d2} are used to improve the noise of M_3 and M_4 since the thermal noise referred to input is eliminated by the degeneration resistor:

$$V_{\text{nteq}}^2 = \frac{16\text{KT}}{3g_{m1}}\left(1 + \frac{1}{g_{m1}g_{m3}R_{d1}^2}\right). \tag{5}$$

The output swing of the first integrator is 500 $\text{mV}_{\text{pp,diff}}$ and has a small impact on the modulator linearity thanks to the feed-forward architecture of the loop filter and push–pull driving stage. The common-mode feedback is realized by resistively sensing the output nodes and controlling the gate voltage of M_3 and M_4 through an error amplifier, which is a replica of the first stage but with diode-connected load and degeneration resistors. The capacitor C_{cmfb} is utilized to introduce a zero to stabilize the loop.

C. Outer Feedback DAC

The outer feedback DAC mainly dominates the modulator linearity performance. NRZ DAC is employed for better jitter immunity. Fig. 11(a) shows the simplified DAC schematic with switch mismatch ΔV. The switch control signal is low crossing for small glitch consideration. The second harmonic distortion due to DEM operation and the mismatch is firstly disclosed in [8]. The switch mismatch, ΔV, translated into error charge through the common-source parasitic capacitor C_q. As shown in Fig. 11(b), we apply a one-cycle DAC signal from code 0 to 8 and back to 0 and a conventional DEM is applied. When the switches are toggled from 0 to 1 or 1 to 0, the error charges interact with integrator capacitor in a signal-dependent manner, around twice the DAC signal frequency, and second-harmonic distortion appears at modulator output. The error current due to error charge is in proportion to the sampling frequency as shown below:

$$I_{\text{error}} \propto \Delta V * C_q * f_s. \tag{6}$$

Therefore, this error can be suppressed by low-sampling-frequency operation. In additiom, the common source capacitor Cq is reduced to 5 fF by careful layout and the matching of switches are particularly concerned.

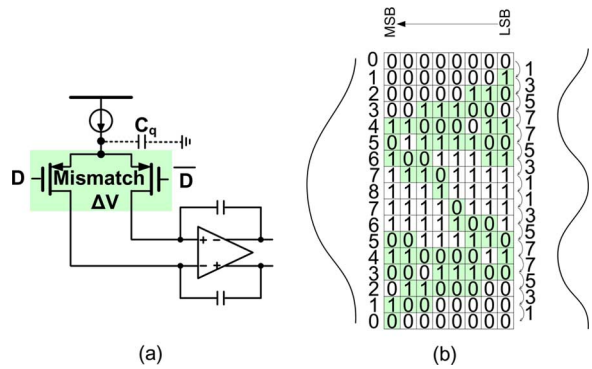

Fig. 11. (a) Simplified schematic of the outer most feedback DAC with switch mismatch. (b) Second-order distortion mechanism example due to DAC error charge and DEM.

D. 6-Bit ASAR-Based Quantizer

Fig. 12 shows the simplified ASAR-based quantizer and the timing diagrams. A 6-bit ASAR ADC with 2-bit digital error correction (DEC) [24] is employed to accommodate setting error in switched-capacitor DAC. With the input bootstrapped switch, which operates at $\text{Vdd} + \text{Vin}$, the signal-dependent clock feed-through can be alleviated. The unit capacitor for C_1-C_{6c} is 2.5 fF with a sandwich structure of two metal layers. The self-timing mechanism is adopted for high speed consideration and the outputs B_1-B_{6C} are latched with a half-cycle delay after the sampling instance of Clk_s. In other words, conversion time of ASAR operation must be finished within 7.7 ns. The data at DAC input is relatched by Clk_dac with a quarter-cycle delay after the rising edge of Clk_latch. The feedback DACs sample the truncated data (D_{tr}) with three-quarter cycle delay after the sampling instance of Clk_s.

The comparator and the asynchronous timing generator are shown in Fig. 13. As shown in Fig. 13(a), a two-stage dynamic comparator [25] is used to save power dissipation because there is no static biasing and the power scales proportional to the sampling frequency. When Clkc is high, A_p and A_n are pulled to ground and then reset outp and outn to ground. When Clkc changes to low, the input difference is amplified and the latch regeneration forces one output to high and the other to low according to the compared result. Once the comparator takes a decision, the valid signal by the logical NAND operation of Ovp

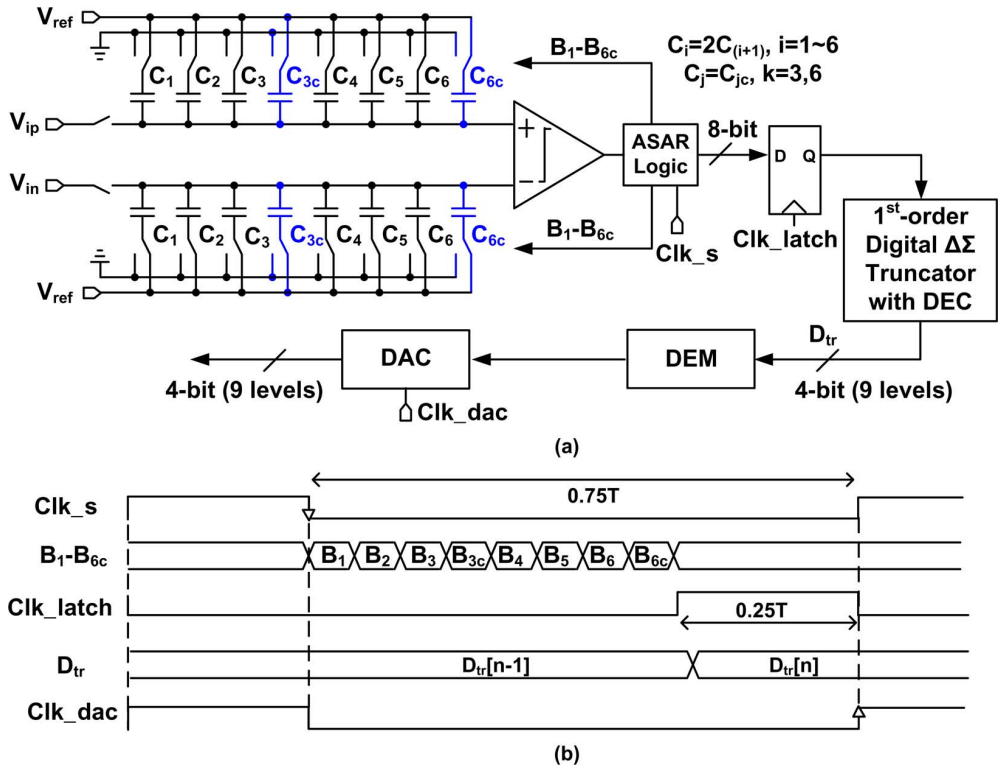

Fig. 12. (a) Block diagram of 6-bit ASAR-based quantizer. (b) Timing diagram.

and Ovn is pulled to high to enable the asynchronous control circuit in Fig. 13(b). The sampling phase of Clk_s is 25% of clock frequency and Clkc is the control signal of the comparator. Clk1 to Clk6c are the control signals of capacitor arrays with monotonic switching mechanism within a half clock cycle. A quarter cycle is left for the delay of the digital ΔΣ truncator and DEM logic. The current consumption of the 6-bit ASAR quantizer including reference generator and buffer is around 300 μA.

IV. Experimental Results

A. Chip Realization

The chip photograph in 40-nm CMOS is shown in Fig. 14. The modulator per channel including reference generator and bias occupies 0.051 mm^2. To reduce feedback path delay induced by interconnected parasitic resistances and capacitances, the high-speed blocks are placed close to each other. The high-speed ASAR-based quantizer occupies only 45 μm × 55 μm, which is competitive to the conventional flash ADC. The logic circuit near the 6-bit ASAR quantizer includes a digital ΔΣ truncator and DEM circuits. The routing from the DEM output to the DAC_1 input is buffered for the driving consideration. Decoupling capacitor is used to filter out the noise in the bias generator for all analog blocks. The modulator dissipated 1.91 mW from a 1.2-V supply. Fig. 15 shows the power breakdown of the presented work. The power consumption in the op-amp3 is larger than that in op-amp2 due to the driving requirement of the ASAR input capacitor array.

B. Measurement Setup

The block diagram of experiment setup is shown in Fig. 16. A signal source by Agilent 8644B drives a bandpass filter, which attenuates its harmonics and noise. The phase-noise performance of this instrument is sufficient without incurring an ambiguous problem of counting the input signal power. The single-ended signal is transformed into differential signals $\mathrm{V_{ip}}$ and $\mathrm{V_{in}}$ by a balun and applied to the modulator. The clock source is generated by Agilent E4432B and converted to differential signals $\mathrm{Clk_p}$ and $\mathrm{Clk_n}$. This differential signals are converted to the required clock source by the on-chip differential-to-single ended buffer. An LVDS receiver is employed for the high-speed data transmissions of 4-bit data and one clock and eliminating noise coupling. The data is captured by Agilent 16802 logic analyzer and data is downloaded to the PC for postprocessing in MATLAB. The captured data are windowed by a Blackman–Harris window and a 1M Fourier transform is applied.

C. Measurement Results

To measure the modulator's linearity, sinusoidal input signals with a maximum input voltage of 2.4-Vpp differential were applied to the modulator. Fig. 17(a) shows a single-tone spectrum with −2 dBFS power at 625 kHz and the second-harmonic distortion is −95.2 dBFS thanks to low sampling frequency and careful layout. The measured signal-to-noise-and-distortion ratio (SNDR) is 79.6 dB. As shown in Fig. 17(b), 500-kHz and 625-kHz in-band two tones with −8 dBFS power are applied to the modulator input, and the second and third intermodulations are 90 and 99 dBc, respectively. Two adjacent channels at 2.8 and 5 MHz with around −8 dBFS power are applied

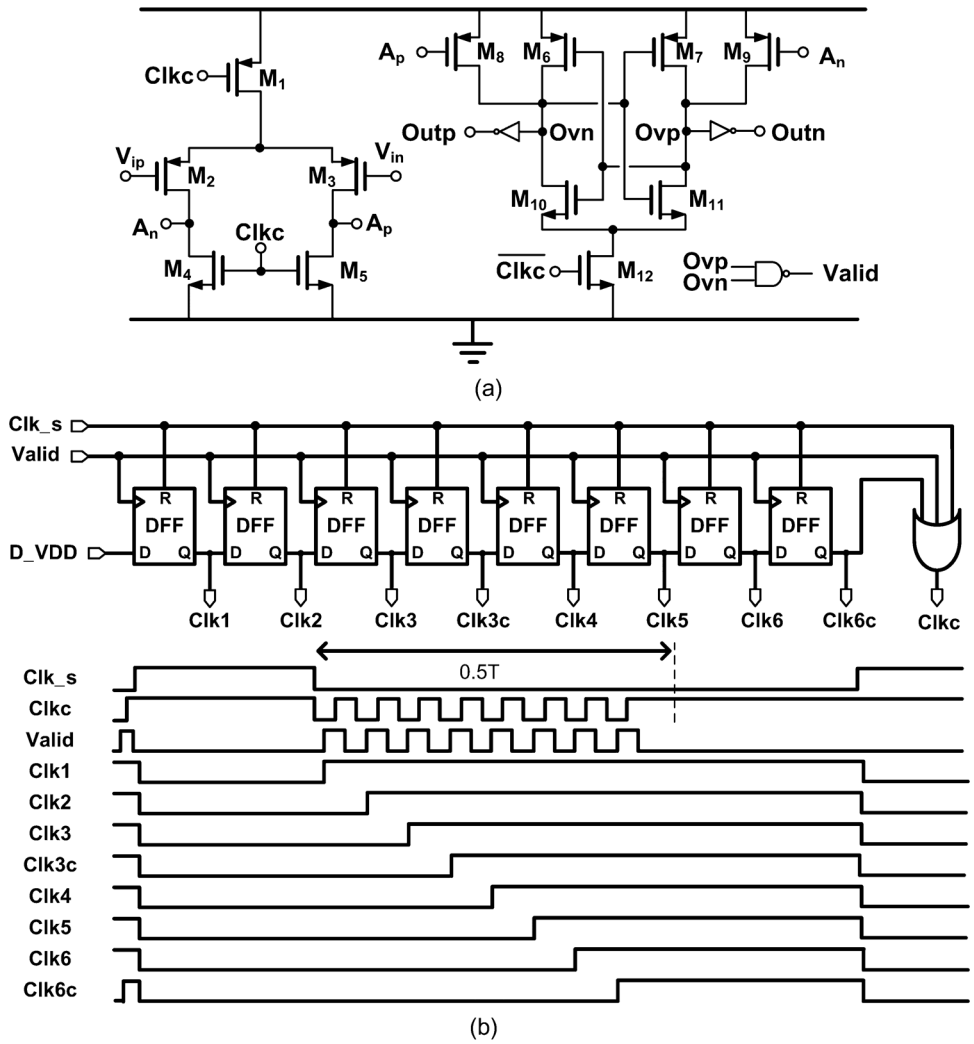

Fig. 13. (a) Schematic of the comparator in quantizer. (b) Asynchronous control logic and timing.

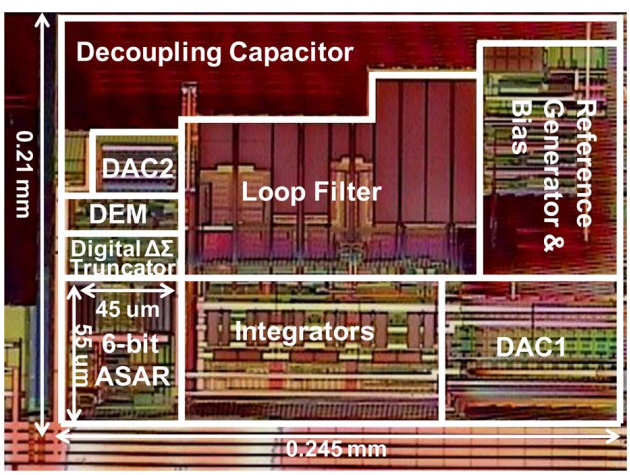

Fig. 14. Die photograph of the CTSDM.

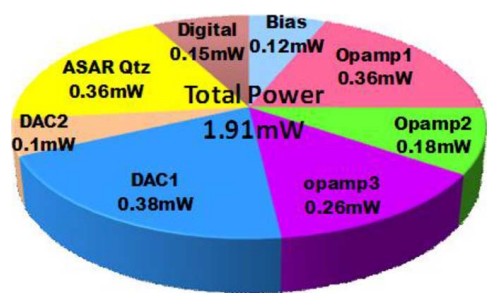

Fig. 15. Pie-chart distribution of the power consumption.

to the modulator to test the out-of-band linearity, as shown in Fig. 18(a). The second inter-modulation tone at 2.2 MHz is −96.3 dBFS and the third inter-modulation tone at 600 kHz is −103 dBFS. In Fig. 18(b), we also apply two blockers at 10 and 21 MHz with −10 dBFS power. Smaller input power levels are used at blocker test because there is a STF peaking at high frequency due to the feed-forward architecture. The measured third inter-modulation tone at 1 MHz is −94.6 dBFS.

Fig. 19 shows the measured SNR and SNDR versus the normalized input levels as a function of input amplitude for WCDMA and GSM/EDGE modes. The modulator achieve 83.4 dB DR in 1.92-MHz BW, and the peak SNR/SNDR is 80/79.6 dB, respectively. In GSM/EDGE mode, we apply a

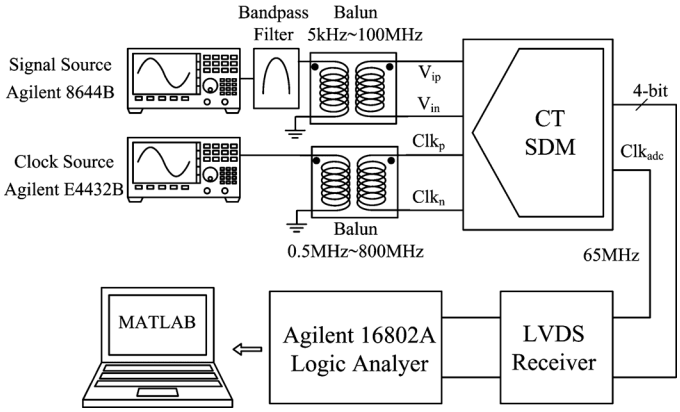

Fig. 16. Measured setup of the CTSDM.

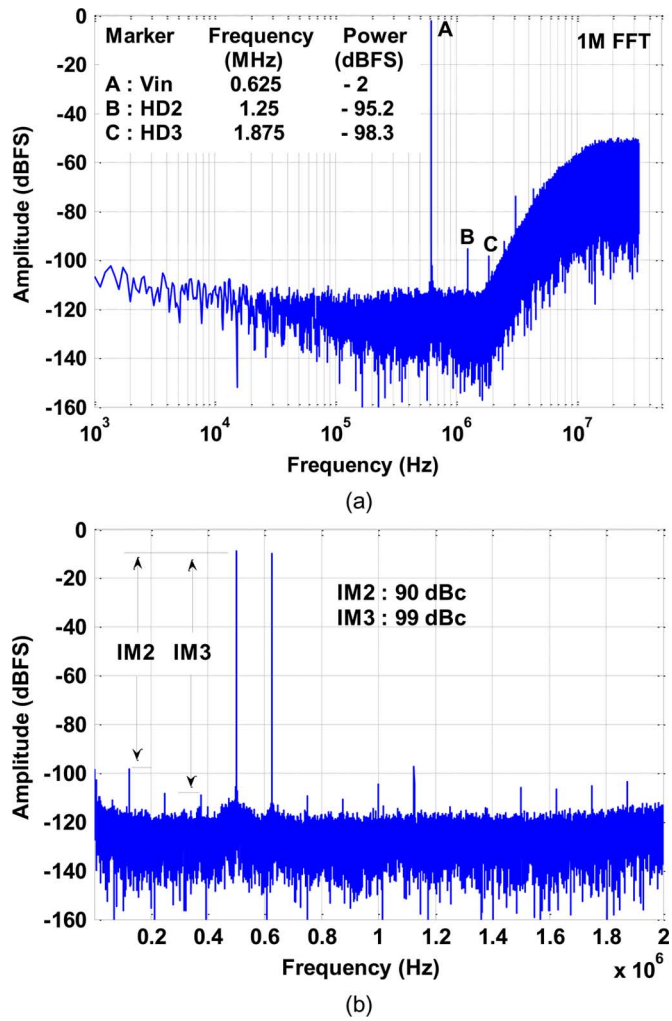

Fig. 17. Measured (a) single-tone spectrum with −2 dBFS at 625 kHz and (b) in-band two-tones at 500 and 625 kHz.

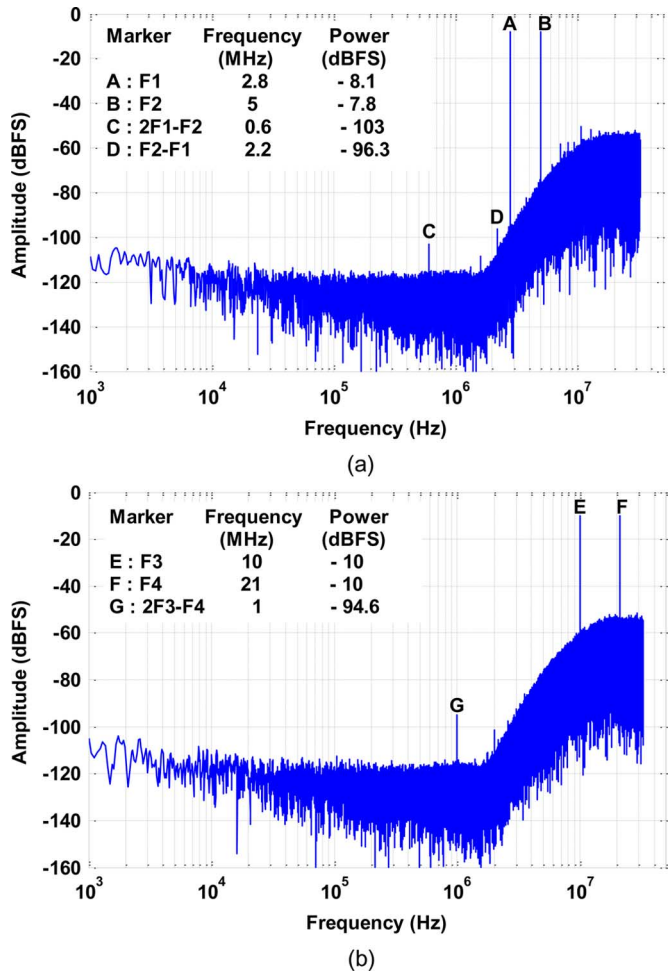

Fig. 18. Measured (a) out-of-band linearity with two adjacent channels and (b) two blockers.

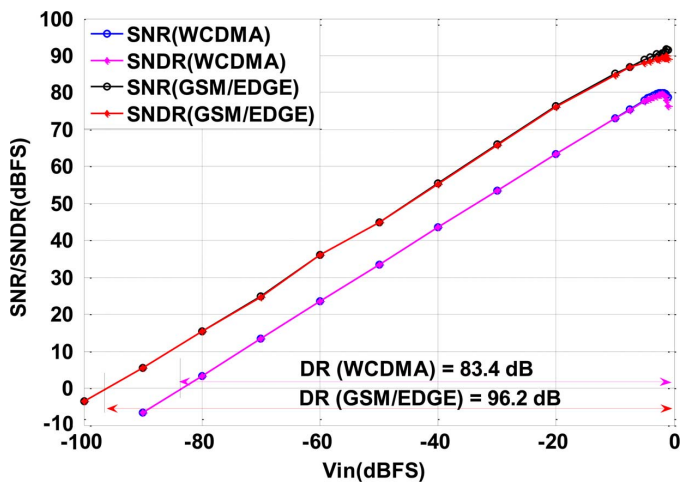

Fig. 19. SNR/SNDR versus input signal level.

100-kHz sinusoidal signal by an Audio Precision and the DR is 96.2 dB with 91.8/90 dB peak SNR/SNDR.

Fig. 20 shows four system-level scenarios for desensitization test of the downlink ADC. Narrowband blocker (NBB), adjacent channel selectivity (ACS), and in-band blocker (IBB) under different powers and receiver front-end gain settings in WCDMA mode are tested individually. As shown in the input signal profiles for each case, the wanted signal is determined by the set point of receiver planning and the adjacent channel/blocker powers of each case are the target values from system evaluation. The wanted signal is set at 625 kHz, and all results

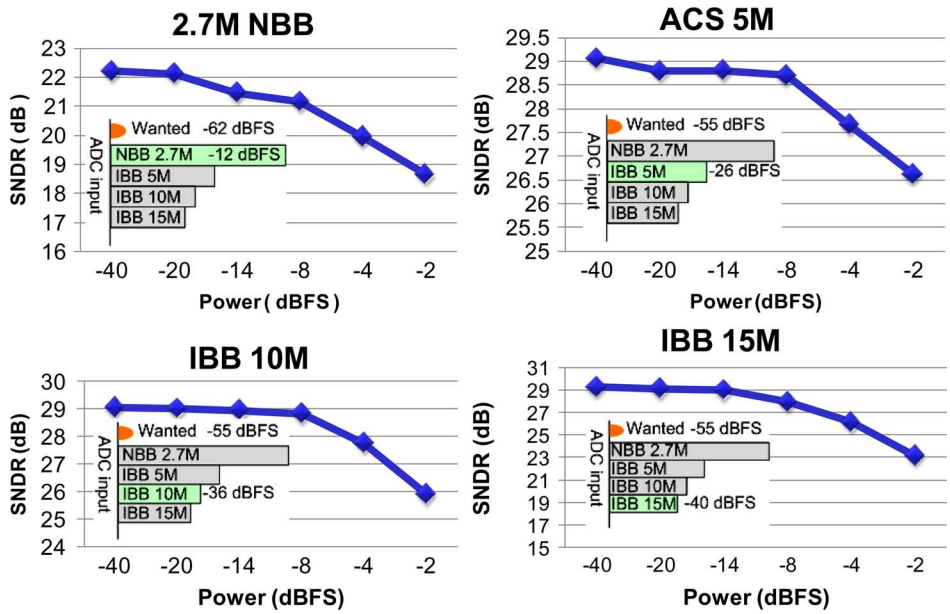

Fig. 20. Desensitization measurements for WCDMA mode.

TABLE I
PERFORMANCE SUMMARY

Ref.	Tech. CMOS	Fs (MHz)	BW (MHz)	DR (dB)	SNR_{max} (dB)	$SNDR_{max}$ (dB)	Power (mW)	V_{DD} (V)	Area (mm^2)	FOM1 (fJ/conv.)	FOM2 (dB)
[3]	130nm	61.44	1.92	77.1	75.7	75.2	5.2	1.2	0.27	280	162.8
[4]	130nm	104	2	-	72	71	3	1.5	0.3	258	-
[5]	65nm	153.6	1.92	73	-	-	3.7	2.5	0.125	260	160.2
[6]	40nm	245	1.92	83	-	78	2.8	1.4	0.085	110	171.4
[10]	180nm	60	1.9	82	81	81	8.1	1.5	1.27	250	165.7
[18]	130nm	184.3	1.92	62	65	59	3.1	1.2	0.36	788	150
[23]	65nm	128	2	80	79.1	79.07	4.52	1.2	0.084	153	166.5
This Work	40nm	65	1.92	83.4	80	79.6	1.91	1.2	0.051	64	173.4

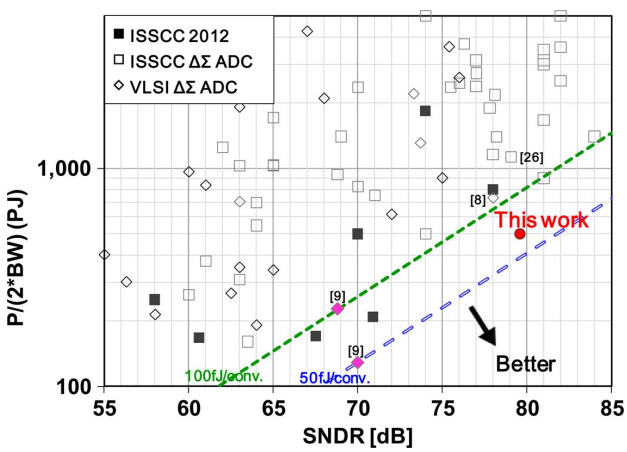

Fig. 21. Compared energy efficiency with the state of the art.

show that less than 1-dB SNDR degradations are achieved from small power to the target one.

D. Comparison With the State of the Art and the Performance Summary

We present a comparison chart between the proposed CTSDM and other state-of-the-art CTSDMs from the literature even though these designs were done in quite different ways in different technologies. Fig. 21 shows the power efficiency in terms of power dissipation per Hertz of Nyquist frequency versus SNDR. Since higher SNDR requires larger power, constant Walden FOM lines with 50 and 100 fJ/conv.-step are proportional to SNDR. As the plot indicates, this work shows better energy efficiency with nearly 80 dB SNDR in 1.92-MHz BW. Table I compares the performance of several CTSDMs with several megahertz BW presented in the literature with this work in detail. The FOM1 [26] in the table is determined by

$$\text{FOM1} = \frac{\text{Power}}{2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02}} \tag{7}$$

Because the noise performance is dominated by thermal noise, it is also relevant to use FOM2 proposed by Schreier [27] by

$$\text{FOM2} = \text{DR} + 10\log_{10}\left(\frac{\text{BW}}{\text{Power}}\right). \tag{8}$$

The proposed ASAR-based CTSDM with digital $\Delta\Sigma$ truncator achieve FOM1 of 64 fJ/conv.-step and FOM2 of 173.4 dB in 1.92-MHz BW.

V. CONCLUSION

This paper presents a CTSDM with 6-bit ASAR quantizer and first-order digital $\Delta\Sigma$ truncator to achieve a power-efficient downlink ADC. By using this technique, low sampling

frequency is available to reduce both the system-level design efforts and the modulator itself. The ac-coupled push–pull driving stage in the first integrator reduces the power dissipation further. The FOM of this CTSDM clocking at 65 MHz achieves 64 fJ/conv.-step, which is quite power-efficient for the application BW of several megahertz. The 6-bit ASAR quantizer occupies only 0.002475 mm^2 in 40-nm CMOS, and the modulator per channel occupies 0.051 mm^2, which is competitive in cellular receiver.

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REFERENCES

[1] P. Crombez, G. V. der Plas, M. S. J. Steyaert, and J. Craninckx, "A single-bit 500 kHz–10 MHz multimode power-performance scalable 83-to-67 dB DR CT $\Delta\Sigma$ for SDR in 90 nm digital CMOS," *IEEE J. Solid State Circuits*, vol. 45, no. 6, pp. 1159–1171, Jun. 2010.

[2] Y. Ke, P. Gao, J. Craninckx, G. V. der Plas, and G. Gielen, "A 2.8-to-8.5 mW GSM/bluetooth/UMTS/DVB-H/WLAN fully reconfigurable CT $\Delta\Sigma$ with 200 kHz to 20 MHz BW for 4 G radios in 90 nm digital CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2010, pp. 153–154.

[3] T. Christen and Q. Huang, "A 0.13 μm CMOS 0.1–20 MHz bandwidth 86–70 dB DR multi-mode DT $\Delta\Sigma$ ADC for IMT-advanced," in *Proc. IEEE ESSCIRC*, Sep. 2010, pp. 414–415.

[4] L. Dorrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, "A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS," *IEEE J. Solid State Circuits*, vol. 40, no. 12, pp. 2416–2427, Dec. 2005.

[5] B. Putter, "A 5th-order CT/DT multi-mode $\Delta\Sigma$ modulator," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 244–245.

[6] J. Gealow, M. Ashburn, C.-H. Lou, S. Ho, P. Riehl, A. Shabra, J. Silva, and Q. Yu, "A 2.8 mW $\Delta\Sigma$ ADC with 83 dB DR and 1.92 MHz BW using FIR outer feedback and TIA-based integrator," in *Proc. IEEE Symp. VLSI Circuits*, June 2011, pp. 42–43.

[7] K. Matsukawa, K. Obata, Y. Mitani, and S. Dosho, "A 10 MHz BW 50 fJ/conv. continuous time $\Delta\Sigma$ modulator with high-order single Opamp integrator using optimization-based design method," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 160–161.

[8] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, Y. Tokunaga, S. Sakiyama, and S. Dosho, "A 69.8 dB SNDR 3rd-order continuous time delta-sigma modulator with a ultimate low power tuning system for a worldwide digital TV-receiver," in *Proc. IEEE CICC*, Sep. 2010.

[9] K. A. O'Donoghue, P. J. Hurst, and S. H. Lewis, "A digitally corrected 5-mW 2-MS/s SC $\Delta\Sigma$ ADC in 0.25-μm CMOS with 94-dB SFDR," *IEEE J. Solid State Circuits*, vol. 46, no. 11, pp. 2673–2684, Nov. 2011.

[10] K. Lee, M. R. Miller, and G. C. Temes, "An 8.1 mW, 82 dB delta-sigma ADC with 1.9 MHz BW and -98 dB THD," *IEEE J. Solid State Circuits*, vol. 44, no. 8, pp. 2202–2211, Aug. 2009.

[11] Y. Geerts, M. S. J. Steyaert, and W. Sansen, "A high-performance multibit $\Delta\Sigma$ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829–1840, Dec. 2000.

[12] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2669–2680, Dec. 2006.

[13] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[14] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[15] M. Furuta, M. Nozawa, and T. Itakura, "A 10-bit, 40-MS/s, 1.21 mW pipelined SAR ADC using single-ended 1.5-bit/cycle conversion technique," *IEEE J. Solid State Circuits*, vol. 46, no. 6, pp. 1360–1370, Jun. 2011.

[16] B. Murmann, "ADC Performance Survey 1997-2012," 2012.

[17] L. Liu, D. Li, Y. Ye, L. Chen, and Z. Wang, "A 95 dB SNDR audio $\Delta\Sigma$ modulator in 65 nm CMOS," in *Proc. IEEE CICC*, Sep. 2011.

[18] M. Ranjbar, A. Mehrabi, O. Oliaei, and F. Carrez, "A 3.1 mW continuous-time $\Delta\Sigma$ modulator with 5-bit successive approximation quantizer for WCDMA," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1479–1491, Aug. 2010.

[19] H.-C. Tsai, C.-L. Lo, C.-Y. Ho, and Y.-H. Lin, "A 1.2 V 64 fJ/conversion-step continuous-time $\Sigma\Delta$ modulator using asynchronous SAR quantizer and digital $\Delta\Sigma$ truncator," in *Proc. IEEE A-SSCC*, Nov. 2012, pp. 241–244.

[20] A. Poon, A. Chang, H. Samavati, and S. S. Wang, "Reduction of inductive crosstalk using quadrupole inductors," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1576–1564, Jun. 2009.

[21] R. H. M. van Veldhoven, "A triple-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, Aug. 2003.

[22] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[23] S.-J. Huang and Y.-Y. Lin, "A 1.2 V 2 MHz BW 0.084 mm2 CT $\Delta\Sigma$ ADC with -97.7 dBc THD and 80 dB DR using low-latency DEM," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 172–173.

[24] C.-C. Liu *et al.*, "A 10 b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386–387.

[25] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4 fJ/conversion-step 10 b 1 MS/s charge-redistribution ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 244–245.

[26] F. Gerfers, M. Ortmanns, and Y. Manoli, "A 1.5 V 12 bit power efficient continuous-time third-order $\Sigma\Delta$ modulator," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1343–1352, Aug. 2003.

[27] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: IEEE, 2005.

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