10.7 A 12b 1.25GS/s DAC in 90nm CMOS with >70dB SFDR up to 500MHz

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The current-steering DACs are commonly used in generating high-frequency signals [1-4]. A current-steering DAC comprises current cells of various sizes. Each of them contains a current source and a current switch. The DAC static linearity, specified as differential nonlinearity (DNL) and integral nonlinearity (INL), is mainly determined by the mutual matching and the output resistance of the current sources. The DAC also exhibits dynamic distortion. It is manifested as spurious-free dynamic range (SFDR) degradation. The SFDR decreases rapidly with increasing input frequency. There are two major sources of dynamic distortion, code-dependent switching transients (CDST) and code-dependent output-loading variation (CDLV). Switching transients are temporal disturbances in DAC output when the current switches in current cells make transitions. The output loading of a DAC varies when the output impedances of current cells change due to the transposition of their current switches. This DAC applies a digital random return-to-zero (DRRZ) technique to mitigate the CDST effect. Compact current cells are designed to minimize the CDLV effect. The current mismatches of the current cells are corrected by background calibration.

Figure 10.7.1 shows the DAC block diagram. All functional blocks, except the output resistive loads R_{L1} and R_{L2}, are integrated on the same chip. The main DAC is segmented into a 6-bit equally weighted MSB DAC (M-DAC) and a 6-bit binary-weighted LSB DAC (L-DAC). The differential output currents from the M-DAC and L-DAC are tied together and connected to R_{L1} and R_{L2} to generate differential output voltage $V_o=V_{o1}-V_{o2}$. The M-DAC comprises 63 identical current cells. Each current cell is designed to output a nominal current of 64I, where I is the DAC unit current. The L-DAC comprises 7 current cells which output a current of 1I, 1I, 2I, 4I, 8I, 16I, and 32I, respectively. There are two 1I current cells in the L-DAC so that a differential V_o of zero can be realized. In our design, I=4μA and $R_{L1}=R_{L2}=25\Omega$ yield a V_o signal range of $0.8V_{pp}$.

The DAC has a DRRZ setup. Figure 10.7.2 shows its operation. When CK is high, the DAC is in the $D_i[k]$ data phase. Its input encoder generates 63 $B_j[k]$ binary control signals to drive the M-DAC and 7 $L_j[k]$ binary control signals to drive the L-DAC. The DAC output V_o reflects the value of input $D_i[k]$. When CK is low, the DAC is in the Z[k] zero phase. The 64 $R_j[k]$ binary control signals drive the M-DAC and L-DAC respectively and make $V_o=0$. The entire L-DAC is treated as a single MSB current cell controlled by $R_0[k]$. The $R_j[k]$ control signals are generated from a pseudo-random number generator (PRNG). Their values change every clock cycle. The injection of $R_j[k]$ randomizes the switching transients so that they appear as noises in the V_o output but not as distortions. Thus, the CDST effect is mitigated. The PRNG is a 32-bit linear feedback shift register. Its 32 outputs and their complements form the 64 $R_j[k]$ signals.

Figure 10.7.3 shows the circuit schematic of the j-th current cell of the M-DAC. MOSFETs M11-M18 and the four inverters form a level-sensitive MUX-latch. When CK is high, the $B_j[k]$ signal is loaded into the latch. When CK is low, the $R_j[k]$ signal is loaded into the latch. The MUX-latch is operated under a 1.2V supply. MOSFETs M5-M6 function as a current switch together. MOSFET M1 and M3 form a cascoded current source with a fixed current of 48I. MOSFET M2 and M4 form another cascoded current source whose output current is mirrored from the $I_{c,j}$ current. Both current sources are operated under a 2.5V supply. M1-M6 are MOSFETs with thick gate oxide. Disregarding the matching requirement, smaller devices are chosen for the current switches and current sources to minimize the CDLV effect. A calibration setup adjusts $I_{c,j}$ to ensure current matching among the current cells.

The calibration runs in the background and calibrates each M-DAC current cell sequentially. The output current of the j-th M-DAC current cell is denoted as $I_{M,j}$ and the total output current of the L-DAC as I_L. The calibration adjusts $I_{M,j}$ to be equal to I_L. Assume the j-th M-DAC current cell is under calibration. Its current mismatch against the L-DAC is $\Delta I=I_L-I_{M,j}$. During the Z[k] zero phase, while the control signal for the L-DAC is $R_0[k]$, the control signal for the j-th current cell is set to the complement of $R_0[k]$. Thus, the mismatch term $R_0[k]$ 1 DI is embedded in V_o during the Z[k] zero phase. The calibration extracts ΔI from V_o and then accordingly adjusts $I_{c,j}$ in order to reduce ΔI to zero. As illustrated in Fig. 10.7.1 and Fig. 10.7.2, V_o is sampled during the zero phase, yielding $V_z=V_{z1}-V_{z2}$. When CK is high, $V_z=0$. The V_z is correlated with $R_0[k]$ by using a chopper. A low-pass filter (LPF) extracts the averaged value of V_p, yielding $V_m=\Delta I x R_L$. A continuous-time delta-sigma modulator (ΔΣM) is used to digitize V_m. The ΔΣM operates at 1/16 CK frequency. The decimation filter (DF) following the ΔΣM is an accumulator that dumps its content every 2^{18} D_s samples. The digital code D_m is then quantized into D_a which is an integer in {0, ±1, ±2, ±4}. The D_a is added to the content of the j-th accumulator (ACC). There are 63 ACCs. Their outputs, $D_{c,j}$, control 63 calibration DACs (C-DACs) respectively. Each C-DAC is a 7-bit current-steering DAC with a I/8 resolution. The output of the j-th C-DAC, $I_{c,j}$, adjusts the output of the j-th M-DAC current cell, $I_{M,j}$.

Figure 10.7.4 shows the schematic of the calibration analog signal path. MOSFETs M1-M4 form the V_o sampler. When CK is high, the V_{z1} and V_{z2} nodes are connected to a V_o common-mode voltage, V_{CM}. MOSFETs M5-M8 form the V_z chopper. The RC pairs, R_{F1}-C_{F1} and R_{F2}-C_{F2}, are the LPFs with a 26.5kHz bandwidth. The LPF output, V_m, is converted into current by a transconductor G_m and then integrated by the following 1st-order ΔΣM. The internal feedback in the DSM comprises a current source I_s and a current switch. Voltage V_m is reset by switch S1 before every calibration measurement. One calibration cycle, during which all 63 M-DAC current cells are updated once, requires 214ms.

The DAC is fabricated in a 90nm CMOS technology. Figure 10.7.7 shows the chip micrograph. Active area is 1100×750μm^2. It consumes 56mW from a 1.2V supply and 72mW from a 2.5V supply. Figure 10.7.5 shows the measured DNL and INL. The DNL is +4.5/–0.55LSB before calibration and improved to +0.45/0.5LSB after calibration. The INL is +10.1/–6.0LSB before calibration and improved to +1.0/–1.2LSB after calibration. Figure 10.7.6 shows the measured SFDR at various input frequencies. The sampling rate is 1.25GS/s. The SFDR is below 57dB before calibration. When both DRRZ and calibration are active, the SFDR is better than 70dB up to 500MHz input frequency and is better than 66dB up to 625MHz. Also shown in Fig. 10.7.6 is the theoretical CDLV limit based on the output impedances of the current cells. This limit does not confine the measured SFDR up to 625MHz signal frequency. After calibration, the SFDR is measured again but with DRRZ disabled. The DAC output is non-return-to-zero (NRZ). In Fig. 10.7.6, the SFDR degradation of the NRZ DAC reveals the effect of CDST and attests the function of DRRZ.

Acknowledgements:
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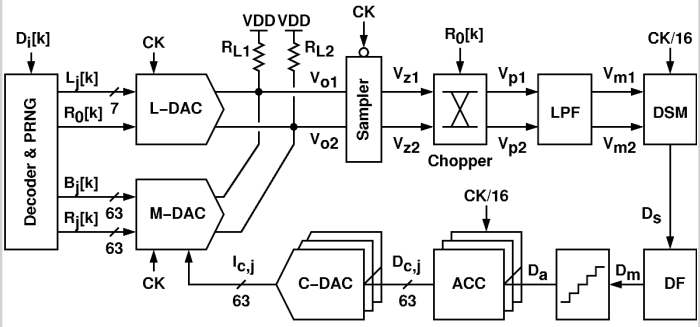

Figure 10.7.1: DAC block diagram.

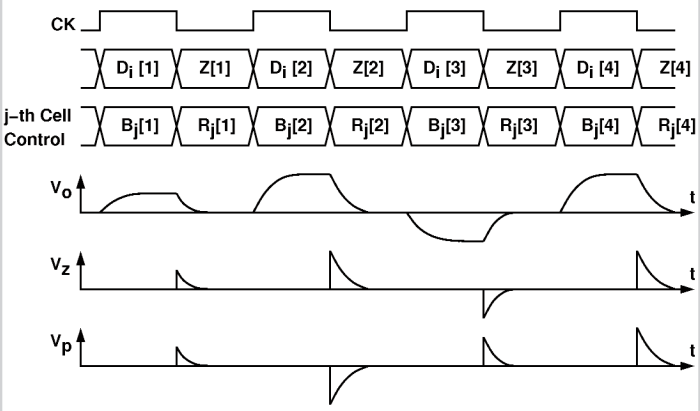

Figure 10.7.2: DAC operation and waveforms.

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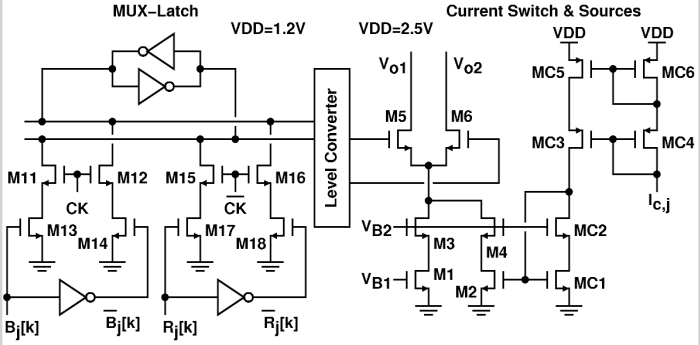

Figure 10.7.3: Schematic of the M-DAC current cell.

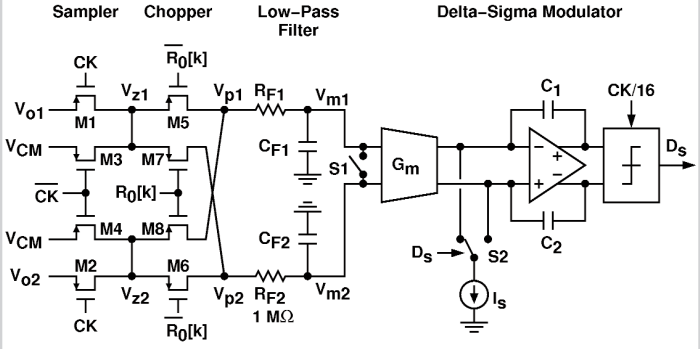

Figure 10.7.4: Schematic of the analog signal-path calibration.

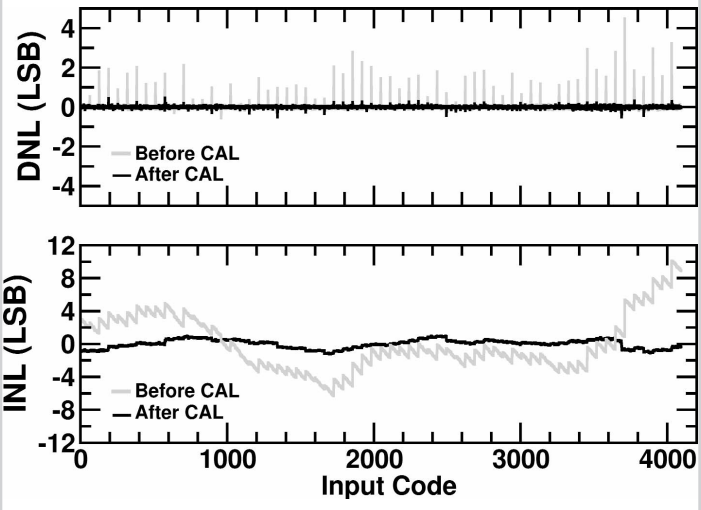

Figure 10.7.5: Measured DNL and INL.

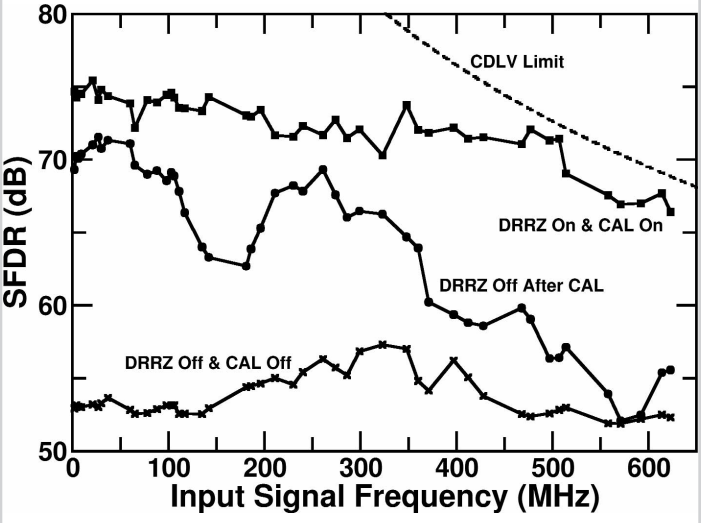

Figure 10.7.6: Measured SFDR versus input signal frequency.

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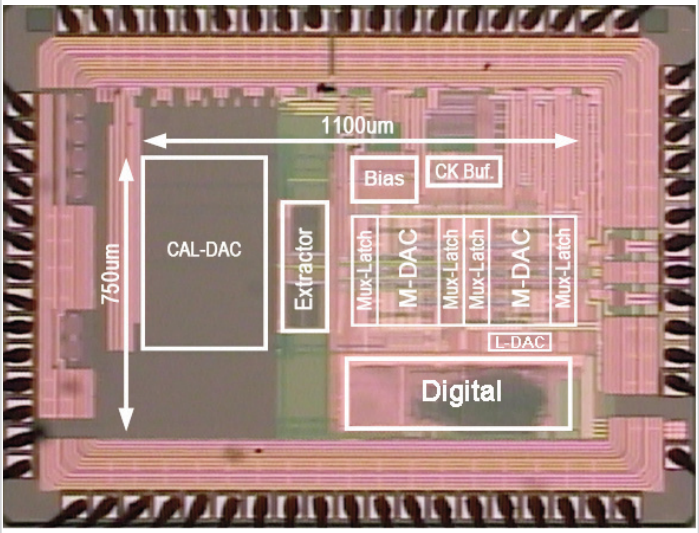

Figure 10.7.7: Chip micrograph.

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