A 2.5–5.6 GHz Subharmonically Injection-Locked All-Digital PLL With Dual-Edge Complementary Switched Injection

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***Abstract*— A 2.5–5.6 GHz low-phase-noise subharmonically injection-locked sub-sampling all-digital phase-locked loop with a dual-edge complementary switched injection technique is presented. While previously reported injection-locked phase-locked loops (ILPLLs) require additional circuitry for resolving a phase alignment mismatch between the PLL loop and injection path, the presented ILPLL exhibits a simplified architecture owing to the proposed injection technique and sub-sampling bang-bang phase detector (SSBBPD). Because the proposed injection technique exploits dual-edge injection, we analyze the performance impact of dual-edge injection when inaccurate injection timing occurs. This paper also offers an analysis of the injection technique based on the charge transfer and derives the realignment factor of the injection. With the proposed injection technique and the direct connection of the digitally controlled oscillator (DCO) clock to the SSBBPD, the timing mismatch between the PLL loop and injection path becomes insensitive to voltage and temperature drift. The proposed ILPLL prototype is fabricated in a 65-nm CMOS process and achieves a 168-fs integrated rms jitter over 1 kHz to 40 MHz at a 5-GHz output frequency with 156.25-MHz reference clock while consuming 15.4 mW with an active area of 0.06 mm^2.**

***Index Terms*— All-digital PLL (ADPLL), dual-edge injection, frequency detector, injection-locked oscillator (ILO), reference spur, sense-amplifier, sub-sampling PLL.**

I. Introduction

PHASE-LOCKED loops (PLLs) have an important role in many high-performance serial link applications. With the requirements for a low area and wide range in the PLLs, it is highly desirable to use an inverter-based ring oscillator. However, due to the inferior phase noise characteristic of the ring oscillator, it is difficult to generate a low-jitter clock because the maximum PLL bandwidth limited to one tenth of the reference frequency.

Recently, injection-locked oscillators (ILOs) have been explored to generate a low jitter clock with low power consumption. There have been several approaches to implementing a clock multiplier with subharmonic injection locking [1]–[25]. The main challenge of the injection-locked clock multiplier (ILCM) is to keep the free-running frequency of the oscillator near the target frequency across the PVT variations. Fig. 1(a) shows a clock multiplier whose frequency is initially set to integer times of the injection clock frequency by a frequency-locked loop (FLL) [1], [2]. The phase noise of the clock multiplier inside the lock-in range f_L is significantly decreased and determined mainly by the phase noise of the injection clock. However, such implementations are difficult to apply in practice because the free-running frequency drifts with voltage and temperature variations. Further, although the oscillator is perfectly tuned with the Nth harmonic injection frequency, injection alone cannot suppress the phase noise sufficiently in the low-frequency region, where flicker noise dominates the noise level. This is because an injection-locked oscillator is basically a first-order low-pass filter in terms of phase noise [3], whereas the attenuation slope of the phase noise in the region below the flicker noise corner frequency f_C is higher than -20 dB/decade. As shown in Fig. 1(b), injection locking with a frequency-tracking loop (e.g., PLL with injection) can be a solution for this purpose [3]–[15]. Fig. 1(c) illustrates a comparison of the phase noise between the injection alone and a PLL with injection. When the oscillator has a higher f_C, the phase noise below f_C decreases significantly by combining the injection and PLL.

Recently, there have been several efforts to employ continuously frequency-tracking loop (FTL) in the PLL-based ILCM, the replica-based ILCM and the real-time FTL-based ILCM. In the PLL-based ILCM [3]–[15], the challenge is to mitigate a timing conflict between the injection path and PLL loop. With the timing mismatch between PLL and injection paths, the frequency error of the oscillator cannot be detected. This is because the injection periodically reset the phase of the oscillator before the phase detection by the PLL path. To solve

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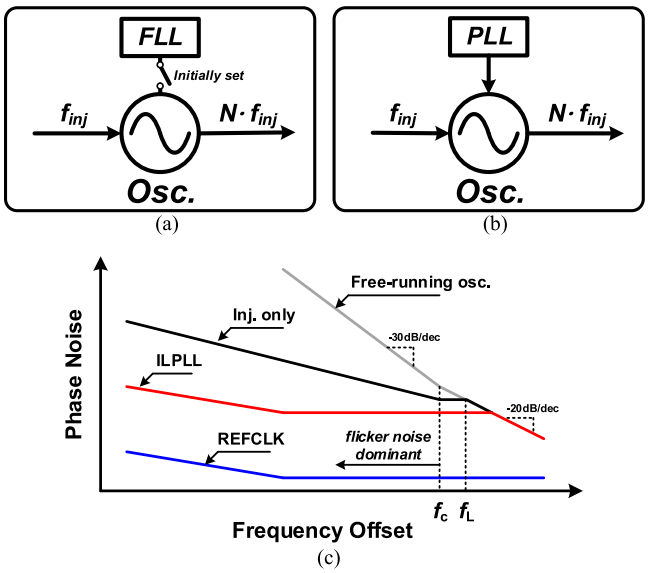


Fig. 1. Clock multiplier schemes using (a) injection only and (b) PLL with injection. (c) Illustrated phase noise comparison between injection only and PLL with injection.

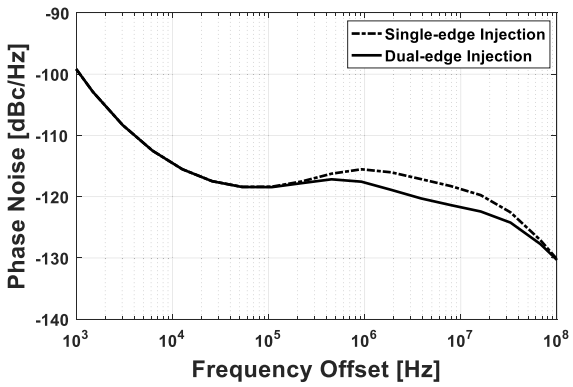


Fig. 2. Simulated phase noise of ILPLL with single-edge injection and dual-edge injection (F_{OUT} = 5 GHz, F_{REF} = 156.25 MHz and β = 0.4).

the timing issue, prior architectures [4]–[6] used an injection timing calibration circuit. However, the additional loop operates in the background, which complicates the structure and entails additional power consumption. To solve the race condition, several ILCMs use a replica oscillator or delay cell [16]–[20] that separates the PLL loop from the injection clock, thereby eliminating interference between two loops. However, this leads to additional power dissipation and area. As an alternative, a real-time FTL-based ILCM using a phase detector has been recently developed [21]–[25]. It has an advantage of adjusting the frequency by detecting the frequency drifts of the oscillator. However, part of the injection effect is sacrificed for detecting the frequency drift in [21]–[23]. Also, limitation of the frequency capture range in [24] and [25] can lead to a harmonic lock when large voltage and temperature variations are encountered.

In this paper, we propose injection-locked PLL (ILPLL) with simplified overall architecture owing to the proposed dual-edge complementary switched injection technique and sub-sampling bang-bang phase detector (SSBBPD) [10]. The proposed ILPLL eliminates the timing conflict between the injection and PLL path without injection timing calibration circuit. Further, it maintains superior jitter performance against the PVT variations. To investigate the effect of dual-edge injection on the reference spur, we analyze the frequency error and derive reference spur when inaccurate injection timing occurs in the ILPLL. Moreover, the SSBBPD makes the phase alignment mismatch between two control paths less sensitive over the voltage and temperature variations. Hence, the proposed ILPLL can generate a wide range clock without adjusting the injection timing because the injection path does not comprise a delay line.

The remainder of the paper is organized as follows. Section II presents the timing issue of the ILPLL including occurrence of frequency error and discusses the impact on the reference spur from inaccurate injection timing. Section III describes the overall architecture with a detailed circuit implementation and its proposed analysis. Section IV discusses the measurement results of the test chip and Section V concludes with a summary.

II. Analysis of Dual-Edge Injection in ILPLL

In the proposed ILPLL, the dual-edge injection is performed to obtain the effect of doubling the multiplying factor. The phase noise comparison between the single-edge injection and the dual-edge injection is shown in Fig. 2. The phase noise transfer function of an injection-locked ADPLL is approximated as a linear model in [14] and the phase noise of the oscillator is based on Leeson's model in [27]. The phase noise of the dual-edge injection is more suppressed since the multiplying factor is halved in the transfer function representing the up-conversion of the reference noise, thereby the dual-edge injection improves the jitter performance. However, the duty-cycle error of the reference clock as well as the timing mismatch between the PLL loop and injection path can cause a reference spur in the ILPLL. The detailed analyses and effects are presented as follows.

In order to derive optimal injection timing in a conventional ILPLL, the total delay by the injection D_1 and PLL feedback D_2 should be integer times the period of the PLL output clock T_{DCO} as shown in Fig. 3(a). This requirement can be expressed as

$$D_1 + D_2 = k \cdot T_{DCO} \ (k = 1, 2, 3, \ldots) \tag{1}$$

where k is the delay in cycles. When $D_1 + D_2$ is not equal to integer times the digitally controlled oscillator (DCO) clock period, the offset frequency appears in the DCO and increases the reference spur as studied in [4]. To further investigate the effect of the dual-edge injection adopted in [9]–[11] and [22], the duty-cycle error of the injection clock is additionally considered. Fig. 3(b) shows the timing diagram of a stable PLL without an injection. When dual-edge injection is performed with the initial phase mismatch θ_{init} and duty-cycle phase error $\Delta\theta_{duty}$, the DCO frequency drift occurs in response to the phase error detected by the PLL loop. Fig. 3(c) presents a timing diagram of a stable PLL with dual-edge injection.

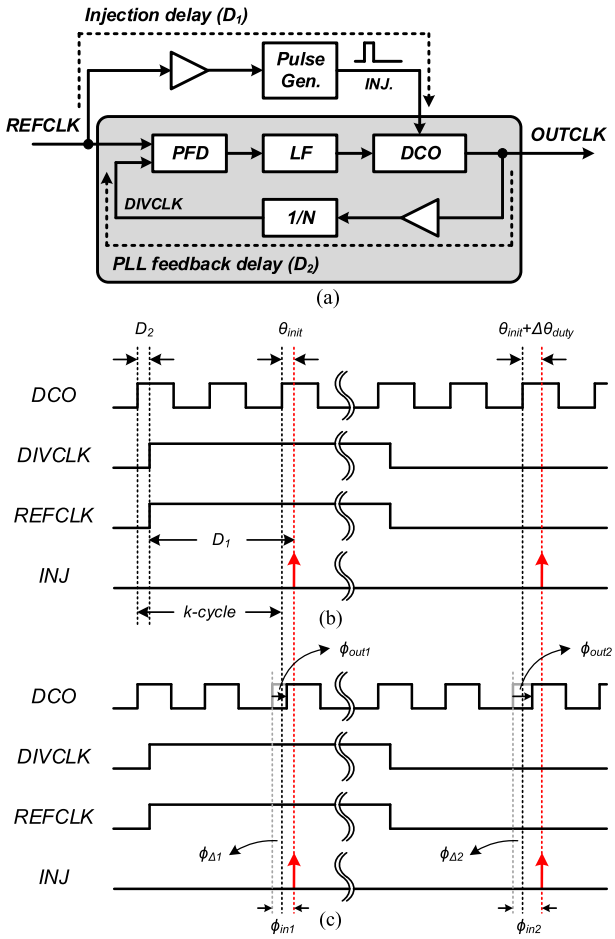


Fig. 3. (a) Block diagram of conventional ILPLL. Timing diagrams of stable PLL (b) without injection and (c) with dual-edge injection.

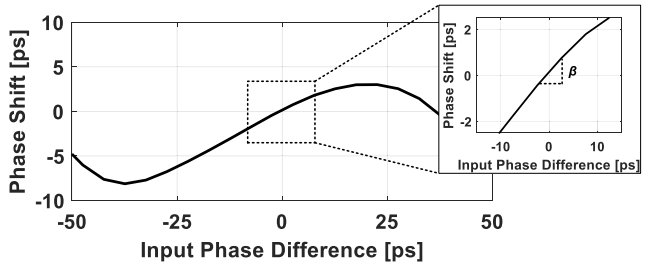


Fig. 4. Simulated phase shift by an injection according to input phase difference with the oscillator of 5-GHz output frequency.

To simplify the analysis, we assume an ideal linear relationship between output phase shift and input phase deviation. Phase domain response (PDR) simulation result of the complementary switched injection [10] is shown in Fig. 4, where the validity of the assumption is demonstrated under small phase shift. The ratio of the output phase shift ϕ_{out1} (ϕ_{out2}) to the input phase deviation ϕ_{in1} (ϕ_{in2}) is denoted by realignment factor β and their relationship can be expressed as $\phi_{out1} = \beta \cdot \phi_{in1}$ ($\phi_{out2} = \beta \cdot \phi_{in2}$). The input phase deviations of dual-edge are expressed as

$$\phi_{in1} = \theta_{init} + \phi_{\Delta1} \tag{2}$$

$$\phi_{in2} = \theta_{init} + \Delta\theta_{duty} + \phi_{\Delta2} \tag{3}$$

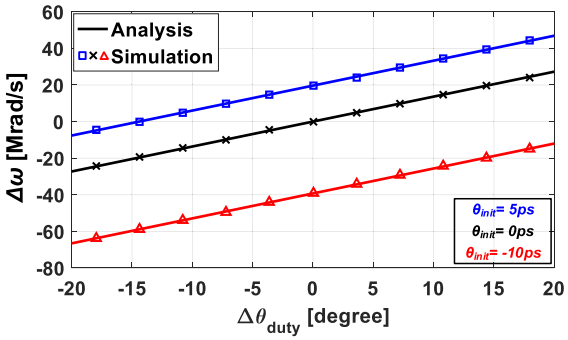


Fig. 5. Calculated and simulated offset frequency according to duty-cycle error and delay mismatch (F_{OUT} = 5 GHz, F_{REF} = 156.25 MHz, k = 0 and $\beta = 0.4$).

where $\phi_{\Delta1}$ and $\phi_{\Delta2}$ are the phase offset on the verge of the injection. These are expressed as

$$\phi_{\Delta1} = k \cdot \Delta\omega \cdot T_{DCO} \tag{4}$$

$$\phi_{\Delta2} = N/2 \cdot \Delta\omega \cdot T_{DCO} - (\phi_{out1} - \phi_{\Delta1}) \tag{5}$$

where $\Delta\omega$ is the offset frequency of the DCO and N is the PLL division factor. The total output phase shift by the dual-edge injection is expressed as

$$\phi_{out1} + \phi_{out2} = N \cdot \Delta\omega \cdot T_{DCO}. \tag{6}$$

According to the (2)–(8), the frequency deviation of the DCO is expressed as

$$\Delta\omega = \frac{\beta \cdot \theta_{init} + \beta/(2-\beta) \cdot \Delta\theta_{duty}}{(N/2 - k \cdot \beta) \cdot T_{DCO}}. \tag{7}$$

The results of the analysis and Verilog simulation are shown in Fig. 5. The simulation is performed on the entire ILPLL model including the injection-locked DCO, the phase detector, and the digital loop filter. In the Verilog model of the injection-locked DCO, the output phase shift by the injection is defined as the product of the input phase deviation and the injection strength. The simulation results verify the analysis and indicates that the offset frequency increases with the duty-cycle error and initial phase mismatch.

From (2)–(7), the reference spur of the ILPLL is derived in the Appendix. For a fixed k, the calculated and simulated reference spur according to the duty-cycle error is indicated in Fig. 6. The duty-cycle error impacts on the both the reference frequency F_{REF} and two times reference frequency $2F_{REF}$ spurs. On the other hand, the initial phase mismatch has minimal influence on the F_{REF} spur and only affects $2F_{REF}$ spur. Therefore, both the duty-cycle error and initial phase mismatch should be minimized for improved performance of both spurs simultaneously. In this work, the presented ILPLL enables $k = 0$ owing to the SSBBPD, which makes injection timing error less susceptible to voltage and temperature variations. Also, it comprises a duty-cycle corrector (DCC) to reduce the reference spurs. Owing to the zero intrinsic injection delay time, the proposed ILPLL can generate a wide range clock without adjusting the injection delay time.

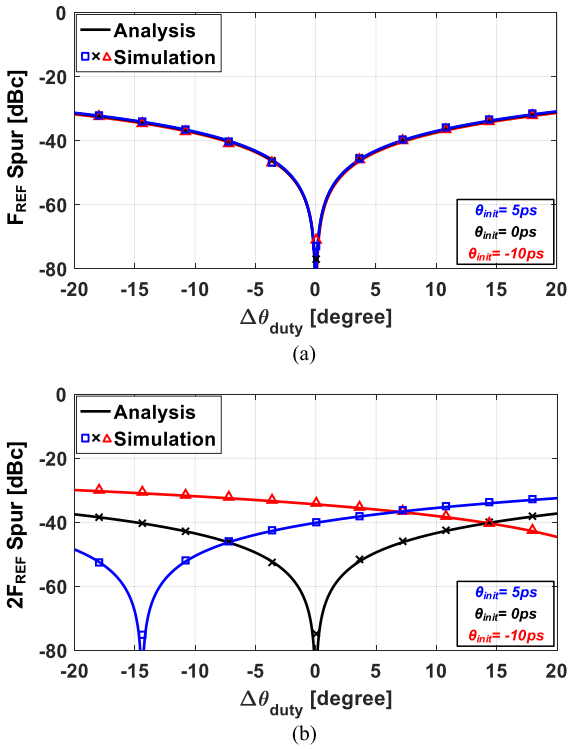


Fig. 6. Calculated and simulated spurs of the (a) F_{REF} and (b) $2F_{REF}$ according to delay mismatch and duty-cycle (F_{OUT} = 5 GHz, F_{REF} = 156.25 MHz, k = 0 and $\beta = 0.4$).

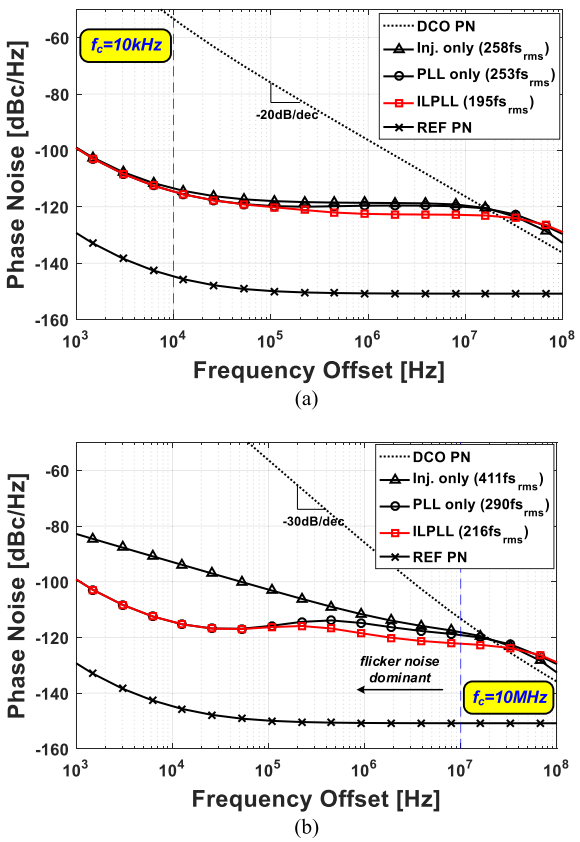


Fig. 7. Simulated phase noise of free-running DCO, reference clock, injection only, PLL only, and PLL with injection when (a) f_C = 10 kHz and (b) f_C = 10 MHz. (f_{out} = 5 GHz, f_{ref} = 156.25 MHz and $\beta = 0.6$).

III. Proposed ILPLL

A. Phase Noise Analysis

In this section, we analyze the phase noise characteristic of the ILCM in relation with the flicker noise corner frequency f_C of the oscillator. Fig. 7(a) shows the phase noise comparisons between injection only, PLL only, and ILPLL when the oscillator has a f_C of 10 kHz. The phase noise with the injection alone scheme is comparable to that of the PLL alone and the ILPLL. The PLL loop marginally improves the phase noise performance as the improvement of the integrate RMS jitter from 1 kHz to 40 MHz is 63 fs. Therefore, considering extra power dissipation and area, the additional PLL loop may not be desired or it would be sufficient to employ a low bandwidth frequency-tracking loop in order to desensitize against PVT variations. On the other hand, when the oscillator has a higher f_C of 10 MHz as shown in Fig. 7(b), the injection alone cannot cut down the phase noise sufficiently due to the first-order attenuation. Therefore, the additional PLL loop must be employed to suppress the phase noise below f_C as the integrated RMS jitter of the ILPLL decreases by about half in comparison with that of the injection alone. It is noteworthy that f_C becomes higher as CMOS technology scales down. In this paper, the proposed ILPLL combines the injection locking with a PLL loop to cope with the high f_C of the ring oscillator.

B. Overall Architecture

The overall architecture of the proposed ILPLL is shown in Fig. 8. It employs the complementary switched injection technique and sub-sampling technique to overcome the injection timing issues. In this architecture, the main PLL loop, which is the sub-sampling PLL, contributes to the suppression of the phase noise of the region under the flicker noise corner frequency as discussed before, and the reference clock injection widens the PLL bandwidth.

The front-end of the reference clock consists of a DCC and single-to-differential converter. The DCC is employed to minimize the F_{REF} and $2F_{REF}$ spur because the injection occurs at the dual-edge clock. From the output of the DCC, the differential injection clock is generated by the single-to-differential converter, which is not only injected into the DCO but also triggers the SSBBPD without a buffer circuit. The SSBBPD samples the DCO clocks before the level shifter, thus the PLL loop and injection path can have the same phase alignment time. In case of the input offset voltage of the SSBBPD, the offset timing of the PLL feedback path can be adjusted by the offset control code. Further, the direct proportional path from the SSBBPD to the DCO is adopted to minimize the loop latency [29]. During the operation of the ILPLL, the FLL works continuously in the background to prevent it from harmonic lock due to voltage and temperature drifts. Also, it supports a wide range of output frequency by controlling the frequency code word (FCW).

C. DCO With Complementary Switched Injection Technique

The circuit implementations of the DCO is described in Fig. 9. The DCO is composed of two digitally-controlled resistors (DCRs): one is for coarse frequency tuning by the FLL [30] and the other is for fine frequency tuning by the

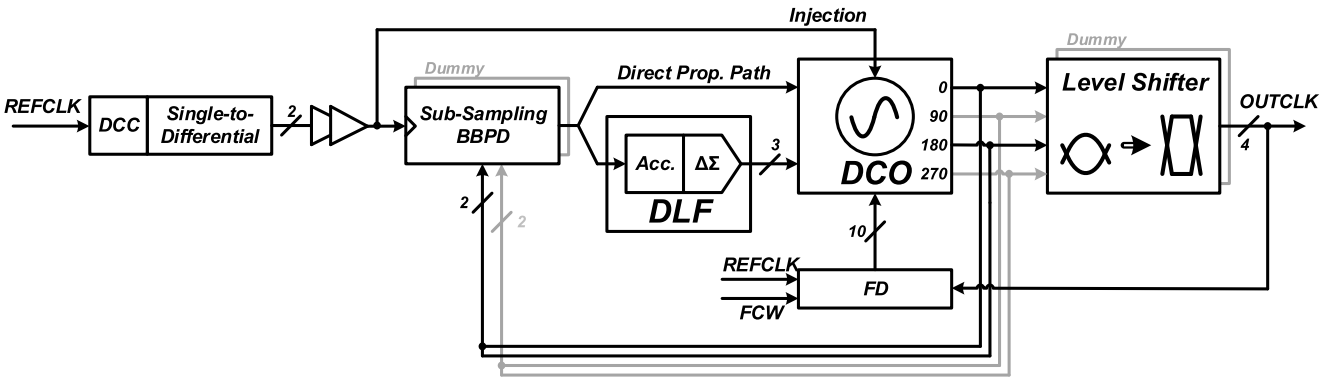


Fig. 8. Overall architecture of proposed ILPLL.

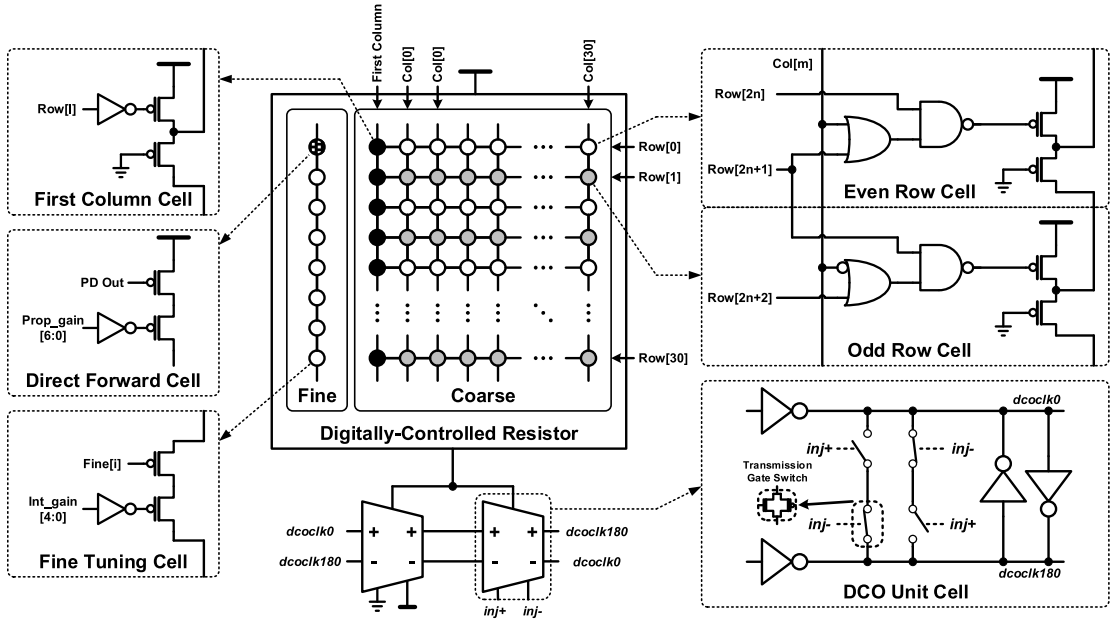


Fig. 9. Injection-locked DCO implementation.

PLL. The step size of the coarse DCR is about 4 MHz and that of the fine DCR can vary from 0.6 MHz to 2 MHz. In order to inject a reference clock into the oscillator, a pulse generator is widely used to create a narrow pulse [3]–[5], [7], [8], [21]–[23]. However, as the frequency of the oscillator increases, it becomes more difficult to generate a short injection pulse. In this work, a complementary switched injection technique is incorporated to accomplish the effect of short injection pulse and zero delay injection [9], [10].

The DCO cell contains two pairs of series-transmission-gate switches between the differential clock nodes. The differential injection clocks operate the switches complementarily and the two pairs of the complementary switches maintain a constant capacitance on the DCO clock nodes. When one switch is off and the other is on, no direct current flows between the differential clock nodes and thus no effect is incurred on the DCO clock phase. On the other hand, when the switch states are swapped, a charge is injected into or drawn from the differential clock nodes. Further, during the transition of the switching operation, i.e., close to the crossing points of the differential injection clocks, direct short-circuit current flows on between the DCO differential clock nodes. As a result, phase shift occurs on the DCO clock.

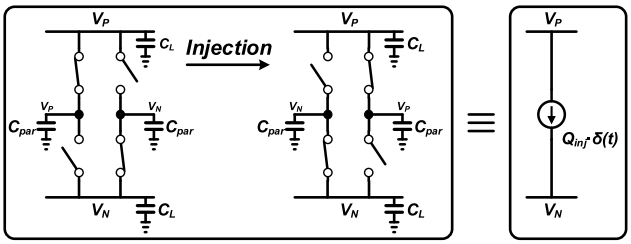


Fig. 10. Simplified model of switched capacitor injection.

In the circuit model of the complementary switched injection shown in Fig. 10, the load capacitance C_L of the DCO clock node and parasitic capacitance C_{par} representing the drain junction and gate-drain capacitance of the switches are included. During injection, there are two mechanisms of current flow between the differential nodes as mentioned above. One is the charge transfer caused by the switched capacitor operation due to the parasitic capacitance and the other is short-circuit current across the switches partially on during the rise/fall overlap time of the injection clock. The simulation results in Fig. 11 indicate that the short-circuit current is negligible in comparison with the current from the switched capacitor operation. This is because

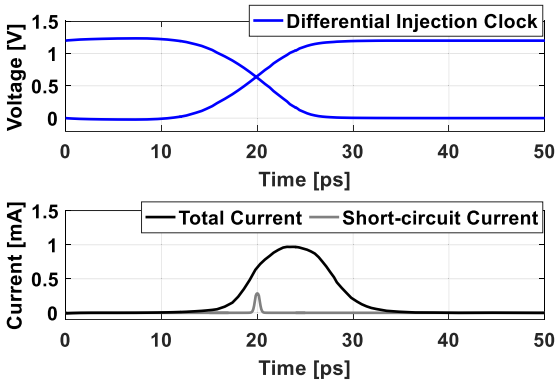


Fig. 11. Simulation result of current between differential nodes during injection.

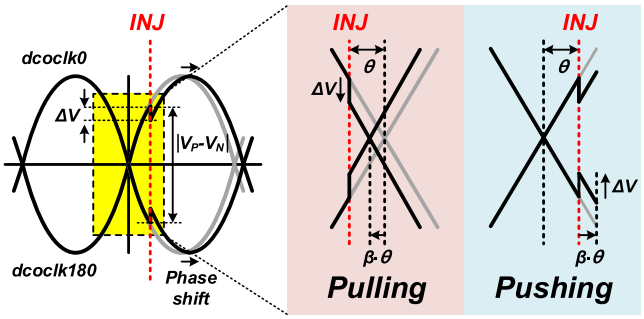


Fig. 12. Simplified injection effect on time-domain waveform.

the series-connected switches are simultaneously turned on weakly and only briefly during the transition time, whereas they are fully turned on and off for the switched capacitor operation. Assuming that the transition time of the injection clock is short, the amount of charge transfer on the *dcoclk0* and *dcoclk180* nodes after injection can be expressed as

$$Q_{inj} = C_{par} \cdot |V_P - V_N| \tag{8}$$

where V_P and V_N are node voltages of the *dcoclk0* and *dcoclk180* at the injection time. Then, the voltage variation of the *dcoclk0* and *dcoclk180* nodes due to the injection can be expressed as

$$\Delta V = |V_P - V_N| \cdot C_{par} / \left(C_{par} + C_L\right). \tag{9}$$

Consequently, under the approximation of linearity near the crossing points of the differential DCO clock as shown in Fig. 12, we can represent a realignment factor as

$$\beta = 2C_{par} / \left(C_{par} + C_L\right). \tag{10}$$

Fig. 13(a) and (b) illustrate the PDR and realignment factor, respectively, when switch size and injection transition time are varied. It indicates that the realignment factor increases with an increased injection switch size. This is because the parasitic capacitance C_{par} has a linear relationship with the switch size. On the other hand, a longer transition time weakens the realignment factor because the clock edges move faster while the injection switches are in the transition region. Consequently, a longer transition time leads to more severe

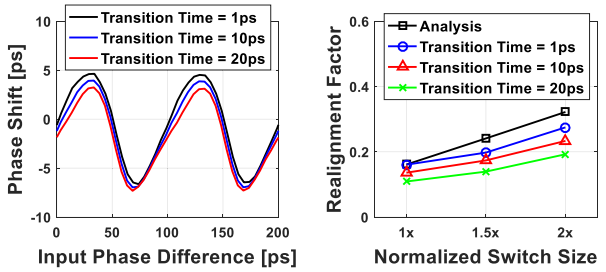


Fig. 13. Simulation results of (a) phase domain response (PDR) and (b) realignment factor according to injection transition time and switch size.

asymmetry in the PDR, which implies that pulling the phase of the oscillator is easier than pushing.

D. SSBBPD and Front-End

In the ILPLL, one of the most important keys to high performance is minimizing the phase alignment mismatch between the PLL loop and injection path. Although the two control paths are initially matched, voltage and temperature drifts cause a timing mismatch depending on the delay sensitivity to the drift. For example, the delay variation of an inverter-based delay line in terms of voltage and temperature variations ranges from -30% to 100% [28]. To solve this problem, an injection timing calibration circuit is proposed in [4]–[6]. However, this entails a substantial increase of power dissipation. In this work, an SSBBPD is adopted instead of the injection timing calibration circuit. As a result, the SSBBPD allows removing the latency of the buffer down to zero and makes the injection timing error less sensitive against the voltage and temperature drift.

The SSBBPD detects the voltage difference between the differential DCO clocks when it is triggered by the reference clock. Therefore, the DCO clock edge and the reference clock edge are aligned by the PLL as shown in Fig. 14(a). With the direct connection of the DCO clock to the SSBBPD, the proposed sense-amplifier [10] based on the tail-less structure eliminates the input capacitance variation due to the clock toggling as shown in Fig. 14(b). In comparison with the conventional sense-amplifier [31], the loading capacitance of the DCO output remains unchanged even if the reference clock toggles. As a result, it enables the DCO frequency to remain constant as indicated in Fig. 14(c).

In the designed sense-amplifier, the standard deviation of the input-referred offset is simulated as 28 mV_{diff}, as shown in Fig 15. This offset voltage can lead to a timing mismatch of the two control paths as shown in Fig. 16(a). Therefore, the sense-amplifier is equipped with a mismatch calibration capability of covering up to 145-mV_{diff} offset by adjusting the offset control code. When the offset control code is initially set, the delay of the PLL feedback path varies less than 2.7 ps over the voltage and temperature variations as shown in Fig. 16(b). As a result, timing mismatch of the phase alignment between the two control paths is reduced to less than 2.7 ps in the presence of the voltage and temperature drift.

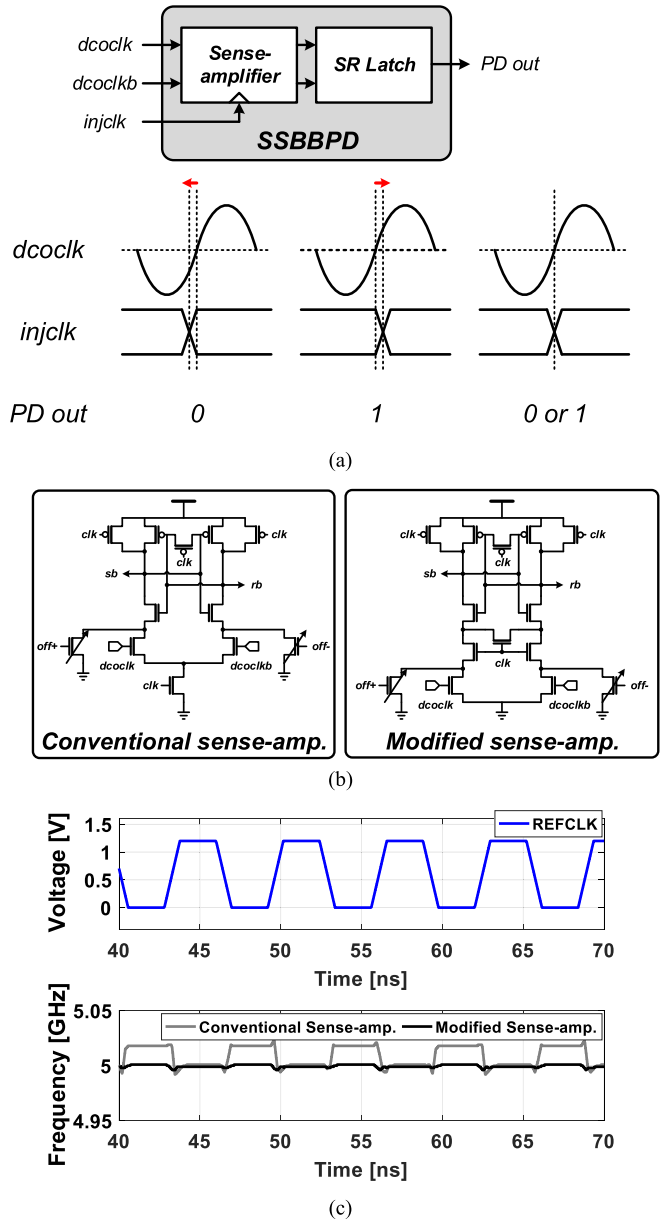


Fig. 14. (a) Time-domain waveforms of the SSBBPD. (b) Conventional sense-amplifier and modified tail-less sense-amplifier. (c) Time-domain DCO frequency between conventional sense-amplifier and modified structure.

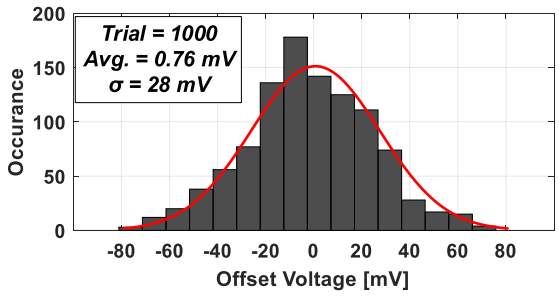


Fig. 15. Monte-Carlo simulation results of the sense-amplifier offset.

The front-end of the reference clock consists of a DCC and single-to-differential converter as shown in Fig. 17. The DCC is composed of two-stage inverter-based unit cell. By inserting controllable pull-up/down MOSFETs in every stage, the rising

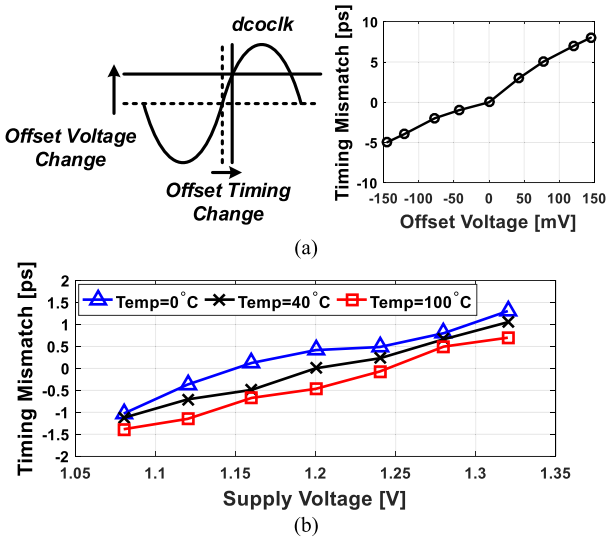


Fig. 16. (a) Simulation results of the timing mismatch according to the offset voltage with illustrated timing diagram. (b) Simulation results of the timing mismatch across supply voltage and temperature variation.

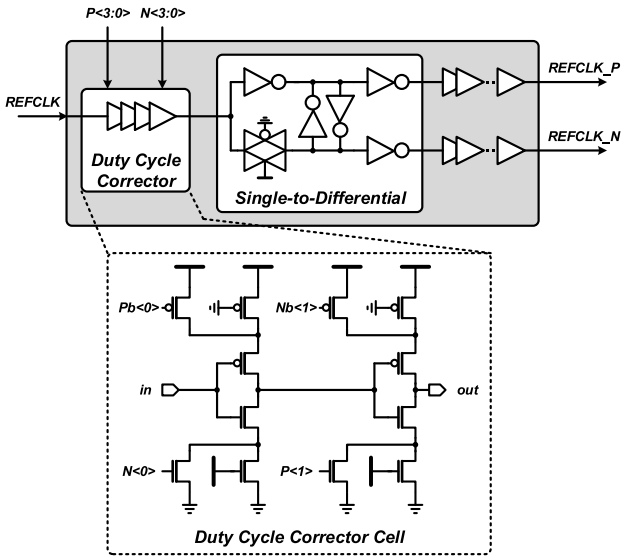


Fig. 17. Block diagram of front-end of reference clock.

and falling time of the buffered reference clock can be controlled and the difference between rising and falling time makes the duty-cycle adjustable. The duty-cycle error can be calibrated from −57 ps to 57 ps.

E. Frequency Detector

In the PLL loop, the frequency detector works at the startup of the PLL and operates in the background. It does not detect the small frequency deviation of the injection-locked oscillator. However, because the frequency of the oscillator can vary significantly with the voltage and temperature variations, it can prevent harmonic lock from the frequency drift. Fig. 18(a) shows the frequency detector, the structure of which is based on [32], with the following timing requirements. First, the *REF_SYNC*, which is a reference clock synchronized by

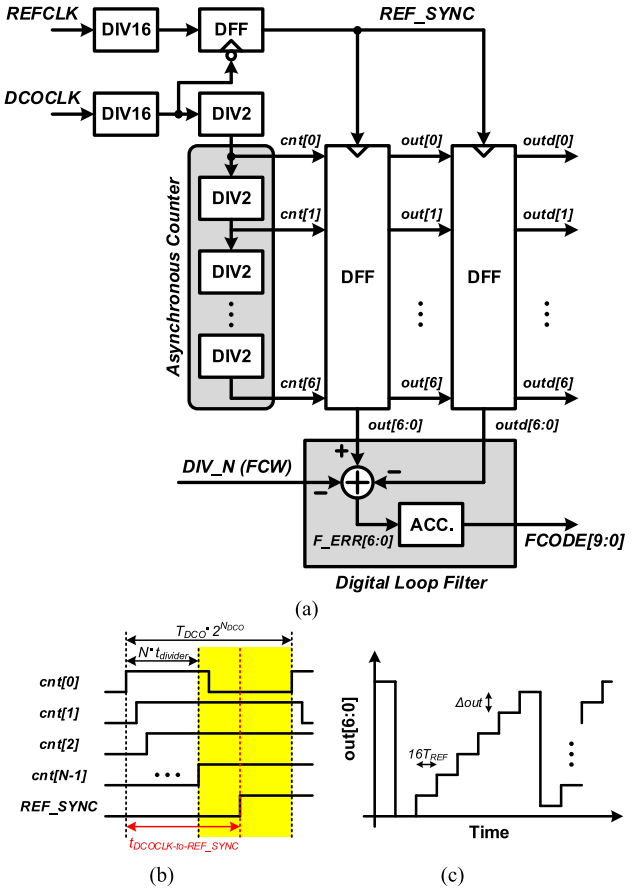


Fig. 18. (a) Block diagram of frequency detector. (b) Timing diagram for timing constraint of frequency detector. (c) Counter output.

DCOCLK, should lag the last output of the divider. Further, the delay from *DCOCLK* to *REF_SYNC* should be less than a period of the *DCOCLK* as shown in Fig. 18(b). Hence, the timing constraint is expressed as

$$N_C \cdot t_{divider} < t_{DCOCLK-to-REF\_SYNC} < T_{DCO} \quad (11)$$

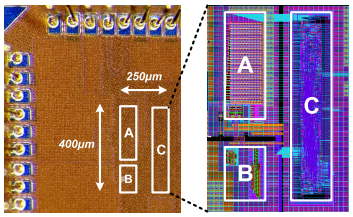
where N_C is the number of dividers in the asynchronous counter and $t_{divider}$ is the latency of the divider. In [32], *REF_SYNC* is synchronized with the negative edge of *DCOCLK* assuming the last output of the divider leads the negative edge of *DCOCLK*. However, as the frequency of the oscillator and the division factor of the PLL increase, it is difficult to satisfy the timing requirements. In order to meet the timing requirements in the proposed ILPLL, the *DCOCLK* is divided before the counter and the requirement is modified as

$$N_C \cdot t_{divider} < (T_{DCO}/2) \cdot 2^{N_{DCO}} \quad (12)$$

where N_{DCO} is the number of divide-by-2 circuits from the*DCOCLK* to the counter input. The number of dividers in the counter and the frequency resolution of the counter can be expressed as

$$N_C = \left\| \log_2 (T_{REF}/T_{DCO}) \right\| + N_{REF} - N_{DCO} + M \quad (13)$$

$$\Delta f_{LSB} = \frac{1}{T_{REF}} \cdot \frac{2^{N_{DCO}}}{2^{N_{REF}}} \quad (14)$$



	Block Description	Power [mW]
A	DCO, SSBBPD	8
B	FD, S-to-D	1
C	Digital Loop Filter	6.4

Fig. 19. Die microphotograph and its block description with power consumption.

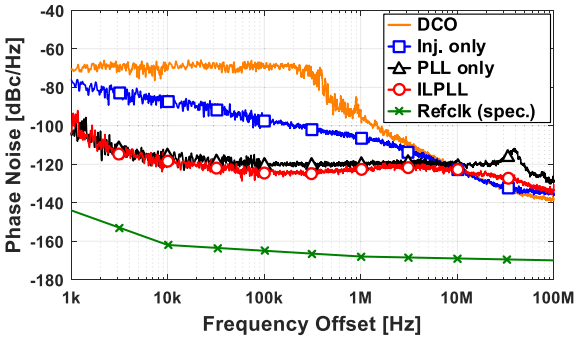


Fig. 20. Measured phase noises of a 5-GHz with injection only, PLL only, and ILPLL.

where T_{REF} is the period of the reference clock, N_{REF} is the number of divide-by-2 circuits from thereference clock to the counter input, and M is the number of additional dividers determined by the DCO maximum frequency. In this work, the designed frequency detector has a parameter of $N_C = 6$ and $\Delta f_{LSB} = 156.25$ MHz, which result from $N_{DCO} = 4$, $N_{REF} = 4$, and $M = 1$, thereby satisfying the timing requirements with detecting up to 10-GHz of DCO frequency. As a result, the frequency error is updated by 16 times the reference period as shown in Fig. 18(c) and derives the target DCO code through a digital accumulator.

IV. Measurements Results

The prototype of the proposed ILPLL was fabricated in 65-nm CMOS technology and occupied a total active area of 0.06 mm^2. Fig. 19 shows the die microphotograph, which indicates that the digital logic occupies the majority of the area. With a 156.25-MHz reference clock, the power consumption of the ILPLL is 15.4 mW with a 1.2-V supply at 5-GHz output frequency.

Fig. 20 shows the phase noise spectrum of the 5-GHz clock. With the 156.25-MHz injection clock, the phase noise does not show sufficient reduction below the 10-MHz offset frequency because the slope of the DCO phase noise in the region is steeper than −20 dB/decade due to the flicker noise. However, with the combination of a PLL and injection, the phase noise decreases to −123.2 dBc/Hz at the 1-MHz offset frequency and the integrated RMS jitter from 1 kHz to 40 MHz becomes 168 fs. These are superior results to those of the PLL alone indicating −121.1 dBc/Hz at 1-MHz offset and 390-fs integrated jitter. This result demonstrates that in-band phase noise is considerably suppressed by the PLL loop and

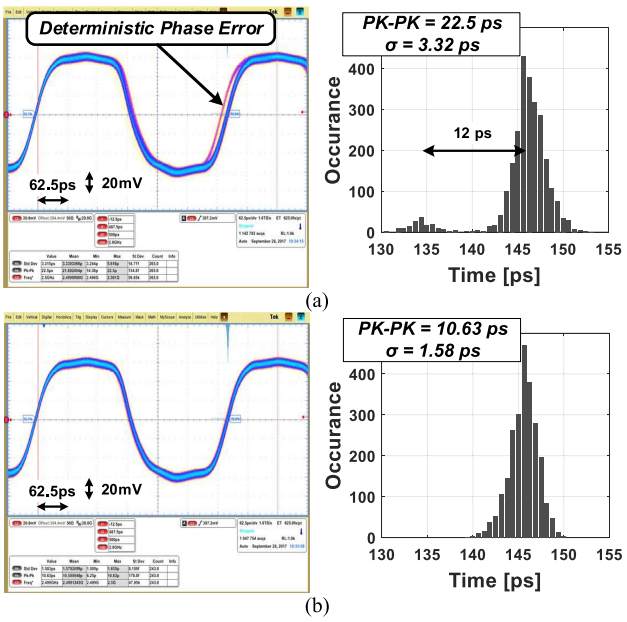


Fig. 21. Measured 2.5-GHz output clock and jitter histogram (a) when delay mismatch occurs and (b) when offset code of the SSBBPD is optimized.

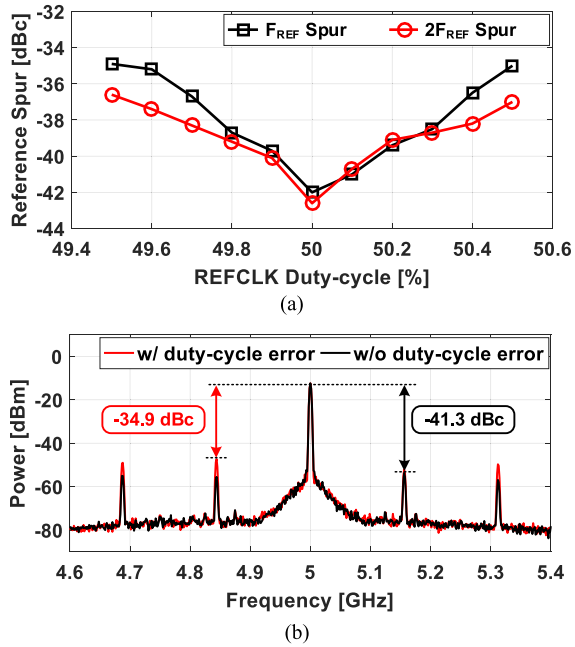


Fig. 22. (a) Measured spurs of the F_{REF} and $2F_{REF}$ versus duty-cycle of the reference clock. (b) Measured output spectrums with and without duty-cycle error of the at 5-GHz frequency.

the phase noise around the PLL bandwidth is reduced by the injection, which results in the reduced peaking as the phase margin is improved.

Fig. 21 shows the measured waveforms of the output clock and jitter histogram with the number of acquisitions more than a million times. When a delay mismatch exists between the injection and PLL paths, the deterministic phase error occurs as indicated in Fig. 21(a). The peak-to-peak jitter and RMS jitter are 22.5 ps and 3.32 ps, respectively.

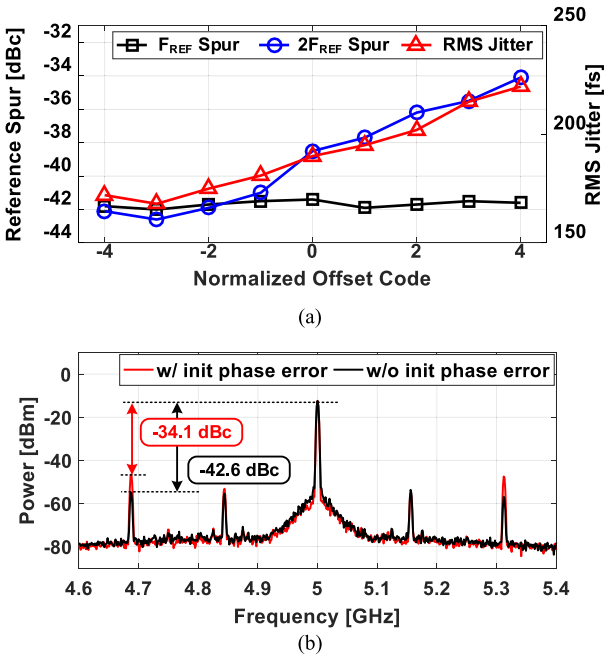


Fig. 23. (a) Measured RMS jitter and spurs of the F_{REF} and $2F_{REF}$ versus offset code. (b) Measured output spectrums with and without delay mismatch at 5-GHz frequency.

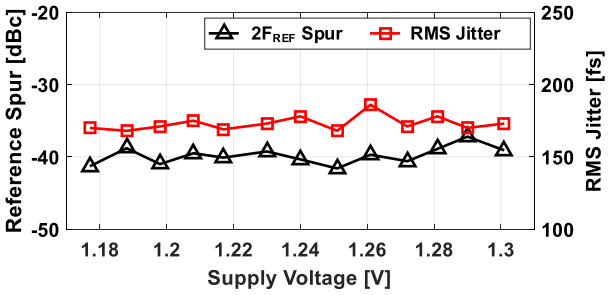


Fig. 24. Measured $2F_{REF}$ spur and RMS jitter over supply voltage variation.

By adjusting the offset code of the SSBBPD, deterministic phase error disappears and peak-to-peak jitter and RMS jitter decrease to 10.63 ps and 1.58 ps, respectively as shown in Fig. 21(b).

Fig. 22(a) presents the measurement results of the F_{REF} and $2F_{REF}$ spur according to the variation of the duty-cycle of the reference clock. With increased duty-cycle error, spur at the F_{REF} and $2F_{REF}$ is degraded as shown in Fig. 22(b). Fig. 23(a) indicates the measurement results of the reference spur and integrated RMS jitter due to the delay mismatch under the 50% duty-cycle reference clock. As previously analyzed, the delay mismatch does not affect the F_{REF} spur. However, it has significant influence on the $2F_{REF}$ spur as shown in Fig. 23(b). In the optimized offset condition, the $2F_{REF}$ spur and the integrated RMS jitter have the best performance. This verifies that there is nearly zero conflict between the two aligning mechanisms in the proposed ILPLL. The F_{REF} spur at the optimized offset condition is -42 dBc, which is mainly due to the supply voltage fluctuation from the reference clocking circuitry leaking the substrate to the DCO, thereby impeding additional improvement of the reference spur.

TABLE I
ILCM PERFORMANCE COMPARISON

	[5]	[7]	[11]	[17]	[18]	[22]	[26]	This Work
Technology [nm]	40	55	65	65	65	65	28	**65**
Topology	PLL	PLL	PLL	Dual-loop	Dual-loop	PLL	MDLL	**PLL**
Reference frequency [MHz]	50	27	150	150	300	125	75	**156.25**
F_{REF} phase noise @ 1MHz [dBc/Hz]	-145	-146.5	NA	-163	NA	NA	NA	**-165**
Dual-edge injection	No	No	Yes†	No	No	Yes†	Yes†	**Yes††**
Output frequency [GHz] (Range [GHz])	1.6 (0.4-1.6)	0.216	0.9 (0.52-1.15)	0.9 (0.39-1.41)	1.2 (0.5-1.6)	5 (2.5-5.75)	2.4	**5 (2.5-5.63)**
Division factor	32	8	6	6	4	40	32	**32**
Integrated RMS jitter [ps] (Range [Hz])	2.29 (10k-30M)	2.4 (1k-40M)	0.42 (10k-10M)	1.7 (10k-40M)	0.7 (10k-40M)	0.34 (1k-40M)	0.7 (1k-40M)	**0.168 (1k-40M)**
Area [mm^2]	0.14	0.03	0.028	0.007	0.022	0.09	0.024	**0.06**
Power [mW]	1.49	6.9	3.8	0.78	0.97	5.3	5.3	**15.4**
F_{REF} / $2F_{REF}$ spur [dBc]	-44 / NA	-70.7 / NA	NA / NA	-41 / -51	-57 / NA	-53.5 / -46	-58 / -51	**-42 / -42.6**
FoM1* [dB]	-231.1	-224	-241.3	-236.5	-243.2	-242.1	-241.3	**-243.6**
FoM2 [dB]**	-246.1	-233	-249.5	-244.3	-249.3	-258.1	-256.4	**-258.7**

* $\text{FoM1} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right)\right]$ † Background duty-cycle calibration

** $\text{FoM2} = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right) \cdot \left(\frac{1}{N}\right)\right]$ †† Foreground duty-cycle calibration

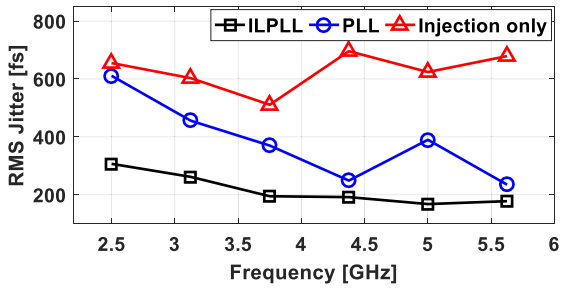


Fig. 25. Measured RMS jitter of different clock frequency.

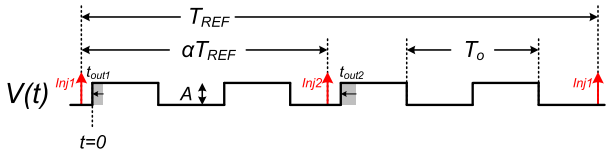


Fig. 26. Time-domain waveform of stable injection-locked clock (e.g., $N = 4$) with dual edge injection.

To verify that the delay mismatch of the ILPLL is insensitive to the supply voltage drift, the $2F_{REF}$ spur and the integrated RMS jitter were measured across the supply voltage variation. Under the condition that the offset cancellation was initially set by the SSBBPD, the $2F_{REF}$ spur and integrated RMS jitter are nearly constant across the supply voltage from 1.17 to 1.3 V as indicated in Fig. 24. Fig. 25 shows the measurement results of the different clock output frequencies by changing the FCW. The integrated RMS jitter of the ILPLL is the lowest including injection alone and PLL alone regardless of the output frequency.

In Table I, the performance of the proposed work is compared with other recently published ILCMs. The proposed work achieves the lowest FoM1 of −243.6 dB, where the FoM1 is defined in [33]. Since ILCMs with small multiplying factor have more injection effects, better performance is shown on FoM1. To consider such injection effect with the multiplying factor, FoM2 includes the multiplying factor for fair comparison. With a FoM2, the proposed work achieves the best performance among the ring oscillator-based ILPLLs in the literature.

V. CONCLUSION

An ILPLL was proposed incorporating a dual-edge complementary switched injection and sub-sampling technique. The effect of an inaccurate injection timing in the ILPLL was analyzed and degradation of the ILPLL performance was calculated in terms of the frequency offset and reference spur. Further, an analysis of the complementary switched injection technique and SSBBPD was presented. With an optimum offset control code in the SSBBPD, the proposed ILPLL generated a wide range of clock frequencies without an additional calibration loop. The proposed ILPLL exhibited a 168-fs integrated jitter and −42 dBc reference spur at 5 GHz ensured robust operation over the voltage and temperature drifts.

APPENDIX
ANALYSIS OF REFERENCE SPUR FOR DUAL-EDGE INJECTION

In this Appendix, from (2)–(7), an analysis of the reference spur is presented when the dual-edge injection is operated on the ILPLL. The calculation is based on the fact that the injection leads to only PM distortion as studied in [34]. Fig. 26 shows the timing waveform of a stable injection-locked clock with dual-edge injection. Assuming that the oscillator works at the frequency of ω_o and the injection clock frequency is ω_{REF} ($\omega_o = N \cdot \omega_{REF} + \Delta\omega$) with duty-cycle of α,

the injection-locked clock is periodic with T_{REF}. Its Fourier series is expressed as

$$V(\mathrm{t}) = a_0 + \sum_{m=-\infty}^{\infty} \left(a_m \cos(m\omega_{REF}t) + b_m \sin(m\omega_{REF}t)\right) \tag{15}$$

where

$$a_0 = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(\mathrm{t})\, dt \tag{16}$$

$$a_m = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(\mathrm{t}) \cdot \cos(m\omega_{REF}t)\, dt \tag{17}$$

$$b_m = \frac{1}{T_{REF}} \int_0^{T_{REF}} V(\mathrm{t}) \cdot \sin(m\omega_{REF}t)\, dt \tag{18}$$

The power of the mth harmonic of the reference can thus be expressed as

$$\begin{aligned} P_m &= a_m^2 + b_m^2 \\ &= \left(\frac{2A}{m\omega_{REF}T_{REF}} \cdot \cos\left(m\omega_{REF}\left(2t_{out2} - NT_o\right)/4\right)\right. \\ &\quad \left. \times \sec(m\omega_{REF}T_o/4) \cdot \sin(mN\omega_{REF}T_o/4)\right)^2 \end{aligned} \tag{19}$$

where A is the amplitude of the clock, T_o is the output frequency of the oscillator, and t_{out2} is the output time shift on the falling edge of the reference clock. Therefore, the spur on n times reference frequency ($n \cdot \mathrm{F_{REF}}$) can be obtained as

$$\mathrm{spur} = 10 \cdot \log_{10}(P_{N\pm n}/P_N). \tag{20}$$

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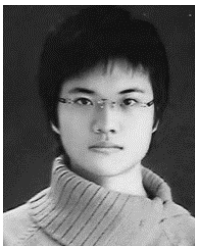

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