A 10-Bit 600-MS/s Time-Interleaved SAR ADC With Interpolation-Based Timing Skew Calibration

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***Abstract*—This brief presents a 10-bit 600 MS/s 4-channel time-interleaved (TI) successive approximation register analog-to-digital converter (ADC). A background calibration algorithm using Lagrange polynomial interpolation is introduced to calibrate timing skew. It consists of digital detection and adaptive derivative-based correction, employing low filter taps and resulting in hardware reduction. Two reference voltage generators are implemented on-chip to provide a stable reference voltage for the sub-ADCs, enhancing the reliability and robustness of the circuits. The TI-ADC prototype is fabricated in the 65-nm CMOS process and occupies an area of 0.69 mm^2. The measurement results show that at a sampling rate of 600 MS/s the ADC achieves a 49-dB SNDR after calibration while dissipating 34 mW from a 1.2/2.5-V supply.**

***Index Terms*—Successive approximation register ADC, time-interleaved (TI), timing skew calibration, finite-impulse response (FIR) filter, reference voltage generator.**

I. Introduction

PORTABLE applications, such as video and image systems, call for medium-to-high resolution, high-speed ADCs while retaining excellent power efficiency. Time-interleaved (TI) technique renders this goal possible by paralleling several ADCs in a consecutive way. Compared to pipeline ADCs, TI-SAR ADCs exhibit a better figure of merit (FoM) [1], [12]. Unfortunately, the TI architecture is strongly impacted by mismatches between sub-ADCs, including offset, gain, and timing mismatches. Among them, timing skew is the most critical limiting factor for TI-ADCs and is challengeable to calibrate. In [4], timing skew is directly removed by a single front-end sampler which operates at the full clock rate. However, huge power consumption and limited linearity performance make this method unfavorable for a 10-bit TI-ADC. Another method that employs a reference channel for calibration is proposed in [5]. With a flash ADC, timing errors can be minimized by a programmable delay line based on least mean square algorithm. Although this mixed-signal solution has no bandwidth limitation, careful analog design should be taken into account to avoid inducing unwanted amount of jitter. Furthermore, another drawback of this method is the increased input capacitance introduced by the reference ADC. All-digital calibration methods potentially avoid this extra jitter problem and take the advantage of the advanced CMOS technology. Fractional delay filters can be employed for correction [3]. The filter coefficients are varied in each calibration cycle, resulting in an increased computation complexity. Furthermore, additional filters are required to reduce the bandwidth penalty.

This brief presents an interpolation-based timing skew calibration technique with low hardware cost and fast convergence speed for TI-ADCs. It employs Lagrange differentiator to extract the derivative of the input signal and then calibrates timing skew adaptively in background. With a low filter tap, the convergence time and power consumption can be greatly reduced. Moreover, on-chip reference voltage generator (RVG) provides a stable reference voltage with high accuracy for the capacitive digital-to-analog converter (CDAC) settling in sub-SAR ADC [2], reducing the gain mismatch and making this brief more practical. A prototype ADC is implemented in 65 nm CMOS to verify the proposed techniques. It achieves a 49 dB SNDR at a sampling rate of 600 MS/s after calibration while consuming 34 mW from a dual supply and occupying an active area of 0.69 mm^2.

The remainder of this brief is organized as follows. Section II presents the digital timing skew calibration scheme and analyses its effective bandwidth and convergence time. Section III introduces the RVG. The measurement results and the conclusion are included in Section IV and Section V, respectively.

II. Interpolation-Based Timing Skew Calibration

Fig. 1 shows the 4-channel TI-ADC architecture. Offset and gain mismatch are calibrated by averaging function [10]. Timing skew calibration is then adopted using the proposed technique. The calibration process for timing skew can be divided into 2 steps. First, Channel 1 is viewed as the reference and its outputs are employed to detect the timing error of channel 3. And then, when channel 3 is calibrated, its outputs together with the outputs of channel 1 are used to detect the timing error of channel 2 and 4.

A. Digital Calibration Algorithm for Timing Skew

Fig. 2 shows the output sequence of the TI-ADC, in which channel 3 encounters timing skew and the others with ideal sample. As timing skew is relatively small compared to the sampling interval, a first-order approximation can be adopted for compensation, and then the updated code is given by

$$\hat{y}_i[k] = y_i[k] - \Delta y_i[k] = y_i[k] - \Delta T_i \frac{dy}{dt} \tag{1}$$

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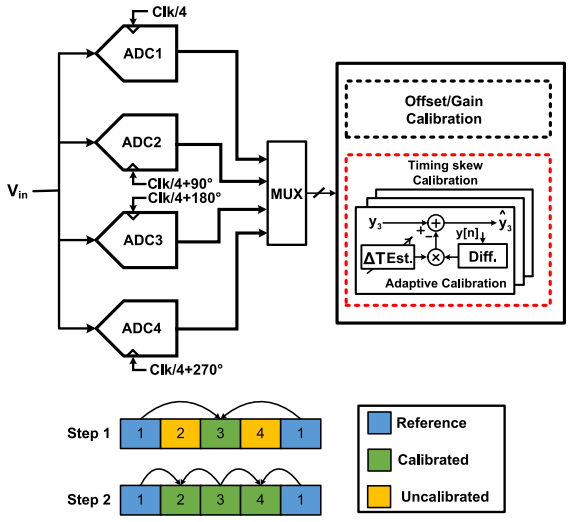

Fig. 1. Calibration methods for the TI-ADC.

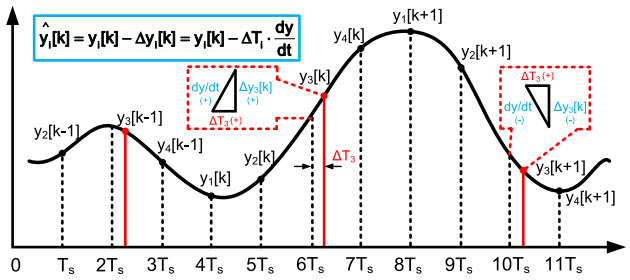

Fig. 2. First-order timing skew calibration.

where the index i represents the channel number ($i = 1, 2, 3,$ and 4), and ΔT_i is the estimated timing skew and can be updated in each calibration cycle. Using a digital detector and corrector, a negative feedback system can be formed in background and the impact of timing skew is gradually minimized.

The autocorrelation function (D_i), which uses the output difference between two adjacent channels, is adopted to evaluate ΔT_i. Only the implementation for channel 3 is illustrated in Fig. 3 for simplicity. The calculation for D_3 is given as

$$D_3 = E[|y_1[k+1] - y_3[k]| - |y_3[k] - y_1[k]|] \tag{2}$$

It can be proven that D_i is proportional to ΔT_i [7]. Channel 3 is calibrated first. Then, y_1, y_2, and y_3 are used to detect ΔT_2. Meanwhile, y_2, y_3, and y_4 are used to detect ΔT_4. Viewing channel 1 as the reference, no calibration is applied to this channel. In this algorithm, we only care about the polarity of D_i instead of its exact value. In practice, the value of D_i reveals small variations rather than zero even when there is no timing skew in i-th channel because of the finite number of samples. Therefore, a positive constant (N_c) close to zero is applied to compare with D_i. Only when $|D_i| \leq N_c$, the calibration loop stops and maintains the estimated ΔT_i, otherwise, ΔT_i would increase/decrease relying on D_i. We note that a proper value of N_c is important to the calibration loop. If N_c is too large, the estimated value of ΔT_i is not accurate. If N_c is too small, the convergence time is relatively large. In this brief, through simulation, N_c is set as 0.5 to make a good trade-off.

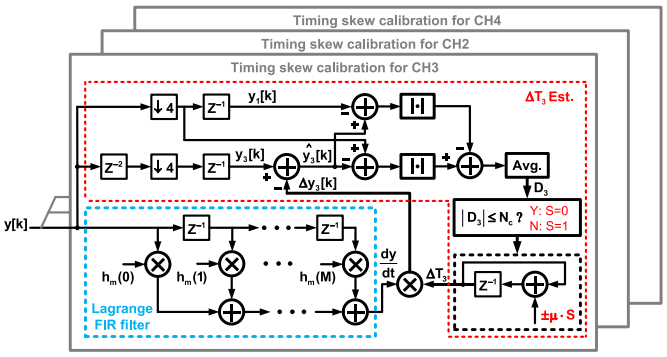

Fig. 3. Timing skew calibration block diagram.

As shown in (1), the remaining challenge is to design a first-order differentiator. Assume the expression of an M-order Lagrange polynomial is

$$Lp(\mathrm{t}) = \sum_{i=0}^{M} C_i t^i \tag{3}$$

We use (3) to fit the output sequence y[k] and then calculate the derivative of the Lagrange polynomial to substitute the derivative of the input signal. By normalizing T_s, M+1 equations are acquired and can be expressed in matrix form

$$(C_0 \;\; C_1 \;\; \cdots \;\; C_M)\,\mathbf{V} = (y[1] \;\; y[2] \;\; \cdots \;\; y[M+1]) \tag{4}$$

where

$$\mathbf{V} = \begin{pmatrix} 1 & 1 & 1 & \cdots & 1 \\ 0 & 1 & 2 & \cdots & M \\ 0 & 1 & 2^2 & \cdots & M^2 \\ \vdots & & & \ddots & \vdots \\ 0 & 1 & 2^M & \cdots & M^M \end{pmatrix} \tag{5}$$

$\mathbf{V}$ is an L×L Vandermonde matrix and L=M+1. The derivative of Lp(t) is

$$\frac{dLp}{dt} = \sum_{i=1}^{M} i C_i t^{i-1} \tag{6}$$

In order to calculate the elements of C_i, we define the inverse matrix of Vandermonde matrix as

$$\mathbf{Z} = \begin{pmatrix} z_{11} & z_{12} & \cdots & z_{1L} \\ z_{21} & z_{22} & \cdots & z_{2L} \\ \vdots & \vdots & \ddots & \vdots \\ z_{L1} & z_{L2} & \cdots & z_{LL} \end{pmatrix} \tag{7}$$

The elements in (7) can be easily acquired in MATLAB and used to further calculate the impulse response of sub-FIR filter, which is given as

$$h_m(i) = \mathbf{Q}_i \mathbf{R}_m \tag{8}$$

$$\mathbf{Q}_i = \begin{pmatrix} z_{i2} & z_{i3} & \cdots & z_{iL} \end{pmatrix} \tag{8.a}$$

$$\mathbf{R}_m = \begin{pmatrix} 1 & 2m & \cdots & Mm^{M-1} \end{pmatrix}^{\mathrm{T}} \tag{8.b}$$

For a given order length (M) and interpolation vector (m), the coefficients in each sub-FIR filter are fixed.

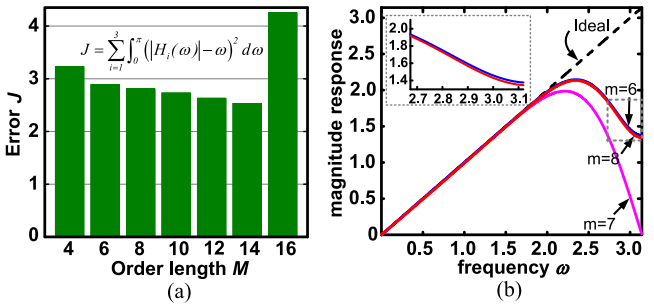

Fig. 4. (a) Relationship between filter order length and error function. (b) Magnitude response of the first-order Lagrange differentiator (M=14).

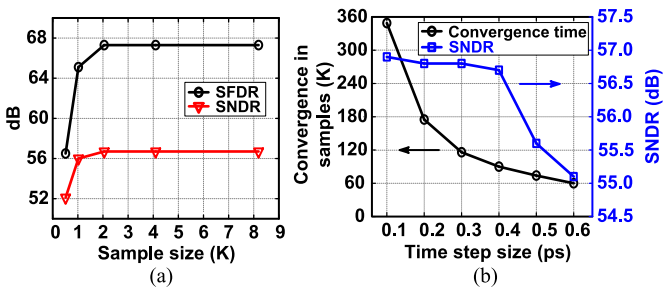

Fig. 5. (a) SNDR and SFDR variations versus the sample size. (b) Simulated convergence time and SNDR at different time step.

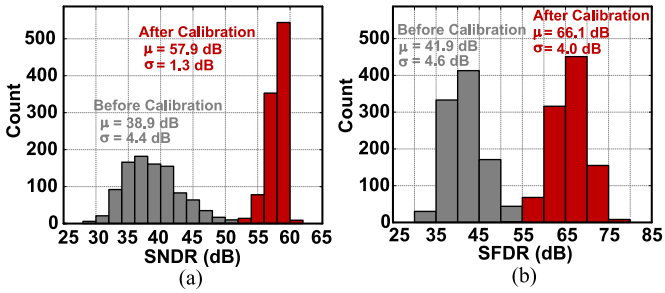

Fig. 6. Histograms of (a) SNDR and (b) SFDR before and after calibration.

B. Error Analysis of the Lagrange Differentiator

The performance of the proposed calibration method primarily hinges upon that of the differentiator. Therefore, it is necessary to analyze the effectiveness of the Lagrange differentiator. The frequency response of the ideal first-order differentiator is expressed as [8]

$$H_{id}(\omega) = j\omega \tag{9}$$

To find the optimal performance of the Lagrange differentiator, an error function is defined by

$$J = \sum_{i=1}^{3} \int_0^{\pi} (|H_i(\omega)| - \omega)^2 d\omega \tag{10}$$

where $H_i(\omega)$ is the transfer function of the i-th filter, whose impulse response is shown as (8). As three channels are set to be calibrated, the error function is the sum of these errors and defines as the total deviations to the ideal transfer function in the first Nyquist zone. Fig. 4 (a) compares the error function J for various order length (M) of the sub-FIR filter. Clearly, when M=14, the designed Lagrange differentiator exhibits the lowest error. Oscillation would occur with M>14, known as the Runge phenomenon, resulting in a sharp increase of J. Fig. 4 (b) shows the magnitude responses of the designed Lagrange differentiators in the first Nyquist zone with M=14, where m=6, 7, and 8 are for channel 2, 3, and 4 respectively. Note that the response of m=6 is nearly the same with m=8 in all frequency scope due to symmetry. In low frequency scope, all Lagrange responses fit the ideal one perfect. However, when $\omega > 2.8$, J would be large enough so that the proposed calibration method would be invalid. Such bandwidth limitation is a common issue in all of the derivative-based calibration methods [8]–[10].

One possible way to deal with this problem is to use complicated IIR filters which may exhibit better performance in high frequency. But design IIR filters have the potential stabilization issues. A more practical way is to slightly improve the sampling frequency of the TI-ADC for some applications. By doing this, the bandwidth will cover the desired input frequency.

C. Characteristics of the Calibration Method

As the convergence time of the proposed calibration method mainly depends on two factors, i.e., sample size used in each calibration cycle and the length of time step (defined as μ in Fig. 3). With larger sample size, the value of D_i reveals smaller variation while results in slower convergence. For a smaller value of μ, the time accumulator in Fig. 3 could achieve better accuracy while sacrifices the convergence speed. There exist an optimized sample size and μ.

A behavioral model of a 4-channel 600-MS/s TI-ADC based on the proposed timing skew calibration is designed in MATLAB to find the proper sample size and μ. In this simulation, it is assumed that there are no offset and gain mismatches among channels. The standard deviation of timing skew is set as $0.01T_s$, and the input frequency is 200 MHz. Fig. 5 (a) shows the sample size versus the SNDR and SFDR after calibration. When the sample size is larger than 2048, the SNDR and SFDR will no longer increase. Therefore, the sample size is chosen as 2048. The simulated time step size versus convergence time and SNDR is shown in Fig. 5 (b). It suggests the optimal value of μ is around 0.4 ps, where the SNDR is larger than 56.5 dB and the convergence time is also small. Fig. 6 shows the histograms for SNDR and SFDR of 1000 Monte-Carlo simulations, where the timing skews are independent and identically distributed Gaussian random variables with zero mean and standard deviation of $0.01T_s$. On average, the improvement of SNDR and SFDR are 19 dB and 24.2 dB, respectively. In the worst case, the SNDR improves from 28.4 dB to 49.6 dB and the SFDR improves from 30.4 dB to 52.3 dB, respectively. In this method, the tolerance of ΔT is $0.1T_s$. We note that the 1-sigma values of SNDR and SFDR are proportional to timing skews, implying that the residue errors are large when timing skews are relatively large. High order compensation is needed to reduce the distributions of SNDR and SFDR. Fig. 7 shows the output spectrum before and after calibration for a multitone input signal. All interleaving spurs are suppressed below −67 dBFS after calibration. The comparisons to other existing methods are shown in Table I. The variance-based algorithm in [5] needs a large number of samples for measuring the power of the errors, resulting in slow convergence. In [9], a least-squares based method is performed for estimating the timing skews and derivative filters

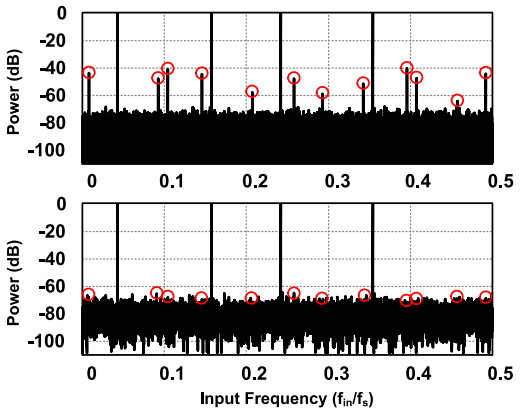

Fig. 7. Output spectrum before and after calibration for a multitone input.

TABLE I
COMPARISON WITH OTHER TIMING SKEW CALIBRATION

	Method	Bandwidth	Convergence	Filter taps
[5]	Mixed	0-0.5 f_s	128K	/
[9]	Digital	0-0.3 f_s	32K	60
[3]	Digital	0-0.45 f_s	100K	82
[6]	Digital	0-0.47 f_s	/	43
This work	Digital	0-0.44 f_s	80K	15

are employed for correcting. The total filter taps in estimation and correction are 60, leading to a large amount of power. In a similar 4-channel system, [3] and [6] use 82-tap and 43-tap fractional delay filters for correction, respectively. The filter tap in the proposed algorithm has the minimal value, meaning low complexity and low power.

III. REFERENCE VOLTAGE GENERATOR

On-chip RVG could reduce the area of decoupling capacitors and reduce the gain mismatch. In this brief, with two high-speed RVGs, four reference voltages are generated for channel pairs 1, 2 and 3, 4, respectively. Fig. 8 shows the open loop followers architecture. The potential of V_{ref} is

$$V_{\text{ref}} = I_1 \cdot R_3 = \frac{mR_3}{R_2} \cdot V_{BG} \tag{11}$$

where m is the ratio of I_1/I_0. It can be seen from (11) that the potential of V_{ref} is process and temperature insensitive, as it tracks the bandgap voltage V_{BG}. The simulated V_{ref} has a maximum variation of 0.7 % in worst case corner over the temperature from −25 °C to 110 °C. Note that the RVG DC offset can be calibrated with a digital equalization solution.

IV. MEASUREMENT RESULTS

The proposed TI-ADC prototype is manufactured in a 1P9M 65 nm CMOS process and occupies an active area of 0.69 mm^2, as shown in Fig. 9. It is crucial to make the layout as compact and symmetric as possible so as to minimize the layout parasitics. The clock generator is located at the center to achieve identical clock path to each channel. Analog input signal arrives from top of the chip and distributes as an H-tree structure. The RVGs are separately placed beside the clock generator. The total power consumption of the proposed TI-ADC, excluding the I/O pads, is 34 mW at 1.2/2.5 V supply.

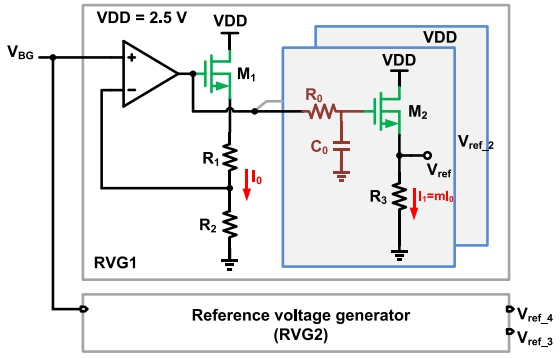

Fig. 8. Schematic of the RVG.

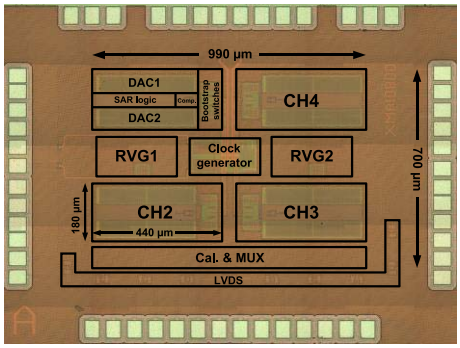

Fig. 9. Die micrograph.

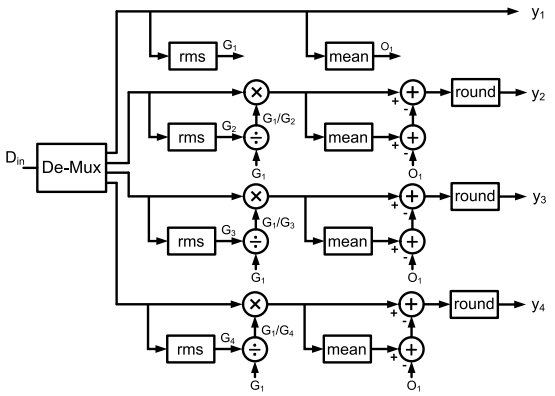

Fig. 10. Gain and offset mismatches calibration.

In the 1.2 V domain, clock generator, 4 channel SAR ADCs, digital circuits and MUX consume 7.9 mW. With 2.5 V supply, the power consumption of RVGs is 26.1 mW.

The dynamic performance of the ADC was measured using single tone testing. Fig. 10 shows the equalization method for gain mismatch and offset mismatch. Note that gain correction should be performed before offset correction since the multiplication would result in the mean value variation, thus introducing new offset mismatch between channels. Fig. 11 shows the measured fast Fourier transform (FFT) spectrums of the TI-ADC with a 2.1 V_{pp}, 100 MHz input signal at 600 MS/s. After gain and offset correction, the SFDR and SNDR of the TI-ADC are improved to 42.2 dB and 39.9 dB, respectively. Thus, it can be seen that the timing skew induced spurs still limit the performance. Then the proposed timing skew calibration is applied and the SFDR and SNDR are

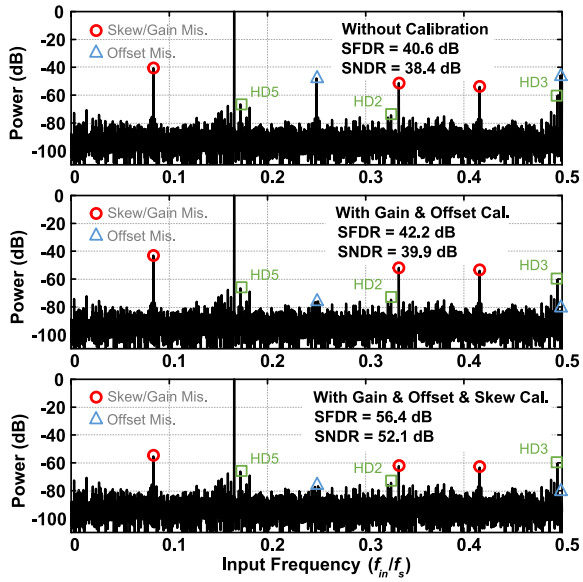

Fig. 11. Measured output spectrum before and after calibration.

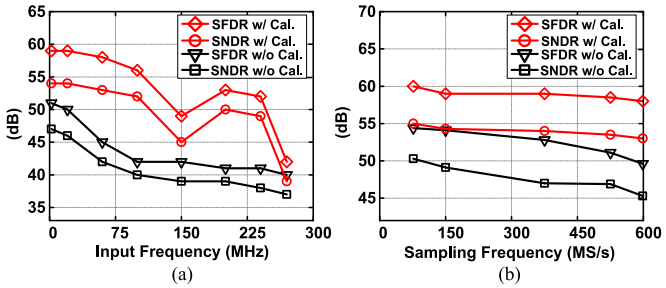

Fig. 12. SNDR and SFDR vs (a) input frequency and (b) sampling frequency.

improved to 56.4 dB and 52.1 dB, respectively. The timing skew calibration is controlled by MATLAB on a PC and is feasible to be realized by digital circuits through Verilog-HDL. The estimated power of the timing skew calibration is 6 mW with gate count of 21 K in 65 nm CMOS. After approximately 1×10^5 samples, the adaptive calibration for channel 3, 2, and 4 are complete. The 3rd and 5th harmonic tones are around -60 dB, which are suspected due to the bandwidth limitation of the sampling switches and can be reduced by increasing the supply voltage.

Fig. 12 plots the measured SNDR and SFDR for various input frequencies at 600 MS/s and for various sampling frequencies with a 10 MHz input, respectively. When input frequency is at 150 MHz, the detection for ΔT_3 would be invalid. This is because no matter how large ΔT_3 is, D_3 equals to 0 at this frequency, namely the singularity [7]. When input frequency beyond 260 MHz, this algorithm will be invalid since the correction module is unable to compensate the error codes. It means the effective range of the proposed algorithm is within (0-0.43 f_s) and confirms the conclusion drawn in Section II-B. The ADC achieves a peak SNDR of 55 dB at 10 MHz input with 600 MS/s sampling rate after calibration. Table II compares the performance of previously reported TI-ADCs with this brief. It is shown that the proposed ADC is comparable to the state-of-the-art in 65 nm technology.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED ADCS

Reference	[10]	[5]	[11]	This work	
Architecture	TI-SAR	TI-SAR	TI-SAR	TI-SAR	
Technology (nm)	40	65	45	65	
Resolution (bit)	9	10	10	10	
f_s (MS/s)	1620	1000	800	600	
Supply voltage (V)	1.1/1.7	1.0	1.1	1.2/2.5	
Power (mW)	93[(1)]	18.9	9.8	7.9	40[(1)]
SNDR (dB)	48	51.4	48	49	
DNL/INL (LSB)	N/A	±1.0	0.7/1.5	0.39/0.94	
Area (mm^2)	0.83	0.78	0.15	0.69	
Skew calibration method	Derivative	Variance	Variance	Derivative	
FoM (fJ/conv. step)	283	62.3	59	57	289

[(1)] Including RVG and digital calibration.

V. CONCLUSION

A 10-bit 600 MS/s four-channel TI-SAR ADC in 65 nm CMOS has been presented. An interpolation-based digital calibration method with low cost and fast convergence speed for timing skew is presented. The FIR filter tap to calibrate one channel is 15, which is lower than prior derivative-based schemes. On-chip reference voltage generators enhance the robustness of this brief. The prototype occupies an active area of 0.69 mm^2 and consumes 34 mW power from the 1.2/2.5 V supply. The Walden FoM of the TI-ADC is 246 fJ/conv. step. The proposed calibration technique is extendable to a larger number of channels.

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