A 56Gb/s PAM4 Wireline Transceiver using a 32-way Time-Interleaved SAR ADC in 16nm FinFET

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Abstract— **A 56Gb/s PAM4 wireline transceiver testchip is implemented in 16nm FinFET. The CML transmitter incorporates an auxiliary current injection at the output nodes to maintain PAM4 amplitude linearity. The receiver consists of continuous-time linear equalizers with constant DC-gain and a 28GSa/s 32-way time-interleaved SAR ADC. The transceiver achieves 1e-8 BER over a backplane channel with 25dB loss at 14GHz while consuming 550mW power, excluding DSP.**

In order to meet increasing bandwidth demand, a new 56Gb/s electrical interface standard was recently proposed [1]. The interface must support legacy channels (i.e., backplane) that were initially designed for NRZ signaling only up to 28Gb/s. These legacy channels often have a very large insertion loss beyond 14GHz with significant reflections. PAM-4 signaling is chosen in order to limit the frequency content of the signal below 14GHz. ADC [3][4] is used in the receiver so that Digital Signal Processing (DSP) can be applied to correct for inter-symbol-interference from these legacy channels. Since a Forward Error Correction (FEC) mechanism is employed in the system, the target BER for this interface is not very stringent (e.g., BER < 1e-4 is currently proposed as standard [1]).

The PAM4 transmitter front-end (Figure 1a) is realized by the current summing of 2X driver (MSB) and 1X driver (LSB). The transmitter must maintain linearity between the four output levels while delivering >1V diff-pp swing. This is achieved by injecting current from an auxiliary supply (1.8V) to the outputs to raise its common mode, and by placing a small cascode device above the tail current source to increase the output impedance, which further improve DC linearity and reduce AC distortion. Open-loop compensation using a replica of driver input differential pair helps maintain optimum output common-mode over PVT. A combined 4-to-2-MUX/pre-driver circuit (Figure 1b) incorporates a pseudo H-bridge scheme with positive feedback. This consumes less power than a conventional CML circuit. The circuit has a high gain at zero crossing, which help suppress clock switching noise at the driver output.

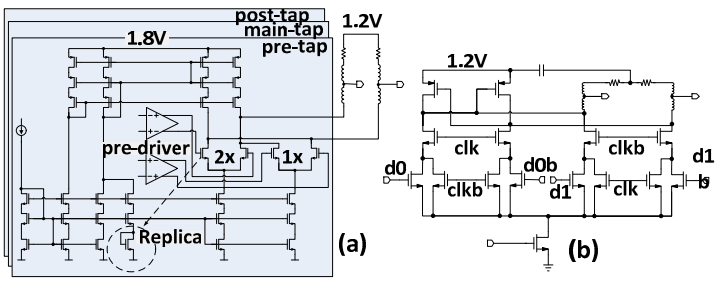

Figure 1: TX Front-End (a) and 4-to-2-MUX/Pre-driver (b)

Figure 2 shows the receiver block diagram. The analog front-end (4 stages of CTLE and AGC) provides signal equalization and conditioning which reduces the resolution and full-scale-range requirement of the ADC [2]. The 28GSa/s ADC converts the differential analog input into 8-bit digital values. The ADC outputs are sampled periodically and stored in a 64Kb (8K symbols) storage. An off-chip FPGA is used to take these 8K symbols, performs DSP, and generates equalized symbols. The DSP inside the FPGA consists of 24-tap FFE and 1-tap DFE. The FPGA also performs equalization, adaptation, clock recovery (CDR), and ADC offset/gain/skew calibrations based on sampled ADC outputs.

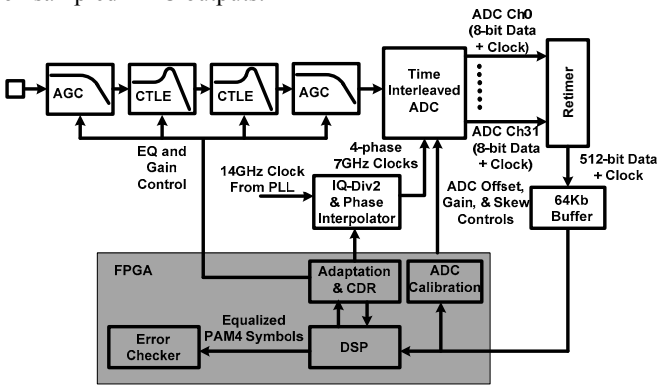

Figure 2: Receiver Block Diagram

The CTLE (Figure 3) is designed to have a constant-DC gain (~0dB) and programmable high-frequency peaking while the AGC has a 10dB programmable DC gain range. Compared to a constant high-frequency gain CTLE (with programmable DC gain), the constant-DC gain CTLE can either reduce the required AGC's gain at high-loss channels and/or improve the linearity of subsequent stage at low-loss channels. Furthermore, this approach minimizes interaction between AGC adaptation loop and CTLE adaptation loop.

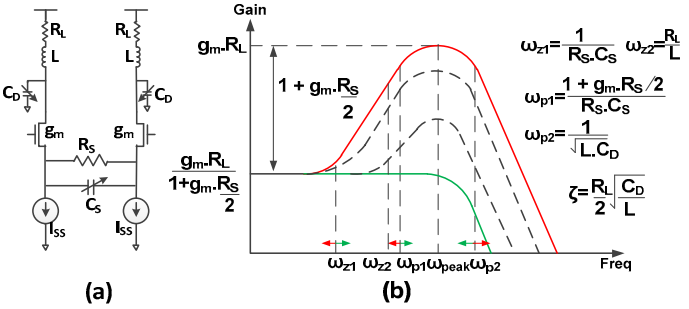

Figure 3: CTLE Circuit

Figure 4a shows the 8-bit 28GSa/s, 600mV diff-pp full-scale range, 32-way time-interleaved SAR ADC used in the receiver. There are two stages of time-interleaving. The first stage is a 4-

way time-interleaver, where the input is sampled and held using four-phase, non-overlapping 7GHz clocks. The second stage is an 8-way time-interleaver, where each of the signals sampled by the 7GHz clocks are further sampled and held using 8-phase 875MHz clocks and converted to digital values using 8 instances of 875MHz SAR ADC. The output of the 32 instances of SAR ADCs are then re-timed to a single 875MHz clock domain and sent to a 64Kb storage. Figure 4b shows the ADC clocking timing diagram. The timing skew calibration of the 7GHz clocks and the gain/offset calibration of the 875MHz ADC instances are performed using pseudo-random data input, in contrast to the use of sinusoidal tones for calibration in [3]. Our approach allows live data calibration where scrambled pseudo-random data is common in most high-speed electrical interfaces.

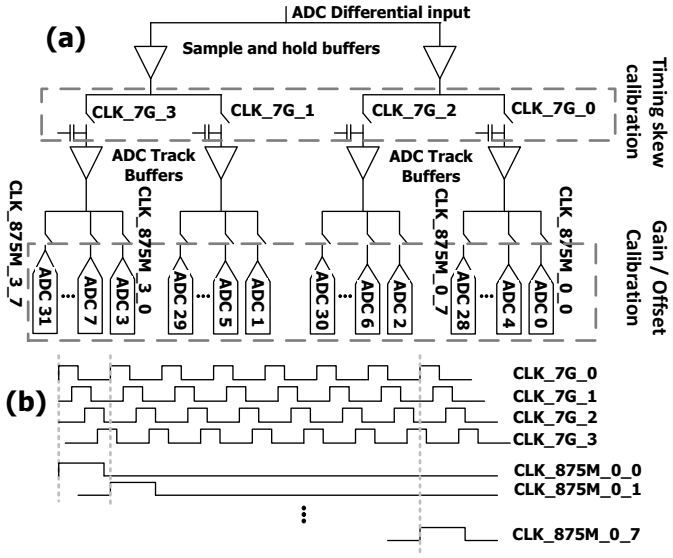

Figure 4: 28GSa/s Time-Interleaved SAR ADC (a) and Clock Timing Diagram (b)

Two TX/RX lanes with common PLL, clock distribution, and bias block is fabricated (Figure 5) in 16nm FinFET. In order to perform direct measurements of the ADC performance, the CTLE in the second RX lane is bypassed.

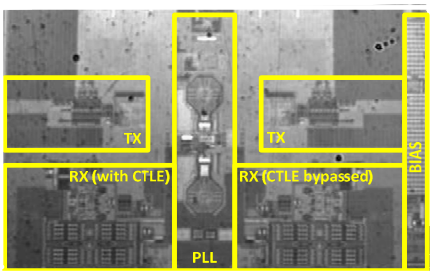

Figure 5: Die Photo

Figure 6 shows the transmitter output eye diagram over ~5dB channel. The transmitter is configured to transmit PRBS7 pattern with ~4.5dB post-tap equalization. The average of the four output levels show good linearity. The ADC performance is measured by feeding sinusoidal inputs at various frequencies, capturing the ADC output using 64Kb storage, and performing FFT. The ADC achieves ENOB of 6.3 at 180HMz and 4.9 at 14GHz, as illustrated in Figure 7.

The link performance is tested by connecting the transmitter output to the receiver over backplane channels. Figure 8 shows eye diagrams at the CTLE/AGC outputs (captured using the ADC as real-time digital oscilloscope) and the post-DSP histograms of the four PAM4 levels (sampled at the CDR lock point) over 200K symbols. The CTLE/AGC outputs show open eye with ~6dB channel (Figure 8a) and closed eye with 25dB channel (8b). In both cases, the DSP open the eye in the post-DSP PAM4-level histograms. The estimated BER is around 10^{-8} based on extrapolation of the histograms.

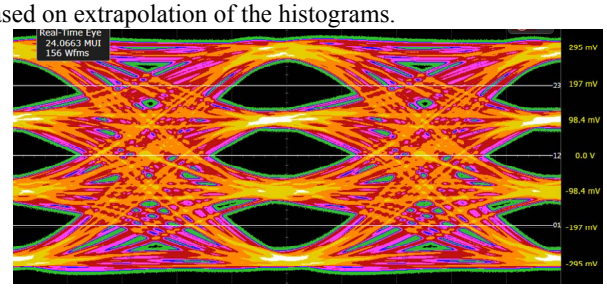

Figure 6: Transmitter PRBS7 Output Eye Diagram

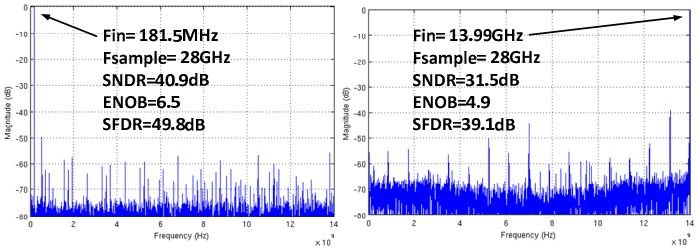

Figure 7: ADC Performance

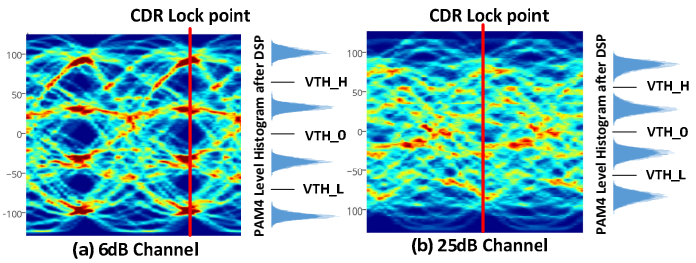

Figure 8: Eye diagram at ADC output and post-DSP PAM4 level for ~6dB channel (a) and 25dB channel (b)

Technology	CMOS 16nm FinFET
Power Supply (V_{avcc}, V_{avtt}, V_{aux})	0.9V, 1.2V, 1.8V
Dual Transceiver Active Area	2.8mm^2
Max TX Swing	1.2V diff-pp
TX RJ (PRBS7, Major Transition)	200fs
ADC ENOB	6.5@0.18GHz, 4.9@14GHz
ADC Power (including ADC clocks)	280mW
BER at 56Gb/s	~1x10^{-8}
Power per lane at 56Gb/s (Does not include DSP)	550mW (140mW TX, 370mW RX, 40mW PLL/Clock Distribution)

Table 1. Performance Summary

Acknowledgments

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References

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