A 12-bit 40 nm DAC Achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s With DEMDRZ Technique

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***Abstract*—For current-steering digital-to-analog converters (DACs), a technique utilizing dynamic-element-matching and digital return-to-zero, called DEMDRZ, is proposed to simultaneously suppress the mismatch- and transient-induced nonlinearity. In doing so, the usage of small-sized current sources and switches is possible, and the spurious-free dynamic range (SFDR) and intermodulation distortion (IMD) for high signal frequencies can be improved. With the DEMDRZ technique, a 12-bit compact, low-power, high-speed, high-resolution DAC is implemented in TSMC 40 nm CMOS process. The DAC architecture, circuit, and layout designs are presented. The implemented DAC achieves > 70 dB SFDR for signals over the 800 MHz Nyquist bandwidth at 1.6 GS/s and < –61 dB IMD for signals over the 1.4 GHz Nyquist bandwidth at 2.8 GS/s. Further, it dissipates 40 mW with a single 1.2 V supply. The active area of the DAC is 0.016 mm², which is less than 6% of other state-of-the-art 12-bit current steering DACs. Furthermore, the implemented DAC performs best with three common figure-of-merits (FoMs).**

***Index Terms*—Compact size, current-steering, DAC, DEM, digital return-to-zero, digital-to-analog converter, DRZ, dynamic element matching, figure-of-merit, FoM, high-resolution, high-speed, IMD, intermodulation distortion, mismatch insensitivity, return-to-zero, RTZ, SFDR, spurious-free dynamic range.**

I. Introduction

CURRENT-STEERING digital-to-analog converters (DACs) are commonly used in wideband applications, e.g., signal generation and multi-carrier communication systems. A critical challenge for DAC design is to realize a high spurious-free dynamic range (SFDR) or low intermodulation distortion (IMD) for wideband applications. To overcome this challenge, three primary problems must be solved, namely, the parasitic capacitance-induced finite output impedance, current-source mismatch-, and transient-induced nonlinearity.

For the first problem, the parasitic capacitance of current sources lowers the high-frequency output impedance, and thereby deteriorates the signal bandwidth of DACs [1], [2]. Current sources with cascoded transistors are commonly used to increase the output impedance [1], [2]; however, the parasitic capacitance due to large transistors used for lower mismatch still limits the high-frequency output impedance. In this work, by reducing the mismatch effect, the current sources, including the cascode transistors, are designed to be as small as possible to reduce the parasitic capacitance and increase the high-frequency output impedance.

The second problem is the nonlinearity stemming from the mismatch of current sources with small transistors [3], [4]. To enable the use of small transistors, several methods have been proposed to prevent the current-source mismatch effect from deteriorating the performance, such as calibration circuits to directly compensate the mismatch error [3], [5], and dynamic-element-matching (DEM) techniques [6]–[9] to randomize the selection of current sources to reduce mismatch effects. Among the above methods, a good DEM technique requires less circuit overhead and complexity, and thus can be effectively used to reduce the mismatch effect and transistor size. By using a DEM technique, the chip area can be smaller, allowing for shorter wires and smaller parasitic capacitance, thereby widening the signal bandwidth and shortening the wires for reducing timing skew.

The third problem is the transient-induced nonlinearity occurring during the DAC's output transition. Fig. 1(a) shows the DAC's output transition with non-return-to-zero (NRZ), where the output transition is strongly dependent on the previous signal, which causes the transient-induced nonlinearity. To reduce this nonlinearity, various return-to-zero (RTZ) methods have been proposed. Fig. 1(b) shows the DAC's output transition with RTZ methods, in which the RTZ methods insert a zero differential output between two adjacent signals to allow the output transition to be independent of the previous signal. Consequently, the RTZ methods reduce the transient-induced nonlinearity. The RTZ methods can be categorized into analog RTZ (ARZ) and digital RTZ (DRZ). ARZ can be realized with large reset transistors added at the DAC output terminals [10], while DRZ can be realized with mid-code insertion [11]. Unlike ARZ, DRZ does not require any reset transistors; hence, there is less parasitic capacitance, cost and power consumption. However the DRZ performance is limited by code dependent switching transients, which can be solved with the technique proposed in this work.

In this paper, a technique that utilizes DEM and DRZ, termed DEMDRZ, is proposed to simultaneously suppress the current-source mismatch- and transient-induced nonlinearity of the implemented DAC to achieve high SFDR and low IMD with a

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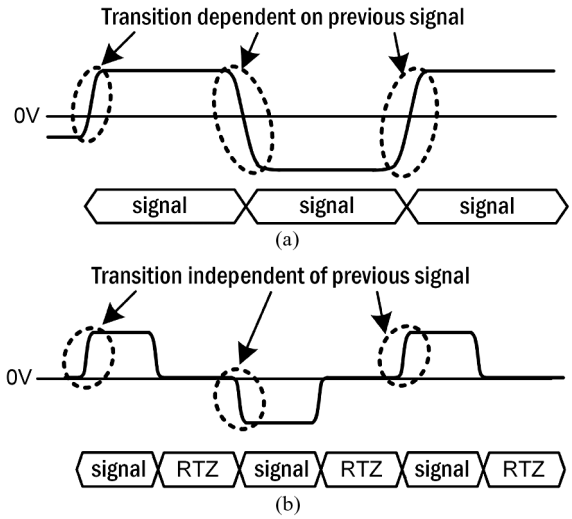

Fig. 1. DAC output transition with (a) NRZ and (b) RTZ.

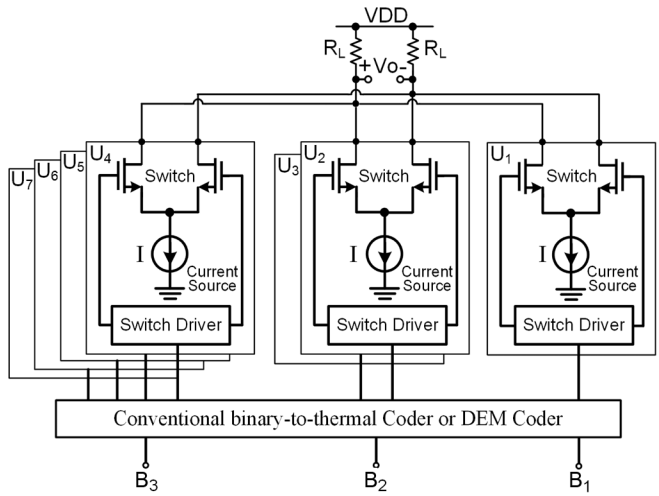

Fig. 2. Three-bit binary-weighted DAC with either a conventional binary-to-thermal coder or a DEM coder.

small chip area. Section II of this paper presents the architecture and operational principle of the DAC with DEMDRZ, while Section III presents the circuit design and implementation. Measurement results and comparisons are given in Section IV, and a conclusion is offered in Section V.

II. Operational Principle of the DEMDRZ

Fig. 2 shows a 3-bit binary-weighted DAC with seven unit elements $(\mathrm{U}_7, \mathrm{U}_6, \ldots, \mathrm{U}_1)$. With a conventional binary-to-thermal coder, the input code B_3, B_2 and B_1 control $\mathrm{U}_7\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4$, $\mathrm{U}_3\mathrm{U}_2$ and U_1, respectively. In order to reduce the size of the DAC, small transistors need to be used for both the current sources and the switches. In this paper, the DEM technique in [7] is adopted to reduce the nonlinearity effects due to the mismatch of small transistors. Thus, a DEM coder, which contains a rotator and a pseudo-random number generator with 16 bit length, is used to replace the conventional binary-to-thermal coder to realize the DEM technique. Fig. 3(a) shows the operation of the DEM technique with three input codes, 110, 001 and 110, where the R represents a random rotation step ranging from 0 to 6. For the first signal phase with R equal to 0, B_3, B_2 and B_1 control $\mathrm{U}_7\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4$, $\mathrm{U}_3\mathrm{U}_2$ and U_1, respectively. For the second signal phase with R equal to 6, B_3, B_2 and B_1 are rotated 6 steps counterclockwise, with respect to the conventional operation, to control $\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4\mathrm{U}_3$, $\mathrm{U}_2\mathrm{U}_1$ and U_7, respectively. For the third signal phase with R equal to 2, B_3, B_2 and B_1 are rotated 2 steps counterclockwise, with respect to the conventional operation, to control $\mathrm{U}_2\mathrm{U}_1\mathrm{U}_7\mathrm{U}_6$, $\mathrm{U}_5\mathrm{U}_4$ and U_3, respectively. In brief, the controlled unit elements are randomized by the random number R to suppress mismatch-induced distortions.

Additionally, RTZ is used to solve the transient-induced nonlinearity between DAC output transitions. For RTZ circuit implementation, according to the rationale stated in Section I, DRZ is used in this paper. Fig. 3(b) shows the DRZ operation, which is similar to the operation of conventional DACs except that the DRZ phases are inserted. During the DRZ phases, the 100 code is inputted and connects the elements $\mathrm{U}_7\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4$ to one output terminal and the remaining elements $\mathrm{U}_3\mathrm{U}_2\mathrm{U}_1$ to the other terminal, respectively, resulting in a differential output voltage equal to the LSB weight, which is near zero. During the DRZ phase, an extra element U_0 can be added to $\mathrm{U}_3\mathrm{U}_2\mathrm{U}_1$ to obtain zero differential output. Without the extra element, the nonzero output effect is negligible in a high-resolution DAC since the weight of the least-significant bit is small. However, the DRZ has the shortcoming of code dependent switching transient, which is also demonstrated in Fig. 3(b). As can be seen, for the input code 110, the switched current cells are always $\mathrm{U}_3\mathrm{U}_2$. In other words, the switching transient induced glitches are correlated with the input codes, and thus its corresponding output levels. This correlation induces distortion tones that degrade the SFDR and IMD of a DAC. The proposed DEMDRZ technique can be used to overcome this problem.

The operation of the DEMDRZ is shown in Fig. 3(c), where the unit selection with randomization is demonstrated using the same input as the DRZ in Fig. 3(b). In addition, during the DRZ phase of DEMDRZ operation, the DEM is disabled by setting R to 0. For the first input 110 with R equal to 0, during the signal phase, the selected current cells are $\mathrm{U}_7\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4$ and $\mathrm{U}_3\mathrm{U}_2$. Then, the code 100 is inputted during the DRZ phase. Hence, $\mathrm{U}_3\mathrm{U}_2$ are switched while the signal phase is changed to the DRZ phase. For the second input 001 with R equal to 6, U_7 is selected during the signal phase, and then $\mathrm{U}_6\mathrm{U}_5\mathrm{U}_4$ are switched during the DRZ phase. Similarly, the third input 110 is the same as the first one, with the exception that the random number R equals 2 in this example. The selected elements are $\mathrm{U}_2\mathrm{U}_1\mathrm{U}_7\mathrm{U}_6$ and $\mathrm{U}_5\mathrm{U}_4$, with $\mathrm{U}_2\mathrm{U}_1$ switched during the DRZ phase. This results in different switched unit elements for the same input code with different values of R. Fig. 4 shows a comparison of NRZ, DRZ [11], and the proposed DEMDRZ with the same input as in Fig. 3. As can be seen, the NRZ suffers from transient-induced nonlinearity caused by output transitions. Although the DRZ provides DRZ phases to reduce NRZ nonlinearity, the code dependent switching transient of DRZ still induces non-negligible distortion. With the proposed DEMDRZ, the code-dependent distortion is randomized by the random number R, which

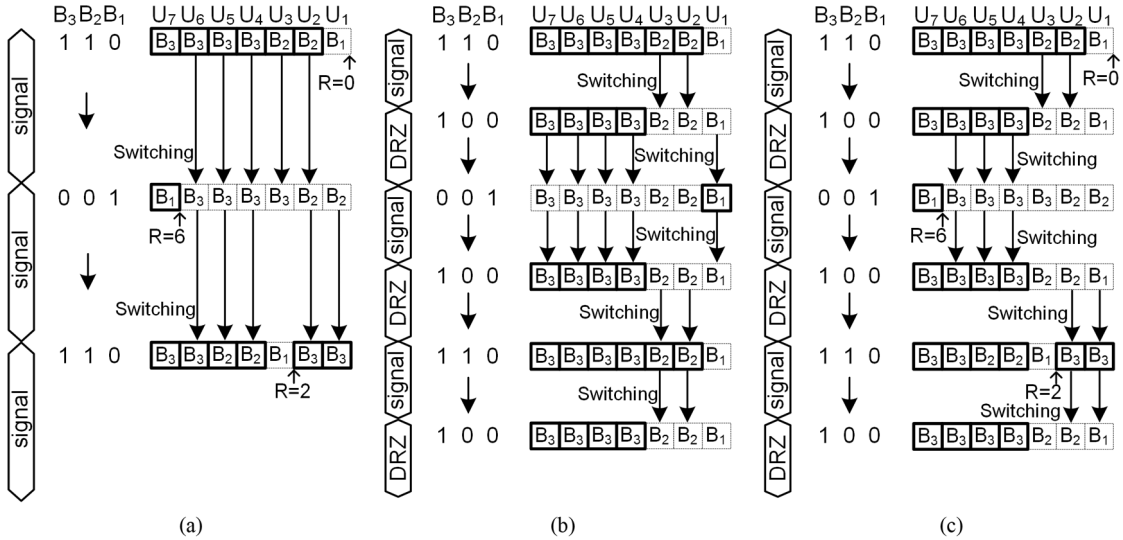

Fig. 3. Operation of (a) DEM (b) DRZ, and (c) DEMDRZ.

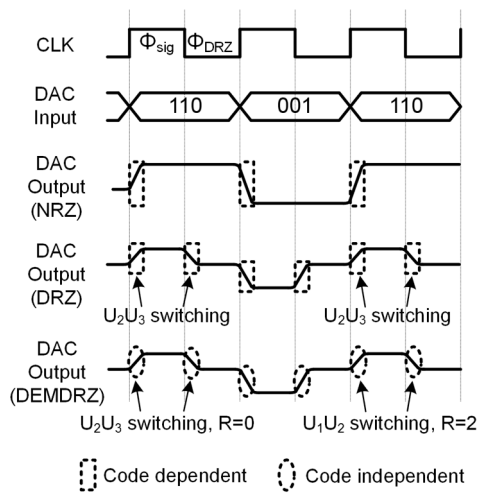

Fig. 4. Output transition comparisons of NRZ, DRZ and the proposed DEMDRZ.

allows the proposed DEMDRZ to simultaneously suppress the current-source mismatch- and transient-induced distortions, and thereby greatly improve the SFDR and IMD.

III. Circuit Design and Implementation

Fig. 5 shows the architecture of the proposed DAC with DEMDRZ, which is segmented into 3 MSB bits, 3 upper LSB (ULSB) bits, 3 LSB bits, and 3 lower LSB (LLSB) bits. The current weighting of the LLSB bit is defined as $\mathrm{I_{LLSB}}$. The current weighting of the other segments are $\mathrm{I_{MSB}} = 512\mathrm{I_{LLSB}}$, $\mathrm{I_{ULSB}} = 64\mathrm{I_{LLSB}}$ and $\mathrm{I_{LSB}} = 8\mathrm{I_{LLSB}}$. As shown in Fig. 5, because the mismatch effect is negligible for the 3-bit LLSB, the DEM coders are only used in the upper 9-bits. The DEMDRZ coder is composed of a DEM coder, a DRZ coder and a multiplexer (MUX). The MUX is used to alternately pass the DEM and DRZ codes to the switch drivers for signal and DRZ phases, respectively. During the signal phase, CLK is 1, and the outputs of the 3 DEM coders and $\mathrm{B_3B_2B_1}$ are passed to the switch drivers. Then, the switch drivers generate complementary outputs to the switches to direct the current sources. During the DRZ phase, CLK is 0, and the outputs of the 4 DRZ coders are passed to the switch drivers. The DRZ coders connect the inputs of the 1st, 3rd, 5th, and 7th MSB $(\mathrm{M_{1,3,5,7}})$ switch drivers to 1. In addition, the inputs of the 2nd, 4th, and 6th MSB $(\mathrm{M_{2,4,6}})$, the 1st$\sim$7th ULSB $(\mathrm{UL_{1\sim7}})$, the 1st$\sim$7th LSB $(\mathrm{L_{1\sim7}})$ and the 1st$\sim$3rd LLSB $(\mathrm{LL_{1\sim3}})$ switch drivers are connected to 0. The above connections implement the mid-code insertion for DRZ, as described in Section II.

Fig. 6 shows 2 SFDR simulations of the proposed DAC in Fig. 5 with and without DEM, respectively. As can be seen, for a SFDR larger than 70 dB, the allowed standard deviation (σ) of the current-source mismatch without DEM is about 1%. With DEM, the σ of current-source mismatch increases to 4%. Each SFDR is the worst case in the 3σ range, i.e., 99.7% yield, of 10,000 runs of Monte-Carlo simulation. Fig. 7 shows the simulated INL curves from 10000 Monte Carlo simulations and their average INL curve with 4% (1σ) mismatch. The maximum INL is 2.7 LSB, while the averaged INL is smaller with DEM. Fig. 8 shows the circuit diagram of the current sources and switches of the proposed DAC. To reduce the total layout area for all current sources and switches, the unit cell of current sources is arranged to the $\mathrm{LL_3}$ bit rather than the $\mathrm{LL_1}$ bit of conventional designs. The current of the $\mathrm{LL_3}$ current source is named $\mathrm{I_u}$; hence, the least current $\mathrm{I_{LLSB}}$ in Fig. 5 equals $1/4 \cdot \mathrm{I_u}$. With a 200 mV overdrive voltage for both the current-source transistor $\mathrm{M_{CS}}$ and the cascoded transistor $\mathrm{M_{CAS}}$, the $\mathrm{M_{CS}}$ dimension can be calculated according to device mismatch data. For 4% (1σ) mismatch, the $\mathrm{M_{CS}}$ for $\mathrm{LL_3}$ bit is sized as width $(\mathrm{W}) = 1.525\ \mu$m and length $(\mathrm{L}) = 1.05\ \mu$m, while the $\mathrm{M_{CAS}}$ is sized as $\mathrm{W} = 0.5\ \mu$m and $\mathrm{L} = 0.25\ \mu$m. Due to the use of DEM, the switch pair can be sized as $\mathrm{W} = 0.12\ \mu$m and $\mathrm{L} = 0.08\ \mu$m. The $\mathrm{LL_2}$ and $\mathrm{LL_1}$ current sources are formed by series-connecting 2 and 4 $\mathrm{M_{CS}}$, resulting in a half and a quarter current of $\mathrm{I_u}$, respectively. Each LSB $(\mathrm{L_{1\sim7}})$, ULSB $(\mathrm{UL_{1\sim7}})$ and MSB $(\mathrm{M_{1\sim7}})$ current source is formed by parallel-connecting 2, 16 and 128

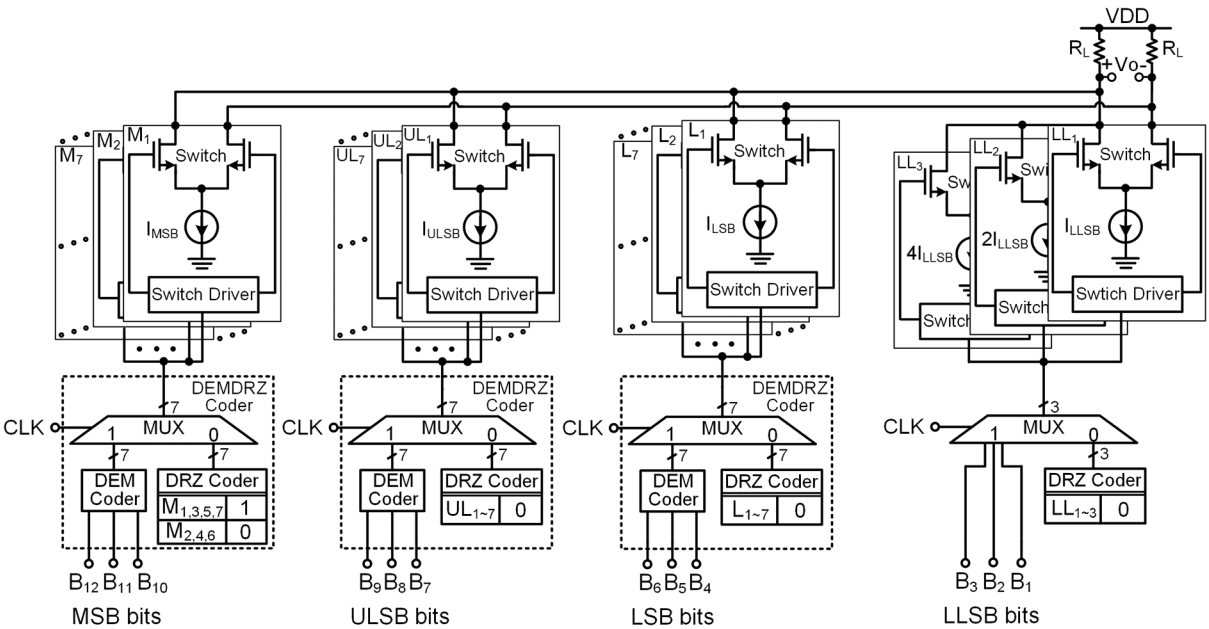

Fig. 5. Architecture of the proposed DAC with $3+3+3+3$ segmentation.

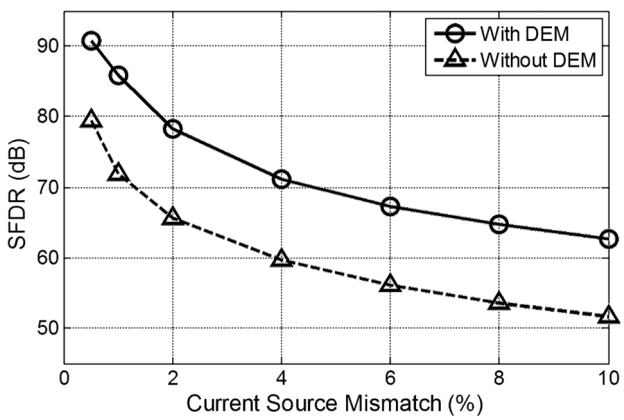

Fig. 6. Behavior simulation of the DEM for the proposed DAC, in which the current source mismatch of 4% (1σ) is chosen.

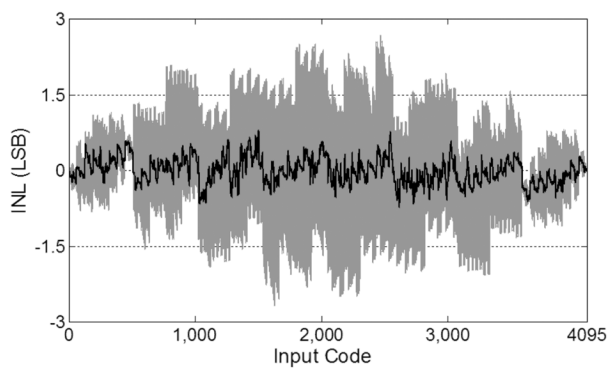

Fig. 7. Simulated INL curves (gray color) from 10000 Monte Carlo simulations with 4% (1σ) mismatch and their average INL curve (black color).

M_{CS}, respectively. To compare the performance of the proposed DEMDRZ to other topologies, SPICE simulation was used. In the simulation with $f_s = 1.6$ GHz, an output of near-DC frequency, $f_{DC} = 0.03 \cdot f_s$, is used to reveal the mismatch-induced nonlinearity; and, an output of near-Nyquist frequency, which causes large numbers of switching elements, $f_{NQ} = 0.487 \cdot f_s$, is used to reveal the transient-induced nonlinearity. The simulation results for NRZ, NRZ+DEM, DRZ, and DEMDRZ are summarized in Table I. For f_{DC} with 4% (1σ) mismatch applied in all current sources and switches, the SFDR performance is dominated by the mismatch-induced nonlinearity. As shown in the Table I, the NRZ+DEM and DEMDRZ more effectively suppress mismatch-induced nonlinearity compared to NRZ and DRZ. For f_{NQ} with and without 4% (1σ) mismatch applied, the SFDR performance is dominated by the transient-induced nonlinearity and is greatly improved when DEMDRZ is used.

Although the output power of the proposed DEMDRZ is half due to the RTZ phase, the flatness of signal amplitude in the wide bandwidth and the better in-band SFDR performance by RTZ phase [10] are more attractive in this paper. For near-Nyquist output frequency, the SFDR performance with DEMDRZ is improved 8.8 dB compared to that without DRZ, as shown in Table I.

The mismatch error within individual MSB, ULSB and LSB segments can be randomized by the DEMDRZ technique, so the gradient mismatch error within each segment, named intra-segment, is mitigated. However, the gradient mismatch error between different segments, named inter-segment, is still a problem because the randomization of DEMDRZ works only within individual segments. As such, a layout floorplan which is simple and compact, but well-compensated for inter-segment gradient mismatch error, is proposed. The floorplan in Fig. 9 also features short metal routings for current source connections and is beneficial for maintaining the high-SFDR bandwidth of DACs. To ensure that the MSB, ULSB, and LSB portions have limited inter-segment mismatch, the MSB, ULSB, and LSB current-source arrays are evenly divided into seven groups, where each group is composed of an MSB current-source array

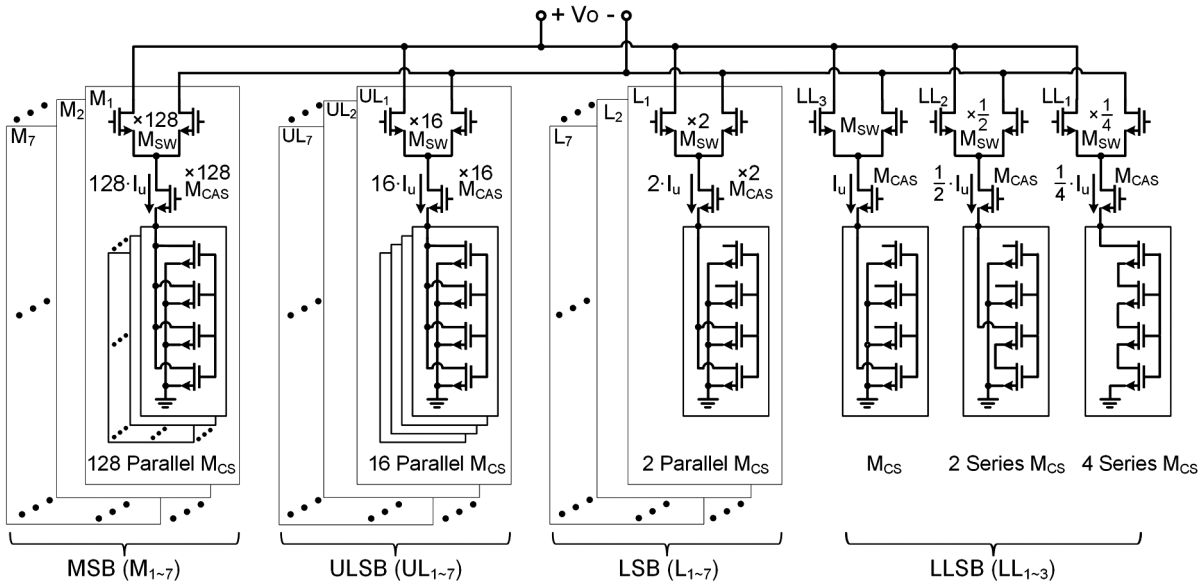

Fig. 8. Circuit diagram of current sources and switch arrays.

TABLE I
SIMULATED SFDR PERFORMANCE OF NRZ, NRZ WITH DEM, DRZ, AND DEMDRZ. $f_{DC} = 0.03 \cdot f_s$, $f_{NQ} = 0.487 \cdot f_s$, AND $f_s = 1.6$ GS/s

f_{out}	Functionality	NRZ	NRZ+DEM	DRZ	DEMDRZ
f_{DC}	No mismatch	76.6 dB	76.4 dB	72.5 dB	74.6 dB
	4% mismatch (current source & switches)	68.9 dB	75.2 dB	67.5 dB	74.1 dB
f_{NQ}	No mismatch	62.4 dB	63.3 dB	68.8 dB	72.4 dB
	4% mismatch (current source & switches)	59.0 dB	63.1 dB	64.5 dB	71.9 dB

containing 128 M_{CS}, a ULSB current-source array containing 16 M_{CS}, and a LSB current-source array containing 2 M_{CS}. The switch arrays are similarly divided, floorplanned and placed close to their corresponding current source groups. As shown in Fig. 9, and compared to a conventional layout arrangement where each segment is "self-grouped", the proposed layout arrangement, named inter-placement, can maintain the current ratio of MSB to ULSB and ULSB to LSB closer to the designed value of 8.

The gradient mismatch quantity has been verified with Monte-Carlo simulations, in which the gradient mismatch error profile with joint error distribution (50% linear + 50% quadratic) was used [9], [12], while the respective gradient mismatch is 2%. Fig. 10 shows the profile, where the rotation angle is used as a parameter to simultaneously turn the X axis and Y axis clockwise to simulate the error distribution under various chip allocations within a silicon wafer, as in [12]. Fig. 11 shows the simulation results of the DEM incorporating the two different layout arrangements. With the inter-placement layout, better SFDR performance is obtained compared to the self-grouped one. In addition, 2% of the gradient mismatch provides large enough tolerance to maintain high yield. Although well-known methods such as common-centroid [2] and random walk [9] are good for gradient error reduction, the proposed inter-placement design does not further partition each of the current sources into 4 or more different sub-current-sources, nor need complicated and long routing wires. Consequently, it is beneficial to reduce parasitic capacitance to increase signal bandwidth.

For better current-source matching, the outermost columns and rows of the whole current source area is surrounded by two dummy rings, which provide identical surroundings to the inner ones. Furthermore, the layout of all current source transistors, including metal routing, is identical to minimize element mismatches. A die photograph of the implemented DAC, including a switch driver array, a switch array, a current-source array, a digital control circuit, and buffer is shown in Fig. 12, where the active area is only 110 μm $\times$ 145 μm.

In a small active area, small transistors and short routing wires induce small parasitic capacitance, maintaining the output impedance at high frequencies [2]. In addition, the small dimension has a small gradient mismatch error, while short and identical wire lengths reduce timing skew for a wider high-SFDR bandwidth. Data latches, which are implemented by D flip-flop, are located at the output of the DEMDRZ coder to synchronize the digital bits. Although small transistors induce random skew variation between digital bits, the skew can be suppressed by the randomization of DEMDRZ.

IV. MEASUREMENTS AND COMPARISONS

Fig. 13 shows the measurement setup, where the DAC's output current is converted to voltage through an off-chip 50 Ω resistive differential load and coupled to a spectrum analyzer through a wideband transformer. The digital inputs and clock

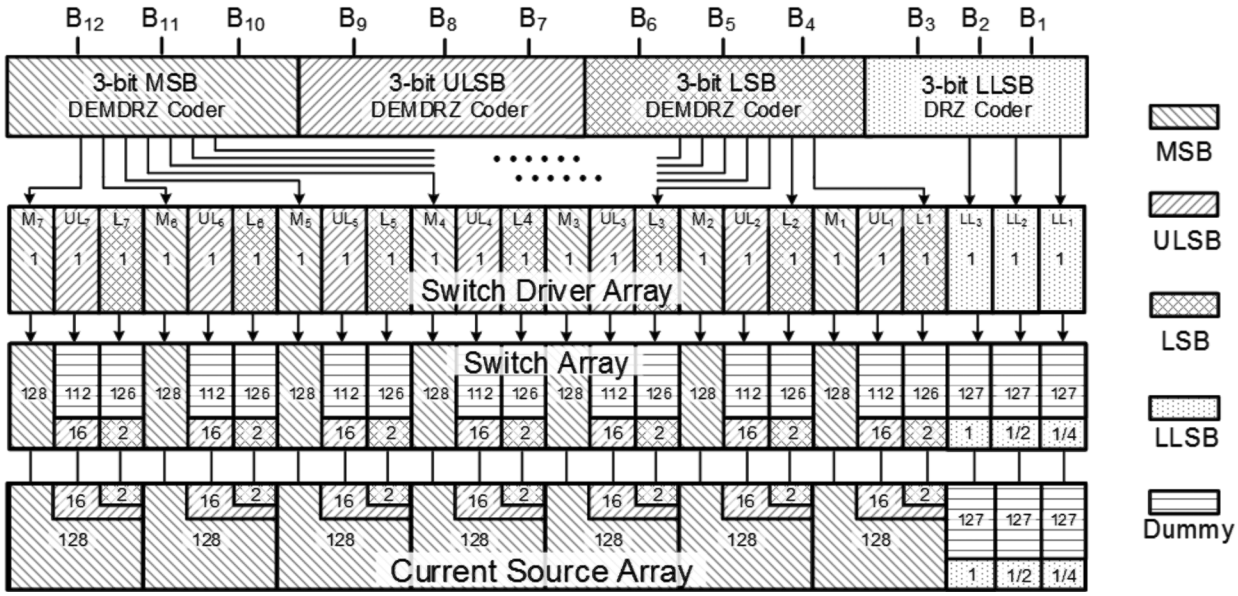

Fig. 9. Floorplan of the proposed DAC.

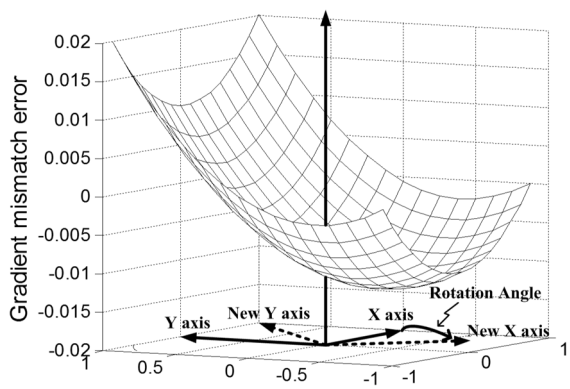

Fig. 10. Gradient mismatch error profile with joint error distribution, where the rotation angle of this profile is zero degree.

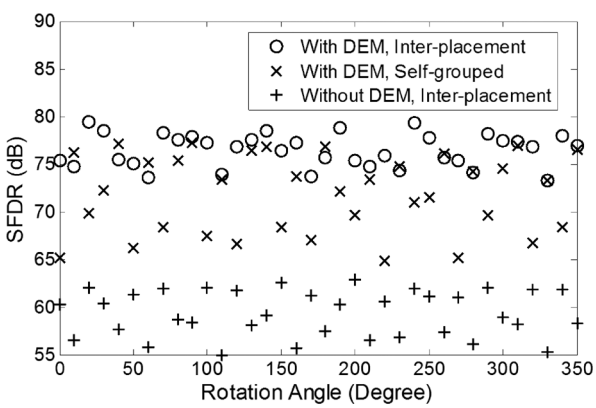

Fig. 11. SFDR Monte-Carlo simulations for the use of DEM with the two different layout patterns, inter-placement (o) and self-grouped ($\times$). The other simulation shows when DEM is not used for the inter-placement ($+$) layout pattern.

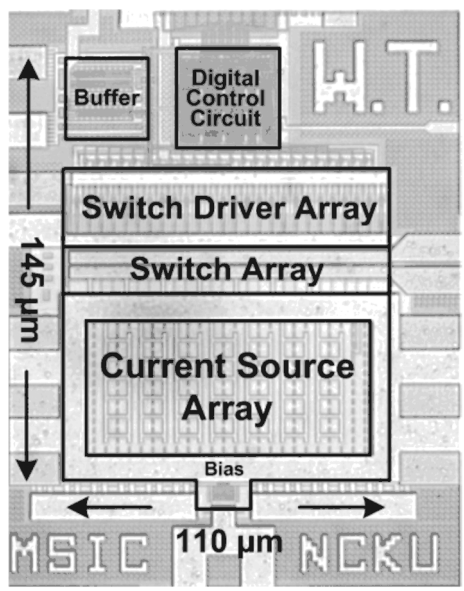

Fig. 12. Photograph of the proposed DAC.

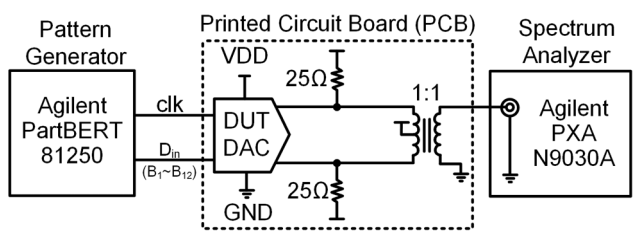

Fig. 13. Measurement setup.

are produced by Agilent ParBERT 81250, and all measurements were performed with a full-scale load current of 16 mA, which corresponds to an 400 mV peak-to-peak voltage swing at the output pins of the IC. However, for the DAC without connecting a spectrum analyzer, the peak-to-peak output swing is 800 mV. Fig. 14(a) shows the measured power spectrum density (PSD) of the DAC with a 15 MHz signal clocked at 1.6 GS/s, where the SFDR is 74 dB. Fig. 14(b) shows the measured PSD with a 784 MHz signal clocked at 1.6 GS/s,

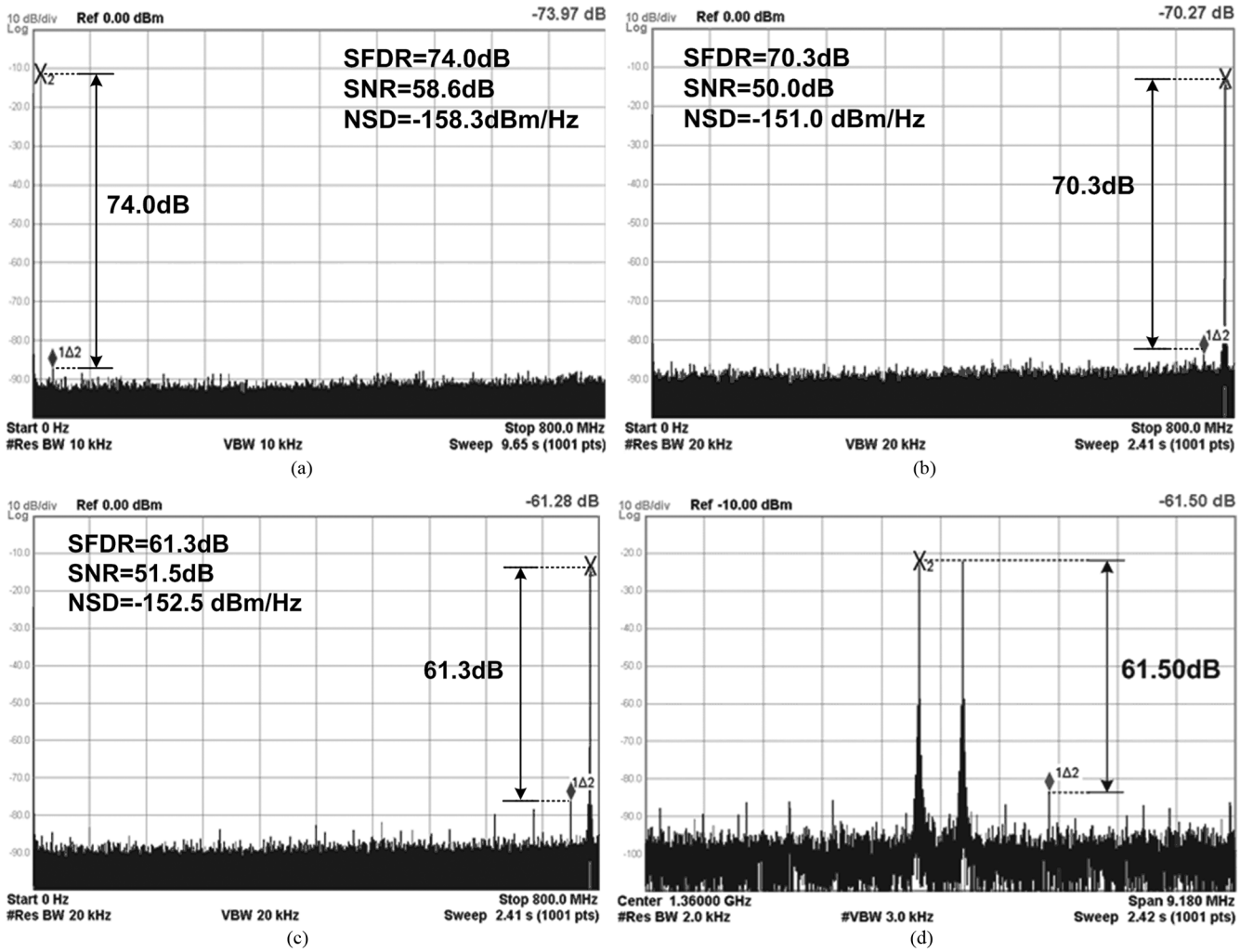

Fig. 14. Measured spectra for (a) SFDR with a 15 MHz signal clocked at 1.6 GS/s, (b) SFDR with a 784 MHz signal clocked at 1.6 GS/s, (c) SFDR with a 784 MHz signal clocked at 1.6 GS/s while DEM is turning off, and (d) IMD with 1360 MHz $\pm$ 0.35 MHz signals clocked at 2.8 GS/s.

where the SFDR is 70.3 dB and the power consumption of the DAC is 40 mW. Fig. 14(c) shows the measured PSD with a 784 MHz signal clocked at 1.6 GS/s while DEM is turned off, which decreases the SFDR to 61.3 dB. This phenomenon is consistent with the simulations in Fig. 6 and Table I. The NSD without DEM in Fig. 14(c) is -152.5 dBm/Hz. Even though the NSD with DEM in Fig. 14(b) is -151.0 dBm/Hz, which is slightly higher than that without DEM, the measured SFDR with DEM is increased from 61.3 dB to 70.3 dB compared to that without DEM.

Fig. 14(d) shows the measured PSD with two signals 1360 MHz $\pm$ 0.35 MHz clocked at 2.8 GS/s, where the IMD is -61.5 dB and the power consumption of the DAC is 47 mW. Fig. 15 shows the measured SFDR with signals clocked at 1.6 GS/s and 2.8 GS/s. Fig. 16 shows the IMD with signals clocked at 1.6 GS/s and 2.8 GS/s, respectively. At 1.6 GS/s, the DAC achieves < -70 dB IMD for signals over the 800 MHz Nyquist bandwidth; while at 2.8 GS/s, the DAC achieves < -61 dB IMD for signals over the 1.4 GHz Nyquist bandwidth. Fig. 17 shows the measured noise spectral density (NSD) with signals clocked at 1.6 GS/s and 2.8 GS/s, in which the NSD remains < -151 dBm/Hz and -131 dBm/Hz over the 800 MHz and 1.4 GHz Nyquist bandwidths, respectively. The measured SFDR versus signal frequency is shown in Fig. 18(a), where comparisons with state-of-the-art CMOS DACs [1], [3], [13] are included. At 1.6 GS/s, the proposed DAC achieves >70 dB SFDR with signals over the 800 MHz Nyquist bandwidth, which outperforms the other state-of-the-art CMOS DACs, which achieve less than 500 MHz bandwidth with a 70 dB SFDR. Fig. 18(b) shows the measured IMD versus signal frequency and comparisons with other state-of-the-art CMOS DACs. The proposed DAC achieves an IMD comparable to other state-of-the-art CMOS DACs; however, its active area requirement is less than 6% of the others, as shown in Fig. 18(c). Fig. 18(c) also shows the comparison of normalized area, active area$/$(feature size)^2, to further demonstrate the contribution due to the circuit design, not the process scaling. Table II summarizes the measurement results of state-of-the-art 12 to 14-bit DACs. Based on these results, the three common figures-of-merit (FoMs) proposed in [5], [14], and [15] are adopted. The proposed DAC performs rather excellently for FoM_1 and FoM_2, and 210 times better for FoM_3.

TABLE II
COMPARISON WITH STATE-OF-THE-ART 12–14 BIT CMOS DACS

	This Work	ISSCC 2012 [13]	JSSC 2011 [3]	JSSC 2009 [1]	
Resolution, N	**12**	14	12	12	
Feature size	**40nm**	0.18μm	90nm	65nm	
Supply (V)	**1.2**	1.8/ 3	1.2/ 2.5	1/ 2.5	
f_{clk} (GS/s)	**1.6**	3	1.25	1.6	2.9
I_{load} (mA)	**16**	20	16	50	
P_{total} (mW)	**40**	<600[a]	128	-	188
BW_{70dB} (MHz)	**800**	350	500	225	200
$BW_{6(N-1)dB}$ (MHz)	**800**	100	625	300	250
$V_{swing,ppd}$ (V)	**0.8**	1	0.8	2.5	
Active area (mm^2)	**0.016**	4	0.825	0.31	
$SFDR_{Best}$ (dB)	**74.0**	84.0	75.0	74.0	74.5
$SFDR_{Worst}$(dB)	**70.3**	52.0	66.0	52.5	-
SNR_{Best} (dB)	**58.6**	-	-	-	-
SNR_{Worst} (dB)	**50.0**	-	-	-	-
IMD(dB)	**<-61 @2.8GS/s**	<-65	-	-	<-52
FoM_1	**8.19E+04**	2.73E+03	2.00E+04	-	5.45E+03
FoM_2	**4.43E+05**	2.12E+04	7.34E+04	-	-
FoM_3	**2.10E+10**	1.12E+07	9.93E+07	-	7.20E+07
Term	FoM_1 [14]	FoM_2 [5]		FoM_3 [15]	
Definition	$\frac{2^N \times BW_{6(N-1)dB}}{P_{total}}$	$\frac{2^{\frac{SFDR_{Best}-1.76}{6.02}} \times 2^{\frac{SFDR_{Worst}-1.76}{6.02}} \times f_{clk}}{P_{total}-P_{load}}$		$\frac{2^{2N} \times BW_{6(N-1)dB}}{P_{total} \times Area}$	

[a] 600mW@5GHz

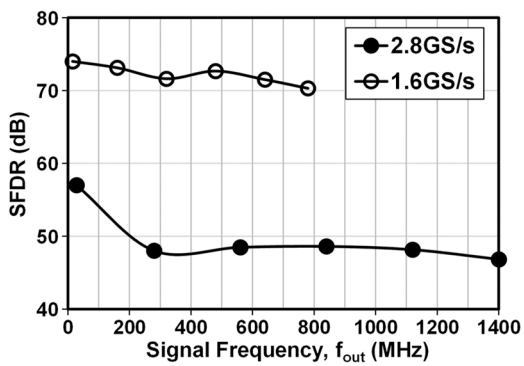

Fig. 15. SFDR versus signal frequency clocked at 1.6 GS/s and 2.8 GS/s.

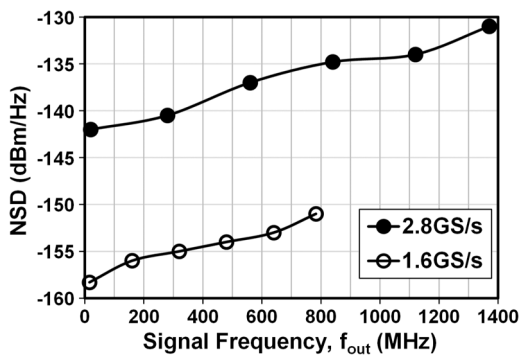

Fig. 17. NSD versus signal frequency clocked at 1.6 GS/s and 2.8 GS/s.

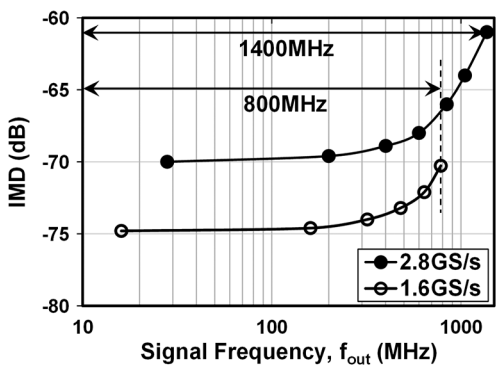

Fig. 16. IMD versus signal frequency under 1.6 GS/s and 2.8 GS/s.

V. CONCLUSION

In this paper, DEMDRZ was proposed to greatly improve SFDR and IMD for high-frequency application. The implemented DAC achieves >70 dB SFDR at 1.6 GS/s and IMD <−61 dB at 2.8 GS/s, respectively. With the small DAC cells due to the adoption of DEMDRZ and the compact layout, the total active area is less than 6% of other state-of-the-art 12-bit DACs. Due to area reduction, overall parasitic capacitance and wire lengths are also reduced, resulting in a wider high-SFDR bandwidth and lower power consumption. Further, the implemented DAC achieves the best FoMs compared to other state-of-the-art DACs. Consequently, the proposed DEMDRZ technique is very suitable for compact, low-power, high-speed, high-resolution current-steering DACs.

ACKNOWLEDGMENT

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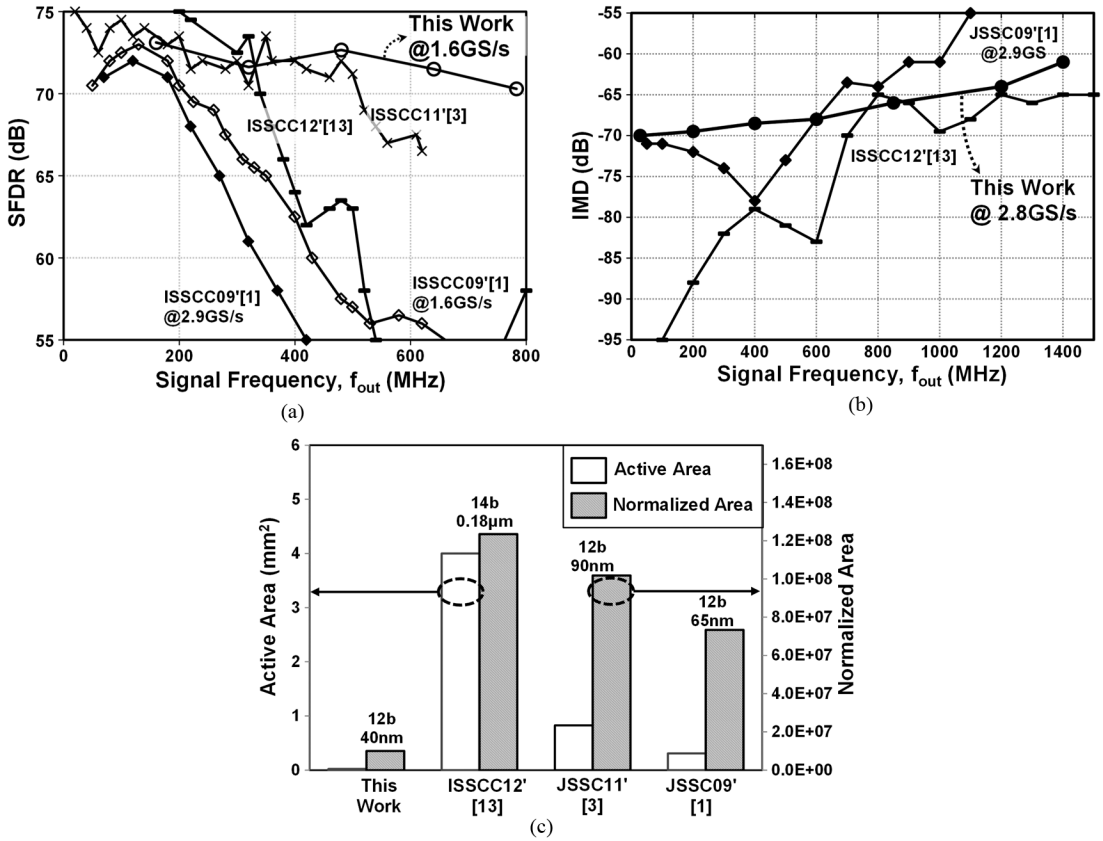

Fig. 18. Comparison with state-of-the-art CMOS DACs for (a) SFDR versus signal frequency, (b) IMD versus signal frequency, and (c) active area and normalized area.

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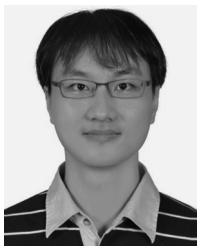

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