A Fast Locking-in and Low Jitter PLL With a Process-Immune Locking-in Monitor

Chung-Yi Li, Chung-Len Lee, Ming-Hong Hu, and Hwai-Pwu Chou

***Abstract*— In this brief, a digital-control adaptive phase-locked loop (PLL) with a digital locking-in monitor (LIM) consisting of a time-to-digital converter (TDC) and a bandwidth control unit (BCU) is proposed to reduce the locking time as well as to suppress the jitter when locked. It uses a delay-independent threshold in a dual-slope transfer function to detect the locked state according to the counting result of the proposed TDC, which feeds to the BCU to switch the bandwidth of PLL. Then the PLL is switched from a wide loop bandwidth (6 MHz) to a narrow bandwidth (3 MHz) in the locked state. To verify the proposed scheme, the proposed adaptive PLL is implemented in a TSMC 0.18 μm 1P6M CMOS process with a supply voltage of 1.8 V. The measurement results show that the locking time is reduced by 67% while with a RMS jitter of only 8.79 ps when operating at 1.6 GHz.**

***Index Terms*— Adaptive phase lock loop, fast locking-in, locking-in monitor (LIM), low jitter, process-immune.**

I. Introduction

The phase-locked loop (PLL) plays a crucial role in most of today's high-speed digital computers and communication systems, in providing the time base, the synchronizing signal, and the local synthesized signal for converting frequencies. For the above applications, it is required that the PLL provides the signal instantaneously and stably. Numerous works have been dedicated to shortening the locking-in time and improving the jitter performance of the PLL [1]–[7]. However, the above two criteria for a PLL are somehow contradictory to each other. The fast lock-in needs a charge-pump (CP) circuit with a large driving capability and a low-pass filter (LF) of a wide band. However, this will lead to a larger jitter once the PLL goes into the locked-in state. Hence it is natural that people resort to adopting the "adaptive" mechanism, i.e., using a CP circuit of a large driving capability and a wide-band LF during the PLL locking-in process and switching to a CP circuit with a low driving capability and an LF of a narrow-band when the PLL reaches the locked-in state. The latter offers a more stable oscillating signal of a lower jitter since the overall loop gain of the PLL is smaller.

However, in all the above works, the detection and the related circuits are mostly composed of analog devices, which are sensitive to the semiconductor process. In this brief, we propose and demonstrate a digital-control type of the adaptive PLL for which the effect caused by the semiconductor process is eluded. The PLL utilizes a time-to-digital converter (TDC) and a bandwidth control unit (BCU), both of which are digital, to detect the locked-in state and to switch the CP and the bandwidth of the PLL to achieve the fast lock-in and low jitter after locked-in. Fabricated device of this PLL demonstrates that it has a fast locking-in time and a low jitter than the same PLL, which does not employ the above mechanism.

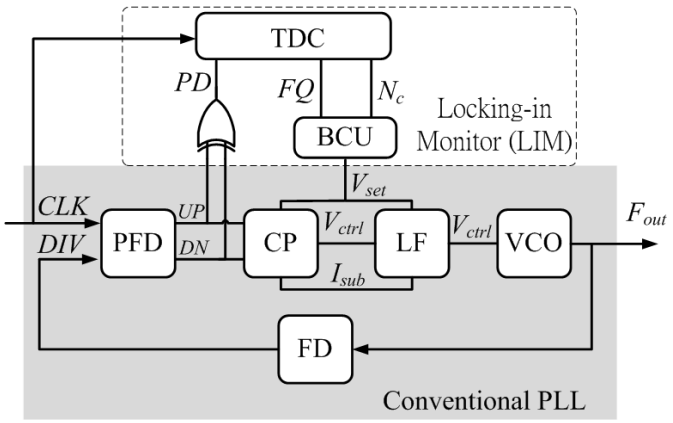

Fig. 1. Block diagram of the proposed adaptive PLL with LIM.

II. Digital-Controlled Mechanism for Adaptive PLL

The block diagram of the proposed adaptive PLL is shown in Fig. 1. In the figure, in addition to the PLL main body, a TDC, an exclusive-or gate, and a BCU, which form the lock-in monitor (LIM) unit whose critical parts are either implemented digitally or made insensitive to the semiconductor process, are added. In addition to the CP circuit of the PLL main body, there is another charge pump circuit, CPTD, in TDC. Both charge pump circuits are designed to be insensitive to the process, which will be explained in detail later. The LF has two modes, i.e., the narrow-band mode and the wide-band mode, which are switchable by the bandwidth control signal $V_{\rm set}$. Whenever the PLL is in the process of locking-in, TDC and BCU detect this condition from the phase difference signal *PD*. CP of the larger driving capability and LF of the wider bandwidth are in operation. This speeds up the locking-in process to shorten the locking time of the PLL. When the PLL has reached the "locked-in" state, TDC detects this condition again. In conjunction with BCU, LIM will send the control signal, $V_{\rm set}$, to switch the PLL to CP circuit with a lower driving capability and the LF of the narrower bandwidth mode to obtain an output of a lower jitter. $I_{\rm sub}$ is utilized to reduce the capacitor size in LF. The details will be explained in a later section.

III. Delay-Independent Transfer Curve

An adaptive PLL has a transfer curve as shown in Fig. 2 where the solid line and dotted line are the wide-band and the narrow-band transfer curves, respectively, and the $\tau(\tau_{\rm D})$ is the phase threshold. When the phase difference of the generated pulse and the reference pulse is smaller than $\tau(\tau_{\rm D})$, the PLL switches into the narrower bandwidth mode. For the conventional phase threshold, τ is equal to $2\pi\,\Delta/T_{\rm CLK}$, where $T_{\rm CLK}$ is the clock period and Δ is the cell delay, which is sensitive to the semiconductor process. In our proposed PLL, $\tau_{\rm D}$ is controlled digitally by the counter, which is digital in

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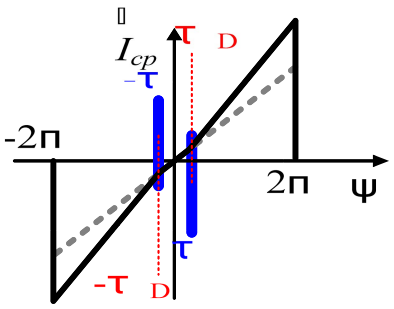

Fig. 2. Transfer curves of the proposed delay-independent adaptive PLL and the conventional one.

form and is insensitive to the semiconductor process. This makes the PLL delay-independent adaptive.

In our case, τ_D is set to be $2\pi \cdot (T_{CLK} = 8)/T_{CLK} = \pi/4$. $T_{CLK}/8$ is the phase threshold (Φ_{th}) when the PLL is to switch the operation mode. It could be any other value. It is a fixed value and is only related to the counter output Nc.

N_c is related to the ratio of the charging and discharging currents I_c and I_d of the CP_{TD}, respectively, as

$$P_{th} = J_{avg} = \frac{I_c}{I_d}\frac{\frac{T_{CLK}}{2}}{N_c} \tag{1}$$

where J_{avg} is the average phase difference of the generated pulses and the reference pulse within the N_c counts before the PLL is locked-in. In our brief, I_d was chosen to be the same as I_c to make the rising time and the falling time of the charging pulse the same value and the shape of the pulse symmetrical. The value of the capacitor C_{PJ} has nothing to do with N_c since the capacitor serves only as a reservoir for charges, Q_{CPJ}, of the charging and discharging currents. For the charging current, Q_{CPJ} is $C_{PJ} \cdot (I_c \cdot T_{CLK})$ and for the discharging current, it is $C_{PJ} \cdot (I_d \cdot N_c \cdot J_{avg})$. These two quantities are equal, so $(I_c \cdot T_{CLK}/2) = (I_d \cdot N_c \cdot J_{avg})$. It is then noted that J_{avg} has nothing to do with C_{PJ} as that in [8]. Thus, when the C_{PJ} has small variations due to the semiconductor process, it does not affect the mode selection mechanism of the PLL.

IV. Details of the Digital-Control Circuits

A. Time-to-Digital Converter

Fig. 3 shows the detailed circuit of TDC, which is composed of a charge pump, CP_{TD}, a comparator CH, which has a hysteresis characteristics (as shown in the right bottom of Fig. 3) with two threshold voltages, V_{thH} and V_{thL}, a D-flip flop (DFF), and a six-bit counter. The current sources of CP_{TD} are controlled by the feedback signal, FQ, which is the output $\bar{Q}$ of DFF. During the locking-in process, FQ = 1 and C_{PJ} gets charged for the positive half cycle of the reference clock CLK as shown in Fig. 4(a). In the figure, V_{cap} is the voltage of the C_{PJ}. The current source I_c is designed to be large enough to charge V_{cap} to exceed V_{thH}, the upper threshold of the comparator CH, within this half cycle. V_{out}, the output of CH, will be switched to HIGH. This will toggle DFF to change its state, i.e., FQ becomes LOW. Then C_{PJ} will enter into the discharging process. During this period, whenever PD goes to HIGH, C_{PJ} gets discharged. PD is a series of pulse trains whose width is dependent of the difference of DIV and CLK in Fig. 1. The larger the difference, the wider of the pulse, and the more of C_{PJ} gets discharged. In other words, the number of PD pulses to discharge V_{cap} to V_{thL} inverse proportional to the width of the pulses. The V_{cap} waveform of Fig. 4(a) shows such a discharging process, where it takes three PD pulses to discharge the C_{PJ} to reach V_{thL}. The six-bit counter is used to count the number of these discharging pulses as shown in

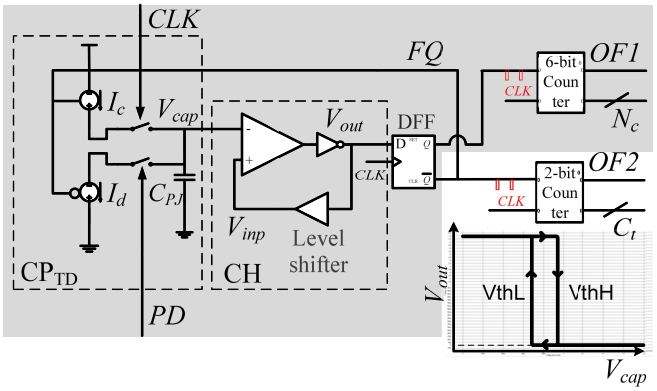

Fig. 3. Design of proposed time-to-digital converter.

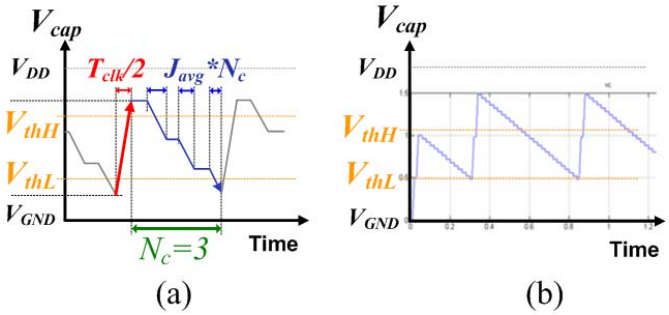

Fig. 4. (a) Mechanism of time-to-digital converter. (b) Doubling charging due to large capacitor.

Fig. 3. As the V_{cap} reaches less than V_{thL}, CH switches its state and the counter stops counting. When the PLL has reached the "locked-in" stage, i.e., the value of counter exceeds 4, a signal N_c is sent out to the BCU, whose detailed circuit will be explained in the next section. In addition to the main body of TDC as shown in gray box in Fig. 3, we add a two-bit counter to count the charging times for tolerating the variance in C_{PJ}. Fig. 4(b) demonstrates that the double charging is detected by the two-bit counter due to the large capacitor C_{PJ}.

In the above, the DFF and the six-bit counter are digital circuits that are insensitive to the semiconductor process. The CP_{TD} and the comparator CH are analog circuits. Their sensitivity to the semiconductor process is minimized to the least through the design techniques to be described later.

B. Bandwidth Control Unit

The detailed circuit of BCU is shown in Fig. 5. It is composed of three flip-flops: DFF1, DFF2, and DFF3. The third bit of the six-bit counter and the FQ from TDC are its input. The third bit is chosen because in our demonstrative design, N_c is chosen to be 4. For TDC, when the FQ switches from logic LOW to HIGH, i.e., the circuit CP_{TD} switches from the discharging process to the charging process, S_{THN} of this BCU will be reset to HIGH by DFF2. Then, DFF3 will send a HIGH to reset DFF1. As a result, output Q of DFF1 resets DFF3 again to make it ready for the next judgment to see whether the PLL has entered into the locked-in state. When the value of N_c of TDC exceeds 4, the third bit of counter is HIGH, i.e., $S_{THP} = 1$. Consequently V_{set} becomes HIGH. At the same time, S_{THN} becomes LOW by DFF2. This $V_{set} = 1$ will make the PLL set into the locked-in state, i.e., the CP and the LF of the narrower bandwidth will be in operation to give a lower jitter. In the above, whenever $FQ = 1$, DFF2 and DFF3 are cleared. This ensures that BCU is ready for sensing the value of N_c for every charging and

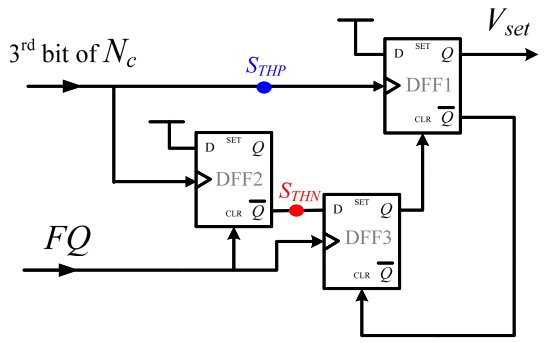

Fig. 5. Proposed bandwidth control unit.

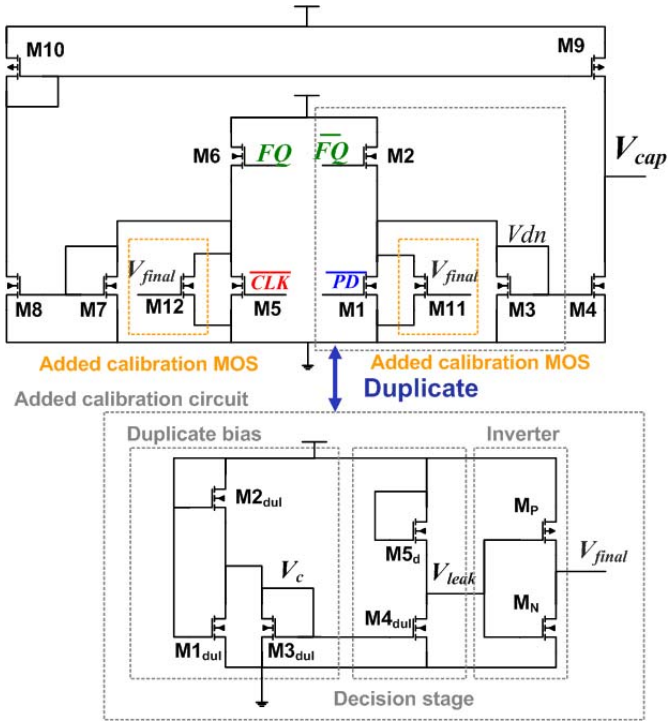

Fig. 6. Detailed charge pump circuit with an autocalibration duplicated circuit.

discharging cycle of CP_{TD}. The values of two signals S_{THP} and S_{THN} are (S_{THP}, S_{THN}) = (0, 1) when the PLL is in the locking-in process and (S_{THP}, S_{THN}) = (1, 0) when the PLL is in the locked-in state.

C. Charge Pump Circuit CP_{TD}

The detailed circuit of the CP_{TD} is shown in Fig. 6. It is a circuit of a pseudo-differential structure that has an advantage of matching the charging and discharging currents against the process variation. When CP_{TD} is operated in discharging process, the output FQ is LOW and transistor M2 of CP_{TD} is on. Before the jitter signal comes, M1 is on, thus the current from M2 mainly flows into M1. At this moment, *Vdn* is determined by the W/L ratio of M1 and M2. This value of *Vdn* is denoted as "*Vdn1*." When the jitter signal comes, M1 is off, the current from M2 will flow into M3 that serves as a current mirror to control M4 via the voltage *Vdn*. However, at this moment, the value of *Vdn* is controlled by the W/L ratio of M2 and M3. This value of *Vdn* is denoted as "*Vdn2*." When *Vdn* changes a little bit from "*Vdn1*" to "*Vdn2*," M4 is turned on already. *Vdn1* can be designed to have a larger value to reduce the M4's turn-on time by choosing a larger W/L ratio of M1 and M2. However, increasing *Vdn1* will introduce the leakage current in M4 for the FS (fast-slow) and FF (fast-fast) corner operation of the circuit since at these corners, the threshold voltage of M4 becomes relatively lower. To solve this problem, two transistors, M11 and M12, whose gates are controlled by the output voltage V_{final} of a duplicated circuit as shown at the bottom in the Fig. 6, are added to autocalibrate the value of *Vdn1*. For the duplicated circuit, M1dul to M4dul have exactly the same sizes of M1 to M4, respectively. This results in V_c whose value equals to *Vdn1*. For the FS and FF corner operations of the circuit, if M4 is turned on with the value of *Vdn1*, $M4_{dul}$ will also be on by V_c. This will make V_{final} be HIGH, which consequently makes M11 be on, and this in turn will decrease *Vdn1*. This mechanism makes the charge pump circuit CP_{TD} function well even at five extreme operation corners [i.e., FF, FS, SF (slow-fast), SS (slow-slow), TT (typical-typical)]. The simulation result shown later will demonstrate this.

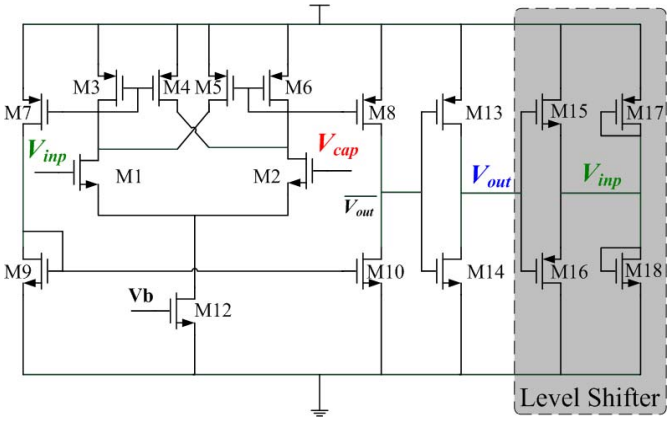

Fig. 7. Proposed hysteresis comparator with positive feedback.

D. Comparator Circuit With Hysteresis CH

The detailed circuit of the comparator CH with a hysteresis characteristic is shown in Fig. 7, for which a positive feedback architecture is adopted. For the circuit, to eliminate the effect of the semiconductor process variation on the reference voltages V_{thH} and V_{thL}, the output of the differential amplifier, V_{out}, is connected to a level shifter, M15–M18, and the output, V_{inp}, is connected to the input node of M1 to form a feedback. When V_{out} is HIGH, M15 is on and M16 is off, the current flows through M15 and M18. At this moment, $V_{inp} = V_{thL}$, whose value is determined by the W/L ratio of M15, M17, and M18. On the contrary, when V_{out} is LOW, $V_{inp} = V_{thH}$, whose value is determined by the W/L ratio of M16, M17, and M18. Since the threshold voltages V_{thL} and V_{thH} depend only on the W/L ratios of M15 and M16 to M17–M18, respectively, they are much easier to be controlled than the case that depends on the band gap voltages on C_{PJ} and on positive input of comparator as in [8]. The five corner experimental results shown in Fig. 8 demonstrate that the threshold voltages V_{thL} and V_{thH} of our proposed CH have smaller variances (111 mV) than that (200 mV) of the PLL according to the architecture of work in [8].

V. Simulation and Measurement Result

A. Simulation Results

The proposed adaptive PLL was implemented under a TSMC 0.18 μm 1P6M CMOS process, and a chip area is 1.053 $\times$ 0.983 μm^2. The divisor of the implemented PLL was 32. To verify the performance of TDC with respect to the process variation, the five operation corners of the TDC with a 20% process variation were simulated with respect to the input jitters. Fig. 9 shows the simulated relative errors of the obtained jitters with respect to the

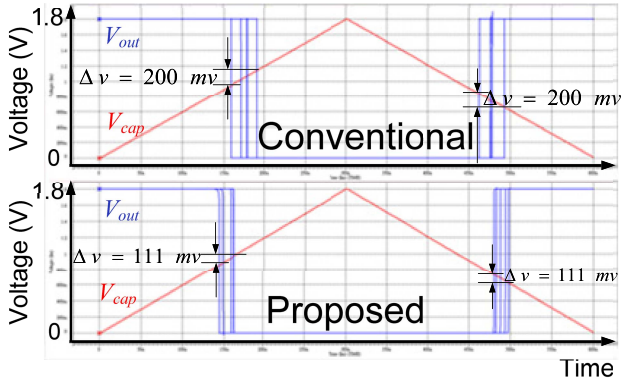

Fig. 8. Process immunity in $V_{\mathrm{th}H}$ and $V_{\mathrm{th}L}$ of five operation corners.

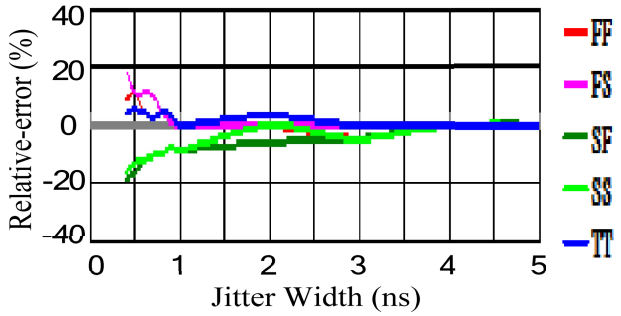

Fig. 9. Relative errors for the five corner operations of the PLL.

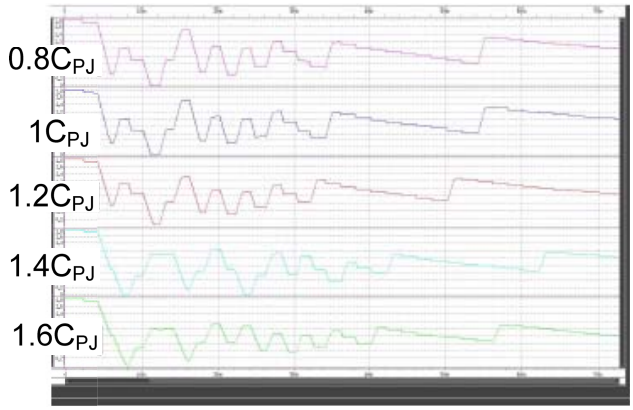

Fig. 10. Simulated Vcap, the voltages on the C_{PJ} when the value of C_{PJ} varies from -20% to $+60\%$ due to the process variations.

input in terms of the width of the injected jitters. For the simulation, jitters of the width from 0.4 ns to 5 ns for a 50 MHz reference signal were injected to the input, i.e., *PD*, of the TDC and the output of N_c were computed to be compared with the injected input jitters. It is seen that the relative errors are less than 20% for the operations of all five corners. For the injected jitter of more than 0.7 ns, the error is even less than 10%. This result demonstrates that the operation of the proposed TDC is insensitive to the process variations. Furthermore, the simulated V_{cap} of the C_{PJ} of the TDC is plotted in Fig. 10 for the cases of the value of C_{PJ} varying by -20% to 60% from its nominal value when the input frequency of the reference signal of the PLL is abruptly changed from 0 Hz to 50 MHz. In the figure, all the curves vary irregularly in initial several cycles and then go to a steady charging and discharging cycle. This figure demonstrates the robustness against process variations of the proposed TDC.

Fig. 11 shows the postsimulation for the V_{ctrl} of the output of the LF when it operates in adaptive mode (blue line), wide-band

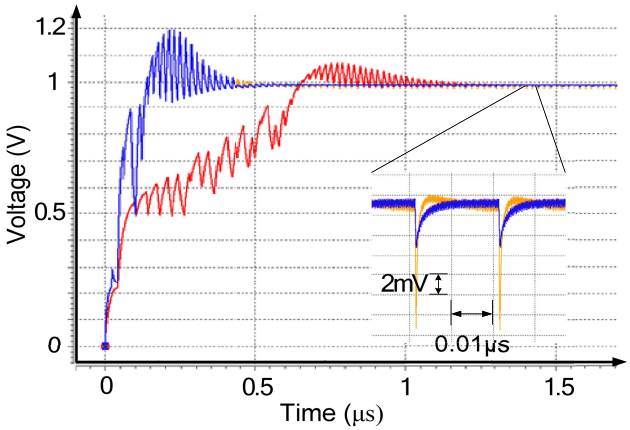

Fig. 11. Post-layout simulation for Vctrl of the output of the LF in the adaptive mode (blue line), wide band mode (orange line), and the narrow band mode (red line) without the adaptive mechanism, respectively. The point when the control signal Vset.

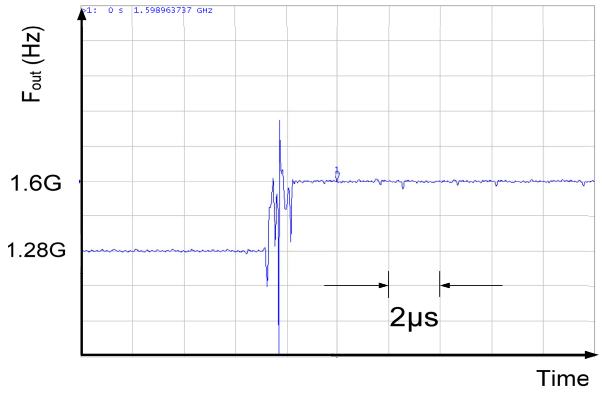

Fig. 12. Transient for digital-controlled adaptive PLL.

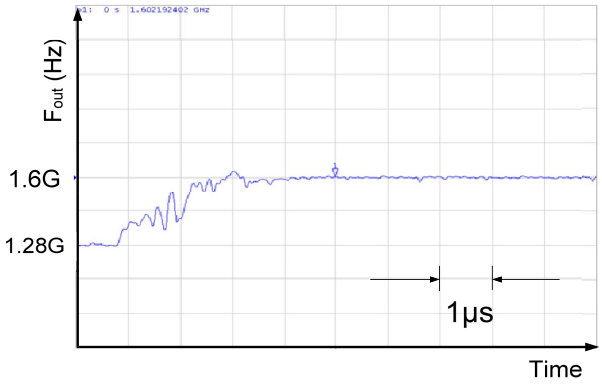

Fig. 13. Transient for narrow-band.

mode (orange line), and narrow-band mode (red line) but without incorporating the adaptive mechanism, respectively. It is seen that the locking time of the adaptive PLL is reduced significantly compared with narrow-band mode. In contrast, the jitter is reduced compared with wide-band mode.

B. Measurement Results

The designed PLL was fabricated and its performance was measured. A Tektronix Digital Phosphor Oscilloscope (7404/20GS/s, up to 4GHz) was used to measure the jitter performance of the PLL. It could be deduced that the peak-to-peak jitter was 45 ps, and the RMS jitter was 8.789 ps, respectively. In addition, an Agilent Signal

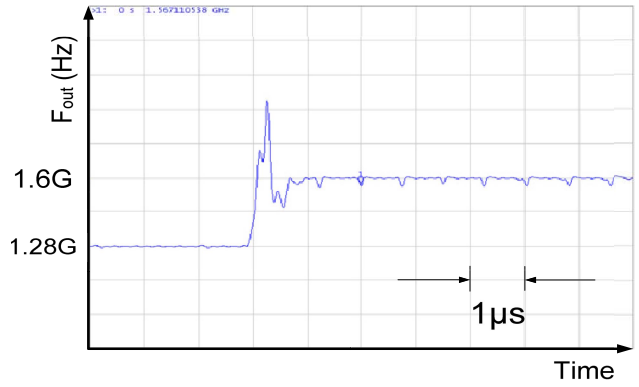

Fig. 14. Transient for wide-band.

Source Analyzer (E5052B/10MHz 7GHz) was used to measure the transient behavior of the PLL. Figs. 12–14 show the measured VCO output F_{out} transients for the adaptive PLL, the PLL with only the narrow-band mode operation, and the PLL with only wide-band mode operation, respectively. The PLLs were switched from 1.28 to 1.6 GHz for the measurement. As it is seen that the adaptive PLL has the improvement on its locking-in time by approximately 67% as compared with that of the narrow-band PLL while has the same ripple the narrow-band PLL when it goes into the locked-in state.

VI. Conclusion

This brief proposes and demonstrates a digitally controlled adaptive PLL, which utilizes digital TDC and BCU to accomplish the locked-in state detection with a bandwidth control algorithm. The algorithm uses a fixed phase threshold with a delay-independent dual-slope transfer function to achieve the bandwidth control. A design for the hysteresis comparator using the positive feedback to achieve the robust thresholds eliminates the use of a reference voltage, which was used in the conventional adaptive PLL designs. Also, a process-immune charge pump circuit is also incorporated. These altogether make the proposed adaptive PLL insensitive to the process variations. Simulation and the implemented chip measurement results show that the PLL is process variation immune and demonstrate the fast locking-in while still maintain the low jitter performance.

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A 5.8 nW 9.1-ENOB 1-kS/s Local Asynchronous Successive Approximation Register ADC for Implantable Medical Device

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***Abstract*— This brief presents a 10-bits successive approximation register analog-to-digital converter (ADC) with a sampling rate of 1 kS/s for implantable medical devices. This ADC is implemented in a 65-nm CMOS process in which leakage current will be a key design parameter. It imposes the highest degree of simplicity in the design of the ADCs architecture. Thus, the transistor count is minimized, which reduces not only the active power, but also the number of leakage sources. The modified top-plate V_{cm}-based switching offers energy efficient switching at the capacitive-DAC (CDAC) and uses simple control logic. In addition, the proposed asymmetrical metal-oxide-metal capacitor reduces the size of the CDAC by 90% for a given gain error. Furthermore, the input referred offset voltage of the dynamic comparator can be improved by the top-plate V_{cm}-based switching method at system level without using any additional transistor. The other building blocks are also simplified for lower power consumption. This ADC occupies an area of 0.046 mm^2. At 0.9 V and 1 kS/s, the 10-bits ADC consumes 5.8 nW, in which, 2.34 nW is contributed by leakage power consumption. The ADC achieves 9.1-ENOB and an energy efficiency of 10.94-fJ/conversion step.**

***Index Terms*— Analog-to-digital converter (ADC), asynchronous, charge recycling, dynamic comparator, energy efficient, low leakage, low power, medical implant, successive approximation (SA), successive approximation register (SAR).**

I. Introduction

Implantable medical devices, like pacemakers, provide a great advantage to one's life in terms of clinical opportunity. However, the electronic systems for these devices have to be extremely efficient in both silicon area and power consumption due to the unique operating environment [1]. Among all the electronics components, analog-to-digital converter (ADC) is one of the most important and power hungry components as it needs to convert various analog electrophysiological signals to digital codes continuously. The bandwidth of these signals can range from dc to a few kilohertzs [2]. Therefore, the ADC does not need a high sampling speed, but requires power consumption that is in the range of nanowatt. In addition, the rising demand for higher system complexity but smaller battery size has pushed the system designers to move toward more advanced technology, which enables tremendous gains in the complexity without an increase in the overall power consumption [1]. However, subthreshold transistor leakage [3], [4], gate-induced drain leakage and gate tunneling [1] start to become a key factor to degrade the system's power efficiency especially for low speed ADC [5].

In this brief, a 1 kS/s 10-bits successive approximation register (SAR) ADC is designed using a 65-nm CMOS process for implantable medical devices. SAR architecture is chosen as it provides good tradeoffs among power efficiency, conversion accuracy, and design complexity [6]–[12]. However, leakage power consumption will become the key system design parameter for this technology. Therefore, this brief approaches a design methodology to solve the leakage problem at its root. That is, reduce the transistor count; thus, the source of leakage. To achieve this objective, the ADC must be

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