A 79 GHz Phase-Modulated 4 GHz-BW CW Radar Transmitter in 28 nm CMOS

Vito Giannini, *Senior Member, IEEE*, Davide Guermandi, Qixian Shi, Alaa Medra, Wim Van Thillo, *Member, IEEE*, André Bourdoux, *Member, IEEE*, and Piet Wambacq, *Member, IEEE*

***Abstract*—Millimeter-wave sensors perform robust and accurate remote motion sensing. We propose a 28 nm CMOS Radar TX that modulates a 79 GHz carrier with a 2 Gsps Pseudo-Noise sequence. The measured modulated output power at 79 GHz in 4 GHz BW is higher than +11 dBm (27°C), while the spurious emissions are below −20 dBc, fully satisfying the spectral mask regulations. The output RF BW where we can lock the injection-locked LO is 13 GHz. Overall, the TX draws 121 mW from a 0.9 V supply resulting in a record efficiency above 10%. More importantly, the TX is functional up to 125 °C still providing more than +7 dBm output power over the same RF BW.**

***Index Terms*—Automotive, CW, domotics, harmonic rejection, injection-locked oscillator, millimeter wave, MIMO, phase modulation, power amplifier, radar, robotics, short-range radars (SRR), temperature measurements, transmitter, 79 GHz.**

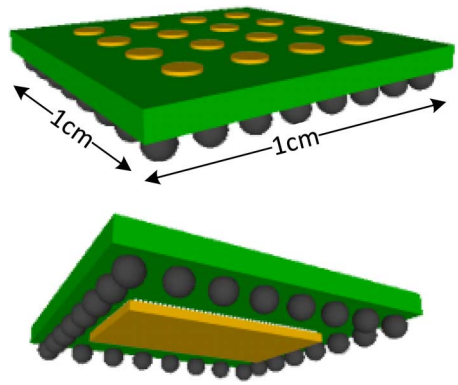


Fig. 1. 3D artist impression of a 4RX+4TX MIMO radar with fully integrated transceiver SoC flip-chipped on the back of the antenna board featuring a size of 1 cm^2.

I. Introduction

MILLIMETER wave (mm-wave) radar sensors detect presence, position, direction and relative speed of remote objects with short latencies. Historically, such systems have been employed in low-volume applications but, if we could integrate them in a smaller form factor, a whole range of new applications could take advantage of their unique properties such as their robustness against bad weather conditions and harsh environments. Fig. 1 shows an artist impression of the system we envision: a MIMO radar transceiver is fully integrated with a digital processor and packaged together with the antennas in a compact package.

The biggest driving force behind such developments is the automotive industry: 77/79 GHz radar will soon enable emergency braking systems in every car [1]. Current state-of-the-art relies on multi-chip SiGe building blocks combined with advanced packaging technologies [2], [3]. However, there is an increasing demand for higher integration levels at reduced power consumption and bill of materials. We believe that CMOS technologies could provide important advantages in this context. Several attempts at integrating CMOS based 24/77/79 GHz radars were reported in the last few years [4]–[10] but the main challenge still remains the capability to satisfy the radar application requirements in combination with the automotive temperature and reliability constraints.

In this paper, we focus on the application requirements that allow person detection over a range of 30 m, so-called short-range radars [1]: a bandwidth higher than 1.5 GHz is needed to achieve finer than 10 cm depth resolution. In classical FMCW radars [3], [7], when bandwidth requirements exceed 1 GHz, depth resolution is eventually limited by the linearity of the frequency slope of the FM PLL. Wide field of view combined with high angular resolution are also required, which at mm-Waves translate in large and power hungry antenna arrays [11].

We propose a Phase-Modulated Continuous Wave (PMCW) Radar TX that operates in the 79 GHz band. With a sampling rate of 2 Gsps and 4 GHz RF bandwidth, we target a resolution of 75 mm. Such radar architecture is digital intensive so that a nanoscale CMOS technology allows for a more power efficient implementation compared to equivalent SiGe state-of-the-art [12]. Furthermore, an increased digital content allows the radar to be self-adaptive and therefore more robust. This work proposes the first 79 GHz radar TX implemented in a 28 nm CMOS technology and is an extension of what was reported in [13].

The paper is organized as follows: in Section II we discuss the system design of the PMCW radar, translating the application requirements into RF specifications. Section III describes the transmitter architecture and discusses challenges and solutions for each building block. Finally, we present extensive measurement results in Section IV. Temperature measurements up to 125 °C are also reported.

Manuscript received April 21, 2014; revised July 08, 2014; accepted August 23, 2014. This paper was approved by Guest Editor Carlo Samori.

V. Giannini, D. Guermandi, W. Van Thillo, and A. Bourdoux are with imec, 3001 Leuven, Belgium (e-mail: vito.giannini@ieee.org).

Q. Shi, A. Medra, and P. Wambacq are with imec, 3001 Leuven, Belgium. They are also with Vrije Universiteit Brussel, Department of Electronics and Informatics (ETRO), B-1050 Brussels, Belgium.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2014.2355819

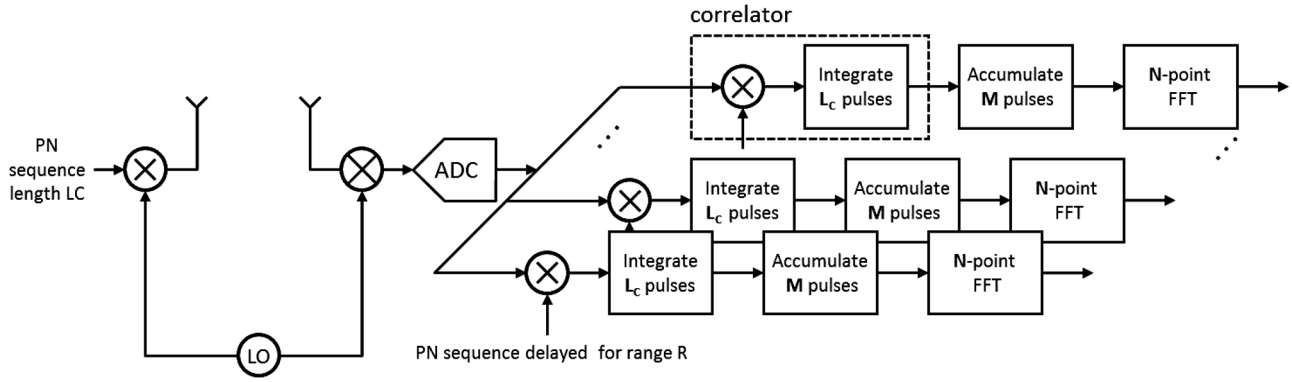


Fig. 2. Considered PMCW radar system model.

II. System Design

The waveform of a PMCW radar [14] is a sequence of binary symbols, often called pseudo noise (PN), that are mapped onto 0 and 180 degree phase shifts of a continuous radio frequency (RF) carrier (we only consider bi-phase modulation). Once a proper PN sequence has been chosen, PMCW has attractive properties both for radar performance and implementation simplicity. First, PMCW has a very sharp, thumbtack-like ambiguity function which implies no range-Doppler ambiguity. Second, multiple-input-multiple-output (MIMO) radar can be implemented in the code domain, which results in a higher angular resolution for a given number of antenna paths. Regarding implementation simplicity, PMCW neither requires a high-speed, fast settling frequency synthesizer nor does it need the synthesizer's slope to be highly linear as in FMCW radars [8]. One final advantage is that it is very easy to embed information such as a car identification number into the PMCW radar signal.

On the other hand, one major disadvantage of wideband PMCW radars is that their baseband bandwidth is large: it always equals half the RF bandwidth, in contrast to FMCW systems where the IF bandwidth can be controlled by the slope of the frequency modulation. The wide bandwidth entails two implementation challenges: high-speed ADCs are required and higher noise levels need to be mitigated. The PMCW system under consideration requires a sampling rate of at least 2 Gsps in the ADCs. To keep power consumption acceptable, it is thus mandatory to keep the resolution of these ADCs as low as possible. In [15], it is shown that a 4-bit ADCs entail no performance degradation for typical short-range pedestrian detection scenarios. These speed and resolution requirements can be met at low power consumption in nanometer CMOS implementations [16]. The higher noise levels can be mitigated by processing gain in the digital signal processing (DSP) section of the radar. To illustrate how this processing gain is achieved, we introduce the basic DSP functionality followed by a link budget calculation in the following sections.

A. Processing Gain in PMCW Radar

The equivalent system level block diagram of the 79 GHz PMCW radar under consideration is illustrated in Fig. 2. Only the main receiver processing blocks are illustrated:

- Correlator: to perform the ranging, the signal is correlated in a bank of correlators, similar to positioning systems such as the Global Positioning System (GPS). We assume that the correlator spacing is equal to the range resolution. Because all correlators operate in parallel in the digital domain, there is no theoretical limit on the number of targets that can be detected concurrently. Therefore we do not need to make assumptions on this number, and the link budget calculation in the next section is performed for one single target.
- Coherent accumulator: to increase the SNR, M correlator outputs are coherently accumulated in the accumulator.
- N-point FFT: to extract the Doppler-domain information, each range gate is processed with an FFT engine. All these engines run in parallel so that there is no limitation on the number of targets that can be detected concurrently.

The total dwell time T_d is then given by

$$T_d = T_c \cdot L_c \cdot M \cdot N \tag{1}$$

where $T_c = 1/R_c = 0.5$ ns is the chip duration and L_c the code length.

The chip rate R_c is chosen as high as possible to achieve the finest range resolution R_{res} achievable according to

$$R_{\mathrm{res}} = \frac{c}{2R_c}. \tag{2}$$

The radar unambiguous range $R_{\max}$ is given by

$$R_{\max} = \frac{c}{2\mathrm{PRF}} = \frac{cL_c}{2R_c} \tag{3}$$

where $\mathrm{PRF} = R_c/L_c$ is the pulse repetition frequency. We target an unambiguous range larger than 30 m, so we need to choose $L_c > 400$. For this work, we choose $L_c = 1000$.

For person detection we target a velocity resolution $v_{\mathrm{res}} \approx 0.25$ m/s. This corresponds to a dwell time of approximately $T_d \approx 10$ ms by virtue of

$$v_{\mathrm{res}} = \frac{\lambda_c}{2T_d} \tag{4}$$

where $\lambda_c = c/F_c = 3.8$ mm is the wavelength of the 79 GHz carrier. In this dwell time, a range bin of 75 mm can be crossed

TABLE I
SYSTEM PARAMETERS FOR THE PMCW RADAR

Parameter	Symbol	Value	Unit
Carrier frequency	F_c	79	GHz
Chip rate	R_c	2	Gsps
Range resolution	R_{res}	75	mm
Sequence length	L_c	1000	chips
Unambiguous range	R_{max}	37.5	m
Number of coherent accumulations	M	150	
FFT size	N	128	bins
Max. unambiguous velocity	v_{max}	12.97	m/s
Velocity resolution	v_{res}	0.20	m/s

TABLE II
LINK BUDGET ANALYSIS FOR THE 79 GHZ PERSON-DETECTION PMCW RADAR. HIGH DIGITAL PROCESSING GAIN IS ESSENTIAL TO CLOSE THE LINK BUDGET

Parameter	Symbol	Value	Unit
Transmit power	P_T	10	dBm
Antenna gain (single-antenna)	G_T, G_R	0	dBi
Target RCS	σ	-8	dBsm
Path loss	$\lambda_c^2/\left[(4\pi)^3\ R^4\right]$	-141	dB
Received power	P_R	-139	dBm
Noise power at Rx output	P_N	-72	dBm
Processing gain	$G_{\text{post-FFT}}$	73	dB
Single-antenna SNR	SNR	6	dB

by a target traveling at $v_{\max} \approx 7.5$ m/s, which is therefore the maximum observable Doppler speed. Combining the Doppler resolution with maximum Doppler speed and rounding up to the nearest power of 2 for efficient hardware implementation yields an FFT size of

$$N = 2^{\lceil \log_2 \frac{2v_{\max}}{v_{\text{res}}} \rceil} = 128 \tag{5}$$

where the factor 2 takes into account positive and negative velocities with respect to the radar. From $T_c = 0.5$ ns, $N = 128$, $L_C = 1000$, $T_d \approx 10$ ms and (1), we derive that $M \approx 156.25$. Choosing $M = 150$ and calculating back yields the final, exact values $T_d = 9.375$ ms, $v_{\text{res}} = 0.20$ m/s and $v_{\max} = 12.97$ m/s. The velocity resolution will in practice be slightly degraded due to FFT windowing, an effect that is not taken into account in this paper. Table I summarizes the main system parameters.

All three DSP operations described above (correlation, accumulation and FFT) provide processing gain by adding signals coherently while noise combines non-coherently. The processing gain before the FFT is given by

$$G_{\text{pre-FFT}} = 10 \log_{10}(L_C M) = 52 \text{ dB} \tag{6}$$

whereas the processing gain of the FFT processing equals

$$G_{\text{FFT}} = 10 \log_{10}(N) = 21 \text{ dB} \tag{7}$$

making the total processing gain after the FFT equal to

$$G_{\text{post-FFT}} = G_{\text{pre-FFT}} + G_{\text{FFT}} = 73 \text{ dB}. \tag{8}$$

Note that it is possible to further integrate non-coherently to further increase the processing gain. As we will see in the next section, this digital processing gain is essential to close the link budget of the envisaged radar system.

B. Link Budget Analysis

To assess signal and noise levels throughout the system, we perform a link budget analysis based on the radar equation:

$$P_R = \frac{P_T G_T G_R \lambda_c^2 \sigma}{(4\pi)^3 R^4} \tag{9}$$

where P_R is the received signal power, P_T is the transmitted power, G_T and G_R are transmit and receive antenna gain, σ is the target radar cross section (RCS) and R is the target range. We design for $P_T = 10$ dBm and assume $G_T = G_R = 0$ dB because we envisage antennas with wide field of view and incorporate antenna feed losses in this factor. As we design for person detection, we set $\sigma = -8$ dBsm [17] and a maximum range $R = 30$ m. Given these parameters, the received power can be as small as $P_R = -139$ dBm for a single-antenna system.

Thermal noise power in the 4 GHz wide band (occupied by the unfiltered 2 Gsps sequence) at the output of a receiver with noise figure (NF) of 10 dB (5 dB LNA [18] and including the antenna feed losses) is approximately -72 dBm, or 67 dB higher than the signal level. Table II summarizes the link budget analysis.

These numbers clearly indicate the need for a high digital processing gain and multiple-antenna systems, either in phased-array or MIMO radar configuration. PMCW radars are thus digital-intensive systems, well suited for CMOS implementation. In the next section we show that PMCW waveforms are also compatible with current 79 GHz spectral regulations.

III. TRANSMITTER ARCHITECTURE AND BUILDING BLOCKS

Fig. 3 shows the block diagram of the proposed radar TX. To minimize the implementation complexity and maximize the TX power efficiency, we choose a PN sequence of unfiltered square chips. Such a waveform at rate $R_c = 2$ Gsps occupies an RF bandwidth of 4 GHz, which is the maximum allowed by the ETSI spectral mask [19] and which yields a resolution $R_{\text{res}} = 75$ mm.

Unfortunately, by using unfiltered square chips we would also generate large side-lobes, which do not comply with the spectral requirements [1] when transmitting at the maximum allowed EIRP of -3 dBm/MHz. Fig. 4 shows the power spectral density (PSD) of an unfiltered 2 Gsps PMCW waveform: such spectrum is centered around 79 GHz with spectral components every Rc/Lc. Assuming +10 dBm power in the main lobe and 9 dB antenna gain, this waveform could be emitted by a 2-antenna phased-array radar transmitter with one 10 dBm PA for each

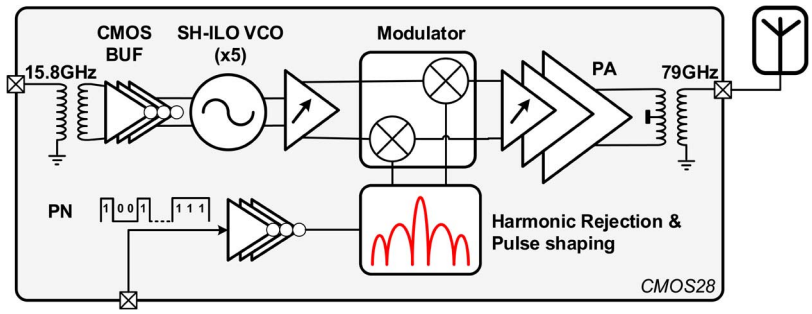


Fig. 3. Block diagram of the proposed phase-modulated radar.

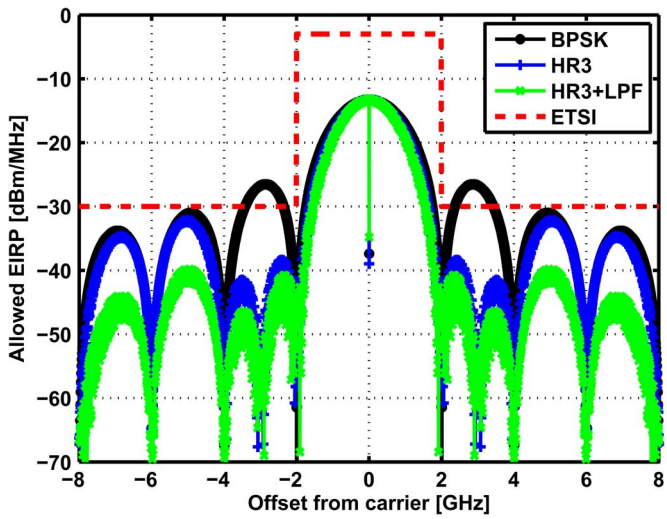


Fig. 4. Spectral mask for the 79 GHz band imposed by ETSI (red) and a typical 2 Gsps PMCW waveform PSD for a +10 dBm PA, 2-antenna, +3dBi antennas (black). Also shown how to prevent violation of the spectral mask by applying the side-lobe suppression technique proposed in this paper (green and blue).

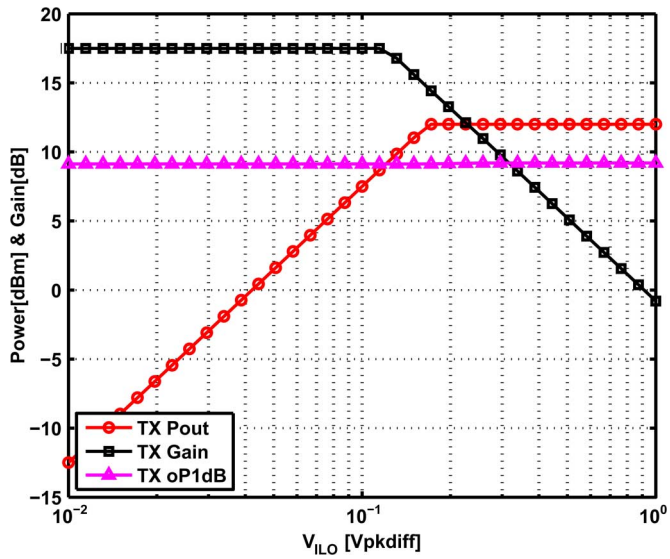


Fig. 5. TX cascade analysis.

antenna and 3 dBi antenna element gain. Even for this system with few antennas and low antenna gain, the sidelobes of the unfiltered PMCW signal, approximately 13 dB lower than the main lobe, clearly violate the spectral mask (black in Fig. 4)

Differently from [2], [12], we solve this problem by rejecting the closest side-lobe and by filtering the others. This is discussed in detail in Section III-B. Overall, this lowers the out-of-band emissions and allows to maximize EIRP. Fig. 4 shows a matlab simulation with the expected PSD shaped by 3rd order harmonic rejection (HR3) as well as the one that combines both HR3 and filtering (HR3+LPF).

Fig. 3 also shows how we generate the 79 GHz carrier frequency. A 15.8 GHz input is multiplied by 5 by a Sub-Harmonically Injection Locked Oscillator (SH-ILO) (Section III-B). We have demonstrated that a 15.8 GHz integer-N PLL with a phase noise of −94 dBc/Hz at 1 MHz offset will be sufficient to cope with the required system specification [20]. After amplification, the 79 GHz SH-ILO output is fed into the RF modulator, which multiplies the signal with the PRN sequence. Finally, the modulated signal goes through a 3-stage power amplifier (Section III-C).

In order to verify the TX system performance and distribute gain, linearity and noise specs over the different RF blocks, we performed cascade analysis simulations. Fig. 5 shows the results detailing the TX output compression point (oP1dB), the signal power and the gain for a range of possible SH-ILO voltage output V_{ILO}. In order to provide sufficient robustness, the TX will need to deliver the required output power over all temperature and process corners: this is achieved by implementing a wide range of gain control in all TX amplifying stages.

Table III shows a possible specification distribution on each TX sub-block used in Fig. 3. As evident from such simulations, we plan to exploit the constant envelope of our phase-modulated signal by transmitting at the PA saturated power for maximizing both output power and energy efficiency.

A. The Sub-Harmonically Injection-Locked Oscillator

The LO strategy and frequency planning require careful consideration to minimize the power consumption and system complexity of phased-array millimeter wave transceivers. Sub-harmonic frequency generation is a popular choice in literature [21]–[23]. One of the key advantages of this approach is that ILOs can be designed to have a wide tuning range without trading it off with phase-noise, the latter being fully dependent on the injected signal in locking conditions. In this work, we make the following choices to fully exploit the benefits of our nanoscale digital technology:

- we choose a 5th order SH-ILO;

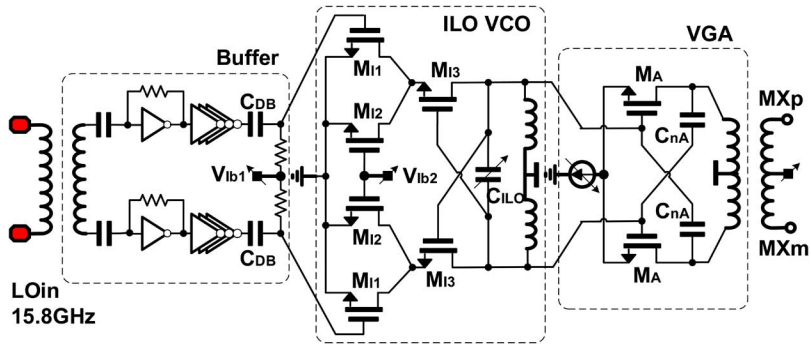


Fig. 6. Schematic of the sub-harmonically injection-locked-oscillator and programmable buffer.

TABLE III
TRANSMITTER CASCADE ANALYSIS AND SPECIFICATIONS

	Gv [dB]	oP1dB [dBm]	Pout [dBm]	Vout [Vpkdif]
SH-ILO				0.25 to 0.5
ILO-Buffer	0 to 4	9	-2.5	0.4 to 0.75
Modulator	-3 to 2	9	-0.5	0.8 to 1
3-stage PA	12.5	10	12	1.2
TX	6 to 18.5	9	12	1.2

- we use simple CMOS inverters to generate a harmonic rich square wave;
- we trade amplitude for locking range where needed.

Fig. 6 shows the detailed schematic of the local oscillator section [24]: it is made of a 15.8 GHz differential input buffer stage, the core 5th order SH-ILO and a programmable gain amplifier.

Compared to a direct 79 GHz LO generation, using a 5th order SH-ILO requires a simpler 15.8 GHz integer-N PLL and reduces the LO distribution cost and complexity. On the other hand, as the harmonic energy unavoidably decreases with increasing frequency, more amplifying stages would be typically required to provide a given signal swing as the multiplication factor is increased, which drives up power consumption. The locking range [25] is indeed given by

$$\omega_{\mathrm{lock}} = \omega_{\mathrm{osc}} \cdot \frac{I_{\mathrm{inj}}}{2 \times Q \times I_{\mathrm{osc}}} \tag{10}$$

where ω_{osc} is the self-resonance frequency, Q is the quality factor of the resonance tank, I_{inj} is the injected current and I_{osc} is the steady-state current of the oscillator. For a wide locking range, a large injection current is clearly needed.

In classical SH-ILO, inductive-peaking buffers are widely used but they result in both large area and power consumption. Also, they require a nonlinear core ILO transistor biased in weak inversion, which is too large to be efficiently driven [26], [27]. As shown in Fig. 6, we rely on simple CMOS inverters to generate a harmonic rich square wave at 15.8 GHz. Pseudo-differential inverter chains work as harmonic generators and input buffers and the 28 nm CMOS process makes it possible to push the operating frequency of inverters up to 16 GHz. The first stage is self-biased with a 20 kΩ resistor. The remaining three cascaded stages enhance the strength of the harmonics. Compared to the use of tuned amplifiers as buffers, the fundamental signal swing is limited by the supply voltage which weakens the direct mechanism of harmonic generation. Nevertheless, other harmonics contribute through intermodulation and direct amplification. As long as the phases of these components are aligned, the sum of desired harmonics increases. Additionally, an inverter chain based buffer has a better reliability than an inductive peaking buffer thanks to the limited voltage swing and there is no risk of bad tuning of a bandpass circuitry.

Fig. 7 shows the two mechanisms on the SH-ILO input transistors M_{I1} which ensure a wide-locking range on the 5th harmonic: the linear behavior amplifies the 5th harmonic of the input square wave (M_{I1} is a cascode amplifier) whereas the nonlinear behavior contributes to further increase the 5th order component also through 3rd order intermodulation between the fundamental and the 3rd harmonic (M_{I1} is an harmonic generator). We analyzed the harmonic generation of an inverter chain based SH-ILO by considering half of the differential ILO core for PSS simulations. To keep the same startup current, both bias voltage and transistor size are kept constant. For a rail to rail square wave input at 15.8 GHz, the amplitude and phase (referred to the input) of the 5th harmonic are detailed in Table IV. As expected, the 5th harmonic generated by HD_5 is weak. But extra components come from the 3rd order intermodulation product that combines the fundamental signal with the third harmonic, which in case of an inverter chain in 28 nm CMOS, is quite strong. Besides the nonlinear mechanisms, the linear amplification through the coupling transistor (M_{I1}) further increases the 5th harmonic by 40%. When more harmonics are taken into account, the final value is 0.91 mA which means the three aforementioned mechanisms dominate the 5th harmonic generation as Fig. 7 indicates. The overall SH-ILO topology is shown in Fig. 6. The Q of the inductor is 15 and the Q of the varactor ranges from 8.5 to 20, both at 79 GHz. M_{I1} needs to be carefully biased: a too low $\mathrm{V_{Ib1}}$ reduces the $\mathrm{f_T}$ which degrades the linear mechanism. Also, transistors in weaker inversion require larger finger width to maintain the startup current. This increases the load of the inverter chain and results in a higher dynamic power. The output phase difference between the different mechanisms is critical for a constructive summing. The phase simulation results in Table IV suggests that the variation of the output

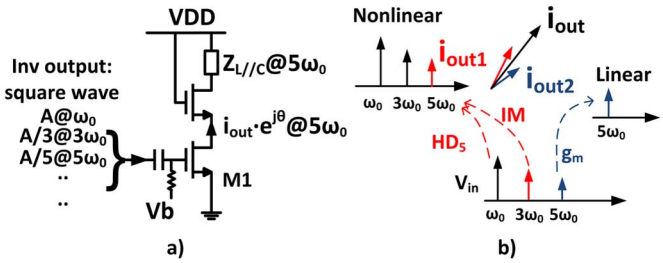


Fig. 7. (a) Test circuits for proposed SH-ILO. (b) Phasor diagram.

TABLE IV
OUTPUT CURRENT AND PHASE AT $5\omega_0$

Input	i_{out}	θ
ω_0	0.31	148.6°
$\omega_0 + 3\omega_0$	0.58	148.7°
$\omega_0 + 3\omega_0 + 5\omega_0$	0.82	143.8°
up to $15\omega_0$	0.91	145.1°

phase over different fifth-harmonic generation mechanisms is less than 5°.

Another interesting feature of the proposed SH-ILO is that it can trade output voltage swing for locking range. As shown in Fig. 6, we make this possible by shunting transistor M_{I2} with s tunable V_{Ib2}: when V_{Ib2} is high the I_{osc} increases which enhances the output voltage swing without changing the optimal bias voltage of M_{I1}. Simulations show that the swing at the output of the differential buffer is 0.55 V and 0.75 V when V_{Ib2} is 0 V and 0.55 V, respectively. On the other hand, the locking range is reduced, apart from the increase of I_{osc}, the fifth-harmonic output current generated from M_{I1} is partially bypassed through the drain of M_{I2}. When a wide locking range is required, V_{Ib2} must be low.

The inverter chain, the SH-ILO core and the buffer consume 9 mA, 10 mA, and 9 mA, respectively, from a 0.9 V supply voltage.

B. The Phase Modulator

In an ideal PMCW radar, the high frequency carrier must be phase-modulated by the PN sequence and therefore the output is a sine wave with phase either 0° or 180°. The instantaneous phase jumps introduce discontinuities in the time-domain waveform, which translate in a very wideband output spectrum (BPSK shown in Fig. 4 for a 2 Gbps PN sequence). Since the side-lobes peaks (power) decrease as $[sin(x)/x]^2$, their amplitude with respect to the main lobe can be computed in dB as

$$AL_{\mathrm{dB}}(n) = -20 \cdot \log\left[\frac{2}{(\pi \cdot (2n+1))}\right]. \qquad (11)$$

That means −13.4 dB and −17.9 dB for the 1st and the 2nd side-lobe, respectively, which violate the ETSI spectral mask (Fig. 4). In order to comply with regulations without decreasing the peak transmitted power and with sufficient margin over temperature and corners, the side-lobes need to be strongly reduced.

A possible solution would be to remove side-lobes by using RF band-pass filters. To achieve sufficient suppression of the side lobes, such filter requires an order higher than 2 which translates in a quality factor of about 20 at 79 GHz. Unfortunately, realizing such a bandpass filter with a good control of the center frequency and the bandwidth is not possible in a standard CMOS technology. Another potential option would be to remove the higher harmonic content of the baseband signal *before* modulating it. This can be achieved with filters on the baseband signal, that would smoothly shape the 0° to 180° phase transition. Various solutions have been proposed to achieve different types of pulse shaping both in the analog [28] as well as in the digital domain by simply oversampling the PN sequence. In general, filters are effective in reducing the far away side lobes, whereas they achieve poor attenuation with the close-by side-lobes.

A viable alternative is Harmonic Rejection (HR) which is an elegant technique widely used in broadband radios, such as Cable TV receivers [29] or software defined radios [30], to reject the LO harmonics during the mixing operation. In classical HR, the input signal is multiplied with delayed and weighted copies of the LO in different sub-mixers: by properly choosing and implementing such delays and weights, the summation of the sub-mixers outputs result in a signal with lower harmonic content. The accuracy of the rejection depends on the maximum achievable phase/gain mismatch and the complexity of such systems grows exponentially with the harmonic order to be canceled.

In this work, we reduce the BPSK side-lobes by combining a 3rd order HR technique to reject close-by side-lobes while we rely on a 1st order programmable pulse shaping to filter out the higher order harmonic content. The optimal bandwidth of the filter is determined by matlab simulations: there is a trade-off between the attenuation of the sidelobes and the reduction of the power in the main side lobe. A bandwidth of about 2 GHz (equal to the bit rate) was chosen as the best trade-off. Compared to a standard LO driving a mixer, PRN transitions do not happen at every clock period and we observe a very limited impact on the TX spectral re-growth. This solution allows to comply with the spectral mask with margin while keeping the modulator as simple as possible, which is especially critical when running at 79 GHz. Differently than in classical HR, we now want to reject the high harmonic content of the baseband digital sequence: HR techniques should then be applied on the baseband signal path rather the LO.

Fig. 8 shows a block diagram of the concept that allows to reject the 3rd order side-lobes. HR requires to split the mixer in two slices, one of which must be fed by the PN sequence delayed by $1/3T_c$. Delays can implemented by means of delay lines or flip-flops and/or dividers if a clock at $3/T_c$ is avaliable whereas the weighted summation is done either in the voltage or current domain by properly scaling the gain.

A more detailed schematic of the mixer core is sketched in Fig. 9: we perform phase modulation by using a double balanced Gilbert cell with swapped LO and baseband inputs, as also done in [12]. Therefore, the input signal coming from the SH-ILO is applied to the sources of the mixer switches MMX via a transformer. A second transformer at the drains of MMX

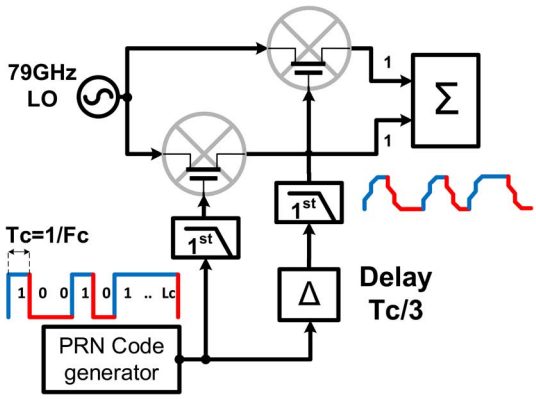


Fig. 8. Block diagram of the proposed side-lobe rejection baseband-mixer.

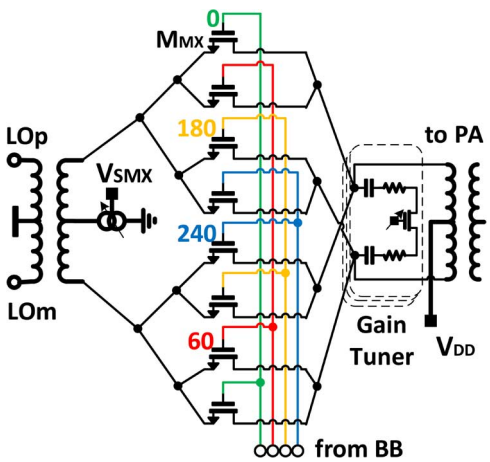


Fig. 9. High-level schematic of the harmonic rejection rejection mixer.

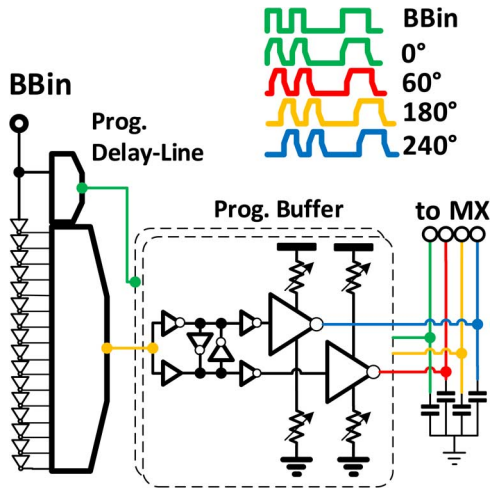


Fig. 10. High-level schematic of the programmable delay line and pulse-shaper baseband.

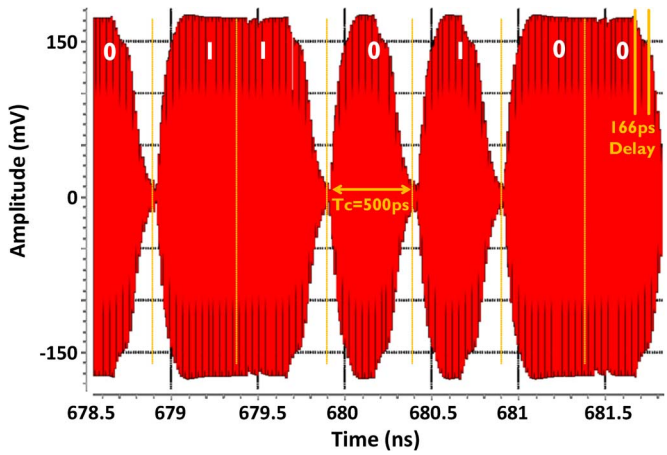


Fig. 11. Time-domain spectre simulation of the implemented HR3 technique running with at a chip rate $R_c = 2$ Gsps which correspond to a symbol period $T_c = 500$ ps. The envelope looks smoother than a standard BPSK modulation. More interestingly, it is possible to observe the 166 ps delay in the smooth envelope variation.

collects the output current and transfers it to the PA. The current in the switching pairs is controlled by a current DAC driven by the voltage V_{SMX}, allowing to make the mixer operate also in passive mode trading current consumption for gain. The mixer is split in two parallel paths: each of them is fed by one of the four different baseband phases.

The four phases are generated at baseband by properly handling the incoming PN sequence. Since a clock running at three times R_c is not available, the 1/3 of the chip period (166 ps) is realized with a delay line made of simple inverters (Fig. 10). The delay can be tuned to the desired value by a DLL, for example using a cascade of 3 of them and locking their total delay to the bit rate R_c, or by selecting by means of multiplexer the inverters outputs of the chain that maximizes the rejection. For simplicity, the latter option has been chosen for the first silicon implementation. The delay accuracy/step is given by the delay of two inverters which is less than 20 ps in a 28 nm CMOS technology.

As shown in Fig. 10, the remaining high-order side-lobes are attenuated by means of analog filtering. A first order analog filter (RC) is easily implemented in a passive form, that is also more linear and less noisy than implementation in active forms. In a CMOS realization, filtering can be conveniently implemented by slowing the final CMOS stages that drive the switches by means of a (programmable) degeneration.

Fig. 11 shows the time domain output of the modulator: differently than in an ideal BPSK, there is a smooth transition between the 0° and 180° phase. This slows the phase transition and reduces the harmonic content of the output signal. The modulator provides a simulated voltage gain up to 2 dB that can be lowered by means of a programmable resistor at the high impedance output (Fig. 9).

C. *The Power Amplifier*

The PA consists of three CS push-pull stages, two of which are shown in Fig. 12. We target 1 Vpeak on the 50 Ω antennas load (+10 dBm), which ideally requires 20 mA output current. We use a 1:1 output balun to minimize the losses, and size the PA transistors M_2 loaded by 25 Ω differential impedance. With a width of 120 μm and minimum length, the transistors M_2 are laid out using a serial gate feed strategy as in [31] with a finger width of 1 μm. M_2 is biased in class A in such a way that the DC drain current is about 28 mA, which allows sufficient margin to cope with the balun losses. The capacitor C_n, stabilizes the

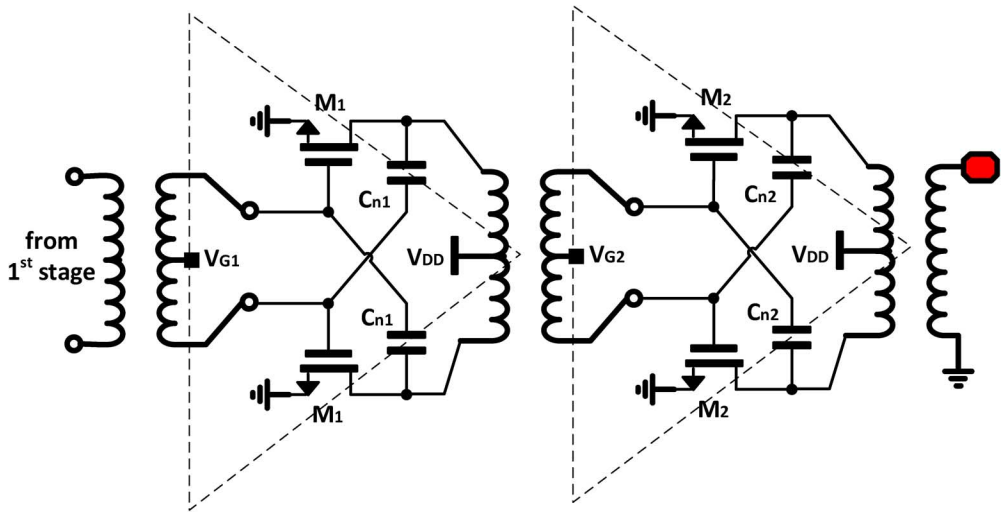


Fig. 12. Schematic of the last two CS push-pull PA stages.

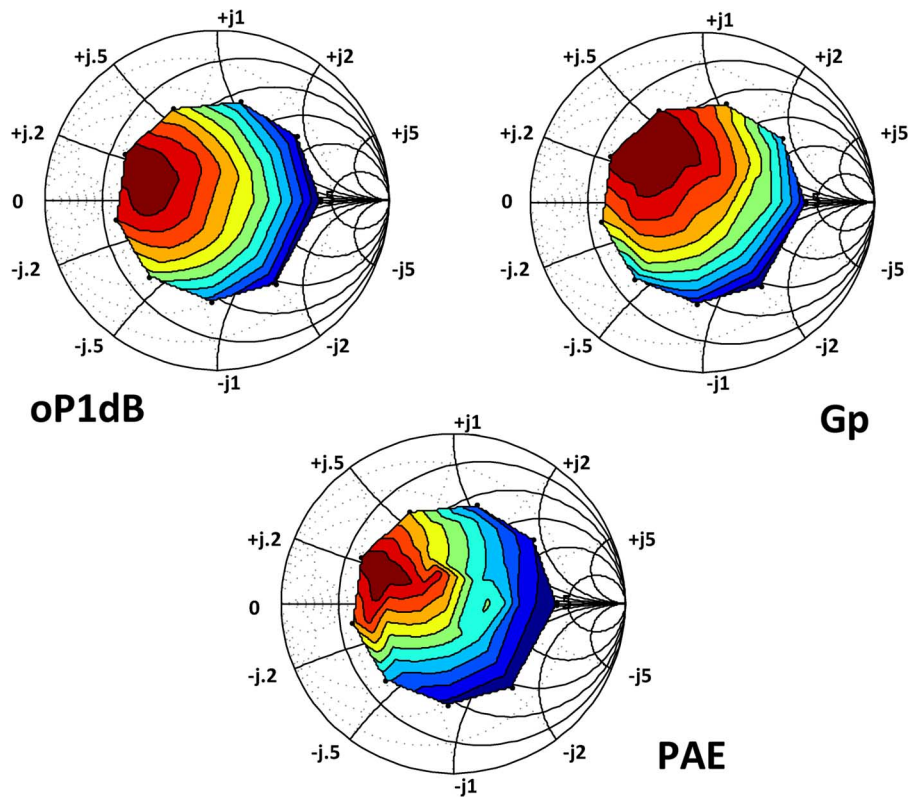


Fig. 13. Load pull were performed from the extracted view. The power contours provide the optimal balun impedance selection.

PA over the required frequency range. Fig. 13 shows the power contours generated from load-pull simulations on the extracted view of the neutralized PA transistor M_2. Interestingly, neutralization allows to overlap the optimal loading impedance regions and maximize at the same time output compression, power gain and efficiency, which would otherwise require different loading conditions. The output balun is then designed to achieve such an optimal impedance as well as maximize the output bandwidth for increased robustness over corners and temperature. The output transformer is designed using a center tapped octagonal topology, which achieves a simulated Q of 16 and 12 (respectively for primary and secondary) and coupling K of about 0.7. Two pre-amplifying stages with similar topologies precede the PA and provide further power gain. Overall, the simulated PA shows more than $+9$ dBm output P1dB, +12 dBm saturated power and 17% PAE.

IV. Measurement Results

We fabricated a few prototypes and test structures in a 28 nm HPM CMOS technology with a 0.9 V supply voltage. RF models were fully characterized to provide sufficient frequency and noise accuracy. We hereby report measurement results

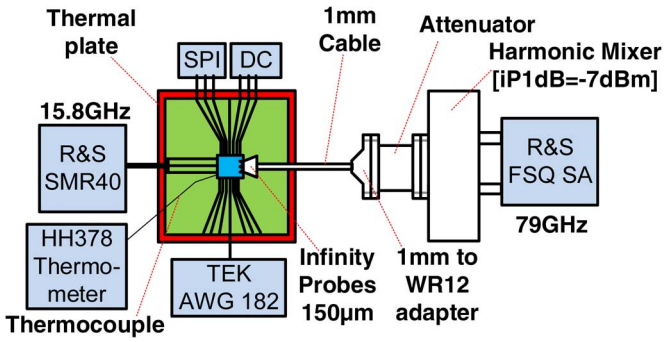


Fig. 14. Drawing of measurement setup.

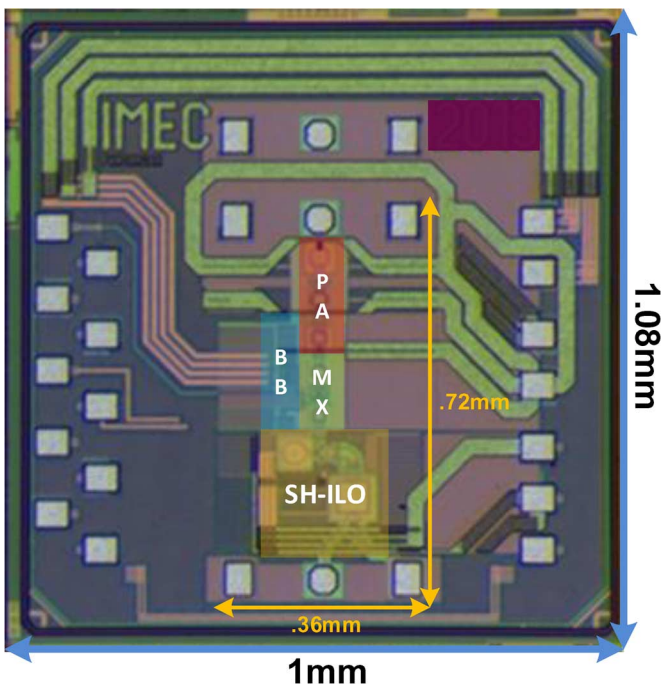


Fig. 15. TX chip micrograph.

on the overall transmitter. As shown in Fig. 14, the DUT is mounted on a test PCB with bond-wired DC supplies and serial programming interface (SPI) lines. The RF input and outputs GSG pads (at both 15.8 GHz and 79 GHz) are probed with 150 μm pitch Cascade Infinity probe, whereas the 2 Gsps baseband PN sequence is provided through a bond wired connection from an AWG. Temperature measurements are also performed by mouting the PCB on a thermal plate and a thermochuck to increase temperature up to 125 °C and by measuring the on-chip temperature with a thermo-couple.

The TX chip micrograph is shown in Fig. 15 with a core area of about 0.26 mm^2 including RF pads and decoupling. The prototype consumes a total 121 mW (25 mW SH-ILO, 1 mW baseband at 2 Gsps, 3 mW modulator, 92 mW 3-stage PA) which appears constant over several samples. The TX output signal at 79 GHz is measured by means of an harmonic mixer (FS-Z90) from a spectrum analyzer (FSU-67).

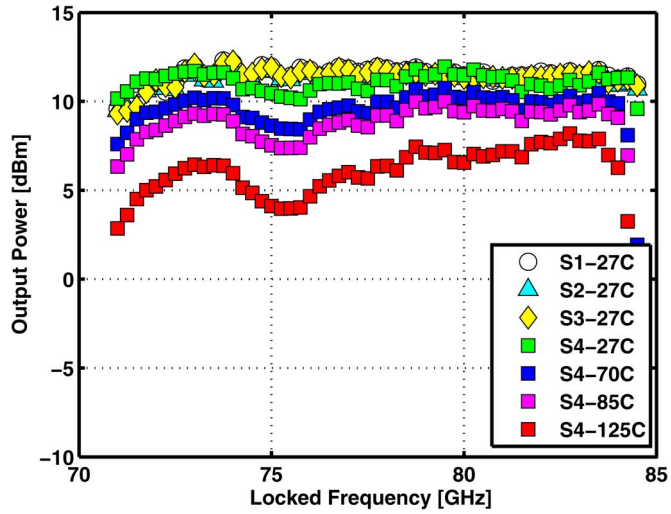


Fig. 16. TX output power versus ILO locked range over 4 different samples and temperature.

A. Chip Measurements

First of all, the chip output power and the setup losses were fully characterized using respectively power sensors and S-parameter measurements with a 67 GHz PNA with 110 GHz extension. The SH-ILO has a locking range of 5 GHz around 79 GHz. By tuning its capacitor bank C_{ILO}, we can always lock the SH-ILO when an input LO frequency between 14.2 GHz and 16.8 GHz is applied through a signal generator. Fig. 16 shows the TX output power versus the SH-ILO locked frequency for four different samples. The measurement is performed for different samples and (for sample 4) at different temperatures. The up-converted RF bandwidth is always higher than 13 GHz and centered around 78 GHz. This allows robust operation in both the 79 GHz and 77 GHz bands. Within this band, the output power is higher than +11 dBm. The RF frequency range is not affected even by the highest operating temperature (125 °C) whereas the maximum output power at 79 GHz drops to 7.2 dBm. We believe this is mainly due to a reduction of transconductance in the PA transistor at high temperature which translates in a drop in the overall TX gain. However, measurements on the stand-alone PA allowed to verify that the saturated power only drops by 1 dB. Such drop could be partially compensated by further trading more ILO amplitude for less locking range, as explained in Section III-A.

Fig. 17 shows that the SH-ILO phase noise follows closely the phase-noise of a R&S SMR40 input source with a 14 dB offset which also confirms that the SH-ILO is fully locked. The difference between the output at 79 GHz and the external source at 15.8 GHz matches the theoretical value of $20 \cdot \log(5)$. The measured external phase noise is flattened after 1 MHz offset due to the added phase noise from the spectrum analyzer and signal source analyzer (Agilent E5052). This makes the phase noise penalty lower than the theoretical value.

Fig. 18 shows the modulated signal centered at 79 GHz with and without the out-of-band lobe rejection for a 2 Gsps PN-sequence, 511 chips long, generated with a Tektronix 7102 arbitrary waveform generator (AWG). This sequence is brought to the PCB using a coaxial cable and onto the Tx

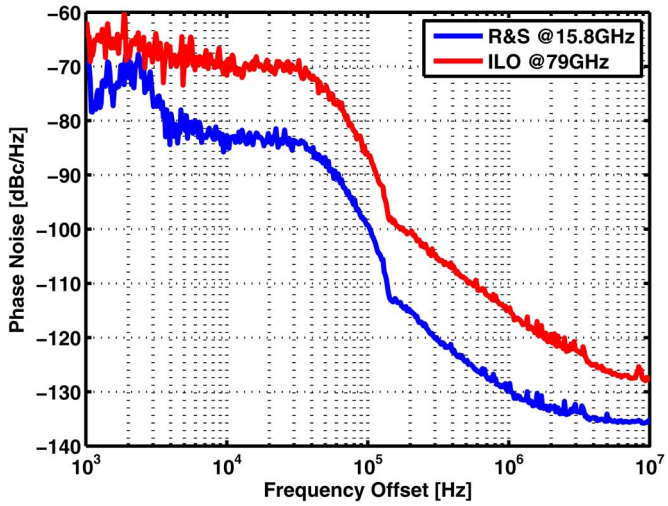


Fig. 17. Phase noise of the locked ILO and external source.

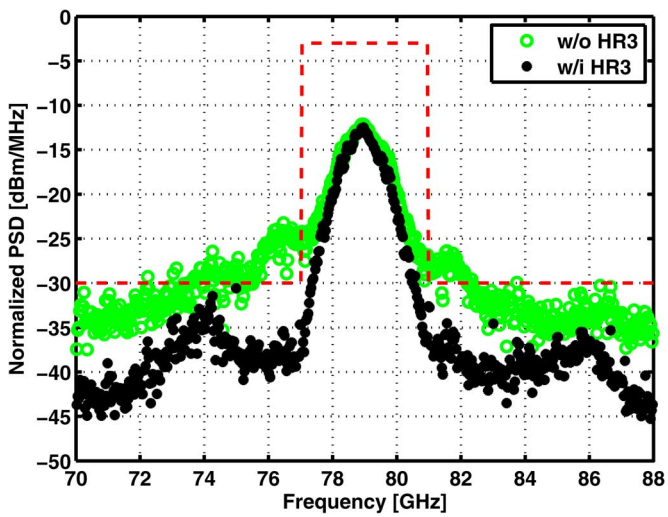


Fig. 18. 79 GHz ETSI Spectral mask and Normalized PN modulated output spectrum at $R_c = 2$ Gsps with and without side-lobe rejection and filtering.

chip with a bond wire. The integrated output power over the 4 GHz RF bandwidth is higher than +11.5 dBm. The 3rd order side-lobe drops from −13 dBc to about −25 dBc. Overall, the out-of-band emissions drop to about −20 dBc with a negligible power consumption penalty. Such results allow to comply with the spectral mask requirements even with a 4 TX code-domain MIMO system.

Similarly, Fig. 19 shows the modulated signal centered at 77 GHz with and without the out-of-band lobe rejection for a 0.5 Gsps PN-sequence.

B. System Test

To verify the end-to-end system performance, wireless tests were performed using a waveguide-based reference receiver. The setup is explained in Fig. 20. The TX chip 79 GHz output is probed and connected through 1 mm-to-WR12 adaptor to a standard horn antenna. The signal is then transmitted wirelessly through the air to the reference receiver. This receiver

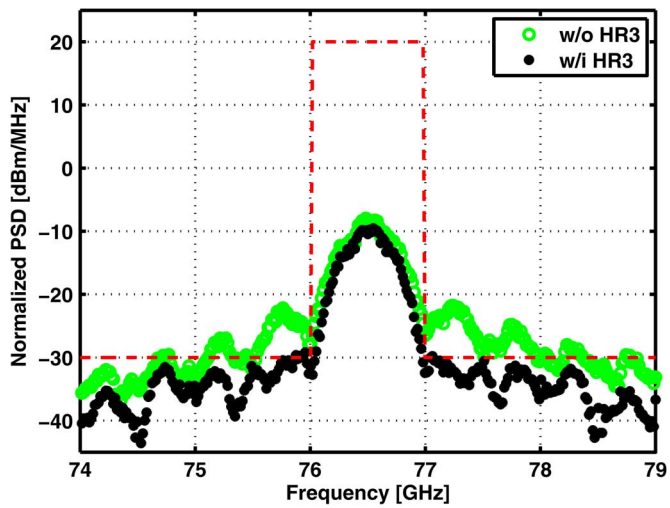


Fig. 19. 77 GHz ETSI Spectral mask and Normalized PN modulated output spectrum at $R_c = 0.5$ Gsps with and without side-lobe rejection and filtering.

is built with off-the-shelf components: standard horn, LNA, IQ downconverter and baseband amplifiers. The 15.8 GHz reference frequency is upconverted to 79 GHz using a custom-built 5× frequency multiplier to mimic the TX on-chip SH-ILO. The received baseband signal is digitized using a Tektronix 6124C real-time scope (10 Gsps and 8b) and sent to a PC for processing in Matlab.

In this setup, the radar is tested in a transmissive configuration rather than in the typical reflective configuration. In other words, the TX transmits directly into the RX, rather than illuminating a target which reflects the signal into the Rx. This transmissive setup was chosen because the setup on the probe station in the laboratory's Faraday cage did not allow to align TX and RX towards a target in an anechoic environment. Nevertheless, this transmissive setup allows to verify the correct operation of the TX chip in both time and frequency domain, which is the main purpose of this measurement.

The result of the system test is shown in Fig. 21. The X-axis shows the measured range of the target, whereas the Y-axis shows the magnitude of the received signals in dB. Two measurements were taken. First, the distance was measured in the reference position (blue curve). One clear peak is visible, with secondary echos 25 dB lower. This dynamic range is much smaller than would be expected in transmissive mode over such a small distance. This limitation is caused by all short-range reflections from the probe station and the metal of the Faraday cage in which the measurement was performed, as well as the range sidelobes of these reflections. The absolute distance of this measurement, 2.37 m, has no meaning because the code offset between TX and RX was not calibrated. For the second measurement, the reference Rx was moved 15 cm further away from the TX (red curve). This measurement yields a peak at 2.445 m, 7.5 cm further than the reference position. This is only half the actual distance increase because the signal processing assumes that the radar operates in reflective configuration, with propagation towards the target and back to the receiver. This measurement thus confirms the proper operation of the radar Tx chip.

TABLE V
STATE-OF-THE-ART IN RADAR MODULATED TRANSMITTERS. COMPARISON IS PERFORMED BY EXTRAPOLATING FROM THE CITED PAPERS THE 1-ANTENNA PATH TX MEASURED PERFORMANCE. POWER CONSUMPTION INCLUDES PA, MODULATORS, LO BUFFERS AND SH-ILO OR VCO RUNNING AT THE CARRIER FREQUENCY F_c

Ref	Tech [nm]	Vdd [V]	Radar Modulation	Mod BW [GHz]	F_c [GHz]	$P_{out,25C}$ [dBm]	$P_{out,125C}$ [dBm]	P_{dc} [mW]	TX Efficiency $P_{out,25C}/P_{dc}$ [%]
[2]	SiGe130	2.5	PMCW	2.1	24	3	n/a	80	3.3
[32]	SiGe180	2.5	n/a	n/a	79	10.5	n/a	452	2.5
[3]	SiGe180	3.3	n/a	n/a	77	16.4	14.4	1750	2.3
[12]	SiGe180	5.5	PMCW	1.24	79	1.5	n/a	4100	0.03
[4]	CMOS90	1.2	FMCW	0.2	77	6.3	n/a	660	0.6
[5]	CMOS90	1.2	FMCW	0.2	77	-2.8	n/a	406	0.13
[6]	CMOS90	1.2	Pulsed	0.2	24	0	n/a	96	1
[7]	CMOS65	1.2	FMCW	0.7	77	5.1	n/a	188	1.7
[8]	CMOS65	1.2	FMCW	1.2	62	5	n/a	89	3.5
[9]	CMOS65	2	n/a	n/a	77	10	n/a	306	3.2
[10]	CMOS65	1	n/a	n/a	79	13.5	10	420	5.3
[33]	CMOS65	1.2	Pulsed	7	160	4	n/a	350	0.7
this work	**CMOS28**	**0.9**	**PMCW**	**2**	**77/79**	**11.5**	**7.2**	**121**	**10.4**

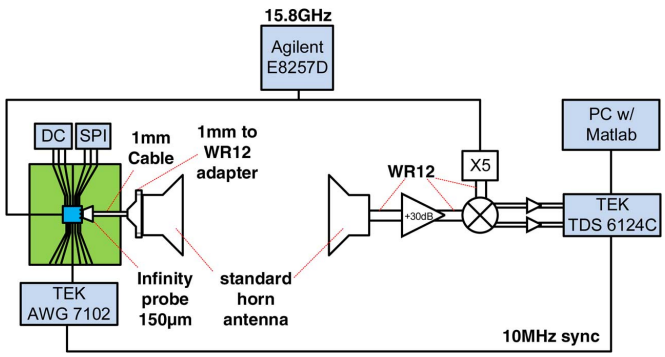


Fig. 20. Schematic representation of the wireless system test. TX and RX are aligned in a transmissive configuration because the typical reflective configuration could not be built on the probe station in the laboratory's Faraday cage.

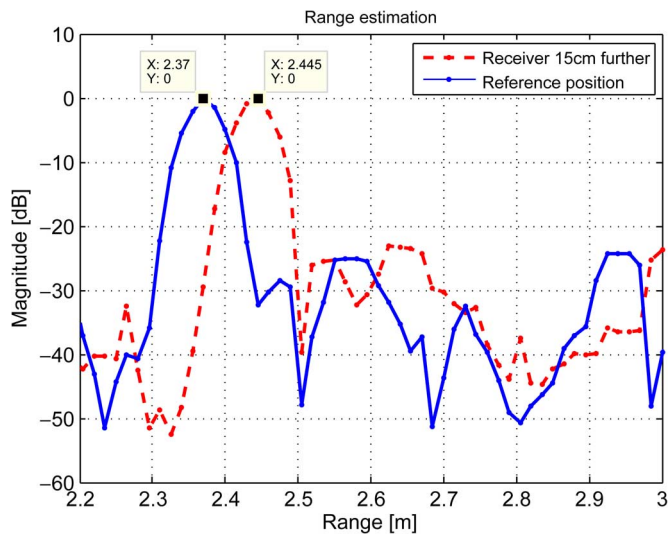


Fig. 21. Wireless system test result. The measured distance difference of 7.5 cm confirms that the Tx operates properly. The actual distance difference is 15 cm in a transmissive setup, which corresponds to 7.5 cm in the targeted reflective setup.

V. CONCLUSION

In this paper, we have described in detail a phase-modulated ETSI compliant 79 GHz radar TX. Table V shows that this work achieves at least 2 times higher bandwidth (i.e., depth resolution) compared to published FMCW TX and a power efficiency (Pout/Pdc) at least 2 times better compared to the best CMOS radar TX reported. Interestingly, compared to published SiGe implementation, the efficiency improves by a factor 5 while still achieving competitive performance at 125 °C temperature. We were able to achieve such results by leveraging the 28 nm CMOS technology and by exploiting a digital intensive architecture. Future work involves the implementation of a receiver as well as the full MIMO radar system with integrated ADCs and correlators. In this work, we have shown a first step towards high-resolution power-efficient code-domain MIMO radars operating at 79 GHz.

ACKNOWLEDGMENT

The authors thank K. Vaesen, B. Parvais, J. Craninckx, C. Soens, S. Brebels, K. Raczkowski, M. Libois, L. Pauwels, I. Ocket, the imec BODI team, INVOMEC and Integrand Software for EMX.

REFERENCES

[1] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 845–860, Mar. 2012.

[2] E. Ragonese, A. Scuderi, V. Giammello, E. Messina, and G. Palmisano, "A fully integrated 24 GHz UWB radar sensor for automotive applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 306–307.

[3] S. Trotta *et al.*, "An RCP packaged transceiver chipset for automotive LRR and SRR systems in SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 778–794, Mar. 2012.

[4] Y. Kawano, T. Suzuki, M. Sato, T. Hirose, and K. Joshin, "A 77 GHz transceiver in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 310–311.

[5] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.

[6] H. Krishnaswamy and H. Hashemi, "A 4-channel 4-beam 24-to-26 GHz spatio-temporal RAKE radar transceiver in 90 nm CMOS for vehicular radar applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2010, pp. 214–215.

[7] J. Lee, Y.-A. Li, M.-H. Hung, and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec. 2010.

[8] W. Wu, X. Bai, R. B. Staszewski, and J. R. Long, "A mm-Wave FMCW radar transmitter based on a multirate ADPLL," in *Proc. 2013 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2013, pp. 107–110.

[9] C. Kim *et al.*, "A CMOS centric 77 GHz automotive radar architecture," in *Proc. 2012 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2012, pp. 131–134.

[10] K.-H. To and V. P. Trivedi, "A 76–81 GHz transmitter with 10 dBm output power at 125 °C for automotive radar in 65 nm bulk CMOS," in *Proc. 2011 IEEE Custom Integrated Circuits Conference (CICC)*, 2011, pp. 1–4.

[11] V. Vidojkovic *et al.*, "CMOS low-power transceivers for 60GHz multi Gbit/s communications," in *Proc. 2013 IEEE Custom Integrated Circuits Conf. (CICC)*, 2013, pp. 1–8.

[12] S. Trotta *et al.*, "A 79 GHz SiGe-bipolar spread-spectrum TX for automotive radar," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2007, pp. 430–613.

[13] V. Giannini *et al.*, "A 79 GHz phase-modulated 4GHz-BW CW radar TX in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2014, pp. 250–251.

[14] N. Levanon and B. Getz, "Comparison between linear FM and phase-coded CW radars," in *IEE Proc.—Radar, Sonar and Navigation*, 1994, vol. 141, no. 4, pp. 230–240.

[15] W. Van Thillo, V. Giannini, D. Guermandi, S. Brebels, and A. Bourdoux, "Impact of ADC clipping and quantization on phase-modulated 79 GHz CMOS radar," in *Proc. 2014 Eur. Microwave Conf. (EuMC)*, Oct. 2014.

[16] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.6 mW 6b 2.2 GS/s 4-times interleaved fully dynamic pipelined ADC in 40 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2010, pp. 296–297.

[17] N. Yamada, Y. Tanaka, and K. Nishikawa, "Radar cross section for pedestrian in 76 GHz band," in *Proc. 2005 Eur. Microwave Conf.*, 2005, vol. 2, 4 pp.

[18] A. Medra, V. Giannini, D. Guermandi, and P. Wambacq, "A 79 GHz variable gain low-noise amplifier and power amplifier in 28 nm CMOS operating up to 125° C," in *Proc. ESSCIRC*, 2014.

[19] *Short range radar equipment operating in the 77 GHz to 81 GHz band; Part 1: technical requirements and methods of measurement*, European Telecommunications Standards Institute, ETSI, Tech. Rep., 2009.

[20] A. Bourdoux, V. Giannini, D. Guermandi, S. Brebels, and W. Van Thillo, "Impact of phase noise on high resolution phase-coded continuous mm-wave radars," in *Proc. 6th Global Symp. Millimeter-Waves*, 2013.

[21] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[22] W. L. Chan and J. R. Long, "A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[23] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A low phase noise quadrature injection locked frequency synthesizer for MM-wave applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2635–2649, Nov. 2011.

[24] Q. Shi, D. Guermandi, V. Giannini, and P. Wambacq, "A 5th subharmonic, inverter-based injection locked oscillator with 72–83 GHz locking range," in *Proc. IEEE RFIC*, 2014.

[25] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[26] M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1869–1878, Aug. 2008.

[27] Z. Chen and P. Heydari, "An 85–95.2 GHz transformer-based injection-locked frequency tripler in 65 nm CMOS," in *2010 IEEE MTT-S Int. Microwave Symp. Dig. (MTT)*, 2010, pp. 776–779.

[28] M. Belkerdid and T. Mears, "New piece-wise-linear SBPSK modulation waveform with robust adjacent channel emissions for UHF SATCOM channels," in *Proc. 2006 IEEE Military Communications Conf., MILCOM*, 2006, pp. 1–7.

[29] M. Bouhamame, L. L. Coco, S. Amiot, and S. Toutain, "A 60 dB harmonic rejection mixer for digital terrestrial TV tuner," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 59, no. 3, pp. 471–478, Mar. 2012.

[30] Z. Ru, E. A. Klumperink, G. Wienk, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, ISSCC*, 2009, pp. 230–231.

[31] M. Seo, B. Jagannathan, J. Pekarik, and M. J. Rodwell, "A 150 GHz amplifier with 8 dB gain and 6 dBm in digital 65 nm CMOS using dummy-prefilled microstrip lines," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3410–3421, Dec. 2009.

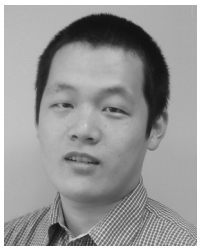
Vito Giannini (S'05–M'07–SM'12) was born in Mesagne, Italy. He received the Laurea degree (M.S.) in electrical engineering from the University of Pavia, Italy, in 2002 and the Ph.D. degree in information engineering from the University of Salento, Lecce, Italy, in 2006.

In 2004, he joined IMEC, Leuven, Belgium, first as visiting scholar and Marie Curie fellow and then as Senior Scientist, working on fully integrated CMOS transceivers for Software Defined Radios and heterogeneous Radio Access Networks. In 2011, he joined a new division of CMC s.r.l. company, Italy, dealing with the design of wireless sensor networks for aerospace and industrial applications. He is now a principal scientist with imec, Belgium, where his research interests are in single-chip millimeter-wave CMOS sensors, imagers as well as radios for wireless backhaul applications.

Dr. Giannini has coauthored more than 50 articles published in peer-reviewed IEEE conferences and journals and the book *Baseband Analog circuits for Software-Defined-Radio* (Springer, 2008). He was a co-recipient of the Fred W. Ellersick Prize 2014 for the best article published in a Communications Society magazine, and of the Young Scientist Award at IEEE ESSCIRC in 2010.

Davide Guermandi was born in Bologna, Italy, in 1975. He received the Laurea and Ph.D. degrees in electrical engineering from the University of Bologna, Bologna, Italy, in 2000 and 2005, respectively.

In 2006 he has been a Visiting Scholar with the Berkeley Wireless Research Center, University of California at Berkeley, CA, USA, working on CMOS circuits for short-range wireless communications based on coupled magnetic field. In 2007 and 2008, he was with STMicroelectronics, Pavia, Italy, working on the implementation of CMOS receivers operating in the 60 GHz frequency range. He was then with Broadcom, Bunnik, The Netherlands, where he worked on highly integrated CMOS tuners for Satellite, CATV, and MoCA Systems. In 2013, he returned to millimeter-wave CMOS design as a Researcher at imec, Leuven, Belgium.



Qixian Shi was born in Shanghai, China in 1986. He received the B.S. from Shanghai Jiao Tong University in 2009 and the M.S. (*cum laude*) from Katholieke Universiteit Leuven in 2011. Since 2011, he started to work in VUB/imec as a Ph.D. student.

His research interests include frequency synthesis for mm-wave transceiver.

Alaa Medra was born in Beheira, Egypt in 1988. He received the B.Sc. degree in electrical engineering from Alexandria University, Egypt, in 2010 and the M.Sc. degree in electrical engineering from Nile University, Egypt, in 2012. Since 2012, he started to work in VUB/imec as a Ph.D. student.

His research interests include front-end receivers operating in the mm-wave frequency range.

Wim Van Thillo received the Master degree in electrical engineering and his undergraduate degree in business economics from the Katholieke Universiteit Leuven, Belgium, in 2005. He received the Ph.D. degree from the same university in 2010 after 4 years of research in imec's wireless communications group.

His research interests include signal processing and system design for millimeter-wave communication and radar systems. He worked for several years on 60 GHz wireless communications. In the summer of 2008, he was a visiting researcher at UC Berkeley's Connectivity Lab. He currently leads the 79 GHz radar activity in imec.

André Bourdoux received the M.S. degree in electrical engineering in 1982 from the Universit Catholique de Louvain-la-Neuve, Belgium.

He joined IMEC in 1998 and is now principal scientist in the Wireless Research group of IMEC, Leuven. He currently leads the system level and algorithmic research on millimetre-wave communications and radar. He is also involved in research activities in the areas of 5G systems. His current research interests are multi-disciplinary, spanning the areas of wireless communications theory and signal processing, with a special emphasis on broadband systems and emerging physical layer techniques. He is the author/co-author of over 60 publications in journals and conferences. He is co-editor of the book *Smart Antennas—State of the Art* (Hindawi, 2005) and co-author of the book *Digital Compensation for Analog Front-Ends* (Wiley, 2008).

Piet Wambacq (S'89–M'91) received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Katholieke Universiteit Leuven, Belgium, in 1986 and 1996, respectively.

Since 1996, he is with imec, Heverlee, Belgium, working as a Principal Scientist on RF CMOS design for wireless applications. He is also a Professor at the university of Brussels (Vrije Universiteit Brussel). He has authored or coauthored two books and more than 200 papers in edited books, international journals, and conference proceedings.

Prof. Wambacq was an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS from 2002 to 2004. He was a co-recipient of the Best Paper Award at the Design, Automation and Test Conference (DATE) in 2002 and 2005. He is a member of the program committee of the IEEE International Solid-State Circuits Conference (ISSCC) and the European Solid-State Circuits Conference (ESSCIRC).