A 2.0–5.5 GHz Wide Bandwidth Ring-Based Digital Fractional-N PLL With Extended Range Multi-Modulus Divider

Ahmed Elkholy, *Student Member, IEEE*, Saurabh Saxena, *Member, IEEE*, Romesh Kumar Nandwana, *Student Member, IEEE*, Amr Elshazly, *Member, IEEE*, and Pavan Kumar Hanumolu, *Member, IEEE*

***Abstract*— Phase noise performance of ring oscillator based digital fractional-N phase-locked loops (FNPLLs) is severely compromised by conflicting bandwidth requirements to simultaneously suppress oscillator phase and quantization noise introduced by the time-to-digital converter (TDC), $\Delta\Sigma$ fractional divider, and digital-to-analog converter (DAC). As a consequence, their figure-of-merit (FoM_J) that quantifies the power–jitter tradeoff is at least 25 dB worse than their LC-oscillator-based FNPLL counterparts. This paper seeks to close this performance gap by extending PLL bandwidth (BW) using quantization noise cancellation techniques and by employing a dual-path digital loop filter to suppress the detrimental impact of DAC quantization noise. Fabricated in 65 nm CMOS process, the proposed FNPLL operates over a wide frequency range of 2.0–5.5 GHz using a modified extended range multi-modulus divider with seamless switching. The proposed digital FNPLL achieves 1.9 ps_{rms} integrated jitter while consuming only 4 mW at 5 GHz output. The measured in-band phase noise is better than −96 dBc/Hz at 1 MHz offset. The proposed FNPLL achieves wide BW up to 6 MHz using a 50 MHz reference and its FoM_J is −228.5 dB, which is the best among all reported ring-based FNPLLs.**

***Index Terms*— ADPLL, DAC, digital PLL, digitally controlled oscillator (DCO), DTC, dual-path, fractional-N, frequency synthesizer, jitter, LMS, multi-modulus divider (MMD), phase-locked loops (PLLs), ring oscillator, TDC, wide bandwidth.**

I. Introduction

FRACTIONAL-N phase-locked loops (FNPLLs) are widely used in large digital systems such as modern processors and in almost all wireless and wireline transceivers. By synthesizing output frequency, F_{OUT}, that is a fractional multiple, $N + \alpha$ (N is an integer, α is a fraction $0 < \alpha < 1$) of fixed reference crystal oscillator frequency, F_{REF} ($F_{OUT} = (N + \alpha)F_{REF}$). By varying N and α, FNPLLs are used to generate variable frequency clocks needed to implement finely granular dynamic frequency scaling in energy efficient processors [1], local oscillator (LO) signal generation in wireless transceivers [2] and to perform clock and data recovery [3] or to implement single chip multi-standard-compliant wireline transceivers capable of operating across a wide and continuous range of data-rates [4]–[7]. Typically, FNPLLs are implemented using the classical analog charge pump PLL architecture to meet jitter and spurious performance requirements. However, they require a large capacitor to implement the loop filter, which incurs a large area penalty. Further, low supply voltage and transistor imperfections in deeply scaled CMOS process also detrimentally impact the performance of the charge pump and degrade FNPLL performance. To alleviate these drawbacks, FNPLLs are being implemented using highly digital architectures that obviate the need for large capacitors and charge pumps. A digital FNPLL is obtained from a conventional charge-pump FNPLL by replacing the phase detector/charge-pump, and the analog loop filter, by a time-to-digital converter (TDC), and a digital loop filter (DLF), respectively. A digital-to-analog converter (DAC) converts output of the DLF (D_C) to a control voltage (V_C) of the VCO as depicted in Fig. 1(a).

A digital FNPLL, in principle, offers several advantages compared to its analog counterpart in terms of loop dynamics reconfigurability, scalability to newer process, and smaller silicon area. As a result, digital FNPLLs are particularly well suited for variable and flexible clock generation in area sensitive application such as multi-core processors, chip-to-chip I/O interfaces, and SoCs platforms [1]. However, in practice, quantization errors introduced by the fractional divider (FDIV), TDC, and DAC degrade digital FNPLL performance. As a result, jitter performance of digital FNPLLs, especially those using ring oscillators, is grossly inferior to their analog counterparts [1], [8]–[12]. Ring oscillators are extremely low-cost, scalable, and can inherently provide multiple phases with a wide tuning range. A compact ring-based FNPLL with a wide output frequency range can be independently utilized per a microprocessor core [1] or a full flexible I/O transceiver lane [5]. However, ring voltage-controlled oscillators (VCOs) fundamentally have poor phase noise performance compared to LC VCOs. While fractional-N multiplying delay-locked loops (MDLLs) [13] can achieve wider bandwidth (BW) than FNPLLs, they have speed limitation due to the use of selection logic which limits the maximum frequency range.

In view of this, we seek to improve the performance of ring oscillator based digital FNPLLs using a combination of architectural- and circuit-level techniques. To this end, a wide

Manuscript received January 12, 2016; revised March 15, 2016; accepted April 10, 2016. Date of publication June 10, 2016; date of current version July 25, 2016. This work was supported by the National Science Foundation under CAREER EECS-0954969. This paper was approved by Guest Editor Patrick Chiang.

A. Elkholy, S. Saxena, R. K. Nandwana, and P. K. Hanumolu are with the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801-2307 USA (e-mail: elkholy2@illinois.edu).

A. Elshazly is with Intel Corporation, Hillsboro, OR 97124 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2557807

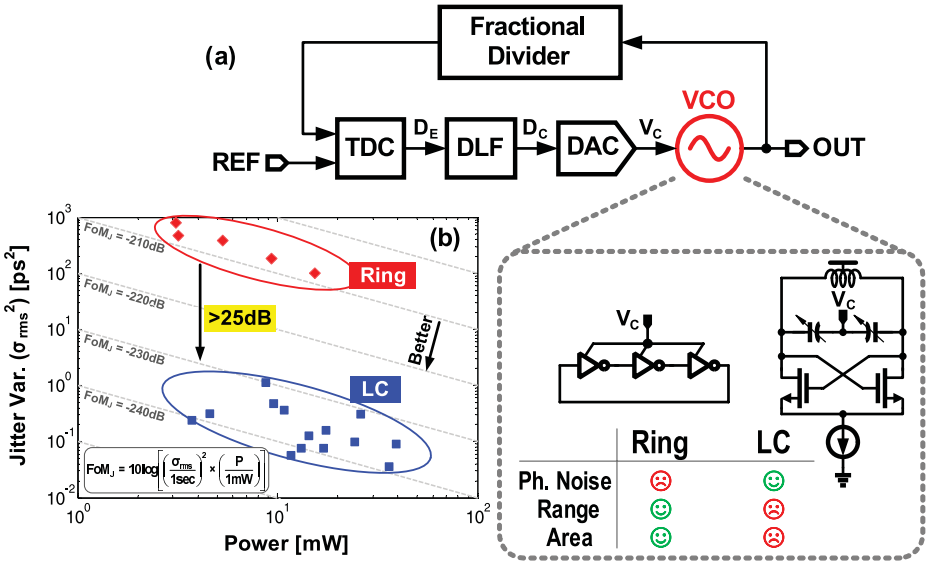

Fig. 1. (a) Digital FNPLL architecture using either ring- or LC-VCO. (b) Figure-of-merit (FOM_J) of state-of-the-art LC- and ring-based digital FNPLLs.

BW ring-based digital FNPLL with a wide output frequency range is presented. The proposed FNPLL achieves low-power, low-jitter performance, by using highly digital/synthesizable enhancement techniques [14]. The quantization errors of TDC and FDIV are suppressed by using a time amplifier (TA) [15] and digital-to-time converter (DTC)-based FDIV noise cancellation [15], [16], respectively. Furthermore, a dual-path digital loop filter architecture is proposed to resolve the DAC quantization noise challenge, which is stressed by the large gain of ring VCOs. This architecture helps also to mitigate the limit cycle behavior, typically associated with digital PLLs, and achieves wide PLL BW ($>0.1F_{REF}$) to maximize suppression of ring VCO phase noise. To attain a wide output range of 2.0–5.5 GHz, a multi-modulus divider (MMD) with wide programmable division range is required. However, using a conventional extended range MMD [17], the fractional operation fails at boundaries extension with a division factor changing between N and N + 1. In this work, we propose a modified extended range MMD that enables seamless switching at the boundaries extension. The prototype digital FNPLL achieves 1.9 ps_{rms} integrated jitter while consuming only 4 mW at 5 GHz. It achieves a jitter-power figure-of-merit (FoM_J) of −228.5 dB, which is the best among all reported ring-based FNPLLs.

The rest of the paper is organized as follows. Section II entails the design trade-offs of ring-based digital FNPLLs. Design details of the proposed ring-based FNPLL are described in Section III. Design and analysis of extended range multi-modulus divider is presented in Section IV. The circuit implementation of critical building blocks of the digital FNPLL is illustrated in Section V. The measured results from the test chip are shown in Section VI. Finally, the key contributions of this work are summarized in Section VII.

II. Ring-Based Digital FNPLL Design Tradeoffs

There are four primary sources of output jitter in a fractional-N DPLL, namely, quantization errors of TDC, DAC, $\Delta\Sigma$ fractional divider (FDIV) and phase noise of VCO. The impact of these quantization errors can be mitigated by noise cancellation or suppression techniques. Suppressing quantization errors introduces conflicting bandwidth (BW) requirements, which typically results in an increased power consumption. To elucidate this further, the TDC and FDIV quantization errors are low-pass filtered, while VCO phase noise is suppressed by a high pass transfer function. Due to this conflicting BW requirement, low noise digital FNPLLs either employ a high resolution TDC or a low noise oscillator, both of which increase power dissipation. In view of this, all digital FNPLLs with reasonable output jitter have employed LC VCOs [15], [16], [18] as they exhibit superior phase noise performance and power efficiency compared to ring-based VCOs. This can be quantified by a widely used VCO figure-of-merit (FoM_{OSC}) defined as:

$$\mathrm{FoM_{OSC}} = -\mathcal{L}(\Delta\omega) + 10\log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \frac{1}{P_{mW}}\right] \quad (1)$$

where ω_o is the VCO frequency, $\mathcal{L}(\Delta\omega)$ is the phase noise at offset $\Delta\omega$, and P_{mW} is the oscillator power consumption in mW. FoM_{OSC} of LC-VCOs is fundamentally higher than ring VCOs [19], which is manifested by about 20 dB performance gap in a recent survey [20]. This translates to a similar performance gap of at least 25 dB in the FoM_J of state-of-the-art ring- and LC-based FNDPLLs [see Fig. 1(b)]. However, LC VCOs have several drawbacks: first, they require thick metal layers, large silicon area, and do not scale with CMOS process. Second, LC VCOs with high quality factor (Q) have a very narrow tuning range. Additionally, generation of multiple clock phases requires additional circuitry of quadrature VCOs [21], I/Q dividers [6], poly-phase filters [7], or delay locked loops (DLLs) [4]. Therefore, LC VCOs are not preferred for area-sensitive applications that require multiple clock phases and/or wide output frequency range.

Fig. 2(a) shows the simulated phase noise of ring-based digital FNPLL when the PLL BW was chosen low enough to make the contribution of quantization errors to the output

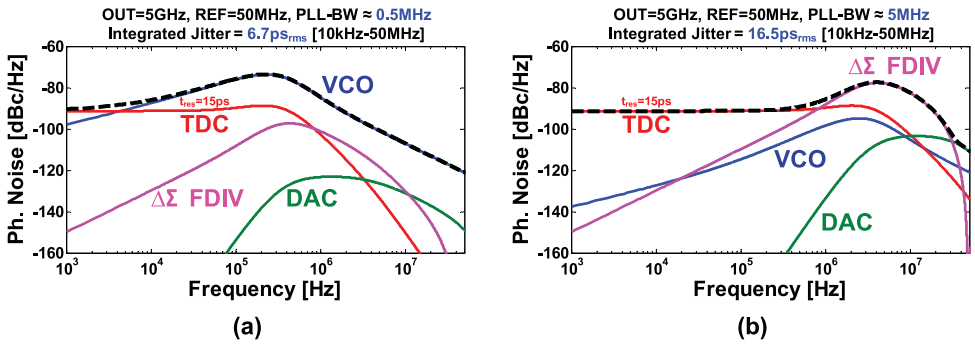

Fig. 2. Simulated digital FNPLL phase noise plots for two cases of bandwidths: (a) low bandwidth to suppress quantization error, and (b) high bandwidth for VCO phase noise suppression.

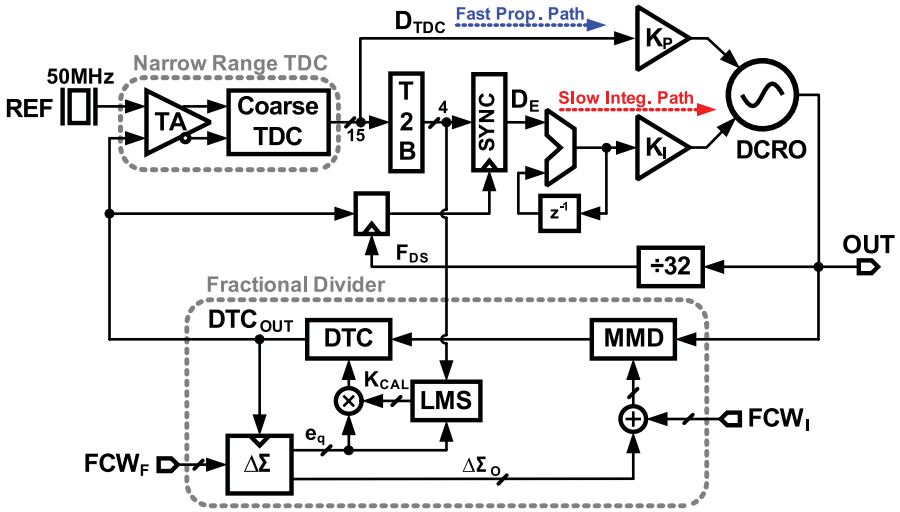

Fig. 3. Detailed block diagram of the proposed ring-based digital FNPLL.

phase noise negligible. In this particular example, we assumed a second-order $\Delta\Sigma$-based FDIV, a conventional TDC with a 15 ps resolution, a 5 bit DAC driven by a second-order $\Delta\Sigma$ modulator clocked at 156 MHz, and a K_{VCO} of 1 GHz/V. The BW is chosen to be about 500 kHz and the reference frequency is 50 MHz with the free running ring VCO phase noise of -87 dBc/Hz at 1 MHz offset. Due to the low BW, the total output phase noise is dominated by the VCO phase noise resulting in a large integrated jitter of about 6.7 ps_{rms}. In the other extreme case, when the PLL BW is increased to as high as 5 MHz ($\approx F_{REF}/10$), VCO phase noise is sufficiently suppressed as depicted in Fig. 2(b). However, output phase noise is dominated by quantization errors from TDC, FDIV, and DAC. The integrated jitter is larger than 16 ps_{rms} in this case. The large frequency drift across temperature of ring VCOs mandates a large gain ($K_{VCO} \approx 1$ GHz/V) to maintain lock across temperature. This leads to a higher impact of DAC quantization noise at the PLL output.

A. Quantization Noise Cancellation

Digital quantization noise cancellation (QNC) techniques are used to cancel FDIV quantization error at the output of the TDC [18], thereby greatly reducing its impact. For accurate cancellation, the cancellation gain is computed in background using an all-digital least-mean square (LMS) correlation technique. In this architecture, the wide dynamic range requirement of the TDC increases its power consumption and compromises its linearity performance, and consequently degrades jitter and spurious performance of the digital FNPLL. Additionally, the TDC must have fine effective resolution (t_{res}) to achieve low in-band phase noise. Assuming the TDC quantization noise ($S_{q_{TDC}}$) is uniformly distributed, The output phase noise due to TDC ($S_{\Phi_{TDC}}$) can be calculated as [15]:

$$S_{\Phi_{TDC}} = |NTF_{TDC}(f)|^2 \, S_{q_{TDC}} = \left[\frac{2\pi t_{res} NG(f)}{T_{REF}}\right]^2 \cdot \left(\frac{1}{12F_{REF}}\right) \quad (2)$$

where $NTF_{TDC}(f)$ is the noise transfer function of TDC noise to the output, and G(f) is the unity-gain PLL close-loop transfer function. Our objective is to develop low-power BW extension techniques to suppress ring-VCO phase noise and leverage its merits of wide range, multi-phases, and low cost, while achieving performance close to LC-based PLLs.

III. Proposed Digital FNPLL Architecture

The detailed block diagram of the proposed digital fractional-N PLL (FNPLL) is depicted in Fig. 3. A time amplifier (TA) magnifies the input phase difference between reference and feedback clocks, which is then digitized using a

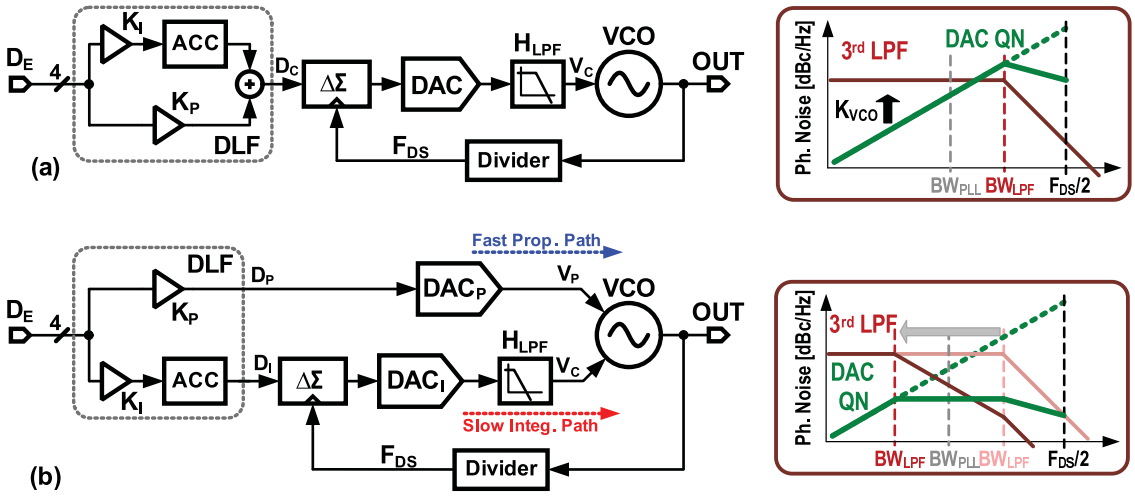

Fig. 4. (a) Conventional DAC and (b) proposed dual-path DAC.

4 bit coarse delay-line based TDC. The implementation details of the TA-TDC is similar to [15]. The PLL has a type-II response using a proportional-integral loop filter structure. The thermometer-coded TDC output directly controls the digitally controlled ring oscillator (DCRO) and implements a fast proportional control. The slow integral control path accumulates the 4 bit binary TDC output, which is synchronized to the $\Delta\Sigma$ DAC clock (F_{DS}), and scaled by K_I. The DTC is added in the feedback path to cancel $\Delta\Sigma$ quantization noise in time domain and implement a truly fractional divider [16]. This limits input range of the TDC and as a result, it operates in the random noise limited region, as the reference and feedback clocks are now aligned as in the case of an integer-N PLL. Consequently, wide dynamic range requirement of the TDC is alleviated, and a low-power, high-resolution, narrow-range TDC can be used [14], [15]. The output of the TDC is used in a LMS correlation algorithm to scale the DTC gain needed to implement precise QNC. Using the QNC scheme and a high resolution TDC ($\sim$ 2 ps), both in-band and out-of-band phase noise performance are greatly enhanced. As a result, at a wide PLL BW of $F_{REF}/10$, which is about 5 MHz in this example, the output integrated jitter is reduced to about 2.5 ps_{rms}. Further improvement in jitter performance is possible by mitigating DAC quantization noise, which dominates phase noise above 10 MHz offsets.

A. Dual-Path DAC

The conventional implementation of a digital loop filter encompasses adding the proportional and integral paths in digital domain as illustrated in Fig. 4(a). The output of the loop filter is mapped using a DAC to control the VCO frequency. The output phase noise due to DAC ($S_{\Phi_{DAC}}$) can be calculated using:

$$S_{\Phi_{DAC}} = |NTF_{DAC}(f)|^2 S_{q_{DAC}} = \left[\frac{V_{DAC} sinc\left(\frac{f}{F_S}\right)}{2^{m_{DAC}}} \cdot \frac{K_{VCO}(1-G(f))}{f}\right]^2 \cdot \left(\frac{1}{12F_S}\right) \quad (3)$$

where $NTF_{DAC}(f)$ is the band-pass noise transfer function of DAC noise to the output, $S_{q_{DAC}}$ is the DAC quantization noise, V_{DAC} is DAC full-scale voltage range, m_{DAC} is DAC number of bits, and F_S is DAC sampling frequency. The $sinc(f/F_S)$ term is due to the DAC zero-order hold for discrete-time to continuous-time conversion. As the required VCO frequency range increases, larger K_{VCO} is used, therefore a higher resolution DAC is needed to reduce the impact of its quantization noise. In order to reduce the hardware complexity of high resolution DACs [18], [22], $\Delta\Sigma$ DAC architecture is typically employed in DPLLs [1], [23], [24], where a digital $\Delta\Sigma$ modulator with order (p), usually clocked at a higher sampling frequency F_{DS}, drives a single- or a multi-bit DAC (m_{DAC}) to shape the quantization noise as shown in Fig. 4. The output phase noise due to quantization error of $\Delta\Sigma$ DAC can be expressed as:

$$S_{\Phi_{DAC}} = \left[\frac{V_{DAC} \text{sinc}\left(\frac{f}{F_{DS}}\right) H_{LPF}(f)}{2^{m_{DAC}}} \cdot \frac{K_{VCO}(1-G(f))}{f}\right]^2 \cdot \left(\frac{1}{12F_{DS}}\right) \cdot \left[2\sin\left(\frac{\pi f}{F_{DS}}\right)\right]^{2p}. \quad (4)$$

A low-pass filter, $H_{LPF}(f)$, helps to suppress DAC shaped noise. Fig. 5(a) shows the magnitude response of $NTF_{DAC}(f)$. But $H_{LPF}(f)$ adds loop latency and may impact PLL stability at wide BW setting. To quantify this, behavioral simulations were performed at 5 GHz output using a 50 MHz reference, and the following parameters: 5 MHz PLL BW, K_{VCO} = 1 GHz/V, V_{DAC} = 0.7 V, m_{DAC} = 5 bits, F_{DS} = 156 MHz, and second-order filter $H_{LPF}(f)$ with poles at 16 MHz and 32 MHz. The limit cycle behavior increases the output integrated jitter to 3.5 ps_{rms} as opposed to 2.5 ps_{rms} calculated using the linear model. Increasing the oversampling clock frequency F_{DS} by four times to 624 MHz reduces DAC noise and a 2 ps_{rms} integrated jitter can be achieved. But this increases DAC power consumption by four times. Besides, it may degrade the dynamic linearity performance of the DAC. Static and dynamic DAC non-linearity folds shaped quantization noise into in-band, and may limit the overall PLL

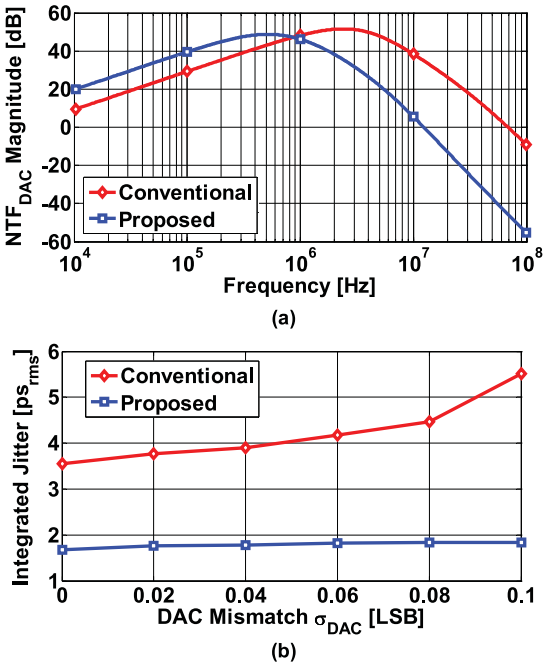

Fig. 5. (a) Simulated noise transfer function (NTF) of conventional and proposed DACs. (b) Simulated integrated jitter of digital FNPLL using conventional and proposed DACs.

phase noise performance. Fig. 5(b) plots the simulated output integrated jitter versus DAC non-linearity.

Reducing the low-pass filter, $H_{LPF}(f)$, bandwidth helps to reduce the impact of DAC imperfections, but as mentioned earlier, it also increases loop delay. To circumvent this, VCO control is split into two paths: a fast proportional control path with a small VCO gain K_{PP}, and a slow integral control path with a large K_{VCO} as shown in Fig. 4(b). A fast 4 bit Nyquist DAC_P directly controlled by TDC output helps to minimize loop latency and eliminates any limit cycle behavior. This limits jitter peaking even with a very wide BW of $F_{REF}/8$. The PLL loop BW is mainly defined by the proportional control K_{PP} as expressed by loop gain transfer function:

$$LG(s) \approx \frac{T_{REF}K_{PP}}{sNt_{res}} \cdot \left(1 + \frac{K_I}{sT_{REF}} \cdot \frac{V_{DAC}}{2^{m_{DAC}}} \cdot \frac{H_{LPF}(s)K_{VCO}}{K_{PP}}\right). \quad (5)$$

This architecture decoupled DAC_I filtering from loop BW. Hence, DAC_I quantization noise can be aggressively filtered as illustrated by the $NTF_{DAC}(f)$ in Fig. 5(a). Dual-path loop filter architecture was used in the context of analog PLLs [25]–[29] to set the integral and proportional path gains independently. In [24], dual-path was exploited to implement integral path in digital domain in a hybrid PLL architecture. Both these architectures are susceptible to static phase offset due to mismatch between integral and analog proportional paths. In our architecture, both proportional and integral paths are implemented in digital and are driven by the same TDC. This greatly reduces the phase offset between the two paths.

Using the dual-path DAC structure, where the filter poles are set at 1 MHz and 10 MHz, and a PLL BW of 5 MHz, DAC quantization noise is greatly filtered well below VCO

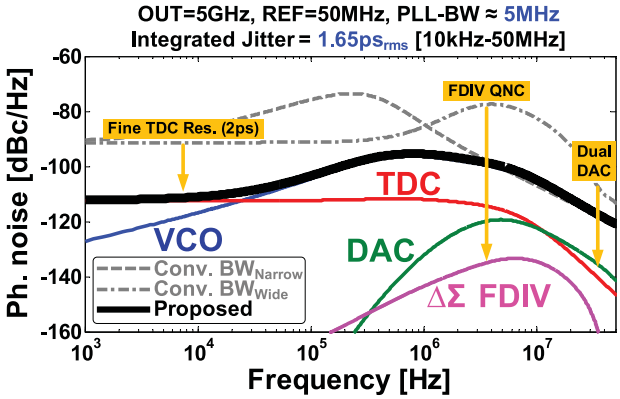

Fig. 6. Simulated phase noise of the proposed ring-based digital FNPLL.

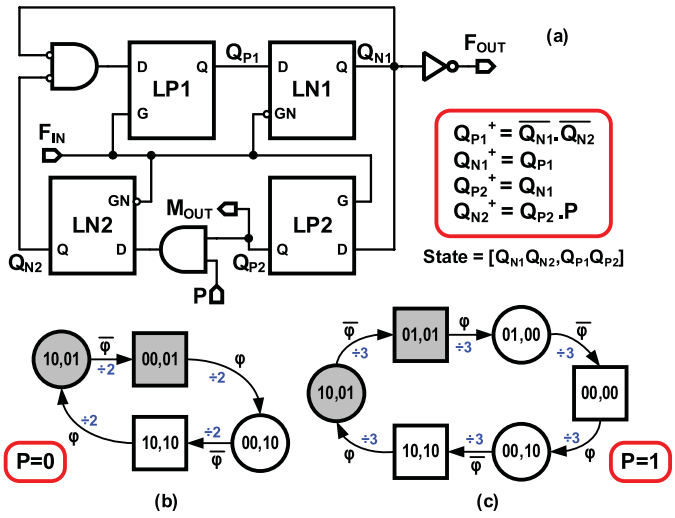

Fig. 7. (a) Block diagram of a divide-by-2/3 cell. State diagrams: (b) in the case of P = 0 and (c) P = 1.

phase noise. This aggressive filtering also helps to reduce the impact of DAC non-linear errors as demonstrated in Fig. 5(b). Output phase noise plot of the proposed fractional-N PLL is shown Fig. 6, where it is now only dominated by VCO phase noise. The simulated output integrated jitter is about 1.65 ps_{rms}. Further improvement in jitter performance is only possible by further increasing PLL BW at the expense of a higher reference frequency. Next, we will discuss the implementation details of the proposed extended range MMD and other key building blocks.

IV. Multi-Modulus Divider (MMD)

The proposed fractional-N PLL provides a wide range of output frequencies (2.0–5.5 GHz) and can operate with a reference clock in a frequency range of 50–100 MHz. A programmable divider with a wide division range (20–110) is needed to achieve this. The pulse swallow divider architecture [30] can provide such a wide programmable division range [31] using a dual-modulus prescaler and two synchronous counters. However, it consumes large power as it relies on high speed synchronous counters. In [32], a multi-modulus divider (MMD) architecture was proposed, in which a series of divide-by-2/3 cells are connected similar to a ripple counter. The power consumption is reduced significantly because:

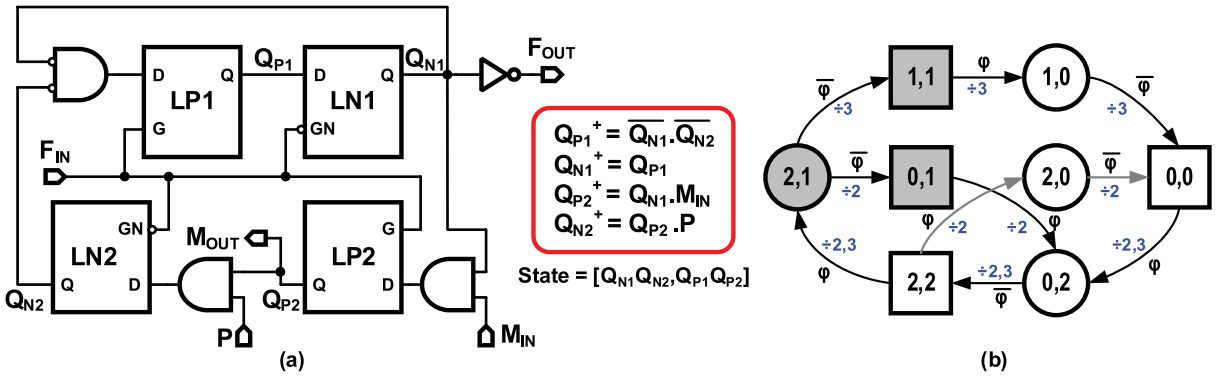

Fig. 8. (a) Block and (b) state diagrams for a divide-by-2/3 cell with modulus control M_{IN}.

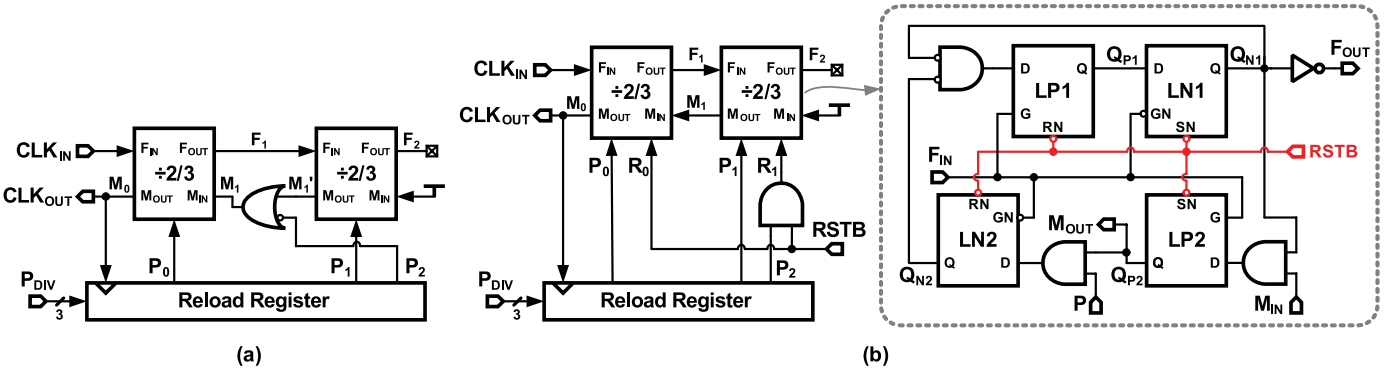

Fig. 9. (a) Conventional two-stage extended range MMD, and (b) proposed two-stage extended range MMD with seamless switching.

(a) clock frequency scales down through the divider chain and (b) there is no need for any intermediate clock buffers. Further, modular nature of the MMD also helps to minimize design time and to optimize layout floor-plan. The division range of MMD can be expressed as:

$$N = 2^0P_0 + 2^1P_1 + \cdots + 2^{n-1}P_{n-1} + 2^n \qquad (6)$$

where n is the number of divide-by-2/3 cells and P is the n bit division control signal. The division range of this conventional MMD is limited to 2^n to $2^{n+1} - 1$ (e.g., for $n = 6$, division range is from 64 to 127), which is not sufficient for PLLs with a wide output range. The division range can be extended by deactivating the last stage using OR gates [17]. However, this approach is susceptible to erroneous division operation when the division factor is dynamically changed as is the case in a fractional-N PLL. For example, when division factor switches between 63 (5-stages) to 64 (6-stages), the six divide-by-2/3 stage needs to be activated back and forth. Under this condition, undefined state of the deactivated cell may cause fractional operation to fail. We further elucidate this particular issue next and present an alternate MMD architecture to overcome it.

A basic divide-by-2/3 circuit depicted in Fig. 7(a) divides by 2 when the control signal $P = 0$, and by 3 when $P = 1$. The divide-by-2/3 circuit consists basically of two positive latches, namely LP1 and LP2, and two negative latches, namely LN1 and LN2. The latches outputs are defined as Q_{P1}, Q_{P2}, Q_{N1}, and Q_{N2} and the divider state is defined as $[Q_{N1}Q_{N2}, Q_{P1}Q_{P2}]$, where next state is calculated using: $Q_{P1}^+ = \overline{Q_{N1}} \cdot \overline{Q_{N2}}$, $Q_{N1}^+ = Q_{P1}$, $Q_{P2}^+ = Q_{N1}$, and $Q_{N2}^+ = Q_{P2} \cdot P$. In case of $P = 0$, latch LN2 input is set to zero, and the circuit behaves as a standard divide-by-2 circuit. The output signal $M_{OUT} = Q_{P2}$, is just a delayed version of Q_{N1} (by half clock cycle). There are four allowed states, the shaded states represent states with $M_{OUT} = 1$. In case of $P = 1$, latch LN2 is active, Q_{N2} is a delayed version of Q_{N1} (one clock cycle). As a result, a slower feedback is added to the main feedback signal Q_{N2} using a NOR gate, and latch LP1 input is held zero for two clock cycles (as opposed to one). The state diagram is illustrated in Fig. 7(c), where division cycle repeats after six state transitions (i.e., three clock cycles). The output signal $M_{OUT} = 1$ represents a divide-by-3 clock with 33% duty cycle.

The divide-by-2/3 circuit used in MMD [17] has a modulus control (M_{IN}) as shown in Fig. 8(a). It uses an extra AND gate, such that it divides-by-3 only when both control inputs P and M_{IN} are high. Next state of LP2 is updated as: $Q_{P2}^+ = Q_{N1} \cdot M_{IN}$. When $M_{IN} = 0$, the lower feedback path is disabled and the circuit behaves as a divide-by-2 circuit (i.e., $F_{OUT} = F_{IN}/2$) and output signal M_{OUT} is set to zero. Fig. 8(b) shows a complete state diagram of the divide-by-2/3 circuit. It combines the state diagrams in Fig. 7 and adds an extra state $[Q_{N1}Q_{N2}, Q_{P1}Q_{P2}] = [10, 00] = [2, 0]$ to account for $M_{IN} = 0$ case. By dynamically controlling M_{IN} signal, higher division factors can be realized by exploiting the inner loop entailing states [2, 0], [0, 0], [0, 2], and [2, 2]. Division range from 4 to 7 can be realized by cascading two divide-by-2/3 cells. To extend division range from 2 to 7, an OR gate is inserted to bypass the second stage [17] in the case of divide-by-2 or 3 as shown in Fig. 9(a). In this case, MSB of the

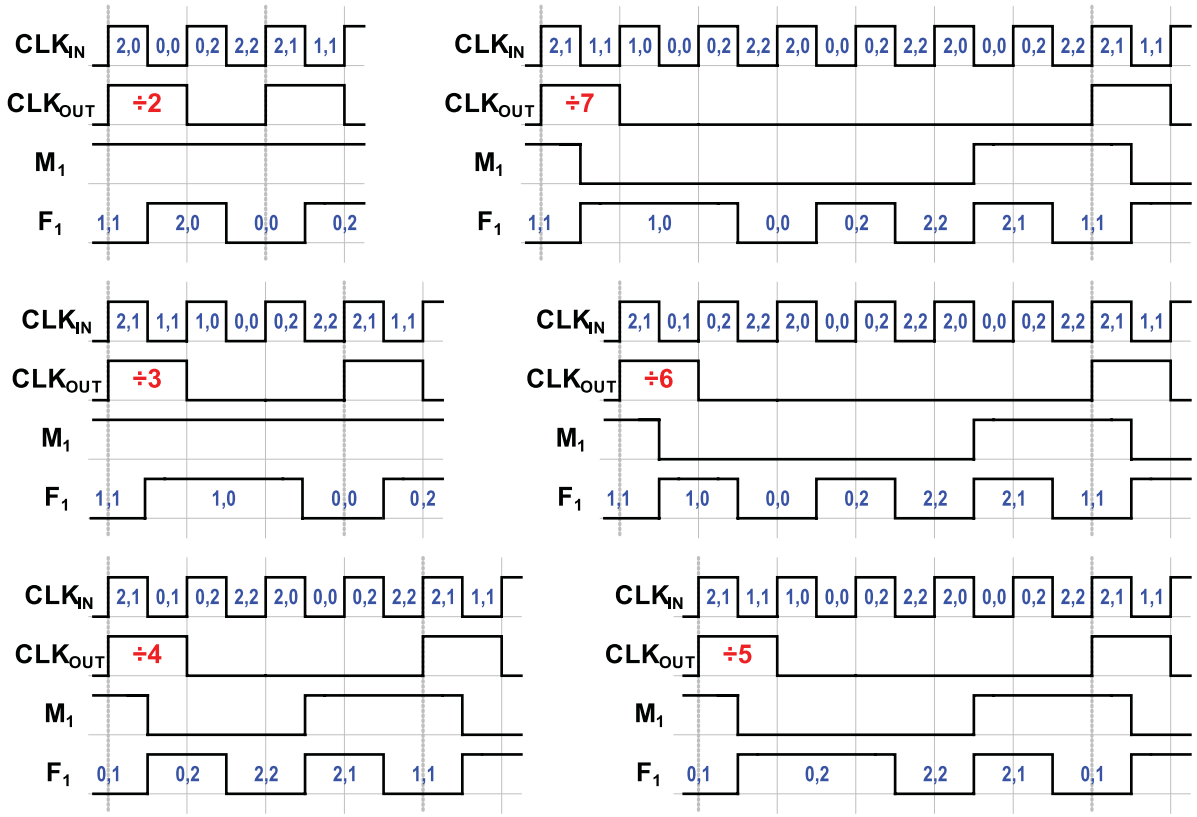

Fig. 10. Timing diagrams of the two-stage MMD for different division operations from 2 to 7.

3 bit control signal ($P_2 = 0$) sets the modulus control $M_1 = 1$. The detailed timing diagrams for division operations from 2 to 7 are shown in Fig. 10, where the states of both stages are highlighted around their input clocks (CLK_{IN} and F_1). For example, during divide-by-4 operation, control signal is ($P_2P_1P_0 = 100$) and the state transition path of first stage repeats with the following sequence: [2, 1], [0, 1], [0, 2], [2, 2], [2, 0], [0, 0], [0, 2], [2, 2].

In fractional-N PLLs, MMD division factor changes dynamically according to the output of $\Delta\Sigma$ modulator. Hence, it is critical to load the P-control signal on the positive edge, such that it remains fixed during the whole division operation as shown in Fig. 9(a). As mentioned earlier, when the division factor changes across extension boundaries (e.g., P changes from 3 to 4), the first division operation fails as illustrated by the timing diagram in Fig. 11(a). Because the bypassed second stage is dividing F_1 by 3 its state keeps changing and is not controlled each time extension is enabled. Therefore, modulus control signals M_1 changes incorrectly and starts the divide-by-4 operation from an unknown state ([2, 0] in this example), instead of state [2, 1]. As a result, the first half of the divide-by-4 operation (i.e., two clock cycles) is bypassed, resulting in a glitch and effectively a wrong divide-by-5 operation.

By observing the second stage behavior during division operations from 4 to 7 (see Fig. 10), we identify that state [2, 1], which indicates the start of division operation, is common to all four cases. This state resides before CLK_{OUT} goes high and the new P control factor is loaded. Therefore, when the second stage is bypassed, we resets its state to [2, 1], so as to achieve seamless switching when the extension is enabled. The proposed MMD with a division range from 2 to 7 is shown in Fig. 9(b), where a reset port (RSTB) is added to deactivate the second stage when the lower division range (2 to 3) is used (RSTB = P_2). The same modified cell can also be used in the first stage to ensure that the first division operation on start-up is correct. Fig. 11(b) shows the timing diagram of the proposed MMD when the division factor is switched from 3 to 4. Now, state of the second stage remains fixed to [2, 1] during the divide-by-3 operation. When P changes from 3 to 4, second stage is activated (RSTB = 1) to perform a divide-by-2 operation. In this example, its state is changed to [0, 1] as $P_1 = 0$ and to [1, 1] if $P_1 = 1$ for divide-by-6 or 7 operation.

Compared to solutions [33], [34] that use multiplexers and extra logic to ensure seamless switching across only one extension boundary, the proposed solution has minimum added hardware and can be generalized to realize seamless operation across multiple extension boundaries. Fig. 12 shows detailed block diagram of the proposed extended range MMD. It is composed of six divide-by-2/3 cells with a reset port plus extension control logic with a reload register. It is crucial to use proper clock signal to update the new P control factor as described before. Therefore, for a division range from 16 to 63, the fifth stage can be switched back and forth, and the modulus M_3 clock is used to reload the new P control factor. The modulus M_4 clock is used for a division range from 32 to 127. A 2×1 multiplexer is used to select the output clock according to the required range. The MMD operates with an input clock

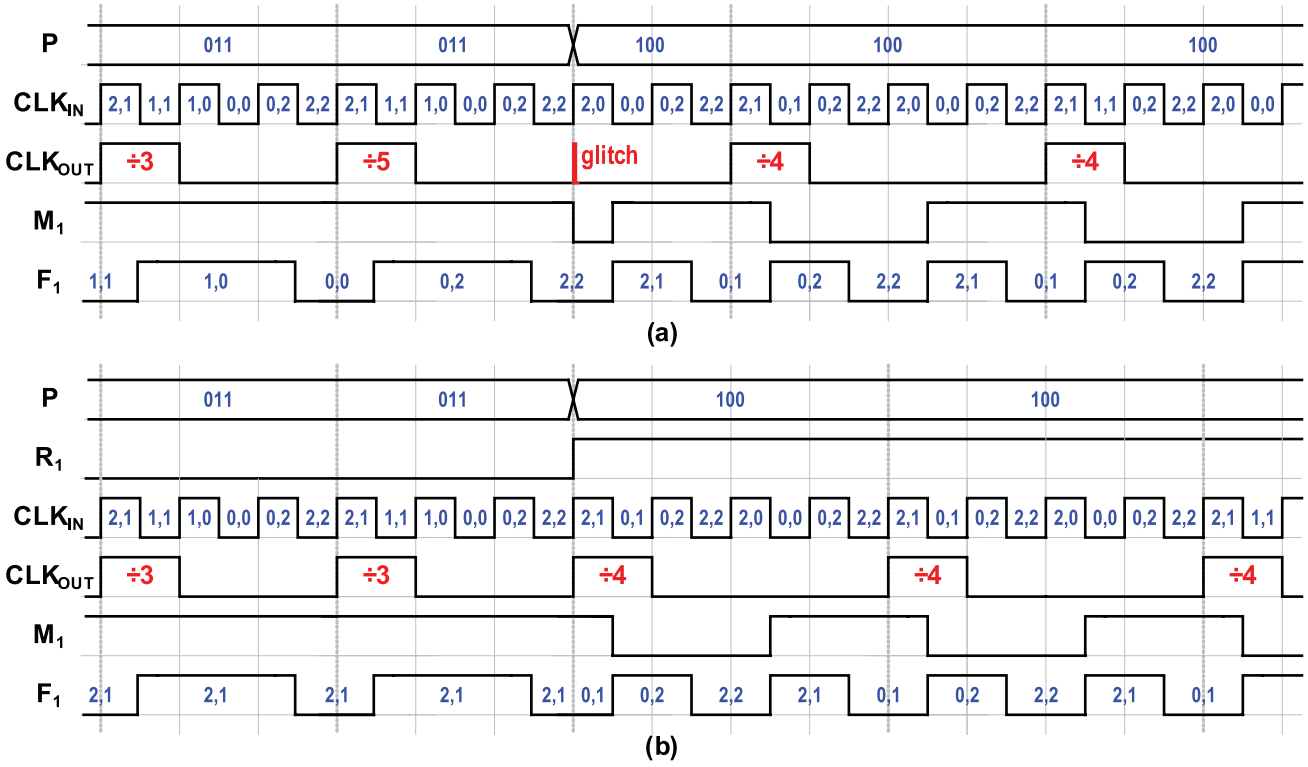

Fig. 11. Timing diagrams of the two-stage MMD when division factor changes from 3 to 4 in the case of (a) conventional MMD, and (b) proposed MMD with seamless switching.

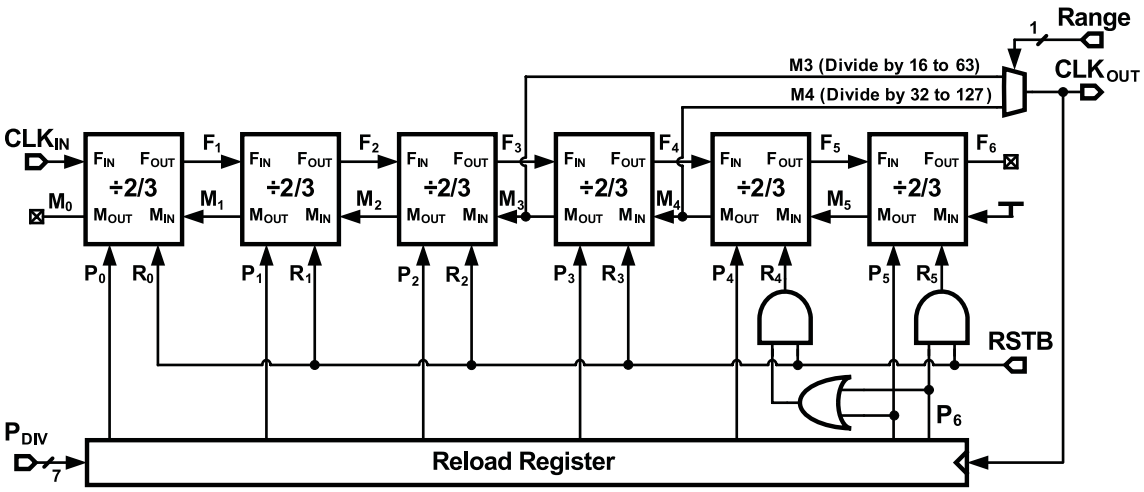

Fig. 12. Detailed block diagram of the proposed MMD with seamless switching across a wide division range from 16 to 127.

frequency of up to 6 GHz, where the first divide-by-2/3 cell is implemented using true single phase clocked (TSPC) DFFs to reduce the power consumption, while the other five cells are implemented using standard-cell CMOS latches.

V. Building Blocks

A. Digitally Controlled Ring Oscillator (DCRO)

The schematic of the proposed split-tuned digitally controlled ring oscillator (DCRO) is shown in Fig. 13. The ring-VCO core is composed of four pseudo differential delay cells. Each delay cell is implemented using two current starved CMOS inverters with a resistor feed-forward coupling (R_F) for differential operation. The current drawn by the delay cells combines the proportional and integral paths to control the oscillator frequency. For the fast proportional path, the 15-level thermometer-coded TDC output (D_P) directly controls the DCRO frequency through a 4 bit current-mode DAC_P. The cell current can be varied to control the PLL bandwidth. The 14 bit accumulator output, D_I, of the slow integral path is truncated to 5 bits using a second-order error-feedback based digital $\Delta\Sigma$ modulator. The output of $\Delta\Sigma$ modulator is converted to 31-levels thermometer-code to minimize the differential non-linearity (DNL) of the 5 bit current DAC_I. Unit cells in the

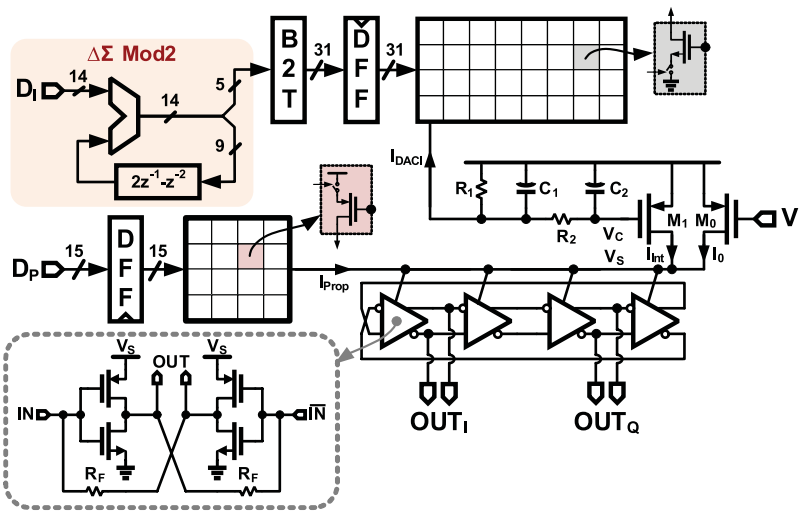

Fig. 13. Schematic of the digitally controlled ring oscillator (DCRO) with dual-path control.

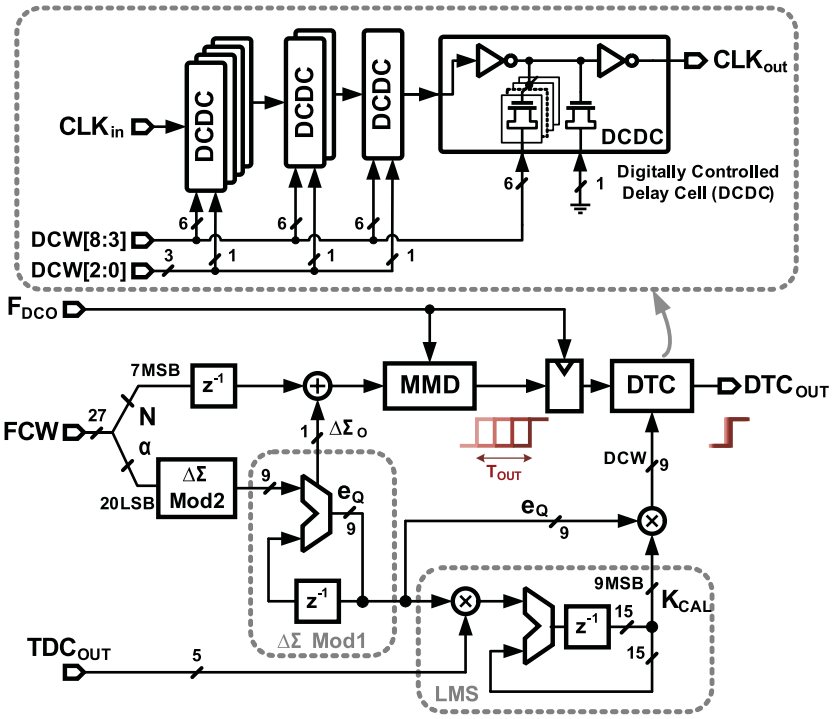

Fig. 14. Implementation details of the fractional divider with LMS calibrated DTC quantization noise cancellation scheme.

DAC are sized to improve static linearity, while adding a DFF in each cell and matching clock routing improves dynamic linearity. The output control current of DAC_I is converted to voltage by programmable resistor R_1, where the voltage control range is maximized. The frequency range of the integral control has to be large enough to maintain DPLL lock across temperature variations. At 5 GHz, simulation results shows the VCO frequency varies about 300 MHz (6%) as temperature changes from −40 °C to 125 °C. The current source transistor M_1 is sized to realize a large K_{VCO} of 1 GHz/V to maintain lock across temperature. A third-order low-pass filter with the third pole located at the drain of current source transistor, M_1, suppresses the shaped quantization error. The bandwidth of the third-order low-pass filter of the integral path can be lowered aggressively to less than 1 MHz with no stability concerns even for a wide DPLL bandwidth of $F_{REF}/10 = 5$ MHz.

B. Fractional Divider

The detailed implementation of the fractional divider is shown in Fig. 14. The output frequency is controlled using a 27 bit input frequency control word (FCW), where the 7 MSBs represent the integer part (N) and the remaining 20 LSBs denote the fractional part (α) of the division ratio, $N + \alpha$. The 20 bit fractional bits are truncated to 9 bits using a second-order $\Delta\Sigma$ modulator, which is implemented using an

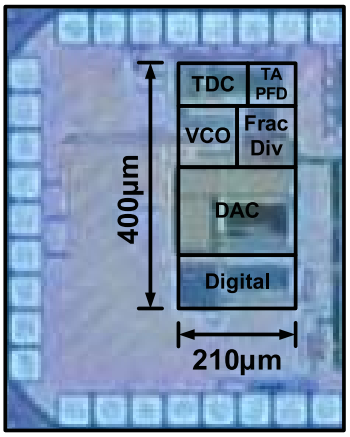

Fig. 15. Die photograph.

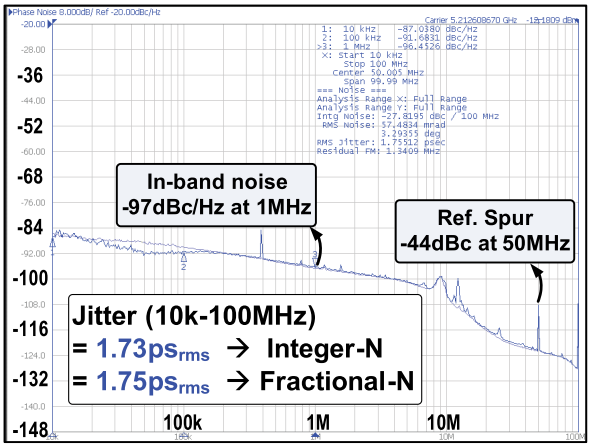

Fig. 16. Measured phase noise at 5.2 GHz output frequency for integer-N and fractional modes.

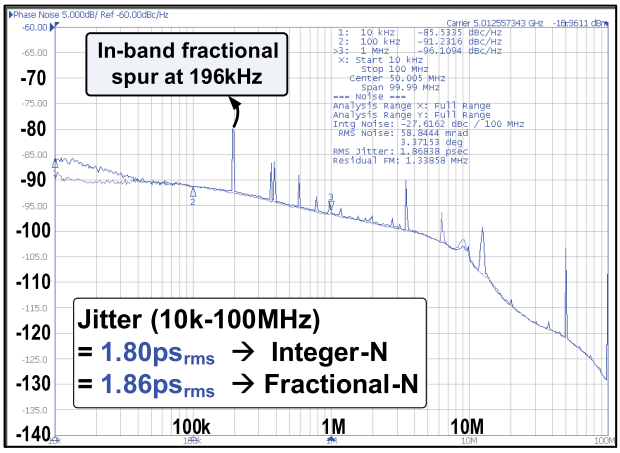

Fig. 17. Measured output spectrum at 5 GHz output frequency with in-band fractional spur at 196 kHz offset.

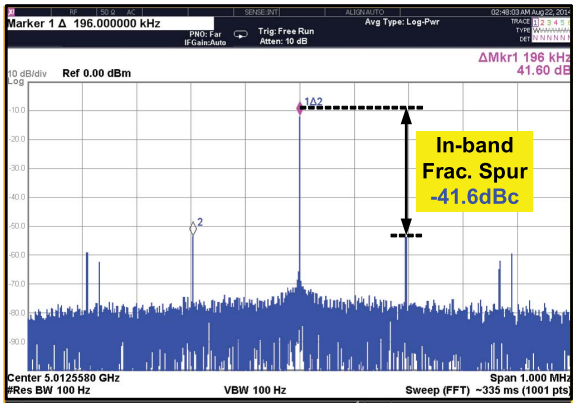

Fig. 18. Measured output spectrum at 5 GHz output frequency and 196 kHz fractional offset.

error-feedback architecture. A 15 bit linear feedback shift register (LFSR) generates a dither signal that can be added to the LSBs. The 9 bit $\Delta\Sigma$ output drives an accumulator, that acts as a first-order $\Delta\Sigma$ modulator, where the accumulator carry, $\Delta\Sigma_O$, is added to the integer control (N) to control the MMD. As a result, MMD is dithered between N and N + 1 such that the average division ratio is $N + \alpha$. The error resulting from truncating 20 bits to 1 bit, denoted as e_Q, appears as phase quantization error at the output of the MMD. The accumulator sum, represents the quantization error signal, e_Q, which is converted to an equivalent phase quantization error using a DTC to realize a QNC scheme in time domain [15], [16]. The gain of DTC is PVT-sensitive and is calibrated using a background LMS algorithm based on the correlation between TDC_{OUT}, which contains residual e_Q, and e_Q itself [16]. The 9 bit DTC is implemented using an 8 stages digitally controlled delay line (DCDL), with a 0.5 ps resolution, similar to the one in [15] and [35].

VI. Measurement Results

A prototype ring-based digital FNPLL was fabricated in 65 nm CMOS process and its die photograph is shown in Fig. 15. It occupies an active area of 0.084 mm^2. A standard 50 MHz external crystal oscillator was used to provide a reference clock that has about 0.8 ps_{rms} measured integrated jitter from 10 kHz to 20 MHz and a noise floor of −147 dBc/Hz. The output frequency can be tuned from 2.0 GHz to 5.5 GHz using a 27 bit FCW, with an approximate frequency resolution of 50 Hz. At 5 GHz output frequency, the total power consumption is less than 4 mW at a supply voltage of 0.9 V, while at 2.5 GHz the FNPLL consumes about 1.35 mW from a supply voltage of 0.7 V. The chip is characterized using Agilent N9000A spectrum analyzer (SA) and Agilent E5052B signal source analyzer (SSA). The measured phase noise of the digital FNPLL at 5.2 GHz is shown in Fig. 16. With a wide bandwidth of 5 MHz, integrated jitter from 10 kHz to 100 MHz is about 1.75 ps_{rms} in both integer and fractional-N modes, while the reference spur is about −44 dBc. The relatively high reference spur is attributed to the wide BW and the reduced filtering in the proportional path. An in-band phase noise of −97 dBc/Hz is achieved at 1 MHz offset. To illustrate effectiveness of DTC-based quantization noise cancellation, digital FNPLL phase noise is measured with and without DTC calibration. When DTC calibration is turned off, $\Delta\Sigma$ quantization noise is not completely cancelled and the residual error saturates the narrow range TDC. This dramatically increases in-band phase noise resulting in an increase of integrated jitter from 1.8 ps_{rms} to about 8.9 ps_{rms}.

The measured phase noise at 5 GHz with in-band fractional spurs is shown in Fig. 17. Fig. 18 shows the measured output

TABLE I
DIGITAL FRACTIONAL-N PLL PERFORMANCE SUMMARY.

	Chen [8] JSSC'10	Grollitsch [9] ISSCC'10	Li [1] ISSCC'12	Jang [10] ISSCC'13	Liu [11] ISSCC'14	Tsai [37] ISSCC'15	This Work	
Technology [nm]	65	65	22	28	20	16	65	
Freq. Range [GHz]	0.6-0.8	0.3-4.0	0.6-3.6	0.032-2.0	0.8-1.6	0.25-4.0	2.0-5.5	
Ref. Freq. [MHz]	26	25	25-200	30	25	200	50	
Supply [V]	1.1-1.3	1.1/1.3	1	1	0.9	0.52-0.8	0.7	0.9
Power [mW]	3.2	9.3	18.4	5.3	3.1	9.3	1.35	4
Out Freq. [GHz]	0.8	3.0	3.2	2	1.6	3	2.5	5
Bandwidth [MHz]	1	0.7	0.003-4	4	4	2	5	5
In-band PN [dBc/Hz]*	-72.1	-74.6	-63.6	-75.7	-74.1	N/A	-91.5	-97
Integrated Jitter [ps_{rms}]	21.5 [1k-100MHz]	13.5 [1k-20MHz]	10 N/A	19.3 [20k-40MHz]	28 [20k-40MHz]	3.3 [10k-1GHz]	3.6 [10k-100MHz]	1.9
FoM_J [dB]**	**-208.3**	**-207.7**	**-207.4**	**-207**	**-206.1**	**-219.8**	**-227.6**	**-228.5**
Power Eff. [mW/GHz]**	4	3.1	5.1	2.65	1.94	3.1	0.54	0.8
Area [mm^2]	0.027	0.038	0.03	0.026	0.012	0.029	0.084	

* Normalized In-band PN to 5GHz, **$\mathrm{FoM_J} = 10\log\left[\left(\frac{\sigma_{\mathrm{rms}}}{1\mathrm{sec}}\right)^2 \cdot \frac{\mathrm{P}}{1\mathrm{mW}}\right]$

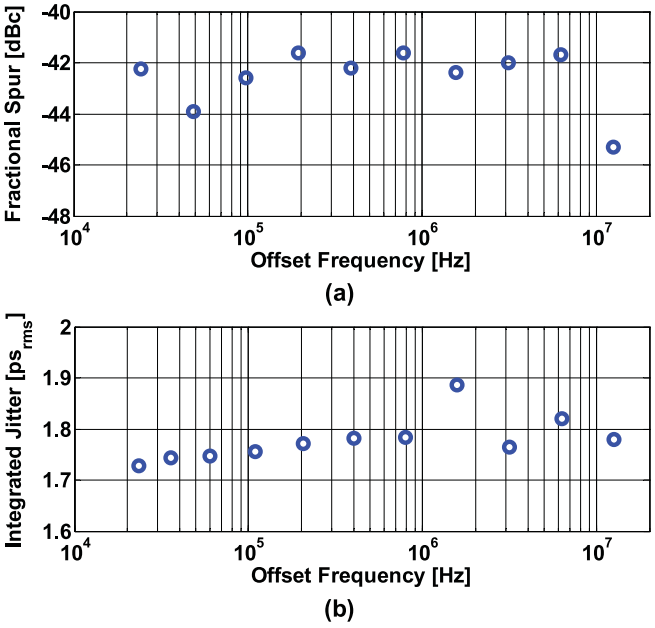

Fig. 19. (a) Measured fractional spur and (b) rms integrated jitter as a function of output fractional frequency offset.

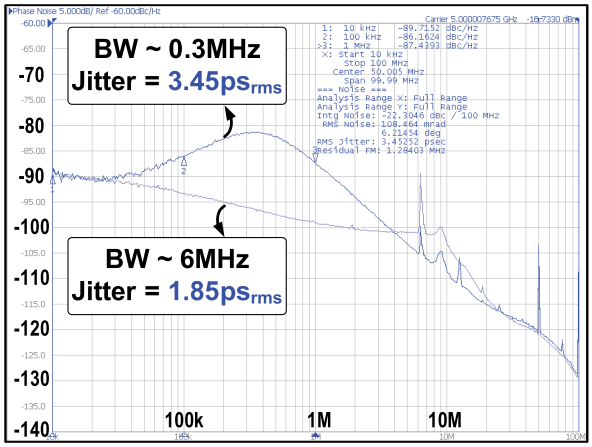

Fig. 20. Measured phase noise for narrow (0.3 MHz) and wide (6 MHz) BW settings at 5 GHz output using 50 MHz reference.

spectrum where the worst case fractional spur is less than −41.6 dBc at 196 kHz fractional offset frequency. Measured fractional spur and integrated jitter are plotted as a function of output fractional frequency offset in Fig. 19. This indicates a worst-case jitter of less than 1.9 ps_{rms}. Fig. 20 shows the measured phase noise for two different BW settings at 5 GHz output. The bandwidth is controlled by changing the proportional DAC_P current. In case of a narrow BW setting of 0.3 MHz, phase noise is dominated by the VCO resulting in a relatively high integrated jitter of 3.45 ps_{rms}. On the other hand, an excellent jitter of 1.85 ps_{rms} is achieved with a wide BW setting of 6 MHz (around $F_{REF}/8$). No jitter peaking or limit cycle behavior was observed. Measured integrated jitter, plotted as a function of loop bandwidth in Fig. 21, illustrates greater than 3 MHz bandwidth is needed to achieve integrated jitter < 1.9 ps_{rms}.

The performance summary and comparison with state-of-the-art ring-based digital FNPLLs are shown in Table I. The

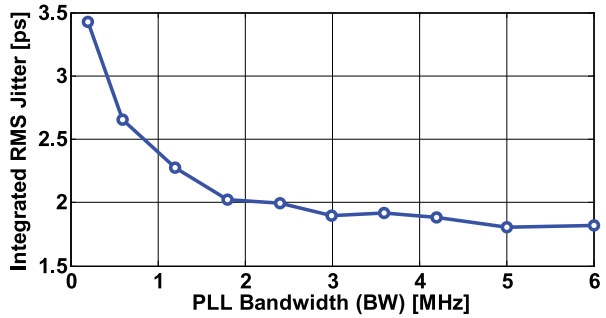

Fig. 21. Measured rms integrated jitter across different bandwidth settings at 5 GHz output frequency.

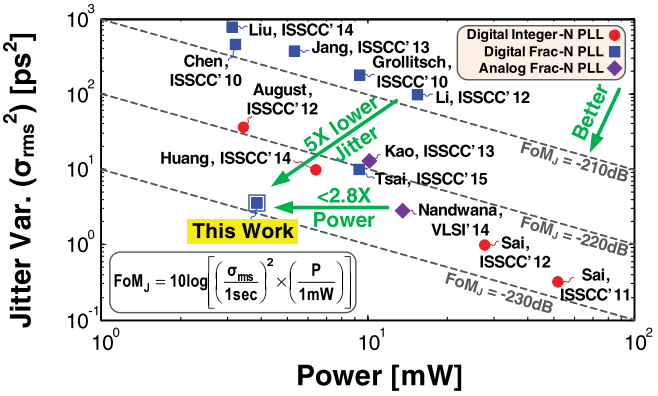

Fig. 22. FoM comparison.

proposed architecture achieves the lowest normalized in-band noise by about 21 dB. This work achieves performance comparable to LC-based FNPLLs while maintaining the merits of ring VCOs. As shown in Fig. 22, the proposed digital FNPLL achieves the best FoM_J of -228.5 dB that reflects jitter and power trade-off. It also outperforms the best reported ring-based analog FNPLL [36] by about 3 dB, while occupying $8\times$ less area.

VII. Conclusion

Ring-based digital FNPLL clock generation offers several advantage in area sensitive applications such as multi-core processors, chip-to-chip I/O interfaces, and SoCs platforms. Ring oscillators are extremely low-cost, compact, scalable, and can inherently provide multiple phases with a wide tuning range, but they suffer from poor phase noise performance. In this paper, we developed PLL bandwidth extension techniques to suppress ring VCO phase noise to leverage its merits, while achieving performance close to LC-based PLLs. A low-power, wide-bandwidth ring-based digital FNPLL with excellent jitter performance and wide output frequency range is demonstrated. It employs a 9 bit DTC-based fractional divider that alleviates TDC dynamic range requirements and a low-power, high-resolution 4 bit TDC to achieve low in-band phase noise. A dual-path loop filter architecture is used to suppress DAC noise and minimize loop latency. A modified extended range multi-modulus divider (MMD) is proposed that enables seamless switching at extension range boundaries. As a result, a wide output frequency range is realized at low power consumption. The measured results indicate an excellent jitter performance, low in-band phase noise, and wide PLL bandwidth of $\text{F}_\text{REF}/8$ with no limit cycles.

References

[1] Y. W. Li, C. Ornelas, H.-S. Kim, H. Lakdawala, A. Ravi, and K. Soumyanath, "A reconfigurable distributed all-digital clock generator core with SSC and skew correction in 22 nm high-k tri-gate LP CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 70–72.

[2] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[3] G. Shu *et al.*, "A 4-to-10.5 Gb/s continuous-rate digital clock and data recovery with automatic frequency acquisition," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 428–439, Feb. 2016.

[4] J. Kim *et al.*, "A 16-to-40 Gb/s quarter-rate NRZ/PAM4 dual-mode transmitter in 14 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

[5] Y. Frans *et al.*, "A 0.5–16.3 Gb/s fully adaptive flexible-reach transceiver for FPGA in 20 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1932–1944, Aug. 2015.

[6] T. Kawamoto *et al.*, "Multi-standard 185 fs_rms 0.3-to-28 Gb/s 40 dB backplane signal conditioner with adaptive pattern-match 36-tap DFE and data-rate-adjustment PLL in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

[7] P. Upadhyaya *et al.*, "A 0.5-to-32.75 Gb/s flexible-reach wireline transceiver in 20 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

[8] M. S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800 MHz fractional-N digital PLL with embedded TDC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2819–2827, Dec. 2010.

[9] W. Grollitsch, R. Nonis, and N. Da Dalt, "A 1.4 psrms-period-jitter TDC-less fractional-n digital PLL with digitally controlled ring oscillator in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 478–479.

[10] T.-K. Jang *et al.*, "A 0.026 mm^2 5.3 mW 32-to-2000 MHz digital fractional-phase locked-loop using a phase-interpolating phase-to-digital converter," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 254–255.

[11] J. Liu *et al.*, "A 0.012 mm^2 3.1 mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 268–269.

[12] K. Takinami, R. Strandberg, P. C. P. Liang, G. Le Grand de Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2650–2660, Nov. 2011.

[13] S. Levantino, G. Marucci, G. Marzin, A. Fenaroli, C. Samori, and A. L. Lacaita, "A 1.7 GHz fractional-N frequency synthesizer based on a multiplying delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2678–2691, Nov. 2015.

[14] A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly, and P. K. Hanumolu, "A 4 mW wide bandwidth ring-based fractional-N DPLL with 1.9 ps_rms integrated-jitter," in *Proc. IEEE Custom Int. Circuits Conf. (CICC)*, 2015, pp. 1–4.

[15] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, Apr. 2015.

[16] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs_rms integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[17] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.

[18] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.

[19] R. Navid, T. H. Lee, and R. W. Dutton, "Minimum achievable phase noise of RC oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 630–637, Mar. 2005.

[20] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M.-C. F. Chang, "A blocker-tolerant inductor-less wideband receiver with phase and thermal noise cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2948–2964, Dec. 2015.

[21] A. A. Hafez, M.-S. Chen, and C.-K. Yang, "A 32–48 Gb/s serializing transmitter using multiphase serialization in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 763–775, Mar. 2015.

[22] J. Lin, B. Haroun, J. S. Wang, T. Mayhugh, and C. Barr, "A PVT tolerant 0.18 MHz to 600 MHz self-calibrated digital PLL in 90 nm CMOS process," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 488–541.

[23] P.-Y. Wang, J.-H. C. Zhan, H.-H. Chang, and H.-H. Chang, "A digital intensive fractional-N PLL and all-digital self-calibration schemes," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2182–2192, Aug. 2009.

[24] W. Yin, R. Inti, A. Elshazly, B. Young, and P. K. Hanumolu, "A 0.7-to-3.5 GHz 0.6-to-2.8 mW highly digital phase-locked loop with bandwidth tracking," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1870–1880, Aug. 2011.

[25] D. Mijuskovic *et al.*, "Cell-based fully integrated CMOS frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 271–279, Mar. 1994.

[26] I. I. Novof, J. Austin, R. Kelkar, D. Strayer, and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and $\pm$50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 30, no. 11, pp. 1259–1266, Nov. 1995.

[27] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

[28] R. Nonis, N. Da Dalt, P. Palestri, and L. Selmi, "Modeling, design and characterization of a new low-jitter analog dual tuning LC-VCO PLL architecture," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1303–1309, Jun. 2005.

[29] M. Ferriss *et al.*, "An integral path self-calibration scheme for a dual-loop PLL," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 996–1008, Apr. 2013.

[30] Y. Akazawa, H. Kikuchi, A. Iwata, T. Matsuura, and T. Takahashi, "Low power 1 GHz frequency synthesizer LSI's," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 1, pp. 115–121, Feb. 1983.

[31] J. W. M. Rogers, C. Plett, and F. Dai, *Integrated Circuit Design for High-Speed Frequency Synthesis*. Boston, MA, USA: Artech House, 2006.

[32] C. Vaucher and D. Kasperkovitz, "A wide-band tuning system for fully integrated satellite receivers," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 987–997, Jul. 1998.

[33] P. Nuzzo, K. Vengattaramane, M. Ingels, V. Giannini, M. Steyaert, and J. Craninckx, "A 0.1–5 GHz dual-VCO software-defined $\Sigma\Delta$ frequency synthesizer in 45 nm digital CMOS," in *Proc. IEEE RFIC Symp.*, 2009, pp. 321–324.

[34] M. Eissa and M. El-Shennawy, "A technique for robust division ratio switching in multi modulus dividers with modulus extension," in *Proc. Int. Conf. Microelectronics (ICM)*, 2010, pp. 84–87.

[35] A. Elkholy, A. Elshazly, S. Saxena, G. Shu, and P. K. Hanumolu, "A 20-to-1000 MHz $\pm$14 ps peak-to-peak jitter reconfigurable multi-output all-digital clock generator using open-loop fractional dividers in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 272–273.

[36] R. K. Nandwana *et al.*, "A calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolation method," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 882–895, Apr. 2015.

[37] T. H. Tsai, M. S. Yuan, C. H. Chang, C. C. Liao, C. C. Li, and R. B. Staszewski, "A 1.22 ps integrated-jitter 0.25-to-4 GHz fractional-N ADPLL in 16 nm FinFET CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

Ahmed Elkholy (S'08) received the B.Sc. (Hons.) and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2008 and 2012, respectively. Currently, he is a research assistant at University of Illinois, Urbana-Champaign, IL, USA, where he is pursuing the Ph.D. degree.

From 2008 to 2012, he was an analog/mixed-signal design engineer at Si-Ware Systems, Cairo, Egypt, designing high-performance clocking circuits and LC-based reference oscillators. He was with Xilinx, San Jose, CA, USA, during summer of 2014, working on high-performance flexible clocking architectures. His research interests include frequency synthesizers, high-speed serial links, and low-power data converters.

Mr. Elkholy received the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award (2015–2016), Analog Devices Outstanding Student Designer Award (2016), M. E. Van Valkenburg Graduate Research Award from the University of Illinois (2016–2017). He also received the IEEE SSCS Student Travel Grant Award (2015), Intel/IBM/Catalyst Foundation CICC Student Award (2015), Edward N. Rickert Engineering Fellowship from Oregon State University (2012–2013), and the Best M.Sc. Thesis Award from Ain Shams University in 2012. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, and the IEEE International Symposium on Circuits and Systems (ISCAS).

Saurabh Saxena (S'10–M'16) received the B.Tech. degree in electrical engineering and the M.Tech. degree in microelectronics and VLSI design from the Indian Institute of Technology Madras, Chennai, India, in 2009, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, IL, USA, in 2015.

He is currently an Assistant Professor in the Department of Electrical Engineering at Indian Institute of Technology Madras, Chennai. His research interests include delta-sigma modulators, high-speed I/O interfaces, and clocking circuits.

Dr. Saxena serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the IEEE International Symposium on Circuits and Systems (ISCAS).

Romesh Kumar Nandwana (S'12) received the B.Tech. degree in electronics and communication engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 2009, and the M.Eng. degree in electrical engineering from the Oregon State University, Corvallis, OR, USA, in 2013. He is currently working towards the Ph.D. degree in electrical and computer engineering at the University of Illinois, Urbana-Champaign, IL, USA.

In the summer of 2015, he was a Research Intern at Xilinx, San Jose, CA, USA, developing clocking circuits for high-speed links. He worked on low-phase noise clock buffers at Linear Technology Corporation, Grass Valley, CA, USA, as an Engineering Intern in the summer of 2011. From 2009 to 2010, he was a Scientist with the Indian Space Research Organization, Ahmedabad, India, working on the design of RF power amplifiers and DC-DC converters for communication satellites. His research interests include frequency synthesizers, digital phase-locked loops, clock and data recovery circuits, high-speed serial links, and low-voltage mixed-signal circuits.

Amr Elshazly (S'04–M'13) received the B.Sc. (Hons.) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2003 and 2007, respectively, and the Ph.D. degree from the Oregon State University, Corvallis, OR, USA, in 2012, all in electrical engineering.

He is currently a Design Engineer at Intel Corporation, Hillsboro, OR, USA, developing high-performance high-speed I/O circuits and architectures for next-generation process technologies. From 2004 to 2006, he was a VLSI Circuit Design Engineer at AIAT, Inc. working on the design of RF building blocks. From 2006 to 2007, he was with Mentor Graphics Inc., Cairo, designing multi-standard clock and data recovery circuits. His research interests include high-speed serial-links, frequency synthesizers, digital phase-locked loops, multiplying delay-locked loops, clock and data recovery circuits, data converter techniques, and low-power mixed-signal circuits.

Dr. Elshazly received the Analog Devices Outstanding Student Designer Award in 2011, the Center for Design of Analog-Digital Integrated Circuits (CDADIC) Best Poster Award in 2012, and the Graduate Research Assistant of the Year Award in 2012 from the College of Engineering at the Oregon State University. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, IEEE International Symposium on Circuits and Systems, IEEE International Conference of Electronic Circuits Systems, and IEEE Asian Solid-State Circuits Conference.

Pavan Kumar Hanumolu (S'99–M'07) received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, Corvallis, OR, USA, in 2006, where he subsequently served as a faculty member until 2013.

He is currently an Associate Professor in the Department of Electrical and Computer Engineering and a Research Associate Professor with the Coordinated Science Laboratory at the University of Illinois, Urbana-Champaign, IL, USA. His research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.

Dr. Hanumolu received the National Science Foundation CAREER Award in 2010. He currently serves as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is a technical program committee member of the VLSI Circuits Symposium and the IEEE International Solid-State Circuits Conference.