A Fractional-N Ring PLL Using Harmonic-Mixer-Based Dual Feedback and Split-Feedback Frequency Division With Phase-Domain Filtering

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***Abstract*— A phase-locked loop (PLL) employing a split-feedback divider and nested-PLL-based phase-domain low-pass filter (PDLPF) within the harmonic-mixer (HM)-based dual-feedback architecture is presented in this article. The proposed architecture not only overcomes the noise shaping frequency limitation seen in a conventional dual-feedback PLL, but also solves stability and noise overhead issues that were present in the prior art. Due to the wide loop bandwidth that can be achieved because of the effective quantization noise suppression by the proposed method, the fractional-N synthesizer is realized with low phase noise and jitter using only ring voltage-controlled oscillator (VCO), allowing an implementation that is low area and robust to magnetic coupling compared with ones using *LC*-VCOs. A proof of concept prototype is implemented in 65-nm CMOS technology that achieves a −229.4-dB jitter-power figure-of-merit (FoM) and −49-dBc worst-case fractional spurs with a 40-MHz reference.**

***Index Terms*— Dual feedback, fractional-N phase-locked loop (PLL), harmonic mixer (HM), inductorless, nested PLL, phase-domain low-pass filter (PDLPF), phase-locked loop, ring voltage-controlled oscillator (VCO), split-feedback divider.**

I. Introduction

FRACTIONAL-N phase-locked loop (PLL), using ring voltage-controlled oscillator (VCO) are challenging circuits to design, since they must deal with both the quantization noise from the multi-modulus divider (MMD) and the large phase noise from the ring VCO, as shown in Fig. 1. Canceling the deterministic quantization noise using a digital-to-time converter (DTC) is an effective method with good jitter-power figure-of-merit (FoM) and low spur values being reported in recent years [1], [2], [3], [4], [5], [6], [7], [8]. However, the characteristic of DTCs is highly sensitive to process, voltage, and temperature (PVT) variations, resulting in gain error and non-linearities that lead to imperfect noise cancellation and spurs. Correcting these errors requires extensive digital calibration, where the characteristic of the DTC is altered. This, in turn, requires statistical operations to be performed and multiple coefficients to be stored and can result in long settling times and increased hardware complexity. In light of these issues, we seek to suppress the quantization noise and fractional spurs in a non-calibration-intensive manner by altering the loop topology and relying on a purely linear-time-invariant (LTI) system.

In order to reduce the MMD quantization noise and fractional spurs, our proposed work considers three concepts: 1) avoiding noise amplification within the loop; 2) increasing the delta–sigma modulator (DSM) frequency to shape the quantization noise more aggressively; and 3) adding a noise filtering function. Avoiding noise amplification can be realized by using harmonic-mixer (HM)-based feedback [9], [10], [11], [12], [13] while increasing the noise shaping frequency, and adding noise filtering can be accomplished by methods, such as split-feedback division with nested-PLL-based phase-domain low-pass filter (PDLPF) [14] and time-domain finite-impulse response (FIR) using clocked delay lines [15], [16], [17], [18], among others. However, as will be explained in detail in Section II, all these architectures have some weaknesses that limit the extent to which the quantization noise can be suppressed.

In this work, we propose a ring-VCO-based fractional-N PLL using a split-feedback divider with a nested-PLL-based PDLPF inside the HM-based dual-feedback architecture. By combining these two methods, our architecture not only retains the benefits of the two separate methods, but also overcomes issues, such as stability degradation and high noise/power overhead, that were present in the prior arts. All of these useful qualities are achieved by altering the loop transfer function using just simple circuit blocks and without relying on complex background calibration schemes such as the least-mean-square (LMS) algorithm. A prototype based

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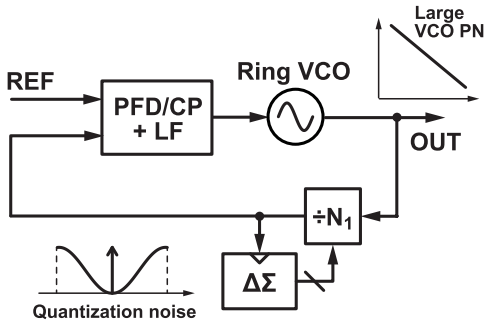

Fig. 1. Phase noise from the VCO and MMD in a ring oscillator-based fractional-N PLL.

on our proposed architecture implemented in 65-nm CMOS achieves a jitter-power FoM of −229.4 dB, which is one of the best values reported for calibration-free ring-based fractional-N PLLs, and is also comparable to the performance of some works using DTCs. We also achieve respectable fractional and reference spurs of −49 and −65 dBc, respectively. This work is an extension of [19].

The rest of this article is organized as follows. In Section II, we take a look at the relevant prior arts and explain their benefits and limitations. Then, in Section III, we show our proposed circuit, explain some of the underlying concepts, and how it resolves many of the issues present in the prior arts. The circuit implementation details are explained in Section IV. Section V shows measurement results and a performance comparison with relevant prior works, including state-of-the-art ring-VCO-based PLLs. Finally, we conclude our work in Section VI.

II. Discussion of the Prior Art

Much research has been done to come up with an effective calibration-free method to suppress the MMD quantization noise. In this section, we look at prior works that are based on three general approaches: avoiding the amplification of the quantization noise, increasing the noise shaping frequency, and adding a filtering function for the quantization noise.

A. Avoiding Noise Amplification

A significant contributing factor for the large MMD quantization noise is the noise amplification in the PLL. As can be seen in Fig. 2(a), the input-referred noise in a feedback system gets amplified by the inverse of the feedback gain β, assuming that the open-loop gain $A(s)\beta$ is sufficiently large. Applying this concept to a fractional-N PLL, we can see that the MMD quantization noise referred to the PLL input (equivalently, the MMD output) gets amplified by the division ratio $N+\alpha$, because the feedback gain β is $[1/(N+\alpha)]$. For practical values of $N+\alpha$, this amplification factor can reach tens of dB, leading to a significant degradation of the output spectrum. On the other hand, if we can use a mixer or HM to perform feedback through frequency subtraction instead of frequency division, as shown in Fig. 2(b), the feedback gain becomes unity, and we are able to avoid noise amplification.

Multiple works in recent years have made use of this concept [9], [10], [11], [12], [13]. A simple and straightforward method is the dual-feedback architecture [9], [10]. As shown in Fig. 3, by using two feedback paths, one based

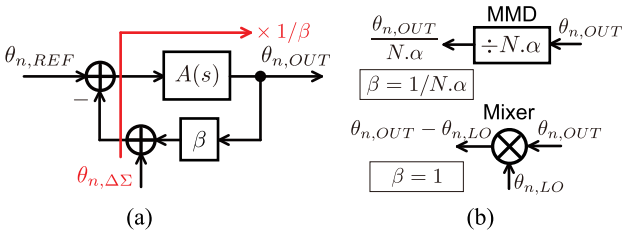

Fig. 2. (a) Amplification of noise in a general feedback system. (b) Two forms of feedback in a PLL [9].

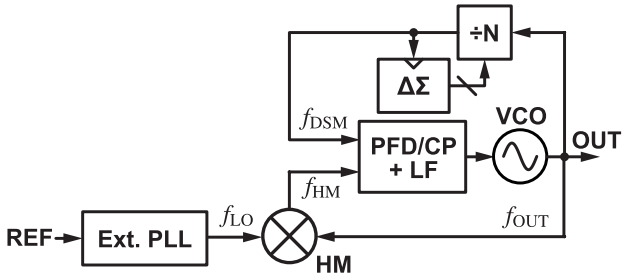

Fig. 3. Dual-feedback PLL architecture for avoiding quantization noise amplification [9], [10].

on an HM and the other based on an MMD, the architecture simultaneously achieves fractional-N operation and avoidance of noise amplification, because the total feedback gain is $1-(1/(N+\alpha)) \approx 1$.

Unfortunately, although the dual-feedback architecture successfully avoids the amplification of the quantization noise, it also has some weaknesses that make the noise suppression insufficient for allowing the use of a ring VCO. A key limitation of the dual-feedback architecture is the DSM noise shaping frequency. As shown in Fig. 4, the HM is usually implemented with an sample-and-hold (S/H) circuit [9], [10], [11], [12], [13]. Therefore, its output contains not only the desired signal component at the HM output frequency f_{HM}, but also some high-frequency tones at $f_{SH} \pm f_{HM}$ (f_{SH} is the S/H clock frequency), which must be filtered out or they can get aliased in-band during phase detection [20], [21]. Here, if we increase f_{HM} too much relative to f_{SH}, the desired signal and unwanted tones will become close to each other in the frequency domain, making it difficult to filter out the high-frequency tones. So, f_{HM} cannot be made very high. Since $f_{HM} = f_{DSM}$ during lock, this means that the DSM frequency also cannot be very high, which, in turn, means that the maximum loop bandwidth is limited, because the quantization noise cannot be shaped aggressively enough to high frequencies. It is also worth noting that the HM can contribute phase noise to the PLL output, although this fortunately is not usually a major issue thanks in part to the fact that the HM noise also does not get amplified, and can be implemented without large noise and power penalties.

B. Increasing the Noise Shaping Frequency

Another approach to suppress the quantization noise is to increase the DSM frequency. By doing so, the quantization noise is shaped to a higher frequency and can be filtered out even with a wide loop bandwidth. A simple way to do this is to multiply the reference frequency by an integer value using a reference multiplier [22], [23], [24]. Although

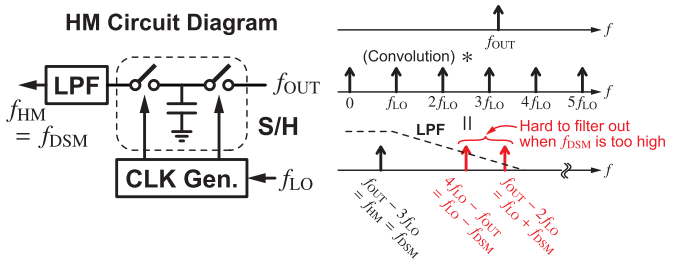

Fig. 4. HM circuit and the limitation of its output frequency due to unwanted tones.

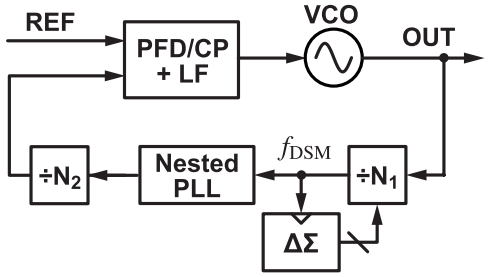

Fig. 5. Use of a split-feedback divider with a nested-PLL-based PDLPF to increase the noise shaping frequency [14].

the concept is straightforward, a reference multiplier can introduce non-negligible phase noise and power consumption of its own, as well as added design complexity, often in the form of duty-cycle correction (DCC) and other background calibration schemes. Furthermore, these issues often become more serious, as we increase the reference multiplication ratio.

We can also increase the noise shaping frequency by splitting the feedback divider into two parts and clocking the DSM with the intermediate signal. This alone will not work, because the second-stage divider acts as an edge selector that samples the input phase, meaning that the high-frequency quantization noise generated by the first-stage divider will get aliased to low frequencies, preventing it from being filtered by the low-pass characteristic of the loop. To overcome this issue, Park et al. [14] inserted a PDLPF for anti-aliasing in the form of a nested PLL, as shown in Fig. 5. While this successfully allows us to increase the DSM frequency without noise folding, the nested PLL itself contributes noise to the overall PLL output resulting in significant overhead. It also degrades the loop stability, because the transfer function of the nested PLL affects that of the entire loop. Another clever way to prevent noise folding was recently proposed in [25]. In this method, the second-stage divider utilizes a multi-phase output, so that all the edges of the first-stage output are preserved even after frequency division. These phases are then compared with the reference using multiple XOR PDs. Since XOR PDs can operate properly even with some input phase offset, the multiple phases from the feedback divider can all be compared with that of the reference signal. While simple and efficient, the linear range of the multi-XOR PD is limited, because all of the XOR PDs must operate in the linear region, meaning that the ratio by which the effective reference frequency can be multiplied is limited. Furthermore, the XOR PD output contains a large reference frequency component that can lead to large spurs in the PLL output spectrum especially if we wish to employ a wide loop bandwidth.

Finally, it should be noted that although increasing the noise shaping frequency helps to suppress the quantization noise, the extent to which it can be increased will ultimately be limited by the power consumption and possible operating frequency of the digital logic inside the DSM. Therefore, the increase in noise shaping frequency should be done within a range where the DSM operates correctly and does not consume too much power.

C. Filtering the Quantization Noise

The third approach we will look at is to add some form of low-pass filtering for the quantization noise in addition to the low-pass characteristic of the PLL. The nested PLL inserted between the split-feedback divider in the method described in Section II-B [14] is one way to perform such filtering. As was already briefly mentioned, however, a major issue here is that because the filtering gets performed on both the quantization noise and the desired feedback signal, the bandwidth of the nested PLL has to be much wider than that of the overall loop to satisfy stability requirements. In fact, according to [14], the bandwidth of the nested PLL must be at least 2.5 times wider than that of the overall loop just to achieve a 0° phase margin when considering a 10% variation in the loop bandwidths, and the actual required bandwidth ratio in a realistic design should be closer to around 5 or 6 as was the case in [14]. If we also consider the fact that the nested-PLL bandwidth must at least be narrow enough to serve as an anti-aliasing filter, we come to the conclusion that the main PLL bandwidth cannot be made very wide after all, despite the fact that we have increased the noise shaping frequency. An ideal situation would be to achieve a wide overall loop bandwidth and a narrow noise filter bandwidth while also suppressing the noise from the noise filter itself, something that we cannot achieve simultaneously with this method.

Another way to filter the quantization noise is to use a time-domain FIR filter, by either creating delayed versions of the MMD output signal [15], [16] or multiple MMDs whose control signals are delayed versions of each other [17], [18]. The important thing here is that the filtering is only performed on the quantization noise and not on the feedback signal. Therefore, the noise filter bandwidth can be designed without having to worry about the overall loop stability. That being said, it is still quite difficult to achieve effective noise suppression with a narrow noise filtering bandwidth. The generation of delayed MMD outputs in [15] and [16] requires a large number of flip-flops clocked by the high-frequency PLL output, leading to a large power consumption and a severe trade-off between noise filtering and the resulting power and complexity overhead. As for the multi-path feedback used in [17] and [18], the number of paths must be increased to improve the noise filtering, which not only leads to increased complexity, but added difficulty to achieve sufficient matching between paths.

III. Proposed Architecture

In this section, the proposed PLL architecture is shown and explained. We first show the proposed architecture and

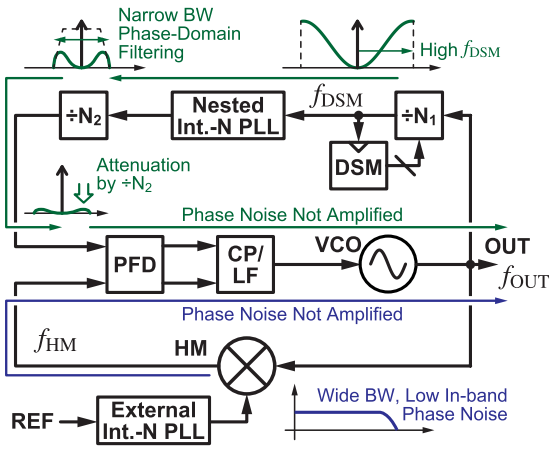

Fig. 6. Proposed architecture using the split-feedback divider with the nested-PLL-based PDLPF inside the HM-based dual-feedback architecture.

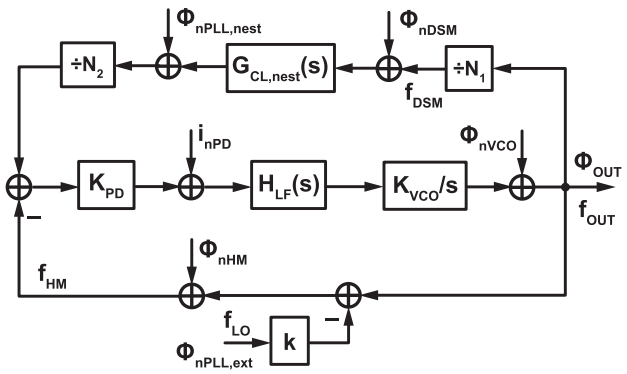

Fig. 7. Linear model of the proposed architecture with main noise sources.

explain its characteristics and advantages qualitatively. Then, we perform some detailed analysis focusing on the loop stability and noise transfer functions (NTFs). Finally, we will compare our proposed architecture with some other methods for quantization noise suppression.

A. Overview of the Proposed Architecture

The overview of the proposed PLL is shown in Fig. 6. It employs the split-feedback divider with PDLPF inside the HM-based dual-feedback architecture. By doing so, this architecture retains several benefits. First, this architecture makes use of both the avoidance of noise amplification and an increase in the DSM noise shaping frequency to achieve effective suppression of the DSM quantization noise. Second, the stability issue present in the conventional split-feedback divider with PDLPF is overcome. This is because the dc gain of the HM-based feedback path is unity, while that of the divider-based path is $(1/N_1N_2)$, meaning that the overall open-loop gain is dominated by the HM-based loop and the characteristic of the nested PLL negligibly affects the overall stability. Finally, the noise contribution from the nested PLL is greatly suppressed because of the avoidance of noise amplification due to the HM-based feedback. The second and third benefits also mean that the bandwidth of the nested PLL can be designed independently of that of the main PLL, allowing a wide bandwidth for the main PLL to suppress the ring-VCO phase noise and a narrow bandwidth for the nested PLL to help filter the quantization noise to be achieved simultaneously. In short, the proposed architecture takes advantage of all three concepts for quantization noise suppression discussed in Section II, while also suppressing the overhead from the nested-PLL-based PDLPF.

B. Stability and Noise Analysis

A linear model of the proposed architecture along with the key noise sources is shown in Fig. 7. f_{OUT}, f_{HM}, f_{DSM}, and f_{LO} are the frequencies at the overall PLL output, HM output, the DSM clock, and the LO of the HM, respectively. K_{PD}, $H_{LF}(s)$, and K_{VCO}/s are the transfer functions of the main PLL PD, its loop filter, and its VCO, respectively. The nested PLL is characterized just by its input to output transfer function $G_{CL,nest}(s)$ and a single output-referred phase noise source $\phi_{nPLL,nest}$, while the external auxiliary PLL is treated as a single equivalent noise source $\phi_{nPLL,ext}$. k is the harmonic index of the HM, i.e., $f_{HM} = f_{OUT} - kf_{LO}$. Finally, ϕ_{nVCO}, ϕ_{nDSM}, i_{nPD}, and ϕ_{nHM} are the noise components contributed by the main PLL VCO, DSM, PD, and HM, respectively, and ϕ_{OUT} is the resulting phase signal at the overall output. The PLL locks to a frequency, such that the frequencies of the feedback signals from the HM-based path and the divider-based path are equal, i.e., $f_{OUT} - kf_{LO} = f_{OUT}/(N_1N_2)$. From this, we can derive the output frequency as $f_{OUT} = (kN_1N_2/(N_1N_2 - 1))f_{LO}$.

We will first look at the stability of the main loop. The open loop gain of the main PLL is given by the following equation:

$$A_{OL}(s) = \frac{K_{PD}K_{VCO}H_{LF}(s)}{s}\left(1 - \frac{G_{CL,nest}(s)}{N_1N_2}\right). \quad (1)$$

The equation consists of two parts: one corresponding to the feed-forward gain of the loop $[(K_{PD}K_{VCO}H_{LF}(s))/s]$, which is the same as that in a typical PLL, and one corresponding to the overall feedback gain, which is equal to the difference between the two feedback paths. Focusing on the latter part, we can see that the total feedback gain is dominated by the HM-based path, because the dc gain of the divider-based path $[(G_{CL,nest}(s))/N_1N_2]$ is equal to the ratio between f_{HM} and f_{OUT}, a value that is typically much smaller than unity. For instance, if the nested PLL has a unity frequency gain, the gain of the divider-based feedback path is a low-pass characteristic with a dc gain of $(1/N_1N_2)$. Therefore, the open-loop gain in (1) can be approximated as follows:

$$A_{OL}(s) \approx \frac{K_{PD}K_{VCO}H_{LF}(s)}{s}. \quad (2)$$

In other words, the overall open-loop transfer function is nearly independent of the characteristic of the nested PLL. This, in turn, means that the bandwidth of the nested PLL can be optimized to suppress the DSM quantization noise, without worrying about stability requirements. In contrast, the simple use of a split-feedback divider with PDLPF in a conventional single-loop architecture (Fig. 5) [14] has an open loop transfer function given by the following equation:

$$A'_{OL}(s) = \frac{K_{PD}K_{VCO}H_{LF}(s)}{s}\frac{G_{CL,nest}(s)}{N_1N_2}. \quad (3)$$

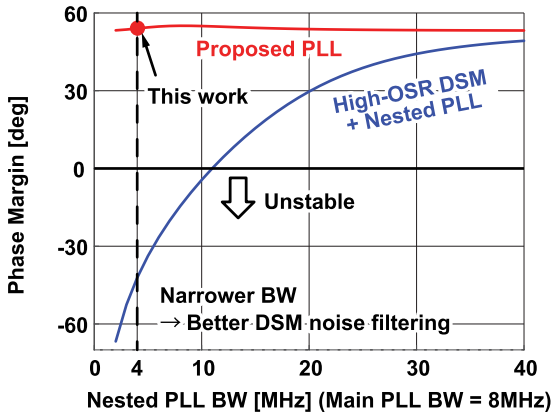

Fig. 8. Relationship between the overall phase margin and the nested-PLL bandwidth for the conventional PLL with split-feedback divider/nested-PLL filter [14] and the proposed PLL.

Now, the closed loop transfer function of the nested PLL is multiplied with the entire equation, meaning that its bandwidth has a significant effect on the overall stability. A plot showing this difference in terms of the phase margin is shown in Fig. 8. It demonstrates how, in the conventional architecture, the overall stability degrades substantially for a narrow nested-PLL bandwidth, while the degradation is negligible in the proposed architecture. Further details will be explained in Section III-C where we compare the proposed method with conventional ones.

Next, we will look at the noise contribution from each source. The NTFs from the noise sources to the output are given by the following equations:

$$\mathrm{NTF_{VCO}} \equiv \frac{\phi_{\mathrm{OUT}}}{\phi_{n\mathrm{VCO}}} = \frac{1}{1+A_{\mathrm{OL}}(s)} \tag{4}$$

$$\mathrm{NTF_{PD}} \equiv \frac{\phi_{\mathrm{OUT}}}{i_{n\mathrm{PD}}} \approx \frac{1}{K_{\mathrm{PD}}}\frac{A_{\mathrm{OL}}(s)}{1+A_{\mathrm{OL}}(s)} \tag{5}$$

$$\mathrm{NTF_{PLL,nest}} \equiv \frac{\phi_{\mathrm{OUT}}}{\phi_{n\mathrm{PLL,nest}}} \approx \frac{1}{N_2}\frac{A_{\mathrm{OL}}(s)}{1+A_{\mathrm{OL}}(s)} \tag{6}$$

$$\mathrm{NTF_{HM}} \equiv \frac{\phi_{\mathrm{OUT}}}{\phi_{n\mathrm{HM}}} \approx \frac{A_{\mathrm{OL}}(s)}{1+A_{\mathrm{OL}}(s)} \tag{7}$$

$$\mathrm{NTF_{DSM}} \equiv \frac{\phi_{\mathrm{OUT}}}{\phi_{n\mathrm{DSM}}} \approx \frac{G_{\mathrm{CL,nest}}(s)}{N_2}\frac{A_{\mathrm{OL}}(s)}{1+A_{\mathrm{OL}}(s)} \tag{8}$$

$$\mathrm{NTF_{PLL,ext}} \equiv \frac{\phi_{\mathrm{OUT}}}{\phi_{n\mathrm{PLL,ext}}} \approx k\frac{A_{\mathrm{OL}}(s)}{1+A_{\mathrm{OL}}(s)} \tag{9}$$

where all of the approximations are based on the fact that the feedback gain is approximately unity.

The NTF for the main VCO $\mathrm{NTF_{VCO}}$ is given by (4). It is a similar high-pass characteristic to that of other conventional PLLs.

The NTF for the PD $\mathrm{NTF_{PD}}$ in the main PLL is given by (5), and this is a low-pass characteristic with a dc gain of $(1/K_{\mathrm{PD}})$. In contrast, the NTF for the PD in a conventional single-loop PLL would be given by

$$\mathrm{NTF_{PD,conv}} = \frac{N}{K_{\mathrm{PD,conv}}}\frac{A_{\mathrm{OL,conv}}(s)}{1+A_{\mathrm{OL,conv}}(s)} \tag{10}$$

where N, $K_{\mathrm{PD,conv}}$, and $A_{\mathrm{OL,conv}}(s)$ are the feedback division ratio, the PD gain, and the open loop gain, respectively, of the conventional single-loop PLL. This has a similar low-pass characteristic, but with a dc gain of (N/K_{PD}). In other words, the noise/power overhead and also the reference spur from the main PLL PD in the proposed architecture can be lower, because the gain is N times lower than that of the conventional PLL. Therefore, even though the proposed PLL and, more generally, the dual-feedback PLL, requires the use of at least two PDs, the one in the main PLL can be designed with low overhead.

The NTF for the nested PLL $\mathrm{NTF_{PLL,nest}}$ is given by (6), which has a low-pass characteristic with a dc gain of $(1/N_2)$. This means that the noise from the nested PLL (containing the noise from its own VCO and PD) gets attenuated by a factor of N_2 by the second-stage divider before getting low-pass filtered by the main loop. Therefore, the nested PLL can be implemented without contributing significant noise or power to the total values.

The NTF for the HM $\mathrm{NTF_{HM}}$ is given by (7), which has a low-pass characteristic with unity dc gain. This means that the output-referred noise of the HM will not be amplified, but simply low-pass filtered by the main loop before reaching the output.

The NTF for the DSM $\mathrm{NTF_{DSM}}$ is given by (8) and is one of the key points of our work, as it shows the highly effective quantization noise suppression of the proposed method. The NTF consists of a cascade of two low-pass characteristics, with an overall dc gain of $(1/N_2)$. In other words, the DSM quantization noise not only gets attenuated by a factor of N_2, but is also low-pass filtered by both the nested PLL and the main PLL, leading to highly effective suppression of the quantization noise. Also, the bandwidth of $G_{\mathrm{CL,nest}}(s)$ can be chosen independently of the bandwidth of the main PLL, as was mentioned in Section III-A, meaning that the filtering for the DSM noise can be enhanced by decreasing the bandwidth of $G_{\mathrm{CL,nest}}(s)$ while also suppressing the main VCO phase noise by increasing the cutoff frequency of $\mathrm{NTF_{VCO}}$. Furthermore, because f_{DSM} is decoupled from f_{HM}, the DSM noise shaping frequency can be increased without being affected by the limitation of the HM output frequency.

Finally, the NTF for the external PLL $\mathrm{NTF_{PLL,ext}}$ is given by (9), which has a low-pass characteristic with a dc gain of approximately k [the exact value is $(kN_1N_2/(N_1N_2-1))$], which is approximately k if $N_1N_2 \gg 1$. This can be derived from the fact that the gain from the HM clock to the HM output is k, while the gain from the HM output to the main PLL output is the inverse of the feedback gain, which is $1-1/(N_1N_2)$). In other words, the noise from the external PLL gets amplified by the ratio between the overall output frequency and the external PLL output frequency and then gets low-pass filtered by the main PLL.

C. Comparison With Conventional Methods

To make the pros and cons of our solution more clear, it is important to compare our concept with that of other types of calibration-free fractional-N PLLs. Since the proposed architecture utilizes the HM-based dual-feedback architecture and the split-feedback divider with the nested-PLL filter,

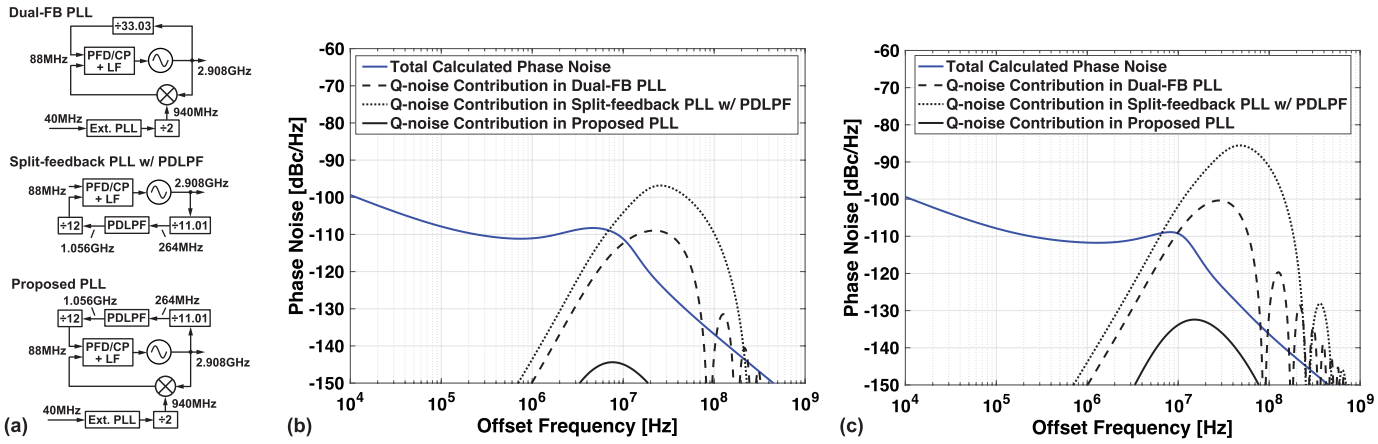

Fig. 9. (a) Conceptual diagram of the comparison settings, along with the calculated noise comparison between the quantization noise contribution in the total output phase noise spectrum for the dual-feedback PLL, the conventional PLL with split-feedback divider and nested-PLL filter, and the proposed PLL for (b) 8-MHz loop bandwidth and (c) 16-MHz loop bandwidth.

we will first compare the proposed method with these two standalone solutions.

Fig. 9(a) shows a block diagram of the circuits being compared along with their frequency settings. The configuration used for the proposed architecture matches that of our actual implementation, which will be explained in detail in Section IV. A 940-MHz clock for the HM is generated from the 1.88-GHz external PLL output, which, in turn, is generated from a 40-MHz reference and a sampling-phase-detector (SPD)-based PLL. The 940-MHz clock signal is used for the third-order HM, which downconverts the 2.908-GHz output signal to 88 MHz. At the same time, the 2.908 GHz output is divided down by a factor of $N_1 = 11 + \alpha$ with an MMD clocked by a third-order DSM to obtain a 264-MHz signal containing quantization noise. The PDLPF multiplies this frequency by 4 to generate a 1.056-GHz signal and is then followed by a divide by $N_2 = 12$ to achieve an effective divide by 3. This configuration is used instead of a simple unity gain PLL and a divide by 3 to match our actual implementation,[1] but this difference has no significant effect on the final result, since the increase in N_2 and the increase in the nested-PLL output frequency cancel each other out. The output frequency of the second-stage divider is 88 MHz, which is the same as the HM output frequency, and any deviation between the two will be corrected by the feedback in the main PLL. The bandwidths of the external, nested, and main PLLs are 20, 4, and 8 MHz, respectively. The main and nested PLLs employ phase frequency detector/charge pump (PFD/CP)-based type-II architectures.

The dual-feedback PLL and the conventional PLL with split-feedback divider and nested PLL are configured to obtain a meaningful comparison with the proposed PLL. The dual-feedback PLL has the same configuration as the proposed PLL, except for the fact that the split-feedback divider and nested PLL are replaced by a single MMD and third-order DSM that divides down the 2.908-GHz output signal to 88 MHz directly. For the PLL with split-feedback divider and nested PLL, the HM-based feedback path is removed, and an 88-MHz signal is provided as a reference signal. The bandwidth of the main PLL is 8 MHz, which is the same as that of the proposed PLL, but the nested-PLL bandwidth is widened to 48 MHz. This is necessary to maintain the stability of the overall loop.

Both conventional architectures have limitations that the proposed PLL solves. As was discussed in Section II and analyzed in detail in [20], the output frequency of the HM cannot be made too large relative to the clock frequency for the S/H in the HM to avoid making the filtering requirements too high. At the same time, the S/H clock frequency itself cannot be made excessively large, because for ring VCOs, the noise to power trade-off degrades substantially at higher frequencies due to the lowered number of stages that can be used. This means that for the dual-feedback PLL, the noise shaping frequency of the DSM is limited, which, in turn, means that the loop bandwidth cannot be made very wide. The proposed PLL also offers significant advantages compared with the PLL with split-feedback divider and nested-PLL filter. First, because of the avoidance of noise amplification due to HM-based feedback, both the quantization noise from the DSM and the phase noise from the nested PLL are greatly suppressed. For the proposed architecture, the noise from the nested PLL and the DSM are attenuated by a factor of N_2 as can be seen from (6) and (8). On the other hand, for the single-loop topology [14], both the DSM quantization noise and the nested-PLL phase noise are amplified by a factor of N_1, because the feedback gain of the first-stage divider is $(1/N_1)$. As a result, the proposed architecture achieves N_1N_2 times better suppression of both the DSM quantization noise and the nested-PLL phase noise.

Another significant advantage of the proposed method is that the nested PLL has a negligible effect on the overall open-loop gain, and its bandwidth can be chosen independently of the main loop characteristics. Fig. 8 shows the relationship between the bandwidth of the nested PLL and the phase margin of the main PLL when the bandwidth of the main PLL is fixed to 8 MHz. For the conventional method

[1] A ring VCO operating at around 1 GHz was already available beforehand, so it was used instead of designing a new 264-MHz ring VCO to save design effort.

with just the split-feedback divider and nested PLL, the phase margin degrades substantially for lower bandwidths and around 12 MHz bandwidth, which corresponds to 1.5 times that of the main loop, and is required just to achieve a 0° phase margin. This factor can increase to 5 or 6 if we wish to obtain a more practical phase margin. Meanwhile, the proposed method suffers from no such degradation for the phase margin, and the nested-PLL bandwidth can be chosen without worrying about the overall loop stability. A potential concern here is that a narrower nested-PLL bandwidth would increase the nested VCO noise contribution and reduce the benefit of the proposed PLL. However, this will not be the case with an appropriate choice of the loop bandwidth. The nested-PLL bandwidth does not have to be extremely narrow, and a bandwidth similar to or slightly narrower than that of the main PLL is enough to enhance the filtering of the quantization noise. If we combine this with the fact that the nested-PLL noise contribution is attenuated by a factor of N_2 as opposed to the conventional architecture where it is amplified by N_1, we can conclude that with an appropriate loop bandwidth, the nested PLL can improve the quantization noise suppression while still contributing negligible noise to the overall output.

Fig. 9(b) shows the calculation results, where we show the calculated output phase noise of our PLL, along with the calculated phase noise contributions from the DSM quantization noise in the dual-feedback PLL, the PLL with the split-feedback divider and nested-PLL filter, and the proposed PLL. For the two conventional PLLs, the noise degradation expected from the quantization noise greatly exceeds the total phase noise achieved in our design, while the proposed architecture suppresses the quantization noise to a negligible level. Furthermore, although the main PLL bandwidth is limited to around 1/10 of the HM output frequency, because we are assuming a PFD/CP-based type-II architecture, the loop bandwidth can be made even wider if we employ an SPD-based type-I architecture, in which case the gap between the two cases will be even larger.

Fig. 9(c) shows a similar phase noise comparison where we extended the main PLL bandwidth to 16 MHz (around 1/5 of the main PLL input frequency) and the nested-PLL bandwidth in the proposed case to 8 MHz. The nested-PLL bandwidth in the conventional PLL was extended to 96 MHz to maintain the bandwidth ratio of 6 required for stability. The noise degradation for all the architectures is even worse than before due to the reduced low-pass filtering of the quantization noise from the main and nested PLLs, but for the proposed PLL, it is still negligible compared with the overall phase noise.

Another architecture worth mentioning is the cascaded PLL, where an integer-N PLL is used as the first stage to provide a high-frequency reference to increase the noise shaping frequency for the quantization noise in the second-stage fractional-N PLL. In terms of quantization noise suppression, this method is similar to the split-feedback-divider-based PLL with PDLPF [14], because both architectures rely solely on increasing the noise shaping frequency to suppress the quantization noise, although there are some other differences, such as the absence of loop stability issues in the cascaded PLL and some extra noise filtering from the nested PLL in the split-feedback-divider-based PLL. This means that a similar noise degradation to that seen in Fig. 9(b) and (c) is expected in a cascaded PLL, and the advantages of the proposed method still hold. The reader may also refer to a comparison between the cascaded PLL and the split-feedback-divider-based PLL given in [14].

Finally, it is important to further elaborate on the pros and cons of the proposed PLL when compared with the DTC-based PLL. The comparison will be made in terms of the phase noise and the settling time. The total settling time of the proposed PLL will be much less than that of the DTC-based PLL, because the locking process only consists of the loop transient, and time consuming processes such as gain and linearity calibration are not required. A potential concern here is that because the proposed architecture makes use of three PLLs, the overall locking time will increase, because the individual PLLs must lock in order. This is not the case, however, since there will be a large overlap between the three locking transients, and the overall locking time will be dominated by that of the slowest loop. To demonstrate this and also obtain an estimate of the worst-case locking time, we performed behavioral simulations of the proposed PLL as well as the three individual PLLs and compared the locking time of the proposed PLL with the sum of the locking times of the individual PLLs. The initial frequency error from the desired values was set to 100, 100, and 50 MHz for the main, external, and nested PLLs, respectively, which is the largest frequency error when assuming that the coarse tuning code for the VCOs is set to the correct values. Fig. 10 shows the locking transients along with block diagrams of the corresponding circuits. The locking time of the overall PLL within a ±2-MHz band error is 460 ns, while the simple sum of the locking times of the individual PLLs within the same band error is 1.11 μs. This shows that the degradation in locking time due to the use of 3 PLLs is small. Furthermore, the locking time of 460 ns is significantly short compared with the reported locking times of the DTC-based architectures, whose calibration can take tens of μs to even ms in the worst case to settle [1], [2], [3], [4], [7], [8].

As for the jitter power performance, both the proposed PLL and the DTC-based PLL suppress the quantization noise to a negligible level, and the proposed PLL suffers from the jitter and power contribution from the extra loops, while the DTC-based PLL suffers from that of the DTC. The DTC contributes white noise at the PLL input whose noise is in a trade-off relationship with the power consumption. An optimization can be made based on the increase in in-band phase noise and the penalty in power consumption. For the proposed PLL, the overhead compared with a single-loop PLL comes from having one extra VCO, since the nested PLL and the main PLL PD contribute negligible noise and power because of the HM-based feedback that avoids their noise being amplified. The actual effect of having an extra VCO depends on the bandwidths of the external and main PLLs. Assuming that the bandwidths are properly chosen to minimize the overall phase noise, if the bandwidth of one of the PLLs ends up much wider than that of the other, the overall noise and power

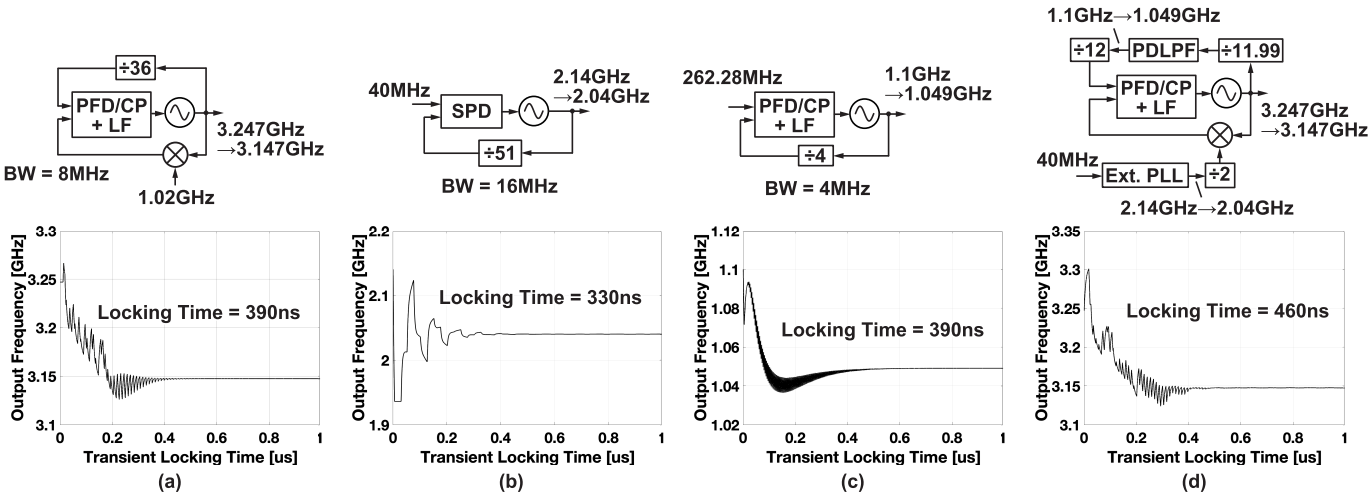

Fig. 10. Simulated locking transients and corresponding block diagrams of (a) standalone main PLL, (b) standalone external PLL, (c) standalone nested PLL, and (d) overall PLL.

will be dominated by the PLL with the narrower bandwidth, and the penalty compared with the single-loop case will be small. On the other hand, if the two PLLs end up having a similar bandwidth, the noise and power consumption will be degraded.

In summary, both the DTC-based PLL and the proposed PLL suppress the quantization noise to a negligible level, but the proposed PLL achieves a faster locking time, because it avoids calibration. The DTC-based PLL suffers from noise and/or power contribution from the DTC, while the proposed PLL suffers from noise and/or power contribution from one extra VCO. The extent to which this extra VCO degrades the overall performance depends on the loop bandwidths.

In conclusion, our proposed architecture has distinct advantages over both the HM-based dual-feedback architecture and the split-feedback divider with nested-PLL-based filter. This shows that by allowing the utilization of multiple approaches for quantization noise suppression, the proposed PLL is indeed effective for improving phase noise performance.

IV. Circuit Implementation

Fig. 11 shows the details of our design. The external auxiliary PLL employs a type-I SPD-based architecture to increase the PD gain and achieve a wide loop bandwidth. The nested and main PLLs employ a type-II PFD/CP-based architecture. As was explained in Section III-C, from a jitter/power performance stand point, it is preferable to use an SPD-based architecture for the main PLL as well, so that the loop bandwidth can be extended to its limit. However, this would require a coarse frequency locked loop (FLL), since the frequency variation of the feedback signal from the HM-based path is much larger than that in a conventional PLL due to the direct downconversion operation. As such, we settled for the somewhat limited bandwidth offered by the PFD/CP architecture, which still allows a wide enough bandwidth to demonstrate the effectiveness of the proposed method while being realizable with less design complexity. All three PLLs use VCOs based on differential ring oscillators. The DSM for the MMD is of the third order, and its operating frequency is between 230 and 314 MHz. The choice of this frequency is based on the fact that while a higher DSM frequency generally leads to improved noise shaping, it cannot be so high that the DSM fails to operate correctly or consumes too much power. Techniques, such as true single-phase clock (TSPC)-based logic and the split-bus DSM architecture, can be employed to increase the DSM frequency further [15].

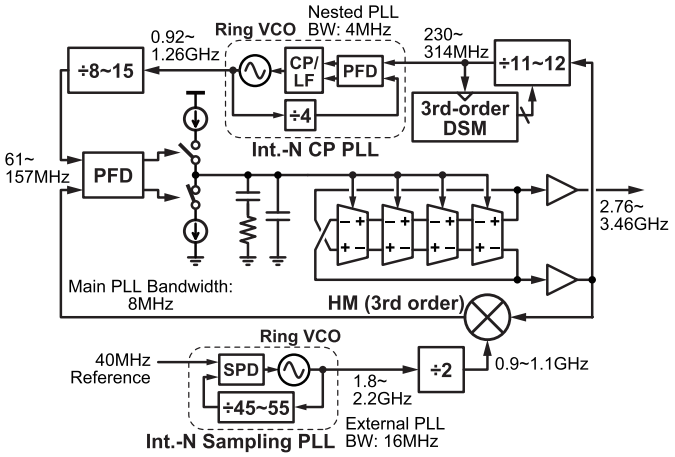

Fig. 11. Details of the overall circuit implementation.

The detailed diagram of the external auxiliary PLL is shown in Fig. 12. It is based on a simple type-I architecture using a two-stage S/H circuit to achieve a wide bandwidth. An SPD is used instead of a sub-sampling PD (SSPD) to achieve robust locking, although in a similar situation to the main PLL, an SSPD with a FLL can be used if we wish to further reduce the noise and power consumption. The slope generator is based on an inverter with a tunable output resistance. It is worth noting that while it is not a focus of our work, the PVT variation of the SPD gain can have an impact on the overall performance of the proposed PLL. Techniques, such as the one recently introduced in [27], can be used to mitigate this issue.

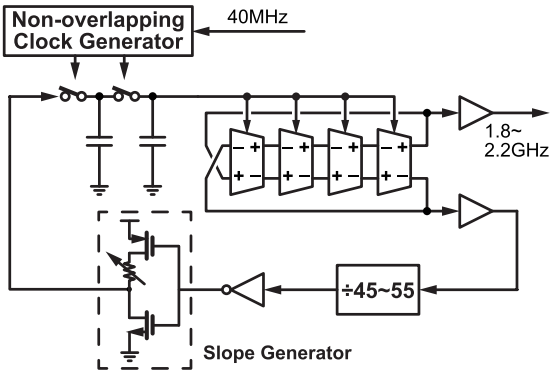

Fig. 12. Details of the external PLL implementation.

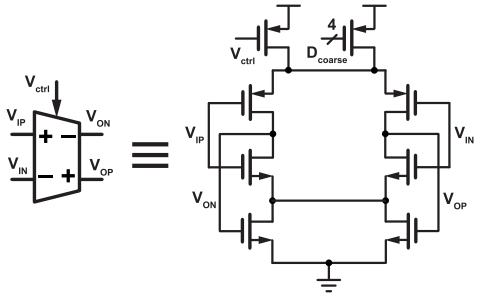

Fig. 13. Architecture of the delay cell used in the VCOs.

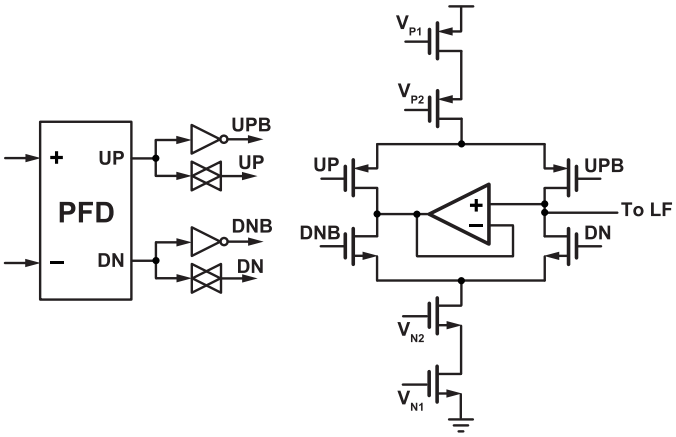

Fig. 14. Circuit diagram of the CP employing cascode current sources and dummy current paths.

The ring VCOs in the main, external, and nested PLLs are differential ring VCOs with four, four, and three stages, respectively. All three VCOs are based on current-starved delay cells similar to the one used in [28], as shown in Fig. 13. The CPs in the main and nested PLLs employ cascode current sources with a complementary current path to suppress on/off transients. The detailed PFD/CP circuit diagram is shown in Fig. 14. The HM circuit is shown in Fig. 15. The S/H is realized using a simple two-stage sampler, based on an architecture similar to that in the SPD of the external PLL. This S/H is followed by a fourth-order LPF to suppress the unwanted high-frequency tones at the S/H output [20].

Fig. 16 shows the chip micrograph along with the power breakdown. The design was fabricated in a 65-nm bulk CMOS process, and the layout occupies a core area of 0.112 mm^2. The

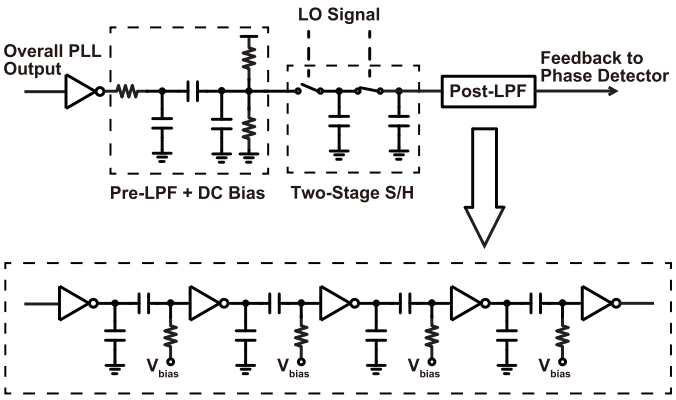

Fig. 15. Circuit diagram of the HM based on a two-stage S/H.

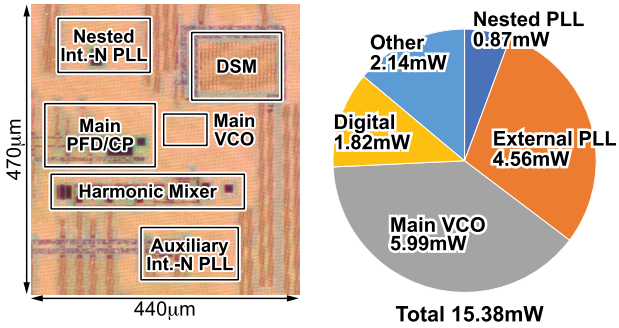

Fig. 16. Chip micrograph along with the power consumption breakdown.

total power consumption is 15.38 mW (excluding the input and output buffers), of which just 0.87 mW (5.7%) is consumed by the nested PLL. This shows that the split-feedback divider with PDLPF in our design can be implemented with a low power overhead.

The circuit was measured in a chip onboard configuration. All the supply voltages have a nominal value of 1.2 V and are generated by onboard LDOs whose supplies come from a single external regulated voltage generator. The 40-MHz reference signal is generated by an external signal generator (R&S SMA 100 B).

V. Measurement Results

Figs. 17 and 18 show the measured phase noise spectra of the external and nested PLLs in standalone operation, their calculated phase noise, and the measured phase noise of their respective VCOs in free-running mode.[2] Reference spurs at 40 MHz and its second-harmonic frequency are observed in Fig. 17 for the external PLL. For the standalone operation of the nested PLL, a 264.35-MHz reference signal was given from an external signal generator to match the operation frequency during the overall operation. In Fig. 17, a slight deviation can be seen between the calculated and measured phase noise of the external PLL at around 20 MHz. This is likely due to the process variation of the SPD gain, but the effect on the overall phase noise is minimal, due to the

[2]The phase noise spectra of the free-running VCOs only extend to 40 MHz due to the limitation of our signal source analyzer (Keysight E5052B) in wide acquisition mode.

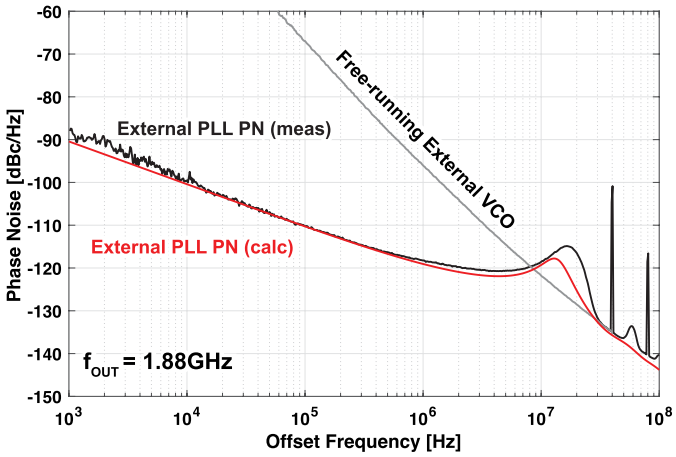

Fig. 17. Measured output phase noise of the external PLL in standalone operation (black line), the calculated phase noise of the external PLL (red line), and the measured phase noise of the external VCO in free-running mode (gray line).

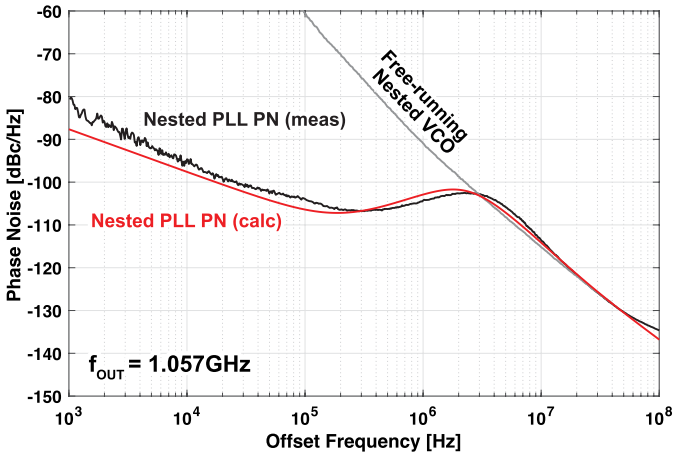

Fig. 18. Measured phase noise of the nested PLL in standalone operation with a 264.35-MHz external reference (black line), the calculated phase noise of the nested PLL (red line), and the measured phase noise of the nested VCO in free-running mode (gray line).

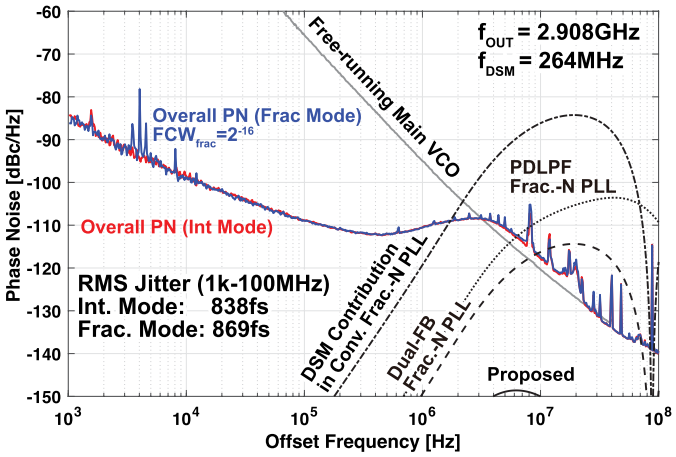

Fig. 19. Measured output phase noise in integer (red line) and fractional (blue line) modes, the measured phase noise of the main VCO in free-running mode (gray line), and the calculated contribution from the DSM quantization noise in the proposed PLL (black solid line), dual-feedback fractional-N PLL (black dashed line), fractional-N PLL using split-feedback divider and PDLPF (black dotted line), and single-loop fractional-N PLL (black dashed-dotted line).

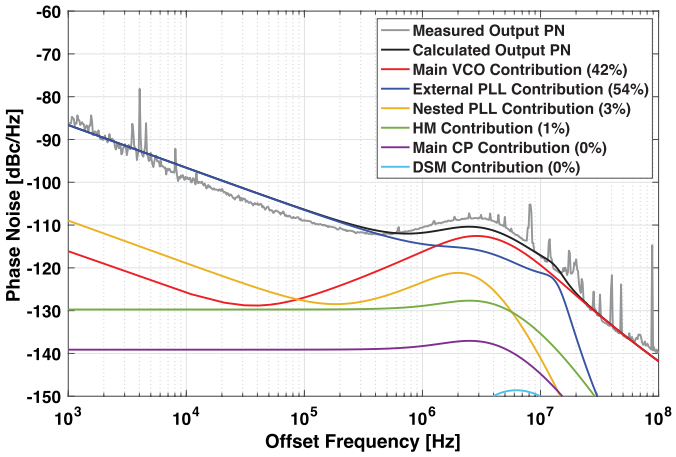

Fig. 20. Measured output phase noise (gray line) along with the calculated phase noise (black line) and contributions from various blocks.

low-pass characteristic of the main PLL. As for the nested PLL shown in Fig. 18, the measured phase noise matches the calculated phase noise well.

Fig. 19 shows the measured phase noise in integer and fractional modes in the red and blue solid lines, respectively, where the carrier frequency is around 2.908 GHz. The fractional part of the frequency control word referred to as FCW_{FRAC} is equal to 2^{-16} for the fractional mode case. It also shows the expected noise contribution from the DSM in a dual-feedback PLL, a PLL with split-feedback division and PDLPF, and a conventional fractional-N PLL in black dashed, dotted, and dashed-dotted lines, respectively, assuming the same loop bandwidth and PFD/CP frequencies for these comparisons as that in our design. The expected noise contribution in the conventional architectures contains large peaks at high frequencies that are not observed in the measured phase noise. Since the difference in phase noise between the integer and fractional modes corresponds to the noise contribution from the DSM, this result shows that the proposed method successfully suppresses the quantization noise much more effectively than the prior arts. The expected DSM noise contribution in the proposed architecture is shown in the black solid line and is well below the overall phase noise, meaning that it leads to negligible noise degradation. The measured phase noise of the main VCO in free-running mode is also shown in gray.[2] The integrated jitter in integer mode is 838 fs, while that in fractional mode is 869 fs. The worst-case jitter over the entire tuning range is 1.03 ps, and the jitter-power FoM varies by around 2 dB over this range.

Fig. 20 shows the measured phase noise in fractional mode along with the calculated overall phase noise and contributions from various blocks. The percentage contributed from each block to the overall integrated phase noise (IPN) is also shown. We can see that the noise is mostly dominated by the main VCO and external PLL, which contribute 42% and 54% of the IPN, respectively, and the noise from other noise sources, including the nested PLL and DSM, is well suppressed with a total IPN contribution of less than 4%. It is worthy to note that the phase noise degradation due to peaking in the

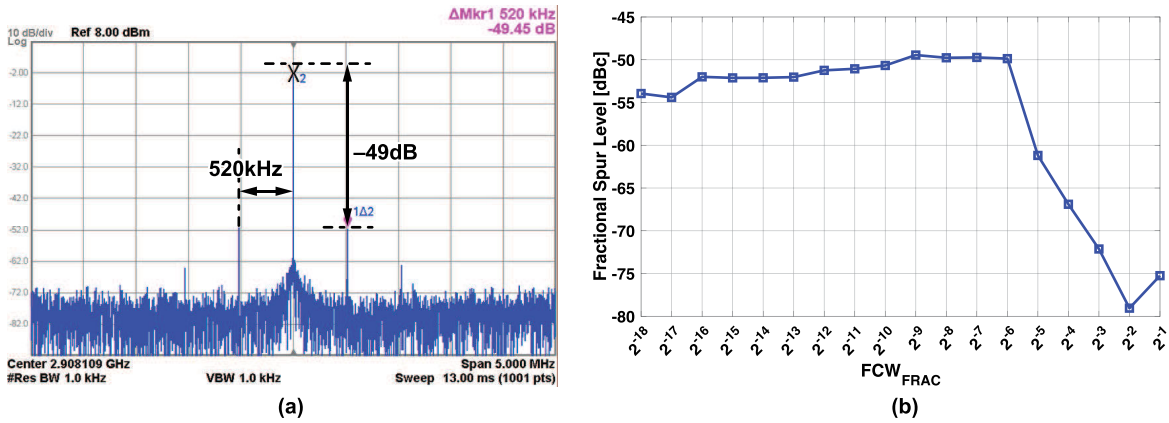

Fig. 21. (a) PLL output spectrum with low-frequency fractional spurs ($FCW_{FRAC} = 2^{-9}$). (b) Plot of the relationship between FCW_{FRAC} and the fractional spur values.

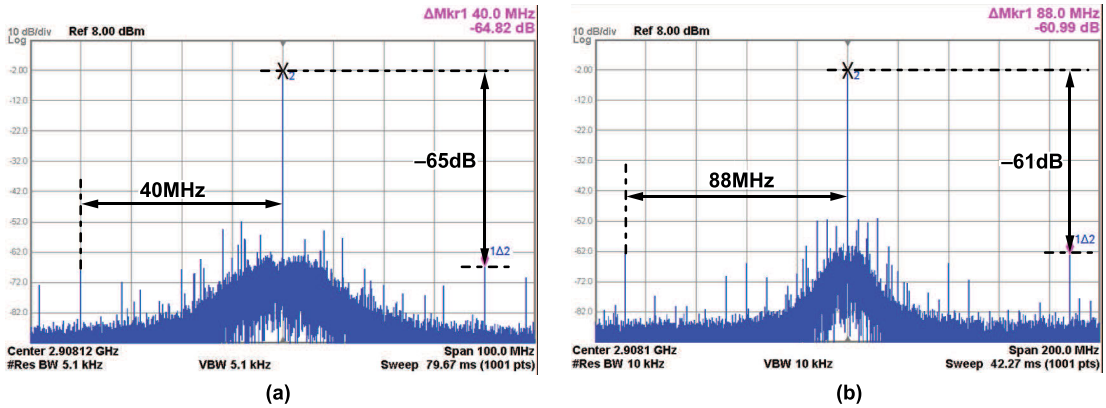

Fig. 22. PLL output spectrum containing (a) overall reference spur at 40 MHz and (b) out-of-band spur at the main PLL input frequency.

external PLL gets filtered by the main PLL and does not result in large performance degradation at the overall output. Also, the noise contribution from the main CP is suppressed to a negligible level because of the unity dc gain characteristic of the HM-based main loop. The bandwidth of the main PLL was slightly narrower than the design target of 8 MHz, and the measurement and calculation results showed the best match when the main PLL bandwidth was set to around 5.5 MHz. The calculation results in Figs. 19 and 20 are based on this adjusted bandwidth setting.

Fig. 21(a) shows the output spectrum of the PLL containing fractional spurs, and Fig. 21(b) shows a plot of the fractional spur values with respect to the corresponding FCW_{FRAC}. The worst-case fractional spur is −49 dBc. In Fig. 22(a), we can see an out-of-band spur at the external reference frequency of 40 MHz. In addition, we can see, in Fig. 22(b), an out-of-band spur at the main PLL input frequency of around 88 MHz. All of the spurs achieve relatively low values because of a combination of cascaded low-pass filtering due to the use of multiple PLLs and the avoidance of noise amplification due to the use of HM-based feedback. Specifically, the fractional spurs benefit from the avoidance of noise amplification, the reference spur at 40 MHz benefits from the cascaded low-pass filtering from the external and main PLLs, and the spur at 88 MHz benefits from the avoidance of noise amplification and the filtering from the main PLL. The spur values can be further improved based on the same techniques used to improve the spurs in single-loop PLLs, such as adding dither in the DSM, linearizing the CP by adding an offset current, or employing a more linear PD in the first place such as an XOR PD. It should be noted that the unexpected tones at 4 MHz and its harmonics seen in Fig. 22 are likely generated due to coupling between the DSM and the reference frequency blocks, since the frequency of the tones is always equal to the DSM frequency minus a multiple of the reference frequency, and the amplitude of the tones is sensitive to the reference and digital supplies. Therefore, they can be mitigated with a better substrate separation and possibly by separating the power supply and ground more carefully. The worst-case coupling spurs are observed to be around −50 dBc. We also observed some leakage from the external PLL output in the overall output spectrum causing around a −53-dBc tone. This too can likely be suppressed by improving the substrate and power supply isolation.

Fig. 23 shows an example of the frequency transients of all the PLLs (black line) measured at the same time, along with their smoothed out versions based on moving average filtering with an averaging factor of 50 (red line). Here, the external PLL frequency changed from 1.88 to 2.04 GHz, the nested-PLL frequency changed from 1.057 to 1.049 GHz,

TABLE I
PERFORMANCE COMPARISON

	This Work	[4] Park JSSC'22	[5] Zhang JSSC'22	[6] Elkholy JSSC'16	[7] Zhang JSSC'23	[8] Santiccioli JSSC'19		[9] Osada SSCL'20	[14] Park JSSC'12		[15] Kong JSSC'17	[16] Kong JSSC'18	[18] Zhang JSSC'20
Method	Dual-Feedback + Split Feedback + PDLPF	DTC w/ 1/8 range reduction	MDLL w/ DTC + TP Calibration	DTC + extended range MMD	MDLL w/ Injection Error Scrambling	MDLL w/ DTC range reduction		HM-based Dual-Feedback	Split-Feedback + PDLPF		Cascaded PLL w/ DSM + Time-Domain FIR	DSM + Time-Domain FIR	DSM + space-time averaging
VCO Topology	Ring	Ring	Ring	Ring	Ring	Ring		LC	Ring	LC	Ring	Ring	Ring
Calibration Required?	No	Yes	Yes	Yes	Yes	Yes		No	No	No	No	No	No
Ref. Freq. [MHz]	40	100	50	50	50	100		~800	32	60	22.6	22.6	50
Output Freq. [GHz]	2.9	5.2	1.5	5.2	1.5	1.65	3.05	3.5	2.4	2.4	2.4	2.4	2.4
BW [MHz]	5.5	70	10*	5	20*	30*		0.8	2	2	10	5.7	2.8
RMS Jitter [fs] (Integ. Range)	869 (1k-100M)	188 (1k-30M)	1690 (10k-10M)	1860 (10k-100M)	800/1000 (10k-10M/10k-30M)	397 (30k-30M)	376 (30k-30M)	503 (10k-100M)	4065**	3227**	1680 (10k-50M)	1500 (10k-50M)	2260 (1k-100M)
Ref. Spur [dBc]	–65/–61***	–64	–43	–44	–58	–56	–54.5	–69	–60	–54.7	–70	–60	–67
Frac. Spur [dBc]	–49	–59	–52	–42	–67	–51.5	54.8	–65	–37	–45	–52.5	–41	–47
Power [mW]	15.38	15.67	11.95	4	13.56	2.5	3.35	6.9	15.2	9.6	6.4	10	4.85
FoM† [dB]	–229.4	–242.6	–224.8	–228.5	–230.6/–228.7	–244	–243.2	–237.6	–216	–220	–227.4	–226.5	–226.1
Locking Time [us]	0.46††	500†††	N/A	N/A	2000†††	700†††		N/A	N/A		N/A	N/A	N/A
Core Area [mm^2]	0.112	0.139	0.18	0.084	0.23	0.0275		0.24	0.17	0.46	0.03	0.096	0.086
Process Node [nm]	65	65	65	65	65	65		65	130		45	45	40

*Estimated from PN spectrum **Calculated from Power Consumption and FoM ***Spur at Main PLL Input Frequency
†FoM = 10log10[(Jitter/1s)2 (Power/1mW)] ††Loop Transient Time †††Calibration Convergence Time

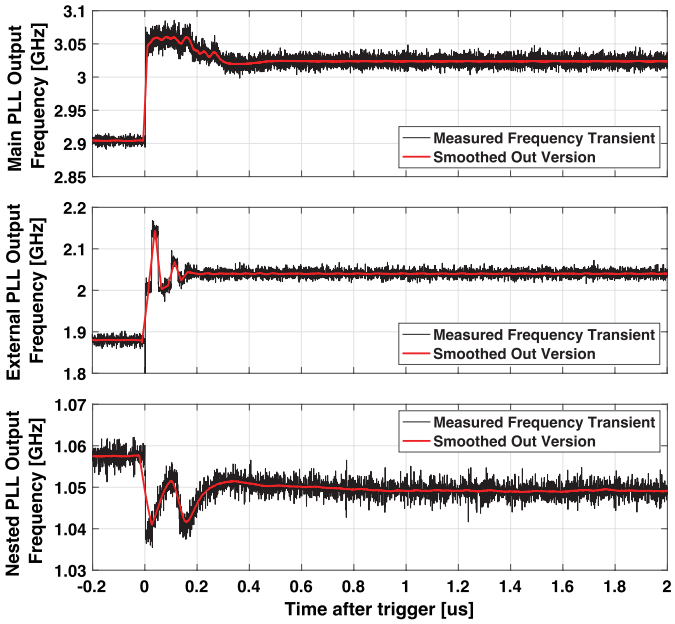

Fig. 23. Measured frequency transients of the main, external, and nested PLLs (black line) along with their smoothed out versions based on moving average filtering with an averaging factor of 50 (red line).

and the overall output frequency changed from 2.908 to 3.147 GHz. The locking time within a ±2-MHz band of the desired output frequency is around 450 ns, a value that is within the worst-case locking time predicted based on the behavioral simulation in Section III-C. Once the coarse tuning codes of the VCOs are set to the correct values, this transient is the only thing that constitutes the locking process, and we can clearly see that this offers an advantage in locking time over calibration intensive architectures just like we demonstrated in the simulation.

Table I shows a comparison of our work with other state-of-the-art ring-VCO-based fractional-N PLLs, fractional-N MDLLs, and also the works involving the HM-based dual-feedback architecture [9] and the split-feedback + PDLPF inside a single-loop PLL [14]. Among the ring-VCO-based works that do not rely on background calibration [14], [15], [16], [18], our work achieves one of the best jitter-power FoMs because of its efficient quantization noise suppression mechanism. If we look at works that employ background calibration based on noise cancellation with DTCs [4], [5], [6], [7], [8], we can see that some of these works achieve a better FoM than that of our work. However, the advantage of calibration-free operation is significant in terms of reduced locking time and complexity. Furthermore, the performance gap can be closed further with an optimal architectural choice and further design optimization. One choice is to employ a type-I SPD-based architecture instead of a type-II PFD/CP-based architecture to allow a wider loop bandwidth and suppress the main VCO phase noise. In addition, there is more room for improvement in the performance of the VCOs used in the main and the external loops, as some recent state-of-the-art ring VCOs achieve around 8-dB better FoMs [15], [16]. The HM-based dual-feedback PLL [9] achieves a better noise/power performance than our work, but is forced to use an LC-VCO due to the insufficient suppression of quantization noise. The work employing the split-feedback divider and PDLPF inside a single-loop PLL [14] has a much worse noise/power performance than our work, also due to the fact that it is forced to have a relatively narrow bandwidth because of the insufficient suppression of quantization noise. An estimation of the locking times based on the dominant factors, such as the loop transient and calibration convergence, is shown. We can see that our work achieves a far shorter locking time than the DTC-based architectures whose calibration takes hundreds of μs to even ms to converge [4], [7], [8]. Some of the works on DTC-based architectures did not report the convergence time [5], [6], but it is likely that the calibration convergence in those works also take in the order of tens of μs to ms, since the general purpose and method of the calibration algorithms are the same. The works dealing with calibration-free architectures on the other hand [9], [14], [15], [16], [18] likely settle in the order of hundreds of ns to μs, since their locking process

mostly consists of only the loop transient like in our work. Finally, it is worth noting that the core area of our work is in line with those of the other ring-VCO-based PLLs, meaning that the use of multiple PLLs in our work does not ruin the advantage of low area for ring VCOs, because each VCO can be realized with sufficiently low area.

VI. Conclusion

In this article, we proposed a ring-VCO-based fractional-N PLL that employs a split-feedback divider with a nested-PLL-based PDLPF inside the HM-based dual-feedback architecture. With the proposed architecture, we were able to achieve highly effective suppression of the quantization noise and also solve various issues, such as stability degradation and noise/power overhead, that were present in the prior arts. Detailed analysis, comparisons with conventional architectures, and measurement results were given to demonstrate the feasibility of the proposed method and its effectiveness in improving the overall phase noise performance.

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