A 1.9–3.8 GHz $\Delta\Sigma$ Fractional-N PLL Frequency Synthesizer With Fast Auto-Calibration of Loop Bandwidth and VCO Frequency

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***Abstract*—A fast and high-precision all-digital automatic calibration circuit that is highly suited for $\Delta\Sigma$ fractional-N synthesizers is designed to achieve a constant loop bandwidth and fast lock time over an octave tuning range. A high-speed frequency-to-digital converter (FDC) measures VCO frequency on-chip with a sub-$f_{\rm REF}$ frequency resolution of $f_{\rm REF}/k$ in a time period of $k \cdot T_{\rm REF}$. The on-chip detected VCO frequency is then used for calibrating the loop bandwidth and the VCO frequency. The loop bandwidth calibration circuit measures the VCO gain $K_{\rm VCO}$ and uses it to precisely control the charge pump current, hence making the loop bandwidth constant. For the VCO frequency calibration, a minimum error code finding block significantly enhances the calibration accuracy by finding the truly closest code to the target frequency. Moreover, this method does not need to activate $\Delta\Sigma$ modulator to achieve sub-$f_{\rm REF}$ calibration resolution, which makes this technique much accurate and faster than the conventional ones. A 1.9–3.8 GHz $\Delta\Sigma$ fractional-N synthesizer is implemented in 0.13 μm CMOS, demonstrating that the loop bandwidth calibration is completed in 1.1–6.0 μs with $\pm 2\%$ accuracy and the VCO frequency calibration is completed in 1.225–4.025 μs, all across the entire octave tuning range.**

***Index Terms*—Auto-calibration, constant loop bandwidth, fractional-N frequency synthesizer, loop bandwidth calibration, PLL, VCO frequency calibration.**

I. Introduction

MULTI-BAND multi-mode support by a single transceiver chip becomes a key resonating thrust in recent wireless communication circuit design. In order to avoid too many PLL synthesizers in the multi-band multi-mode RF transceivers, it is highly desirable to have a single widely-tunable PLL synthesizer that still can provide fast lock time, low phase noise, and constant loop bandwidth across the entire tuning range. Usually in PLL synthesizers, the wide tuning range is realized by employing an LC tuned VCO that has a switched capacitor bank (capbank) [1], [2], which produces closely spaced multiple sub-band tuning curves to cover the required tuning range. With the multiple sub-band tuning curves having low VCO gain $K_{\rm VCO}$, synthesizers can keep the phase noise low. However, this structure brings out severe drawbacks especially as the required tuning range becomes much wider and even over an octave. It is known that when the total capacitance of the switched capacitor bank varies in a linear proportion to the cap-bank code n, $K_{\rm VCO}$ and the sub-band frequency spacing $f_{\rm step}$ vary in a cubic power of the total tuning range [2]. For example, $K_{\rm VCO}$ and $f_{\rm step}$ will vary three octaves for an octave frequency tuning range. With such a wide variation of $K_{\rm VCO}$ and $f_{\rm step}$, PLL performances such as lock time, phase noise, and loop bandwidth will suffer from huge variation. Thus, it is highly desirable to have a fast and accurate auto-calibration of the VCO frequency and loop bandwidth so that the PLL can maintain the closed-loop characteristics relatively unchanged over a wide tuning range.

Loop bandwidth calibration is to maintain the PLL's closed-loop bandwidth constant over the tuning range. Many loop-gain calibration techniques were reported in regard to PLL based phase-modulator transmitter designs [3]–[9]. But, their calibration times could not be shortened enough due to the closed-loop operation. Much faster calibration can be done by performing the calibration in open-loop. Previous open-loop calibration techniques automatically adjust the charge pump current to compensate for pre-estimated $K_{\rm VCO}$ variation [10], [11]. But, since the actual value of $K_{\rm VCO}$ after chip fabrication could not be accurately known due to the PVT variation, these approaches showed limited accuracy.

VCO frequency calibration is the process to find the closest sub-band tuning curve to a target frequency before the PLL's closed-loop locking process begins. There had been many methods reported so far [12]–[19]. However, they all showed severe speed-resolution limitation, and more importantly, they were not suitable for the $\Delta\Sigma$ fractional-N synthesizer. The frequency counting near the reference frequency $f_{\rm REF}$ [15], [16] demonstrated rather long calibration time of over tens of μs due to the slow counting, and it should become even slower for $\Delta\Sigma$ fractional-N synthesizer. The period comparison method based on the time-to-voltage conversion [17], [18] or the PFD-based edge comparison [19] showed very fast calibration, but they could not be used for the $\Delta\Sigma$ fractional-N synthesizer if $\Delta\Sigma$ modulator is activated during the calibration for achieving sub-$f_{\rm REF}$ accuracy.

In this work, we present an auto-calibration technique for the loop bandwidth and VCO frequency. This technique is mainly

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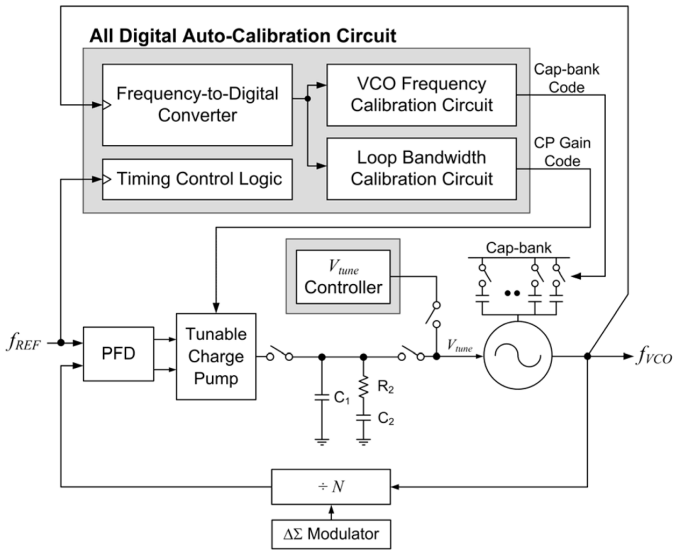


Fig. 1. Proposed auto-calibration circuit in PLL.

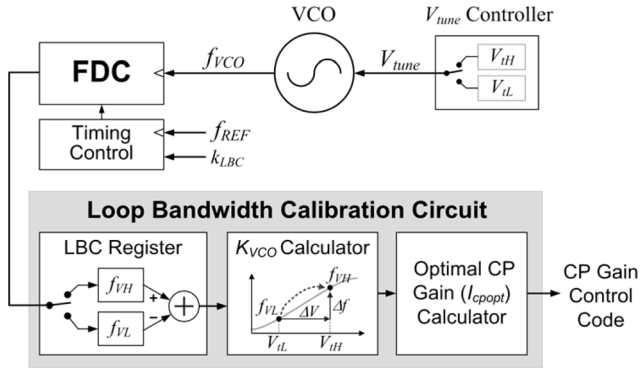


Fig. 2. Block diagram of the loop bandwidth calibration circuit.

based on a high-speed frequency-to-digital converter (FDC). The FDC accurately detects the VCO frequency on chip, and the accurate information of the VCO frequency is used for the VCO frequency calibration and the loop bandwidth calibration. The proposed calibration method operates in open-loop, which ensures fast calibration time, while it provides comparable accuracy with the conventional closed-loop calibration methods. Also, this method is highly suited for $\Delta\Sigma$ fractional-N synthesizer.

This paper is organized as follows. Section II describes the proposed auto-calibration technique for the loop bandwidth and the VCO frequency. Section III presents the design of a 1.9–3.8 GHz $\Delta\Sigma$ fractional-N PLL adopting the proposed calibration technique. Section IV describes the CMOS implementation of the PLL and measurement results. Finally, Section V presents the conclusion.

II. Proposed Auto-Calibration Technique

The FDC-based auto-calibration circuit is shown with a $\Delta\Sigma$ fractional-N synthesizer in Fig. 1. The LC VCO has a switched capacitor bank to produce multiple low-$K_{\rm VCO}$ sub-band tuning curves for covering a wide tuning range. The charge pump current is tuned to control the loop bandwidth. The auto-calibration circuit comprises a high-speed frequency-to-digital converter (FDC), a loop bandwidth calibration (LBC) circuit, a VCO frequency calibration (VFC) circuit, a timing control logic, and a $V_{\rm tune}$ controller.

The high-speed FDC counts the VCO signal in a time period of $k \cdot T_{\rm REF}$, and converts the VCO frequency $f_{\rm VCO}$ to a digital value corresponding to $k \cdot T_{\rm REF} \cdot f_{\rm VCO}$. The FDC's frequency resolution $f_{\rm res}$ is then given by

$$f_{\rm res} = \frac{f_{\rm REF}}{k}. \tag{1}$$

This FDC output is utilized for the subsequent loop bandwidth and VCO frequency calibrations. The VCO frequency calibration circuit searches for a cap-bank code that makes the VCO frequency closest to the target frequency. The loop bandwidth calibration circuit detects two VCO frequencies at two points of VCO tuning voltages $V_{\rm tH}$ and $V_{\rm tL}$, and obtains the actual $K_{\rm VCO}$ value on a chip. This $K_{\rm VCO}$ value is used to control the charge pump current for setting the loop bandwidth to a desired value. The timing control logic generates the required clock and control signals. The $V_{\rm tune}$ controller supplies three control voltages $(V_{\rm DD}/2, V_{\rm tH}, V_{\rm tL})$ to the VCO tuning node $V_{\rm tune}$ during the calibration processes.

A. Loop Bandwidth Calibration

In a charge pump PLL, the closed-loop bandwidth $\omega_{\rm LBW}$ is approximately given by

$$\omega_{\rm LBW} \approx R_2 \cdot \frac{I_{\rm CP}}{2\pi} \cdot \frac{K_{\rm VCO}}{N} \tag{2}$$

where R_2 is the loop filter resistor, $I_{\rm CP}$ is the charge pump current, and N is the PLL's total division ratio. Since the loop filter R_2 variation can be compensated by using the same type resistor in generating $I_{\rm CP}$ [7], [10], the remaining parameter to compensate for obtaining the constant loop bandwidth is $K_{\rm VCO}/N$. Previous approaches for this were based on the simulation-based estimated data of $K_{\rm VCO}$ [10], [11], which limited the calibration accuracy because it could not cope with the $K_{\rm VCO}$'s actual variation after chip fabrication. Therefore, in order to accurately compensate the $K_{\rm VCO}$ variation, accurate on-chip detection of $K_{\rm VCO}$ is required.

Fig. 2 illustrates the structure of the loop bandwidth calibration circuit. It is composed of a register, a $K_{\rm VCO}$ calculator, and an optimal charge pump gain $(I_{\rm cpopt})$ calculator. The FDC extracts two frequencies $f_{\rm VH}$ and $f_{\rm VL}$ at two tuning voltages of $V_{\rm tH}$ and $V_{\rm tL}$, respectively, which are then stored in the LBC register. Then, $K_{\rm VCO}$ value is computed by $(f_{\rm VH} - f_{\rm VL})/(V_{\rm tH} - V_{\rm tL})$. Finally the optimal charge pump current $I_{\rm cpopt}$ is found by using the relation $I_{\rm CP} \sim N/K_{\rm VCO}$. For this loop bandwidth calibration, the frequency resolution can be set to $f_{\rm REF}/k_{\rm LBC}$ by assigning $k_{\rm LBC} \cdot T_{\rm REF}$ time for the FDC's frequency counting.

The accuracy of the loop bandwidth calibration method is governed by two factors: the FDC's frequency resolution and the charge pump current resolution. First, the calibration accuracy governed by the FDC's frequency resolution can be written as

$$\mathrm{LBC}_{\rm accuracy} = \frac{1}{\lfloor K_{\rm VCO} \cdot (V_{\rm tH} - V_{\rm tL})/(f_{\rm REF}/k_{\rm LBC}) \rfloor}. \tag{3}$$

Since f_{REF} and $(V_{\mathrm{tH}} - V_{\mathrm{tL}})$ are constant, (3) indicates that the accuracy is determined by K_{VCO} and k_{LBC}. The denominator of (3) should be an integer number because the counting operation of the FDC is a quantization process in time domain. Thus, the floor function $\lfloor\ \rfloor$ is used, which gives the greatest integer value less than or equal to the real number in it. It is required to maintain the calibration accuracy constant over the wide tuning range. Since K_{VCO} will vary across the tuning range, k_{LBC} needs to be adjusted properly. For instance, with $f_{\mathrm{REF}} = 40$ MHz, $\Delta V = V_{\mathrm{tH}} - V_{\mathrm{tL}} = 0.4$ V, and K_{VCO} ranging from 20 to 160 MHz/V across an octave tuning range, k_{LBC} must be properly adjusted from 125 to 16 in order to ensure the loop bandwidth calibration accuracy within ±2%.

The second factor to affect the loop bandwidth calibration accuracy is the charge pump current resolution. Since the charge pump current is digitally controlled, its discrete change will affect the calibration accuracy. The calibration accuracy determined by the charge pump current resolution can be written as

$$\mathrm{LBC}_{\mathrm{accuracy}} = \frac{K_{\mathrm{VCO,max}}/N_{\mathrm{max}}}{K_{\mathrm{VCO,min}}/N_{\mathrm{min}}} \cdot \frac{1}{m_{\mathrm{cp}}} \tag{4}$$

where m_{cp} is the number of steps of the charge pump current. In order not to diminish the overall calibration accuracy, m_{cp} should be sufficiently large. For example, for an octave tuning range, K_{VCO} and N will vary by 8 and 2 times, respectively, then K_{VCO}/N will vary by 4 times. In order to guarantee the calibration accuracy within ±1.5%, m_{cp} should be at least 7-bit resolution (128 steps).

B. VCO Frequency Calibration

The VCO frequency calibration circuit structure is shown in Fig. 3. It comprises a frequency error (f_{err}) detector, a minimum error code finder, a binary searcher, and a final code selector. At the start of the calibration process, V_{tune} is fixed at $V_{\mathrm{DD}}/2$, and the FDC converts the VCO frequency to a digital value $f_V(n)$ with a conversion resolution of $f_{\mathrm{REF}}/k_{\mathrm{VFC}}$ in the time of $k_{\mathrm{VFC}} \cdot T_{\mathrm{REF}}$. After this, $f_V(n)$ is compared with the target frequency value $f_{\mathrm{target}} (= k_{\mathrm{VFC}} \cdot N_{\mathrm{target}})$ and the frequency error $f_{\mathrm{err}}(n)$ $(= f_V(n) - f_{\mathrm{target}})$ is obtained. The target frequency f_{target} is precisely set by letting N_{target} include fractional as well as integer. In this design, 7 bits are assigned to the fractional part, thus a resolution of $f_{\mathrm{REF}}/128$ is obtained. The sign bit of $f_{\mathrm{err}}(n)$ indicates whether the VCO frequency is higher or lower than the target frequency. This information is used for the subsequent binary search process. At the same time, the absolute value of the frequency error $|f_{\mathrm{err}}(n)|$ is stored at the minimum error code finder register. This process is repeated by C times, where C is the total number of bits of the capacitor bank. After completing the C-step search, the final code selector produces the code that has ever shown the smallest $|f_{\mathrm{err}}|$ during the binary search process. This final code selection process greatly enhances the accuracy of the VCO frequency calibration. The conventional methods of [15], [16] without such minimum error code finder and the final code selector of this work only gave an odd numbered code as a final result. A slightly improved method that was able to find a more optimal code between the last two searched codes was reported in [18]. But it should also have limited accuracy when the closest code occurs even before the last two searched codes. Compared to those previous methods, this work always provides the truly closest code to the target frequency.

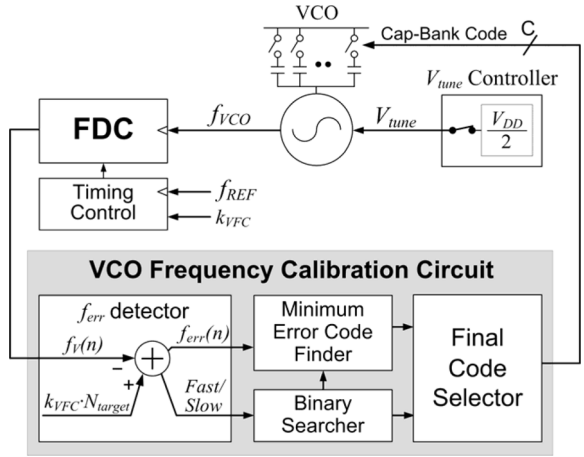


Fig. 3. Block diagram of the VCO frequency calibration circuit.

The resolution of the VCO frequency calibration is necessary to be less than f_{REF} in most fractional-N synthesizers since the sub-band frequency spacing is usually less than f_{REF} in the fractional synthesizers. However, the conventional methods in [15]–[18] will take much longer time to provide sub-f_{REF} resolution because they need to activate the ΔΣ modulator during the calibration. Another conventional method in [19] even cannot activate the ΔΣ modulator because the division ratio jittering will make the pulse edge comparison difficult, which will make it unsuitable for ΔΣ fractional synthesizers. By contrast, the calibration resolution of this work is solely determined by the FDC resolution. The FDC resolution is given by $f_{\mathrm{REF}}/k_{\mathrm{VFC}}$, which is easily set to sub-f_{REF} by simply increasing k_{VFC}. It is necessary to adjust k_{VFC} properly across the entire tuning range since $f_{\mathrm{step}}(n)$ varies in proportion to the cubic power of f_{VCO}. For instance, for an octave tuning range, f_{step} at the low end will be 8 times smaller than that at the high end. In that case, k_{VFC} needs to be adjusted by 8 times to ensure the calibration resolution to be always less than $f_{\mathrm{step}}(n)/2$. Also, it should be noted that this method does not need to activate the ΔΣ modulator during the calibration for achieving sub-f_{REF} resolution. It is because the precise target frequency is set by a digital value $k_{\mathrm{VFC}} \cdot N_{\mathrm{target}}$, whereas the conventional methods such as [15]–[18] will not know the precise target frequency unless the ΔΣ modulator is operated. Note that activating ΔΣ modulator during calibration will require much longer calibration time (at least 4 times longer [20]). As a result, the proposed method is very fast and accurate.

III. ΔΣ Fractional-N Synthesizer With the Proposed Auto-Calibration

An octave tuning range ΔΣ fractional-N PLL synthesizer is designed by employing the proposed auto-calibration technique. The PLL is a fourth-order type-II charge pump structure having a third-order passive loop filter. The PLL architecture is shown in Fig. 4. A single LC tuned VCO covers the octave

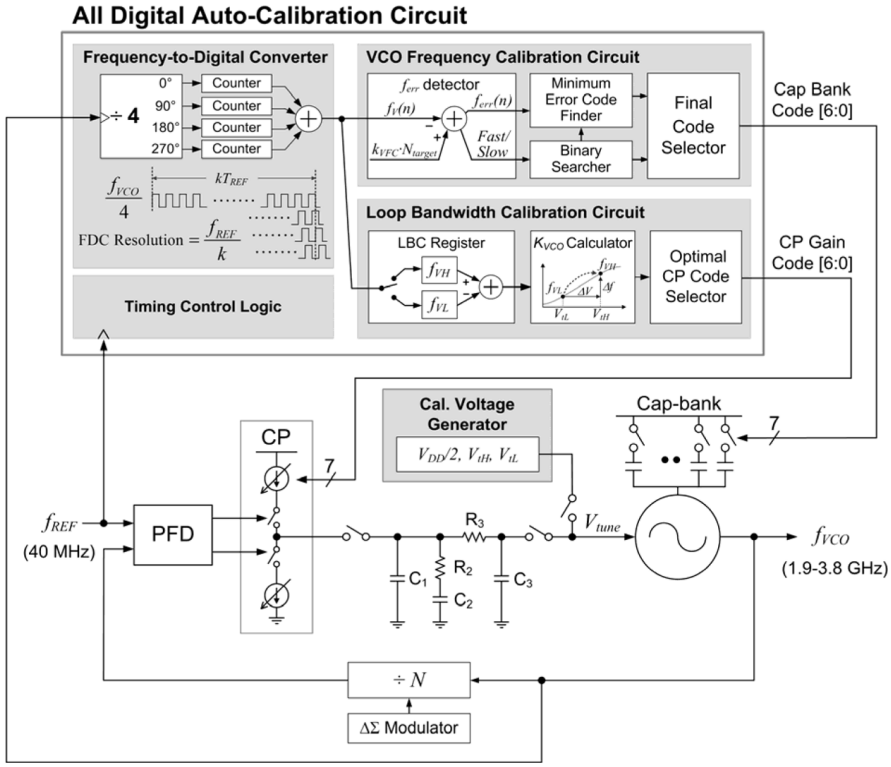


Fig. 4. The 1.9–3.8 GHz $\Delta\Sigma$ fractional-N PLL synthesizer with the proposed auto-calibration circuit.

bandwidth from 1.9 to 3.8 GHz with a 7-bit binary-weighted capacitor bank. The charge pump circuit is digitally tuned between 7.8 μA to 1 mA in 7-bit resolution to meet the required bandwidth calibration accuracy. The $\Delta\Sigma$ modulator is MASH-111 type with 20-bit resolution.

A. Auto-Calibration Circuit

The auto-calibration technique described in Section II is designed to work with the fractional-N PLL. As can be seen in Fig. 4, the high-speed FDC is fed directly by the VCO signal and first divides it down to $f_{\rm VCO}/4$ by using the quadrature-phase pre-divider. The pre-divide-by-4 circuit [20] effectively generates differential quadrature output signal from a single-ended input signal, which saves the current consumption and silicon area compared to the conventional current mode logic (CML) circuits. After the pre-divider, the subsequent four counters that connect to each of the quadrature phase output signals aggregately count the VCO frequency. With this, each counter can operate at a reduced speed of $f_{\rm VCO}/4$ while the overall counter resolution is not diminished. The sum of the four counters results represents the VCO frequency in a digital value, which is noted by $f_V(n)$, $f_{\rm VH}$, and $f_{\rm VL}$ in Fig. 4.

The operation of the calibration circuit is explained with the illustrations of Fig. 5. Fig. 5(a) depicts the waveforms of $f_{\rm VCO}, V_{\rm tune}$, and $I_{\rm CP}$ during the calibration process. Fig. 5(b) illustrates how $f_{\rm VCO}$ changes in the VCO tuning curve plane during the calibration process. The calibration process begins with the VCO frequency calibration mode. In this mode, $V_{\rm tune}$ is fixed at $V_{\rm DD}/2$, and the 7-step binary search process is carried out. The final code selection using the minimum error code finder produces the final VCO capbank code at $t_{\rm VFC}$ [Fig. 5(a)]. Next in the loop bandwidth calibration mode, $V_{\rm tune}$ is sequentially switched from 0.4 V ($V_{\rm tL}$) to 0.8 V ($V_{\rm tH}$) to find $f_{\rm VL}$ and $f_{\rm VH}$, and finally $K_{\rm VCO}$ value is computed. Based on this value, the optimal charge pump current $I_{\rm cpopt}$ is found to set the loop bandwidth to a desired value. The time duration for this calibration is $t_{\rm LBC}$ in Fig. 5(a). After this two-step open-loop calibration is completed, the PLL loop is closed and a normal locking process starts. Finally, PLL is locked to the target frequency at $t_{\rm lock}$. Fig. 6 is the flowchart describing the total calibration process. The total calibration time including all the control timings and settling margins is $\{(\mathrm{C}\cdot(k_{\rm VFC}+2)+3)+2\cdot k_{\rm LBC}+4\cdot k_{\rm Vtune}\}\cdot T_{\rm REF}$, where C is the number of cap-bank bits, and $k_{\rm VFC}, k_{\rm LBC}$, and $k_{\rm Vtune}$ are the number of $T_{\rm REF}$ periods spent for the VCO frequency calibration, the loop bandwidth calibration, and the $V_{\rm tune}$ settling for $V_{\rm tune}$ controller, respectively. For instance, with $T_{\rm REF}=25$ ns, C $=7$, $k_{\rm VFC}=4$, $k_{\rm LBC}=16$, $k_{\rm Vtune}=4$, the total calibration time will be 2.325 μs.

The proposed calibration circuit successfully covers the process variation. The calibration accuracy is not affected by the process variation because the calibration process is purely a digital process. On the other hand, if voltage and temperature (VT) changes significantly after the calibration is completed, it can affect the calibration result and thereby PLL performance. According to the simulations, $K_{\rm VCO}$ and $f_{\rm VCO}$ of the designed VCO are found to vary by 5.6% and 0.45% over the temperature variation from -40 to $+120^{\circ}$C and by 32.5% and 5.3% over the voltage variation from 1.0 to 1.4 V, respectively. The $K_{\rm VCO}$ change can cause the loop bandwidth change, and the $f_{\rm VCO}$ change can cause the phase noise degradation or even unlocking of PLL. However, note that not only the proposed technique but

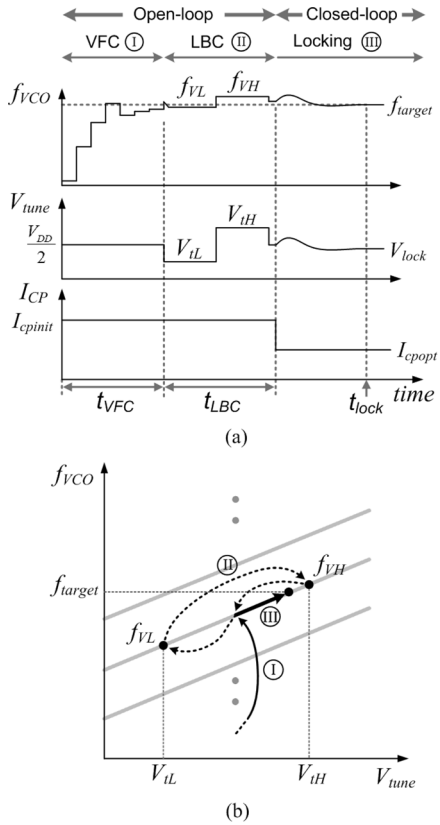


Fig. 5. (a) $f_{\rm VCO}, V_{\rm tune}$, and $I_{\rm CP}$ during calibration and locking process. (b) Transition of $f_{\rm VCO}$ in the tuning curve plane during the calibration process.

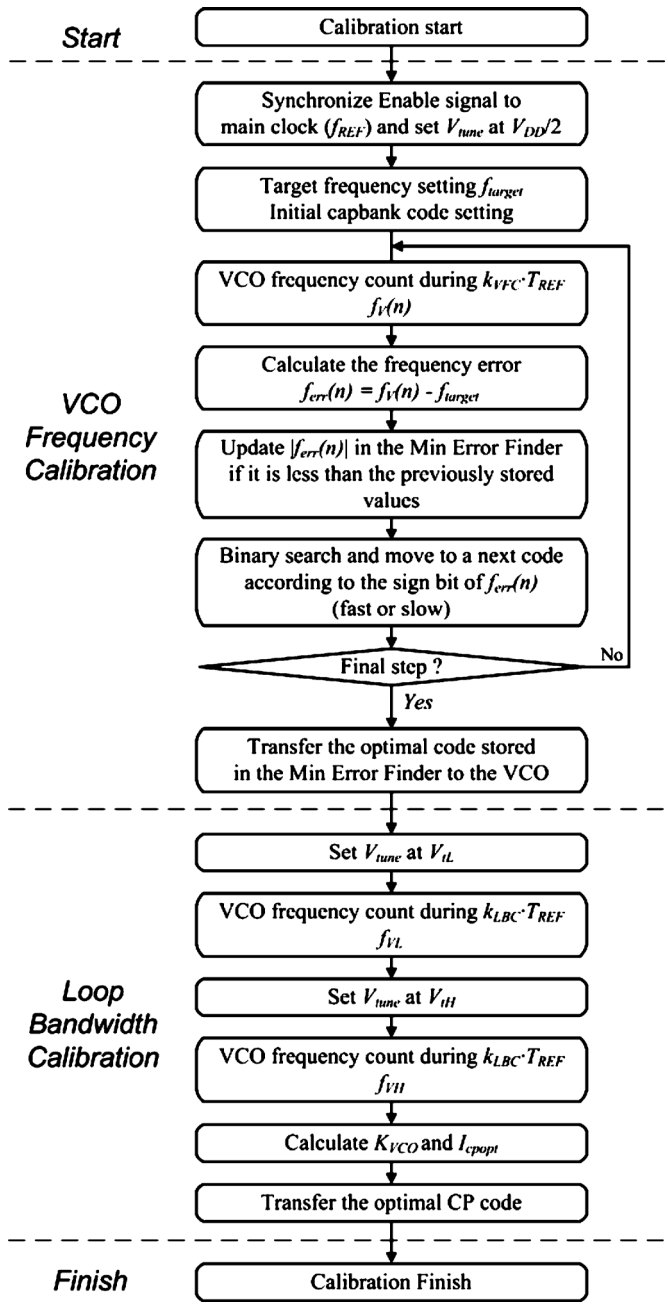


Fig. 6. Flowchart of the calibration process.

also all the previous calibration techniques [8]–[19] possess the same potential problem. To solve this problem, a background monitoring circuit of the VT variation can be employed. Once the voltage and temperature are found to change significantly after the calibration is finished and the PLL is in the normal operation state, the PLL can be put to a re-calibration stage. Meanwhile, the $f_{\rm VCO}$ change problem due to the VT variation can be overcome by employing such previous methods as the background $V_{\rm tune}$ monitoring technique [21] and the analog dual tuning scheme [10], [22].

B. VCO and Charge Pump

Fig. 7 shows the circuit schematic of the octave bandwidth LC VCO covering 1.9 to 3.8 GHz. It is a fully differential cross-coupled negative-$g_{\rm m}$ type. An on-chip low-pass filter composed of R_1 and C_1 is employed to suppress the $1/f$ and thermal noise coupling. The bypass capacitor C_2 is placed at the common source node of $\rm M_3$ and $\rm M_4$ to reject the unwanted noise coupling from $2 \cdot f_{\rm VCO}$ [23]. The inductor L_1 compensates the reduced parallel resistance of the tank at the low-end frequency region, thus keeps the oscillation stable for the entire tuning range [23], [24]. For the LC tank, $L_{\rm tank}$ is set to 1.2 nH, and the 7-bit binary-weighted cap-bank is realized by using metal-insulator-metal (MIM) unit capacitors of 70 fF. The varactor averaging technique with three off-biased varactors minimizes the $K_{\rm VCO}$ variation on a single sub-band tuning curve [25]. It minimizes the unwanted accuracy degradation of the loop bandwidth calibration against the possible $K_{\rm VCO}$ variation within $V_{\rm tL}$ and $V_{\rm tH}$.

Fig. 8 shows the programmable charge pump circuit schematic. The charge pump is designed in 7-bit binary-weighted current switching structure. It produces the output current from 7.8 μA to 1 mA in 128 discrete steps. The linearity of the charge pump current over the 128-step variation will affect the accuracy of the loop bandwidth calibration. Thus, the size of the current switching FETs $\rm M_{16}$–$\rm M_{29}$ are carefully designed and laid out to minimize mismatches. Measurement results show that the output current deviation from a perfect linear relation is maintained within $\pm 0.2\%$. To improve the up/down current matching in the output voltage range between $V_{\rm tL}$ and $V_{\rm tH}$, the operational amplifier based feedback structure

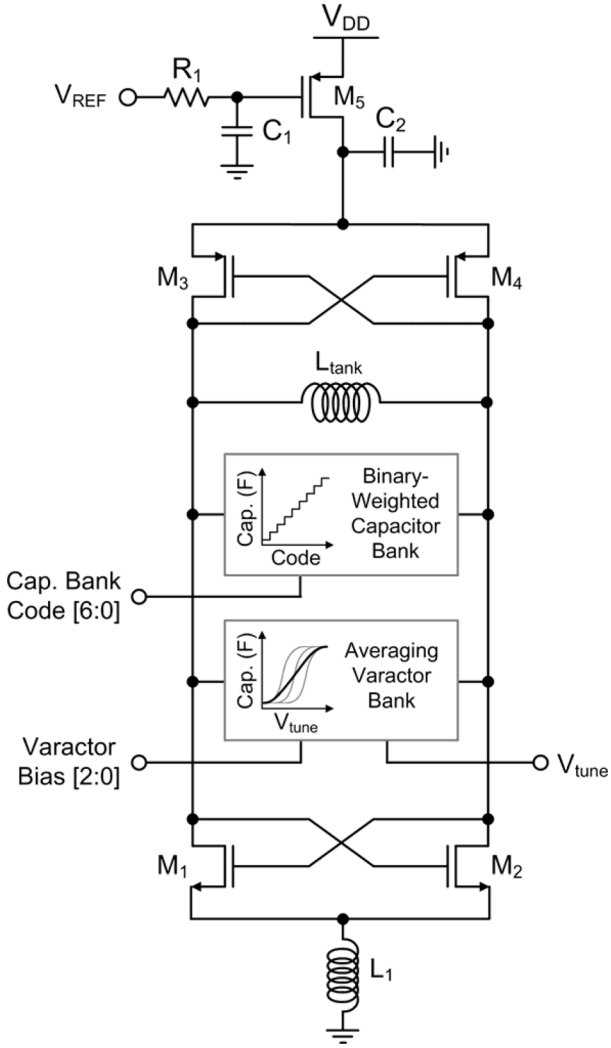


Fig. 7. VCO.

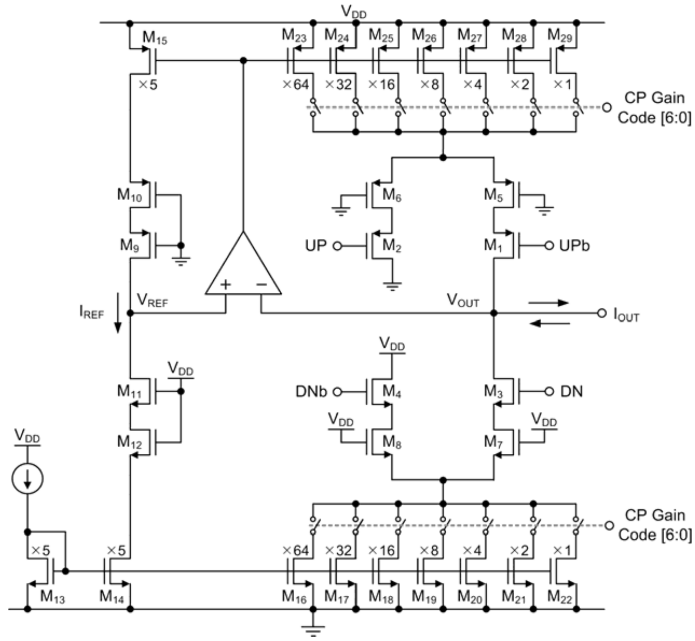


Fig. 8. Charge pump.

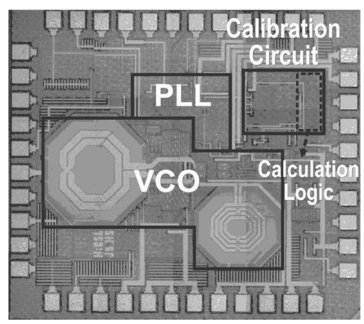


Fig. 9. Chip micrograph.

is used [26]. This structure effectively minimizes the current mismatch between the up/down currents and thus reduces the spur level. The dummy FETs $\mathrm{M_5}-\mathrm{M_8}$ added between the UP/DN switches and the current switching FETs effectively suppress the output current peaking caused by possible timing mismatches between the UP/DN pulses.

IV. Implementation Results

The $\Delta\Sigma$ fractional-N synthesizer with the proposed auto-calibration circuit is fabricated in 0.13 μm CMOS process. Fig. 9 shows the chip micrograph. The die size is 1250×1450 $\mu\mathrm{m}^2$ including the pad frame. The active area of PLL is 0.651 mm^2, of which the calibration circuit occupies 0.0875 mm^2 ($= 350 \times 250$ $\mu\mathrm{m}^2$). The chip is mounted on a printed circuit board and tested. The total current consumption is 12.8 mA from a single 1.2 V supply. The calibration circuit consumes 3.63 mA during the calibration process, of which 3.56 mA is consumed by the high-speed FDC. After the calibration is completed, the calibration circuit is powered down. Thus, the PLL's total current consumption of 12.8 mA does not include the current consumption of the calibration circuit.

Fig. 10(a) shows the measured tuning characteristics. The tuning range covers 1.9–3.8 GHz. The inset shows that the sub-band tuning curves are well separated and not overlapping in any region. Based on Fig. 10(a), K_{VCO} is computed and plotted in Fig. 10(b). As can be seen, K_{VCO} is almost constant within the V_{tune} range of 0.2 to 1 V in a single tuning curve, which is due to the averaging varactor structure. However, K_{VCO} across the entire sub-band tuning curves varies from 22.5 to 168 MHz/V, which is almost 8 times. The sub-band spacing f_{step} at the low and high ends are also found to vary about 8 times from 5 MHz and 44 MHz. The almost 8 times variation of K_{VCO} and f_{step} agrees well with the theoretical expectation given by [2].

The phase noise of the VCO and PLL spectrum are characterized across the total tuning range. Agilent power spectrum analyzer E4440A was used for the phase noise and spectrum measurement. Fig. 11(a) is the phase noise when the VCO output frequency is tuned to the high-end 3923 MHz. It shows -90.5 and -116.4 dBc/Hz at 100 kHz and 1 MHz offset, respectively. At lower frequency region, the phase noise is found to improve further. For instance, at the VCO output frequency of 1900 MHz, the phase noise is -102 and -124.8 dBc at 100 kHz and 1 MHz

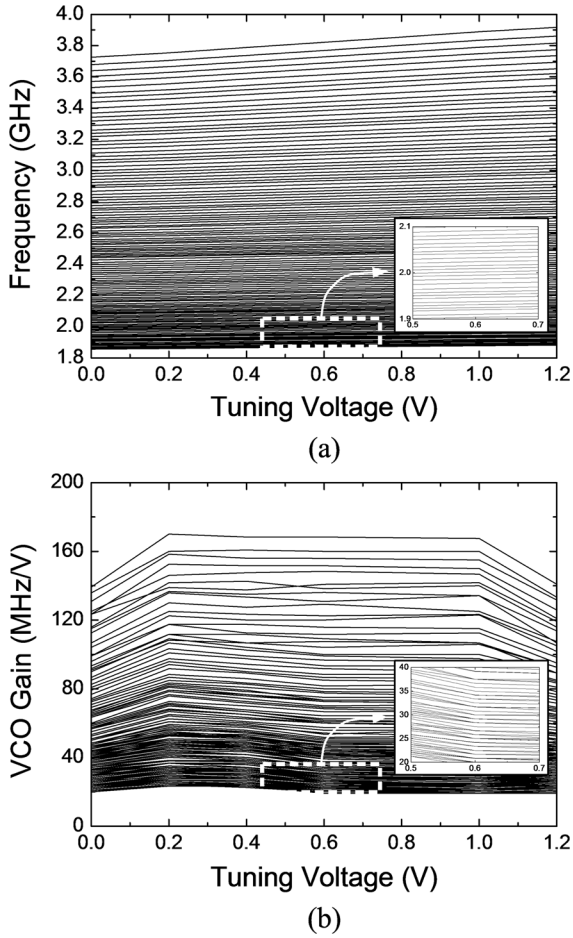


Fig. 10. VCO tuning characteristics. (a) Output frequency. (b) VCO gain (K_{VCO}).

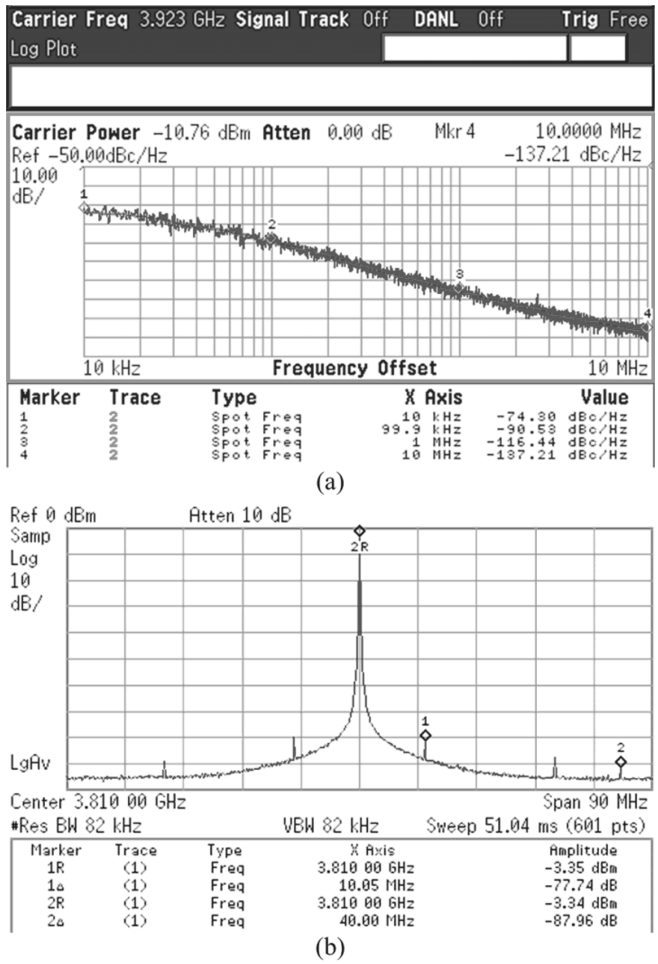
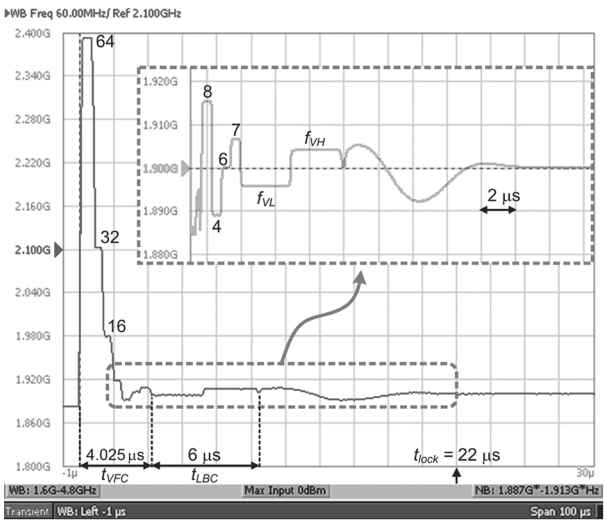


Fig. 11. (a) VCO phase noise at 3.92 GHz. (b) PLL spectrum at 3.81 GHz.

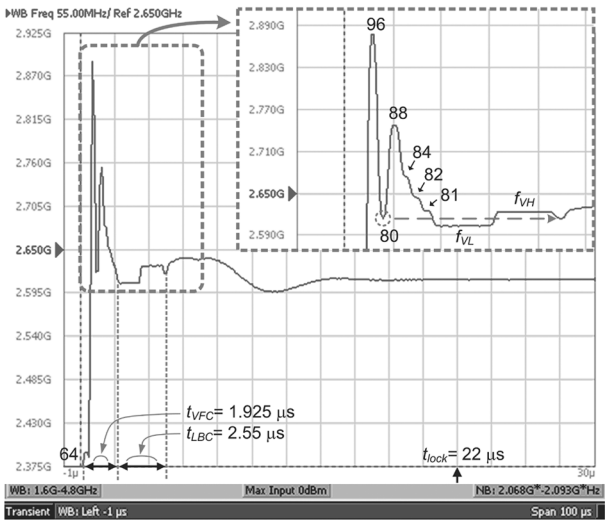
offsets, respectively. The VCO's figure of merit, called power-frequency tuning normalized (PFTN), which was introduced in [27], is used for performance comparison with the previous wideband VCOs having over 50% tuning range in [2], [28], and [29]. The PFTN of this VCO is 3.4 dBc/Hz at 3923 MHz, which is found to be better than the VCOs in [2], [28], and [29] that showed 2.3, −1.8, and 3.2 dBc/Hz, respectively. Fig. 11(b) shows the PLL output spectrum at 3810 MHz. The reference and fractional spurs are −87.9 and −77.7 dBc, respectively. Note that the reference spur appears exactly at the reference frequency of 40 MHz.

Successful operation of the automatic calibration of the VCO frequency and loop bandwidth over the entire tuning range is verified through measurements. Since f_{step} varies from 5 to 44 MHz across the VCO tuning range, k_{VFC} is set from 20 to 4 so that the calibration resolution can always reside in no larger than $f_{\mathrm{step}}/2$. At the high-end region of the tuning range where f_{step} is 44 MHz, k_{VFC} is set to 4, which sets the calibration resolution to $f_{\mathrm{REF}}/4$ (=10 MHz), which is smaller than $f_{\mathrm{step}}/2$ (=22 MHz). At the low-end region of the tuning range where f_{step} is 5 MHz, k_{VFC} is set to 20, which sets the calibration resolution to $f_{\mathrm{REF}}/20$ (=2 MHz), which is smaller than $f_{\mathrm{step}}/2$ (=2.5 MHz). In the mid-region of the tuning range, k_{VFC} is set in between 4 and 20. Meanwhile, the accuracy of loop bandwidth calibration is also dependent on the FDC frequency resolution. In order to maintain the accuracy in ±2%, k_{LBC} is properly set between 114 and 16 to cope with the almost eight times variation of K_{VCO}. Fig. 12 shows the time-domain measurement results showing the calibration process. They are measured by using an Agilent signal source analyzer E5052A. Fig. 12(a)–(c) show three calibration procedures at the low ($f_{\mathrm{target}} = 1900$ MHz), mid ($f_{\mathrm{target}} = 2611.95$ MHz), and high ($f_{\mathrm{target}} = 3767$ MHz) ends of the tuning range, respectively. For each measurement, k_{VFC} and k_{LBC} are set to 20 and 114, 8 and 45, and 4 and 16, respectively. As a result, the calibration times for the VCO frequency and the loop bandwidth for Fig. 12(a)–(c) are 4.025 and 6 μs, 1.925 and 2.55 μs, and 1.225 and 1.1 μs, respectively.

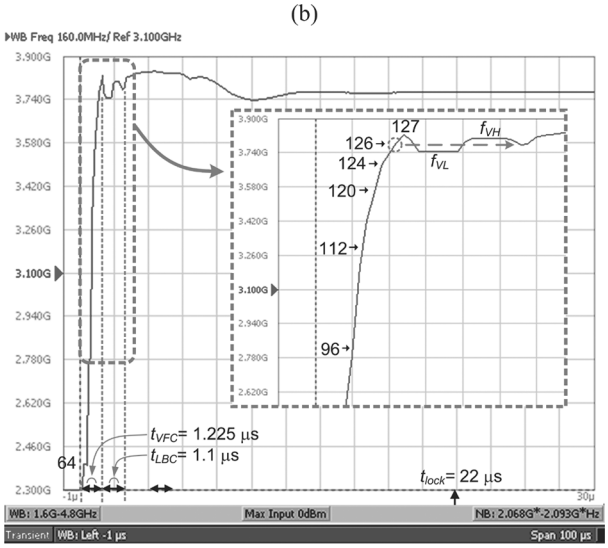
As can be seen, during the VCO frequency calibration, the VCO frequency changes in seven steps following the binary search algorithm. It is observed that the final code selection process is functional and provide the truly closest code to the target frequency at the final step of the VCO frequency calibration. Fig. 12(a) and (c) shows that the final code is the second to the last code, and Fig. 12(b) shows that the final code is the fifth one before the last code. The results clearly demonstrate that the proposed final code selection process based on the minimum error code finder is successfully functional and effective to enhance the VCO frequency calibration accuracy.



(a)



(b)



(c)

Fig. 12. Time-domain measurements of the PLL locking process including the VCO frequency and loop bandwidth calibrations. (a) 1900 MHz. (b) 2611.95 MHz. (c) 3767 MHz.

After the VCO frequency calibration is completed, the loop bandwidth calibration is carried out, which is confirmed by observing that the VCO frequency changes sequentially from f_{VL} to f_{VH}. After the loop bandwidth calibration is completed, the normal closed-loop locking process begins.

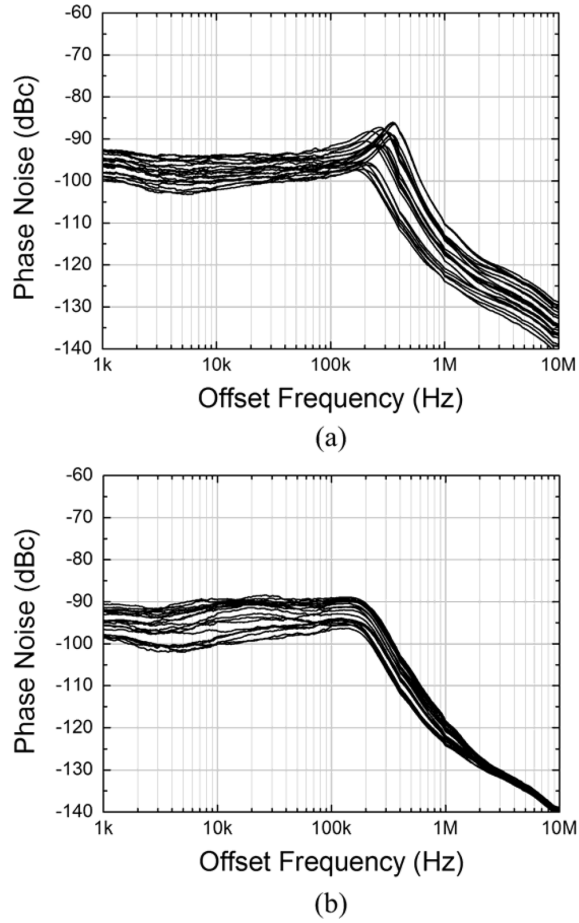


Fig. 13. PLL closed-loop transfer characteristics before and after the loop bandwidth calibration over the entire band between 1.9 and 3.8 GHz. The phase noise is measured after a divide-by-2 circuit. (a) Before the calibration. (b) After the calibration.

The effects of the loop bandwidth calibration are examined in the closed-loop transfer characteristics. Fig. 13 shows the PLL output spectrum before and after the loop bandwidth calibration. As can be seen, the originally widely spread frequency response curves remarkably converges after the calibration. Note that the measurement is done via a divide-by-2 after the VCO. The loop bandwidth and the phase noise before and after the calibration are also compared in Fig. 14. Fig. 14(a) shows that the original loop bandwidth is widely scattered from 211 to 572 kHz. But after the loop bandwidth calibration, it becomes almost constant 224 kHz with only $\pm 2\%$ variation. Fig. 14(b) compares the phase noises at offset frequencies of 1, 5, and 10 MHz before and after the calibration. As can be seen, the phase noise and its variation over the tuning range are improved significantly. For instance, at 10 MHz offset, the phase noise is improved by 8.6-dB at 1900 MHz output frequency and the total 11.3 dB variation before the calibration is reduced to only 2.7 dB after the calibration.

As can be observed in Fig. 13, the in-band phase noise is degraded after the loop bandwidth calibration. For instance, it is increased by as much as 4.3 dB at 10 kHz offset. The increase

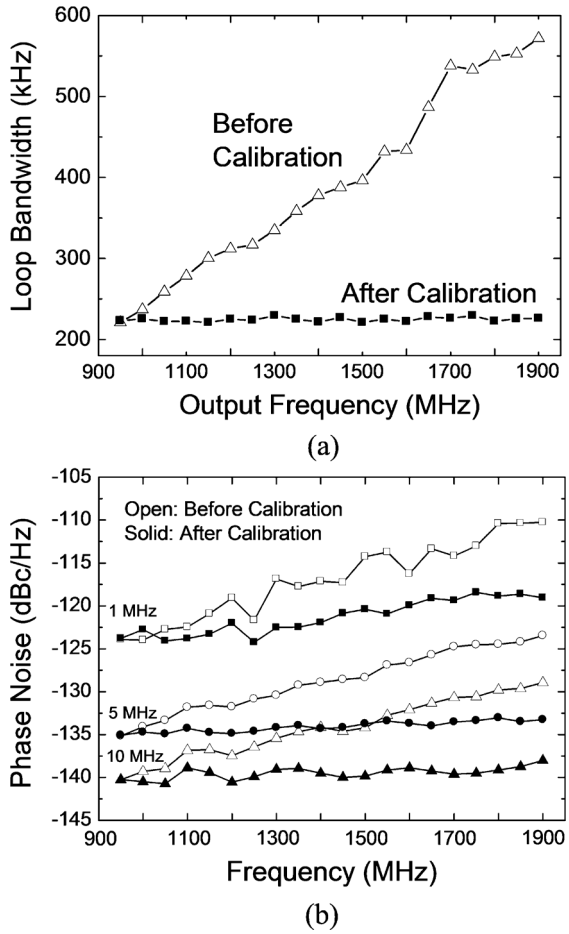


Fig. 14. Loop bandwidth calibration effects before and after the calibration. (a) Loop bandwidth. (b) Phase noise.

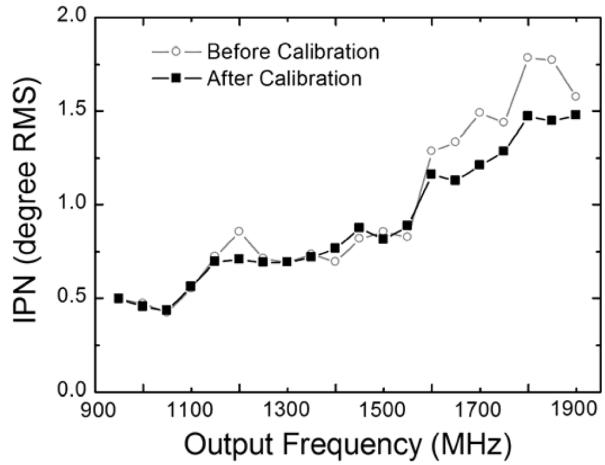


Fig. 15. Integrated phase noise (IPN) over the entire tuning range before and after the loop bandwidth calibration.

TABLE I
PLL PERFORMANCE SUMMARY

Technology	0.13 μm CMOS
PLL frequency range	1900 – 3800 MHz
Spot phase noise (after divide-by-2)	< -89.66 dBc/Hz @ 10 kHz offset < -89.2 dBc/Hz @ 100 kHz offset < -117.57 dBc/Hz @ 1 MHz offset
Integrated phase noise (1 kHz ~ 10 MHz)	0.495 rms degree (@950 MHz) 1.477 rms degree (@1900 MHz)
Reference spur	-87 dBc
Fractional spur	-77 dBc
Calibration time	< 10.025 μsec for loop bandwidth and VCO calibrations
Lock time	< 22 μsec including calibration time
Supply voltage	1.2 V
Current consumption	12.8 mA

of the in-band phase noise is mainly due to the reduction of the charge pump current during the loop bandwidth calibration. It is known that the PLL output phase noise is inversely proportional to the square of charge pump current gain [30]. Even with the elevated in-band phase noise, it is observed that the integrated phase noise is not affected much. The integrated phase noise over the tuning range is shown in Fig. 15. At the high-end frequency region, it is interesting to note that the integrated phase noise is even improved by 0.1 to 0.3 degree after the calibration. This improvement is due to the disappearance of the phase noise peaking around the corner frequency after the calibration, which is also observable in Fig. 13.

The measured PLL performance is summarized in Table I. The total calibration time for VCO frequency and loop bandwidth is less than 10.025 μs over the entire frequency band of 1.9–3.8 GHz. The total PLL lock time including the total calibration time is less than 22 μs.

Table II compares the proposed calibration technique with the previously reported methods. The comparisons are summarized separately for the loop bandwidth and VCO frequency calibrations. First, the proposed loop bandwidth calibration technique provides the fastest ($<6\,\mu$s) calibration time due to the open-loop operation, whereas the closed-loop calibration methods in [8], [9] require much longer time. Nevertheless, its accuracy is as good ($\pm 2\%$) as the closed-loop calibration method of [8] due to the on-chip $K_{\rm VCO}$ detection capability. Without the on-chip $K_{\rm VCO}$ detection capability, the calibration accuracy would be much worse as in [10] and [11]. Also, note that this PLL has the largest tuning range, which leads to much severe variation of $K_{\rm VCO}$. Even with the much wider tuning range, this method demonstrates better or comparable accuracy with the previous methods, which is also due to the on-chip $K_{\rm VCO}$ detection capability.

The proposed VCO frequency calibration technique is based on the absolute frequency error detection method, whereas the previous techniques are based on either the relative frequency or period comparison. The single-bit calibration time for obtaining a resolution of $f_{\rm REF}/k$ is only $k \cdot T_{\rm REF}$, which is much faster than the relative frequency comparison techniques of [15], [16]. This aspect can be also interpreted as this technique provides the better calibration accuracy in a given calibration time period. The final code selection algorithm in the proposed technique enhances the calibration accuracy significantly. Another advantage of the proposed technique is that the $\Delta\Sigma$ modulator does not need to be activated for achieving sub-$f_{\rm REF}$ accuracy during the calibration, while the conventional techniques

TABLE II
COMPARISON OF PLL AUTO-CALIBRATION TECHNIQUES

Loop Bandwidth Calibration						VCO Frequency Calibration						
	This Work	[8]	[9]	[10]	[11]		This Work	[15]	[16]	[17]	[18]	[19]
On-chip loop parameter detection method	K_{VCO} measurement	PLL step response measurement	PLL step response measurement	None	None	VCO frequency calibration scheme	Frequency error measurement in digital	Relative frequency comparison	Relative frequency comparison	Analog comparison of period	Analog comparison of period	Digital comparison of period
Determining factor for charge pump current	K_{VCO}/N §	Step response	Step response	V_{tune}	N	Single-bit calibration time for resolution f_{REF}/k	$k{\cdot}T_{REF}$	$N/4{\cdot}(k{\cdot}T_{REF})$†	$N/8{\cdot}(k{\cdot}T_{REF})$	$4{\cdot}(k{\cdot}T_{REF})$	$4{\cdot}(k{\cdot}T_{REF})$	N.A.
Loop state during calibration	Open	Closed	Closed	Closed	Closed	Final code selection algorithm	True closest code selection after binary search	Simple binary search	Simple binary search	Simple linear search	Closer code selection between the last two searched codes	Linear search
Calibration accuracy	± 2%	± 2%	± 10 %	± 4%	± 9%	ΔΣ modulator during calibration‡	Off-state	Must be enabled	Must be enabled	Must be enabled	Must be enabled	N.A
Calibration time	1.1 – 6 μs	25 μs	66 μs	N.A.ǂ	N.A.ǂ	Calibration time	1.225 – 4.025 μs	12.6 μs	50 μs	4 μs	0.35 μs	13.5 μs
PLL frequency range (GHz)	1.9 – 3.8 (67 %)	0.88 – 0.92 (4 %)	2.40 – 2.48 (3 %)	3.1 – 3.9 (23 %)	4.0 – 4.8 (18 %)	VCO frequency range (GHz)	1.9 – 3.8 (67%)	1.15 – 1.75 (41%)	1.5 – 2.48 2.2 – 3.78 (49 and 53%)	8.67 – 10.12 (15%)	2.5 – 4.0 (46%)	1.8 – 3.1 (53%)
PLL Active Area (mm^2)	0.651*	N.A.	N.A.	1.5	1.012	PLL Active Area (mm^2)	0.651*	4.56*	1.9	1.35	0.63	0.3
Technology	0.13 μm CMOS	0.25 μm BiCMOS	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	Technology	0.13 μm CMOS	0.5 μm CMOS	0.11 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	65 nm CMOS

§ N is PLL total division ratio.
ǂ Not applicable because it does not perform calibration, but only compensation.
* Loop filter is not included.
† k is the number of reference clock period used for frequency counting.
‡ If ΔΣ modulator is enabled, calibration will take longer.

in [15]–[18] must activate the ΔΣ modulator during the calibration when the sub-f_{REF} accuracy is needed in ΔΣ fractional-N PLL's. Thus, the proposed VCO frequency calibration technique is much faster and more accurate, thus highly suited for ΔΣ fractional-N synthesizers.

V. CONCLUSION

The FDC-based all-digital auto-calibration technique for constant loop bandwidth and fast VCO frequency calibration is presented for the 1.9–3.8 GHz ΔΣ fractional-N synthesizer. Over the octave tuning range, the loop bandwidth calibration maintains the closed-loop bandwidth within ±2% through accurate on-chip K_{VCO} detection. The VCO frequency calibration successfully finds the truly closest code to the target frequency through the minimum error finding capability. Since the calibration is carried out in open-loop, the calibration times for the loop bandwidth and VCO frequency are greatly minimized, and the experimental results are 1.1–6.0 μs and 1.225–4.025 μs, respectively, over the 1.9–3.8 GHz octave tuning range. Also, this technique is highly suited for ΔΣ fractional-N synthesizers since it does not need to activate ΔΣ modulator for sub-f_{REF} resolution. With the proposed auto-calibration technique, the PLL's closed-loop performances such as lock time, loop bandwidth, and phase noise are well maintained over the octave tuning range.

REFERENCES

[1] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1998, pp. 555–558.
[2] J. Kim, J. Shin, S. Kim, and H. Shin, "A wide-band CMOS LC VCO with linearized coarse tuning characteristics," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 5, pp. 399–403, May 2008.
[3] D. R. McMahill and C. G. Sodini, "A 2.5-Mb/s GFSK 5.0-Mb/s 4-FSK automatically calibrated $\Sigma-\Delta$ frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 18–26, Jan. 2002.
[4] B. Huff and D. Draskovic, "A fully-integrated bluetooth synthesizer using digital pre-distortion for PLL-based GFSK modulation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, June 2003, pp. 173–174.
[5] E. Gotz, H. Krobel, G. Mazinger, B. Memmler, C. Miinker, B. Neurauter, D. Romer, J. Rubach, W. Schelmbauer, M. Scholz, M. Simon, U. Steinacker, and C. Stoger, "A quad-band low power single chip direct conversion CMOS transceiver with ΣΔ-modulation loop for GSM," in *Proc. European Solid-State Dev. Research Conf.*, Sept. 2003, pp. 217–220.
[6] S. T. Lee, S. J. Fang, D. J. Allstot, A. Bellaouar, A. Fridi, and P. Fontaine, "A 1.5 V 28 mA fully-integrated fast-locking quadband GSM-GPRS transmitter with digital auto-calibration in 130 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2004, p. 188, 521.
[7] C. H. Lee, H. Lee, and P. Good, "A fully integrated GMSK modulator using BiCMOS $\Sigma-\Delta$ frequency synthesizer with automatic loop gain calibration," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, June 2005, pp. 219–222.
[8] Y. Akamine, M. Kawabe, K. Hori, T. Okazaki, M. Kasahara, and S. Tanaka, "ΔΣ PLL transmitter with a loop-bandwidth calibration system," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 497–506, Feb. 2008.
[9] H. Shanan, G. Retz, K. Mulvaney, and P. Quinlan, "A 2.4 GHz 2 Mb/s versatile PLL-based transmitter using digital pre-emphasis and auto calibration in 0.18 μm CMOS for WPAN," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2009, pp. 420–421.
[10] T. Wu, P. K. Hanumolu, K. Mayaram, and U. K. Moon, "Method for constant loop bandwidth in LC-VCO PLL frequency synthesizers," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 427–434, Feb. 2009.
[11] A. Rao, M. Mansour, G. Singh, C. H. Lim, R. Ahmed, and D. R. Johnson, "A 4–6.4 GHz LC PLL with adaptive bandwidth control for a forwarded clock link," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2099–2108, Sept. 2008.
[12] T. H. Lin and W. J. Kaiser, "A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 424–431, Mar. 2001.

[13] A. Aktas and M. Ismail, "CMOS PLL calibration techniques," *IEEE Circuits and Dev. Mag.*, vol. 20, no. 5, pp. 6–11, Sept./Oct. 2004.
[14] W. B. Wilson, U. K. Moon, K. R. Lakshmikumar, and L. Dai, "A CMOS self-calibrating frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1437–1444, Oct. 2000.
[15] H. I. Lee, J. K. Cho, K. S. Lee, I. C. Hwang, T. W. Ahn, K. S. Nah, and B. H. Park, "A ΣΔ fractional-N frequency synthesizer using a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1164–1169, July 2004.
[16] M. Marutani, H. Anbutsu, M. Kondo, N. Shirai, H. Yamazaki, and Y. Watanabe, "An 18 mW 90 to 770 MHz synthesizer with agile auto-tuning for digital TV tuners," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2006, pp. 192–193.
[17] T. H. Lin and Y. J. Lai, "An agile VCO frequency calibration technique for a 10-GHz CMOS PLL," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 340–349, Feb. 2007.
[18] J. Lee, K. Kim, J. Lee, T. Jang, and S. Cho, "A 480-MHz to 1-GHz sub-picosecond clock generator with a fast and accurate automatic frequency calibration in 0.13-μm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 67–70.
[19] M. Kondou, A. Matsuda, H. Yamazaki, and O. Kobayashi, "A 0.3 mm^2 90-to-770 MHz fractional-N synthesizer for a digital TV tuner," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2010, pp. 248–249.
[20] J. Shin and H. Shin, "A fast and high-precision VCO frequency calibration technique for wideband ΔΣ fractional-N frequency synthesizers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1573–1582, July 2010.
[21] H.-R. Lee, M.-S. Hwang, B.-J. Lee, Y.-D. Kim, D. Oh, J. Kim, S.-H. Lee, D.-K. Jeong, and W. Kim, "A 1.2-V-only 900-mW 10 GB ethernet transceiver and XAUI interface with robust VCO tuning technique," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2148–2158, Nov. 2005.
[22] W. Rhee, H. Ainspan, D. Friedman, T. Rasmus, S. Garvin, and C. Cranford, "A uniform bandwidth PLL using a continuously tunable single-input dual-path LC VCO for 5 Gb/s PCI express Gen2 application," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 63–66.
[23] E. Hegazi, H. Sjöland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
[24] Y. Wu and V. Aparin, "A monolithic low phase noise 1.7 GHz CMOS VCO for Zero-IF cellular CDMA receivers," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2004, pp. 396–535.
[25] J. Mira, T. Divel, S. Ramet, J.-B. Begueret, and Y. Deval, "Distributed MOS varactor biasing for VCO gain equalization in 0.13 μm CMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2004, pp. 131–134.
[26] J. Lee, M. S. Keel, S. I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *Electron. Lett.*, vol. 36, no. 23, pp. 1907–1908, Nov. 2000.
[27] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, June 2001.
[28] M. Demirkan, S. P. Bruss, and R. R. Spencer, "Design of wide tuning-range CMOS VCOs using switched coupled-inductors," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1156–1163, May 2001.
[29] D. Hauspie, E.-C. Park, and J. Craninckx, "Wide-band VCO with simultaneous switching of frequency band, active core, and varactor size," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1472–1480, July 2007.
[30] F. M. Gardner, *Phaselock Techniques Third Edition*. New York: John Wiley & Sons Inc., 2005.

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