An Area-Efficient 10-Bit Source-Driver IC With LSB-Stacked LV-to-HV-Amplify DAC for Mobile OLED Displays

Gyu-Wan Lim, Gyeong-Gu Kang, Hyunggun Ma, Moonjae Jeong, and Hyun-Sik Kim, *Senior Member, IEEE*

***Abstract*— This article presents an ultra-compact 10-bit source driver IC (SD-IC) developed for mobile organic light-emitting diode (OLED) displays. The proposed LSB-stacked low-voltage (LV)-to-high-voltage (HV)-amplify digital-to-analog converter (DAC) allows the area-consuming 8-bit voltage selector to be implemented with compact LV transistors (LV-MOS) as well as obtains an additional DAC resolution of 2-bit by dissipating little die area. By virtue of the LV-MOS voltage selector, level-shifters (L/S) can also be eliminated, further lowering the column channel size. In addition to its compactness, the proposed SD-IC merits a high uniformity attained from a mismatch-insensitive switched-capacitor (SC) 4×-multiplier and a globally sampled 2-bit stack-up voltage. A technique to elaborately cancel the offset of the buffer amplifier is also included in this work. The prototype 600-channel SD-IC was fabricated in a 130-nm 1.5/5-V CMOS technology. The maximum differential nonlinearity (DNL) and integral nonlinearity (INL) were measured to be −0.39 and 0.9 LSB, respectively, with a 1-LSB voltage of 4.1 mV. An achieved deviation of voltage outputs (DVOs) was 4.82 mV, which is low enough to be comparable to the 1-LSB voltage. The proposed 10-bit channel size of 2688 μm^2 is a 65.2% reduction in comparison to conventional 8-bit SD-IC.**

***Index Terms*— Chip area efficiency, deviation of voltage outputs (DVOs), digital-to-analog converter (DAC), gain loss, offset cancellation, organic light-emitting diode (OLED) display, resolution, source (column) driver, switched-capacitor (SC), voltage selector.**

I. Introduction

SOURCE driver IC (SD-IC), which is formed of multiple column channels, plays a crucial role in converting digital display data into an analog signal and driving it into the pixel, thereby considerably affecting image quality in the organic light-emitting diode (OLED) displays. As the spatial resolution of OLED displays continues to rise even in mobile devices, more than a 1000 column channels are mandated to be integrated into an SD-IC. Moreover, the data resolution of the digital-to-analog converter (DAC) that occupies the majority die area of the column channel must be increased to improve display color-depth. As a result, enhancing area efficiency is becoming increasingly critical in the design of cutting-edge SD-ICs to boost DAC resolution as well as integrate more column channels on a chip.

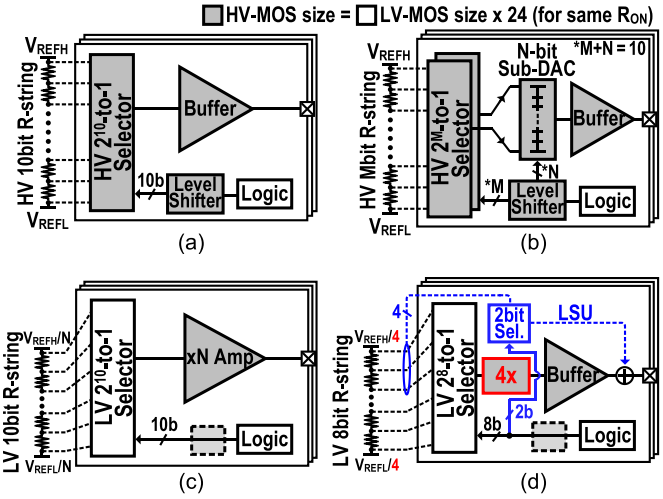

Fig. 1. SD-IC architectural comparison: (a) typical R-string DAC [1], [2]; (b) voltage-interpolative DAC using in-channel sub-DAC [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41]; (c) voltage-amplifying DAC [42]; and (d) proposed LSB-stacked LV-to-HV-amplify DAC.

Fig. 1(a) depicts a typical 10-bit SD-IC architecture consisting of R-DAC-based column channels that share a global resistor-string (R-string) [1], [2]. Its major drawback is that the size of the switch-arrayed voltage selector in the R-DAC increases proportionally to a power of two with DAC resolution [3], [4]. Moreover, given that the full-scale range (FSR $=V_{REFH} - V_{REFL}$) of the R-DAC is directly correlated with the dynamic range in an OLED display, not only the voltage selector but also accompanying level-shifters (L/S) must be constructed with area-consuming high-voltage MOSFETs (HV-MOSs) to cover a wide FSR [5], [6], [7], [8], [9], [10], [11]. Accordingly, even modern CMOS technology nodes are still unable to dramatically shrink the SD-IC size.

Thus far, many efforts to improve the DAC area efficiency have been made [4], [12], [13], [14], [15], [16], [17], [18],

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[19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42]. Among them, the SD-ICs employing voltage-interpolating sub-DAC have become the mainstream, including buffer-embedded interpolation [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], resistor-resistor (RR) sub-DAC [31], [32], [33], [34], [35], [36], [37], and switched-capacitor (SC) sub-DAC [38], [39], [40], [41]. As shown in Fig. 1(b), the column driver channel generates $(M + N)$-bit analog output using an N-bit sub-DAC that interpolates between two voltages selected from the M-bit global reference; this may significantly reduce the channel size, compared to the typical form of Fig. 1(a). However, the use of a two-output HV voltage selector, which takes up twice the area of a one-output one, is mandatory for voltage interpolation. The mismatch between in-channel sub-DACs is also inescapable, significantly impacting the interchannel uniformity, which is one of the key performance metrics in an SD-IC. To resolve the large size of the HV voltage selector, Kim et al. [42] introduced a low-voltage (LV) R-DAC in which the area-consuming voltage selector is built with compact (90-nm 1.2-V) LV-MOSs. As depicted in Fig. 1(c), while the global R-string's FSR is reduced by N times, the subsequent voltage amplifier with a gain of N reconstructs it to the desired level. Despite the LV R-DACs compactness, the interchannel gain mismatch between in-channel voltage amplifiers could degrade the display uniformity. Although a capacitor-rotating solution was also proposed in [42] to mitigate this issue, the resulting low-frequency flicker noise is likely to be visible to human eyes.

In this article, we present an ultra-compact-sized 10-bit SD-IC [43] even without adopting voltage-interpolation. As shown in Fig. 1(d), the two key innovations of this work include: 1) a mismatch-insensitive LV-to-HV-amplify DAC, which enables an 8-bit voltage selector to be realized with only LV-MOSs while obtaining the HV output, and 2) a deviation-free 2-bit LSB stack-up (LSU) technique enabling a finer resolution while consuming little area. Considering a 1.5-V thin-gate LV-MOS is 24× smaller than a 5-V thick-gate HV-MOS for the same turn-on resistance (R_{ON}) in 130-nm CMOS process, this work can achieve dramatic shrinkage of the chip size due to the all-LV-MOS-based R-DAC in conjunction with the elimination of accompanying L/S. In addition, both our innovations are highly robust to process variations and thus contribute to overcoming interchannel mismatch, which is a drawback of prior voltage-interpolative schemes. The content of this article is organized as follows. Section II describes the fundamental principles of the proposed techniques. In Section III, theoretical analysis will be provided to explore design optimization. Section IV shows the measurement results and compares this work against the most recent SD-ICs.

II. Proposed 10-Bit LSB-Stacked LV-to-HV-Amplify DAC

A. DAC Structure and Operational Principle

Fig. 2 shows the column channel architecture of the proposed 10-bit SD-IC, which is mainly composed of four parts: a LV 8-bit voltage selector; a mismatch-insensitive SC 4×-multiplier; a V_{LSU}-stack-up circuit with an LV 2-bit voltage selector; and an output buffer amplifier. An analog voltage corresponding to the upper 8-bit input is generated at V_{4X}, while a lower 2-bit voltage of V_{LSU} is sampled at C_{LSU}. Finally, the sum of V_{4X} and V_{LSU} (V_{LSU} is stacked on V_{4X}) is driven to the final output (V_{out}) via the buffer amplifier. Fig. 3 illustrates the operational timing diagram. The proposed DAC operates in three phases: V_{LSU}-sampling (Phase 1), V_{4X}-drive (Phase 2), and V_{LSU}-stack-up (Phase 3). During these phases, the offset (V_{OS}) of the amplifier is also sampled and canceled. Detailed behavior with the operational phases will be described in Section II-D.

Fig. 4 shows the fundamental principle of the proposed LSB-stacked LV-to-HV-amplify 10-bit DAC with 1-LSB_{HV10b} voltage = $FSR/2^{10}$, where FSR ($=V_{REFH} - V_{REFL}$) is designed to be approximately 5 V (HV domain). The 10-bit input data, $D\langle 9{:}0\rangle$, is divided into two parts: MSB 8-bit (upper $D\langle 9{:}2\rangle$) and LSB 2-bit (lower $D\langle 1{:}0\rangle$). In the first step, the upper bits, $D\langle 9{:}2\rangle$, are input into the 8-bit LV voltage selector. An LV-domain analog output (V_X) is then selected from a 256-segmented LV R-string that is referenced by $V_{REFH}/4$ (top) and $V_{REFL}/4$ (bottom). As a result, the 1-LSB_{LV8b} voltage of the 8-bit LV R-string equals $(1/4)\cdot FSR/2^8$, which is identical to the 1-LSB_{HV10b} voltage in the HV domain. Simultaneously, the analog voltage V_{LSU} ($=V_{REFH}/4 - V_{2b}$) for the lower bits of $D\langle 1{:}0\rangle$ is sampled to the capacitor C_{LSU} (100 fF) through the 2-bit LV voltage selector connected to the same LV R-string. In the second step, the SC-based 4×-multiplier amplifies V_X (in the LV domain) exactly fourfold to achieve the HV-domain MSB 8-bit output V_{4X} ($=4\cdot V_X$). This analog 4×-multiplication is equivalent to a logical up-shift of two bits. In the last step, V_{LSU} (=LSB 2-bit voltage) is stacked on the V_{4X} (=MSB 8-bit voltage), and finally, the HV-domain analog output V_{out} ($=V_{4X} + V_{LSU}$) for 10-bit data of $D\langle 9{:}0\rangle$ is obtained and can be expressed as

$$\begin{aligned} V_{out} &= V_{4X} + V_{LSU} = 4\cdot V_X + \left(\frac{V_{REFH}}{4} - V_{2b}\right) \\ &= 4\cdot\left(\frac{FSR}{4}\sum_{i=2}^{9}\frac{D[i]}{2^{10-i}}\right) + \left(\frac{FSR}{4}\sum_{i=0}^{1}\frac{D[i]}{2^{8-i}}\right) \\ &= FSR\sum_{i=0}^{9}\frac{D[i]}{2^{10-i}}. \end{aligned} \tag{1}$$

The LSU can extend the DAC resolution from 8 to 10-bit using a 2-bit LV voltage selector (realized only with four LV-MOS switches), thereby delivering extreme shrinkage compared to the pure 10-bit voltage selector consuming 4× the size of an 8-bit voltage selector. In addition, since the 10-bit data of $D\langle 9{:}0\rangle$ is input only to the LV circuits, the L/S are unneeded.

To accomplish the required gamma correction in SD-ICs for OLED display systems, there are two options: 1) nonlinear gamma control using a (partially) nonlinear R-string DAC [21], [40], [42], and 2) linear gamma control with a linear DAC and digital look-up tables (LUTs) [12], [13], [44], [45], [46]. Given that the proposed

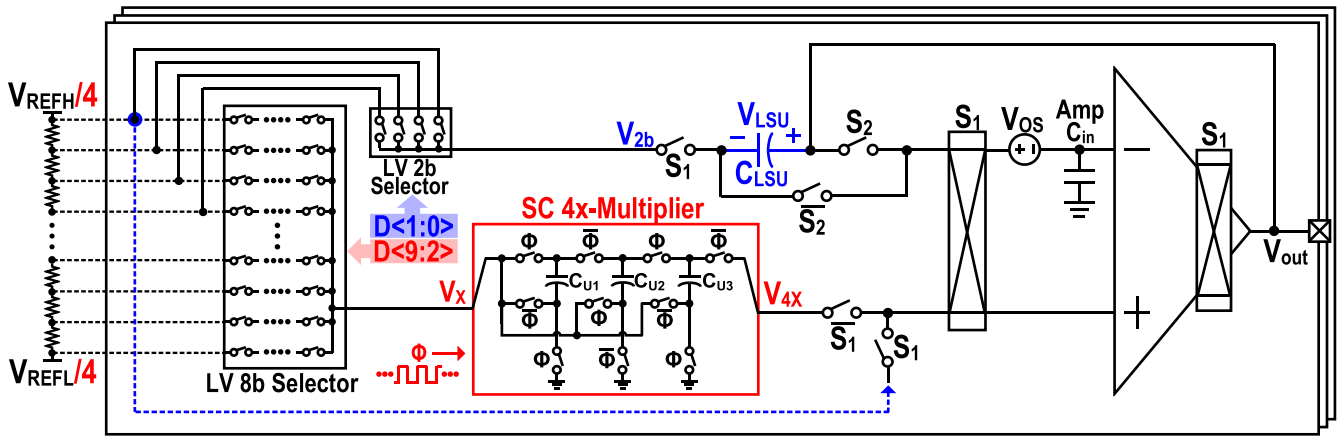


Fig. 2. Detailed design of the proposed 10-bit column driver channel in SD-IC.

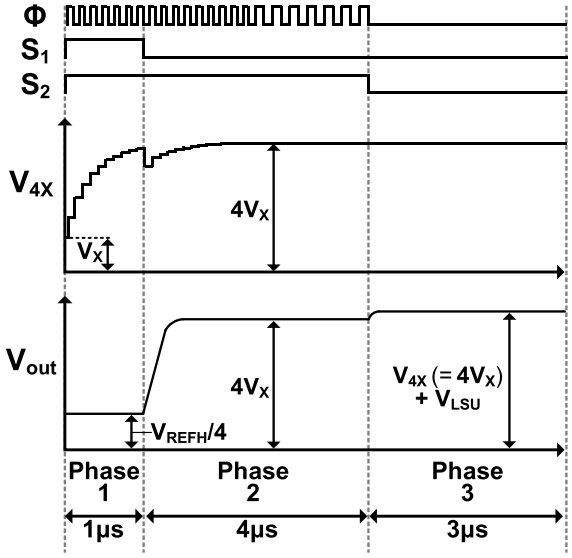


Fig. 3. Operational key waveforms and timing diagram.

LSU technique capable of effectively extending the DAC resolution from 8 to 10-bit applies the notion of "1-LSB_{LV8b} voltage = 1-LSB_{HV10b} voltage" in the fully linear R-string, the gamma correction in this work must be performed with the LUT-based linear gamma control. In comparison to nonlinear gamma control, which assigns different voltage amounts to the nonlinear R-string, the LUT-based linear gamma control method wastes some input bits of the linear DAC, slightly lowering effective color-depth [12], [44]. On the other hand, it can perform independent gamma correction for R, G, and B with individual LUTs, thereby keeping the color temperature constant for wide gray levels [13], [44], [45].

B. Channel Area Reduction

Fig. 5 shows the SD-ICs column channel layout designs for exploring the contributions of the proposed size-reduction strategies. First, the FSR of the global R-string is 4× lowered in this work to design the voltage selector only with compact LV-MOSs rather than area-consuming HV-MOSs. It contributes to taking up 5× less die space than a traditional 10-bit channel, although the SC 4×-multiplier is additionally inserted. Moreover, the elimination of the L/S results in a further 3% area-reduction. Second, the area-efficient 2-bit conversion of the proposed LSU technique enables to decrease in the resolution of the voltage selector from 10 to 8-bit, leading to the 4× shrinkage in the voltage selector. In summary, the proposed 10-bit column driver channel only occupies 10% of the die area of the conventional 10-bit one.

C. Mismatch-Insensitive SC 4×-Multiplier

A straightforward method to amplify (LV domain) V_X to (HV domain) V_{4X} is to use a charge-based voltage amplifier with an op-amp [42], as shown in Fig. 6(a). It can perform a 4×-multiplication if $C_X = 4 \cdot C_Y$. However, the variation of its voltage gain ($=V_{4X}/V_X$) is directly affected by the capacitor mismatch between C_X and C_Y and has a significant effect on the DAC linearity. Furthermore, because it should be individually built-in for each independent column channel, the gain variation can increase the output voltage dispersion in a multichannel SD-IC. Fig. 6(b) shows the proposed mismatch-insensitive SC 4×-multiplier circuit. Contrary to Fig. 6(a), each capacitor in the SC 4×-multiplier of Fig. 6(b) is designed to behave as a floating voltage source independent of the capacitance value, resulting in strong immunity to process variations.

Fig. 7 shows the detailed operation of the proposed 4×-multiplier. When Φ = ON, C_{U1} is charged to V_X, and the voltage across C_{U3} gets closer to $3{\cdot}V_X(=V_X + 2 \cdot V_X)$ by C_{U2} connected in series with the input V_X. During the phase of Φ = OFF, $2{\cdot}V_X$ is applied across C_{U2} due to the series-connected C_{U1}. By repeating "Φ = ON" and "Φ = OFF" multiple times in this way, the final 4×-multiplied output $V_{4X}(= 4{\cdot}V_X)$ is obtained on C_L, which is the input capacitance (C_{in}) of the output buffer. As depicted in Fig. 7, the SC-based 4×-multiplier achieves the final output by piling up the voltage-stacks charged on the capacitors. Consequently, it is highly insensitive to capacitor mismatch, ensuring not only the linearity of the DAC but also high uniformity among multiple-column channels. For performing a fine 4×-multiplication, several clock (Φ) cycles are necessary; the required minimum

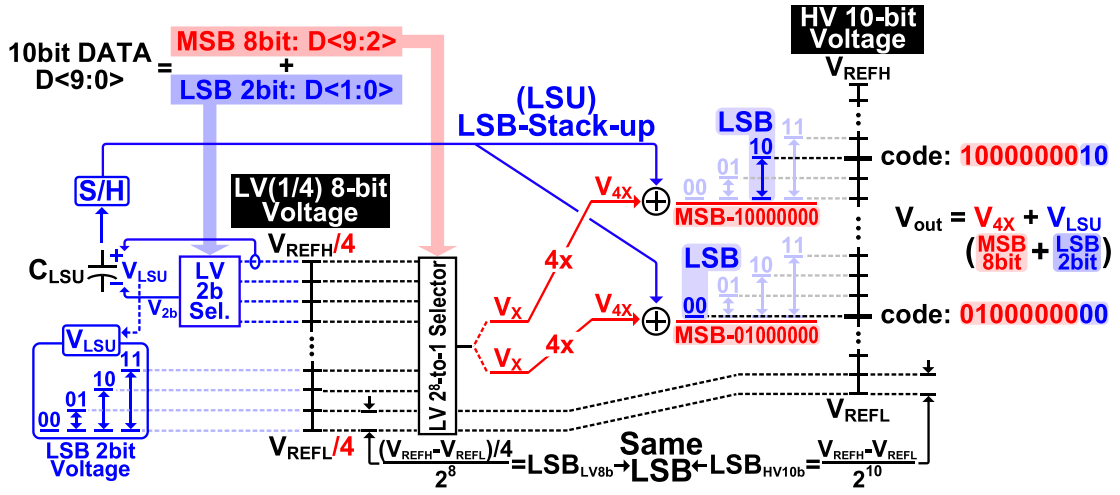


Fig. 4. Operational principle of the proposed LSB-stacked LV-to-HV-amplify 10-bit DAC.

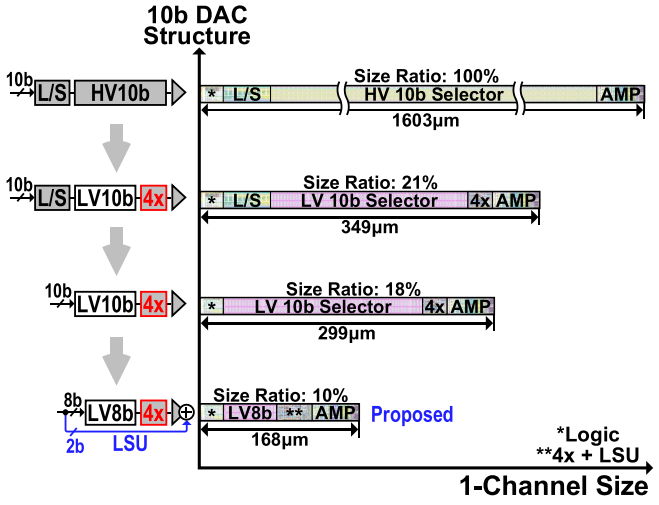


Fig. 5. Comparison of column channel layout designs to investigate the contributions of the proposed area-reduction techniques.

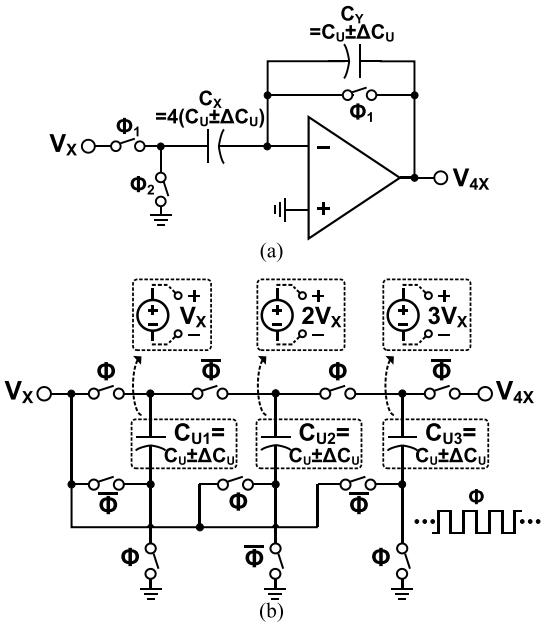


Fig. 6. (a) Conventional charge-based voltage amplifier [42]. (b) Proposed mismatch-insensitive SC 4×-multiplier.

number of Φ cycles with its optimum frequency (f_Φ) will be investigated in Section III-C.

Fig. 8 shows the 1000-point Monte-Carlo simulation results of the typical charge-based voltage amplifier [see Fig. 6(a)] and the proposed SC 4×-multiplier [see Fig. 6(b)]. To demonstrate the SC 4×-multiplier's mismatch-insensitivity, only the capacitance dispersion ($\sigma = 0.1\%$ in 130-nm CMOS) of the metal–insulator–metal (MiM) capacitors is applied in Fig. 8, and a unit capacitance (C_U) of 100 fF is used in both ($C_X = 4C_U = 4C_Y$ and $C_{U1} = C_{U2} = C_{U3} = C_U$). As shown in Fig. 8(a), the behavioral model of Fig. 6(a) with variance-applied MiM capacitors has a high-gain variation of 0.73%. Meanwhile, the proposed SC 4×-multiplier exhibits a trivial gain variation of $1.57 \times 10^{-6}\%$ under the same condition, as shown in Fig. 8(b). It should also be highlighted that the SC 4×-multiplier utilizes $3{\cdot}C_U$, accounting for only 60% of $5{\cdot}C_U$ required by the charge-based voltage amplifier. Fig. 8(b) also displays the post-layout Monte-Carlo simulation result of the SC 4×-multiplier when all nonidealities are enabled, such as MiM capacitor mismatch, threshold (V_{TH}) dispersion of transistors, and parasitic capacitances (with their variations) influencing the SC 4×-multiplier's gain loss. It shows a maximum gain variation of 0.03%, validating that the proposed SD-IC has sufficient immunity to process variations to obtain high interchannel uniformity.

D. Detailed Operational Phases

Fig. 9(a) illustrates the detailed operation sequence in the LSB-stacked LV-to-HV-amplify 10-bit DAC shown in Fig. 2. At the initial phase (Phase 1), the lower 2-bit voltage, $V_{LSU}(=V_{REFH}/4 - V_{2b})$, and the inverted offset ($-V_{OS}$) of the buffer amplifier are simultaneously sampled on C_{LSU} by turning on S_1 and S_2 switches. To sample $-V_{OS}$ at C_{LSU}, it is necessary to flip the offset voltage's polarity using the

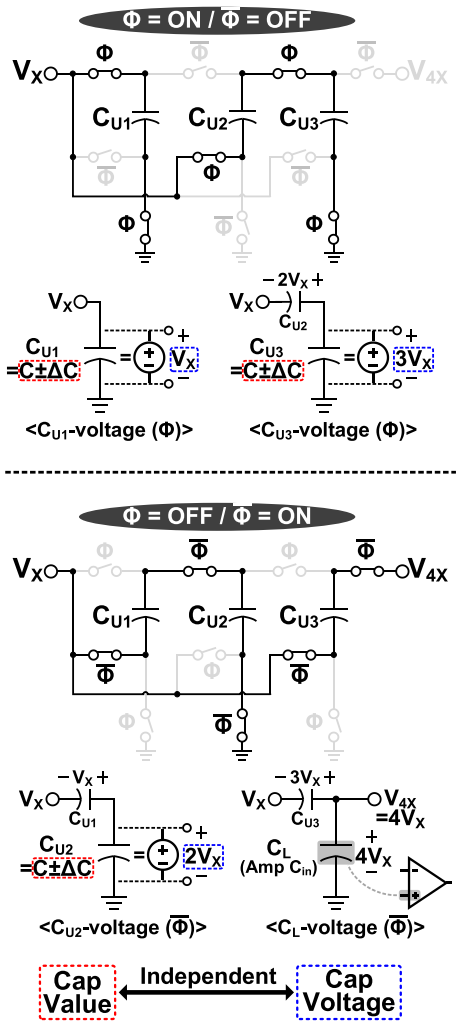
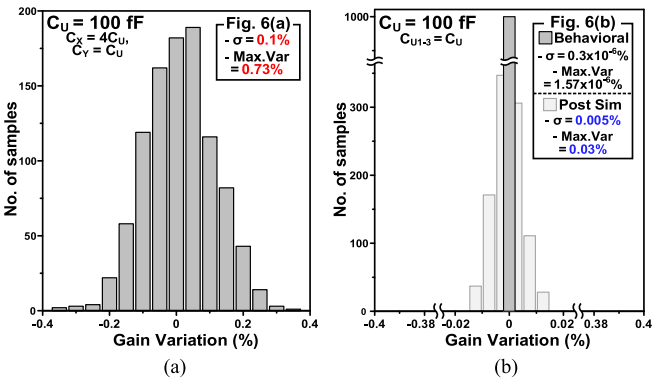


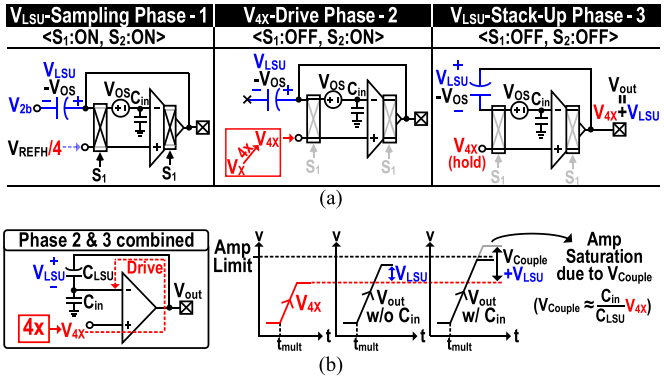
Fig. 7. Pile-up of capacitor-voltage stacks in the proposed SC 4×-multiplier.



(a) (b)

Fig. 8. Monte-Carlo simulation results: (a) typical charge-based voltage amplifier of Fig. 6(a) and (b) proposed SC 4×-multiplier of Fig. 6(b).

path-swappers placed at the input and output of the amplifier; this is done by activating S_1. During the Phase 1, the V_X is selected from the LV 8-bit R-string, and the SC 4×-multiplier begins a V_X-to-V_{4X} amplification before connecting the V_{4X} node to the amplifier input, as depicted in Fig. 3. Next, in the V_{4X}-drive phase (Phase 2) with S_1-OFF and S_2-ON, the upper 8-bit voltage, V_{4X}, of the SC 4×-multiplier is driven to the



(a) (b)

Fig. 9. (a) Operational sequence of the proposed DAC. (b) Coupling issue if V_{4X}-drive and V_{LSU}-stack-up phases are not separated.

positive input of the buffer amplifier. During this phase, the top plate of C_{LSU} is opened (floated) to prevent the V_{4X}'s transition from being ac-coupled to C_{LSU}. After V_{4X} is settled to $4{\cdot}V_X$, the Φ-clocking frequency (f_Φ) of the 4×-multiplier is lowered to reduce the dynamic power consumption. Lastly, at the V_{LSU}-stack-up phase (Phase 3), the 4×-multiplier stops switching ($f_\Phi = 0$), and the 2-bit V_{LSU} is piled up on the V_{4X} by turning off S_1 and S_2, completing the 10-bit D/A-converted $V_{\mathrm{out}}(=V_{4X} + V_{\mathrm{LSU}})$. The offset ($+V_{\mathrm{OS}}$) of the amplifier is also canceled out during this phase by the previously sampled $-V_{\mathrm{OS}}$ on C_{LSU} and the path-swapping behavior. The detailed operation sequence of Fig. 9(a) can be confirmed again in the timing diagram depicted in Fig. 3. Fig. 9(b) explains why the V_{4X}-drive and V_{LSU}-stack-up phases must be separated. If they are performed concurrently without floating the top plate of C_{LSU}, the final V_{out} is prone to be distorted and saturated due to the unwanted error V_{couple} coupled via C_{LSU} and C_{in}.

When observing the V_{LSU}-stack-up circuit depicted in Figs. 2 and 9(a), technical concerns of charge injection and clock feedthrough are likely to arise, but have little effect on the DAC linearity. The S_1-switch on the left side of C_{LSU} causes a nearly input-independent error owing to V_{2b}, which fluctuates very weakly within a lower 2-bit range. The S_2-switches connected to the right side and the bottom of C_{LSU} are complementary, hence canceling out the switching errors on their own.

III. Design Considerations and Chip Implementation

A. DAC Linearity

Parasitic capacitance strayed on the top-plate of MiM capacitor slightly distorts the SC 4×-multiplier gain to be $4 \cdot (1 - \alpha)$, where α is the gain decrement factor. Also, it may lead to a discrepancy between the 4×-multiplier-based 8-bit conversion and the 2-bit LSU, thereby impacting on the linearity of the 10-bit DAC. Fig. 10 illustrates the voltage-step errors caused by α in the LSB-stacked LV-to-HV-amplify DAC. If accepting the unavoidable gain loss of α, the desired voltage-step would be defined to be $(1 - \alpha) \cdot V_{\mathrm{Rstr}}$, where V_{Rstr} is the 1-$\mathrm{LSB}_{\mathrm{LV8b}}$ voltage segmented from the LV 8-bit R-string. However, because the V_{LSU} corresponding to the

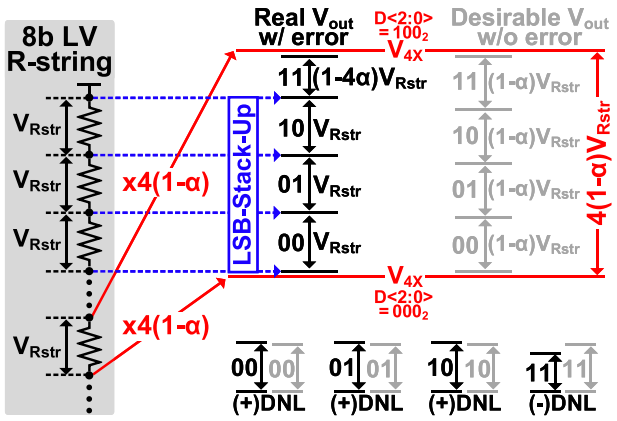


Fig. 10. Nonlinearity (DNL error) induced by the 4×-multiplier's gain loss (α).

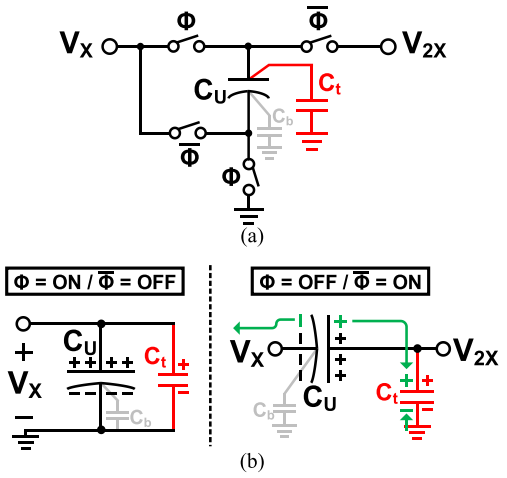


Fig. 11. (a) Simplified SC 2×-multiplier. (b) Equivalent model according to Φ.

lower 2-bit $D\langle 1{:}0\rangle$ is directly sampled from the same global R-string without 4×-multiplication, it is clearly independent of α. As a result, the voltage-steps for $D\langle 1{:}0\rangle = `00_2'$ to '$10_2$' are identical to $V_{\mathrm{Rstr}}$, but the voltage-step for $D\langle 1{:}0\rangle = `11_2'$ is determined as $(1-4\alpha)\cdot V_{\mathrm{Rstr}}$ due to the accumulated gain loss. If calculating the differential nonlinearity (DNL) with the desired voltage-step of $(1-\alpha)\cdot V_{\mathrm{Rstr}}$, the DNLs corresponding to $D\langle 1{:}0\rangle =$ "00_2" to "10_2" will have a positive value and can be expressed as

$$(+)\mathrm{DNL} = \frac{V_{\mathrm{Rstr}}}{(1-\alpha)V_{\mathrm{Rstr}}} - 1 = \frac{\alpha}{1-\alpha}[\mathrm{LSB}]. \tag{2}$$

On the other hand, the DNL value for $D\langle 1{:}0\rangle = `11_2'$ will be negative and can be given by

$$(-)\mathrm{DNL} = \frac{(1-4\alpha)V_{\mathrm{Rstr}}}{(1-\alpha)V_{\mathrm{Rstr}}} - 1 = \frac{-3\alpha}{1-\alpha}[\mathrm{LSB}]. \tag{3}$$

The bottom of Fig. 10 describes the concepts of (2) and (3). The maximum DNL of the proposed DAC is likely to be determined by (3) rather than (2), and thus, the criterion to attain "DNL $<$ 0.5 LSB" can be derived as "$\alpha < 0.14$ (14%)."

B. Derivation of the SC 4×-Multiplier's Gain Loss (α)

Before investigating the gain loss of α in the SC 4×-multiplier, a more simplified 2×-multiplier will be explored for the sake of simplicity, as shown in Fig. 11. When $\Phi =$ ON, the voltages across both C_U and the top-plate parasitic C_t are charged evenly to V_X. Next, during the phase of $\Phi =$ OFF, the C_U is connected in series with V_X to create $V_{2X} = 2\cdot V_X$. However, some of the charges held in C_U inevitably leak to C_t because the voltage across C_t needs to be increased from V_X to V_{2X}. As a result of C_t, the SC 2×-multiplier suffers a gain loss. In contrast, the bottom-plate parasitic C_b has no effect on the gain loss. During the two operation phases shown in Fig. 11(b), total charge conservation can be expressed as

$$Q_{U,\phi} + Q_{t,\phi} = Q_{U,\bar{\phi}} + Q_{t,\bar{\phi}} \tag{4}$$

and

$$C_U V_X + C_t V_X = C_U(V_{2X} - V_X) + C_t V_{2X}. \tag{5}$$

Employing (5), we can get the V_X-to-V_{2X} voltage gain given by

$$\frac{V_{2X}}{V_X} = 2\left(1 - \frac{1}{2}\frac{C_t/C_U}{1 + C_t/C_U}\right). \tag{6}$$

As can be observed in (6), the top-plate parasitic C_t must be reduced for its gain to be close to two. Fortunately, the structural merit of the MiM capacitor, which is used as C_U, facilitates minimizing C_t.

Fig. 12 shows the detailed parasitic capacitances affecting the gain loss in the SC 4×-multiplier. In Fig. 12, C_{t1-3} are the top-plate parasitic capacitances of C_{U1-3}, and C_{c12} (C_{c23}) indicates the coupling capacitance located between C_{U1} (C_{U2}) and C_{U2} (C_{U3}). To be more simplified, the impacts of C_t and C_c on the gain loss can be considered separately. In a similar manner to (4)–(6), the SC 4×-multiplier's gain when taking only C_t into account is calculated to be (7), as shown at the bottom of the next page. Also, the voltage gain affected by C_c can be expressed as (8), as shown at the bottom of the next page. Incorporating (7) and (8) yields the gain loss of α, which is approximately determined as

$$\alpha \approx \frac{1}{4}\frac{\sum_{i=1}^{3}\frac{C_{ti}}{C_{Ui}}}{1+\sum_{i=1}^{3}\frac{C_{ti}}{C_{Ui}}} + \frac{1}{2}\frac{\sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right)+\sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right)}{1+\sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right)+\sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right)}. \tag{9}$$

Fig. 13 compares the calculation model of (9) with the simulated gain loss (α). In our layout design, the parasitic C_t and C_c were extracted to be 5.6 and 0.5 fF, respectively. As seen in Fig. 13, the calculation with (9) is closely similar to the simulated one, proving that the model of (9) is accurate enough. It can also be observed in (9) and Fig. 13 that higher C_U reduces the gain loss of α. However, because the die area is directly proportional to C_U, optimum choice of C_U is necessary to assure compactness as well as DAC linearity (degraded by α). In this work, the C_U was chosen as 100 fF, occupying a modest area of 67 μm^2 and having low α of 4.8% ($<$14% for DNL $=$ 0.5 LSB).

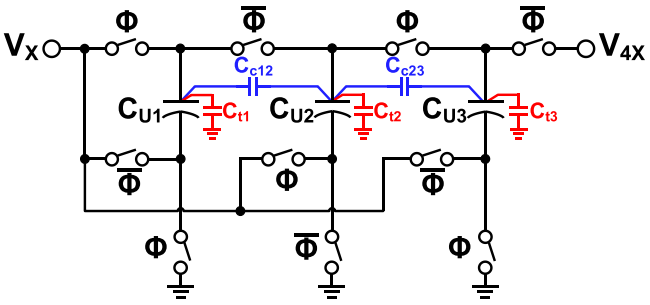


Fig. 12. Parasitic capacitances affecting the gain loss of the SC 4×-multiplier.

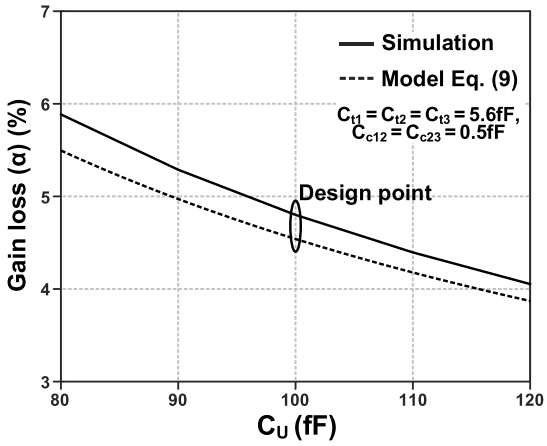


Fig. 13. Simulated gain loss versus calculated gain loss by (9).

Fig. 14 displays the calculated, simulated, and measured α with $C_U = 100$ fF. The gain loss acquired by the post-layout simulation is roughly 1% higher than the calculated α because of nondominant parasitic capacitances other than C_t and C_c. Such nondominant parasitic capacitances are prone to alter depending on the voltage (V_X) of the SC 4×-multiplier because they are mainly formed by the stray capacitances of the MOSFET switches. Even if their capacitance values change due to inconstant V_X, the impact on the variation of α can be negligible, considering that their contributions are too minor compared to relatively constant C_t and C_c. The

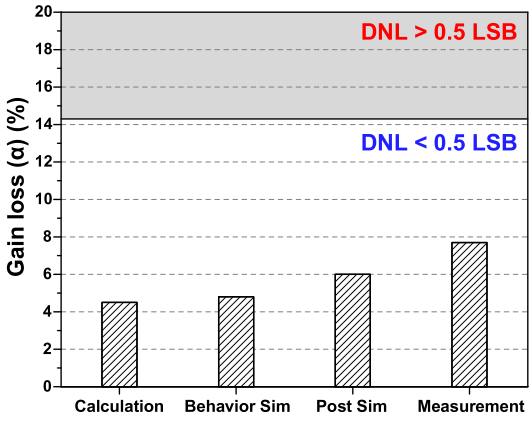


Fig. 14. Gain loss obtained by calculation, simulation, and chip measurement.

measured α after fabricated chip test is 7.8%, which is still lower than the baseline (14%) that exhibits a DNL of 0.5 LSB.

C. Optimization of SC 4×-Multiplier

The capacitance $C_U (= C_{U1-3})$ and switching frequency f_Φ are key design parameters for the SC 4×-multiplier. They determine the V_X-to-V_{4X} settling speed and accuracy, which have significant impacts on the required conversion time and linearity in the proposed DAC. Since how to select C_U has previously been discussed, this section will focus on the optimal design of f_Φ.

In the determination of f_Φ, the RC time-constant (τ_{m1}) at V_{4X}, which is formed by C_L (input capacitance (C_{in}) of the buffer amplifier) and the equivalent resistance (R_{mult}) of the SC circuit, should be taken into account, as shown in Fig. 15. In the SC 4×-multiplier design similar to a Dickson charge-pump [47], R_{mult} can be modeled as $12/(C_U \cdot f_\Phi)$, and the time-constant τ_{m1} is thus defined by

$$\tau_{m1} = R_{mult} C_L = \left(\frac{12}{C_U f_\phi}\right) C_L. \tag{10}$$

Assuming a transition of V_{4X} from $V_{\text{REFH}}/4$ (≈ 1.2 V), the V_{4X} will settles exponentially to the target value of $4 \cdot V_X$,

$$\left(\frac{V_{4X}}{V_X}\right)_{C_t} = 4\left[1 - \frac{1}{4}\frac{\sum_{i=1}^{3}\left(\frac{C_{ti}}{C_{Ui}}\right) + 2\frac{C_{t1}C_{t2}}{C_{U1}C_{U2}} + 2\frac{C_{t2}C_{t3}}{C_{U2}C_{U3}} + 2\frac{C_{t3}C_{t1}}{C_{U3}C_{U1}} + 3\frac{C_{t1}C_{t2}C_{t3}}{C_{U1}C_{U2}C_{U3}}}{1 + \sum_{i=1}^{3}\left(\frac{C_{ti}}{C_{Ui}}\right) + \frac{C_{t1}C_{t2}}{C_{U1}C_{U2}} + \frac{C_{t2}C_{t3}}{C_{U2}C_{U3}} + \frac{C_{t3}C_{t1}}{C_{U3}C_{U1}} + \frac{C_{t1}C_{t2}C_{t3}}{C_{U1}C_{U2}C_{U3}}}\right] \approx 4\left(1 - \frac{1}{4}\frac{\sum_{i=1}^{3}\frac{C_{ti}}{C_{Ui}}}{1 + \sum_{i=1}^{3}\frac{C_{ti}}{C_{Ui}}}\right) \tag{7}$$

$$\left(\frac{V_{4X}}{V_X}\right)_{C_c} = 4\left[1 - \frac{1}{2}\frac{\sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right) + \sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right) + \frac{C_{c12}C_{c23}}{C_{U1}C_{U2}} + \frac{C_{c12}C_{c23}}{C_{U2}C_{U3}} + 2\frac{C_{c12}C_{c23}}{C_{U3}C_{U1}}}{1 + \sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right) + \sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right) + \frac{C_{c12}C_{c23}}{C_{U1}C_{U2}} + \frac{C_{c12}C_{c23}}{C_{U2}C_{U3}} + 2\frac{C_{c12}C_{c23}}{C_{U3}C_{U1}}}\right]$$
$$\approx 4\left(1 - \frac{1}{2}\frac{\sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right) + \sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right)}{1 + \sum_{i=1}^{2}\left(\frac{C_{c12}}{C_{Ui}}\right) + \sum_{i=2}^{3}\left(\frac{C_{c23}}{C_{Ui}}\right)}\right) \tag{8}$$

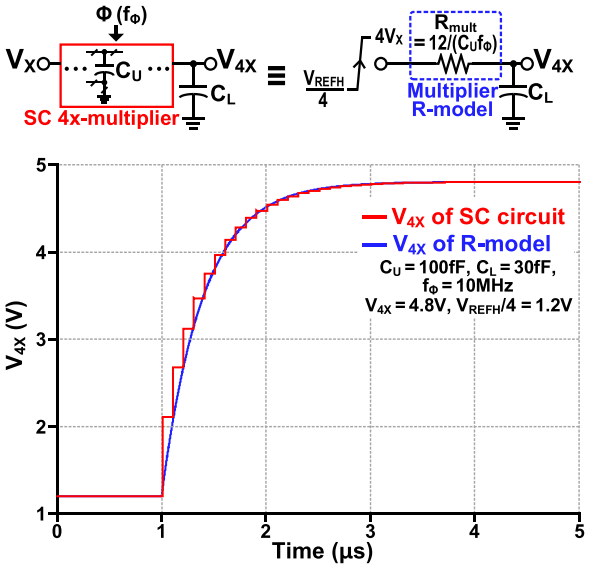


Fig. 15. Equivalent R-model (R_{mult}) of the SC 4×-multiplier.

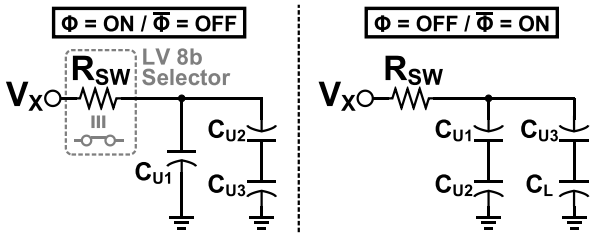


Fig. 16. Equivalent RC model of the SC 4×-multiplier according to Φ.

as follows:

$$V_{4X}(t) = 4 \cdot V_X - \left(4 \cdot V_X - \frac{V_{\text{REFH}}}{4}\right) \exp\left(-\frac{t}{\tau_{m1}}\right). \quad (11)$$

As a result, the following requirement of (12) must be satisfied so that V_{4X} settles higher than the baseline meeting "DNL < 0.5 LSB [refer to (3)]" during the V_X-to-V_{4X} amplifying time (T_{4X}), which is far less than the duration of the V_{4X}-drive phase:

$$V_{4X}(t = T_{4X}) > (4 \cdot V_X)(1 - 0.14). \quad (12)$$

Applying $C_L = 30$ fF, $T_{4X} = 2$ μs, and maximum $V_{4X} = 4.8$ V, the minimum required $C_U \cdot f_\Phi$ can be derived as

$$C_U f_\phi > 0.3 \times 10^{-6}\ [\Omega^{-1}]. \quad (13)$$

It should be noted that (13) assumes a worse scenario than the actual operation of the proposed DAC in the aspect of V_{4X} settling. As seen in Figs. 2 and 3, the SC 4×-multiplier begins switching without $C_L (= C_{\text{in}}$ of the amplifier) in advance before the V_{4X}-drive (Phase 2). Therefore, during the V_{4X}-drive phase, V_{4X} can settle to the desired value much faster than (11).

Another factor to consider is the settling time of C_U's bias voltage, which may be delayed by the nonideal resistance (R_{SW}) of the 8-bit voltage selector that selects V_X from the global R-string. If it is not rapid enough, the assumption of (10) is difficult to be guaranteed. Fig. 16 shows the equivalent

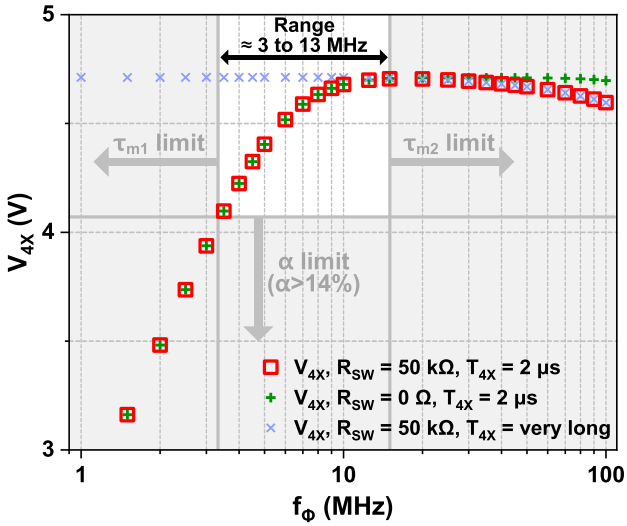


Fig. 17. Settled V_{4X} voltages for Φ-clocking frequency (f_Φ) when $V_X = 1.2$ V.

RC model of the SC 4×-multiplier. The time-constant (τ_{m2}) when Φ = ON is longer than that of Φ = OFF and can be expressed as

$$\tau_{m2} = R_{\text{SW}} \cdot \left(C_{U1} + \frac{1}{1/C_{U2} + 1/C_{U3}}\right) = R_{\text{SW}} \cdot (1.5C_U). \quad (14)$$

Assuming the bias voltage of each C_U needs to be charged to 99.3%, $5 \cdot \tau_{m2}$ should be less than half of $1/f_\Phi$. Note that it is sufficiently marginal condition because the C_U's bias voltage can still be progressively charged as Φ repeats. By substituting R_{SW} with 50 kΩ (voltage selector's equivalent resistance), the maximum criterion for $C_U \cdot f_\Phi$ can thus be calculated as follows:

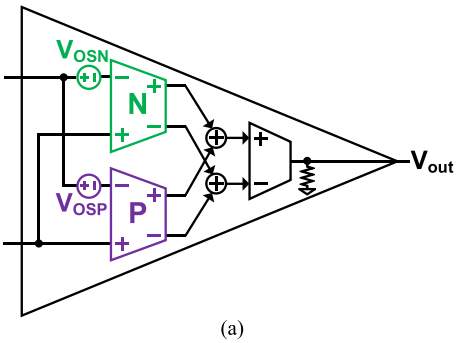
$$C_U f_\phi < 1.3 \times 10^{-6}\ [\Omega^{-1}]. \quad (15)$$

Since the C_U was chosen as 100 fF with considerations of die area and linearity in Section III-B, incorporating (13) and (15) yields an optimal range of f_Φ, as follows:

$$3\ \text{MHz} < f_\phi < 13\ \text{MHz}. \quad (16)$$

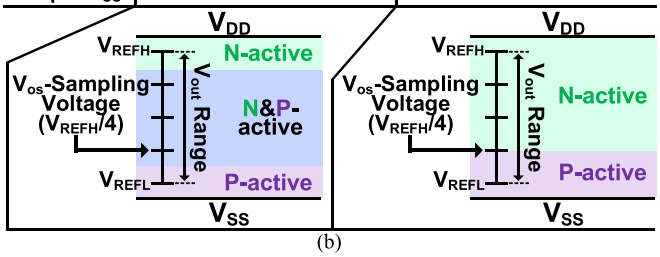
In this work, f_Φ is designed to be 10 MHz to initially boost the V_X-to-V_{4X} conversion speed and is lowered to 5 MHz in the middle of the V_{4X}-drive phase (Phase 2) to reduce power consumption, as depicted in Fig. 3.

Fig. 17 shows the settled V_{4X} voltages (red-square dots) with respect to f_Φ when $V_X = 1.2$ V, $C_U = 100$ fF, and $T_{4X} = 2$ μs. This demonstrates that the time-constant τ_{m1} of (10) limits the minimum f_Φ required to satisfy the condition of (12). Meanwhile, assuming T_{4X} is unconstrained, the τ_{m2} of (14) caused by R_{SW} rather decreases V_{4X} below the target level when f_Φ is set too high. Consequently, Fig. 17 reconfirms the optimum f_Φ range given in (16), as well as our design (f_Φ is initially 10 MHz and then reduced to 5 MHz) can be a reasonable choice for balancing accuracy and power consumption.

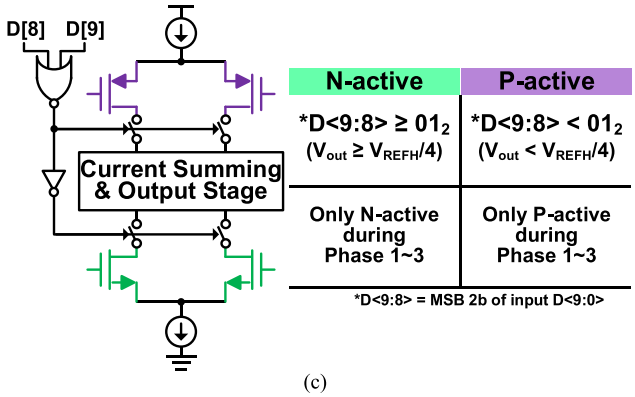


(a)

	Conventional		Proposed	
	$V_{out} \approx V_{DD}$	$V_{out} \approx V_{SS}$	$V_{out} \approx V_{DD}$	$V_{out} \approx V_{SS}$
Active Input @ Phase 2	N & P	N & P	N	P
V_{OS_sample} @ Phase 2	V_{OSN} & V_{OSP}	V_{OSN} & V_{OSP}	V_{OSN}	V_{OSP}
Active Input @ Phase 3	N	P	N	P
V_{OS_out} @ Phase 3	V_{OSN}	V_{OSP}	V_{OSN}	V_{OSP}
Sampled V_{OS} = Output V_{OS}	X ☹		O ☺	



(b)



(c)

Fig. 18. (a) Typical rail-to-rail amplifier. (b) V_{OS_sample} and V_{OS_out} in accordance with V_{out}. (c) Proposed V_{out}-adaptive DIP control scheme for $V_{OS\_sample} = V_{OS\_out}$.

Nonideal switching effects, such as charge injection and clock feedthrough, are common concerns in the design of SC circuits. In the SC 4×-multiplier, each switch is adjacent to other switches operating in the opposite phase, as shown in Fig. 7. Such complementary switch-arrangement can help with self-compensation of nonideal switching errors. Even if the errors could not be fully compensated, their impact on DNL performance would be minimal since the absolute error difference between adjacent input codes is negligibly small. In visual applications, note that the DAC linearity is mostly evaluated by the DNL rather than the INL, taking into account the human-eye's perception characteristics.

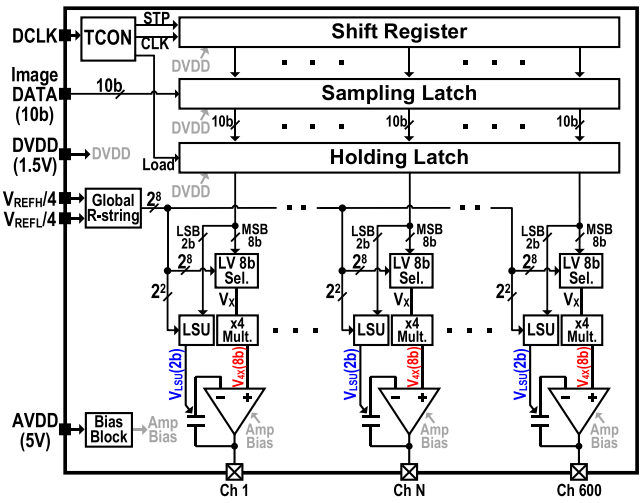


Fig. 19. Top architecture of the proposed 600-channel SD-IC.

D. Interchannel Uniformity and Adaptive Offset Cancellation

The proposed LSB-stacked LV-to-HV-amplify DAC has the architectural merit of lower output deviation in the multi-channel SD-IC for the following reasons. First, both the LV 8-bit voltage selectors (selecting V_X) and the LV 2-bit voltage selectors (producing V_{LSU}) of all column channels share the common global R-string; hence, the process variation cannot disperse V_X as well as V_{LSU} across channels. Second, the SC 4×-multiplier, which generates V_{4X} from V_X, is also very insensitive to the capacitor mismatch, as shown in Fig. 8(b). In particular, the post-layout Monte-Carlo simulation of Fig. 8(b) demonstrates that, despite an insignificant but inescapable gain loss (α), the variance of the SC 4×-multiplier gain is well constrained to be $\sigma = 0.005\%$ even when all nonidealities are applied. Third, the offset (V_{OS}) of the amplifier in each independent channel can be inherently canceled out during the DAC operation described in Fig. 9(a). The final DAC output, including V_{OS}, can be given as

$$V_{out} = V_{4X}(=4V_X) + V_{LSU} - V_{OS\_sample} + V_{OS\_out} \quad (17)$$

where V_{OS_sample} is the sampled offset at the V_{LSU}-sample (Phase 1), and V_{OS_out} is the canceled offset by the V_{LSU}-stack-up (Phase 3). When looking at (17), V_{OS} seems to be a removable factor, but careful consideration is mandated to ensure that $V_{OS\_sample} = V_{OS\_out}$.

Fig. 18(a) shows the internal design of the conventional amplifier. It typically consists of n- and p-type differential input pairs (DIPs) to cover a rail-to-rail voltage range of V_{out}. The N-DIP has an input-referred offset, V_{OSN}, but it differs from the P-DIPs offset, V_{OSP}, because they are clearly uncorrelated. At the V_{LSU}-sample (Phase 1), the voltage of $V_{REFH}/4$ is applied to the amplifier input, as shown in Fig. 9(a). Accordingly, the offset (V_{OS_sample}) sampled on C_{LSU} includes V_{OSN} as well as V_{OSP} because both N- and P-DIP are activated at a quarter of FSR ($=V_{REFH}/4$). On the other hand, if V_{out} is close to the maximum output ($\approx V_{DD}$) or the minimum output (≈ 0 V), only one of the N- and P-DIP is activated at the V_{LSU}-stack-up (Phase 3), resulting in $V_{OS\_sample} \neq V_{OS\_out}$.

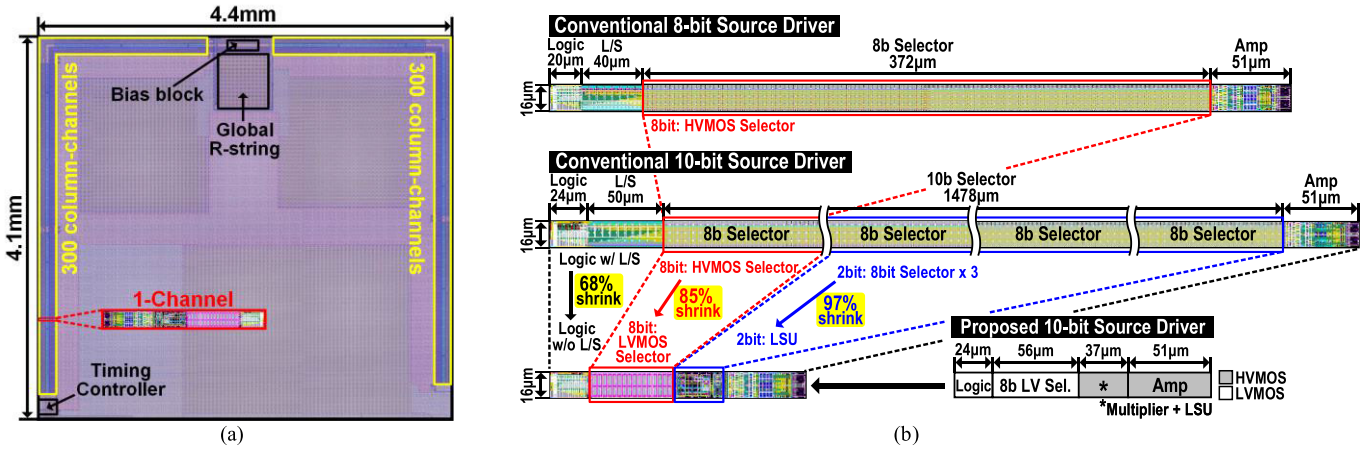


Fig. 20. (a) Micrograph of the fabricated SD-IC. (b) One-channel area comparison between conventional (8-bit and 10-bit) SD-IC and the proposed 10-bit SD-IC.

The issue of inconsistent offset voltage is also summarized in the left-side of Fig. 18(b).

Fig. 18(c) shows the proposed V_{out}-adaptive offset cancellation scheme. The key idea to make $V_{\text{OS\_sample}}$ equal to $V_{\text{OS\_out}}$ is to activate only one of N- and P-DIP during all behavioral phases (Phases 1–3) in accordance with the upper 2-bit $D\langle 9{:}8\rangle$ of the input data. When $D\langle 9{:}8\rangle$ is higher (less) than '01_2', V_{out} is predicted to be larger (lower) than $V_{\text{REFH}}/4$, and only the N-DIP (P-DIP) is activated to accommodate it. Consequently, the range where both N- and P-DIP are concurrently active is eliminated, as described in the right-side of Fig. 18(b). Owing to the consistent activation of DIP (either N- or P-DIP) during all phases, both $V_{\text{OS\_sample}}$ and $V_{\text{OS\_out}}$ can contain the identical offset voltage, leading to $V_{\text{OS\_sample}} = V_{\text{OS\_out}}$. As a result of the proposed V_{out}-adaptive DIP control, $V_{\text{OS\_sample}}$ and $V_{\text{OS\_out}}$ in (17) can be perfectly canceled out, significantly contributing to high interchannel uniformity in the proposed SD-IC.

E. Top Architecture of Source-Driver IC

The top architecture of the proposed SD-IC is illustrated in Fig. 19. Total of 600 column driver channels are integrated in this chip. In addition to the proposed DAC, each column channel includes 10-bit sampling and holding latches for the distribution of digital display data. The digital 10-bit data is sequentially transferred to each column channel, and the sampling latch captures the data pertaining to its channel with the shift register's synchronization. Every 1-horizontal (1-H) time, all holding latches are simultaneously updated. Finally, the data contained in the holding latch is converted to an analog signal (V_{out}), which is then driven to a pixel on the display panel. The proposed SD-IC was designed to typically operate with a drivable FSR ranging from 300 mV (V_{REFL}) to 4.5 V (V_{REFH}).

Considering that a large number of column driver channels are integrated into the SD-IC, the following are some of our design methodologies used in this work. First, shielding lines composed of the same metal layers as those of the MiM capacitors used for the SC 4×-multiplier were inserted between the column driver channels. If they are biased to a silent dc voltage, it can aid in resolving the crosstalk issue, in which

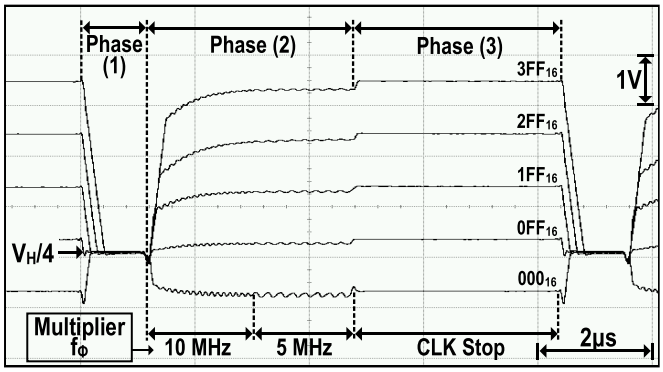


Fig. 21. Measured waveforms of V_{out} for five different data inputs.

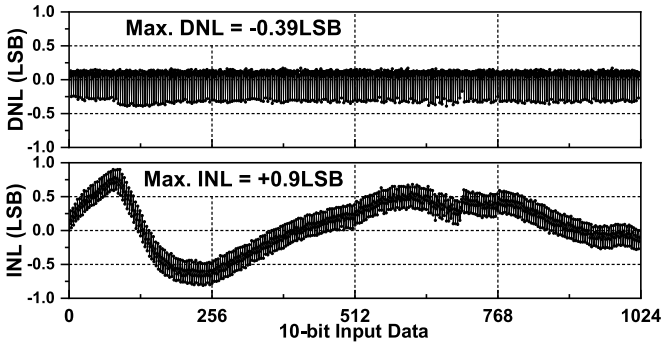


Fig. 22. Measured DNL and INL at 10-bit resolution.

the switching noises of the SC circuit are coupled to the neighboring channels. Second, repeaters reconstructing global control signals (S_1 and S_2) and clock (Φ) into clear digital forms were placed at every given distance on their routing lines to distribute them to channels over a long distance. Although the repeaters add a delay to the digital signal delivery, this has no significant impact on the functionality of each column channel if all signals (S_1, S_2, and Φ) have the same delay achieved by matching the repeater design. Furthermore, the difference in latency of Φ at each column channel would not be a considerable concern because each column channel

TABLE I
PERFORMANCE SUMMARY IN COMPARISON WITH PREVIOUS STATE-OF-THE-ART SD-ICS

	JSSC'14 [40]	IEEE TCE'19 [23]	JSSC'19 [28]	TCAS-II'20 [29]	JSSC'21 [42]	TCAS-II'21 [30]	**This Work**
Target Display (Panel Load)	60-Hz FHD Mobile LCD (30 kΩ & 30 pF)	Mobile LCD (10 kΩ & 30 pF)	UHD Large-Sized LCD (5 kΩ & 300 pF)	60-Hz QHD Mobile OLED (10 kΩ & 46 pF)	Mobile LCD or OLED (30 kΩ & 30 pF)	UHD 55-inch OLED (6.5 kΩ & 100 pF)	60-Hz WQXGA Mobile OLED (30 kΩ & 30 pF)
CMOS Technology	110-nm	100-nm	180-nm	80-nm	90-nm	180-nm	130-nm
Gray Scale	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
Output Range	0.25 to 4.75 V	0.25 to 4.75 V	0.2 to 17.8 V	1 to 6 V	0.2 to 4.8 V	2 to 13.5 V	0.3 to 4.5 V
DNL / INL	0.25 / 0.43 LSB	0.4 / 0.7 LSB	0.14* / 0.46* LSB	0.31 / 0.58 LSB	0.2 / 0.42 LSB	0.47* / 0.41* LSB	0.39 / 0.9 LSB
Static Current Dissipation per Channel	0.9 μA	1 μA	7 μA	N/A	2.8 μA	7.5* μA	1.8 μA
Chip Power Consumption	N/A	20 mW (642 channels)	216 mW (1026 channels)	N/A	N/A	128.2* μW per 1-channel	28.8 mW (600 channels)
Max. DVO	5.6 mV	15 mV	16 mV	1.65 mV	7.9 mV	N/A	**4.82 mV**
1-Channel Total Area	5010 μm^2 (334 × 15)	6440 μm^2 (460 × 14)	11730 μm^2 (510 × 23)	7390 μm^2 (739 × 10)	5328 μm^2 (296 × 18)	27160 μm^2 (970 × 28)	**2688 μm^2 (168 × 16)**
Area Shrinkage**	15.4 %	10.7 %	N/A	32.6 %****	31.0 %	N/A	**65.2%**
Area Ratio***	186 %	239 %	436 %	275 %	198 %	1010 %	**100%**

* Simulated results. ** Compared to conventional 8-bit R-DAC, of which layout was individually done by each reference paper.
*** 100% × (1-channel total area of each reference paper / 1-channel total area of this work). **** Area shrinkage without logic and L/S.

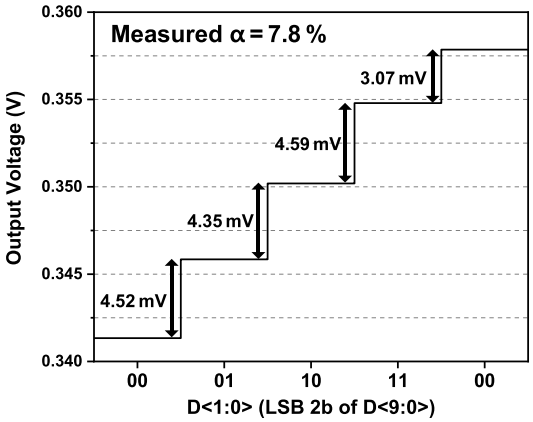


Fig. 23. Measured voltage steps to estimate the actual gain loss of α.

can work independently to some extent within 1-H time. In our post-layout simulation, the total delay of Φ from the timing-controller to the 600th column channel at a distance of 11.8 mm was simulated to be 5.3 ns under $f_\Phi = 10$ MHz.

IV. MEASUREMENT RESULTS

The proposed 600-channel 10-bit SD-IC was fabricated in a 130-nm 1P6M CMOS process, as shown in Fig. 20(a). LV-domain analog circuits, including 8-bit and 2-bit voltage selectors, and digital blocks operate at 1.5-V supply voltage, while HV analog circuits, such as the SC 4×-multiplier and amplifier, are performed under a supply voltage of 5 V.

Fig. 20(b) shows the single-channel layout design of the proposed SD-IC in comparison with the conventional R-DAC-based 8-bit and 10-bit column driver channels. Compared to conventional 10-bit R-DAC, the proposed DAC design solution reduces the logic area by 68% due to the removal of L/S, shrinks the size of the 8-bit DAC portion by 85% by utilizing only LV-MOSs, and realizes an additional 2-bit by consuming only 3% of the 3× area of the 8-bit voltage selector owing to the LSU technique. In summary, the proposed SD-IC occupies 168 × 16 μm^2 per channel, which is only 10% of the die area of the conventional 10-bit SD-IC.

Fig. 21 shows the captured output (V_{out}) waveforms for five different 10-bit data inputs of $D\langle 9{:}0\rangle$ with an emulated panel load of 30 kΩ and 30 pF. Three operational phases (Phases 1–3), which are explained in Figs. 3 and 9(a), can also be verified in Fig. 21. In this work, the 1-H time of 8.2 μs was aimed for a WQXGA-resolution display panel with a frame rate of 60 Hz. By increasing f_Φ up to the maximum frequency of 13 MHz within the optimum range shown in Fig. 17, the duration of the V_{4X}-drive phase (Phase 2) has the potential to be reduced further. Furthermore, it is possible to shorten the period of the V_{LSU}-stack-up phase (Phase 3) to 2 μs, while ensuring the ultimate settling of $V_{out}(=V_{4X}+V_{LSU})$ at a pixel after passing via the panel load. As a result of them, the achievable minimum 1-H time of this work is projected to be 5.3 μs, which corresponds to a 120-Hz WQHD-resolution display panel.

The measured DNL and INL at 10-bit resolution are shown in Fig. 22. With the 1-LSB voltage of 4.1 mV, the worst DNL and INL were measured to be −0.39 and +0.9 LSB, respectively. Because DNL values are closely correlated with the SC 4×-multiplier's gain loss (α), as discussed in Section III-A, the output voltage steps for the lower 2-bit $D\langle 1{:}0\rangle$ were also measured, as shown in Fig. 23. From Fig. 23, the actual α was estimated to be 7.8%, and it well matches with the DNL value.

Fig. 24 shows the deviation of voltage outputs (DVOs) obtained from four different chips, as measured across a range of gray levels. Fig. 24(a) shows that the DVOs measured at a low gray level were 3.82 mV (chip #1), 4.39 mV (chip #2), 4.3 mV (chip #3), and 4.82 mV (chip #4). The results

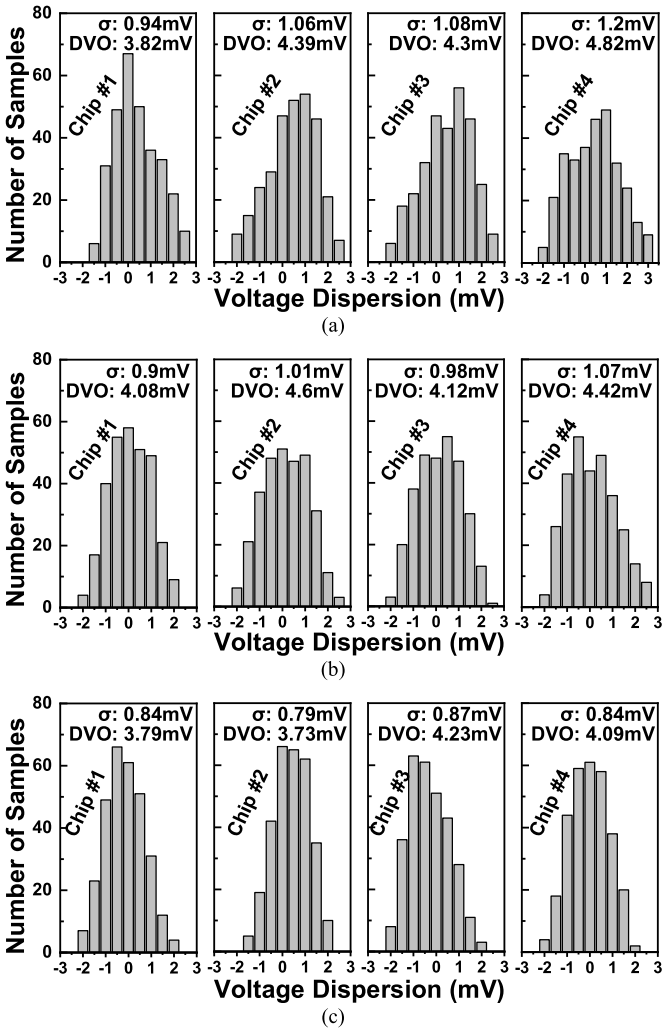


Fig. 24. Measured DVO of four different chips: (a) low gray-level; (b) mid gray-level; and (c) high gray-level.

pertaining to mid and high gray levels were similarly aligned, as illustrated in Fig. 24(b) and (c). The DVO represents the uniformity of the proposed SD-IC by showing the dispersions of the output voltages across multiple channels. In other words, a lower DVO implies better interchannel uniformity. This work obtained excellent DVOs comparable to 1-LSB voltage, demonstrating that the proposed DAC solution is highly insensitive to process variations, such as capacitor mismatch and amplifier offset, as described in Section III-D.

The proposed SD-IC was utilized to demonstrate a 100 × 100 mini-LED display, as shown in Fig. 25(a). Using an external FPGA board, the display data is programed into the SD-IC serially. The SD-IC then converts the digital data to an analog signal, which is driven to the 100 × 100 mini-LED display panel. The 1-H time of the proposed SD-IC was fixedly designed to be 8.2 μs, which was validated in Fig. 21. Thus, in this demonstration, the voltage holding time was deliberately extended to be compatible with the low resolution of the tested mini-LED display. Several demonstration photos are shown in Fig. 25(b). These demonstrations visually validate the high contrast ratio and fine grayscales realized by the proposed 10-bit DAC. However, the experimental tests with

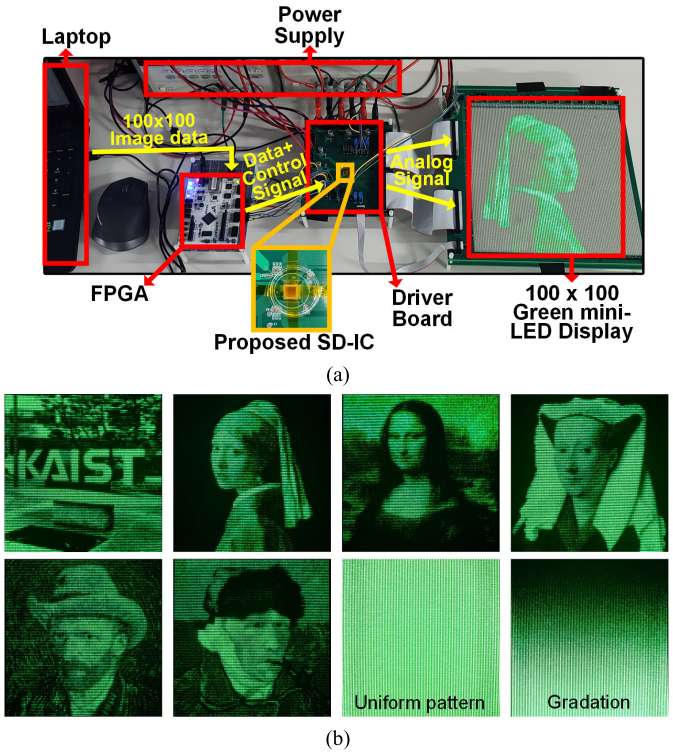


Fig. 25. Real display demonstration to evaluate the proposed SD-IC: (a) display driving system setup and (b) 100 × 100 mini-LED display photographs.

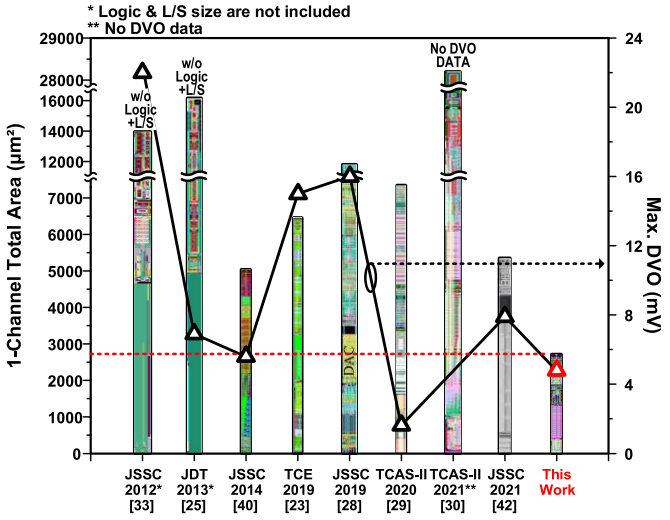


Fig. 26. Comparison of one-channel sizes and measured DVOs.

mini-LEDs used in Fig. 25 have an explicit limitation. Since our SD-IC dedicated to OLED displays uses a voltage-mode driving technique, the mini-LEDs are susceptible to a wavelength (color) shift. For color-shift suppression, pulsewidth modulation (PWM) has been commonly employed to drive LED displays [48]. Therefore, it is essential to note that the purpose of our monochrome mini-LED demonstration is not to test its color gamut but to evaluate the gray-scale depth driven by the proposed SD-IC sensuously.

Table I summarizes the measured performance of the proposed SD-IC and compares it to existing state-of-the-art chips.

This work capable of driving a wide FSR ranging from 0.3 to 4.5 V achieves the smallest size (168 × 16 μm per channel) and superior DVO (4.82 mV) performance (excluding [29]) among the 10-bit SD-ICs. Offset cancellation with the proposed V_{out}-adaptive DIP control, which was described in Section III-D, considerably contributes to improvement in interchannel uniformity (low DVO). Despite having a maximum DNL of less than 0.5 LSB, the proposed SD-IC could not have the best linearity when compared to earlier works; this is dominantly due to the unit capacitance (C_U) of the SC 4×-multiplier being optimally selected to minimize die area while adequately suppressing its gain loss (guaranteeing DNL $<$ 0.5 LSB in 10-bit resolution), as discussed in Sections III-A and III-B. Also, the imperfect matching in the layout design of the global R-string is thought to be one reason for degrading the INL.

As seen in the last row of Table I, the one-channel total area of the proposed SD-IC is approximately 2×-to-4× smaller than those of other chips. In the aspect of area reduction, the proposed LSB-stacked LV-to-HV-amplify DAC shrinks the one-channel area by 65.2% when compared to a conventional 8-bit R-DAC, while other works reduce the channel size by roughly 10%–30%. Fig. 26 graphically compares the one-channel size and the measured DVO of the recently reported SD-ICs, including the proposed chip. As can be seen, our proposed SD-IC exhibits an extremely small size and excellent DVO performance compared to other reported SD-ICs.

V. Conclusion

In this work, a 600-channel display SD-IC was designed and verified through chip fabrication and measurements. Because of the all LV-based voltage selectors and the ultra-compact 2-bit LSB-stack-up approach, as well as the removal of L/S, the proposed LSB-stacked LV-to-HV-amplify 10-bit DAC greatly shrinkages the one-channel size. Moreover, the proposed DAC exhibits outstanding interchannel uniformity in virtue of the mismatch-insensitive nature of the SC 4×-multiplier, which generates the 8-bit voltage (V_{4X}), and the 2-bit LSB-stack-up technique sampling the 2-bit voltage (V_{LSU}) from the global R-string. Offset cancellation with the proposed V_{out}-adaptive DIP control also considerably contributes to improvement in uniformity. In the design of the SC 4×-multiplier, highly elaborated optimizations in terms of linearity and size have been developed and analyzed, resulting in the best performance from the fabricated SD-IC. The proposed 10-bit SD-IC achieves a one-channel size of 2688 μm^2, which is the smallest reported to date, while offering a competitive DVO of 4.82 mV. Moreover, since the proposed DAC design solution is mostly based on the LV domain, the size of the column driver channel has great potential to be reduced further by the use of scaled CMOS technologies.

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References

[1] I. Knausz and R. J. Bowman, "A low power, scalable, DAC architecture for liquid crystal display drivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2402–2410, Sep. 2009.

[2] C.-W. Lu, C.-C. Shen, and W.-C. Chen, "An area-efficient fully R-DAC-based TFT-LCD column driver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2588–2601, Oct. 2010.

[3] J.-H. Kim, B.-D. Choi, and O.-K. Kwon, "1-billion-color TFT-LCD TV with full HD format," *IEEE Trans. Consum. Electron.*, vol. 51, no. 4, pp. 1042–1050, Nov. 2005.

[4] P. Liu and Y. E. Chen, "A 10-bit CMOS DAC with current interpolated gamma correction for LCD source drivers," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 22, no. 6, pp. 958–965, Jun. 2012.

[5] D. Marano, G. Palumbo, and S. Pennisi, "Low-power dual-active class-AB buffer amplifier with self-biasing network for LCD column drivers," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 2832–2835.

[6] D. Marano, G. Palumbo, and S. Pennisi, "Self-biased dual-path push-pull output buffer amplifier topology for LCD driver applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 29–32.

[7] C. Lu, P. Yin, H. Kuo, and S. Pennisi, "A low-quiescent current two-input/output buffer amplifier for LCDs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2012, pp. 1975–1978.

[8] A. D. Grasso, D. Marano, F. Esparza-Alfaro, A. J. Lopez-Martin, G. Palumbo, and S. Pennisi, "Self-biased dual-path push-pull output buffer amplifier for LCD column drivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 663–670, Mar. 2014.

[9] H. Kim and D. Kim, "An active-matrix OLED driver CMOS IC with compensation of non-uniform routing-line resistances in ultra-thin panel bezel," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 484–500, Feb. 2018.

[10] A. D. Grasso, G. Palumbo, and S. Pennisi, "Dual push–pull high-speed rail-to-rail CMOS buffer amplifier for flat-panel displays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 12, pp. 1879–1883, Dec. 2018.

[11] J.-S. Kim, J.-Y. Lee, and B.-D. Choi, "Slew-rate-enhanced rail-to-rail buffer amplifier for TFT LCD data drivers," *Electron. Lett.*, vol. 48, no. 15, pp. 924–925, Jul. 2019.

[12] M. J. Bell, "An LCD column driver using a switch capacitor DAC," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2756–2765, Dec. 2005.

[13] Y.-K. Choi et al., "A compact low-power CDAC architecture for mobile TFT-LCD driver ICs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 176–605.

[14] I.-S. Park, T.-W. Kim, J.-Y. Lee, and B.-D. Choi, "Data driver architecture and driving scheme of AMOLED microdisplay for mobile projectors," *IEEE Trans. Consum. Electron.*, vol. 55, no. 4, pp. 2365–2371, Nov. 2009.

[15] B.-D. Choi and C.-W. Byun, "Data driving methods and circuits for compact and high-image-quality AMOLED mobile displays," *IEEE Trans. Consum. Electron.*, vol. 56, no. 2, pp. 1102–1107, May 2010.

[16] C.-W. Lu, P.-Y. Yin, and Y.-T. Lin, "A column driver architecture with double time-division multiplexing RDACs for TFT-LCD applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2352–2364, Oct. 2014.

[17] T.-J. An, M.-S. Hwang, W.-J. Choe, G.-C. Ahn, and S.-H. Lee, "Area-efficient time-shared digital-to-analog converter with dual sampling for AMOLED column driver IC's," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 10, pp. 3227–3240, Oct. 2018.

[18] J.-S. Kang et al., "A 10 b driver IC for a spatial optical modulator for full HDTV applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 138–592.

[19] J.-S. Kang et al., "10-bit driver IC using 3-bit DAC embedded operational amplifier for spatial optical modulators (SOMs)," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2913–2922, Dec. 2007.

[20] Y.-J. Jeon et al., "A piecewise-linear 10 b DAC architecture with drain-current modulation for compact AMLCD driver ICs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 264–265.

[21] Y.-J. Jeon et al., "A piecewise linear 10 bit DAC architecture with drain current modulation for compact LCD driver ICs," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3659–3675, Dec. 2009.

[22] H.-M. Lee et al., "A 10 b column driver with variable-current-control interpolation for mobile active-matrix LCDs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 266–267.

[23] H. Lee, Y. Jeon, S. Lee, B. Lee, and G. Cho, "An area and power efficient interpolation scheme using variable current control for 10-bit data drivers in mobile active-matrix LCDs," *IEEE Trans. Consum. Electron.*, vol. 65, no. 2, pp. 253–262, May 2019.

[24] C.-B. Park, K.-D. Kim, S.-W. Lee, G.-S. Park, S.-T. Ryu, and G.-H. Cho, "A 10 b linear interpolation DAC using body-transconductance control for AMLCD column driver," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2010, pp. 1–4.

[25] C. Lu, C. Hsiao, Y. Lin, and M. F. Chang, "A 10-bit DAC with 1.6-bit interpolation cells for compact LCD column driver ICs," *J. Display Technol.*, vol. 9, no. 3, pp. 176–183, Mar. 2013.

[26] C. Lu, C. Hsiao, and P. Yin, "A 10-b two-stage DAC with an area-efficient multiple-output voltage selector and a linearity-enhanced DAC-embedded op-amp for LCD column driver ICs," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1475–1486, Jun. 2013.

[27] S.-Y. Ryu et al., "A 13-bit universal column driver for various displays of OLED and LCD," *J. Soc. Inf. Display*, vol. 24, no. 5, pp. 277–285, May 2016.

[28] C. Lu et al., "A 10-bit 1026-channel column driver IC with partially segmented piecewise linear digital-to-analog converters for UHD TFT-LCDs with one billion color display," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2703–2716, Oct. 2019.

[29] J. Na, S. Hong, and O. Kwon, "A highly linear 10-bit DAC of data driver IC using source degeneration load for active matrix flat-panel displays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 11, pp. 2312–2316, Nov. 2020.

[30] X. Guo and H. Li, "Gray code-based 10-bit source driver for large-size OLED display," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2307–2311, Jul. 2021.

[31] Y.-C. Sung, O.-K. Kwon, and J.-K. Kim, "10-bit source driver with resistor-resistor-string digital-to-analog converter," *J. Soc. Inf. Display*, vol. 14, no. 4, pp. 371–377, Apr. 2006.

[32] C. Lu, P. Yin, C. Hsiao, and M. F. Chang, "A 10 b resistor-resistor-string DAC with current compensation for compact LCD driver ICs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 318–320.

[33] C. Lu, P. Yin, C. Hsiao, M. F. Chang, and Y. Lin, "A 10-bit resistor-floating-resistor-string DAC (RFR-DAC) for high color-depth LCD driver ICs," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2454–2466, Oct. 2012.

[34] P. Yin, C. Lu, Y. Chen, H. Liang, and S. Tseng, "A 10-bit low-power high-color-depth column driver with two-stage multi-channel RDACs for small-format TFT-LCD driver ICs," *J. Display Technol.*, vol. 11, no. 12, pp. 1061–1068, Dec. 2015.

[35] J. Kim, J. Yoon, and B. Choi, "A low-area 10 b column driver with resistor-resistor-string DAC for mobile active-matrix LCDs," in *Proc. IEEE Asia Pacific Conf. Circuits Syst. (APCCAS)*, Oct. 2016, pp. 548–550.

[36] D. Jung et al., "A 12-bit multi-channel R-R DAC using a shared resistor string scheme for area-efficient display source driver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 3688–3697, Nov. 2018.

[37] C. Lu, P. Yin, and M. Lin, "A 10-bit two-stage R-DAC with isolating source followers for TFT-LCD and AMOLED column-driver ICs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 2, pp. 326–336, Feb. 2019.

[38] C.-W. Lu and L.-C. Huang, "A 10-bit LCD column driver with piecewise linear digital-to-analog converters," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 371–378, Feb. 2008.

[39] H. Kim, J. Yang, S. Park, S. Ryu, and G. Cho, "A 5.6 mV inter-channel DVO 10 b column-driver IC with mismatch-free switched-capacitor interpolation for mobile active-matrix LCDs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 392–393.

[40] H. Kim, J. Yang, S. Park, S. Ryu, and G. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[41] G. Kang et al., "A 12-bit mobile OLED/μLED display driver IC with cascaded loading-free capacitive interpolation DAC and 6.24 V/μs-slew-rate buffer amplifier," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[42] J. Kim, J. Yoon, and B. Choi, "A low-area and fully nonlinear 10-bit column driver with low-voltage DAC and switched-capacitor amplifier for active-matrix displays," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 488–500, Feb. 2021.

[43] G. Lim, G. Kang, H. Ma, M. Jeong, and H. Kim, "A 10 b source-driver IC with LSB-stacked LV-to-HV-amplify DAC achieving 2688 μm^2/channel and 4.8 mV DVO for mobile OLED displays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 110–112.

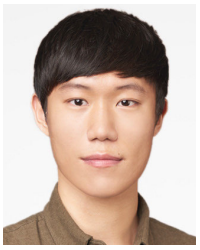
[44] H. Kano, T. Nosaka, K. Higuchi, A. Yusa, and A. Takahashi, "Development of 13 bit source driver/timing controller chip-set with RGB individual gamma control and evaluation report on the panel," in *SID Symp. Dig. Tech. Papers*, May 2008, pp. 1414–1417.

[45] H. Kim, S.-I. Chang, S. Youn, K. Foo, and T. Kim, "OLED display gamma LUT optimization based on principal component analysis," in *SID Symp. Dig. Tech. Papers*, Sep. 2020, pp. 463–466.

[46] J. Bae et al., "A small area 10-bit linear gamma DAC with voltage adder for large-sized active matrix flat panel displays," in *Proc. Int. Symp. Integr. Circuits (ISIC)*, Dec. 2014, pp. 496–499.

[47] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1231–1240, Aug. 1997.

[48] P. L. Lee et al., "A 10-bit 1280 $\times$ 720 micro-LED display driver with 2-transistor pixel circuits and current-mode pulse width modulation," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 134–137, 2022.



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