

RS14100 WiSeMCU™ Wi-Fi® and Dual-mode Bluetooth® 5 Wireless Secure MCU CA1/CC1 Modules

Overview

1.1 Features

Microcontroller

- ARM Cortex-M4F core with up to 180 MHz, 225 DMIPS performance
- Integrated FPU, MPU and NVIC
- SWD and JTAG debug options
- Internal and external oscillators with PLLs
- Flash In-Application Programming (IAP), In-System Programming (ISP) and Over-the-Air Wireless Firmware Upgrade
- Power-On Reset (POR), Brown-Out and Black-out Detect (BOD) with separate thresholds
- Support Multiple power domains to achieve lower current consumption

Memory

- Up to 4 MB integrated or external Quad-SPI flash with inline AES engine and XIP
- Up to 208 KB SRAM
- 64 KB ROM has boot code and software drivers
- 32 byte One-time programmable (eFuse) memory
- 4-way set-associative 16 KB I-Cache

Security

- HW device identity and key storage with PUF
- Trusted Execution Environment with Secure Boot loader
- Accelerators: AES128/256, SHA256/384/512, HMAC, RSA, ECC, ECDH, RNG, CRC
- Secure XIP from flash
- Secure boot loading performed by secure processor
- Secure firmware update
- Tamper detection with Hardware disable, Secure RTC, Secure Hardware Watchdog and other Secure Peripherals connected to the Trusted Execution Environment.
- Programmable Secure Hardware Write protect for Flash sectors

Digital Peripherals

- USB HS OTG with integrated HS transceiver



- 10/100 Mbps Ethernet MAC with RMII
- SD/SDIO MMC 3.0 card host, SDIO 2.0 slave
- 3x USART, 4x SPI, 3x I2C, 2x I2S, SIO, CAN 2.0B, PWM, QEI
- Timers: 5x 32-bit, 1x 16/32-bit, 1x 24-bit, WDT, RTC
- Up to 40 GPIOs with GPIO multiplexer
- FIM

Analog Peripherals

- 12-bit 16-ch, 5 Msps ADC, 10-bit DAC
- 3x Op-amps, 2x Comparators, IR detector and Temperature Sensor
- 8 capacitive touch sensor inputs
- Voice Activity Detection (VAD)

Wi-Fi

- Compliant to single-spatial stream IEEE 802.11 a/b/g/n with single band (2.4 GHz in **CA1** module) and dual band (2.4 and 5 GHz in **CC1** module) support
- Support for 20 MHz and 40 MHz channel bandwidths
- Transmit power up to +18dBm in 2 GHz and +13.5 dBm in 5 GHz
- Receive sensitivity as low as -96 dBm in 2 GHz and -89 dBm in 5 GHz
- Data Rates:- 802.11b:Upto11 Mbps ; 802.11g/a:Upto54 Mbps ; 802.11n: MCS0 to MCS7
- Operating Frequency Range:- 2412 MHz – 2484 MHz, 4.9 GHz – 5.975 GHz
- Application data throughput up to 40 Mbps in integrated-TCP/IP stack mode

Bluetooth

- Compliant to dual-mode Bluetooth 5
- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity:- LE: -95 dBm, LR 125 Kbps: -106 dBm

- <8 mA transmit current in BT 5 mode, 2 Mbps data rate
- Data rates: 125 kbps, 500 kbps, 1 Mbps, 2Mbps, 3 Mbps
- Operating Frequency Range:- 2.402 GHz - 2.480 GHz
- EDR+2.1, 4.0, 4.1, 4.2 and 5.0
- BT LE 1 Mbps, 2 Mbps and Long Range modes
- BLE Secure connections
- BLE supports 8 center roles and 2 peripheral roles concurrently.
- BT auto rate and auto TX power adaptation
- Piconet with Seven active logical links. Scatternet with two slave roles while still being visible.
- BT inbuilt stack support for L2CAP, AVDTP, AVCTP, RFCOMM, SDP, ATT, SMP
- BT profile support for SPP, A2DP, AVRCP, HFP, PBAP, IAP, GAP, GATT, IAP1, IAP2, HID

RF Features

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch
- Integrated Antenna and u.FL connector
- Diversity is supported

Embedded Wi-Fi Stack

- Support for Embedded Wi-Fi Client mode, Wi-Fi Access point mode, Wi-Fi Direct and Enterprise Security
- Supports advanced Wi-Fi security features: WPA/WPA2-Personal and Enterprise (EAP-TLS, EAP-FAST, EAP-TTLS, EAP-PEAP, EAP-LEAP, PEAP-MSCHAP-V2)
- Integrated TCP/IP stack (IPv4/IPv6), HTTP/HTTPS, DHCP, ICMP, SSL 3.0/TLS 1.2, Web sockets, IGMP, DNS, DNS-SD, SNMP, FTP Client
- Over-the-Air Wireless firmware upgrade and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Embedded Bluetooth Stack

- EDR+2.1, 4.0, 4.1, 4.2 and 5.0
- BT LE 1 Mbps, 2 Mbps and Long Range modes
- BLE Secure connections
- BLE supports 8 center roles and 2 peripheral roles concurrently.
- BT auto rate and auto TX power adaptation
- Piconet with Seven active logical links. Scatternet with two slave roles while still being visible.

- BT inbuilt stack support for L2CAP, AVDTP, AVCTP, RFCOMM, SDP, ATT, SMP
- BT profile support¹ for SPP, A2DP, AVRCP, HFP, PBAP, IAP, GAP, GATT, IAP1, IAP2, HID

MCU Sub-system Power Consumption

- Active current as low as 19uA/MHz in low power mode
- Active current as low as 65uA/MHz in high power mode
- Deep sleep mode current: ~450nA
- Dynamic Voltage & Frequency Scaling
- Deep sleep mode with only timer active – with and without RAM retention

Power States

- Reset State
- Active States
 - PS1
 - PS2
 - PS3
 - PS4
- Standby States
 - PS2-STANDBY
 - PS3-STANDBY
 - PS4-STANDBY
- Sleep States
 - PS2-SLEEP
 - PS3-SLEEP
 - PS4-SLEEP
- Shutdown States
 - PS0

Wireless Sub-system Power Consumption

- Wi-Fi Standby Associated mode current: 40uA @ 1-second beacon listen interval
- Wi-Fi 1 Mbps Listen current: 14mA
- Wi-Fi LP chain Rx current: 19mA
- Deep sleep current <1uA, Standby current (RAM retention) < 10uA

Software and Regulatory Certification

- Wi-Fi Alliance¹
- Bluetooth Qualification¹
- FIPS 140-2 Certification¹
- Regulatory certifications support (FCC, IC, CE/ETSI, TELEC)¹

Operating Conditions

- Wide operating supply range: 1.75 V to 3.63 V
- Operating temperature: -40°C to +85°C (Industrial grade)

Evaluation Kit

- WiSeMCU Single Band EVK: RS14100-SB-EVK1

- WiSeMCU Dual Band EVK: RS14100-DB-EVK1

Development Environment

- Redpine SmartStudio™ unified development platform

¹Contact Redpine for availability and options.

1.2 Applications

- Internet of Things (IoT)
- Multimedia
- Consumer Electronics
- Home Appliances and White Goods
- Industrial IoT
- Home Automation
- Smart Gateway and Metering
- Smart locks
- Security Camera/Video Doorbells
- Wireless audio applications
- Asset tracking
- Medical and Healthcare
- Thermostats
- Wearables
- Drone
- Point-of-Sale
- Audio Headset

1.3 Description

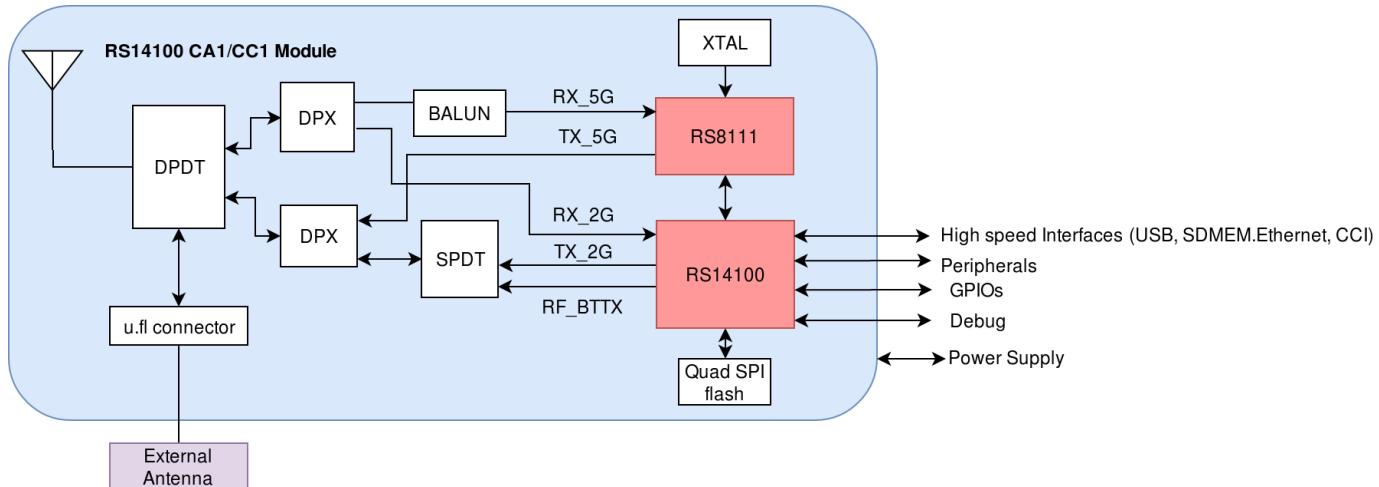
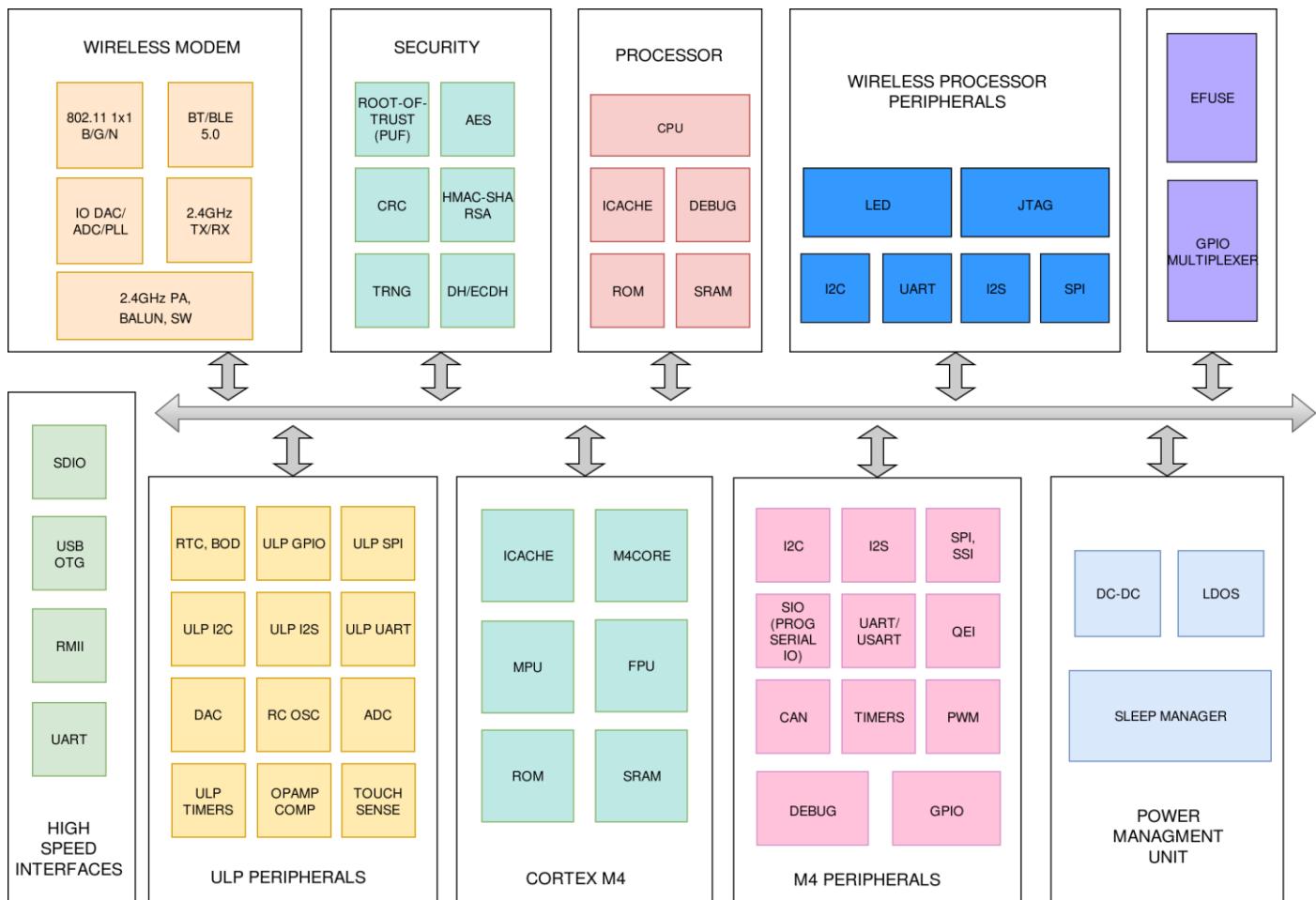
Redpine Signals' RS14100 single band CA1 modules and dual band CC1 modules are Wireless Secure MCUs with a comprehensive multi-protocol wireless sub-system. It has an integrated ultra-low-power microcontroller, a built-in wireless subsystem, advanced security, high performance mixed-signal peripherals and integrated power-management. An ARM Cortex-M4F running up to 180MHz and Redpine's ThreadArch® 4-Threaded processor running up to 160MHz. The Cortex-M4F is dedicated for peripheral and application related processing whereas all the networking and wireless stacks run on independent threads of the ThreadArch®. The wireless subsystem has low-cost CMOS integration of a multi-threaded MAC processor (ThreadArch®), baseband digital signal processing, analog front-end, calibration eFuse, 2.4GHz RF transceiver and integrated power amplifier thus providing a fully-integrated solution for a range of embedded wireless applications. The modules are FCC, IC, and ETSI/CE certified.

Part Number	Wireless	CPU Freq	Flash+RAM	GPIOs
RS14100-SB00-140F-CA1	SBW+BT5	100 MHz	4 MB+208 KB	40
RS14100-SB00-240F-CA1	SBW+BT5	180 MHz	4 MB+208 KB	40
RS14100-DB00-140F-	DBW+BT5	100 MHz	4 MB+208 KB	40

Part Number	Wireless	CPU Freq	Flash+RAM	GPIOs
CC1				
RS14100-DB00-240F-CC1	DBW+BT5	180 MHz	4 MB+208 KB	40

Table 1 Device Information

1.4 Block Diagrams

**Figure 1 CA1/CC1 Module Block Diagram****Figure 2 RS14100 Hardware Block Diagram**

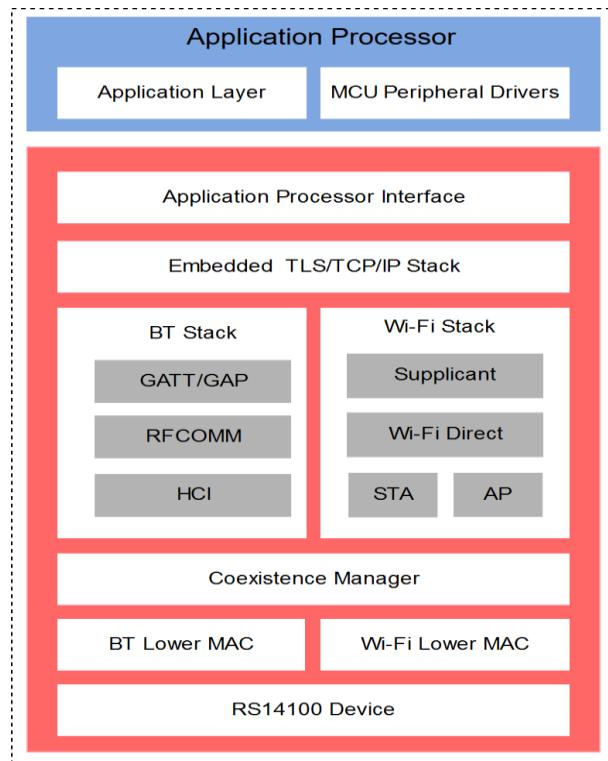


Figure 3 RS14100 Software Block Diagram

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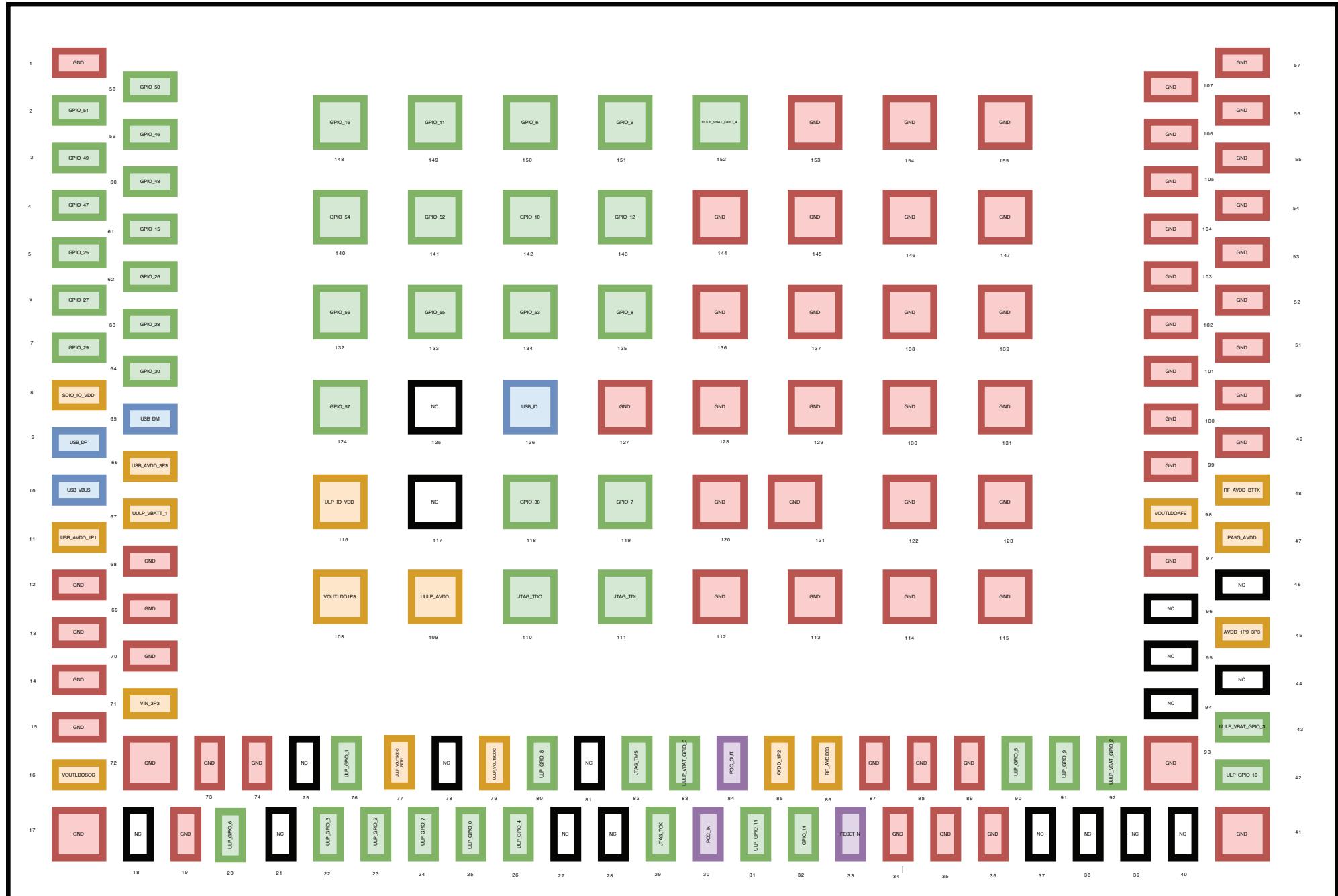
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2 RS14100 CA1/CC1 module Pinout and Pin Description

2.1 Pin Diagram



10

Power Supplies

1

Host

1

GPIO & Peripherals

Grounds

NC

1

Host RF & Control

1

GPIO & Peripherals Miscellaneous

2.2 Pin Description

2.2.1 RF & Control Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RESET_N	33	UULP_VBATT_1	Input	NA	Active-low reset asynchronous reset signal
POC_IN	30	UULP_VBATT_1	Input	NA	Power On Control Input
POC_OUT	84	UULP_VBATT_1	Output	NA	Power On Control Output

Table 2 RF & Control Interfaces

2.2.2 Power & Ground Pins

Pin Name	Type	Pin Number	Direction	Description
UULP_VBATT_1	Power	67	Input	Always-on VBATT Power supply to the UULP domains
VIN_3P3	Power	71	Input	Digital Power Supply
VOUTLDOSOC	Power	16	Output	Output of SoC LDO
VOUTLDO1P8	Power	108	Output	Output of 1.8V LDO
VOUTLDOAFE	Power	98	Output	Output of AFE LDO
SDIO_IO_VDD	Power	8	Input	I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
ULP_IO_VDD	Power	116	Input	I/O Supply for ULP GPIOs
PA5G_AVDD	Power	47	Input	Power supply for the 5 GHz RF Power Amplifier
RF_AVDD_BTTX	Power	48	Input	Power supply for Bluetooth Transmit circuit. Connect to VOUTLDOAFE as per the Reference Schematics.
RF_AVDD33	Power	86	Input	Power supply for the 5 GHz RF
AVDD_1P9_3P3	Power	45	Input	Power supply for the 5 GHz RF
AVDD_1P2	Power	85	Input	Power supply for the 5 GHz RF. Connect to VOUTLDOSOC as per the

Pin Name	Type	Pin Number	Direction	Description
				Reference Schematics.
UULP_VOUTSCDC	Power	79	Output	UULP Switched Cap DCDC Output
UULP_VOUTSCDC_RETN	Power	77	Output	UULP Retention Supply Output
UULP_AVDD	Power	109	Input	Power supply for the always-on digital and ULP peripherals. Connect to UULP_VOUTSCDC as per the Reference Schematics.
USB_AVDD_3P3	Power	66	Input	Power Supply for the USB interface
USB_AVDD_1P1	Power	11	Input	Power supply for the USB core
GND	Ground	1, 12, 13, 14, 15, 17, 19, 34, 35, 36, 41, 49, 50, 51, 52, 53, 54, 55, 56, 57, 68, 69, 70, 72, 73, 74, 87, 88, 89, 93, 97, 99, 100, 101, 102, 103, 104, 105, 106, 107, 112, 113, 114, 115, 120, 121, 122, 123, 127, 128, 129, 130, 131, 136, 137, 138, 139, 144, 145, 146, 147, 153, 154, 155	GND	Common ground pins

Table 3 Power and Ground Pins

2.2.3 Peripheral Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
GPIO_6	150	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_7	119	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					configuration.
GPIO_8	135	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_9	151	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_10	142	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_11	149	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_12	143	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_14	32	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_15	61	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					Refer to GPIO Muxing Tables for configuration.
GPIO_16	148	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_25	5	SDIO_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_26	62	SDIO_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_27	6	SDIO_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_28	63	SDIO_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_29	7	SDIO_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_30	64	SDIO_IO_VDD	Inout	Pullup	Default: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_38	118	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_46	59	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_47	4	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_48	60	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_49	3	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_50	58	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
GPIO_51	2	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_52	141	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_53	134	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_54	140	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_55	133	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_56	132	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
GPIO_57	124	VIN_3P3	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					configuration.
ULP_GPIO_0	25	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_1	76	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_2	23	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_3	22	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_4	26	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_5	90	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_6	20	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_7	24	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_8	80	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_9	91	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_10	42	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
ULP_GPIO_11	31	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
UULP_VBAT_GPIO_0	83	UULP_VBATT_1	Output	High	Default : EXT_PG_EN Sleep: EXT_PG_EN Refer to GPIO Muxing Tables for configuration.
UULP_VBAT_GPIO_2	92	UULP_VBATT_1	Inout	HighZ	Default: HighZ Sleep: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					Refer to GPIO Muxing Tables for configuration.
UULP_VBAT_GPIO_3	43	UULP_VBATT_1	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
UULP_VBAT_GPIO_4	152	UULP_VBATT_1	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to GPIO Muxing Tables for configuration.
JTAG_TCK	29	VIN_3P3	Input	Pullup	JTAG interface clock.
JTAG_TDI	111	VIN_3P3	Input	Pullup	JTAG interface input data.
JTAG_TMS	82	VIN_3P3	Input	Pullup	JTAG interface Test Mode Select signal. Bi-directional data pin for SWD Interface.
JTAG_TDO	110	VIN_3P3	Output	Pullup	JTAG interface output data. Serial wire output for SWD Interface. This pin can also be used as ISP_ENABLE. Pull down to enable ISP mode. In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART, SPI and SDIO interfaces. This can be done after the part is integrated on end user board. Boot loader can be requested to boot in ISP mode by pulling down a specific GPIO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes uses JTAG pins for functional use. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description ^{1,2,3}
					gain the control and to reprogram the flash.
USB_VBUS	10	USB_AVDD_3P3	Input	NA	5V USB VBUS signal from the USB connector.
USB_DP	9	USB_AVDD_3P3	Inout	NA	Positive data channel from the USB connector.
USB_DM	65	USB_AVDD_3P3	Inout	NA	Negative data channel from the USB connector.
USB_ID	126	USB_AVDD_3P3	Input	NA	ID signal from the USB connector.

Table 4 Peripheral Interfaces

1. "Default" state refers to the state of the device after initial boot loading and firmware loading is complete.
2. "Sleep" state refers to the state of the device after entering Sleep state.
3. Please refer to "**RS14100 Hardware Reference Manual**" for software programming information.

2.2.4 Miscellaneous Pins

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
NC	18, 21, 27, 28, 37, 38, 39, 40, 44, 46, 75, 78, 81, 94, 95, 96, 117, 125	NA	NA	NA	No connect.

Table 5 Miscellaneous Pins

2.3 GPIO Pin Multiplexing

Available GPIO's

1. The possible GPIO combinations for each Peripheral Interface are listed in "**Valid GPIO sets for peripherals**" section below
2. GPIO_64 to GPIO_75 and ULP_GPIO_16 to ULP_GPIO_29 are virtual GPIO's and can be mapped onto the physical GPIO's. Refer to "**Digital Functions**" Section for peripheral mapping on these GPIO's.

2.3.1 SoC GPIO's

The SoC GPIOs below (GPIO_6 to GPIO_57) are available in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in SoC GPIO's section of the Hardware Reference Manual.

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 14	GPIO Mode = 15
GPIO_6	GPIO	SIO_0	UART2_TX	SSI_MST_D ATA0	I2C1_SDA	I2S_2CH_D OUT_0	SCT_OUT_0	QEI_IDX	SMIH_CD_N		MCU_QSPI_CLK	RMII_TXD1	NWP_GPIO_6
GPIO_7	GPIO	SIO_1	UART2_RX	SSI_MST_D ATA1	I2C1_SCL	I2S_2CH_CL K	SCT_OUT_1	QEI_PHB	SMIH_WP	SCT_OUT_1	MCU_QSPI_CSNO	RMII_TXD0	
GPIO_8	GPIO	SIO_2	USART1_RX	SSI_MST_CL K			SCT_OUT_2	QEI_PHA	PWM_1L		MCU_QSPI_D0	RMII_REF_C_LK	NWP_GPIO_8
GPIO_9	GPIO	SIO_3	USART1_TX	SSI_MST_CS 0		SDMEM_PR ESENT	SCT_OUT_3	QEI_DIR	PWM_1H		MCU_QSPI_D1	RMII_TXEN	NWP_GPIO_9
GPIO_10	GPIO	USART1_IR_TX	USART1_CL K	SSI_MST_CS 1	I2C2_SCL	I2S_2CH_DI N_0	SCT_OUT_4	RMII_RXD1	PWM_2H		MCU_QSPI_D2	SSI_SLV_CS	NWP_GPIO_10
GPIO_11	GPIO	SIO_5	USB_DRVV_BUS	SSI_MST_CL K	I2C2_SDA	I2S_2CH_W S	SCT_OUT_5	RMII_MDC	PWM_2L		MCU_QSPI_D3	SSI_SLV_CL K	NWP_GPIO_11

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 14	GPIO Mode = 15
GPIO_12	GPIO	USART1_IR_RX	UART2_TX	SSI_MST_D ATA0	I2C1_SCL	USART1_RT_S	SCT_OUT_6	RMII_MDO	SCT_IN_0		MCU_CLK_O_UT	SSI_SLV_MI_SO	NWP_GPIO_12
GPIO_14	GPIO	ULP_GPIO_7	USART1_RX	GSPI_MST1_MISO	SCT_IN_2	USB_DRVV_BUS	SCT_OUT_0	RMII_CRS_D_V					
GPIO_15	GPIO	MCU_CLK_O_UT	UART2_RX	SSI_MST_D ATA1	I2C1_SDA	USART1_CT_S	SCT_OUT_7	RMII_RXD0	GSPI_MST1_CLK			SSI_SLV_MO_SI	NWP_GPIO_15
GPIO_16	GPIO	SIO_4	USB_DRVV_BUS	SSI_MST_CS0	CAN1_RXD	GSPI_MST1_CS0	I2S_2CH_W_S	XTAL_ON_IN	SSI_SLV_CS		ULP_GPIO_17	RMII_CRS_D_V	
GPIO_25	GPIO	SIO_4	USART1_CL_K	SSI_MST_CL_K	I2C1_SCL	RMII_TXD1	SCT_IN_2	SCT_OUT_0	SMIH_CLK	UART2_TX		AGPIO_18	
GPIO_26	GPIO	SIO_5	USART1_TX	SSI_MST_D ATA0	I2C1_SDA	RMII_TXD0	SCT_IN_3	SCT_OUT_1	SMIH_CMD	UART2_RX		AGPIO_19	
GPIO_27	GPIO	SIO_6	USART1_RX	SSI_MST_D ATA1	GSPI_MST1_CS0	I2S_2CH_W_S	SCT_IN_4	USART1_RT_S	SMIH_D0	SSI_SLV_CS	QEI_IDX	AGPIO_20	
GPIO_28	GPIO	SIO_7	USART1_CL_K	SSI_MST_CS0	GSPI_MST1_CLK	I2S_2CH_CL_K	I2C2_SCL	USART1_CT_S	SMIH_D1	SSI_SLV_CL_K	QEI_PHB	AGPIO_21	
GPIO_29	GPIO	CAN1_RXD	USART1_RX	SSI_MST_CS1	GSPI_MST1_MISO	I2S_2CH_DI_N_0	I2C2_SDA	SCT_OUT_2	SMIH_D2	SSI_SLV_MO_SI	QEI_PHA	AGPIO_22	
GPIO_30	GPIO	CAN1_TXD	USART1_TX	SSI_MST_CS2	GSPI_MST1_MOSI	I2S_2CH_D_OUT_0	RMII_TXEN	SCT_OUT_4	SMIH_D3	SSI_SLV_MI_SO	QEI_DIR	AGPIO_23	
GPIO_38	GPIO	REF_CLK_O_UT	UART2_CTS	SDMEM_PRESENT			ULP_GPIO_28		PWM_3L		PWM_TMR_EXT_TRIGGER_1		
GPIO_46	GPIO	CAN1_RXD	UART2_RX	ULP_GPIO_28	GSPI_MST1_CS3	USART1_DS_R	SCT_OUT_2	I2S_2CH_DI_N_1	SMIH_CLK		MCU_QSPI_CLK		
GPIO_47	GPIO	CAN1_TXD	UART2_TX	SSI_MST_CS3	GSPI_MST1_CS2	USART1_DC_D	SCT_OUT_3	I2S_2CH_D_OUT_1	SMIH_CMD		MCU_QSPI_D0		
GPIO_48	GPIO	SIO_0	ULP_GPIO_	SSI_MST_CS	UART2_RS4	USART1_DT	SCT_OUT_4	I2S_2CH_W	SMIH_D0		MCU_QSPI_		

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 14	GPIO Mode = 15
			16	2	85_EN	R		S			D1		
GPIO_49	GPIO	SIO_1	ULP_GPIO_17	UART2_RTS	GSPI_MST1_CS1	I2S_2CH_CLK	SCT_OUT_5	RMII_TXD1	SMIH_D1		MCU_QSPI_CSN0		
GPIO_50	GPIO	SIO_2	ULP_GPIO_18	UART2_CTS	UART2_RS4_85_RE	I2C1_SCL	SCT_OUT_0	RMII_TXD0	SMIH_D2		MCU_QSPI_D2		
GPIO_51	GPIO	SIO_3	ULP_GPIO_19	USB_XTAL_ON	UART2_RS4_85_DE	I2C1_SDA	SCT_OUT_1	RMII_TXEN	SMIH_D3		MCU_QSPI_D3		
GPIO_52	GPIO	SIO_4	MCU_QSPI_CLK	TRACE_CLK_IN	ULP_GPIO_29	USART1_RI	SCT_OUT_7	RMII_RXD1	SMIH_WP		MCU_QSPI_DQS		
GPIO_53	GPIO	SIO_5	MCU_QSPI_CSN0	TRACE_CLK		USART1_IR_RX	SCT_IN_3	RMII_MDC	SMIH_CD_N		MCU_QSPI_CSN1		
GPIO_54	GPIO	SIO_6	MCU_QSPI_D0	TRACE_D0		USART1_IR_TX	ULP_GPIO_20	RMII_MDO	SMIH_D4		MCU_QSPI_D4		
GPIO_55	GPIO	SIO_7	MCU_QSPI_D1	TRACE_D1		USART1_RS485_EN	ULP_GPIO_21	RMII_REF_C_LK	SMIH_D5		MCU_QSPI_D5		
GPIO_56	GPIO		MCU_QSPI_D2	TRACE_D2		USART1_RS485_RE	ULP_GPIO_22	RMII_CRS_D_V	SMIH_D6		MCU_QSPI_D6		
GPIO_57	GPIO		MCU_QSPI_D3	TRACE_D3		USART1_RS485_DE	ULP_GPIO_23	RMII_RXD0	SMIH_D7		MCU_QSPI_D7		

Table 6 SoC GPIO Pin Multiplexing

1. GPIO's 25 to 30 can be used for Analog functions when GPIO Mode = 14. Multiple Analog functions are available on each pin as shown in the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Hardware Reference Manual for more details.
2. GPIO's 6 to 15 can be used for Network Processor functions when GPIO Mode = 15. The NWP functions available on these GPIO's is shown in the below NWP functions Pin Multiplexing Table.

2.3.2 ULP GPIO's

The ULP GPIOs listed in the table below (ULP_GPIO_0 to ULP_GPIO_11) are available in the normal mode of operation (Power-states 4 and 3) and also in Ultra-low power mode of operation of the Microcontroller (Power-states 2 and 1). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Hardware Reference Manual.

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7
ULP_GPIO_0	GPIO	ULP_SPI_CLK	ULP_I2S_DIN	ULP_UART_RTS	ULP_I2C_SDA		GPIO_64	AGPIO_0
ULP_GPIO_1	GPIO	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	Timer0	GPIO_65	AGPIO_1
ULP_GPIO_2	GPIO	ULP_SPI_DIN	ULP_I2S_WS	ULP_UART_RX	ULP_SPI_CS1	COMP1_OUT	GPIO_66	AGPIO_2
ULP_GPIO_3	GPIO	ULP_SPI_CS0	ULP_I2S_CLK	ULP_UART_TX	ULP_SPI_DIN		GPIO_67	AGPIO_3
ULP_GPIO_4	GPIO	ULP_SPI_CS1	ULP_I2S_WS	ULP_UART_RTS	ULP_I2C_SDA		GPIO_68	AGPIO_4
ULP_GPIO_5	GPIO	IR_PG_EN	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL		GPIO_69	AGPIO_5
ULP_GPIO_6	GPIO	ULP_SPI_CS2	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA		GPIO_70	AGPIO_6
ULP_GPIO_7	GPIO	IR_INPUT	ULP_I2S_CLK	ULP_UART_TX	ULP_I2C_SCL	Timer1	GPIO_71	AGPIO_7
ULP_GPIO_8	GPIO	ULP_SPI_CLK	ULP_I2S_CLK	ULP_UART_CTS	ULP_I2C_SCL	Timer0	GPIO_72	AGPIO_8
ULP_GPIO_9	GPIO	ULP_SPI_DIN	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA	COMP1_OUT	GPIO_73	AGPIO_9
ULP_GPIO_10	GPIO	ULP_SPI_CS0	ULP_I2S_WS	ULP_UART_RTS	IR_INPUT	UULP_VBAT_GPIO_4	GPIO_74	AGPIO_10
ULP_GPIO_11	GPIO	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_TX	ULP_I2C_SDA		GPIO_75	AGPIO_11

Table 7 ULP GPIO Pin Multiplexing

1. All the ULP GPIOs can be used for Analog functions when ULP GPIO Mode = 7. Multiple Analog functions are available on each pin as shown in

the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Hardware Reference Manual for more details.

2. All the ULP GPIO's can be used for Digital functions when ULP GPIO Mode = 6. The digital functions available on these GPIOs is shown in the below Digital Pin Multiplexing Table.

2.3.3 UULP VBAT GPIO's

The UULP VBAT GPIOs listed in the table below (UULP_VBAT_GPIO_0 to UULP_VBAT_GPIO_4) are available in the normal mode of operation (Power-states 4 and 3), in Ultra-low power mode of operation (Power-states 2 and 1) and also in the retention and deep sleep mode of operation (Retention and Power-state 0). For a description of power-states, refer to the Hardware Reference Manual. Each of this UULP VBAT GPIO's Pin function is controlled by the GPIO Mode register mentioned in UULP VBAT GPIO's section of the Hardware Reference Manual.

UULP VBAT GPIO	UULP VBAT GPIO Mode = 0	UULP VBAT GPIO Mode = 1	UULP VBAT GPIO Mode = 2	UULP VBAT GPIO Mode = 3	UULP VBAT GPIO Mode = 4	UULP VBAT GPIO Mode = 5	UULP VBAT GPIO Mode = 6	UULP VBAT GPIO Mode = 7	Default
UULP_VBAT_GPI 0_0	GPIO	EXT_PG_EN							EXT_PG_EN
UULP_VBAT_GPI 0_2	GPIO		MCU_GPIO2_WA KEUP		XTAL_32KHZ_IN			VOLT_SENSE	MCU_GPIO2_WA KEUP
UULP_VBAT_GPI 0_3	GPIO		MCU_GPIO3_WA KEUP			XTAL_32KHZ_IN		COMP_P	GPIO
UULP_VBAT_GPI 0_4	GPIO		MCU_GPIO4_WA KEUP				XTAL_32KHZ_IN	COMP_N	GPIO

Table 8 UULP VBAT GPIO Pin Multiplexing

2.3.4 NWP Functions

GPIO	Function
NWP_GPIO_6	LED
NWP_GPIO_8	UART1_RX

NWP_GPIO_9	UART1_TX
NWP_GPIO_10	WLAN_ACTIVE
NWP_GPIO_11	BT_ACTIVE
NWP_GPIO_12	BT_PRIORITY
NWP_GPIO_15	UART2_TX

Table 9 NWP Functions for SoC GPIOs

1. Software can program above different functions.
2. Please refer to "**RS14100 Wireless SAPI Manual**" for software programming information.

2.3.5 Analog Functions

GPIO	ADC Function	Touch Function	DAC Function	Comparator Function	OpAmp Function
AGPIO_0	ADCP0	TOUCH6		COMPA_P0	OPAMP1P2
AGPIO_1	ADCP10 / ADCN0			COMPA_N0	
AGPIO_2	ADCP1			COMPB_P0	OPAMP1P3
AGPIO_3	ADCP11 / ADCN1	TOUCH5		COMPB_N0	
AGPIO_4	ADCP2	C_int_res_in	DAC0	COMPA_N1	OPAMP1OUT0
AGPIO_5	ADCP12 / ADCN2	res_out		COMPA_P1	OPAMP2P1
AGPIO_6	ADCP3	TOUCH4			OPAMP1P4
AGPIO_7	ADCP15 / ADCN5	TOUCH3			OPAMP1P1 / OPAMP1N1
AGPIO_8	ADCP4	TOUCH0 / C_int_res_in			OPAMP1P5
AGPIO_9	ADCP14 / ADCN4	TOUCH1			OPAMP2OUT0

GPIO	ADC Function	Touch Function	DAC Function	Comparator Function	OpAmp Function
AGPIO_10	ADCP5	TOUCH2 / res_out			OPAMP3P0 / OPAMP3N0
AGPIO_11	ADCP13 / ADCN3	TOUCH7			OPAMP2P0 / OPAMP2N0
AGPIO_18	ADCP7				
AGPIO_19	ADCP17 / ADCN7				
AGPIO_20	ADCP8	TOUCH_VREF_EXT			OPAMP3OUT0
AGPIO_21	ADCP18 / ADCN8				
AGPIO_22	ADCP9				
AGPIO_23	ADCP19 / ADCN9				

Table 10 Analog Functions for SoC/ULP GPIOs

1. Software can program above different functions.
2. Please refer to "**Hardware Reference Manual**" for software programming information.

2.3.6 Digital Functions

The SoC GPIOs below (GPIO_64 to GPIO_75) are available in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in SoC GPIO's section of the Hardware Reference Manual.

GPIO	GPIO Mode = 0	GPIO Mode = 1	GPIO Mode = 2	GPIO Mode = 3	GPIO Mode = 4	GPIO Mode = 5	GPIO Mode = 6	GPIO Mode = 7	GPIO Mode = 8	GPIO Mode = 9	GPIO Mode = 10	GPIO Mode = 14
GPIO_64	GPIO	SIO_0	SCT_IN_0	SCT_OUT_4	SSI_MST_CS1	GSPI_MST1_CS2	UART2_RX	QEI_IDX	PWM_TMR_EXT_TRIGGER_1_A	PWM_FAULT		
GPIO_65	GPIO	SIO_1	SCT_IN_1	SCT_OUT_5	SSI_MST_CS2	GSPI_MST1_CS3	UART2_TX	QEI_PHA	PWM_TMR_EXT_TRIGGER_2_B	PWM_FAULT		
GPIO_66	GPIO	SIO_2	SCT_IN_2	SCT_OUT_6	UART2_CTS	I2C2_SCL	PWM_1L	QEI_PHB	PWM_TMR_USB_DRVVB			

										EXT_TRIGGER_3	US			
GPIO_67	GPIO	SIO_3	SCT_IN_3	SCT_OUT_7	UART2_RTS	I2C2_SDA	PWM_1H	QEI_DIR	PWM_TMR_EXT_TRIGGER_4	USB_XTAL_0N				
GPIO_68	GPIO	UART2_RX	USART1_CTS	SSI_MST_CLK	CAN1_RXD	SIO_0	SCT_OUT_0	I2C1_SCL	PWM_1H	PMU_TEST_1	I2S_2CH_CLK			
GPIO_69	GPIO	UART2_TX	USART1_RS485_DE	SSI_MST_DATA0	CAN1_TXD	SIO_1	SCT_OUT_1	I2C1_SDA	PWM_1L	PWM_SLP_EVENT_TRIGGER	I2S_2CH_WS			
GPIO_70	GPIO	UART2_CTS	USART1_RS485_EN	SSI_MST_CS1	PMU_TEST_2	SIO_2	SCT_OUT_2	I2C2_SCL	PWM_2L	PWM_TMR_EXT_TRIGGER_1	I2S_2CH_DIN_0			
GPIO_71	GPIO	UART2_RTS	USART1_RS485_RE	SSI_MST_DATA1	GSPI_MST1_CS1	SIO_3	SCT_OUT_3	I2C2_SDA	PWM_2H	PWM_TMR_EXT_TRIGGER_2	I2S_2CH_DOUT_0			
GPIO_72	GPIO	UART2_RX	USART1_CLK	SSI_MST_CLK	GSPI_MST1_CLK	I2S_2CH_CLK	SCT_OUT_4	I2C1_SCL	PWM_3L	SSI_SLV_CLK	USART1_CTS			
GPIO_73	GPIO	UART2_TX	USART1_RTS	SSI_MST_CS0	GSPI_MST1_CS0	I2S_2CH_WS	SCT_OUT_5	I2C1_SDA	PWM_3H	SSI_SLV_CS	XTAL_ON_IN			
GPIO_74	GPIO	CAN1_RXD	USART1_RX	SSI_MST_DA0	GSPI_MST1_MISO	I2S_2CH_DIN_0	SCT_IN_4	I2C2_SCL	PWM_4L	SSI_SLV_MO_SI	SCT_OUT_6			
GPIO_75	GPIO	CAN1_TXD	USART1_TX	SSI_MST_DA1	GSPI_MST1_MOSI	I2S_2CH_DOUT_0	SCT_IN_5	I2C2_SDA	PWM_4H	SSI_SLV_MISO	SCT_OUT_7			

Table 11 Digital Functions for ULP GPIOs

The ULP GPIOs below (ULP_GPIO_16 to ULP_GPIO_29) are available in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Hardware Reference Manual. Each of these GPIO's Pin function is controlled by the GPIO Mode register mentioned in ULP GPIO's section of the Hardware Reference Manual.

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7
ULP_GPIO_16	GPIO	ULP_SPI_CLK	ULP_I2S_DIN	ULP_UART_RTS	ULP_I2C_SDA			
ULP_GPIO_17	GPIO	ULP_SPI_DOUT	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL	Timer0		
ULP_GPIO_18	GPIO	ULP_SPI_DIN	ULP_I2S_WS	ULP_UART_RX	ULP_SPI_CS1	COMP1_OUT		
ULP_GPIO_19	GPIO	ULP_SPI_CS0	ULP_I2S_CLK	ULP_UART_TX	ULP_SPI_DIN			
ULP_GPIO_20	GPIO	ULP_SPI_CS1	ULP_I2S_WS	ULP_UART_RTS	ULP_I2C_SDA			

ULP_GPIO	ULP GPIO Mode = 0	ULP GPIO Mode = 1	ULP GPIO Mode = 2	ULP GPIO Mode = 3	ULP GPIO Mode = 4	ULP GPIO Mode = 5	ULP GPIO Mode = 6	ULP GPIO Mode = 7
ULP_GPIO_21	GPIO	IR_PG_EN	ULP_I2S_DOUT	ULP_UART_CTS	ULP_I2C_SCL			
ULP_GPIO_22	GPIO	ULP_SPI_CS2	ULP_I2S_DIN	ULP_UART_RX	ULP_I2C_SDA			
ULP_GPIO_23	GPIO	IR_INPUT	ULP_I2S_CLK	ULP_UART_TX	ULP_I2C_SCL	Timer1		
ULP_GPIO_28	GPIO	ULP_SPI_CS1	ULP_I2S_CLK		ULP_I2C_SDA			
ULP_GPIO_29	GPIO	ULP_SPI_CS2	ULP_I2S_DIN	COMP2_OUT	ULP_I2C_SCL	Timer1		

Table 12 ULP GPIO Pin Multiplexing

2.4 Valid GPIO sets for peripherals

Functions can be split pin wise across all GPIO's except for below restrictions. For synchronous interfaces there are some restrictions on clubbing of GPIO's into synchronous buses to ensure the timings mentioned in section **RS14100 SoC Specifications**. For example single synchronous interface cannot be split across ULP & SOC gpio's. Below table will provide all possible pin combinations for all Functions. For GPIO mode related information refer to above Pin Multiplexing tables.

ULP SSI (Synchronous Serial Interface) Master		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
ULP_SPI_CLK	ULP_GPIO_0 / ULP_GPIO_8	GPIO_48
ULP_SPI_CS0	ULP_GPIO_3 / ULP_GPIO_10	GPIO_51
ULP_SPI_CS1	ULP_GPIO_2 / ULP_GPIO_4	GPIO_38 / GPIO_46 / GPIO_50 / GPIO_54
ULP_SPI_CS2	ULP_GPIO_6	GPIO_52 / GPIO_56
ULP_SPI_DIN	ULP_GPIO_2 / ULP_GPIO_3 / ULP_GPIO_9	GPIO_50 / GPIO_51
ULP_SPI_DOUT	ULP_GPIO_1 / ULP_GPIO_11	GPIO_15 / GPIO_49
ULP I2S Master/Slave		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
ULP_I2S_CLK	ULP_GPIO_3 / ULP_GPIO_7 / ULP_GPIO_8	GPIO_14 / GPIO_38 / GPIO_46 / GPIO_51 / GPIO_57

ULP_I2S_WS	ULP_GPIO_2 / ULP_GPIO_4 / ULP_GPIO_10	GPIO_50 / GPIO_54
ULP_I2S_DIN	ULP_GPIO_0 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_48 / GPIO_52 / GPIO_56
ULP_I2S_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_16 / GPIO_49 / GPIO_55
ULP I2C INTERFACE		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
ULP_I2C_SCL	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_7 / ULP_GPIO_8	GPIO_14 / GPIO_16 / GPIO_49 / GPIO_52 / GPIO_55 / GPIO_57
ULP_I2C_SDA	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_6 / ULP_GPIO_9 / ULP_GPIO_11	GPIO_38 / GPIO_46 / GPIO_48 / GPIO_54 / GPIO_56
ULP UART INTERFACE		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
ULP_UART_TX	ULP_GPIO_3 / ULP_GPIO_7 / ULP_GPIO_11	GPIO_14 / GPIO_51 / GPIO_57
ULP_UART_RX	ULP_GPIO_2 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_50 / GPIO_56
ULP_UART_CTS	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_8	GPIO_16 / GPIO_49 / GPIO_55
ULP_UART_RTS	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_10	GPIO_48 / GPIO_54
IR Interface		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
IR_INPUT	ULP_GPIO_7 / ULP_GPIO_10 /	GPIO_57
IR_PG_EN	ULP_GPIO_5	GPIO_55
Timer Interrupt Interface		
IO Functionality	Combinations possible on ULP GPIO's	Combinations possible on SoC GPIO's
Timer0	ULP_GPIO_1 / ULP_GPIO_8	GPIO_16 / GPIO_49
Timer1	ULP_GPIO_7	GPIO_52 / GPIO_57
MCU SSI (Synchronous Serial Interface) Master		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's

SSI_MST_CLK	GPIO_8 / GPIO_11 / GPIO_25	ULP_GPIO_4 / ULP_GPIO_8
SSI_MST_CS0	GPIO_9 / GPIO_16 / GPIO_28	ULP_GPIO_9
SSI_MST_CS1	GPIO_10 / GPIO_29	ULP_GPIO_0 / ULP_GPIO_6
SSI_MST_CS2	GPIO_30 / GPIO_48	ULP_GPIO_1
SSI_MST_CS3	GPIO_47	
SSI_MST_DATA0	GPIO_6 / GPIO_12 / GPIO_26	ULP_GPIO_10 / ULP_GPIO_5
SSI_MST_DATA1	GPIO_7 / GPIO_15 / GPIO_27	ULP_GPIO_7 / ULP_GPIO_11

MCU SSI (Synchronous Serial Interface) Slave

IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
SSI_SLV_CLK	GPIO_11 / GPIO_28	ULP_GPIO_8
SSI_SLV_CS	GPIO_10 / GPIO_16 / GPIO_27	ULP_GPIO_9
SSI_SLV_MISO	GPIO_12 / GPIO_30	ULP_GPIO_11
SSI_SLV_MOSI	GPIO_15 / GPIO_29	ULP_GPIO_10

GSPI (General SPI) Interface

IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
GSPI_MST1_CLK	GPIO_15 / GPIO_28	ULP_GPIO_8
GSPI_MST1_CS0	GPIO_16 / GPIO_27	ULP_GPIO_9
GSPI_MST1_CS1	GPIO_49	ULP_GPIO_7
GSPI_MST1_CS2	GPIO_47	ULP_GPIO_0
GSPI_MST1_CS3	GPIO_46	ULP_GPIO_1
GSPI_MST1_MISO	GPIO_14 / GPIO_29	ULP_GPIO_10
GSPI_MST1_MOSI	GPIO_30	ULP_GPIO_11

SMIH (SD/SDIO/MMC Host Controller) Interface

IO Functionality	Combinations possible on SoC GPIO's

SMIH_CLK	GPIO_25 / GPIO_46
SMIH_CMD	GPIO_26 / GPIO_47
SMIH_D0	GPIO_27 / GPIO_48
SMIH_D1	GPIO_28 / GPIO_49
SMIH_D2	GPIO_29 / GPIO_50
SMIH_D3	GPIO_30 / GPIO_51
SMIH_D4	GPIO_54
SMIH_D5	GPIO_55
SMIH_D6	GPIO_56
SMIH_D7	GPIO_57
SMIH_CD_N	GPIO_6 / GPIO_53
SMIH_WP	GPIO_7 / GPIO_52

ETHERNET INTERFACE

IO Functionality	Combinations possible on SoC GPIO's
RMII_REF_CLK	GPIO_8 / GPIO_55
RMII_CRS_DV	GPIO_14 / GPIO_16 / GPIO_56
RMII_MDC	GPIO_11 / GPIO_53
RMII_MDO	GPIO_12 / GPIO_54
RMII_TXEN	GPIO_9 / GPIO_30 / GPIO_51
RMII_TXD0	GPIO_7 / GPIO_26 / GPIO_50
RMII_TXD1	GPIO_6 / GPIO_25 / GPIO_49
RMII_RXD0	GPIO_15 / GPIO_57
RMII_RXD1	GPIO_10 / GPIO_52

I2S Master/Slave

IO Functionality	Combinations possible on SoC GPIO's	
I2S_2CH_CLK	GPIO_7 / GPIO_28 / GPIO_49	ULP_GPIO_4 / ULP_GPIO_8
I2S_2CH_WS	GPIO_11 / GPIO_16 / GPIO_27 / GPIO_48	ULP_GPIO_5 / ULP_GPIO_9
I2S_2CH_DIN_0	GPIO_10 / GPIO_29	ULP_GPIO_6 / ULP_GPIO_10
I2S_2CH_DIN_1	GPIO_46	
I2S_2CH_DOUT_0	GPIO_6 / GPIO_30	ULP_GPIO_7 / ULP_GPIO_11
I2S_2CH_DOUT_1	GPIO_47	

Cortex-M4F Trace Interface

IO Functionality	Combinations possible on SoC GPIO's	
TRACE_CLK	GPIO_53	
TRACE_CLKIN	GPIO_52	
TRACE_D0	GPIO_54	
TRACE_D1	GPIO_55	
TRACE_D2	GPIO_56	
TRACE_D3	GPIO_57	

CAN INTERFACE

IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
CAN1_TXD	GPIO_30 / GPIO_47	ULP_GPIO_5 / ULP_GPIO_11
CAN1_RXD	GPIO_16 / GPIO_29 / GPIO_46	ULP_GPIO_4 / ULP_GPIO_10

I2C1 INTERFACE

IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
I2C1_SCL	GPIO_7 / GPIO_12 / GPIO_25 / GPIO_50	ULP_GPIO_4 / ULP_GPIO_8
I2C1_SDA	GPIO_6 / GPIO_15 / GPIO_26 / GPIO_51	ULP_GPIO_5 / ULP_GPIO_9

I2C2 INTERFACE		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
I2C2_SCL	GPIO_10 / GPIO_28	ULP_GPIO_2 / ULP_GPIO_6 / ULP_GPIO_10
I2C2_SDA	GPIO_11 / GPIO_29	ULP_GPIO_3 / ULP_GPIO_7 / ULP_GPIO_11
PWM Interface		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
PWM_1H	GPIO_9 / GPIO_18	ULP_GPIO_3 / ULP_GPIO_4
PWM_1L	GPIO_8	ULP_GPIO_2 / ULP_GPIO_5
PWM_2H	GPIO_10	ULP_GPIO_7
PWM_2L	GPIO_11	ULP_GPIO_6
PWM_3H	GPIO_14	ULP_GPIO_9
PWM_3L	GPIO_38	ULP_GPIO_8
PWM_4H		ULP_GPIO_11
PWM_4L		ULP_GPIO_10
PWM_FAULTA		ULP_GPIO_0
PWM_FAULTB		ULP_GPIO_1
PWM_SLP_EVENT_TRIG		ULP_GPIO_5
PWM_TMR_EXT_TRIG_1	GPIO_38	ULP_GPIO_0 / ULP_GPIO_6
PWM_TMR_EXT_TRIG_2		ULP_GPIO_1 / ULP_GPIO_7
PWM_TMR_EXT_TRIG_3		ULP_GPIO_2
PWM_TMR_EXT_TRIG_4		ULP_GPIO_3
QEI Interface		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
QEI_DIR	GPIO_9 / GPIO_30	ULP_GPIO_3

QEI_IDX	GPIO_6 / GPIO_27	ULP_GPIO_0
QEI_PHA	GPIO_8 / GPIO_29	ULP_GPIO_1
QEI_PHB	GPIO_7 / GPIO_28	ULP_GPIO_2
SIO		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
SIO_0	GPIO_6 / GPIO_48	ULP_GPIO_0 / ULP_GPIO_4
SIO_1	GPIO_7 / GPIO_49	ULP_GPIO_1 / ULP_GPIO_5
SIO_2	GPIO_8 / GPIO_50	ULP_GPIO_2 / ULP_GPIO_6
SIO_3	GPIO_9 / GPIO_51	ULP_GPIO_3 / ULP_GPIO_7
SIO_4	GPIO_16 / GPIO_25 / GPIO_52	
SIO_5	GPIO_11 / GPIO_26 / GPIO_53	
SIO_6	GPIO_27 / GPIO_54	
SIO_7	GPIO_28 / GPIO_55	
USART1		
IO Functionality	Combinations possible on SoC GPIO's	
USART1_CLK	GPIO_10 / GPIO_25 / GPIO_28	ULP_GPIO_8
USART1_CTS	GPIO_15 / GPIO_28	ULP_GPIO_4 / ULP_GPIO_8
USART1_RTS	GPIO_12 / GPIO_27	ULP_GPIO_9
USART1_DCD	GPIO_47	
USART1_DSR	GPIO_46	
USART1_DTR	GPIO_48	
USART1_IR_RX	GPIO_12 / GPIO_53	
USART1_IR_TX	GPIO_10 / GPIO_54	
USART1_RI	GPIO_52	

USART1_RS485_DE	GPIO_57	ULP_GPIO_5
USART1_RS485_EN	GPIO_55	ULP_GPIO_6
USART1_RS485_RE	GPIO_56	ULP_GPIO_7
USART1_RX	GPIO_8 / GPIO_14 / GPIO_27 / GPIO_29	ULP_GPIO_10
USART1_TX	GPIO_9 / GPIO_26 / GPIO_30	ULP_GPIO_11
SCT		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
SCT_IN_0	GPIO_12	ULP_GPIO_0
SCT_IN_1		ULP_GPIO_1
SCT_IN_2	GPIO_14 / GPIO_25	ULP_GPIO_2
SCT_IN_3	GPIO_26 / GPIO_53	ULP_GPIO_3
SCT_IN_4	GPIO_27	ULP_GPIO_10
SCT_IN_5		ULP_GPIO_11
SCT_OUT_0	GPIO_6 / GPIO_14 / GPIO_25 / GPIO_50	ULP_GPIO_4
SCT_OUT_1	GPIO_7 / GPIO_26 / GPIO_51	ULP_GPIO_5
SCT_OUT_2	GPIO_8 / GPIO_29 / GPIO_46	ULP_GPIO_6
SCT_OUT_3	GPIO_9 / GPIO_47	ULP_GPIO_7
SCT_OUT_4	GPIO_10 / GPIO_30 / GPIO_48	ULP_GPIO_0 / ULP_GPIO_8
SCT_OUT_5	GPIO_11 / GPIO_49	ULP_GPIO_1 / ULP_GPIO_9
SCT_OUT_6	GPIO_12	ULP_GPIO_2 / ULP_GPIO_10
SCT_OUT_7	GPIO_15 / GPIO_52	ULP_GPIO_3 / ULP_GPIO_11
UART2 INTERFACE		
IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
UART2_TX	GPIO_6 / GPIO_12 / GPIO_25 / GPIO_47	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_9

UART2_RX	GPIO_7 / GPIO_15 / GPIO_26 / GPIO_46	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8
UART2_CTS	GPIO_38 / GPIO_50	ULP_GPIO_2 / ULP_GPIO_6
UART2_RTS	GPIO_49	ULP_GPIO_3 / ULP_GPIO_7
UART2_RS485_EN	GPIO_48	
UART2_RS485_RE	GPIO_50	
UART2_RS485_DE	GPIO_51	

Miscellaneous Interface

IO Functionality	Combinations possible on SoC GPIO's	Combinations possible on ULP GPIO's
REF_CLK_OUT	GPIO_38	
MCU_CLK_OUT	GPIO_12 / GPIO_15	
SDMEM_PRESENT	GPIO_9 / GPIO_38	
USB_DRVVBUS	GPIO_11 / GPIO_14 / GPIO_16	
USB_XTAL_ON	GPIO_51	
XTAL_ON_IN	GPIO_16	ULP_GPIO_9

2.5 Functional Description

2.5.1 Digital Functions

Pin Name	Direction	Description
CAN (Controller Area Network) Interface		
CAN1_RXD	Input	CAN Receive Data
CAN1_TXD	Output	CAN Transmit Data
GSPI (General SPI) Interface		

Pin Name	Direction	Description
GSPI_MST1_CLK	Output	Output Clock from the GSPI master to external slave
GSPI_MST1_CS0 to GSPI_MST1_CS3	Output	Active Low CSN. GSPI Master can select a maximum of 4 slaves.
GSPI_MST1_MISO	Input	Input data to master from external slave
GSPI_MST1_MOSI	Output	Output data from master to external slave

I2C (Inter-integrated Circuit) Interface

I2Cx_SCL, ULP_I2C_SCL	Inout	I2C Serial Clock x= 1, 2
I2Cx_SDA, ULP_I2C_SDA	Inout	I2C Serial Data x= 1, 2

2 Channel I2S (Inter-IC Sound) Interface

I2S_2CH_CLK	Output/	I2S Clock
ULP_I2S_CLK	Input	Output in Master Mode and Input in Slave Mode
I2S_2CH_WS	Output/	Active high I2S Word Select
ULP_I2S_WS	Input	Output in Master Mode and Input in Slave Mode
I2S_2CH_DIN_0 to I2S_2CH_DIN_1	Input	I2S Input Data
ULP_I2S_DIN		
I2S_2CH_DOUT_0 to I2S_2CH_DOUT_1	Output	I2S Output Data
ULP_I2S_DOUT		

QSPI (Quad SPI) Interface

MCU_QSPI_CLK	Output	Output clock to the external SPI slave.
MCU_QSPI_CS0 to MCU_QSPI_CS1	Output	Active Low Chip Select to select a maximum of two slaves.
MCU_QSPI_D0 to MCU_QSPI_D7	Inout	QSPI Data. Supports both QUAD and OCTA Data. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid.

Pin Name	Direction	Description
		In Octa Mode, all the bits are valid
MCU_QSPI_DQS	Input	Data Strobe signal
SMIH (SD/SDIO/MMC Host Controller) Interface		
SMIH_CLK	Output	Output Clock from the SMIH Controller
SMIH_CMD	Output	Output Command from the SMIH Controller
SMIH_D0 to SMIH_D7	Inout	Bidirectional 8-bit Data
SMIH_CD_N	Input	Active Low Card Detect
SMIH_WP	Input	Active Low Write Protect
Cortex-M4F Trace Interface		
TRACE_CLK	Output	Trace Clock from Cortex-M4F
TRACE_CLKIN	Input	Trace Port Clock to Cortex-M4F. Connect to GPIO_38 (REF_CLK_OUT) when Cortex-M4F Trace functionality is needed
TRACE_D0 to TRACE_D3	Output	Trace Port Data bus from Cortex-M4F
PWM (Pulse Width Modulation) Interface		
PWM_xH	Output	PWM output signals. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge.
PWM_xL	Output	x = 1,2,3,4
PWM_FAULTA	Input	External fault signal A
PWM_FAULTB	Input	External fault signal B
PWM_SLP_EVENT_TRIG	Output	Special event trigger for synchronizing analog to digital conversions.
PWM_TMR_EXT_TRIGGER_1 to PWM_TMR_EXT_TRIGGER_4	Input	External trigger for base timers to increment. Each Channel has separate trigger input.
QEI (Quadrature Encode Interface)		

Pin Name	Direction	Description
QEI_DIR	Output	Position counter direction. '1' means counter direction is positive. '0' means counter direction is negative.
QEI_IDX	Input	QE Index. Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position.
QEI_PHA	Input	QE Phase A input
QEI_PHB	Input	QE Phase B input
RMII (Reduced media-independent interface)		
RMII_CRS_DV	Input	PHY Receive Data Valid
RMII_MDC	Output	Management Data Clock
RMII_MDO	Inout	Management Data
RMII_REF_CLK	Output/ Input	Output Clock when clock is provided from Internal PLL The Clock is taken from external interface when internal PLL is not used.
RMII_RXD0 to RMII_RXD1	Input	Receive Data
RMII_TXD0 to RMII_TXD1	Output	Transmit Data
RMII_TXEN	Output	Active High Transmit Data Enable. When asserted indicates that Transmit Data is valid.
SCT (State Configurable Timer) Interface		
SCT_IN_0 to SCT_IN_5	Input	Timer input event
SCT_OUT_0 to SCT_OUT_7	Output	Timer output event
SIO (Serial Input Output) Interface		
SIO_0 to SIO_7	Inout	Serial Input-Output Data
SSI (Synchronous Serial Interface) Master		
SSI_MST_CLK	Output	Output clock from SSI Master

Pin Name	Direction	Description
ULP_SPI_CLK		
SSI_MST_CS0 to SSI_MST_CS3	Output	Active Low Chip select
ULP_SPI_CS0 to ULP_SPI_CS2		
SSI_MST_DATA0 to SSI_MST_DATA1	Inout	Bidirectional Data
ULP_SPI_DOUT	Output	Master Output Data
ULP_SPI_DIN	Input	Master Input Data
SSI (Synchronous Serial Interface) Slave		
SSI_SLV_CLK	Input	Input clock to SSI Slave
SSI_SLV_CS	Input	Active Low Chip select
SSI_SLV_MISO	Output	Slave Output Data
SSI_SLV_MOSI	Input	Slave Input Data
UART Interface		
UART2_CTS, ULP_UART_CTS	Input	Active low Clear to Send
UART2_RTS, ULP_UART_RTS	Output	Active low Request to Send
UART2_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART2_RS485_EN	Output	Active high RS485 Enable
UART2_RS485_RE	Output	Receiver Enable. Polarity is programmable.
UART2_RX, ULP_UART_RX	Input	Serial Input
UART2_TX, ULP_UART_TX	Output	Serial Output
USART Interface		

Pin Name	Direction	Description
USART1_CLK	Inout	Serial interface clock
USART1_CTS	Input	Active low Clear to Send
USART1_RTS	Output	Active low Request to Send
USART1_DCD	Input	Active low Data Carrier Detect
USART1_DSR	Input	Active low Data Set Ready
USART1_DTR	Output	Active low Data Terminal Ready
USART1_IR_RX	Input	IrDA SIR Input
USART1_IR_TX	Output	IrDA SIR Output
USART1_RI	Input	Active low Ring Indicator
USART1_RS485_DE	Output	Driver Enable. Polarity is programmable.
USART1_RS485_EN	Output	Active high RS485 Enable
USART1_RS485_RE	Output	Receiver Enable. Polarity is programmable.
USART1_RX	Input	Serial Input
USART1_TX	Output	Serial Output
Timers Interrupt Interface		
Timer0 and Timer1	Output	Active-high interrupts from Timers
IR Interface		
IR_INPUT	Input	IR Data Pattern Input
IR_PG_EN	Output	Active-high enable signal to the external IR Sensor.
Miscellaneous Interface		
REF_CLK_OUT	Output	Clock from internal source. Connect to GPIO_52 (TRACE_CLKIN) when Cortex-M4F Trace functionality is needed
MCU_CLK_OUT	Output	All the Clocks that are used by Cortex-M4F SoC are

Pin Name	Direction	Description
		multiplexed and connected on this pin
SDMEM_PRESENT	Input	Active-high signal to indicate that an SD Memory Card is connected along with the device's SDIO Slave to an SDIO Host
USB_DRVVBUS	Output	Signal from USB Controller to be connected to off-chip charge pump circuit.
USB_XTAL_ON	Output	If the reference clock to the USB PLL is fed through GPIO_25, this signal is used to control the Crystal Oscillator which generates the reference clock
XTAL_ON_IN	Input	Crystal oscillator enable input when crystal is shared by another chip

UULP VBAT Pin Interface

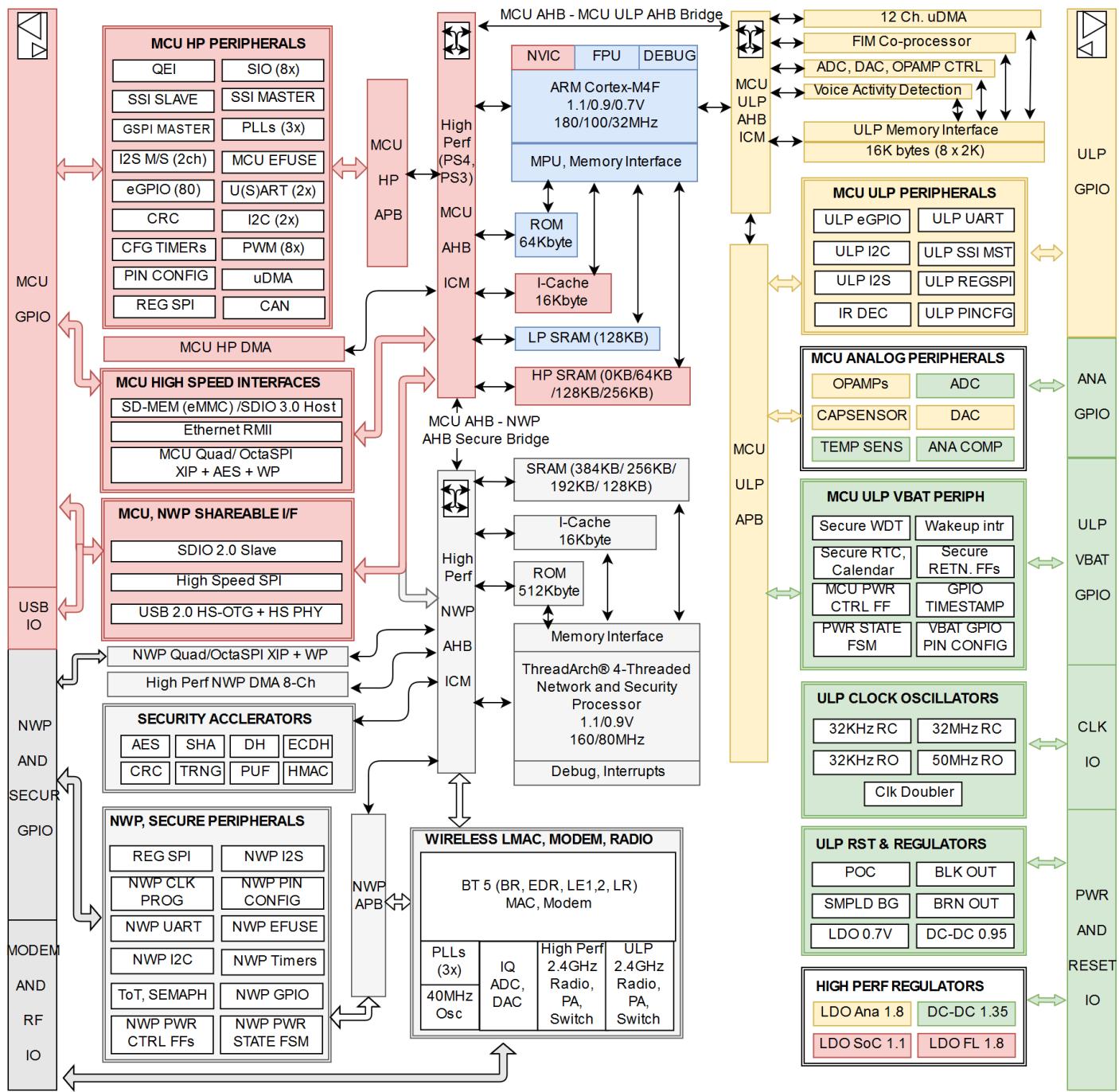
EXT_PG_EN	Output	Enable to an external Buck boost regulator or Power gate that controls the supply to all supply pins of the chip except the UULP VBAT supply
XTAL_32KHZ_IN	Input	Low Frequency clock input from an External 32KHz Crystal oscillator
MCU_GPIO2/3/4_WAKEUP	Input	GPIOs that can be used as Wakeup interrupt to MCU while in Retention or Deep sleep mode

2.5.2 Analog Functions

Pin Name	Direction	Description
ADC Interface		
ADCP0 - ADCP19	Input	The 20 single ended input channels that are multiplexed onto the ADC P0 - P9 can be coupled with N0 - N9 for differential mode of operation of the ADC

Pin Name	Direction	Description
ADCN0 - ADCN9	Input	The N pins of the 10 possible differential channels multiplexed onto the ADC
DAC Interface		
DAC0, DAC1	Output	Possible output pins from the internal DAC
OpAmp Interface		
OPAMP xyz	Input	<p>Multiplexed inputs of the three OpAmps. xyz denote the OpAmp number, the terminal and the multiplexing on that pin of the OpAmp</p> <p>x = OpAmp number (1, 2 or 3)</p> <p>y = P or N terminal of OpAmp</p> <p>z = 0, 1, 2, 3, 4, 5 (Multiplexing at OpAmp input pin). Note that OPAMP1P is available at 6 locations, OPAMP2P, 3P and 1N are available at 2 locations each and OPAMP2N and 3N pins are available at only one location</p>
OPAMP1OUT0/1, OPAMP2/3OUT0	Output	Outputs of the three OpAmps. Note that OPAMP1 output is available at two possible pin locations whereas OPAMP2 and 3 outputs are available at a fixed pin
Comparator Interface		
COMP xyz		<p>Multiplexed inputs of the two Comparators. xyz denote the Comparator number, the terminal and the multiplexing on that pin of the Comparator</p> <p>x = Comparator number (A or B)</p> <p>y = P or N terminal of OpAmp</p> <p>z = 0, 1 (Multiplexing at Comparator Input pin). Note that each input pin of both comparators is available on two possible GPIO pins.</p>
Touch Interface		
TOUCH0/1/2/3/4/5/6/7	Input	Capacitive Touch inputs

3 RS14100 CA1/CC1 module System Block Diagram



MCU POWER STATE VS BLOCK AVAILABILITY COLOR CODING LEGEND:

PS4/3 ACTIVE & STANDBY	PS4/3/2 ACTIVE & STANDBY	PS4/3/2/1 ACTIVE & STANDBY	PS4/3/2/1/0 ACTIVE, STANDBY, SLEEP & DEEPSLEEP	WIRELESS NWP POWER STATES ARE INDEPENDENT OF MCU
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NOTE: SRAM is operational in ACTIVE/STANDBY states, SRAM can be retained in SLEEP states (partial or whole) & SRAM contents are lost in DEEPSLEEP state

Figure 4 System Block Diagram

4 RS14100 CA1/CC1 module Specifications

4.1 Absolute Maximum Ratings

Functional operation above maximum ratings is not guaranteed and may damage the device.

Symbol	Parameter	Min	Max	Units
T _{store}	Storage temperature	-40	+125	°C
T _{j(max)}	Maximum junction temperature	-	+125	°C
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	-0.6	3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	-0.5	3.63	V
VINBCKDC	Power supply for the on-chip Buck	-0.5	3.63	V
VINLDOSOC	Power supply for SoC LDO	-0.5	1.8	V
IO_VDD_1	I/O supplies for GPIOs	-0.5	3.63	V
IO_VDD_4	I/O supplies for GPIOs	-0.5	3.63	V
ULP_IO_VDD	I/O supplies for ULP GPIOs	-0.5	3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	-0.5	3.63	V
PA5G_AVDD	Power supply for the 5 GHz RF Power Amplifier	-0.5	3.63	V
RF_AVDD	Power supply for the 2.4 GHz RF and AFE	-0.5	1.98	V
RF_AVDD_BTTX	Power supply for Bluetooth Transmit circuit.	-0.5	1.21	V
RF_AVDD33	Power supply for the 5 GHz RF	-0.5	3.63	V
AVDD_1P9_3P3	Power supply for the 5 GHz RF	-0.5	3.63	V
AVDD_1P2	Power supply for the 5 GHz RF	-0.5	1.32	V
UULP_AVDD	Power supply for the always-on digital and ULP peripherals	-0.5	1.21	V
USB_AVDD_3P3	Power supply for the USB interface	-0.5	3.63	V
USB_AVDD_1P1	Power supply for the USB core	-0.5	1.26	V
ESD _{HBM}	Electrostatic discharge tolerance (HBM) Compliant with JEDEC specification JS-001-2017		2000	V
ESD _{CDM}	Electrostatic discharge tolerance (CDM) Compliant with JEDEC specification JS-002-2014	-	500	V
LU	Latchup Immunity ICE criteria at ambient temp of 25°C Compliant with JESD78D	-50	100	mA
I _{max}	Maximum Current consumption in TX mode	-	400	mA
P _{max}	RF Power Level Input to the chip	-	10	dBm
I _{pmax}	Peak current rating for power supply	-	500	mA

Table 13 Absolute Maximum Ratings

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
T _{ambient}	Ambient temperature	-40	25	85	°C
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	3	3.3	3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	3	3.3	3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	1.8	3.3	3.63	V
VINBCKDC	Power supply for the on-chip Buck	3	3.3	3.63	V
VINLDOSOC	Power supply for SoC LDO	1.1	1.35	1.55	V
IO_VDD_1	I/O supply for GPIOs	3	3.3	3.63	V
IO_VDD_4	I/O supply for GPIOs	1.8	3.3	3.63	V
ULP_IO_VDD	I/O supply for ULP GPIOs	1.8	3.3	3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	1.8	3.3	3.63	V
PA5G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	3	3.3	3.63	V
RF_AVDD	Power supply for the 2.4 GHz RF and AFE	1.3	1.35	1.8	V
RF_AVDD_BTTX	Power supply for Bluetooth Transmit circuit.	1.0	1.1	1.2	V
RF_AVDD33	Power supply for the 5 GHz RF	3	3.3	3.6	V
AVDD_1P9_3P3	Power supply for the 5 GHz RF	1.9	3.3	3.6	V
PLL_AVDD	Power supply for the on-chip PLLs	1.3	1.35	1.8	V
AVDD_1P2	Power supply for the 5 GHz RF (1.2V)	1.05	1.1	1.2	V
UULP_AVDD	Power supply for the always-on digital and ULP peripherals	0.95	1.0	1.21	V
USB_AVDD_3P3	Power supply for the USB interface	3.0	3.3	3.63	V
USB_AVDD_1P1	Power supply for the USB core	0.99	1.1	1.21	V

Table 14 Recommended Operating Conditions

4.3 DC Characteristics

4.3.1 Reset Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH}	High level input voltage	0.8 * VDD	-	3.63	V
V _{IL}	Low-level input voltage	-0.5	-	0.3 * VDD	V
V _{hys}	Hysteresis voltage	0.05 * VDD	-	-	V

Table 15 Reset Pin

¹The minimum supply voltage at first power-up needs to be 2.4V and the battery can then drain to 2.14V when the POC_IN is connected to POC_OUT.

4.3.2 Power On Control (POC) and Reset

The power on control has two options depending on the voltage level of the UULP_VBATT_1/2 supplies (VBATT supply). The POC_IN input of the chip can be connected to the internally generated POC_OUT signal if the VBATT supply is greater than 2.15V. If the VBATT supply is between 1.72 and 2.15V, then the POC_IN signal needs to be controlled from an external source.

4.3.2.1 POC_OUT Connected to POC_IN

The IC generates a POC (Power On Control) signal - POC_OUT that is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to safe state the IC till a valid supply is available for proper operation. This power management is functional in both power up and power down sequences.

During power up, until the UULP_AVDD reaches 0.7V and till the UULP_VBATT_1 and UULP_VBATT_2 (VBATT supply) reach 1.8V, the POC_OUT signal stays low. Once the UULP_AVDD exceeds 0.7V and VBATT supply exceeds 1.8V, the POC_OUT becomes high and normal operation of the IC starts.

Once the POC_OUT becomes high, it stays high. But if VBATT becomes lower than the Blackout threshold voltage, POC_OUT becomes low.

The following figure illustrates the power up sequence when POC_OUT is connected to POC_IN. As shown in the figure below, the RESET_N signal should be high 1ms after POC_OUT signal becomes high. The RESET_N signal can be controlled via options like an R/C circuit or another MCU's GPIO.

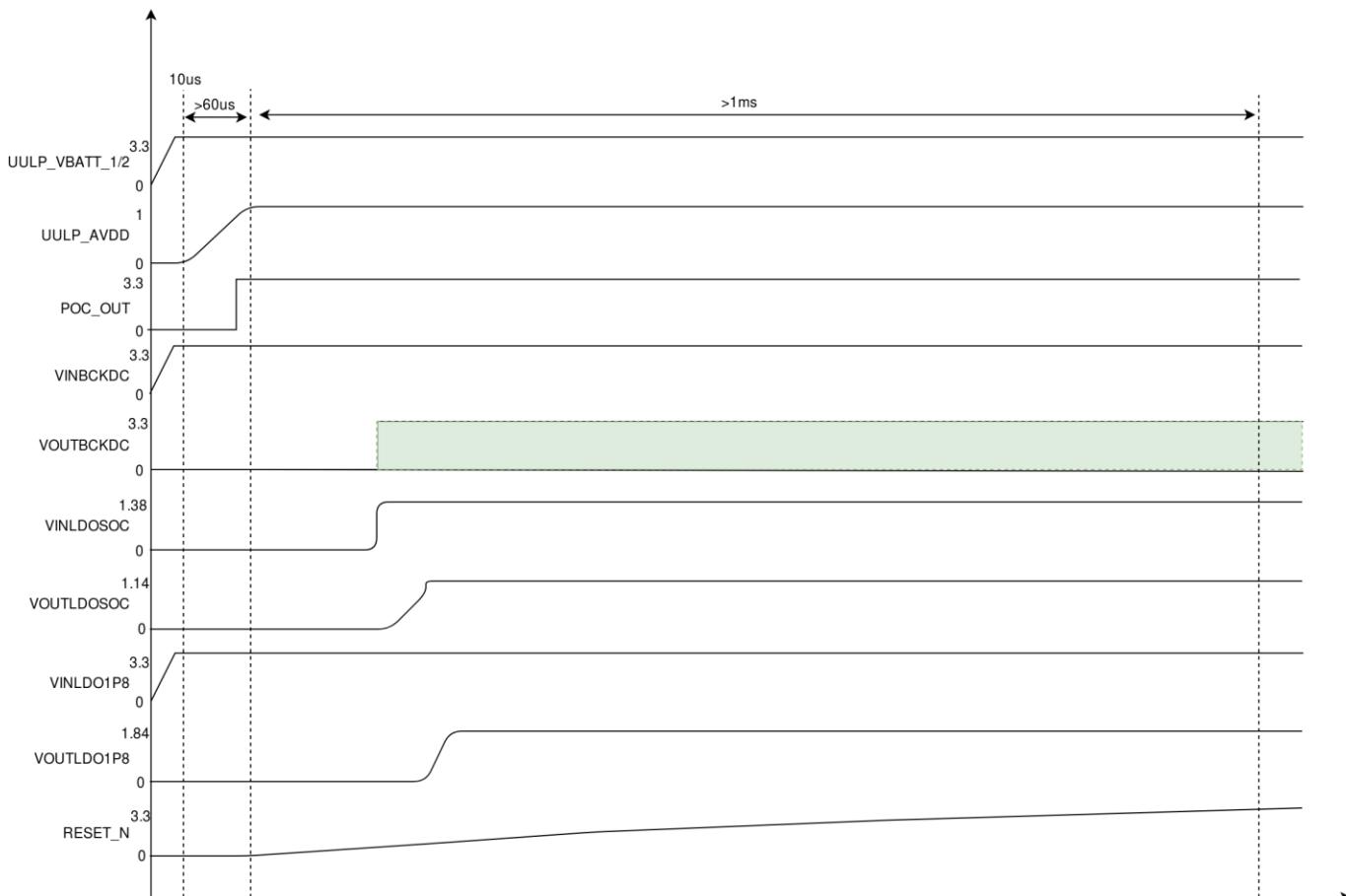
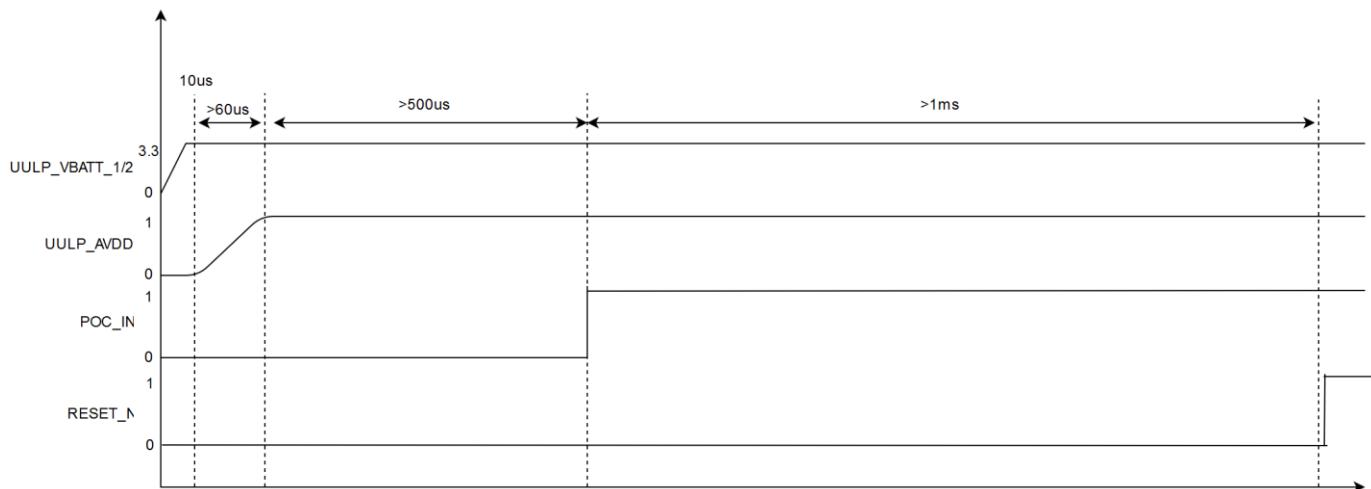


Figure 5 Power Up Sequence for POC_OUT Connected to POC_IN

4.3.2.2 External Control for POC_IN

The POC_IN and RESET_N signals should be controlled from external source like R/C circuits and/or another MCU's GPIOs when the VBATT supply is between 1.72 and 2.15V. The figure below illustrates the requirement for controlling POC_IN and RESET_N with respect to the VBATT and UULP_AVDD supplies.

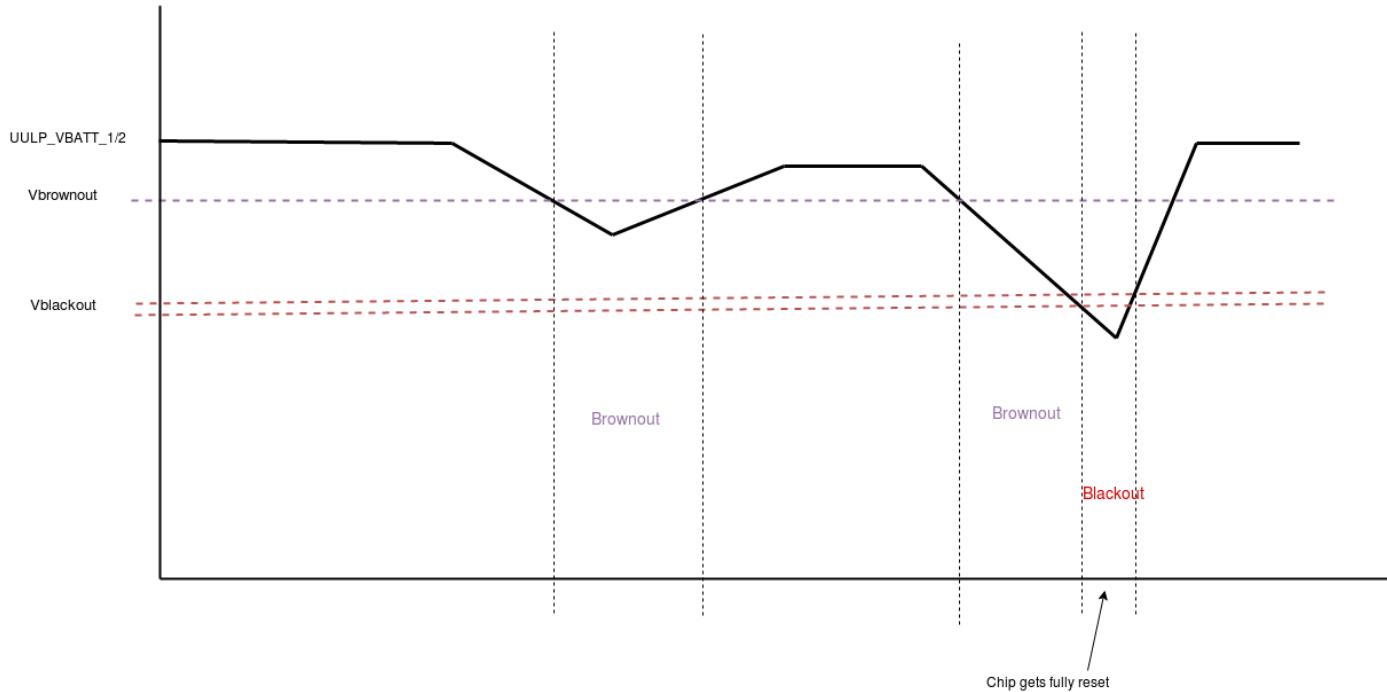
**Figure 6 Power Up Sequence with External Control for POC_IN**

4.3.3 Blackout monitor

The blackout comparator has a delay of less than 1us and current consumption of 4uA. It is enabled by default upon power up. Blackout is typically asserted when the UULP_VBATT (VBATT) supply goes lower than 1.8V (see table below), and it is de-asserted when VBATT supply goes higher than 1.9V. Upon a blackout event, the RESET_N signal is autonomously pulled low. The blackout monitor circuit performs this function only when POC_OUT is connected to POC_IN.

The blackout monitor block should be enabled to monitor the VBATT voltage only in high power modes. It can be switched off upon entry into low power mode to save the 4uA. In low power modes battery level detection can be implemented using the Nano-Power Brownout detection comparator.

When system is in low power mode , the blackout comparator is enabled upon a brownout event.

**Figure 7 Blackout monitor**

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
Blackout VTL	VBATT voltage at which the Blackout monitor resets the IC			1.89	2.15	V
Blackout VTH	VBATT voltage at which the Blackout monitor releases the IC from reset			1.99	2.25	V

Table 16 Blackout Monitor Electrical Specifications

4.3.4 Nano Power Comparator and Brown Out Detection (BOD)

The Nano Power comparator subsystem consists of a sampled comparator, reference buffer and resistor bank.

Features

- The comparator can be used to compare 2 external inputs from any of VOLT_SENSE, COMP_P, COMP_N signals
- External input (any of VOLT_SENSE, COMP_P, COMP_N signals) to internal programmable voltage reference
- Internal programmable voltage reference to a programmable supply voltage divider (This feature enables brown out detection)
- Three button wakeup is supported using single VOLT_SENSE signal

The comparator also has inbuilt hysteresis. The comparator has to be enabled to enable reference buffer and resistor bank. The reference buffer buffers the bandgap reference voltage and also has a voltage divider which gives programmable 100mV to 1.1V output. The resistor bank is used to detect battery voltage from 1.75V to 3.65V with a 50mV step. Since each bod_threshold value refers to a particular battery voltage, the battery voltage is found by comparing resistor bank output with reference buffer output using comparator for different bod_threshold values. For details on how to use slotting in BOD, refer to the BOD in UULP_VBAT Peripherals section of the Hardware Reference Manual.

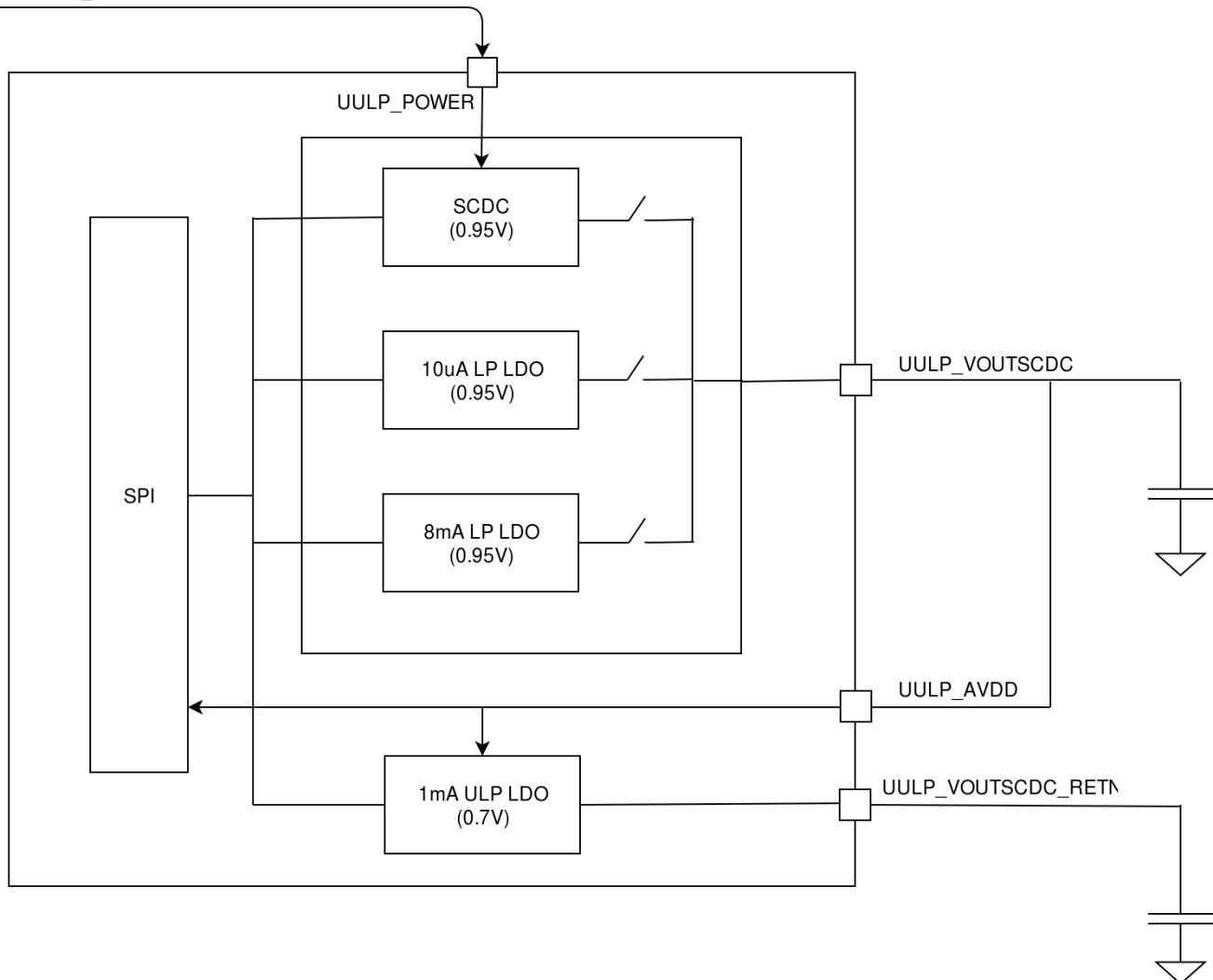
Parameter	Parameter Description	Conditions	Min	Typ	Max	Unit
T _{d_comp}	Delay from clock edge to comparator output	100mV overdrive		60		ns
T _{resp_comp}	The time delay from enable to output of comparator			0.3		us
V _{ref}	Programmable voltage reference range		0.1		1.1	V
V _{ref_step}	Programmable voltage reference step size			0.1		V
T _{set_buffer}	Settling time of voltage reference buffer			0.6		us
V _{os_comp}	The minimum voltage difference required between inputs to make output high	Typical value corresponds to 1-sigma variation		1.4		mV
V _{hyst_comp}	Hysteresis = 2'd1			60		mV
	Hysteresis = 2'd3			90		mV
ICMR_comp	Input common-mode range		0		VBATT-0.2	V
Iq_comp	Current consumption on VBATT with all blocks enabled, Sampling rate = 32KHz			70		uA
Iq_BOD_1SPS	Current consumption on VBATT with only BOD mode enabled @1SPS			25		nA

Table 17 Nano Power BOD Electrical Specifications

4.3.5 ULP Regulator

ULP (Ultra Low Power) regulators are used to power low power Always-ON (AON) digital and analog power management circuitry inside the IC. In addition to this, the ULP regulators can also be used to power the SRAMs and M4 core. The ULP regulators include two high power LDOs, a Low power LDO, and a switched capacitor DC-DC regulator. These regulators operate directly off of UULP_VBATT (VBATT supply).

4.3.5.1 Block Diagram UULP_VBATT

**Figure 8 ULP Regulator**

4.3.5.2 SC-DCDC

SC-DCDC stands for a Switched Capacitor DC-DC regulator. It operates from VBATT and generates a programmable output voltage. It has two major modes of operation, viz. LDO mode and DC-DC mode. And further each of these modes have a low power and high power option.

The IC starts up in the LDO mode and later switches to DC-DC Mode. For details on options to bypass any of the voltage regulators, refer to the ULP Regulators section in the Hardware Reference Manual.

4.3.5.2.1 SC-DCDC - LDO Mode

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V _{in}	Input Voltage Range		1.71		3.6	V
I _{load max}	Maximum load current	HP Mode			8	mA
		LP Mode			30	uA
I _q	Quiescent Current	HP Mode		17		uA
		LP Mode		5		nA

Table 18 SC-DCDC - LDO Mode Electrical Specifications

4.3.5.2.2 SC-DCDC - DC-DC Mode

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V _{in}	Input Voltage Range		1.71		3.6	V

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
$I_{load\ max}$	Maximum load current	HP Mode			8	mA
		LP Mode			300	uA
Efficiency			36.5	60	85	%

Table 19 SC-DCDC - DC-DC Mode Electrical Specifications

The ULP regulator switches from SC-DCDC mode to LDO mode for Vin lower than 2.4V

4.3.5.3 SC-DCDC - RETN MODE LDO

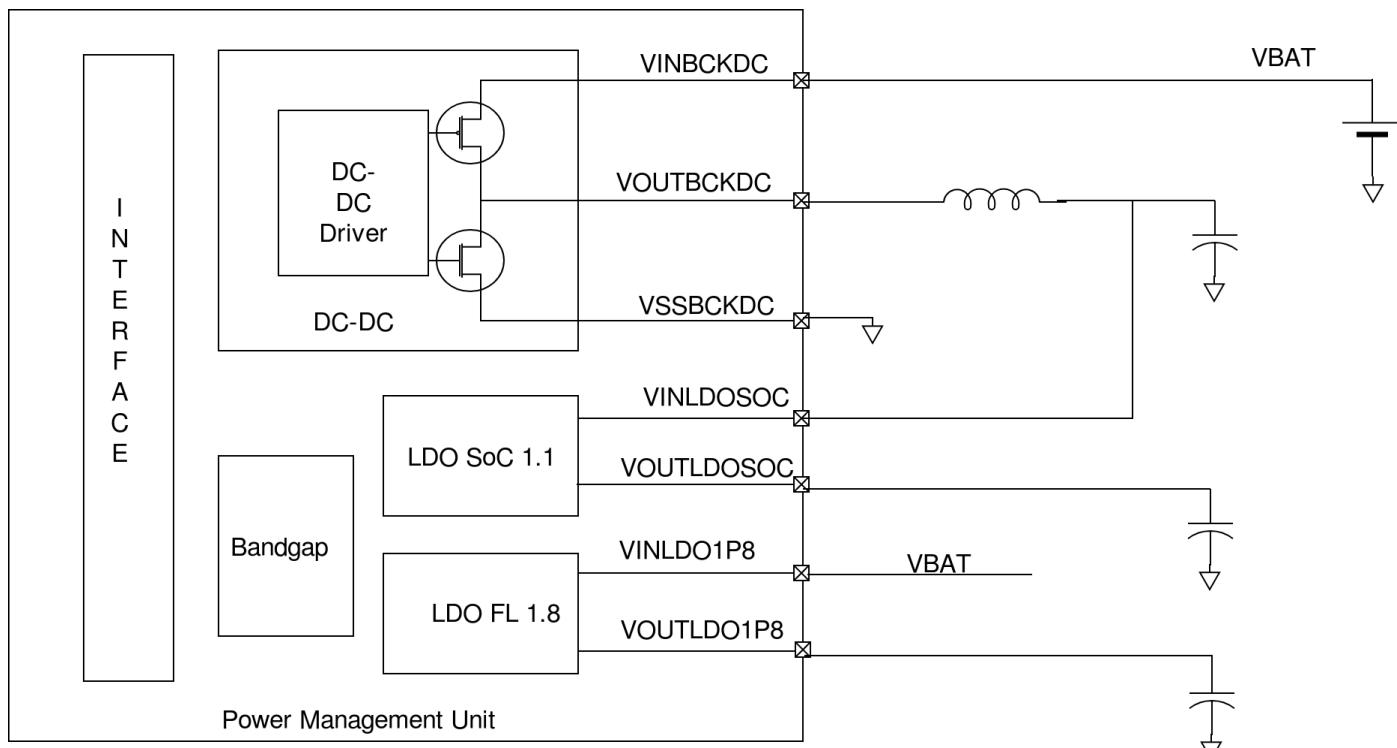
This LDO works off of the voltage generated by SC-DCDC regulator and generates a programmable output voltage. For details on options to bypass the voltage regulators, refer to the ULP Regulators section in the Hardware Reference Manual.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V_{in}	Input Voltage Range		0.95		1.1	V
V_{out}	Output Voltage Range		0.72	0.75	0.8	V
$I_{load\ max}$	Maximum load current	HP Mode			1	mA
		LP Mode			100	uA
I_q	Quiescent Current	HP Mode		2.5		uA
		LP Mode		30		nA

Table 20 RETN MODE LDO Electrical Specifications

4.3.6 SoC Power Management Unit

This section describes and specifies the Power Management Unit solution for the mixed signal System on Chip (SoC).

**Figure 9 Power Management Unit**

The major features are

- 1.4V DCDC switching converter

- 1.1V LDO for SOC digital supply
- 1.8V LDO for Flash supply
- For details on options to bypass any of the voltage regulators, refer to the POWER MANAGEMENT UNIT section in the Hardware Reference Manual

4.3.6.1 LC Buck Converter

- Provides stable programmable voltage from 0.8V to 1.55V.
- Output current upto 300mA.
- To down-convert the battery voltage with max efficiency of 90%.
- V_{in} range from 1.8V to 3.6V.
- Power save mode at light load currents.
- 100% duty cycle for lowest dropout.
- Typ. 600nA quiescent current in power save mode.
- Soft start

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage		1.71	3.3	3.6	V
V_{out}	Output Voltage Range		0.8	1.4	1.6	V
I_{load}	Load current	Active mode		250	300	mA
I_q	Quiescent Current	Normal Mode(with switching)		0.2		mA
		power save mode		<1		uA
I_{shdn}	Shutdown Supply Current			<0.1		uA

Table 21 LC Buck Converter Electrical Specifications

4.3.6.2 SoC LDO

- Provides stable programmable voltage from 0.8V to 1.55V.
- Output current up to 300mA.
- V_{in} range from 1.25 V to 1.98 V.
- Soft start

Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{in}	Input Supply Voltage		1.1		1.98	V
V_{out}	Output Voltage Range		0.5	1.1	1.3	V
V_{drop_out}	Dropout voltage		200			mV
I_{load}	Load current				300	mA
I_q	Quiescent Current	Normal Mode		72		uA
I_{shdn}	Shutdown Supply Current			0.1		uA

Table 22 SoC LDO Electrical Specifications

4.3.6.3 Flash LDO

- Provides stable programmable voltage from 1.6V to 2.9 V.
- Output current up to 125 mA.
- V_{in} range from 1.71 V to 3.6 V.

- Soft start

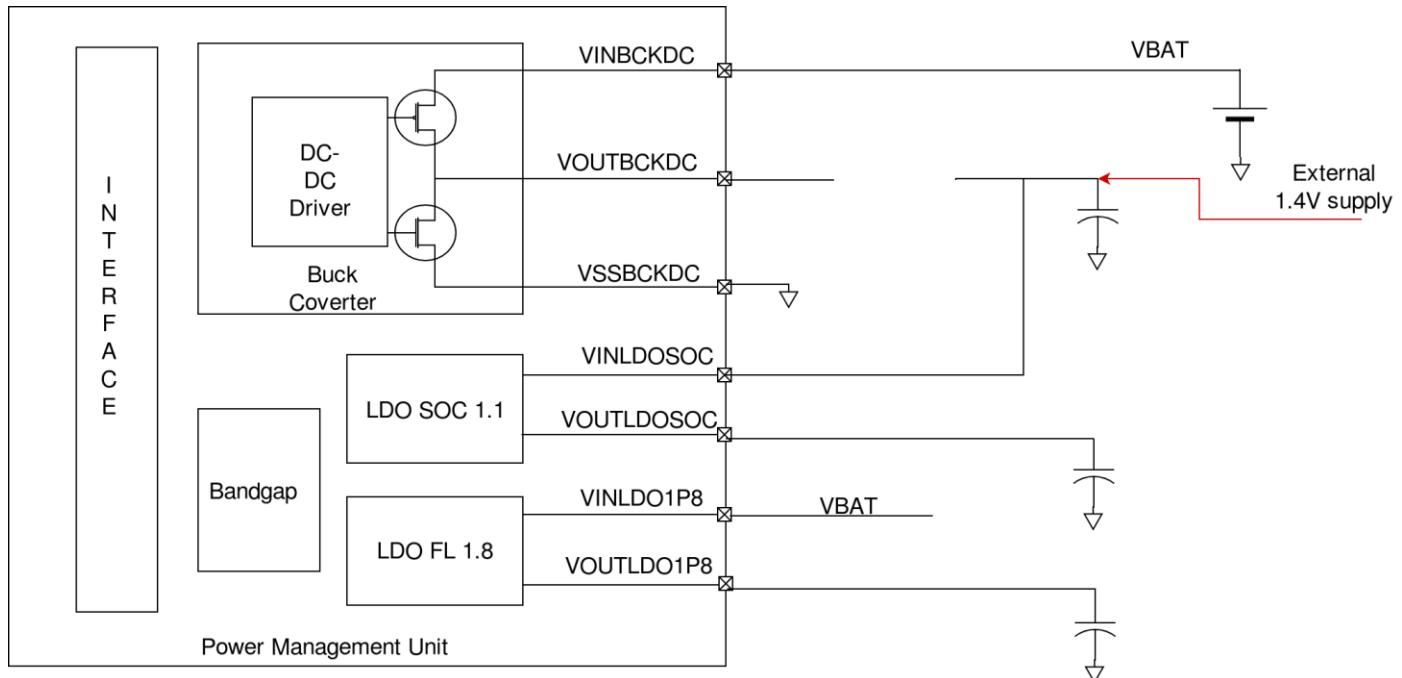
Parameter	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V _{in}	Input Supply Voltage		1.71		3.6	V
V _{out}	Output Voltage Range		1.6	1.8	2.9	V
V _{drop_out}	Dropout voltage		110			mV
I _{load}	Load current				125	mA
I _q	Quiescent Current	V _{out} = 1.84V		62		uA
I _{shdn}	Shutdown Supply Current			0.1		uA

Table 23 Flash LDO Electrical Specifications

4.3.6.4 PMU Bypass Options

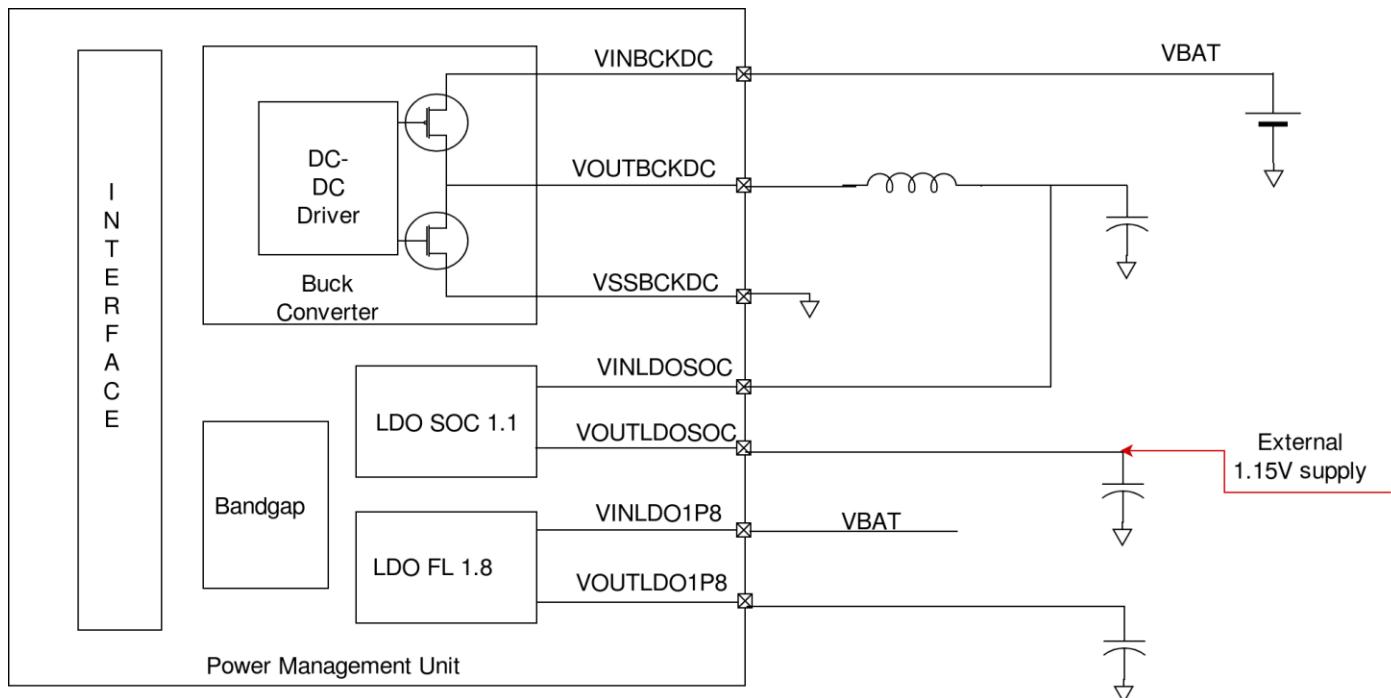
4.3.6.4.1 LC Buck bypass

To bypass PMU internal LC buck and use external supply, the PMU should be connected as per the following configuration. In this configuration, buck inductor is removed and 1.4 V external supply is given to VINLDOSOC.

**Figure 10 DC-DC 1.35 bypass**

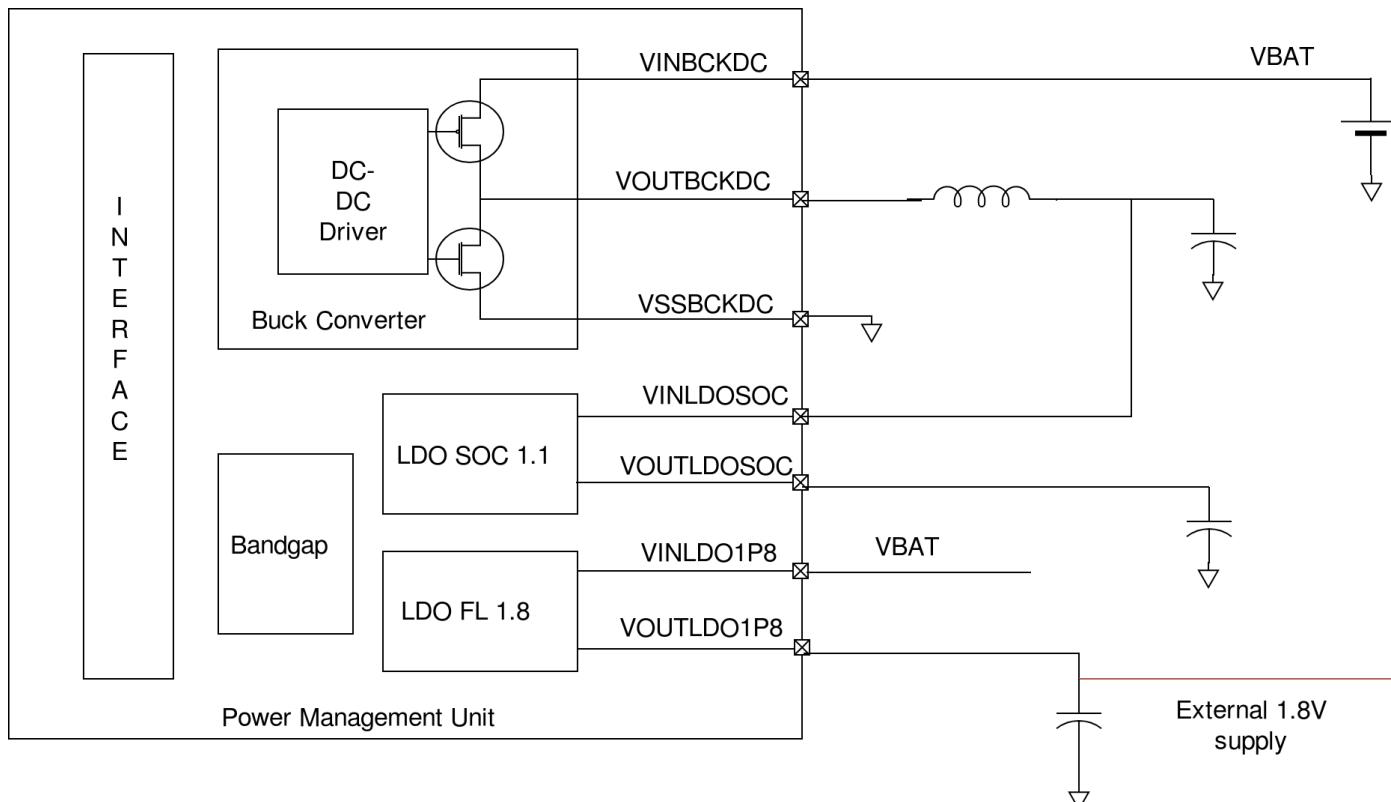
4.3.6.4.2 LDO SOC 1.1 bypass

To bypass PMU internal LDO SOC 1.1 and use external supply, the PMU should be connected as per the following configuration. In this configuration, LDO SOC 1.1 output is connected to the external supply of 1.15V.

**Figure 11 LDO SOC 1.1 bypass**

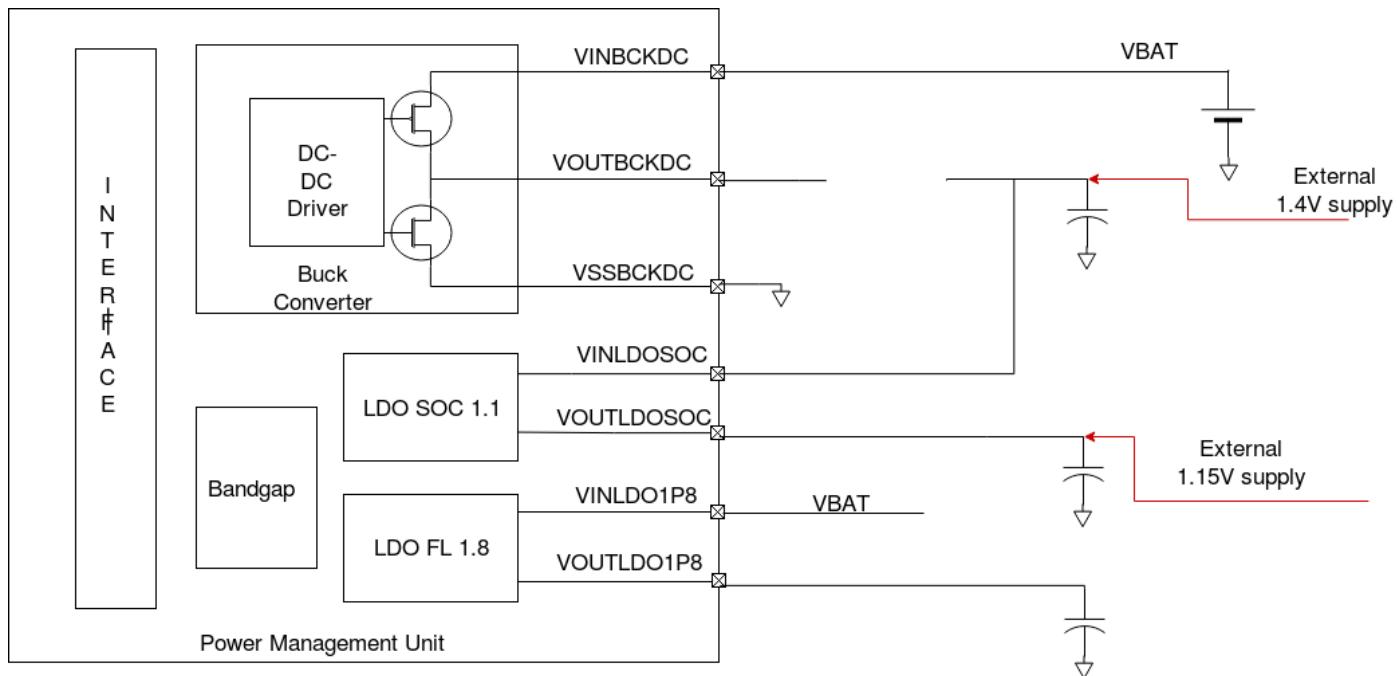
4.3.6.4.3 LDO FL 1.8 bypass

To bypass PMU internal LDO FL 1.8. the PMU should be connected as per the following configuration.



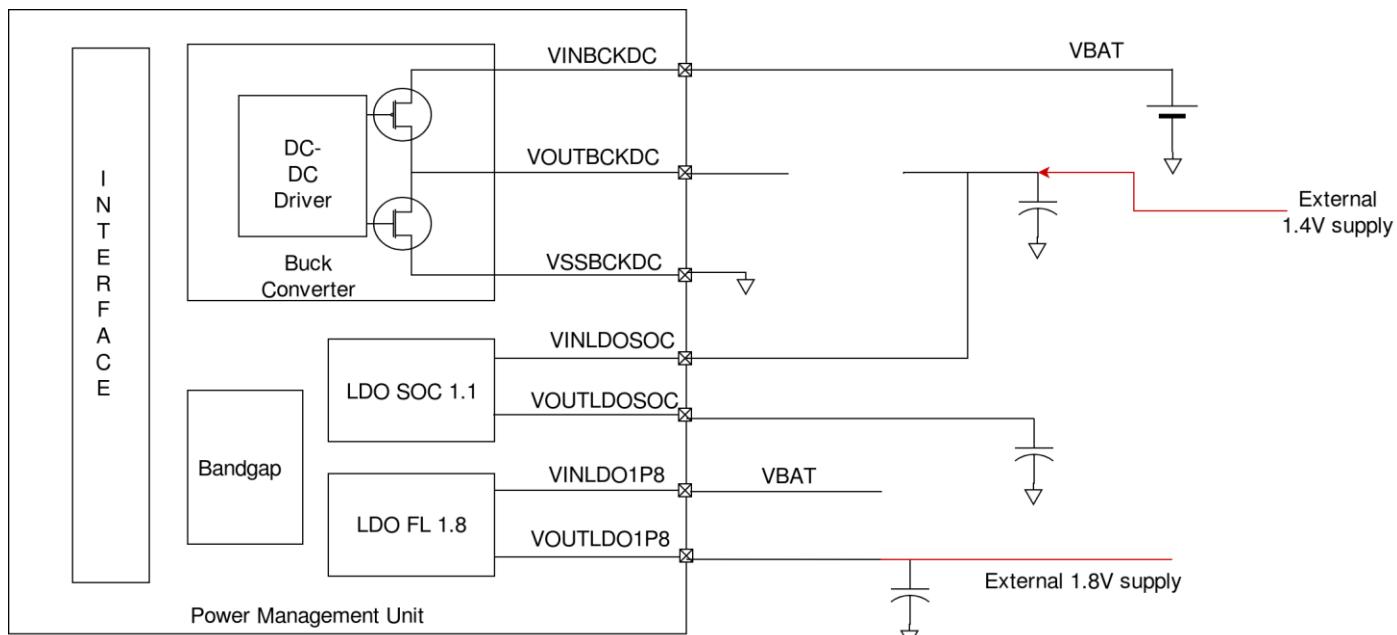
4.3.6.4.4 LC Buck + LDO SOC 1.1 bypass

To bypass PMU internal LC buck converter and LDO SOC 1.1. the PMU should be connected as per the following configuration.

**Figure 12 DC-DC 1.35 + LDO SOC 1.1 bypass**

4.3.6.4.5 LC Buck + LDO FL 1.8 bypass

To bypass PMU internal LC buck converter and LDO FL 1.8. the PMU should be connected as per the following configuration.

**Figure 13 DC-DC 1.35 + LDO FL 1.8 bypass**

4.3.6.4.6 LDO SOC 1.1 + LDO FL 1.8 bypass

To bypass PMU internal LDO SOC 1.1 and LDO FL 1.8. the PMU should be connected as per the following configuration.

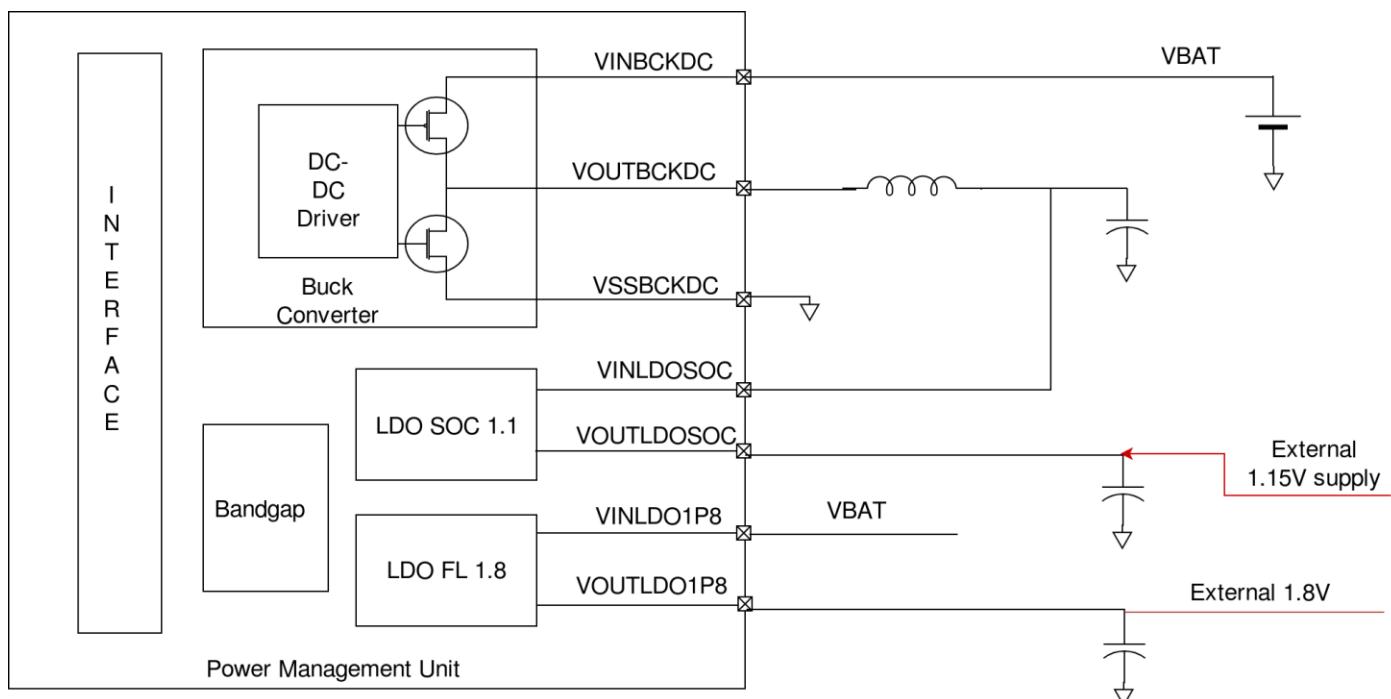


Figure 14 LDO SOC 1.1 + LDO FL 1.8 bypass

4.3.6.4.7 LC Buck + LDO SOC 1.1 + LDO FL 1.8 bypass

To bypass PMU internal LC buck converter, LDO SOC 1.1 and LDO FL 1.8. the PMU should be connected as per the following configuration.

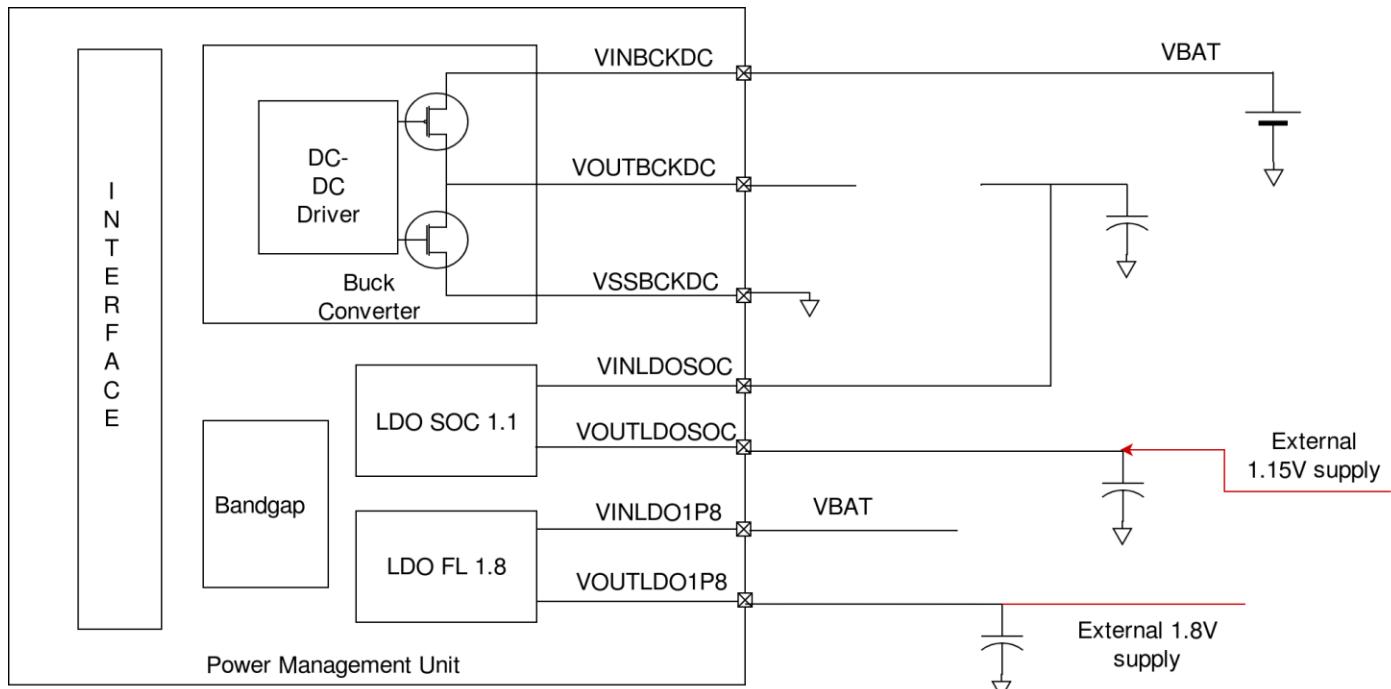


Figure 15 DC-DC 1.35 + LDO SOC 1.1 + LDO FL 1.8 bypass

4.3.7 Digital Input Output Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH}	High level input voltage	2.0	-	3.63	V
V _{IL}	Low level input voltage	-0.3	-	0.8	V
V _{hys}	Hysteresis voltage	0.1 VDD	-	-	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{OL}	Low level output voltage	-	-	0.4	V
V _{OH}	High level output voltage	VDD-0.4	-	-	V
I _{OL}	Low level output current (programmable)	2.0	4.0	12.0	mA
I _{OH}	High level output current (programmable)	2.0	4.0	12.0	mA

Table 24 Digital I/O Signals

4.3.8 USB

Parameter	Conditions	Min.	Typ.	Max.	Units
V _{cm} DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	-	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	-	2 2	V
Power supply ripple noise (Analog 3.3V)	< 160 MHz	-50	-	50	mV

Table 25 USB

4.3.9 Pin Capacitances

Symbol	Parameter	Min.	Typ.	Max.	Unit
C _{io}	Input/output capacitance, digital pins only	-	-	2.0	pF

Table 26 Pin Capacitances

4.3.9.1 Open-Drain I2C Pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH}	High level input voltage	0.7 VDD	-	-	V
V _{IL}	Low level input voltage	0	-	0.3 VDD	V
V _{hys}	Hysteresis voltage	0.1 x VDD	-	-	V
I _{OL}	VOL = 0.4, Low-level output current; pin configured as standard mode or fast mode	4.0	-	-	mA
I _{OL}	VOL = 0.4 Low-level output current; pin configured as standard mode or fast mode	VDD-0.4	-	-	V

Table 27 Open-Drain I2C Pins

4.4 AC Characteristics

4.4.1 Clock Specifications

RS14100 chipsets require two primary clocks:

- Low frequency 32 KHz clock for sleep manager and RTC
 - Internal 32 KHz RC clock is used for applications with low timing accuracy requirements
 - 32 KHz crystal clock is used for applications with low timing accuracy requirements

- High frequency clocks for NWP , MCU and MCU PLL
 - 40 MHz clock for the threadArch™ processor, baseband subsystem and the radio
 - 32MHz RC clock
 - High frequency ring oscillator

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused.

4.4.1.1 Low frequency clocks

The 32 KHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

4.4.1.1.1 32 KHz RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Units
F _{osc}	Oscillator Frequency		32.0		KHz
F _{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%
Jitter	RMS value of Edge jitter (TIE)		91		ns
Peak Period Jitter	Peak value of Cycle Jitter with 6σ variation		789		ns

Table 28 32 KHz RC oscillator

4.4.1.1.2 32 KHz External Oscillator

A low swing external 32 KHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.

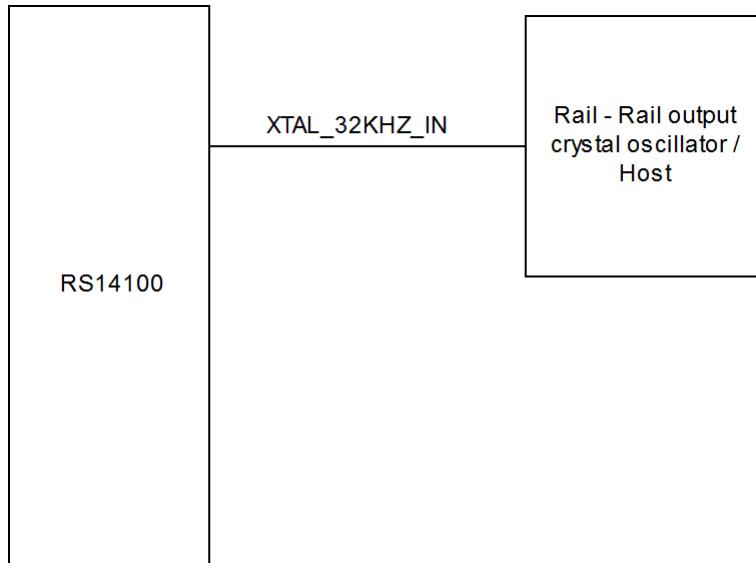


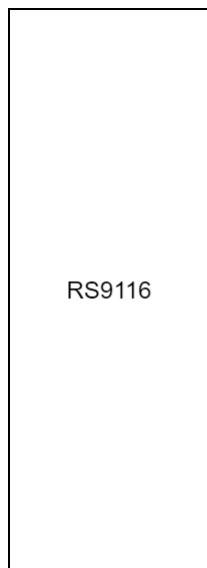
Figure 16 External 32 KHz oscillator - Rail to Rail

Parameter	Parameter Description	Min	Typ	Max	Units
F _{osc}	Oscillator Frequency		32.768		KHz
F _{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V _{AC}	Input AC peak-peak voltage swing at input pin.	0.3	-	VBATT-0.3	Vpp

Table 29 32 KHz external oscillator specifications

4.4.1.2 40 MHz Clock

The 40 MHz internal oscillator mode can be used by connecting a 40 MHz crystal between the pins XTAL_P and XTAL_N. Load capacitance is integrated inside the chipset and calibrated and the calibrated value can be stored in eFuse using calibration software.



Parameter	Parameter Description	Min	Typ	Max	Units
Fosc	Oscillator Frequency		40		KHz
Fosc_Acc	Frequency Variation with Temp and Voltage	-20		20	ppm
ESR	Equivalent series resistance			60	Ω
Load cap	Load capacitance range	5		10	pF

Table 30 40 MHz crystal specifications**4.4.1.3 32MHz RC Oscillator****Applications**

- Used for ULP-TA-Subsystem modules
- SoC in start-up state. This clock must be used by the SoC in start-up state while the 40MHz XTAL is starting up. It can be used as reference for the SOC-PLL for initial start-up

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
Fosc	Oscillation Frequency	Trimmed Frequency		31.7		MHz
Fosc_Acc	Accuracy with factory calibrated settings			4	%	
	Accuracy with user calibration					
Tstart	Enable to first clock edge			2.2		us
TIE	Total integrated noise			3.1		ns
Quiescent Current	ON Current From UULP_AVDD			110		uA
Shut Down Current	OFF Current From UULP_AVDD			4.5		nA

Table 31 32MHz RC Electrical Specifications

4.4.2 SDIO 2.0 Slave

4.4.2.1 Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{sdio}	SDIO_CLK	-	-	25	MHz
T _s	SDIO_DATA, input setup time	4	-	-	ns
T _h	SDIO_DATA, input hold time	1	-	-	ns
T _{od}	SDIO_DATA, clock to output delay	-	-	13	ns
C _L	Output Load	5	-	10	pF

Table 32 AC Characteristics - SDIO 2.0 Slave Full Speed Mode

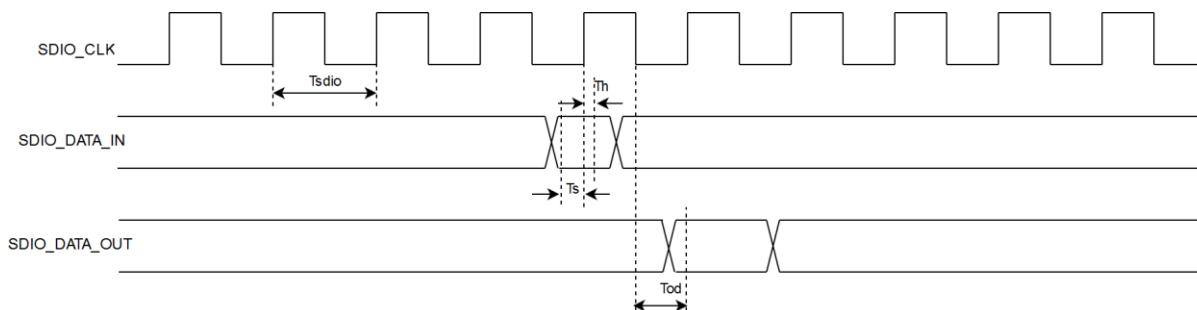


Figure 17 Interface Timing Diagram for SDIO 2.0 Slave Full Speed Mode

4.4.2.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{sdio}	SDIO_CLK	25	-	50	MHz
T _s	SDIO_DATA, input setup time	4	-	-	ns
T _h	SDIO_DATA, input hold time	1	-	-	ns
T _{od}	SDIO_DATA, clock to output delay	2.5	-	13	ns
C _L	Output Load	5	-	10	pF

Table 33 AC Characteristics - SDIO 2.0 Slave High Speed Mode

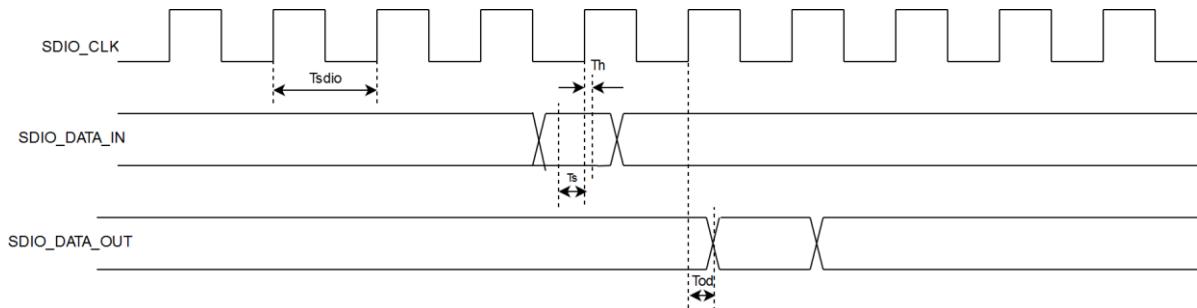


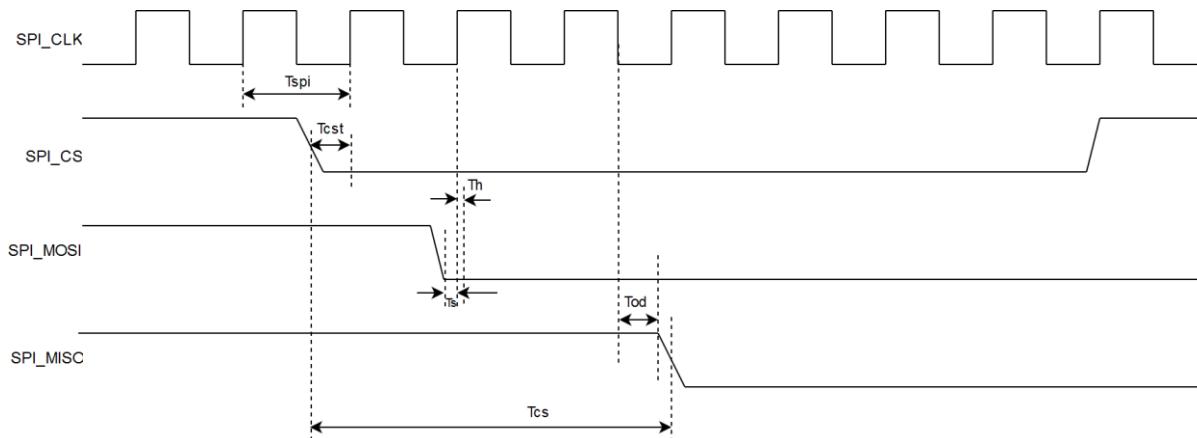
Figure 18 Interface Timing Diagram for SDIO 2.0 Slave High Speed Mode

4.4.3 SPI Slave

4.4.3.1 Low Speed Mode

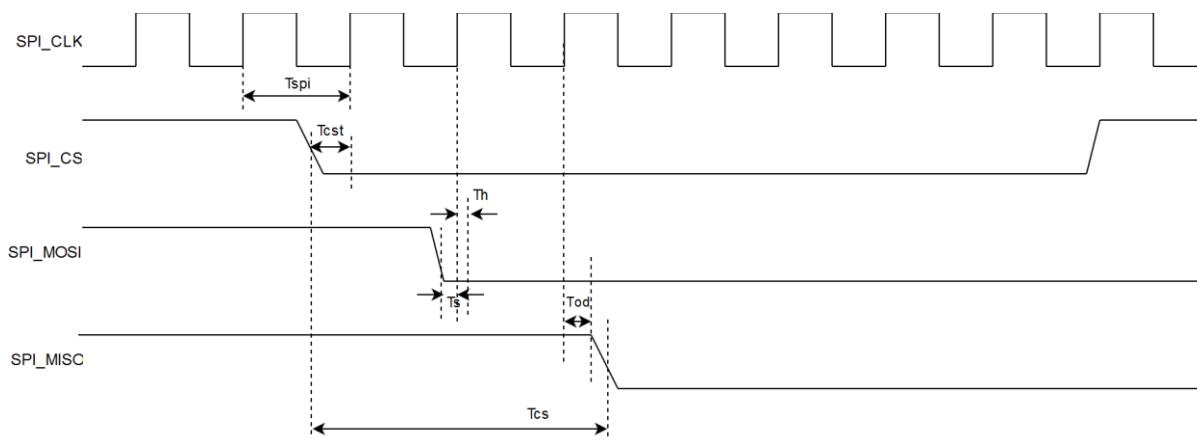
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{spi}	SPI_CLK	0	-	25	MHz

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{cs}	SPI_CS to output delay	-	-	7.5	ns
T _{cst}	SPI CS to input setup time	4.5	-	-	-
T _s	SPI_MOSI, input setup time	1.33	-	-	ns
T _h	SPI_MOSI, input hold time	1.2	-	-	ns
T _{od}	SPI_MISO, clock to output delay	-	-	8.75	ns
C _L	Output Load	5	-	10	pF

Table 34 AC Characteristics - SPI Slave Low Speed Mode**Figure 19 Interface Timing Diagram for SPI Slave Low Speed Mode**

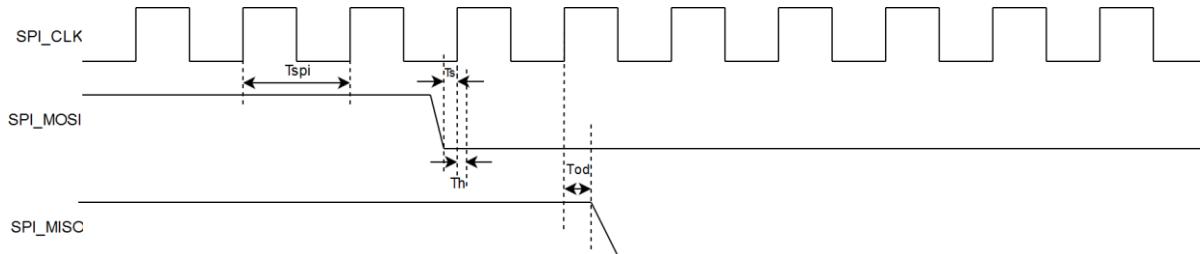
4.4.3.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{spi}	SPI_CLK	25	-	80	MHz
T _{cs}	SPI_CS to output delay	-	-	7.5	ns
T _{cst}	SPI CS to input setup time	4.5	-	-	-
T _s	SPI_MOSI, input setup time	1.33	-	-	ns
T _h	SPI_MOSI, input hold time	1.2	-	-	ns
T _{od}	SPI_MISO, clock to output delay	2.5	-	8.75	ns
C _L	Output Load	5	-	10	pF

Table 35 AC Characteristics - SPI Slave High Speed Mode**Figure 20 Interface Timing Diagram for SPI Slave High Speed Mode**

4.4.3.3 Ultra High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{spi}	SPI_CLK	-	-	100	MHz
T _s	SPI_MOSI, input setup time	1.33	-	-	ns
T _h	SPI_MOSI, input hold time	1.2	-	-	ns
T _{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C _L	Output Load	5	-	10	pF

Table 36 AC Characteristics - SPI Slave Ultra High Speed Mode**Figure 21 Interface Timing Diagram for SPI Slave Ultra High Speed Mode**

4.4.4 USB

4.4.4.1 Low Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _r	Rise Time	75	-	300	ns
T _f	Fall Time	75	-	300	ns
Jitter	Jitter	-	-	10	ns

Table 37 AC Characteristics - USB Low Speed Mode

4.4.4.2 Full Speed Mode

Parameter	Parameter	Min.	Typ.	Max.	Unit
T _r	Rise Time	4	-	20	ns
T _f	Fall Time	4	-	20	ns
Jitter	Jitter	-	-	1	ns

Table 38 AC Characteristics - USB Full Speed Mode

4.4.4.3 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _r	Rise Time	0.5	-	-	ns
T _f	Fall Time	0.5	-	-	ns
Jitter	Jitter	-	-	0.1	ns

Table 39 AC Characteristics - USB High Speed Mode

4.4.5 UART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
Tuart	CLK	0	-	20	MHz
T _{od}	Output delay	0	-	10	ns
T _s	Input setup time	0	-	5	ns
C _L	Output load	5	-	25	pF

Table 40 AC Characteristics - UART

4.4.6 GPIO pins

Parameter	Parameter Description	Condition ns	Min.	Typ.	Max.	Unit
T _{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	2.5	ns
T _{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	2.5	ns
T _{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.3	ns
T _{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.0	ns
T _r	Rise time	Pin configured as input	0.3	-	1.3	ns
T _f	Fall time	Pin configured as input	0.2	-	1.2	ns

Table 41 AC Characteristics - GPIO Pins

4.4.7 Flash Memory

Parameter	Parameter Description	Condition ns	Min.	Typ.	Max.	Unit

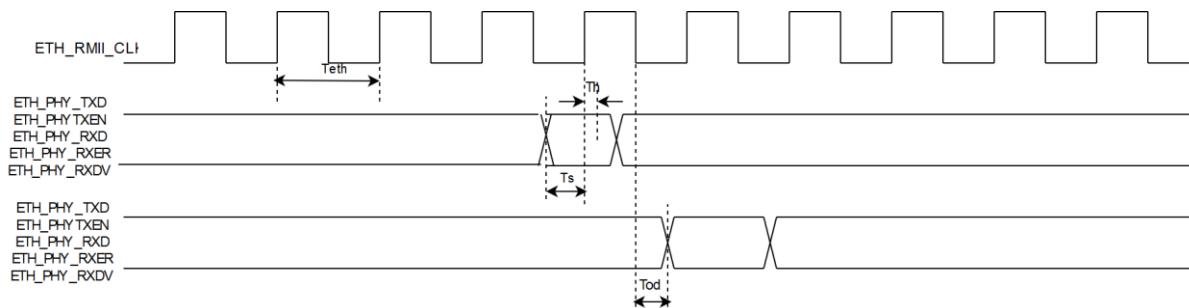
Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
N _{endu}	Endurance	Sector erase/program	10000	-	-	cycles
		Page erase/program, page in large sector	10000	-	-	cycles
		Page erase/program, page in small sector	10000	-	-	cycles
T _{ret}	Retention time	Powered	10	-	-	years
		Unpowered	10	-	-	years
T _{er}	Erase time	Page, sector or multiple consecutive sectors	-	100	-	ms
T _{prog}	Programming time		-	1	-	ms

Table 42 AC Characteristics - Flash Memory

4.4.8 Ethernet

4.4.8.1 RMII Mode

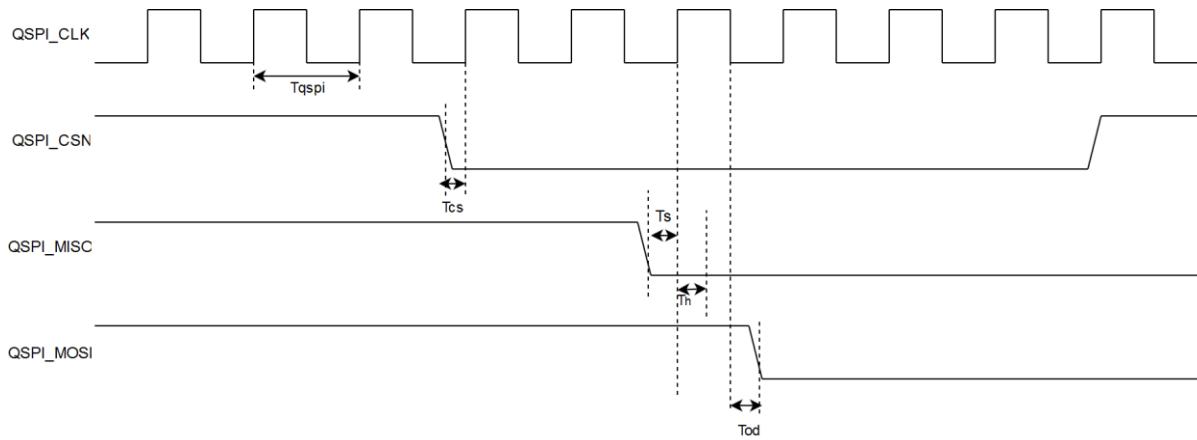
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
F _{eth}	Reference clock frequency	0	-	50	MHz
PPM	Reference clock accuracy	-50	-	+50	-
T _s	setup time (ETH_PHY_TXD_O[3:0], ETH_PHY_TXEN_O, ETH_PHY_RXD_I[3:0], ETH_PHY_RXER_I, ETH_PHY_RXDV_I)	4.05	-	-	ns
T _h	hold time (ETH_PHY_TXD_O[3:0], ETH_PHY_TXEN_O, ETH_PHY_RXD_I[3:0], ETH_PHY_RXER_I, ETH_PHY_RXDV_I)	2	-	-	ns
C _L	Output Load	5	-	10	pF
T _{od}	Output Delay	3	-	14.5	ns
T _r	Output Rise Time(0.8V to 2V)	1	-	5	ns
T _f	Output Fall Time(2V to 0.8V)	1	-	5	ns
D	Duty Cycle	35	-	65	%

Table 43 AC Characteristics - Ethernet RMII Mode**Figure 22 Interface Timing Diagram for Ethernet RMII Mode**

4.4.9 QSPI

4.4.9.1 SDR Full Speed Mode (Rising Edge Sampling)

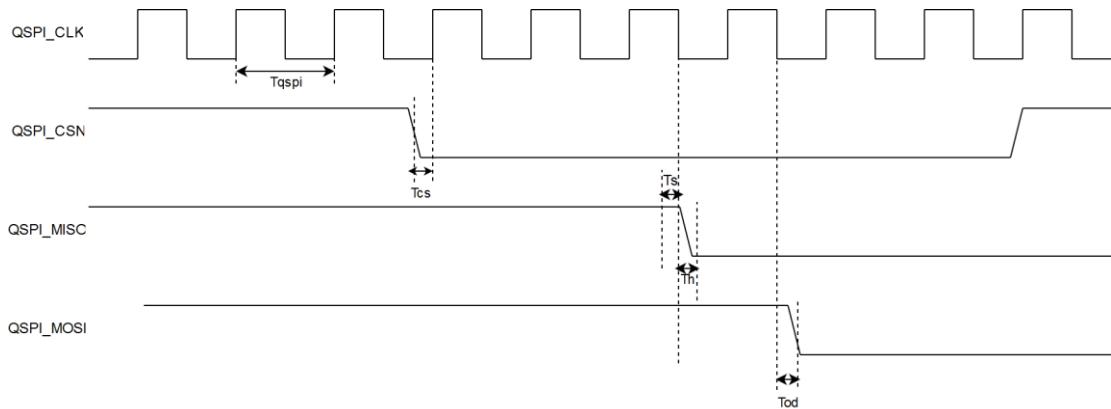
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{qspi}	qspi_clk	0	-	58	MHz
T _{cs}	qspi_cs, to clock edge(this is achieved functionally)	8.6	-	-	ns
T _s	qspi_miso, setup time	1.53	-	-	ns
T _h	qspi_miso, hold time	1.2	-	-	ns
T _{od}	qspi_mosi, clock to output valid	-0.5	-	2.4	ns
C _L	Output Load	5	-	10	pF

Table 44 AC Characteristics - QSPI (GPIO Pins) SDR Full Speed Mode (Rising Edge Sampling)**Figure 23 Interface Timing Diagram for QSPI (GPIO Pins) SDR Full Speed Mode (Rising Edge Sampling)**

4.4.9.2 SDR High Speed Mode (Falling Edge Sampling)

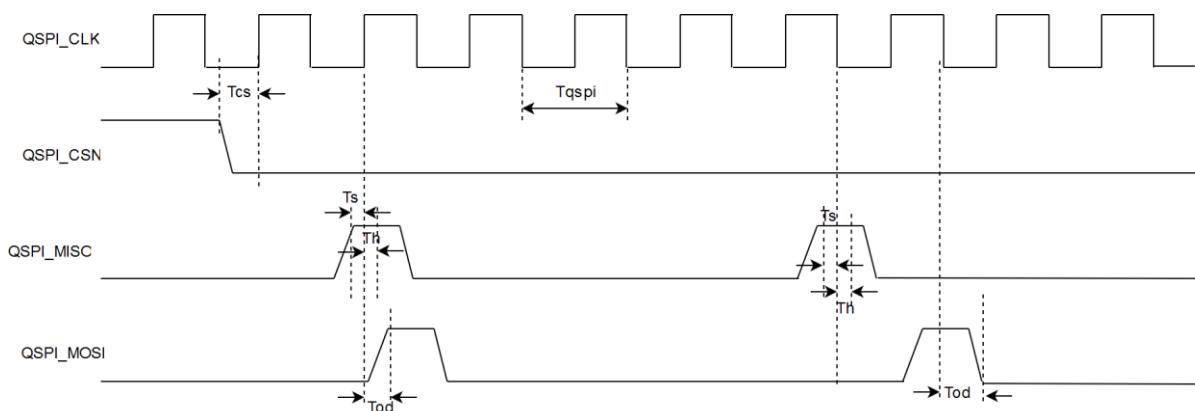
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{qspi}	qspi_clk	0	-	116	MHz
T _{cs}	qspi_cs, to clock edge(this is achieved functionally)	4.3	-	-	ns

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_s	qspi_miso, setup time	1.53	-	-	ns
T_h	qspi_miso, hold time	1.2	-	-	ns
T_{od}	qspi_mosi, clock to output valid	-0.5	-	2.4	ns
C_L	Output Load	5	-	10	pF

Table 45 AC Characteristics - QSPI (GPIO Pins) SDR High Speed Mode (Falling Edge Sampling)**Figure 24 Interface Timing Diagram for QSPI (GPIO Pins) SDR High Speed Mode (Falling Edge Sampling)**

4.4.9.3 DDR Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{qspi}	qspi_clk	0	-	72	MHz
T_{cs}	qspi_cs, to clock edge(this is achieved functionally)	6.2	-	-	ns
T_s	qspi_miso, setup time	1.7	-	-	ns
T_h	qspi_miso, hold time	1	-	-	ns
T_{od}	qspi_mosi, clock to output valid	0.9	-	5.2	ns
C_L	Output Load	5	-	10	pF

Table 46 AC Characteristics - QSPI (GPIO Pins) DDR Mode**Figure 25 Interface Timing Diagram for QSPI (GPIO Pins) DDR Mode**

4.4.10 I2C Master and Slave

4.4.10.1 Fast Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{i2c}	SCL	100	-	400	KHz
T _{low}	clock low period	1.3	-	-	us
T _{high}	clock high period	0.6	-	-	us
T _{sstart}	start condition, setup time	0.6	-	-	us
T _{hstart}	start condition, hold time	0.6	-	-	us
T _s	data, setup time	100	-	-	ns
T _{sstop}	stop condition, setup time	0.6	-	-	us
C _L	Output Load	5	-	10	pF

Table 47 AC Characteristics - I2C Fast Speed Mode

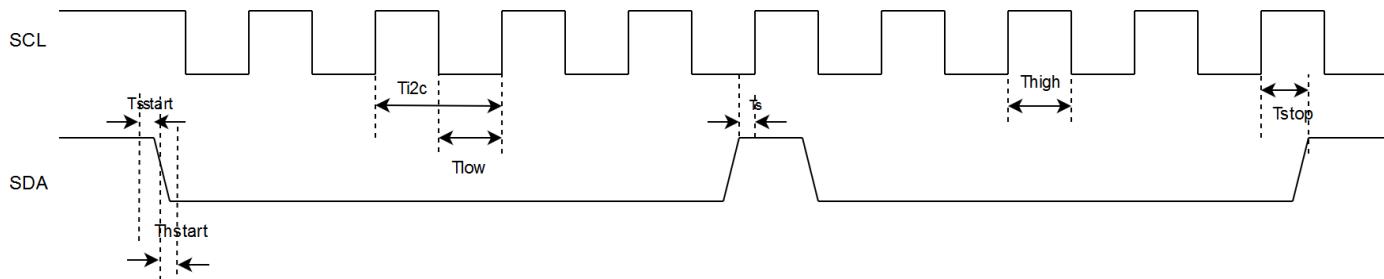
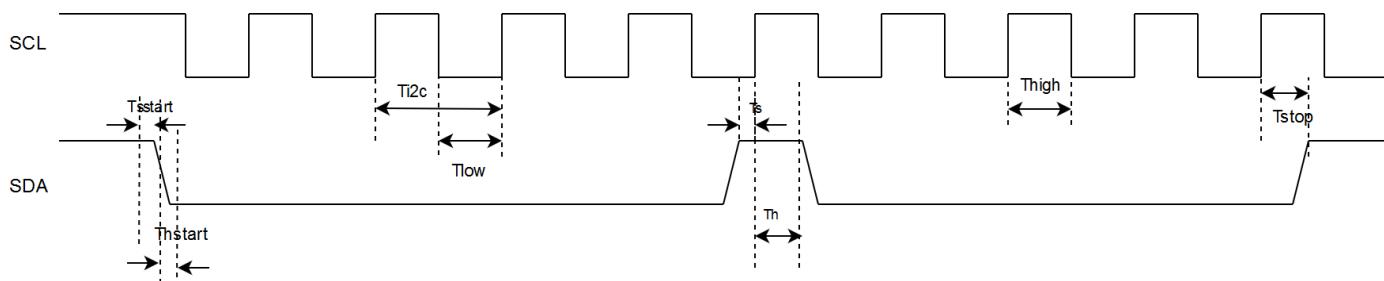


Figure 26 Interface Timing Diagram for I2C Fast Speed Mode

4.4.10.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{i2c}	SCL	0.4	-	3.4	MHz
T _{low}	clock low period	160	-	-	ns
T _{high}	clock high period	60	-	-	ns
T _{sstart}	start condition, setup time	160	-	-	ns
T _{hstart}	start condition, hold time	160	-	-	ns
T _s	data, setup time	10	-	-	ns
T _h	data, hold time	0	-	70	ns
T _{sstop}	stop condition, setup time	160	-	-	ns
C _L	Output Load	5	-	10	pF

Table 48 AC Characteristics - I2C High Speed Mode

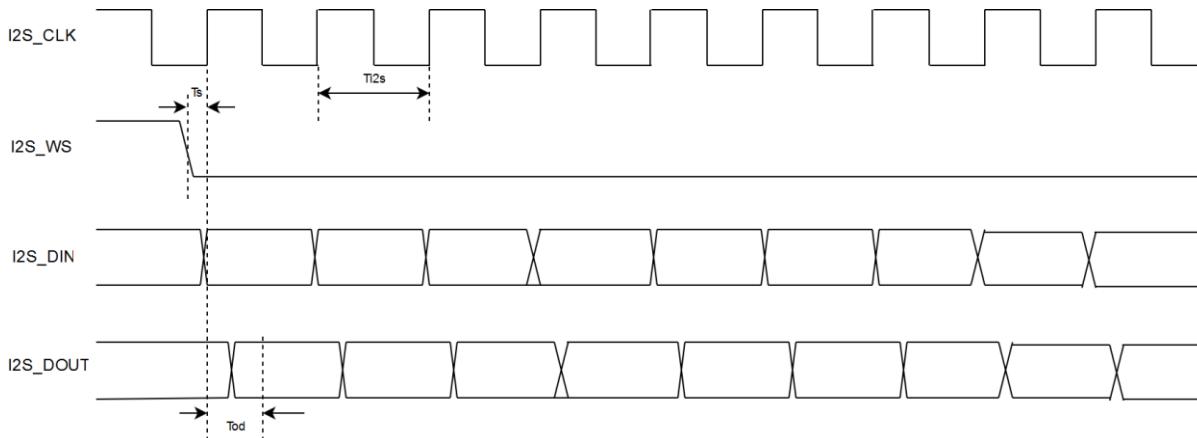
**Figure 27 Interface Timing Diagram for I2C High Speed Mode**

4.4.11 I2S/PCM Master and Slave

4.4.11.1 Master Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

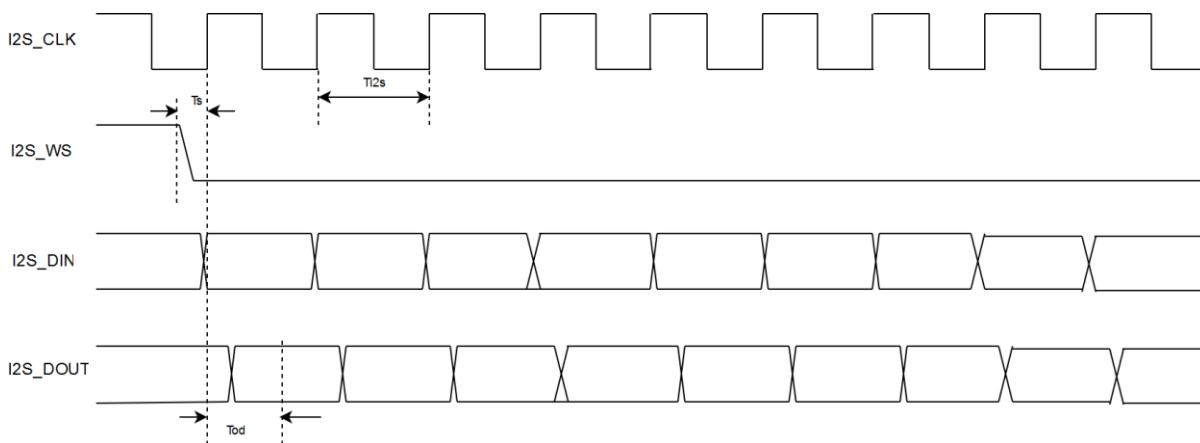
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
Ti2s	i2s_clk	0	-	25	MHz
T _s	i2s_din,i2s_ws setup time	10	-	-	ns
T _h	i2s_din,i2s_ws hold time	0	-	-	ns
T _{od}	i2s_dout output delay	0	-	12	ns
C _L	i2s_dout output load	5	-	10	pF

Table 49 AC Characteristics - I2S/PCM Master Mode**Figure 28 Interface Timing Diagram for I2S Master Mode**

4.4.11.2 Slave Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
Ti2s	i2s_clk	0	-	25	MHz
T _s	i2s_din,i2s_ws setup time	8	-	-	ns
T _h	i2s_din,i2s_ws hold time	0	-	-	ns
T _{od}	i2s_dout output delay	0	-	17	ns
C _L	i2s_dout output load	5	-	10	pF

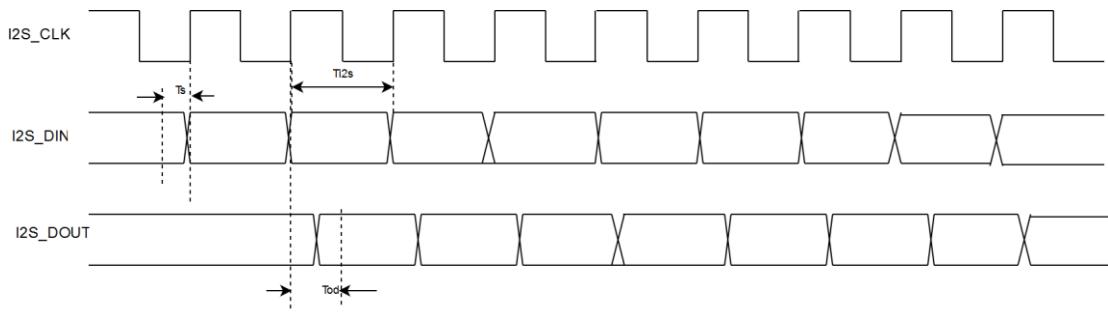
Table 50 AC Characteristics - I2S/PCM Slave Mode**Figure 29 Interface Timing Diagram for I2S Slave Mode**

4.4.12 ULP I2S/PCM Master and Slave

4.4.12.1 Master Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	20	MHz
T_s	i2s_din,i2s_ws setup time w.r.t negedge	15	-	-	ns
T_h	i2s_din,i2s_ws hold time w.r.t negedge	0	-	-	ns
T_{od}	i2s_dout output delay	0	-	15	ns
C_L	i2s_dout output load	5	-	10	pF

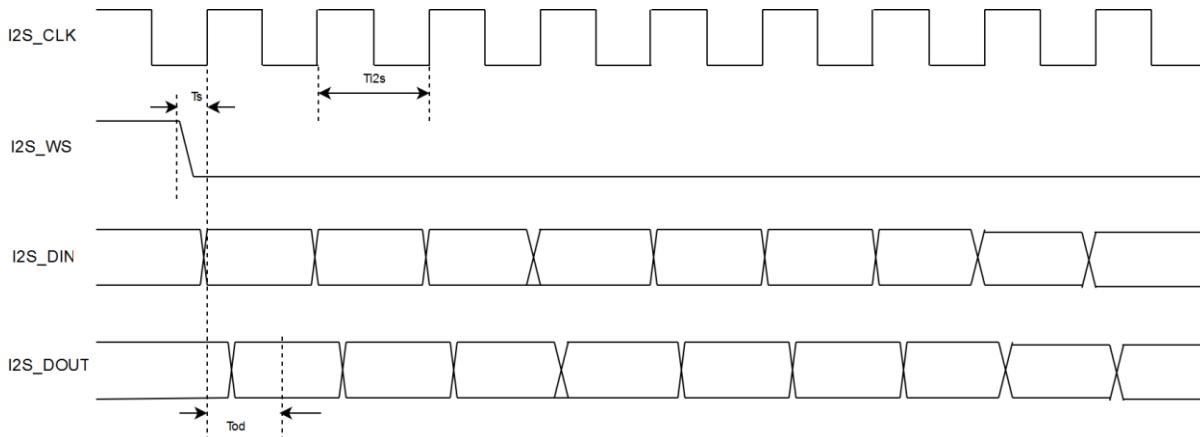
Table 51 AC Characteristics – ULP I2S/PCM Master Mode**Figure 30 Interface timing Diagram for ULP I2S/PCM Master**

4.4.12.2 Slave Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	20	MHz
T_s	i2s_din,i2s_ws setup time w.r.t negedge	5	-	-	ns
T_h	i2s_din,i2s_ws hold time w.r.t negedge	0	-	-	ns

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{od}	i2s_dout output delay	0	-	20	ns
C _L	i2s_dout output load	5	-	10	pF

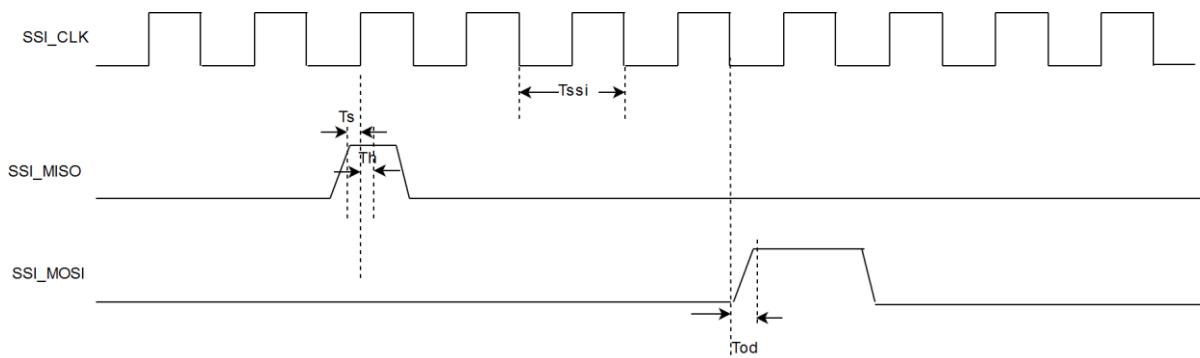
Table 52 AC Characteristics - ULP I2S/PCM Slave Mode**Figure 31 Interface Timing Diagram for ULPI2S Slave**

4.4.13 SSI Master/Slave

4.4.13.1 Master Full Speed Mode

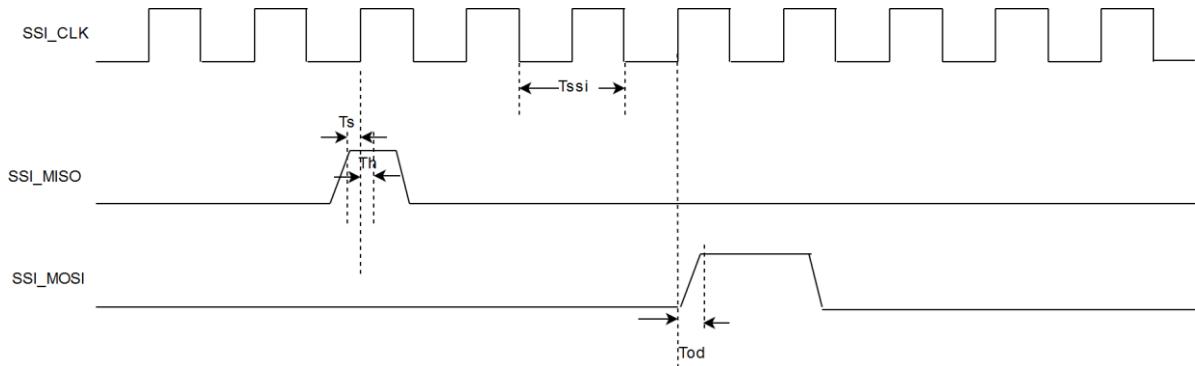
Negedge driving and posedge sampling

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{ssi}	SSI_CLK	0	-	20	MHz
T _s	SSI_MISO, input setup time	17	-	-	ns
T _h	SSI_MISO, input hold time	0	-	-	ns
T _{od}	SSI_CS, SSI莫斯, clock to output valid	0	-	16	ns
C _L	Output Load	5	-	10	pF

Table 53 AC Characteristics - SSI Master Full Speed Mode**Figure 32 Interface Timing Diagram for SSI Master Full Speed Mode**

4.4.13.2 Master High Speed Mode

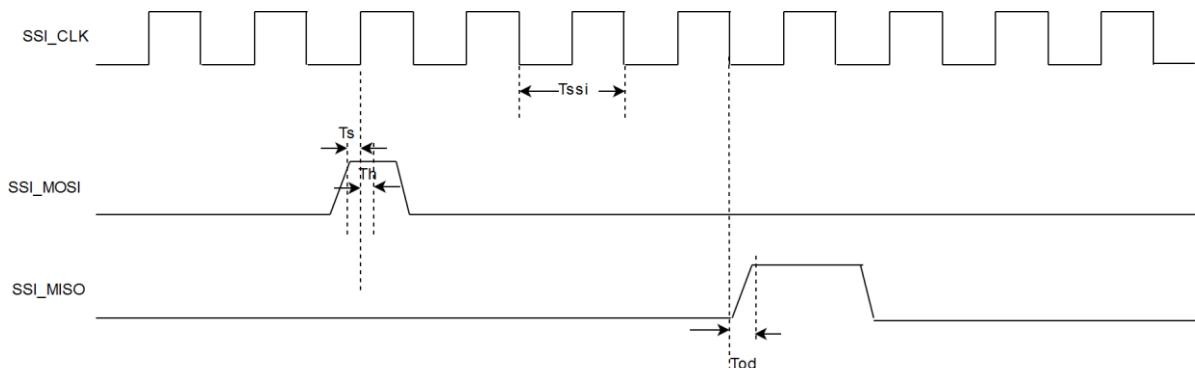
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{ssi}	SSI_CLK	0	-	40	MHz
T _s	SSI_MISO, input setup time	17	-	-	ns
T _h	SSI_MISO, input hold time	2	-	-	ns
T _{od}	SSI_CS,SSI_MOSI, clock to output valid	1	-	16	ns
C _L	Output Load	5	-	10	pF

Table 54 AC Characteristics - SSI Master High Speed Mode**Figure 33 Interface Timing Diagram for SSI Master**

4.4.13.3 Slave Full Speed Mode

Negedge driving and posedge sampling

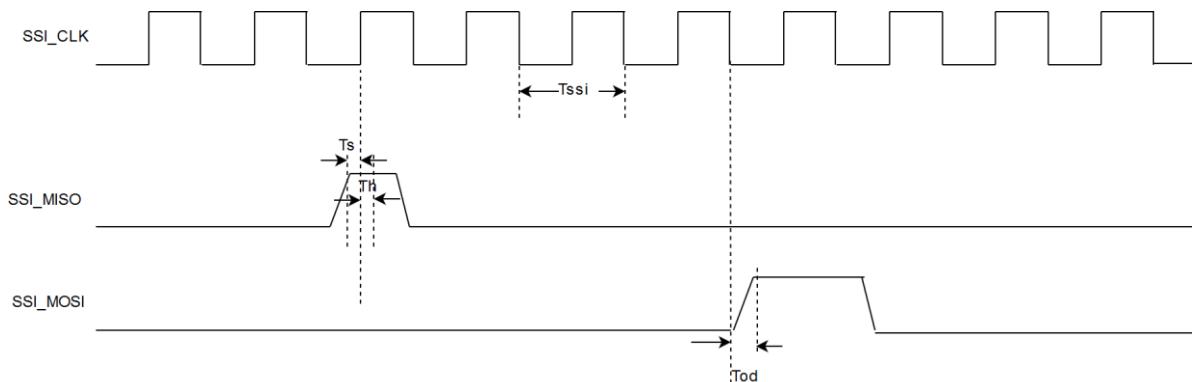
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{ssi}	SSI_CLK	0	-	20	MHz
T _s	SSI_MOSI,CS, input setup time	20	-	-	ns
T _h	SSI_MOSI, input hold time	0	-	-	ns
T _{od}	SSI_MISO, clock to output delay	-	-	24	ns
C _L	Output Load	5	-	10	pF

Table 55 AC Characteristics - SSI Slave Full Speed Mode**Figure 34 Interface Timing Diagram for SSI Slave Full Speed Mode**

4.4.14 ULP SSI Master

4.4.14.1 Master Full Speed Mode
Negedge driving and posedge sampling

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{ssi}	SSI_CLK	0	-	10	MHz
T _s	SSI_MISO, input setup time	20	-	-	ns
T _h	SSI_MISO, input hold time	0	-	-	ns
T _{od}	SSI_CS, SSI莫斯, clock to output valid	0	-	25	ns
C _L	Output Load	5	-	10	pF

Table 56 AC Characteristics - ULP SSI Master Full Speed Mode**Figure 35 Interface Timing Diagram for ULPSSI -- Full Speed Mode**

4.4.15 GPIO/MC-PWM/QEI/SCT Timer/SIO Interfaces

Paramter	Parameter Description	Min.	Typ.	Max.	Unit
T _{sct}	CLK	0	-	10	MHz
T _{od}	Output delay	0	-	20	ns
T _s	Input setup time	0	-	10	ns
C _L	Output load	5	-	10	pF

Table 57 AC Characteristics – GPIO/PWM/QEI

4.4.16 USART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{usart}	Interface CLK	0	-	20	MHz
T _{od}	Clock to Output delay	0	-	20	ns
T _s	Input setup time	0	-	10	ns
C _L	Output load	5	-	10	pF

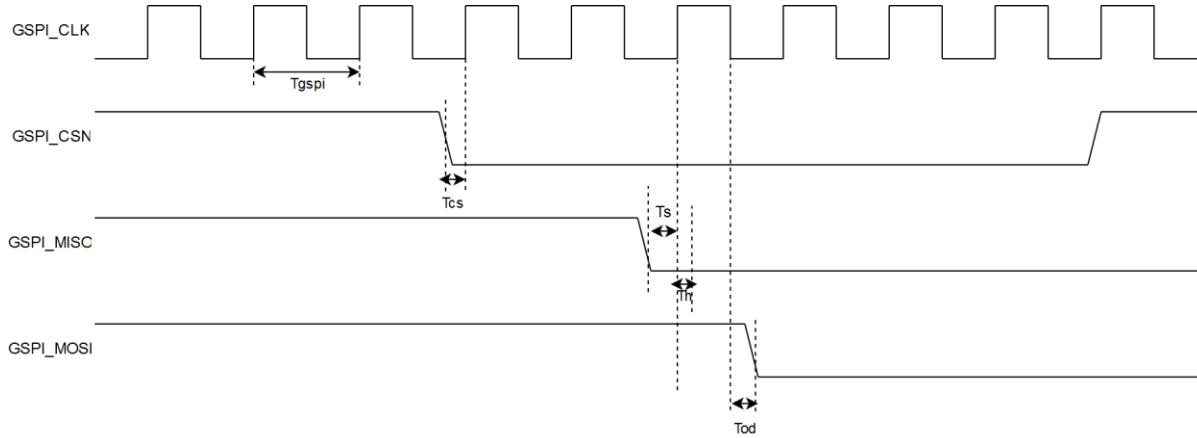
Table 58 AC Characteristics - USART

4.4.17 GSPI Master

4.4.17.1 Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit

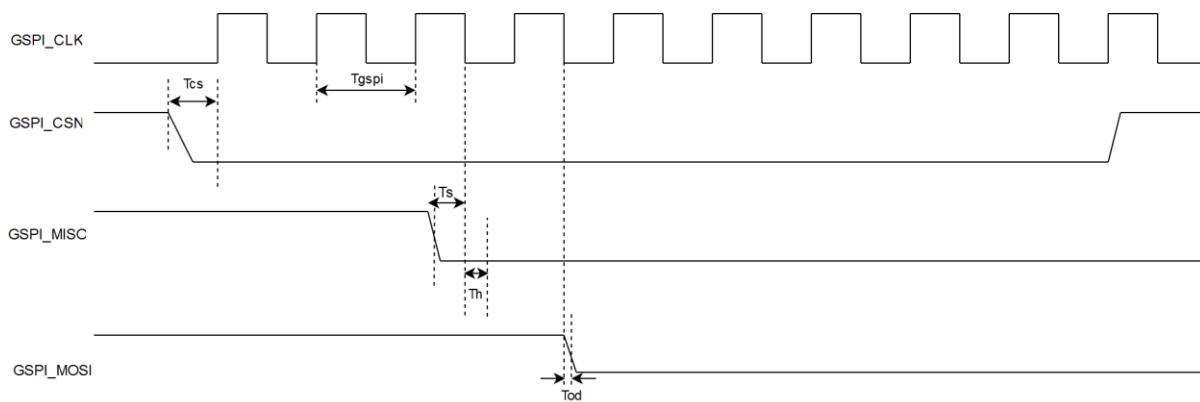
Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{gspi}	gspi_clk	0	-	58	MHz
T _{cs}	gspi_cs, to clock edge(this is achieved functionally)	4.16	-	-	ns
T _s	gspi_miso, setup time	1.66	-	-	ns
T _h	gspi_miso, hold time	1.2	-	-	ns
T _{od}	gspi_cs, gspi_mosi, clock to output valid	1	-	7.33	ns
C _L	Output Load	5	-	10	pF

Table 59 AC Characteristics - GSPI Master Full Speed Mode**Figure 36 Interface Timing Diagram for GSPI Master Full Speed Mode**

4.4.17.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{gspi}	gspi_clk	0	-	116	MHz
T _{cs}	gspi_cs, to clock edge(this is achieved functionally)	4.16	-	-	ns
T _s	gspi_miso, setup time	1.66	-	-	ns
T _h	gspi_miso, hold time	1.2	-	-	ns
T _{od}	gspi_cs, gspi_mosi, clock to output valid	1	-	7.33	ns
C _L	Output Load	5	-	10	pF

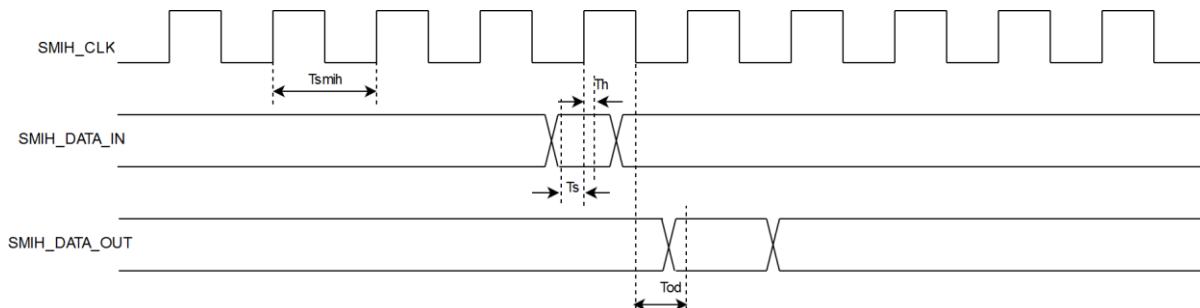
Table 60 AC Characteristics - GSPI Master High Speed Mode

**Figure 37 Interface Timing Diagram for GSPI Master High Speed Mode****4.4.18 CAN interface**

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{can}	Interface CLK	0	-	10	MHz
T _{od}	Clock to Output delay	0	-	20	ns
T _s	Input setup time	0	-	10	ns
C _L	Output load	5	-	10	pF

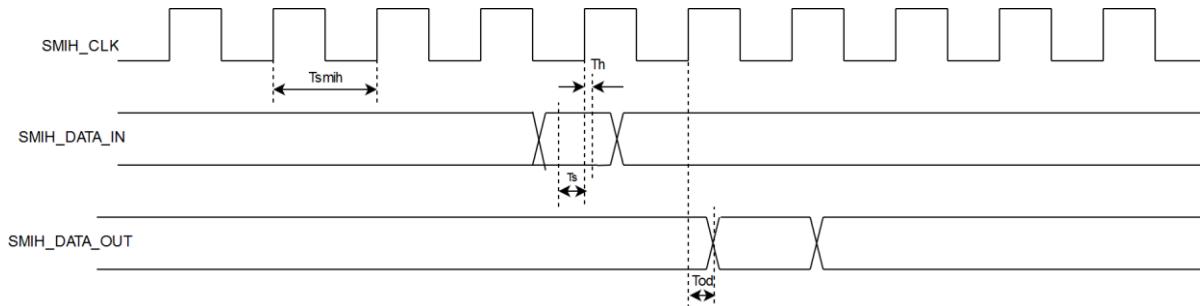
Table 61 AC Characteristics - CAN Interface**4.4.19 SD Memory Host Controller****4.4.19.1 SDR Full Speed Mode**

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{smih}	SMIH_CLK	-	-	26	MHz
T _s	SMIH_DATA, input to setup time	6	-	-	ns
T _h	SMIH_DATA , input to hold time	2	-	-	ns
T _{od}	SMIH_DATA , clock to output delay	0	-	14	ns
C _L	Output Load	5	-	10	pF
	Voltage	-	1.8/3.3	-	V

Table 62 AC Characteristics - SD Memory Host Controller SDR Full Speed Mode**Figure 38 Interface Timing Diagram for SMIH - Full Speed Mode**

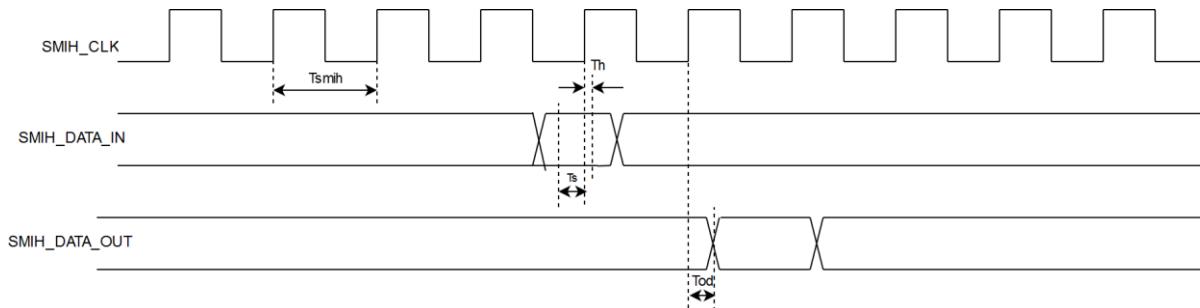
4.4.19.2 SDR High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{smih}	SMIH_CLK	26	-	52	MHz
T _s	SMIH_DATA, input to setup time	6	-	-	ns
T _h	SMIH_DATA , input to hold time	2	-	-	ns
T _{od}	SMIH_DATA , clock to output delay	2.45	-	14	ns
C _L	Output Load	5	-	10	pF
	Voltage	-	1.8/3.3	-	V

Table 63 AC Characteristics - SD Memory Host Controller SDR High Speed Mode**Figure 39 Interface Timing Diagram for SMIH High Speed Mode**

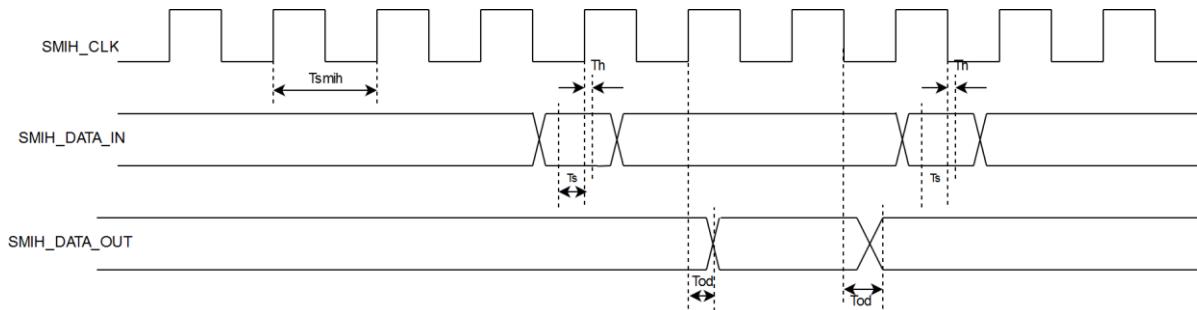
4.4.19.3 SDR Ultra High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{smih}	SMIH_CLK	52	-	80	MHz
T _s	SMIH_DATA, input setup time (w.r.t input clock)	3	-	-	ns
T _h	SMIH_DATA, input hold time	0.8	-	-	ns
T _{od}	SMIH_DATA, clock to output delay	1.25	-	7.5	ns
C _L	Output Load	5	-	10	pF
VDDIO	Power supply to IO domain	1.65	1.8	1.98	V

Table 64 AC Characteristics - SD Memory Host Controller SDR Ultra High Speed Mode**Figure 40 Interface Timing Diagram for SMIH -Ultra High Speed Mode**

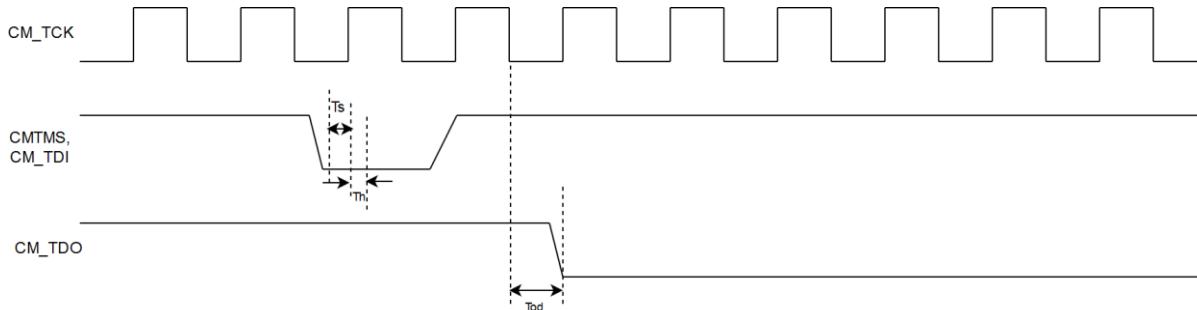
4.4.19.4 DDR Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{smih}	SMIH_CLK	0	-	40	MHz
T _s	SMIH_DATA, input setup time (w.r.t input clock)	5	-	-	ns
T _h	SMIH_DATA, input hold time	0.8	-	-	ns
T _{od}	SMIH_DATA, clock to output delay	1.25	-	7	ns
C _L	Output Load	5	-	10	pF
VDDIO	Power supply to IO domain	1.65	1.8	1.98	V

Table 65 AC Characteristics - SD Memory Host Controller DDR Mode**Figure 41 Interface Timing Diagram for SMIH/MMC DDR Mode**

4.4.20 Cortex-M4F JTAG

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{tck}	TCK period	-	-	20	MHz
T _s	Setup	5	-	-	ns
T _h	Hold	4	-	-	ns
T _{od}	Output Delay	0	-	38.5	ns
C _L	Output Load	5	-	10	pF

Table 66 AC Characteristics - Cortex-M4F JTAG**Figure 42 Interface Timing Diagram for Cortex-M4F JTAG**

4.4.21 Cortex-M4F Trace

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T _{trace}	TRACECLK Period	0	-	100	MHz
T _{od}	Output Delay	0.8	-	8	ns
C _L	Output Load	5	-	10	pF

Table 67 AC Characteristics - Cortex-M4F Trace

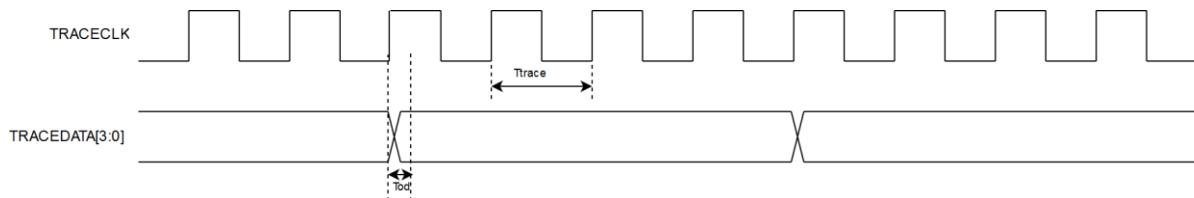


Figure 43 Interface Timing Diagram for Cortex-M4F Trace

4.5 Analog Peripherals

The following analog peripherals are available

- 2x Analog Comparators
- 3x General purpose Op-Amp
- 16 channel, 12 bit, 5 MSPS Analog to Digital Converter with both single ended and differential modes
- 10 bit, 5 MSPS Digital to Analog Converter

4.5.1 Analog Comparators

Analog comparator is a peripheral circuit that compares two analog voltage inputs and gives a logical output based on comparison.

There are 9 different inputs for each pin of comparator, and 2 of the 9 are external pin inputs.

The following cases of comparison are possible

1. Compare external pin inputs
2. Compare external pin input to internal voltages.
3. Compare internal voltages.

The comparator compares inputs p and n to produce an output, cmp_out.

$$p > n, \text{cmp_out} = 1$$

$$p < n, \text{cmp_out} = 0$$

Analog Peripherals consists of 2 comparators whose inputs can be programmed independently. The reference buffer and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
T _{d_comp}	Delay of the comparator	100mV overdrive		60	115	ns
T _{resp_comp}	The time delay from enable to output of comparator			0.3		us
V _{ref}	Programmable voltage reference range		0.1		1.1	V

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V _{ref_step}	Programmable voltage reference step size			0.1		V
T _{set_buffer}	Settling time of voltage reference buffer			0.7		us
V _{os_comp}	The minimum voltage difference required between inputs to make output high	Typical value corresponds to 1-sigma variation		1.4		mV
V _{hyst_comp}	Hysteresis = 2'd1			60		mV
	Hysteresis = 2'd3			90		mV
ICMR_comp	Input common-mode range		0		ULP_IO_VD D-0.2	V
I _{q_comp}	Current consumption on VBATT with all blocks enabled, Sampling rate = 32KHz			70		uA
I _{q_1KSPS}	Current consumption @1KSPS (on time =2us, off time=998us)			0.25		uA

Table 68 Analog Comparator Electrical Specifications

4.5.2 Auxiliary (AUX) LDO

This LDO generates AUX_AVDD which is programmable from 1.6V to 2.8V. The LDO supports a maximum load current of 25mA with a dropout voltage of 300mV. It is an external compensated LDO which is stable for load currents ranging from 0 to 25mA, with the load cap of 1uF. AUX_AVDD is also used as reference to the ADC and DAC.

Paramater	Parameter Description	Conditions	Min	Typ	Max	Units
V _{out}	Output voltage range		1.6		2.8	V
V _{step}	Output voltage programmable step size			80		mV
V _{drop}	Dropout voltage			0.3		V
I _{load}	Load current capability				25	mA
I _q	Quiescent current			80		μA
I _{bypass}	LDO current in Bypass mode			5		nA
T _{startup}	Time taken for V _{out} to reach 95% of its stable value when a step enable is given to the LDO			30		us

Table 69 AUX LDO Electrical Specifications

4.5.3 Analog to Digital Converter

- 12 bit precision ADC
- Single ended mode and differential mode configuration
- Typical current consumption at 5 MSPS is 2.5mA.
- Two clock latency

Parameter	Parameter Description	Conditions	Min	Typ.	Max	Units
N	Resolution of ADC			12		bits

Parameter	Parameter Description	Conditions	Min	Typ.	Max	Units
N _{channel}	Number of channels – Single ended Mode			16		-
	Number of channels – Differential Mode					
f _{ADC}	ADC sampling and input clock frequency			5		MHz
V _{AIN}	Input voltage range – Single ended Mode		0	AUX_AVDD	V	
	Differential Input voltage range – Differential Mode		0			
R _{in}	Input resistance	Single Channel input conversion		100		KΩ
C _{sampled}	ADC internal sample and hold capacitor			3		pF
C _{fixed}	Fixed capacitance from multiplexers and ESD protection			2		pF
t _s	Sampling time		0.1			uS
t _{start}	Power up time			40		us
G _{err}	Gain Error		-2		2	%
Offset	Offset		-2		2	mV
DNL	Differential nonlinearity			1		LSB
INL	Integral nonlinearity			1.5		LSB
ENOB	Effective number of bits			10.5		bits
SNDR	Signal to noise and distortion ratio			63		dB
I _{active}	Input frequency 100kHz at 5Msps			1.5		mA

Table 70 ADC Electrical Specifications

4.5.4 Digital to Analog Convertor

- 10 bit precision DAC
- Single ended voltage outputs
- 1.8 to 3.6V supply operation.
- Typical current consumption at 5 MSPS is 1mA.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
VOL	Lowest output voltage			0.15*AUX_AVDD		V
VOH	Highest output voltage			0.85*AUX_AVDD		V
R _{load}	Resistive load	Connect to ground	5			KΩ
C _{load}	Load capacitance				50	pF
I _{active}	Average current consumption	Load (50pF, 5 kOhm) at		1.2		mA

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
		AUX_AVDD = 3.3V				
DNL	Differential nonlinearity			1		LSB
INL	Integral nonlinearity			1		LSB
SNDR	At an input frequency of 100kHz and sampling frequency of 5MHz			54		dB
ENOB	At an input frequency of 100kHz and sampling frequency of 5MHz			9		bits
t_settling	Settling time when input code changes from min to max value			100		ns
t_start	Startup Time from OFF state		2.4	2.6	2.9	us

Table 71 DAC Electrical Specifications

4.5.5 Op-Amp

There are 3 general purpose Operational Amplifiers (Op-Amps) offering rail-to-rail inputs and outputs. The Op-Amps can be configured as:

1. Unity gain amplifier
2. Trans-Impedance Amplifier (TIA)
3. Non-inverting Programmable Gain Amplifier (PGA)
4. Inverting Programmable Gain Amplifier (PGA)
5. Non-inverting Programmable hysteresis comparator
6. Inverting Programmable hysteresis comparator
7. Cascaded Non-Inverting PGA
8. Cascaded Inverting PGA
9. Two Op-Amps Differential Amplifier
10. Instrumentation Amplifier

- In the above list, #7, #8, #9 are configured by cascading 2 Op-Amps
- In the above list, #10 is configured by cascading 3 Op-Amps

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V _{in}	Input Voltage range		0		AUX_AVDD	V
V _{out}	output voltage range	1mA, source or sink	0.1		AUX_AVDD - 0.1	V
I _{out}	output current capability, source or sink	0.5 < Vout < AUX_AVDD-0.5			3	mA
e _n	Output integrated noise (1Hz to 1MHz) (UGB mode)	power mode = high C _L =50pF		35		uVrms
		power mode = low C _L =50pF		40		uVrms

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
V_{os}	Input offset voltage (1 sigma)	power mode = high $C_L=50\text{pF}$		1.9		mV
		power mode = low $C_L=50\text{pF}$		1.7		mV
Ge1	Gain error, unity gain buffer mode, $RL=1\text{Kohm}$	power mode = high $C_L=50\text{pF}$		1		%
		power mode = low $C_L=50\text{pF}$		1		%
PM	Phase margin, in UGB mode	power mode = high $C_L=50\text{pF}$		59		°C
		power mode = low $C_L=50\text{pF}$		63		°C
GBW	Gain-bandwidth product	power mode = high $C_L=50\text{pF}$		17		MHz
		power mode = low $C_L=50\text{pF}$		7.5		MHz
T _{start}	Startup time	power mode = high $C_L=50\text{pF}$		0.5		us
		power mode = low $C_L=50\text{pF}$		0.9		us
THD_UGB	Total Harmonic Distortion, at 100KHz (UGB mode)	power mode = high $C_L=50\text{pF}$		-50		dB
		power mode = low $C_L=50\text{pF}$		-48		dB
THD	Total Harmonic Distortion, at 10KHz (Non inv amp mode, gain = 51)	power mode = high $C_L=50\text{pF}$		-58		dB
		power mode = low $C_L=50\text{pF}$		-56		dB
PSRR	DC Power supply rejection ratio	power mode = high $C_L=50\text{pF}$		84		dB
		power mode = low $C_L=50\text{pF}$		96		dB
CMRR	DC Common mode rejection ratio	power mode = high $C_L=50\text{pF}$		70		dB
		power mode = low $C_L=50\text{pF}$		71		dB
Idd	Quiescent current - 1 Op-Amp	power mode = high $C_L=50\text{pF}$		0.95		mA
		power mode = low $C_L=50\text{pF}$		315		uA
SR	Slew Rate	power mode = high $C_L=50\text{pF}$		60		V/us
		power mode = low $C_L=50\text{pF}$		20		V/us

Table 72 Opamp Electrical Specifications

4.5.6 Temperature Sensor

- Consists of RO based and BJT based temp sensor.
- Generates PTAT Voltage from BJT based band gap.
- Buffered PTAT voltage is given at ADC Input.
- Output of the ADC is linear function of temperature.
- Generates Temperature dependent and independent clock
- Digital logic to convert the output clock to temperature

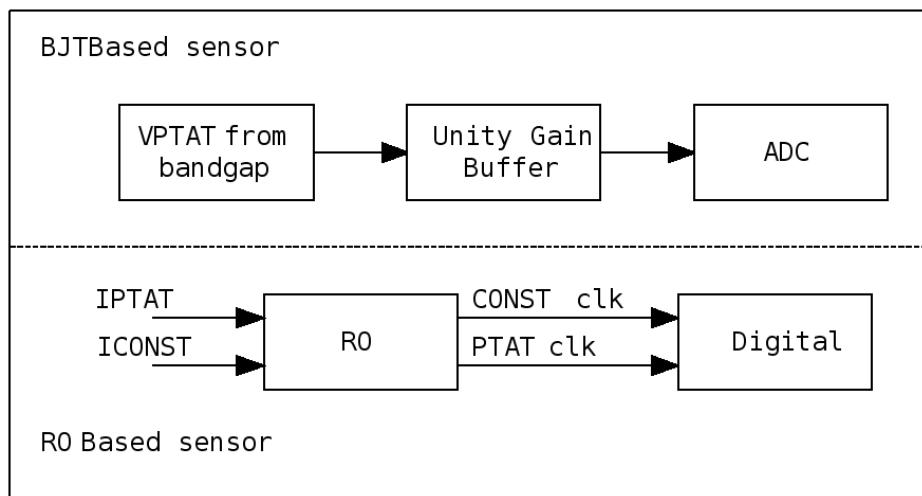


Figure 44 Temperature Sensors

The BJT based sensor works for temperature range from -40°C to 125°C and AUX_VDD voltage variation from 1.8V to 3.6V. It outputs the digital word having a resolution of nearly 1°C. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor. Typically, the block consumes 110uA of current and leakage current is 800pA.

The RO based sensor will output 2 clocks i.e. one varies linearly with temperature and other is independent of temperature. The PTAT clock cycles are counted in the fixed duration set by the other constant clock and this count value is proportional to the temperature. Current consumption of RO based sensor is 5uA and leakage of nearly 1.15nA.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
Accuracy				5		°C
T _{start}	Startup time			2.5		us
I _q	Quiescent current			105		uA

Table 73 BJT Based Temperature Sensor Electrical Specifications

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
T _{start}	Startup time			20		us
Accuracy	Maximum variation in F2/F1 across corners. Report at	T = -40°C to 85°C T = -40°C to 120°C		5 12		°C

Parameter	Parameter Description	Conditions	Min	Typ	Max	Units
I _q	Quiescent current			5		uA

Table 74 RO Based Temperature Sensor Electrical Specifications

4.6 RF Characteristics

In the sub-sections below,

- All WLAN Sensitivity numbers and Adjacent channel numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n data rates.
- For WLAN ACI cases, the desired signal power is 3dB above standard defined sensitivity level.
- For Bluetooth C/I cases, the desired signal power is 3dB above standard defined sensitivity level.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in the Recommended Operating Conditions

4.6.1 WLAN 2.4 GHz Transmitter Characteristics

4.6.1.1 Transmitter characteristics with 3.3V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port on channel 6 (2437 MHz)⁽¹⁾

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	DSSS - 1 Mbps	EVM< -9 dB	-	17.5	-	dBm
	DSSS - 2 Mbps	EVM< -9 dB	-	17.5	-	dBm
	CCK- 5.5 Mbps	EVM< -9 dB	-	17.5	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	17.5	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	17.5	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	17.5	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	17.5	-	dBm
	OFDM - 18 Mbps	EVM< -13 dB	-	17.5	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	17	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	17	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	17	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	15	-	dBm
	MCS0 Mixed Mode	EVM< -5 dB	-	17.5	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	17.5	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	17.5	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	17.5	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 40MHz Bandwidth, compliant with IEEE mask and EVM	MCS4 Mixed Mode	EVM< -19 dB	-	16	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	15.5	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB	-	15	-	dBm
	MCS7 Mixed Mode	EVM< -27 dB	-	12	-	dBm
Transmitter Emissions (6 Mbps @ Maximum Power)	MCS0 Mixed Mode	EVM< -5 dB	-	10.5	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	10.5	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	10.5	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	10.5	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	10	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	10.5	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB	-	10.5	-	dBm
	MCS7 Mixed Mode	EVM< -27 dB	-	10	-	dBm
Harmonic Emissions (1 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-148	-	dBm/Hz
	869-960 MHz	CDMAOne, GSM850	-	-158	-	dBm/Hz
	1450-1495 MHz	DAB	-	-151	-	dBm/Hz
	1570-1580 MHz	GPS	-	-151	-	dBm/Hz
	1592-1610 MHz	GLONASS	-	-132	-	dBm/Hz
	1710-1800 MHz	DSC-1800-Uplink	-	-130	-	dBm/Hz
	1805-1880 MHz	GSM 1800	-	-110	-	dBm/Hz
	1850-1910 MHz	GSM 1900	-	-122	-	dBm/Hz
	1910-1930 MHz	TDSCDMA,LTE	-	-135	-	dBm/Hz
	1930-1990 MHz	GSM1900, CDMAOne,WCDMA	-	-130	-	dBm/Hz
	2010-2075 MHz	TDSCDMA	-	-127	-	dBm/Hz
	2110-2170 MHz	WCDMA	-	-119	-	dBm/Hz
	2305-2370 MHz	LTE Band 40	-	-112	-	dBm/Hz
	2370-2400 MHz	LTE Band 40	-	-95	-	dBm/Hz
	2496-2530 MHz	LTE Band 41	-	-102	-	dBm/Hz
	2530-2560 MHz	LTE Band 41	-	-113	-	dBm/Hz
	2570-2690 MHz	LTE Band 41	-	-128	-	dBm/Hz
	5000-5900 MHz	WLAN 5G	-	-148	-	dBm/Hz

Table 75 WLAN 2.4 GHz Transmitter Characteristics (3.3V)

- Up to 2dB variation in power from channel-to-channel. To meet FCC emission limits, edge

channels (1 and 11) have reduced TX power.

4.6.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth ⁽¹⁾	1 Mbps DSSS	-	-96	-	dBm
	2 Mbps DSSS	-	-90	-	dBm
	5.5 Mbps CCK	-	-89	-	dBm
	11 Mbps CCK	-	-86.5	-	dBm
	6 Mbps OFDM	-	-90	-	dBm
	9 Mbps OFDM	-	-90	-	dBm
	12 Mbps OFDM	-	-89	-	dBm
	18 Mbps OFDM	-	-87	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-80	-	dBm
	48 Mbps OFDM	-	-75.5	-	dBm
	54 Mbps OFDM	-	-74	-	dBm
	MCS0 Mixed Mode	-	-89.5	-	dBm
	MCS1 Mixed Mode	-	-87	-	dBm
	MCS2 Mixed Mode	-	-84	-	dBm
	MCS3 Mixed Mode	-	-82	-	dBm
	MCS4 Mixed Mode	-	-78	-	dBm
	MCS5 Mixed Mode	-	-73	-	dBm
	MCS6 Mixed Mode	-	-71	-	dBm
	MCS7 Mixed Mode	-	-70	-	dBm
Sensitivity for 40MHz Bandwidth	MCS0 Mixed Mode	-	-86	-	dBm
	MCS1 Mixed Mode	-	-84	-	dBm
	MCS2 Mixed Mode	-	-81	-	dBm
	MCS3 Mixed Mode	-	-78	-	dBm
	MCS4 Mixed Mode	-	-74	-	dBm
	MCS5 Mixed Mode	-	-70	-	dBm
	MCS6 Mixed Mode	-	-67.5	-	dBm
	MCS7 Mixed Mode	-	-66.5	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
Maximum Input Level for PER below 10%	802.11 b	-	8	-	dBm
	802.11g	-	-10	-	dBm
	802.11n	-	-10	-	dBm
RSSI Accuracy Range		-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-6	-	dBm
	824–849 MHz	-	-5	-	dBm
	880–915 MHz	-	-8	-	dBm
	1710–1785 MHz	-	-21	-	dBm
	1850–1910 MHz	-	-17	-	dBm
	1920–1980 MHz	-	-20	-	dBm
	2300–2400 MHz	-	-58	-	dBm
	2570–2620 MHz	-	-22	-	dBm
	2545–2575 MHz	-	-20	-	dBm
Return Loss		-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS	-	36	-	dB
	11 Mbps DSSS	-	37	-	dB
	6 Mbps OFDM	-	38	-	dB
	54 Mbps OFDM	-	22	-	dB
	MCS0 Mixed Mode	-	38	-	dB
	MCS7 Mixed Mode	-	20	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	44	-	dB
	11 Mbps DSSS	-	35	-	dB
	6 Mbps OFDM	-	46	-	dB
	54 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	46	-	dB
	MCS7 Mixed Mode	-	28	-	dB

Table 76 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

1. Sensitivities for channels 6,7,8 & 11 are up to 2dB worse

4.6.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

Parameter	Condition	Min	Typ	Max	Units
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Parameter	Condition	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth ⁽¹⁾	1 Mbps DSSS	-	-94	-	dBm
	2 Mbps DSSS	-	-87.5	-	dBm
	5.5 Mbps CCK	-	-86.5	-	dBm
	11 Mbps CCK	-	-83.5	-	dBm
	6 Mbps OFDM	-	-87.5	-	dBm
	9 Mbps OFDM	-	-87	-	dBm
	12 Mbps OFDM	-	-86.5	-	dBm
	18 Mbps OFDM	-	-84	-	dBm
	24 Mbps OFDM	-	-81	-	dBm
	36 Mbps OFDM	-	-77	-	dBm
	MCS0 Mixed Mode	-	-87	-	dBm
	MCS1 Mixed Mode	-	-84.5	-	dBm
	MCS2 Mixed Mode	-	-82	-	dBm
	MCS3 Mixed Mode	-	-79	-	dBm
	MCS4 Mixed Mode	-	-75	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	0	-	dBm
	802.11g	-	-10	-	dBm
	802.11n	-	-10	-	dBm
RSSI Accuracy Range		-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-8	-	dBm
	824–849 MHz	-	-8	-	dBm
	880–915 MHz	-	-10	-	dBm
	1710–1785 MHz	-	-16	-	dBm
	1850–1910 MHz	-	-14	-	dBm
	1920–1980 MHz	-	-20	-	dBm
	2300–2400 MHz	-	-55	-	dBm
	2570–2620 MHz	-	-24	-	dBm
	2545–2575 MHz	-	-23	-	dBm
Return Loss		-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS	-	40	-	dB
	11 Mbps DSSS	-	36	-	dB
	6 Mbps OFDM	-	42	-	dB
	36 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	40	-	dB

Parameter	Condition	Min	Typ	Max	Units
Alternate Adjacent Channel Interference	MCS4 Mixed Mode	-	30	-	dB
	1 Mbps DSSS	-	50	-	dB
	11 Mbps DSSS	-	38	-	dB
	6 Mbps OFDM	-	48	-	dB
	36 Mbps OFDM	-	38	-	dB
	MCS0 Mixed Mode	-	48	-	dB
	MCS4 Mixed Mode	-	36	-	dB

Table 77 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

1. Sensitivities for channels 6,7,8 & 11 are up to 2dB worse.

4.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

4.6.4.1 Transmitter characteristics with 3.3 V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at the antenna port. ⁽¹⁾

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power	BR		-	12	-	dBm
	EDR 2Mbps		-	12	-	dBm
	EDR 3Mbps		-	12	-	dBm
	LE 1Mbps		-	17	-	dBm
	LE 2Mbps		-	17	-	dBm
	LR 500 Kbps		-	17	-	dBm
	LR 125 Kbps		-	17	-	dBm
Power Control Step	BR, EDR		-	3	-	dB
Adjacent Channel Power M-N = 2	BR		-	-	-20	dBm
	EDR		-	-	-20	dBm
	LE		-	-	-20	dBm
	LR		-	-	-20	dBm
Adjacent Channel Power M-N > 2	BR		-	-	-40	dBm
	EDR		-	-	-40	dBm
	LE		-	-	-30	dBm
	LR		-	-	-30	dBm
BR Modulation Characteristics	DH1		-25	-	25	kHz
	DH3		-40	-	40	kHz

Parameter	Condition	Notes	Min	Typ	Max	Units
	DH5		-40	-	40	kHz
	Drift Rate		-20	-	20	kHz/50 us
	Δf_1 Avg		140	-	175	kHz
	Δf_2 Max		115	-		kHz
EDR Modulation Characteristics	RMS DEVM, EDR2		-	15	-	%
	RMS DEVM, EDR3		-	5.5	-	%
	99% DEVM, EDR2		-	23	-	%
	99% DEVM, EDR3		-	9.5	-	%
	peak DEVM, EDR2		-	28	-	%
	peak DEVM, EDR3		-	13.5	-	%
BLE Modulation Characteristics	Δf_1 Avg		225	-	275	kHz
	Δf_2 Max		185	-	-	kHz
	Δf_2 Avg/ Δf_1 Avg		0.8	-	-	-
Transmitter Emissions (BR @Maximum output power)	776-794 MHz	CDMA2000	-	-160	-	dBm/Hz
	869-960 MHz	CDMAOne, GSM850	-	-160	-	dBm/Hz
	1450-1495 MHz	DAB	-	-160	-	dBm/Hz
	1570-1580 MHz	GPS	-	-160	-	dBm/Hz
	1592-1610 MHz	GLONASS	-	-160 ⁽²⁾	-	dBm/Hz
	1710-1800 MHz	DSC-1800-Uplink	-	-115	-	dBm/Hz
	1805-1880 MHz	GSM 1800	-	-148	-	dBm/Hz
	1850-1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910-1930 MHz	TDSCDMA,LTE	-	-135	-	dBm/Hz
	1930-1990 MHz	GSM1900, CDMAOne, WCDMA	-	-101	-	dBm/Hz
	2010-2075 MHz	TDSCDMA	-	-148	-	dBm/Hz
	2110-2170 MHz	WCDMA	-	-115	-	dBm/Hz
	2305-2370 MHz	LTE Band 40	-	-140	-	dBm/Hz
	2370-2400 MHz	LTE Band 40	-	-134	-	dBm/Hz
	2496-2530 MHz	LTE Band 41	-	-125	-	dBm/Hz
	2530-2560 MHz	LTE Band 41	-	-138	-	dBm/Hz
	2570-2690 MHz	LTE Band 41	-	-138	-	dBm/Hz
	5000-5900 MHz	WLAN 5G	-	-148	-	dBm/Hz

Table 78 Bluetooth Transmitter Characteristics on HP RF Chain 3.3V

1. Up to 2dB variation in power from channel-to-channel.
2. Noise-floor is -160dBm/Hz with spurious tone power of -68dBm at 1601.33 MHz when the

transmitted signal is at 2402 MHz

4.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

TA = 25°C. Parameters are measured at the antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Transmit Power	BR	-	-	-3.5	dBm
	LE 1Mbps	-	-	-3.5	dBm
	LE 2Mbps	-	-	-3.5	dBm
	LR 500 Kbps	-	-	-3.5	dBm
	LR 125 kbps	-	-	-3.5	dBm
Adjacent Channel Power M-N = 2	BR	-	-	-20	dBm
	LE	-	-	-20	dBm
	LR	-	-	-20	dBm
Adjacent Channel Power M-N > 2	BR	-	-	-40	dBm
	LE	-	-	-30	dBm
	LR	-	-	-30	dBm
BR Modulation Characteristics	DH1	-25	-	25	kHz
	DH3	-40	-	40	kHz
	DH5	-40	-	40	kHz
	Drift Rate	-20	-	20	kHz
	Δf1 Avg	140	-	175	kHz
	Δf2 Max	115	-	-	kHz
BLE Modulation Characteristics	Δf1 Avg	225	-	275	kHz
	Δf2 Max	185	-	-	kHz
	Δf2 Avg/Δf1 Avg	0.8	1.5	-	-

Table 79 Bluetooth Transmitter Characteristics on LP 0 dBm RF Chain

4.6.6 Bluetooth Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at the antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off ^{(1),(2)}	BR (1 Mbps), 339 bytes, DH5 Packet, BER= 0.1%	-	-90.5	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-91.5	-	dBm
	EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet, BER= 0.01%	-	-84.5	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-92	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-90	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-99	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-103	-	dBm
Maximum Input Level	BR, EDR2, EDR3,BER= 0.1%	-	-15	-	dBm
	LE 1Mbps, 2Mbps,PER=30.8%	-	-3	-	dBm
	LR 500kps, 125kbps,PER=30.8%	-	8	-	dBm
C/I Performance	BR, co-channel, BER=0.1%	-	9	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-	-2	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-	-19	-	dB
	BR, adjacent >= ±3 MHz BER=0.1%	-	-19	-	dB
	BR, Image channel BER=0.1%	-	-11	-	dB
	BR, adjacent to Image channel BER=0.1%	-	-22	-	dB
	EDR2, co-channel BER=0.1%	-	11	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-	-2	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-	-17	-	dB
	EDR2, adjacent >= ±3 MHz BER=0.1%	-	-17	-	dB
	EDR2, Image channel BER=0.1%	-	-9	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-	-22	-	dB
	EDR3, co-channel BER=0.1%	-	19	-	dB
	EDR3, adjacent +1/- MHz BER=0.1%	-	3	-	dB
	EDR3, adjacent +2/-2 MHz BER=0.1%	-	-12	-	dB
	EDR3, adjacent >= ±3 MHz BER=0.1%	-	-12	-	dB
	EDR3, Image channel BER=0.1%	-	-2	-	dB
	EDR3, adjacent to Image channel BER=0.1%	-	-15	-	dB
LE 1Mbps	LE 1Mbps, co-channel PER=30.8%	-	19	-	dB
	LE 1Mbps, adjacent +/-1 MHz PER=30.8%	-	13	-	dB
	LE 1Mbps, adjacent +2/-2 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent +3/-3 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent >= ±4 MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-11	-	dB
	LE 1Mbps, 1MHz adjacent to Image channel	-	-17	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
	PER=30.8%				
	LE 2Mbps, co-channel PER=30.8%	-	19	-	dB
	LE 2Mbps, adjacent +/-2 MHz PER=30.8%	-	13	-	dB
	LE 2Mbps, adjacent +4/-4 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent $\geq \pm 6 $ MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-11	-	dB
	LE 1Mbps, 2MHz adjacent to Image channel PER=30.8%	-	-17	-	dB

Table 80 Bluetooth Receiver Characteristics on HP RF Chain

- BR, EDR:** Sensitivities for channels 38,78 are up to 4dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)
- BLE, LR:** Sensitivities for channels 19,39 are up to 3dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)

4.6.7 Bluetooth Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at the antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off ^{(1),(2)}	BR (1 Mbps), 339 bytes, DH5 Packet BER= 0.1%	-	-88	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-91.5	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-89	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-87	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-96.5	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-101	-	dBm
Maximum Input Level	BR, EDR2 BER= 0.1%	-	-16	-	dBm
	LE 1Mbps, 2Mbps PER=30.8%	-	-3	-	dBm
	LR 500kps, 125kpbs PER=30.8%	-	8	-	dBm
BER Floor		-	1e-4	-	%
C/I Performance	BR, co-channel BER= 0.1%	-	9	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-	-2	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-	-19	-	dB
	BR, adjacent $\geq \pm 3 $ MHz BER=0.1%	-	-19	-	dB
	BR, Image channel BER=0.1%	-	-11	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
	BR, adjacent to Image channel BER=0.1%	-	-22	-	dB
	EDR2, co-channel BER=0.1%	-	11	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-	-2	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-	-17	-	dB
	EDR2, adjacent $\geq \pm 3 $ MHz BER=0.1%	-	-17	-	dB
	EDR2, Image channel BER=0.1%	-	-9	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-	-22	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	19	-	dB
	LE 1Mbps, adjacent +/-1 MHz PER=30.8%	-	13	-	dB
	LE 1Mbps, adjacent +2/-2 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent +3/-3 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent $\geq \pm 4 $ MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-11	-	dB
	LE 1Mbps, 1MHz adjacent to Image channel PER=30.8%	-	-17	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	19	-	dB
	LE 2Mbps, adjacent +/-2 MHz PER=30.8%	-	13	-	dB
	LE 2Mbps, adjacent +4/-4 MHz PER=30.8%	-	-19	-	dB
	LE 1Mbps, adjacent $\geq \pm 6 $ MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-11	-	dB
	LE 1Mbps, 2MHz adjacent to Image channel PER=30.8%	-	-17	-	dB

Table 81 Bluetooth Receiver Characteristics on LP RF Chain

- BR, EDR:** Sensitivities for channels 38,78 are up to 4dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)
- BLE, LR:** Sensitivities for channels 19,39 are up to 3dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)

4.6.8 WLAN 5GHz Transmitter Characteristics

TA = 25°C, Parameters are measured at antenna port on channel 100 (5500 MHz)⁽¹⁾

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	OFDM - 6 Mbps	EVM< -5 dB	-	12	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	13.5	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	13.5	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
	OFDM - 18 Mbps	EVM< -13 dB	-	13.5	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	13.5	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	13.5	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	12	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	7.5	-	dBm
	HT - MCS0	EVM< -5 dB	-	13.5	-	dBm
	HT - MCS1	EVM< -10 dB	-	13.5	-	dBm
	HT - MCS2	EVM< -13 dB	-	13.5	-	dBm
	HT - MCS3	EVM< -16 dB	-	13.5	-	dBm
	HT - MCS4	EVM< -19 dB	-	13.5	-	dBm
	HT - MCS5	EVM< -22 dB	-	12.5	-	dBm
	HT - MCS6	EVM< -25 dB	-	7	-	dBm
	HT - MCS7	EVM< -27 dB	-	5	-	dBm
Transmit Power for 40MHz Bandwidth, compliant with IEEE mask and EVM	MCS0 Mixed Mode	EVM< -5 dB	-	8	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	8	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	8	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	8	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	8	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	8	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB	-	7.5	-	dBm
	MCS7 Mixed Mode	EVM< -27 dB	-	4.5	-	dBm
Transmitter Emissions (6 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-159	-	dBm/Hz
	869-960 MHz	CDMAOne, GSM850	-	-159	-	dBm/Hz
	1450-1495 MHz	DAB	-	-158	-	dBm/Hz
	1570-1580 MHz	GPS	-	-158	-	dBm/Hz
	1710-1800 MHz	DSC-1800-Uplink	-	-158	-	dBm/Hz
	1805-1880 MHz	GSM 1800	-	-158	-	dBm/Hz
	1850-1910 MHz	GSM 1900	-	-158	-	dBm/Hz
	1910-1930 MHz	TDSCDMA,LTE	-	-158	-	dBm/Hz
	1930-1990 MHz	GSM1900, CDMAOne, WCDMA	-	-158	-	dBm/Hz
	2010-2075 MHz	TDSCDMA	-	-159	-	dBm/Hz
	2110-2170 MHz	WCDMA	-	-159	-	dBm/Hz
	2305-2370 MHz	LTE Band 40	-	-159	-	dBm/Hz

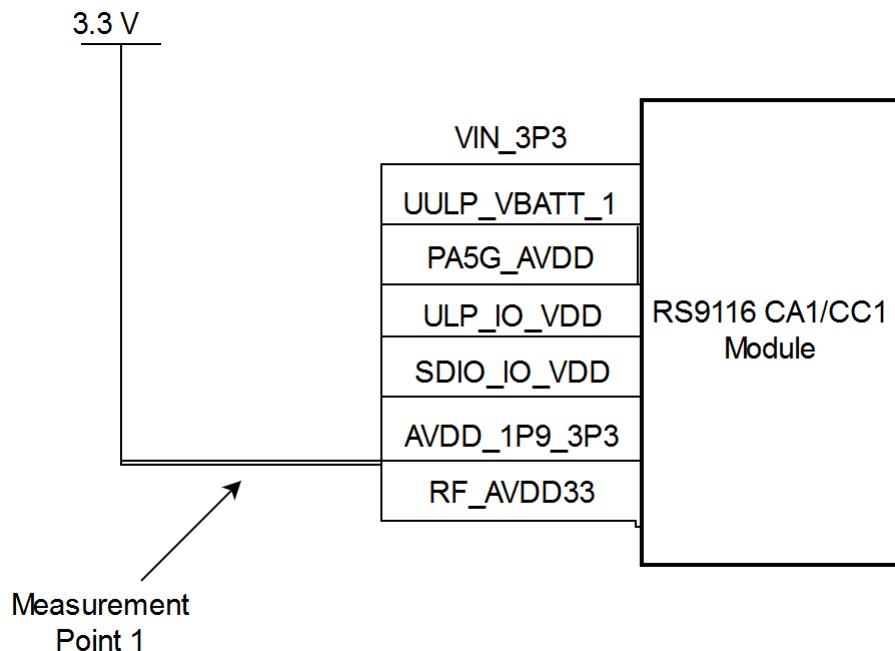
Parameter	Condition	Notes	Min	Typ	Max	Units
	2370–2400 MHz	LTE Band 40	-	-159	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-159	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-159	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-155	-	dBm/Hz

Table 82 WLAN 5 GHz Transmitter Characteristics

- Up to 3dB variation in power from channel-to-channel.

4.7 Typical Current Consumption

4.7.1 3.3 V



4.7.1.1 WLAN

Parameter	Description	Value	Units
1 Mbps Listen	LP Chain	14	mA
1 Mbps RX Active	LP Chain	20	mA
IEEE 802.11g - 6 Mbps RX Active	HP Chain	49	mA
IEEE 802.11g - 72 Mbps RX Active	HP Chain	49	mA
11 Mbps TX Active	Tx Power = Maximum (18dBm) Tx Power = 8dBm	270 130	mA mA
IEEE 802.11g - 6 Mbps TX Active	Tx Power = Maximum (18dBm) Tx Power = 8dBm	285 130	mA mA

Parameter	Description	Value	Units
IEEE 802.11g - 54 Mbps TX Active	Tx Power = Maximum (15dBm)	200	mA
	Tx Power = 8dBm	130	mA
IEEE 802.11g - 72 Mbps TX Active	Tx Power = Maximum (12dBm)	180	mA
	Tx Power = 8dBm	130	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Standby Associated, DTIM = 1	2.4GHz Band	586	uA
	5GHz Band	-	uA
Standby Associated, DTIM = 3	2.4GHz Band	238	uA
	5GHz Band	-	uA
Standby Associated, DTIM = 10	2.4GHz Band	102	uA
	5GHz Band	189	uA

4.7.1.2 Bluetooth BR and EDR

Parameter	Description	Value	Units
TX Active Current, 1 Mbps BR	LP chain, Tx Power = -2 dBm	9.9	mA
	HP chain, Tx Power = Maximum (12 dBm)	130	mA
RX Active Current, 1 Mbps BR	LP chain	10.2	mA
	HP chain	26.7	mA
TX Active Current, 2 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	130	mA
RX Active Current, 2 Mbps EDR	LP chain	10.2	mA
	HP chain	26.7	mA
TX Active Current, 3 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	140	mA
RX Active Current, 3 Mbps EDR	HP chain	26.7	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Inquiry Scan	Scan Interval = 1.28s	-	mA
	Scan Window = 128ms		
Page Scan	Scan Interval = 1.28s	-	mA

Parameter	Description	Value	Units
	Scan Window = 128ms		
Inquiry and Page Scan	Inquiry/Page Scan Interval = 1.28s Scan Window = 128ms	-	mA
SNIFF Mode	Sniff Interval = 500ms Attempts = 2 Tx Power = 2 dBm, HP chain	-	uA
A2DP Source	Rate = 229kbps, Packet = 3-DH5,Tx Power = 2 dBm, HP chain	-	uA
A2DP Sink	Rate = 229kbps, Packet = 3-DH5,Tx Power = 2 dBm, HP chain	-	uA

4.7.1.3 Bluetooth LE

Parameter	Description	Value	Units
TX Active Current	LP chain, Tx Power = -2 dBm LP Chain, Tx Power = 2 dBm HP Chain, Tx Power = Maximum (18 dBm)	8.9 - 190	mA
RX Active Current	LP chain HP chain	10.9 26.7	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Advertising, Unconnectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	45	uA
Advertising, Connectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	60	mA
Connected	Connection Interval = 1.28s	44	uA

Parameter	Description	Value	Units
	No Data		
	Tx Power = -2 dBm, LP chain		
Connected	Connection Interval = 200ms	144	uA
	No Data		
	Tx Power = 0 dBm, LP chain		
Scanning	Scan Interval = 1.28s	-	uA
	Scan Window = 11.25ms		
	LP Chain		

4.7.1.4 Wireless Coexistence

Parameter	Description	Value	Units
Wi-Fi Standby Associated + BLE Connected	Wi-Fi: 2.4GHz, DTIM = 3 BLE: Connection Interval = 200ms	360	uA
Wi-Fi Standby Associated + BLE Connectable Advertising	Wi-Fi: 2.4GHz, DTIM = 3 BLE: Advertising Interval = 1.28s	256	uA
Wi-Fi Standby Associated + BLE Connected + BT-A2DP Audio streaming	Wi-Fi: 2.4GHz, DTIM = 3 BLE: Connection Interval = 200ms BT: A2DP Source	-	uA
Wi-Fi Standby Associated + BLE Connected	Wi-Fi: 5GHz, DTIM = 3 BLE: Connection Interval = 200ms	660	uA
Wi-Fi Standby Associated + BLE Connectable Advertising	Wi-Fi: 5GHz, DTIM = 3 BLE: Advertising Interval = 1.28s	460	uA
Wi-Fi Standby Associated + BLE Connected + BT-A2DP Audio streaming	Wi-Fi: 5GHz, DTIM = 3 BLE: Connection Interval = 200ms BT: A2DP Source	-	uA

5 RS14100 CA1/CC1 module Detailed Description

RS14100 includes two processors. An ARM Cortex-M4F running up to 180MHz and Redpine's ThreadArch® 4-Threaded processor running up to 160MHz. The Cortex-M4F is dedicated for peripheral and application related processing whereas all the networking and wireless stacks run on independent threads of the ThreadArch®. In addition, in adherence to the Trusted Execution Environment architecture - the ThreadArch® subsystem also acts as the secure processing domain and takes care of secure boot, secure firmware upgrade and provides access to security accelerators and secure peripherals through pre-defined APIs. The bus matrices of Cortex-M4F and ThreadArch® are separate and asynchronous. Though the two processors are present in a single chip - it is ensured that the ThreadArch® based "Networking, Security and Wireless subsystem" is completely separated from the ARM Cortex-M4F based "Application subsystem". Thus, these two processors have separate power, clocks/PLLs, bus-matrices, and memory. This provides two key advantages - programming, operating and power-state independence between the two processors and enhanced security by restricting access to the ThreadArch® subsystem.

5.1 ARM Cortex M4F

The ARM Cortex-M4F is the main application processor in RS14100. It is a high-performance 32-bit processor designed by ARM for the microcontroller market. It is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division. The Cortex M4F microcontroller integrated into RS14100 supports the following features:

- MPU (Memory Protection Unit) with 8 memory regions, FPU (Floating Point Unit) and NVIC with 64 levels of interrupt priority.
- Debug port with both JTAG as well as Serial Wire Debug (SWD) interface. Comprehensive debug functionality including data matching for a watch-point generation.
- To provide optimal power vs performance tradeoff, unique gear-shifting is available for the Cortex-M4F that enables optimal power consumption based on the required performance. The available power-states are PS4 (at 1.1V): max 180MHz, PS3 (at 0.9V): max 100MHz, PS2 (at 0.7V): max 32MHz. More details are provided in the power-architecture section
- Architectural clock gates are included to minimize dynamic power dissipation.
- The ThreadArch® and Cortex-M4F communicate through thread to thread interrupting and memory.
- On-chip SRAM of 144K/208K/272Kbytes based on the RS14100 chip configuration
- Out of the above SRAM, 16Kbytes is present in the Ultra-low-power peripheral subsystem. This memory is present on the S-bus of the Cortex-M4F and is primarily used by the ULP MCU peripherals like VAD, FIM, ULP I2S, etc.
- 64Kbytes of ROM which holds the Cortex-M4F peripheral drivers.
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with external quad/octa SPI SDR/DDR flashes.
- Based on the RS14100 package configuration up to 4MBytes of "in-package" Quad SPI flash is available for the Cortex-M4F
- eFuse of 32 bytes (available for customer applications)
- 225 DMIPS performance

The Cortex-M4F core includes the following core peripherals:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

System control block

The System control block (SCB) is the programmers model interface to the processor. It provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

Memory protection unit

The Memory protection unit (MPU) improves system reliability by defining the memory attributes for different memory regions. It provides up to eight different regions and an optional predefined background region. It provides fine grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data, and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

The memory map and the programming of the MPU split the memory map into regions. Each region has a defined memory type, and some regions have additional memory attributes. The memory type and attributes determine the behavior of accesses to the region.

The memory types are:

- **Normal** The processor can re-order transactions for efficiency, or perform speculative reads.
- **Device** The processor preserves transaction order relative to other transactions to Device or Strongly-ordered memory.
- **Strongly-ordered** The processor preserves transaction order relative to all other transactions. The different ordering requirements for Device and Strongly-ordered memory mean that the memory system can buffer a write to Device memory, but must not buffer a write to Strongly-ordered memory.

The additional memory attributes include:

- **Shareable:** For a shareable memory region, the memory system provides data synchronization between bus masters in a system with multiple bus masters, for example, a processor with a DMA controller. Strongly-ordered memory is always shareable. If multiple bus masters can access a non-shareable memory region, the software must ensure data coherency between the bus masters.
- **Execute Never (XN):** Means the processor prevents instruction accesses. A fault exception is generated only on execution of an instruction executed from an XN region.

Floating-point unit

The Floating-point unit (FPU) provides IEEE754-compliant operations on single-precision, 32-bit, floating-point values. It supports addition, subtraction, multiplication, division and square root.

5.1.1 Memory Architecture

There are on chip ROM, RAM and off chip FLASH connectivity. Sizes of ROM/RAM/FLASH will vary depending on the chip configuration.

Highlights:

- Unified memory architecture - software can partition the memory between code and data usage
- Multiport - RAMs support multiport access - allowing simultaneous access from different masters(I, D, DMAs) to non overlapping regions without any cycle penalty
- ROM/RAMs are tightly coupled to the processor I/D buses to reduce the latency and power
- Supports memory protection - generates trap if unintended master accesses the memory

The Cortex-M4F processor has following memory:

- On-chip SRAM of 144K/208K/272Kbytes based on the chip configuration
- Out of the above SRAM, 16Kbytes is present in the Ultra-low-power peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like VAD, FIM, ULP I2S, etc.
- 64Kbytes of ROM which holds the M4F peripheral drivers.
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with external quad/octa SPI SDR/DDR flashes.
- Based on the package configuration up to 4MBytes of "in-package" Quad SPI flash is available for the M4F
- eFuse of 32 bytes (available for customer applications)

5.1.2 Security

- HW device identity and key storage with PUF
- Trusted Execution Environment with Secure Boot loader
- Accelerators: AES128/256, SHA256/384/512, HMAC, RSA, ECC, ECDH, RNG, CRC
- Secure XIP from flash

- Secure boot loading performed by secure processor
- Secure firmware update
- Tamper detection with Hardware disable, Secure RTC, Secure Hardware Watchdog and other Secure Peripherals connected to the Trusted Execution Environment.
- Programmable Secure Hardware Write protect for Flash sectors

5.1.3 Interrupts

- Nested vectored interrupt controller (NVIC) for interrupts handling
- Supports 99 interrupts
- Flexible exception and interrupt management
- Nested exception/interrupt support
- Vectored exception/interrupt entry
- Interrupt configurations, prioritization, and interrupt masking

5.1.3.1 Vector table

When an exception event takes place and is accepted by the processor core, the corresponding exception handler is executed. To determine the starting address of the exception handler, a vector table mechanism is used. The vector table is an array of word data inside the system memory, each representing the starting address of one exception type. The vector table is relocatable and the relocation is controlled by a programmable register in the NVIC called the Vector Table Offset Register (VTOR). After reset, the VTOR is reset to 0; therefore, the vector table is located at address 0x0 after reset. The beginning of the memory space contains the vector table, and the first two words in the vector table are the initial value for the Main Stack Pointer (MSP), and the reset vector, which is the starting address of the reset handler. After these two words are read by the processor, the processor then sets up the MSP and the Program Counter (PC) with these values.

For example, if the reset is exception type 1, the address of the reset vector is 1 times 4 (each word is 4 bytes), which equals 0x00000004, and the NMI vector (type 2) is located at $2 \times 4 = 0x00000008$. The address 0x00000000 is used to store the starting value of the Main Stack Pointer.

5.1.3.2 Vectored Interrupt Table (VIT)

99 interrupts are mapped on NVIC. MCU HP peripheral interrupts, MCU ULP peripheral interrupts, MCU UULP peripheral interrupts and NWP peripheral interrupts are mapped into following Vectored interrupt table.

Interrupt Number	Interrupt
19 : 0	MCU ULP peripheral Interrupts
29: 20	MCU UULP peripheral Interrupts
74:30	MCU HP peripheral interrupts
98:75	NWP peripheral interrupts

5.1.3.2.1 MCU HP Peripheral Interrupts

There are 45 MCU HP peripheral interrupts in 9116 chip. Following table provides the list of MCU HP peripheral interrupts and their interrupt number in vector interrupt table.

Interrupt Number in VIT	MCU HP Peripheral interrupt
30	Reserved
31	GPDMA interrupt
32	Reserved
33	MCU HP UDMA interrupt
34	SCT interrupt
35	HIF Interrupt 1
36	HIF Interrupt 2

Interrupt Number in VIT	MCU HP Peripheral interrupt
37	SIO Interrupt
38	USART 1 Interrupt
39	UART 2 Interrupt
40	Reserved
41	EGPIO wakeup interrupts
42	I2C Interrupt
43	Reserved
44	SSI Slave Interrupt
45	Reserved
46	GSPI Master 1 Interrupt
47	SSI Master Interrupt
48	MCPWM Interrupt
49	QEI Interrupt
51 : 50	GPIO Group Interrupt
59 : 52	GPIO Pin Interrupt
60	QSPI2 Interrupt
61	I2C 2 Interrupt
62	Ethernet Interrupt
63	Reserved
64	I2S master Interrupt
65	Reserved
66	Can 1 Interrupt
67	Reserved
68	SDMEM Interrupt
69	PLL clock ind Interrupt
70	Reserved
71	Reserved
72	Reserved
73	USB interrupt
74	NWP P2P interrupt

5.2 Interconnect

The following are the buses and bridges that form the interconnect in RS14100. MCU refers to the Cortex-M4F and NWP refers to the ThreadArch® Network Processor.

- High Performance MCU AHB Interconnect Matrix (ICM)
- MCU AHB to APB dual bridge
- MCU AHB to ULP MCU AHB bridge
- ULP MCU AHB ICM
- ULP MCU AHB to APB bridge
- MCU AHB - NWP AHB bridge
- High Performance NWP AHB ICM
- NWP AHB to APB dual bridge

The High Performance MCU AHB ICM is a multilayer interconnect implementation of the AHB protocol designed for higher performance and higher frequency systems. A 14 Master x 13 Slave AHB ICM is used. For further details on the masters and slaves, the interconnect configuration/connections possible between them and address mapping, refer to the Hardware Reference Manual.

5.2.1 Address Mapping

5.2.1.1 MCU AHB Slaves Address Mapping

Following table has the base addresses of memories and high speed peripherals.

	Module Name	Size	Start Address
Memories			
	LP SRAM	128KB	0x0000_0000
	HP SRAM1	64KB	0x0002_0000
	HP SRAM2	64KB/192KB	0x0003_0000
	ROM	64KB	0x0030_0000
AHB Peripherals			
	QSPI Direct Access Mode	64MB	0x0800_0000
	QSPI Indirect Access Mode	1MB	0x1200_0000
	SDIO/SPI Slave	64KB	0x2020_0000
	USB	64KB	0x2021_0000
	SMIH Controller	128KB	0x2022_0000
	Ethernet	128K	0x2024_0000
	Icache	64KB	0x2028_0000
	GPDMA	512KB	0x2108_0000
	ULPSS AHB Bridge	256KB	0x2404_0000
	APB Bridge	64MB	0x4400_0000
	NWP AHB Bridge	512MB	0x0080_0000 / 0x0400_0000 / 0x1000_0000 / 0x2010_0000 / 0x2040_0000 / 0x2100_0000 / 0x2200_0000 /

	Module Name	Size	Start Address
			0x4000_0000

5.2.1.2 MCU APB Peripherals Address Mapping

Following table has the base addresses of all low speed MCU peripherals.

Peripheral	Base Address
PERI-1 Power Domain	
UART1	0x4400_0000
USART1	0x4400_0100
I2C1	0x4401_0000
SSI_MST	0x4402_0000
UDMA	0x4403_0000
PERI-2 Power Domain	
SSI_SLV1	0x4501_0000
UART2	0x4502_0000
GSPI_1	0x4503_0000
CONFIG_TIMER	0x4506_0000
CAN1_CONTROLLER	0x4507_0000
CRC	0x4508_0000
HWRNG	0x4509_0000
Other Domains	
VIC	0x4611_0000
ROM_PATCH	0x4612_0200
EGPIO	0x4613_0000
REG_SPI	0x4618_0000
PMU	0x4600_0000
PAD_CFG	0x4600_4000
MISC_CFG	0x4600_8000
EFUSE	0x4600_C000
PERI-4 Power Domain	
SIO	0x4700_0000
I2C2	0x4704_0000
I2S	0x4705_0000
QEI	0x4706_0000
PWM	0x4707_0000

5.2.1.3 ULP MCU APB Peripherals Address Mapping

Following table has the base addresses of all low speed ULP MCU peripherals.

Peripheral	Starting Address
ULP I2C	0x2404_0000
ULP I2S	0x2404_0400
ULP SSI	0x2404_0800
IR	0x2404_0C00
ULP Config	0x2404_1400
ULP UART	0x2404_1800
ULP TIMER	0x2404_2000
Touch Sensor	0x2404_2C00
VAD	0x2404_3400
AUX ADC DAC Controller	0x2404_3800
NPSS_APB	0x2404_8000
ULP EGPI0	0x2404_C000
IPMU Reg Access SPI	0x2405_0000
ULP Memory	0x2406_0000
FIM	0x2407_0000
ULP UDMA	0x2407_8000

5.3 USB Host Interface

The Universal Serial Bus (USB) is a cable bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host scheduled, token based protocol. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation. The On-The-Go (OTG) Supplement to the USB Specification extends USB to peer-to-peer application. Using USB OTG technology, consumer electronics, peripherals and portable devices can connect to each other (for example, a digital camera can connect directly to a printer, or a keyboard can connect to a Personal Digital Assistant) to exchange data. With USB OTG, develop a fully USB compliant peripheral device that can also assume the role of a USB host. The OTG state machines determine the role of the device based on connector signals, and then initializes the device in the appropriate mode of operation (host or peripheral) based on how it is connected. After connecting the devices can negotiate using the OTG protocols to assume the role of host or peripheral based on the task to be accomplished.

MCU supports one High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY. The USB OTG module allows to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

- Complies with Universal Serial Bus specification 2.0.
- Complies with USB On-The-Go supplement
- Complies with Enhanced Host Controller Interface Specification
- Supports auto USB 2.0 mode discovery
- Supports all high-speed USB compliant peripherals with maximum speed of 480 Mbps
- Supports all full-speed USB compliant peripherals with maximum speed of 12Mbps
- USB-IF Certified
- Support interrupts

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Protocol-aware DMA engine for high USB data through-put, low system CPU and system bus loading

5.4 Power Architecture

RS14100 achieves ultra low power without compromising on features that have been traditionally considered "power-hungry". Hierarchical partitioning and numerous system and circuit level innovations have been used to achieve ultra low power while retaining high performance capability. Unlike in GHz microprocessors, majority (>75%) of power consumption in traditional microcontrollers occurs outside the processor - typically in the bus-matrix, memory, PLLs, regulators and peripherals. On first look it would seem to be possible to have two processor cores (typically Cortex-M4F and M0+) in an SoC to get power savings similar to those in microprocessors. But, without careful design, the gains in system power consumption would be incremental since the power is reduced in the processor alone. Additionally, software and development complexity is introduced with two cores due to inter-core communication, limitations in the instruction set of the smaller core and resulting code incompatibility and code redundancy. It is necessary in many applications to have the same code run in an ultra-low-power mode until the need for speed occurs. Also, it should be noted that the "gear shifting" approach through dynamic voltage and frequency scaling (DVFS) alone doesn't achieve significant power savings. Through DVFS, careful optimization and hierarchical design for all components of the SoC, RS14100 achieves better power consumption using Cortex-M4F than typical off-the-shelf M0+ implementations. RS14100 can gear shift from "180MHz @ 60uA/MHz in PS4 down to 20MHz @ 19uA/MHz in PS2". Some of the other features of RS14100 which help in achieving state-of-the-art ultra low power are listed below:

- Two integrated buck switching regulators (High performance and ULP) to enable efficient Dynamic Voltage Scaling across wide operating mode currents ranging from <1uA to 300mA
- High performance and ultra-low-power MCU peripheral subsystems and buses.
- Multiple voltage domains with Independent voltage scaling of each domain
- Fine grained power-gating including buses and pads.

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/Shutdown) and the power control for different Group of Peripherals. In addition, wakeup from any of the Standby/Sleep/Shutdown states based on hardware events or peripheral interrupts is supported. The Standby and Shutdown states can be reached from Active mode only and through a WFI instruction. Wakeup from Standby/Sleep/Shutdown states is through a hardware event or interrupt (Peripheral or External).

5.4.1 Highlights

- Two integrated buck switching regulators (High performance and ULP) to enable efficient Dynamic Voltage Scaling across wide operating mode currents ranging from <1uA to 300mA
- High performance and ultra-low-power MCU peripheral subsystems and buses.
- Multiple voltage domains with Independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/pads are inactive.
- Multiple Active states using "gear-shifting" approach based on processing requirements, thereby reducing power consumption for low-power applications.
- Flexible switching between different Active states with controls from Software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default thereby reducing the power consumption in inactive state.
- Low wakeup times as configurable by Software.

5.4.2 Power domains

All the Applications, High Speed Interfaces and Peripherals are segregated into multiple power domains to achieve lower current consumption when they are inactive. At reset, all the domains are powered ON.

The table below describes the different group of peripherals for which power is controlled through software

S.No	Section	Domain Name	Functionality of the Power Domain
1	APPLICATIONS	DEBUG	Debug Functionality for Cortex-M4F
		FPU	Floating Point Unit for Cortex-M4F
		ICACHE	ICache for the Cortex-M4F Processor
		ROM	ROM Core/Interface
		SRAM	SRAM Banks
2	HIGH SPEED INTERFACE	QSPI	Quad/Octa SPI SDR/DDR Flash Interface
		ETHERNET	10/100 Ethernet Controller with RMII
		SDMEM	SDMEM, eMMC, SDIO 3.0 Interface
		USB	USB 2.0 OTG
3	HP-PERIPHERALS	PERI-DOMAIN1	SPI/SSI Master, I2C, USART and Micro-DMA Controller.
		PERI-DOMAIN2	UART, SPI/SSI Slave, Generic-SPI Master, Config Timer, CAN, Random-Number Generator and CRC Accelerator.
		PERI-DOMAIN3	SIO, I2C, I2S Master/Slave, QEI and MCPWM.
		DMA	General Purpose DMA Controller
		SDIO-SPI	SDIO 2.0 Slave, SPI Slave.
		EFUSE	EFUSE for configuration information
4	HIGH SPEED FLASH MEMORY	FLASH-LDO	LDO-FL 1.8 for Flash Memory
5	HIGH-FREQ-PLL	PLL-REGISTERS	PLL Programming Registers for High frequency clocks.
6	DDR-FLASH-DLL	QSPI-DLL	DLL for Quad/Octa DDR Flash Interface
7	ULP-PERIPHERALS	DMA	Micro-DMA Controller
		IR	IR Receiver
		ADC-DAC	ADC and DAC Controller
		I2C	I2C Master/Slave
		SSI	SPI/SSI Master
		UART	UART
		VAD	Voice Activity Detection

S.No	Section	Domain Name	Functionality of the Power Domain
		TOUCH	Capacitive Touch Sensor Controller
		FIM	IIR/FIR Filter, Interpolation, Matrix Multiplication, etc.
		TIMER	Timers
8	UULP-PERIPHERALS	WDT	Watch Dog Timer
		TS	Temperature Sensor Controller
		PS	Process Sensor Controller
		RTC	Real-Time Clock
		STORAGE-DOMAIN1	Storage Flops - Set1. Contains 8bytes
		STORAGE-DOMAIN2	Storage Flops - Set2. Contains 8bytes
		STORAGE-DOMAIN3	Storage Flops - Set3. Contains 16bytes
		SLEEP-FSM	FSM for Sleep/Wakeup
		CLOCK-CALIB	Calibration block for Sleep Clock.
		BBFFS	Programming Registers which can be retained during sleep.
		DS-TIMER	DEEP SLEEP Timer.
		TIMESTAMP	Timestamping Controller.
		LP-FSM	Low-Power FSM
		RETEN	Retention Flops which can be retained during sleep.
9	Analog-PERIPHERALS	Aux-ADC	Auxillary ADC
		Aux-DAC	Auxillary DAC
		BOD	Brown-Out Detector

Table 83 List of Power Domains

The SRAM is also segregated into multiple power domains to achieve lower current consumption as per the Memory requirement. The power for the SRAM domains in active states can be controlled in the following manners

- SRAM Domains as described in the table below can be powered down for unused SRAM sections. The RAM contents are not retained in this mode
- Deep-Sleep (Lower power consumption) mode. The RAM contents are retained in this mode. The SRAM is not accessible in this state. This is configurable on a Bank granularity.

The table below describes the segregation of power domains for SRAM (400KB).

S.No	Section	Domain Name	Functionality of the Power Domain

S.No	Section	Domain Name	Functionality of the Power Domain
1	HP-SRAM1	HP-SRAM1-1	16KB of SRAM (1x Banks)
2		HP-SRAM1-2	32KB of SRAM (2x Banks)
3		HP-SRAM1-3	16KB of SRAM (1x Banks)
4	HP-SRAM2	HP-SRAM2-1	16KB of SRAM (1x Banks)
5		HP-SRAM2-2	32KB of SRAM (2x Banks)
6		HP-SRAM2-3	80KB of SRAM (5x Banks)
7		HP-SRAM2-4	64KB of SRAM (4x Banks)
8	LP-SRAM	LP-SRAM-1	4KB of SRAM (1x Banks)
9		LP-SRAM-2	4KB of SRAM (1x Banks)
10		LP-SRAM-3	4KB of SRAM (1x Banks)
11		LP-SRAM-4	4KB of SRAM (1x Banks)
12		LP-SRAM-5	32KB of SRAM (2x Banks)
13		LP-SRAM-6	64KB of SRAM (4x Banks)
14		LP-SRAM-7	16KB of SRAM (1x Banks)
15	ULP-SRAM	ULP-SRAM-1	2KB of SRAM (1x Banks)
16		ULP-SRAM-2	2KB of SRAM (1x Banks)
17		ULP-SRAM-3	2KB of SRAM (1x Banks)
18		ULP-SRAM-4	2KB of SRAM (1x Banks)
19		ULP-SRAM-5	2KB of SRAM (1x Banks)
20		ULP-SRAM-6	2KB of SRAM (1x Banks)
21		ULP-SRAM-7	2KB of SRAM (1x Banks)
22		ULP-SRAM-8	2KB of SRAM (1x Banks)

5.4.3 Voltage Domains

All the Applications, High Speed Interfaces and Peripherals are segregated into multiple voltage domains to configure the operating voltages in different power states. This section describes the voltage domains and voltage source options available for each domain. These are configured based on the Power state which the device is operating in. The voltage for each domain can be shut-off during sleep by configuring the source to LDO SoC 1.1 (This supply is turned OFF during Sleep).

The table below lists down the different voltage sources and the possible output voltages of each source at different Power states. The voltage sources are described in detail in the Power Management Section.

S.No	Voltage Source	Possible O/P Voltage
1	LDO SoC 1.1	1.1V
		1.0V
2	DC-DC 0.95	1.0V
3	LDO 0.7V	0.7V

Table 84 List of Voltage Sources

The table below lists down the different voltage domains and the possible voltage sources for each domain.

S.No	Voltage Domain	Functionality	LDO SoC 1.1	DC-DC 0.95	LDO 0.7V
1	PROC-DOMAIN	Processor, DEBUG, FPU	Yes	Yes	Yes
2	HIGH-VOLTAGE-DOMAIN	ICACHE, HIGH-SPEED-INTERFACES, HP-PERIPHERALS, HP-SRAM	Yes	No	No
3	LOW-VOLTAGE-LPRAM-16KB	LP-SRAM-1, LP-SRAM-2, LP-SRAM-3, LP-SRAM-4,	Yes	Yes	No
4	LOW-VOLTAGE-LPRAM	ROM LP-SRAM-5, LP-SRAM-6, LP-SRAM-7	Yes	Yes	No
5	LOW-VOLTAGE-ULPPERIPH	ULP-PERIPHERALS	Yes	Yes	No
6	LOW-VOLTAGE-ULPRAM	ULP-SRAM	Yes	Yes	No
7	LOW-VOLTAGE-UULPPERIPH	UULP-PERIPHERALS	No	Yes	No

Table 85 List of Voltage Domains

5.4.4 Power States

The power states available in different modes including the power variants of the processor are listed below

- Reset State
- Active States
 - PS1
 - PS2
 - PS3
 - PS4
- Standby States
 - PS2-STANDBY
 - PS3-STANDBY
 - PS4-STANDBY
- Sleep States
 - PS2-SLEEP
 - PS3-SLEEP
 - PS4-SLEEP
- Shutdown States

- PS0

After reset, the processor starts in PS4 state which is the highest activity state where the full functionality is available. The other Active states (PS2/PS3) will have limited functionality or Processing power.

A transition from Active states (PS2/PS3/PS4) to any other state can only be triggered by software.

A transition from Standby/Sleep/Shutdown states can be triggered by an enabled interrupt as configured by software before entering these states.

A transition from Standby/Sleep to Active state is possible from where these states are entered.

There are different wakeup sources available in each Standby/Sleep/Shutdown states.

The figure below shows the transitions between different power states.

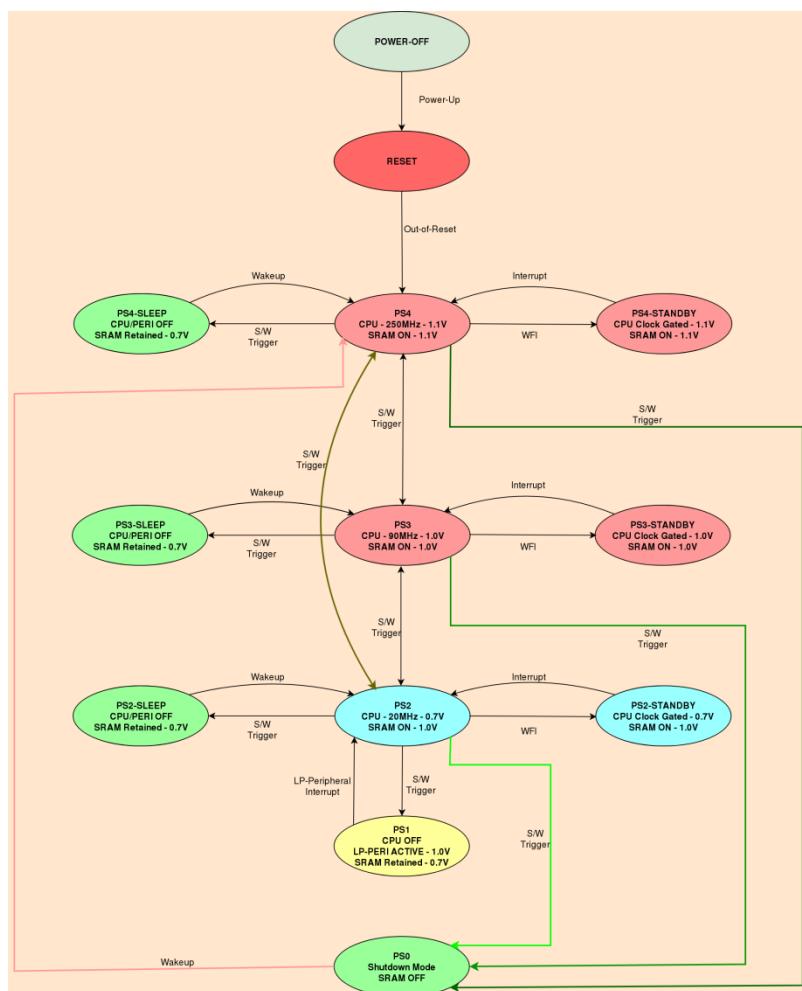


Figure 45

Power states

5.4.4.1 PS4

This is an Active state where the complete functionality is available. The CPU, Peripherals and SRAM operate on the LDO SoC 1.1V Supply at voltage of 1.1V.

This functionality available in this state includes the following

- Maximum CPU Operating frequency of 180MHz. The CPU can operate on the HIGH-FREQ-PLL output clocks.
- APPLICATIONS - DEBUG, FPU, ICACHE and ROM.
- HIGH SPEED INTERFACE - as listed in the Power Domains table above.
- HIGH-FREQ-PLL - as listed in the Power Domains table above.
- DDR-FLASH-DLL - as listed in the Power Domains table above.
- All the Peripherals consisting of HP-PERIPHERALS, ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in the power domains section above.
- All the GPIO's

- Complete SRAM of 400KB (HP-SRAM1, HP-SRAM2, LP-SRAM and ULP-SRAM).
- PS4 wakeup time is around 1.2msec

5.4.4.2 PS3

This is an Active state where the complete functionality is available similar to PS4 state and operates at a lower voltage thereby reducing current consumption. The CPU, Peripherals and SRAM operate on the LDO SoC 1.1 Supply with output voltage of 1.0V. The Maximum CPU frequency is limited to 90MHz in this state.

5.4.4.3 PS2

This is an Active state where a limited set of functionality is available and operates a much lower voltage compared to PS3/PS4 thereby achieving lower current consumption. The CPU, Peripherals and SRAM can operate at different voltages and are configurable by software before entering this state.

The functionality available in this state includes the following

- CPU Operating frequency depends on the voltage source selected for PS2 state. The CPU operates on the ULP-Peripheral AHB Interface clock.
 - If LDO 0.7V is used, Maximum frequency is 20MHz.
 - If DC-DC 0.95 is used, Maximum frequency is 50MHz.
- APPLICATIONS - DEBUG, FPU and ROM.
- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in the power domains table above.
- ULP-GPIO and UULP Vbat GPIO's are available
- Total SRAM of 144KB (LP-SRAM and ULP-SRAM).
- PS2 wakeup time is around 200usec

5.4.4.4 PS1

This state can be entered from PS2 only through a Software Instruction. The CPU is power-gated and a limited set of peripherals are active. The peripheral interrupts are used as wakeup source or to trigger sleep once the peripheral functionality is complete. The Peripherals and SRAM operate at the same voltage as PS2 state. The peripherals need to be configured by the Software for the defined functionality in the PS2 state before entering this state.

The functionality available in this state includes the following

- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in the power domains table above.
- ULP-GPIO and UULP Vbat GPIO's are available
- SRAM of 128KB (LP-SRAM) can be retained in this state.
- SRAM of 16KB (ULP-SRAM) is active for Peripheral functionality.

5.4.4.5 STANDBY

This includes multiple states like PS4-STANDBY, PS3-STANDBY and PS2-STANDBY. These are Standby states entered from PS4/PS3/PS2 state through a WFI instruction. CPU is clock gated in this state.

All the Interrupts in the NVIC table will act as a wakeup source in PS4-STANDBY and PS3-STANDBY state. Wakeup sources for PS2-STANDBY state are defined in the wakeup sources section below.

5.4.4.6 SLEEP

This includes multiple states like PS4-SLEEP PS3-SLEEP and PS2-SLEEP/PS1-SLEEP which can be entered from PS4, PS3 and PS2 state respectively through a Software instruction. In addition, PS2-SLEEP state can be entered from PS1 state through a peripheral interrupt. The CPU is power-gated and a much lower set of peripherals are available.

The status of resources in this state are

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- UULP Vbat GPIO's are available
- SRAM needs to be retained.

Wakeup sources for these states are defined in the Wakeup sources section below.

5.4.4.7 PS0

This is a Shutdown state entered from PS4 state through a Software instruction. The CPU is power-gated and a much smaller set of peripherals are available.

The status of resources in this state are

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- UULP Vbat GPIO's are available
- SRAM need not be retained.

5.4.5 Memory Retention in Sleep / Shutdown states

The table below indicates the SRAM banks and Backup Register Array which can be retained in each Sleep/Shutdown state.

S.No	Power State	HP-SRAM (256KB)	LP-SRAM (128KB)	ULP-SRAM (16KB)	Backup Register Array (32 bytes)
1	PS4-SLEEP	Yes	Yes	Yes	Yes
2	PS3-SLEEP	Yes	Yes	Yes	Yes
3	PS2-SLEEP	Yes	Yes	Yes	Yes
4	PS0	No	No	No	Yes

Table 86 SRAM in different states

5.4.6 Wakeup Sources

The table below indicates the wakeup sources available in Standby/Sleep/Shutdown states.

S.No	Wakeup Source	PS2-STANDBY	PS4-SLEEP	PS3-SLEEP	PS2-SLEEP	PS1	PS0
1	UULP Vbat GPIO	Yes	Yes	Yes	Yes	Yes	Yes
2	Watch-Dog Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
3	Analog Comparator	Yes	Yes	Yes	Yes	Yes	Yes
4	BOD	Yes	Yes	Yes	Yes	Yes	Yes
5	ULP-Peripheral SDC	Yes	No	No	No	Yes	No
6	Wireless Processor Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
7	Deep-Sleep Timer Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
8	Alarm Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
9	Second Based Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
10	Milli-Second Based Interrupt	Yes	Yes	Yes	Yes	Yes	Yes
11	ULP-Peripheral GPIO Group Interrupt	Yes	No	No	No	Yes	No
12	ULP-Peripheral GPIO Pin Interrupt	Yes	No	No	No	Yes	No
13	ULP-Peripheral FIM Interrupt	Yes	No	No	No	No	No
14	ULP-Peripheral SPI/SSI	Yes	No	No	No	Yes	No

S.No	Wakeup Source	PS2-STANDBY	PS4-SLEEP	PS3-SLEEP	PS2-SLEEP	PS1	PS0
	Master Interrupt						
15	ULP-Peripheral IR Interrupt	Yes	No	No	No	Yes	No
16	ULP-Peripheral I2S Interrupt	Yes	No	No	No	Yes	No
17	ULP-Peripheral I2C Interrupt	Yes	No	No	No	Yes	No
18	ULP-Peripheral UART Interrupt	Yes	No	No	No	Yes	No
19	ULP-Peripheral ADC/DAC Interrupt	Yes	No	No	No	Yes	No
20	ULP-Peripheral DMA Interrupt	Yes	No	No	No	Yes	No
21	ULP-Peripheral GPIO Wakeup Interrupt	Yes	No	No	No	Yes	No
22	ULP-Peripheral Touch Sensor Interrupt	Yes	No	No	No	Yes	No
23	ULP-Peripheral Timer Interrupt	Yes	No	No	No	Yes	No
24	ULP-Peripheral VAD Interrupt	Yes	No	No	No	Yes	No

Table 87 List of Wakeup Sources in different states

5.5 Digital and Analog Peripherals and Interfaces

In addition to the wireless interfaces, RS14100 provides a rich set of peripherals and interfaces - both digital and analog - thus enabling varied systems and applications. The following are the categories of the peripherals and interfaces, description of each category and list of the peripherals in that category:

5.5.1 Digital Peripherals and Interfaces

5.5.1.1 CAN Controller

- Conforms to Bosch CAN 2.0B specifications.
- Supports 11 and 29 bit wide message identifiers
- Supports data rate up to 1 Mbps
- Supports hardware message filtering (dual/single filters)
- 64-byte receive FIFO, 16-byte transmit buffer
- Overload frame is generated on FIFO overflow
- Normal & Listen-only modes supported
- Supports single shot transmission
- Ability to abort transmission
- Supports readable error counters
- Supports Last Error Code
- Programmable clock frequency

- Supports generation of interrupt for different events

5.5.1.2 I2C

- Up to three I2C master/slave controllers - two in MCU HP peripherals and one in MCU ULP subsystem
- I²C standard compliant bus interface with open-drain pins
- Configurable as Master or Slave
- Four speed modes: Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1Mbps) and High-Speed Mode (3.4 Mbps)
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Support for Clock synchronization and Bus Clear
- Programmable SDA Hold time

The I²C controllers also support additional features listed below to reduce the load on the processor:

- Integrated transmit and receive buffers with support for DMA
- Bulk transmit mode in I2C Slave mode
- Interrupt based operation (polled mode also available)

5.5.1.3 UART/USART

- Up to two UART and one USART controllers
- Programmer interface compatible with the 16450
- 9-bit serial data support
- Multi-drop RS485 interface support
- 5, 6, 7 and 8-bit character encoding with even, odd and no parity
- 1, 1.5 (only with 5 bit character encoding) and 2 stop bits
- Hardware Auto flow control (RTS/CTS)
- IrDA 1.0 SIR mode support (only for UART2) with up to 115.2 K baud data rate and programmable pulse duration and low-power reception capabilities

The UART controllers also support additional features listed below, which help in achieving better performance and reduce the burden on the processor:

- Programmable fractional baud rate support
- Programmable baud rate supporting upto 7.3 Mbps
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Prioritized interrupt identification

The following features are supported by the USART controller in the MCU HP peripherals (USART1):

- Support for both synchronous and asynchronous modes.
- Supports full duplex and half duplex (single wire) mode of communication.
- 1-9 bit wide character support.
- Supports programmable baud rates upto 20 Mbps in synchronous mode
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events.

The USART controller in the MCU ULP subsystem (ULP_USART) supports the following additional power-save features:

- After the DMA is programmed in PS2 state for USART transfers, the MCU can switch to PS1 state (processor is shutdown) while the USART controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the USART controller completes the data transfer and, triggered by the Peripheral Interrupt, shifts either to the sleep state (without processor intervention) or the active state

5.5.1.4 I²S / PCM

- Up to two I²S controllers
- Each I²S supports PCM mode of operation
- The I²S_2CH supports two stereo channels while the ULP_I²S and the NWP/Security subsystem I²S support one stereo channel
- Programmable Audio data resolutions of 12, 16, 20 and 24
- Supported audio sampling rates are 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96 and 192 kHz
- Support for master and slave modes
- Full duplex communication due to the independence of transmitter and receiver

The PCM mode of operation supports the following additional features:

- Mono audio data is supported
- Supports two modes for data transmission with respect to the Frame Synchronization signal – the MS bit is transmitted in the same clock cycle as the Frame Synchronization signal is asserted or one clock cycle after the Frame Synchronization signal is asserted
- Programmable FIFO thresholds with maximum FIFO depth of 8 and support for DMA
- Supports generation of interrupts for different events

The I²S in the MCU ULP subsystem supports the following additional power-save features:

- After the DMA is programmed in PS2 state for I²S transfers, the MCU can switch to PS1 state (processor is shutdown) while the I²S controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the I²S controller completes the data transfer and, triggered by the Peripheral Interrupt, shifts either to the sleep state (without processor intervention) or the active state

5.5.1.5 Quadrature Encoder Interface (QEI)

- Tracks encoder wheel position
- Programmable for 1x, 2x or 4x position counting. Increments/decrements depending on direction
- Index counter for revolution counting
- Velocity capture using built-in timer.
- Supports position counter reset for rollover/underflow or Index pulse
- Position, Index and Velocity compare registers with interrupts
- Supports logically swapping the A and B inputs
- Accepts decoded signal inputs (clock and direction) in timer mode

5.5.1.6 Motor Control PWM

- Part of the MCU HP peripheral subsystem
- Supports upto eight PWM outputs with four duty cycle generators
- Complementary and Independent output modes are supported
- Dead time insertion in Complementary mode
- Manual override option for PWM output pins. Output pin polarity is programmable
- Supports generation of interrupt for different events
- Supports two hardware fault input pins
- Special event trigger for synchronizing analog-to-digital conversions

5.5.1.7 Synchronous Serial Interface (SSI) Master

- Up to two Synchronous Serial Interface (SSI) masters
- Support for Motorola SPI, TI SSP and National Semiconductors Microwire protocols
- The SSI_MST provides an option to connect upto four slaves and supports Single, Dual and Quad modes.

- The ULP_SSI_MST supports Single-bit mode and can be connected to only one slave
- Programmable receive sampling delay

In addition to the above features, the SSI Masters reduce the load on the processor by supporting the features below:

- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events.
- Programmable division factor for generating SSI clock out.

The ULP_SSI_MST supports following additional power-save feature:

- After the DMA is programmed in PS2 state for SSI transfers, the MCU can switch to PS1 state (processor is shutdown) while the SSI Master continues with the data transfer
- In PS1 state (ULP Peripheral mode) the SSI Master completes the data transfer and, triggered by the Peripheral Interrupt, shifts either to the sleep state (without processor intervention) or the active state

5.5.1.8 Synchronous Serial Interface (SSI) Slave

- Support for SSI Masters which comply with Motorola SPI, TI SSP and National Semiconductors Microwire protocols
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events

5.5.1.9 Serial Input Output (SIO)

- Can be used to implement serial interfaces like I2C, UART and SPI protocols
- Supports eight GPIO pins
- Supports eight SIOs
- Supports Pattern matching
- Performs serial to parallel and parallel to serial conversion
- Provides DMA flow control signals
- Supports generation of interrupt for different events.
- Programmable clock division factors for generating SIO clock out

5.5.1.10 Configurable Timers

- Supports 8 configurable inputs and 8 outputs signals
- Supports four 32-bit configuration timers
- Each 32-bit timer can be configured to contain one 32-bit or two 16-bit timers. It take clocks or events as a tick
- Wide range of features like starting the counter, stopping the counter, continuing the counter from the stopped value, halt, increment the counter and capturing the events
- Support for PWM signals as output with any cycle/pulse length and superimpose a waveform on the PWM signal. It can start the ADC at any time in sync with PWM signal
- Support for DMA flow control
- Generates interrupt for different events

5.5.1.11 CRC Accelerator

- Part of MCU HP peripheral subsystem
- Support for one 32 bit polynomials
- Support for one 32 bit stream-in data widths
- Supports DMA flow control

5.5.1.12 Enhanced GPIO (EGPIO)

- Two EGPIO controllers - one in MCU HP and MCU ULP subsystem
- Supports various alternate functions like set, clear, toggle on all the pins
- Option to program Mode for the each GPIO pin independently

- Supports edge and level detection based on which interrupts will be raised.
- MCU HP GPIO supports 8 pin, 4 wakeup and 4 group interrupts. MCU ULP GPIO supports 8 pin, 2 wakeup and 2 group interrupts

5.5.1.13 Generic SPI Master

- Part of MCU HP peripheral subsystem
- Supports single bit SPI master mode.
- Support for Mode-0 and Mode-3 (Motorola)
- Supports both Full speed and High speed modes
- SPI clock out is programmable to meet required baud rates
- Support for full duplex mode
- Connect upto four SPI peripheral devices
- Support byte swapping during read and write operation
- Support upto 32 KB of read data from a SPI device in a single read operation
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Generates interrupt for different events

5.5.1.14 Hardware Random Number Generator

- Part of MCU HP peripheral subsystem
- Supports 32-bit True Random Number Generator
- Supports 32-bit Pseudo Random Number Generator
- Option to selectively enable these random number generators

5.5.1.15 Ethernet Controller

- Part of MCU HP peripheral subsystem
- Supports 10/100 Mbps data transfer rates in compliant with IEEE 802.3
- RMII interface to communicate with an external Ethernet PHY
- Supports both full-duplex and half-duplex operation
- Option for Automatic Pad/CRC Stripping on receive frames
- Supports Internal DMA
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports variety of flexible address filtering modes
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces to the Application
- Option for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
- Supports generation of interrupt for different events

5.5.1.16 SD Memory and IO Host Controller (SMIHC) Controller

- Part of MCU HP peripheral subsystem

Spec Compliance

- Compliant to SD Host Controller Standard Specification Version 3.0
- Compliant to SD 3.0 Physical Layer Specification Version 3.01
- Compliant to SDIO Specification Version 3.0
- Compliant to JEDEC JESD84-B50 eMMC 5.0 Specification

SD3.0 Supported Features

- UHS modes are supported - SDR50/DDR50

- Clock Tuning
- Asynchronous Interrupt Support
- SDSC/SDHC/SDXC/SDHS Cards

MMCA 5.0 Supported Features

- Supports Extended Security Commands
- Supports eMMC mode
- Data Tag Mechanism and Packet Commands support for eMMC
- Supports DDR mode
- MMC plus and MMC mobile cards

General Supported Features

- Suspend/Resume
- Read Wait
- SD/MMC Bus Width are 1,4 and 8bits
- Supports Internal DMA
- Supports generation of interrupt for different events

5.5.1.17 General Purpose DMA (GPDMA)

- Two masters interface over AHB bus
- Supports 8 channels
- Linked-list based descriptors
- Has two AHB masters for parallel data transfer. Master is selectable for descriptor fetch, per channel and per source and destination
- Dynamically configurable FIFO for 8 channels
- Programmable source and destination burst sizes
- Programmable beats per bursts
- Source and Destination address alignment
- Programmable Transfer Types: Memory to Memory, Memory to Peripheral and Peripheral to Memory
- Programmable priority encoded arbiter
- Supports generation of interrupt for different events
- Support for DMA squash
- Support for memory Zero Fill and One Fill

5.5.1.18 Micro DMA (uDMA)

- Supports 32 channels
- Each DMA channel has dedicated handshake signals and programmable priority level
- Supported transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Supports multiple DMA cycle types and transfer data widths
- Programmable number of transfers in a single DMA cycle
- Average throughput is four cycles per one word reading
- Each DMA channel can access a primary, and alternate, channel control data structure
- Supports generation of interrupt for different events
- Support half-word (16 bit) and word (32 bit) size transfers

5.5.1.19 eFuse Controller

- Provides 32 bytes eFuse as one-time programmable memory locations

- Supports eFuse programming and read operations
- Supports memory mapped and FSM based read operation
- Supports Key Loading to security blocks

5.5.1.20 Filter-Interpolation-Multiplication (FIM)

FIM is used in a wide range of applications for performing complex operations like Filtering, Interpolation, Multiplication and Add/Subtract operations.

- Supported complex operations:
 - FIR Filtering.
 - IIR Filtering.
 - Interpolation.
 - Scalar Addition.
 - Scalar Subtraction.
 - Scalar Multiplication.
 - Vector Addition.
 - Vector Subtraction.
 - Vector Multiplication.
 - NORM Square computation.
 - Matrix Multiplication.
- Maximum input length of 1023 for Addition, Subtraction and Multiplication.
- Maximum output length of 1023 for Filtering and Interpolation.
- Supports fixed point operations through programmable shifting.
- Supports inputs with 32-bit precision for Real operations and 16-bit precision for Complex operations.
- Supports the saturation on the Output Data.
- Interface with ULP-SRAM (16KB) for Inputs and Outputs.
- Interrupt Generation for Processor wakeup from Standby states.

5.5.1.21 SPI Flash Controller

The SPI Flash Controller is a 1/2/4/8-wired interface for serial access of data from Flash. It can be used in either Single, Dual, Quad or Octa modes with support for SDR and DDR to read the Processor's instructions and for data transfers to/from the Flash. The Controller supports inline decryption of encrypted instructions read from the Flash before they are passed on to the Processor's Instruction Cache. Instructions are read using the Direct Fetch mode while data transfers use the Indirect Access mode. The SPI Flash Controller in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with Flash ICs from multiple vendors. The Direct Fetch mode is used to read instructions and data directly from Flash without any processor intervention. It supports inline decryption using an AES engine for the instructions stored in Flash. The Indirect Access mode is used to read and write data/instructions from Flash. The two modes - Direct Fetch and Indirect Access - can be used to access the same Flash or two different Flashes (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The SPI Flash Controller has independent AHB slaves for these modes of access.

- Supports Single/Dual/Quad/Octa (S/D/Q/O) modes for reading processor instructions and data transfers to/from Flash.
- Support for SPI Mode-0 and Mode-3
- Support for both SDR and DDR mode Flashes
- Supports both 8 and 16-bit Flash commands.
- Support both 24 and 32-bit addressing modes
- Supports inline decryption (AES) for while reading encrypted instructions from the Flash
- Supports up to two Flashes connected to CSN0 and CSN1
- Direct Fetch Mode:

- Instructions are read from Flash using the Direct Fetch mode which does not need any processor involvement after the initial configuration of the Controller. The read command used for this mode is programmable depending on the Flash used.
- Direct Fetch mode supports Wrap / Incremental / Single read operations.
- Supports prefetch option - enabling this option makes the SPI Controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
- Supports continuous fetch option to reduce instruction fetch delay from Flash - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
- Supports programmable CSN high time.
- Indirect Access Mode:
 - Configuration of Flash and reading/writing data from/to the Flash uses the Indirect Access mode which requires the processor to program the SPI Flash controller for each access.
 - Supports reading of up to 32KB bytes of data from Flash in a single read operation.
 - In addition to 24 and 32-bit addressing, the SPI Controller supports 9, 10 and 16-bit addressing in this mode.
- Clock Configuration
 - Support for selection of source clock between AHB bus clock and PLL clock.
 - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Transmission of Extra-byte after the address phase is supported. The contents of this byte are programmable. There is also an option to only transmit the first nibble of the extra byte and maintain a Hi-z on the bus for the next nibble.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the Flash requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports dual Flash mode - reading of data from two flashes simultaneously.
- Supports Flash Write Protect
- Supports interrupt generation based on different events

5.5.1.22 Watchdog Timer

The WatchDog Timer is used to generate an interrupt on timeout and a reset in case of system failure which can be caused by an external event like ESD pulse or due to a software failure. Also the Interrupt can be used as a Wakeup source for transitioning from SLEEP/STANDBY to ACTIVE states.

- Independent watchdog timer.
- Interrupt is generated before the system reset is applied which can be used as a wakeup source.
- Generates reset upon Lockup indication from Processor.
- Configurable low frequency clock (32KHz RO, RC and Xtal).
- Configurable timeout period.
- Able to operate when CPU is in SLEEP state during power-save applications
- Individually controllable power domain for low-power applications.

5.5.1.23 Calendar

Calendar block acts a RTC with time in seconds, minutes, hours, days, months, years and centuries. The real-time can also be read through APB with accuracy less than a second by reading the millisecond count value and further less also by reading the number of counts of APB clock in 1 millisecond of RTC clock. Accuracy is high.

- Calendar block can provide a seconds trigger and also a msec trigger.
- Calendar block takes care of no.of days in each month and also leap years. It can count up to 4 centuries.

- Real time is readable through APB and also programmable through APB.
- Option to choose either RC clock RO clock as calendar clock.

5.5.1.24 General Purpose Timers

The MCU Timer block supports four 32-bit timers, which can be used to generate various timing events for the software. Each of the four timers can be independently programmed to work in periodic or one-shot mode and can be configured either as a microsecond timer or as a counter.

- Four independent 32bit timers
- Supports per timer enable and disable.
- Option to configure each timer as a 32-bit counter or 32-bit microsecond timer.
- Supports 1 μ s mode and 256 μ s modes per timer.
- Accounts for integral and fractional value of the time units programmed.
- Microsecond timer supports two modes:
 - 1 Microsecond mode : The time unit is 1 μ s. Number of microseconds required to be counted has to be programmed.
 - 256microsecond mode : The time unit is 256 μ s. Number of 256 μ s units required to be counted has to be programmed. This is useful when the timer is being used for counting large time values and microsecond based tracking not required.
- One shot and periodic modes per timer.
- Option to interrupt the processor on timeout.

5.5.1.25 Secure Storage

The Block is used for storing configuration values with data protection feature.

- MCU has 3 set's for storage block
 - First chunk is 64 bits.
 - Second chunk is 64 bits
 - Third Chunks is 128 bits
- Each chunk is a power domain.
- Secure mode is available for first and second Chunk.
- Storage space can be used for storing Configuration values

5.5.2 Analog Peripherals and Interfaces

5.5.2.1 Capacitive Touch

- 8 input channels - all the input channels are shared with GPIOs
- 1 shield channel - To reduce sensitivity to mesh capacitance
- Capacitive input and resistor input are connected to two GPIOs each
- Programmable input clock source from the available clocks in the chip
- Controls the rate of scanning for all sensors with configurable inter sensor scan ON time
- Supports both samples streaming and cumulative average mode
- DMA capable
- 8, 16 and 32-bit pseudo-random number for generating two non overlapping streams with configurable delay
- Programmable polynomial and seed values for pseudo-random number generator
- Provides wake up indication after capacitive touch sensing

5.5.2.2 Analog to Digital Converter (ADC)

The ADC with up to 12 bits of resolution at 10 MSPS

- 12 bit ADC Output in 2's complement representation

- GPIO's in High Power mode for ADC Operation
 - Signal Ended Mode
 - 20 External configuration selection
 - 5 Internal configuration selection
 - Internal Temperature sensor
 - 3 Opamps Outputs
 - DAC output for internal reference
 - Differential Mode
 - 10 external differential mode configuration selection
 - 4 Internal configuration selection.
 - 3 Opamps Outputs
 - DAC output for internal reference
- GPIO's in Low Power mode for ADC Operation
 - Signal Ended Mode
 - 14 External configuration selection.
 - 5 Internal configuration selection.
 - - Internal Temperature sensor.
 - 3 Opamps Outputs
 - DAC output for internal reference
 - Differential Mode
 - 6 external differential mode configuration selection.
 - 4 Internal configuration selection.
 - 3 Opamps Outputs
 - DAC output for internal reference
- 10MHz to 32KHz allowed ADC_CLK
- Configurable DAM to support 16 channels for storing AUXADC data. Date is ULP SRAM.
- Measurement range 0 to AUXADC_VREF(1.8v to 3.3v)

The ADC has five modes of operation:

- Single ended input with noise averaging
- Single ended input without noise averaging
- Differential input with noise averaging
- Differential input without noise averaging
- Shutdown mode.

5.5.2.3 Digital to Analog Converter (DAC)

DAC can take 10 bit digital inputs and convert them into analog voltage within range $5*vdd/36$ to $31*vdd/36$. Vdd can vary from 1.8 volts to 3.6 volts.

- 10bit resolution
- Single ended DAC
- Monotonic by design
- Max sampling frequency is 5MHz for DAC_CLK
- supports Operational mode and Shutdown modes

5.5.2.4 OPAMP

- 3 general purpose Operational Amplifiers (OPAMP) offering rail-to-rail inputs and outputs.
- Each of the three opamps has 2 inputs (inp, inn) and 1 output.
- opamps can take inputs from GPIOs and their outputs can be seen on GPIOs
- configured in either low power mode or high power mode
- opamps can be configured as:
 - Unity gain amplifier
 - Trans-Impedance Amplifier(TIA)
 - Non-inverting Programmable Gain Amplifier (PGA)
 - Inverting Programmable Gain Amplifier
 - Non-inverting Programmable hysteresis comparator
 - Inverting Programmable hysteresis comparator
 - Cascaded Non-Inverting PGA
 - Cascaded Inverting PGA
 - Two opamps Differential Amplifier
 - Instrumentation Amplifier

5.5.2.5 Analog Comparators

Analog comparators peripheral consists of two analog comparators, a reference buffer, a scaler and a resistor bank. Both comparators can take inputs from GPIOs.

The comparator compares analog inputs p and n to produce a digital output, cmp_out according to:

p > n, cmp_out = 1

p < n, cmp_out = 0

The following cases of comparison are possible

- Compare external pin inputs
- Compare external pin input to internal voltages.
- Compare internal voltages.

The inputs of 2 comparators can be programmed independently. The reference buffer, scaler and resistor bank are shared between the two comparators and can be enabled only when atleast one of the comparators is enabled.

5.5.2.6 Temperature Sensor

There are two independent temperature sensors integrated. Ring Oscillator(RO) based temperature sensor and BJT based temperature sensor.

BJT based sensor works for temperature range from -40degree to 125degree and voltage variation from 1.8V to 3.6V. It outputs the digital word having resolution of nearly 1 degree C. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor.

RO based sensor outputs 2 clocks. The temperature is determined by counting the clocks and applying an equation.

5.5.2.7 IR Decoder

This is a general purpose Infrared receiver, which can decode all IR protocol (RC5,NEC,.. etc) with Software intervention. It take IR pulses from external IR sensor connected through GPIO's

- IR Decoder clocked by a low power 32 KHz RC clock
- Programmable Active and Sleep window duration for IR data monitoring
- Wakeup source to existing low power sleep state

5.5.2.8 Voice Activity Detection (VAD)

VAD detects voice activity on the samples provided. The samples can be collected through ADC from an Analog Source or I²S from a Digital Source.

- Support Multiple Algorithms based detection

- Zero Crossing (ZCR).
- Auto Correlation Function (ACF).
- Weighted Auto Correlation Function (WACF).
- Average Magnitude Difference Function (AMDF).
- Support flexible storage of samples in Memory.
- Support multiple SRAM banks using ping-pong method for processing samples.

5.6 Boot process and Bootloader

The Bootloader controls the initial operation of the device after any form of reset. The Bootloader supports Flash programming and initial startup of the application code. It also provides APIs to the application code for programming the Flash. Bootloader supports following features:

- Two Bootloaders - Security Bootloader and Application Bootloader
- Support for ISP (In-System Programming) through multiple interfaces - UART, SPI, USB, USB-CDC and SDIO
- Auto-detection of ISP interface
- Support for secure boot
- Support for secure firmware upgrade using PUF based Roots-of-Trust (RoT)
- Anti-rollback protection
- Secure Key Management and Protection
- Support for different flash protection levels and write-protected Flash
- Secure XIP from Flash
- Support for multiple isolated images and selection
- Fail-proof migration of current active firmware to new (update) firmware
- Public key cryptography (digital signature) based authentication
- Provision to move to factory default firmware and keys

The RS14100 includes two Bootloaders - Security Bootloader and Application Bootloader. The Security Bootloader runs on the Security processor and the Application Bootloader runs on the Cortex M4 processor. On any reset, execution will always start in Security Bootloader, which is responsible for all security features, ISP and firmware upgradation. Once the Security Bootloader finishes its tasks, it enables the Application Bootloader. The Application Bootloader is responsible for transferring data to RAM from Flash and also for executing the wakeup sequence.

The following are the sources, which can trigger the Bootloader:

- Primary reset (RESET_N_PAD)
- Power on reset (POC_IN)
- Watchdog reset
- Black out monitor
- Reset request through SYSRESETREQn bit in the Cortex-M4 processor

5.6.1 Secure Bootup

On reset, the Security Bootloader configures the module hardware based on the configuration present in the eFuse. It also passes the required information from the eFuse to the Application Bootloader. The Security Bootloader validates the integrity and authenticity of the firmware in the Flash and invokes the Application Bootloader. It detects and prevents execution of unauthorized software during the boot sequence. The Bootloader uses public & private key based digital signatures to recognize authentic software. The Security Bootloader provides provision for inline execution (XIP) of encrypted firmware from Flash. The Bootloader provides 3 flash protection levels which can be used to secure different sections of the Flash for different purposes:

- Protection level 1: Stored at manufacturing, not allowed to modify by the Security Bootloader

- Protection level 2: Allowed to modify by the Bootloader only, usually used to maintain secure information used/consumed by Bootloader
- Protection level 3: Allowed to modify by the Bootloader only, usually used to maintain protected firmware images.

The protection levels are written to Flash during the manufacturing process. The write-protection feature prevents the application program from changing the Flash protection levels. The Bootloader supports multiple isolated firmware and provision to select the firmware to execute on bootup.

The Security Bootloader is enabled or disabled during the manufacturing process.

5.6.2 Secure Firmware Upgrade

The secure firmware upgrade feature of the Bootloader checks the authenticity of the new firmware image along with its integrity. The Bootloader automatically detects the host interface in use and configures the host interface hardware accordingly. The Bootloader updates the image only after successfully validating the authenticity and integrity of the image. It prevents downgrade to a lower version of firmware using the anti-rollback feature, if it is enabled. The Bootloader also supports transparent migration to a wirelessly updated image and protection against failures by providing recovery mechanisms.

5.6.3 Secure Zone

The Secure Zone provides a secure execution environment to store confidential data and to run secure applications. The Bootloader configures Secure Zone, secure firmware upgrade and secure bootup in "Secure Zone enabled" mode. This mode is programmed during the manufacturing process.

5.6.4 In-System Programming (ISP)

In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART, SPI, USB, USB-CDC and SDIO (GPIO-25 to GPIO-30) interfaces. This can be done after the part is integrated on end-user board. Boot loader can be requested to boot in ISP mode by pulling down a specific GPIO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes use JTAG pins for functional use. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash.

5.7 Trace and Debug Support

MCU implements complete hardware debug solution. This provides high system visibility of the processor and memory through either a traditional JTAG port or a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices. For system trace, the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin. The Embedded Trace Macrocell (ETM) delivers unrivaled instruction trace capture in an area far smaller than traditional trace units, enabling to implement full instruction trace for the first time.

In Serial Wire Viewer (SWV) mode, a one-bit serial protocol is used and this reduces the number of output signal to one, but the maximum bandwidth for trace output will also be reduced. When combining SWV with Serial-Wire debug protocol, the Text Data Output (TDO) pin normally used for Joint Test Action Group (JTAG) protocol can be shared with SWV

The Trace Port Interface Unit (TPIU) is used to output trace packets from the Instrumentation Trace Macrocell (ITM), Data Watchpoint and Trace (DWT), and Embedded Trace Macrocell (ETM) to the external capture device.

The Cortex-M4 TPIU supports two output modes:

- Clocked mode, using up to 4-bit parallel data output ports
- SWV mode, using single-bit SWV output

5.8 Wireless Subsystem

The wireless subsystem is an ultra-low-power, single spatial stream, 802.11n + BT/BLE5.0 Convergence. The wireless subsystem has low-cost CMOS integration of a multi-threaded MAC processor (threadArch®), baseband digital signal processing, analog front-end, calibration eFuse, 2.4GHz and 5GHz RF transceiver, integrated power amplifier, and Quad-SPI Flash thus providing a fully-integrated solution for a range of embedded wireless applications.

5.8.1 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n, 802.11j (hosted mode) with integrated radio, modem, and MAC in the 2.4-GHz and 5-GHz ISM band
- Support for 20 MHz and 40 MHz channel bandwidths
- Supports all common Wi-Fi security modes for personal and enterprise networks, with on-chip security accelerators
- Support for Client mode, Access point mode, Wi-Fi Direct, Concurrent Client and Access Point mode, Enterprise Security
- Transmit power up to +18 dBm with integrated PA in 2.4 GHz band and +13.5 dBm in 5 GHz band
- Receive sensitivity as low as -96.5 dBm in 2.4 GHz band and -89 dBm in 5 GHz band
- Data Rates:- 802.11b: Upto11 Mbps ; 802.11g: Upto54 Mbps ; 802.11n: MCS0 to MCS7

5.8.1.1 MAC

- Conforms to IEEE 802.11b/g/n/j standards for MAC
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, and WMM support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH for WAPI

5.8.1.2 Baseband Processing

- Supports DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, 54 Mbps, MCS0 to MCS7)
- Supports IEEE 802.11n single-stream modes with data rates up to 150 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

5.8.2 Bluetooth

- Transmit power up to +18 dBm with integrated PA
- Receive sensitivity:- LE: -93 dBm, LR 125 Kbps: -104 dBm
- <8 mA transmit current in BT 5 mode, 2 Mbps data rate
- Supports BT EDR+2.1, 4.0, 4.1, 4.2 and 5.0
- Supports Piconet with Seven active logical links. Scatternet with two slave roles while still being visible.
- Bluetooth security features: Authentication, Pairing, and Encryption
- BLE Secure connections
- BLE supports 8 center roles and 2 peripheral roles concurrently.
- BT auto rate and auto TX power adaptation
- Supports low power connection states such as sniff and sniff sub-rating modes.
- 3-wire MWS coexistence
- Adaptive Frequency Hopping, Interlaced scanning, Quality of Service, Channel Quality Driven Data Rate

- Channel assessment algorithm provides a fast and accurate determination of occupied channels for use in adaptive frequency hopping (AFH) mode.
- Configurable in 2 modes, hosted (with HCI) and fully embedded (without HCI) with profiles available
- I2S/PCM interface for digital audio
- Data rates:
 - BT: 1 Mbps, 2Mbps, 3 Mbps
 - BLE: 1Mbps, 2Mbps and Long Range modes (125 kbps, 500 kbps).

5.8.2.1 MAC

5.8.2.1.1 Link Manager

- Creation, modification & release of logical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Services the data transport requests from L2CAP and provides required QOS
- Support for security using ECDH hardware accelerator

5.8.2.1.2 Link Controller

- Encodes and decodes header of BT packets
- Manages flow control, acknowledgment, retransmission requests, etc.
- Stores the last packet status for all logical transports
- Chooses between SCO & ACL buffers depending on the control information coming from BBP resource manager
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

5.8.2.1.3 Host Controller

- Receives & decodes the HCI commands received from the Bluetooth Host.
- Propagates the decoded commands to respective modules
- Responsible for transmitting and receiving packets from and to Host
- Formats the responses coming from other modules of Bluetooth Controller as events and sends them to the Host.

5.8.2.1.4 Device Manager

- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BT Device operations except data transport operations
- Storing link keys
- BT Controller state transition management
- Slot synchronization & management
- Access contract management
- Scheduler

5.8.2.2 Baseband Processing

- Supports GFSK (1 Mbps), EDR-DQPSK, EDR-D8PSK
- Supports BLE and Bluetooth long range
- Supports Data rates up to 3 Mbps

5.8.3 RF Transceiver

- Integrated 2.4 GHz transceiver with highly programmable operating modes
- Integrated 5 GHz transceiver with highly programmable operating modes
- Integrated matching networks and diplexers
- Integrated antenna with additional U.FL connector
- Internal oscillator with 40 MHz crystal
- Inbuilt automatic boot up and periodic calibration enables ease of integration

5.8.3.1 Receiver and Transmitter Operating Modes

The 9116 radio is highly configurable. The available radio operating modes are

- WLAN 2G HP TX - WLAN 2G High-Performance Transmitter
- WLAN 2G HP RX - WLAN 2G High-Performance Receiver
- WLAN 2G LP RX - WLAN 2G Low-Power Receiver
- WLAN 5G TX - WLAN 5G Transmitter
- WLAN 5G RX - WLAN 5G Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter
- BLE LP RX - Bluetooth LE Low-Power Receiver
- BT HP TX - Bluetooth Classic High-Performance Transmitter
- BT HP RX - Bluetooth Classic High-Performance Receiver
- BT LP TX - Bluetooth Classic Low-Power Transmitter EDR rates are not supported.
- BT LP RX - Bluetooth Classic Low-Power Receiver. EDR 3Mbps rate is not supported.

5.8.4 Wireless Software

The wireless software package supports Embedded Wi-Fi Client mode, Wi-Fi Access point mode, Wi-Fi Direct, Enterprise Security and dual-mode BT 5.0 functionality. The software package includes complete firmware and application profiles. It has a wireless coexistence manager to arbitrate between protocols.

5.8.4.1 Wireless Co-Existence Manager

- Arbitration between WiFi, BT, and BLE
- Application-aware arbitration
- Adaptive frequency hopping (AFH) in BT is based on WLAN channels usage
- Pre-inter thread interrupts generation for radio switching
- QoS assurance across different traffics

5.8.4.2 Network Stack

5.8.4.2.1 WiFi

- Integrated IPv4, IPv6, and TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU
- Support of 10 simultaneous TCP, UDP, or RAW sockets
- Support of 2 simultaneous SSL3.0\TLS1.2 sockets
- Built-in network protocols:
 - Static IP, DHCPv4, DHCPv6 with DAD and Stateless Autoconfiguration
 - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND

- DNS client for easy connection to the local network and the Internet
- IGMP
- DNS-SD
- SNMP
- FTP client
- POP3
- SNTP
- SMTP
- Built-in Web Socket
- Built-in network application and utilities:
 - HTTP/HTTPS
- Web page content stored on serial Flash
- APIs for setting\configuring application content
- Service discovery: Multicast DNS service discovery allows a client to advertise its service without a centralized server.
- DHCP server
- Ping

5.8.4.2.2 Bluetooth stack protocols

- L2CAP
- AVDTP
- AVCTP
- RFCOMM
- SDP
- ATT
- SMP

5.8.4.2.3 Bluetooth Profiles

- SPP
- A2DP
- AVRCP
- HFP
- PBAP
- IAP
- GAP
- GATT
- IAP1
- IAP2
- HID

5.8.4.3 Security

Wireless software supports multiple levels of security including FIPS 140-2 and PUF (Physically Unclonable Function) to create a highly secure system. This enhances the security capabilities available for the development of IoT devices.

5.8.4.3.1 Wifi

- Personal standards
 - WPA2-PSK

- WPA-PSK
- WEP
- Mixed mode
- Enterprise standards for client mode
 - EAP-TLS
 - EAP-FAST
 - EAP-TTLS
 - EAP-PEAP
 - EAP-LEAP
 - PEAP-MSCHAP-v2
- Secure Sockets
 - Protocol versions: SSL v3/TLS 1.0/TLS 1.1/TLS 1.2
 - On-chip powerful crypto engine for fast, secure Wi-Fi and internet connections
 - Server authentication
 - Client authentication
 - Socket upgrade to secure socket
- Secure HTTP server (HTTPS).

5.8.4.3.2 Bluetooth

- Authentication
- Pairing
- Encryption
- BLE Secure connections

5.8.4.3.3 Accelerators

The RS14100 chipset integrates multiple powerful on-chip accelerators for fast and secure connections.

5.8.4.3.3.1 AES

- Supports key expansion for 128/192/256 bit length cipher keys.
- Supports Encryption/Decryption of data in blocks of 128bits.
- Supports ECB and CBC modes.
- Supports MIC computation

5.8.4.3.3.2 SHA

- SHA is a Digital Signature Algorithm (DSA) compliant to Digital Signature Standard (DSS).
- Generates message digest (condensed representation of a message) of 160/224/256-bit length for input in multiples of 512 bits and 384/512-bit length for input in multiples of 1024 bits.
- SHA generates a unique message digest for a unique message sequence.

5.8.4.3.3.3 HMAC

- Capable of performing HMAC for SHA types SHA-1, SHA-224, SHA-256, SHA-384, SHA-512
- Support for inputting the key only once and to perform HMAC on different sets of messages.

5.8.4.3.3.4 Diffie-Hellman (DH)

- Supports key size up to 2048 bits
- Supports multiplication for different sizes of vectors
- Supports exponentiation for variable exponent sizes
- Generates interrupt on completion of Exponentiation loop

5.8.4.3.3.5 ECDH

- Supports 192 and 256bit Elliptical curve DH
- Supports Point doubling, addition, and multiplication

5.8.4.3.3.6 CRC Accelerator

- Support for one 32 bit polynomials
- Support for one 32 bit stream-in data widths
- Supports DMA flow control

5.8.4.3.3.7 Hardware Random Number Generator

- Supports 32-bit True Random Number Generator
- Supports 32-bit Pseudo Random Number Generator
- Option to selectively enable these random number generators

5.8.4.3.3.8 eFuse controller

- Provides 512 bytes eFuse as one-time programmable memory locations
- Supports eFuse programming and read operations
- Supports memory mapped and FSM based read operation
- Supports Key Loading to security blocks

5.8.5 Wireless Subsystem Peripherals

RS14100 chipsets integrate a wide range of peripheral to enable several connectivity applications.

5.8.5.1 I2S / PCM

- Support for master and slave modes
- Each I2S supports PCM mode of operation
- I2S support one stereo channel
- Programmable Audio data resolutions of 12, 16, 20 and 24
- Supported audio sampling rates are 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96 and 192 kHz
- Full duplex communication due to the independence of transmitter and receiver
- Programmable FIFO thresholds with maximum FIFO depth of 8 and support for DMA
- Supports the generation of interrupts for different events

The PCM mode of operation supports the following additional features:

- Mono audio data is supported
- Supports two modes for data transmission with respect to the Frame Synchronization signal – the MS bit is transmitted in the same clock cycle as the Frame Synchronization signal is asserted or one clock cycle after the Frame Synchronization signal is asserted

5.8.5.2 I2C

- Supports both I2C master/slave controller
- I²C standard compliant bus interface with open-drain pins
- Configurable as Master or Slave
- Four-speed modes: Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1Mbps) and High-Speed Mode (3.4 Mbps)
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Support for Clock synchronization and Bus Clear

- Programmable SDA Hold time

The I²C controllers also support additional features listed below to reduce the load on the processor:

- Integrated transmit and receive buffers with support for DMA
- Bulk transmit mode in I²C Slave mode
- Interrupt based operation (polled mode also available)

5.8.5.3 UART

- Programmer interface compatible with the 16450
- 9-bit serial data support
- Multi-drop RS485 interface support
- 5, 6, 7 and 8-bit character encoding with even, odd and no parity
- 1, 1.5 (only with 5-bit character encoding) and 2 stop bits
- Hardware Auto flow control (RTS/CTS)

The UART controllers also support additional features listed below, which help in achieving better performance and reduce the burden on the processor:

- Programmable baud rate support
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Interrupt based operation (polled mode also available)
- Supports the generation of interrupts for different events

5.8.5.4 LED

- Programmable ON and OFF periods that control the duration of the LED blink.
- Supports the following modes
 - Continuous LED ON
 - Continuous LED OFF
 - Continuous blinking mode
 - Event Blinking mode(Blinks only when events are detected)
- Can be configured for monitoring hardware/firmware events

5.8.6 Low power modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Low Power (LP) mode with only the host interface active
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to LP or ULP modes

5.8.6.1 ULP mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 KHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer

- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

5.8.7 Wireless Subsystem Memory

5.8.7.1 On-chip memory

The ThreadArch® processor has the following memory:

- On-chip SRAM of 384K/256K/192K/128Kbytes based on chip configuration
- 512Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 512 bytes (used to store primary boot configuration, security and calibration parameters)

5.8.7.2 Serial Flash

The Wireless subsystem utilizes a serial Flash to store processor instructions and other data. The SPI Flash Controller is a 1/2/4-wired interface for serial access of data from Flash. It can be used in either Single, Dual or Quad modes. Instructions are read using the Direct Fetch mode while data transfers use the Indirect Access mode.

5.9 Pad Configuration

There are multiple processor sub-systems containing SZP (Secure Zone Processor), MCU HP (High Performance) and MCU ULP (Ultra Low Power) which share these common set of GPIO pads. These GPIO pads are controllable by either SZP, MCU HP or MCU ULP. PAD selection register has to be programmed to control the PAD behavior for each GPIO. The SZP and MCU HPGPIOS are available only in PS4/PS3 power states whereas MCU ULP GPIOs are available in all the power states except sleep modes. The UULP Vbat GPIOs are available in all power states.

The SZP, MCU HP and MCU ULP GPIOs PAD are programmable, multi-voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS (Low Voltage CMOS) input or LVCMOS Schmitt trigger input and programmable pull-up/pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200MHz can be achieved under small capacitive loads.

The following PAD configurations can be controlled by software for SZP, MCU HP and MCU ULP GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8V, 2.5V, 2.8V, 3.0V, 3.3V)
- Power-on-Start (POS) capable
- Optimized for EMC (low di/dt switching supply noise) with SSO (Simultaneous Switching Output) factor of 8
- Four (4) Programmable output drive strengths (rated 2mA, 4mA, 8mA, and 12mA)
- Selectable output slew-rate (slow / fast)
- Open drain output mode (Logic low or high on input and use OEN as data input)
- LVCMOS/LVTTL compatible input with selectable hysteresis
- Programmable input options (pull-up, pull-down, repeater, or plain input)
- No power sequence requirements, I/Os are tri-stated when core power is not valid (POC control). These are tri-stated even if the system is under reset or in the deep sleep power state.

The following PAD configurations can be controlled by software for UULP Vbat GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8V, 2.5V, 2.8V, 3.0V, 3.3V)

6 RS14100 CA1/CC1 module Reference Schematics, BOM and Layout Guidelines

6.1 Schematics

The below diagram shows the typical schematic for RF Transceiver and WiSe-MCU applications.

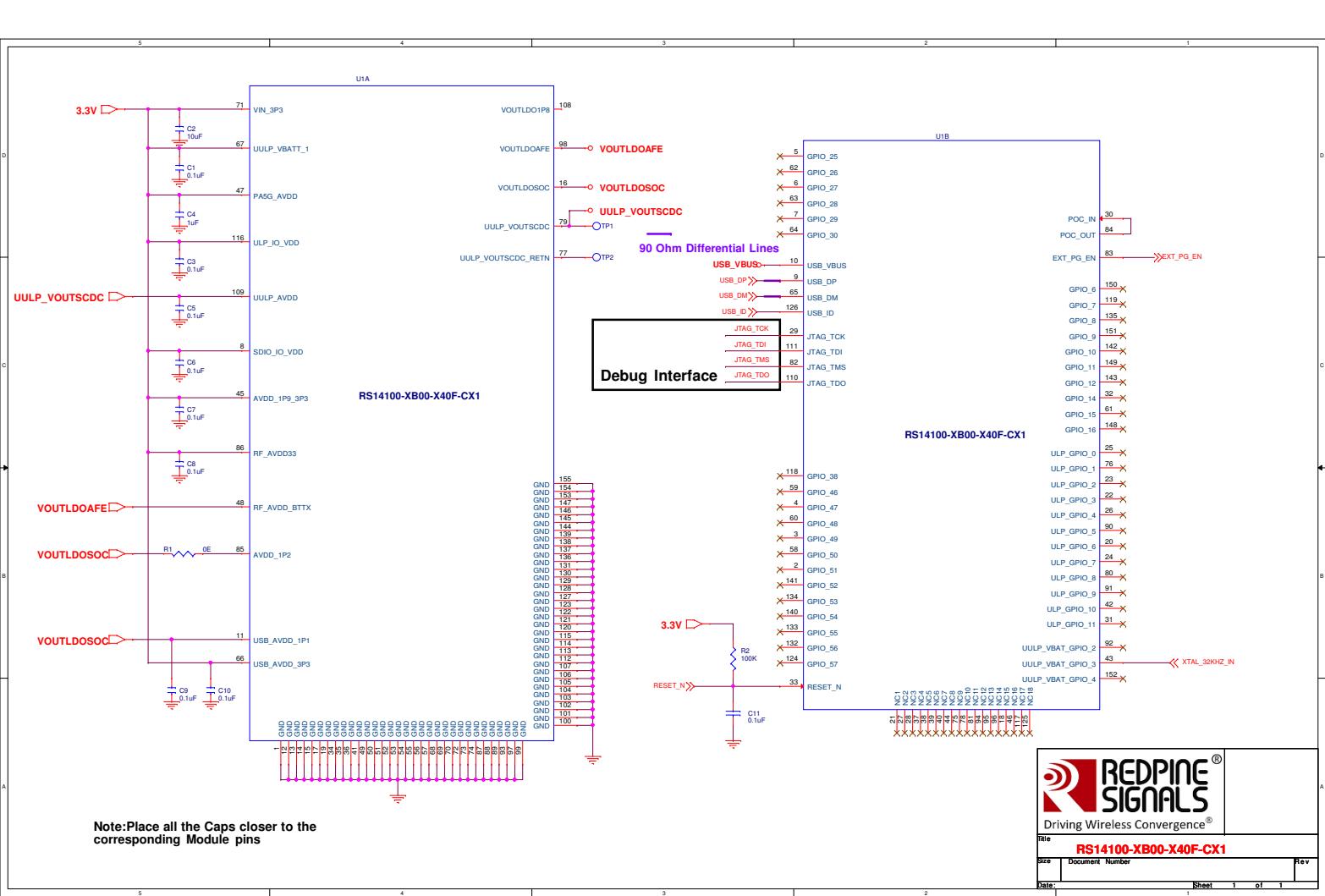


Figure 46 Schematics

1. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
2. Capacitor "C9 and C10" needs to be populated only if USB/USB-CDC interface is used.
3. Supplies "USB_AVDD_1P1" and "USB_AVDD_3P3" needs to be driven only if USB/USB-CDC interface is used

6.2 Bill of Materials

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	1	C2	10uF	CAP CER 10UF 10V X5R 0805	0805	Murata	GRM21BR61A106KE19L
2	1	C4	1uF	CAP CER 1UF 10V 10% X5R 0402	0402	Murata	GRM155R61A105KE15D
3	9	C1,C3,C5,C6,C7,C8,C9, C10,C11	0.1uF	CAP CER 0.1UF 10V X5R 0402	0402	Murata	GRM155R61A104KA01D
4	1	R1	0E	RES SMD 0 OHM JUMPER 1/16W 0402	0402	Yageo	RC0402JR-070RL
5	1	R2	100K	RES SMD 100K OHM 5% 1/16W 0402	0402	Yageo	RC0402JR-07100KL
6	1	U1		Single/Dual Band Wireless MCU Module		Redpine	RS14100-SB00-240F-CA1 / RS14100-SB00-140F-CA1 / RS14100-DB00-240F-CC1 / RS14100-DB00-140F-CC1

Table 88 Bill of Materials

6.3 Layout Guidelines

The following guidelines outline the integration of the module:-

1. The following Supply Pins needs to be STAR routed from the Supply Source VINBCKDC

1. VIN_3P3
2. UULP_VBATT_1
3. PA5G_AVDD
4. ULP_IO_VDD
5. SDIO_IO_VDD
6. AVDD_1P9_3P3
7. RF_AVDD33

2. There should be no metal planes or traces in the region under the PCB antenna and beside it for at least 3 mm. The module should be placed such that the antenna portion is on the edge of the PCB.

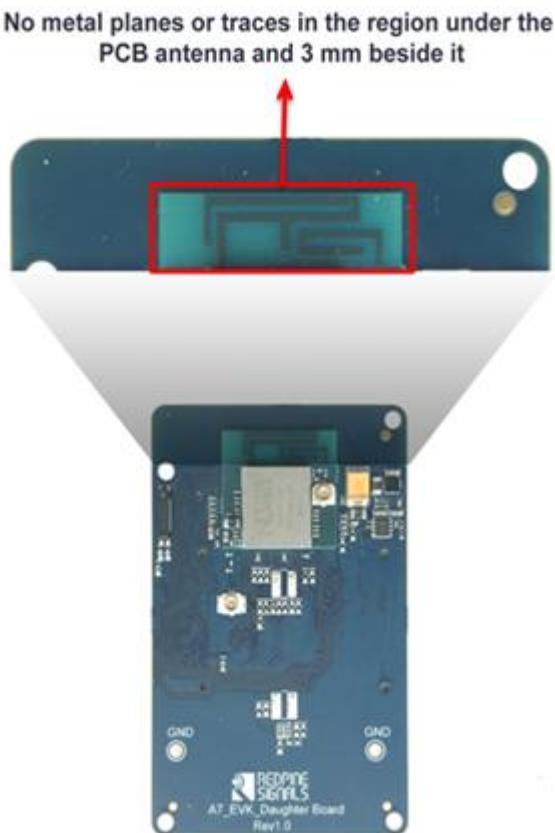


Figure 47 PCB Antenna Guidelines

3. For USB, it is recommended that the components and their values in the BoM be adhered to.

4. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (say, a) which achieves 90Ω of differential impedances, 45Ω for each trace.

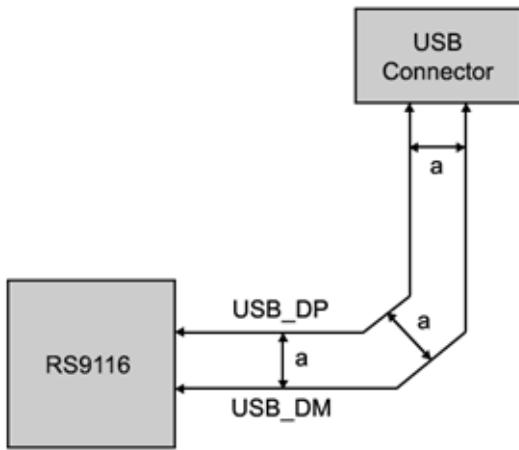


Figure 48 Spacing between USB_DP and USB_DM

5. In order to minimize crosstalk between the two USB differential signals (USB_DP and USB_DM) and other signal traces routed close to them, it is recommended that a minimum spacing of $3 \times a$ be maintained for low-speed non-periodic signals and a minimum spacing of $7 \times a$ be maintained for high-speed periodic signals.

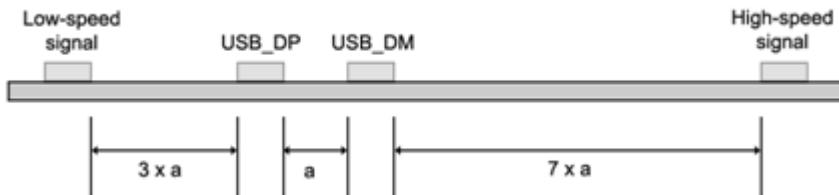


Figure 49 Spacing for Low-speed and High-speed signals around USB_DP/USB_DM

6. It is recommended that the total trace length of the signals between the RS9116 module and the USB connector be less than 450mm.

7. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer2 is a Ground plane. Furthermore, there must be only one ground plane under high-speed signals in order to avoid the high-speed signals crossing to another ground plane

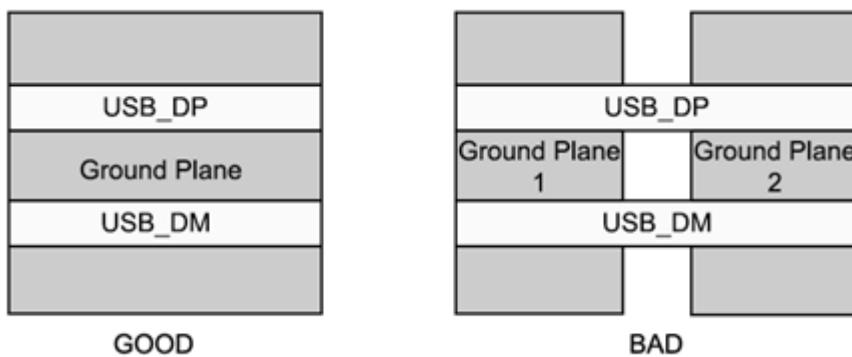


Figure 50 USB Signals and the Ground Plane

The details of u.FL connector for external antenna :-

The module with integrated antenna comes with an option to connect an external antenna through a u.FL connector. The choice between the on board antenna and the external antenna can be made through a software command. The figures below show the u.FL connector integrated on the module. The connector on the external antenna should be pushed down to fit into the u.FL connector connected to the module.

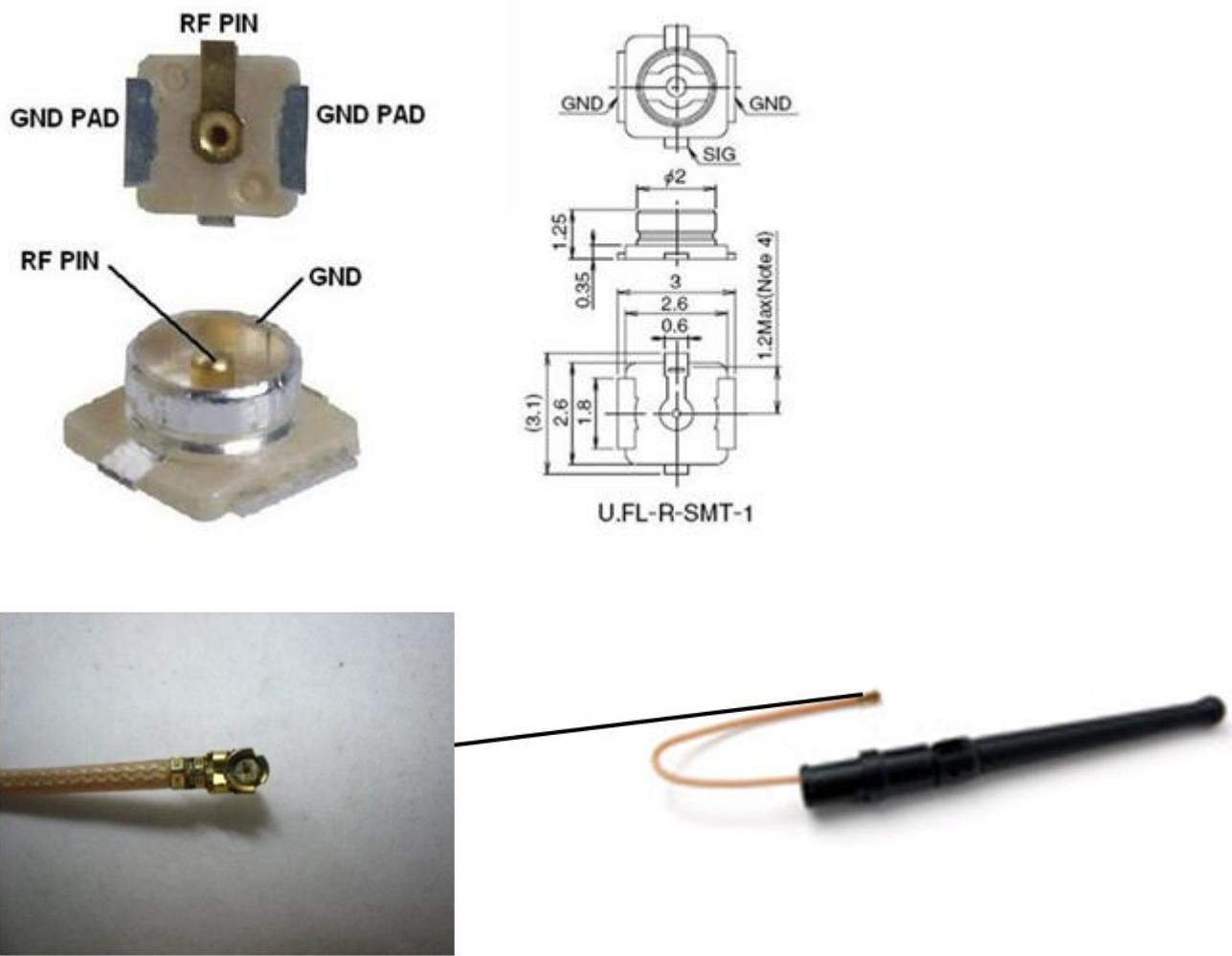


Figure 51 External Antenna

7 RS14100 CA1/CC1 module Storage, Handling and Soldering Conditions

7.1 Recommended Reflow Profile

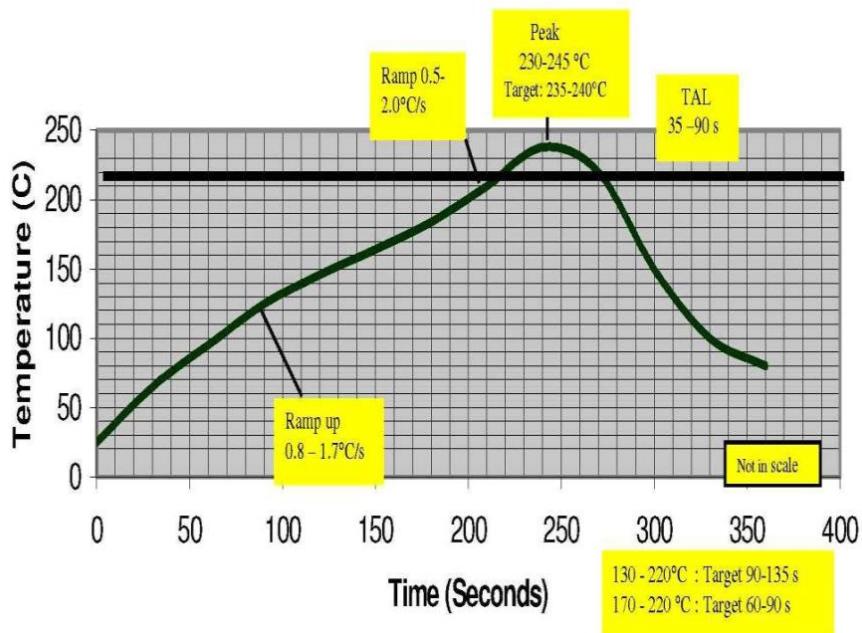


Figure 52 Reflow Diagram

Note:

The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it. The recommended belt speed is 50-60 Cm/Min. A finished module can go through two more reflow processes.

7.2 Baking Instructions

The packages are moisture sensitive (MSL3 grade) and devices must be handled appropriately. After the devices are removed from their vacuum-sealed packs, they should be taken through reflow for board assembly within 168 hours at room conditions or stored at under 10% relative humidity. If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125°C.

8 RS14100 CA1/CC1 module Package Description

8.1 Modules with Package Codes CA1, CC1

8.1.1 Mechanical Characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	15 x 15.7 x 2.2	mm
Tolerance	± 0.2	mm

Table 89 Mechanical Characteristics - CA1, CC1

8.2 Dimensions

Parameter	Value (L X W X H)	Units
Module Dimensions	15 x 15.7 x 2.2	mm
Tolerance	± 0.2	mm

Table 90 Module Dimensions

8.2.1 Packing Information of Modules with Package Codes CA1/CC1

The modules are packaged and shipped in Trays.

Each tray for the CA1 and CC1 packages can accommodate 112 modules. The mechanical details of the tray for the CA1 and CC1 package are given in the figure below.

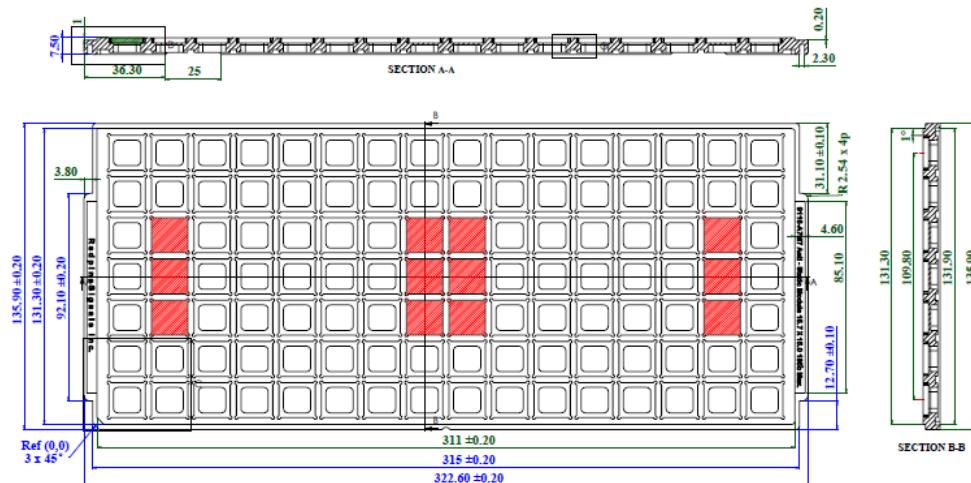


Figure 53 Packing Information of Modules with Package Codes CA1, CC1

8.3 Package Outline

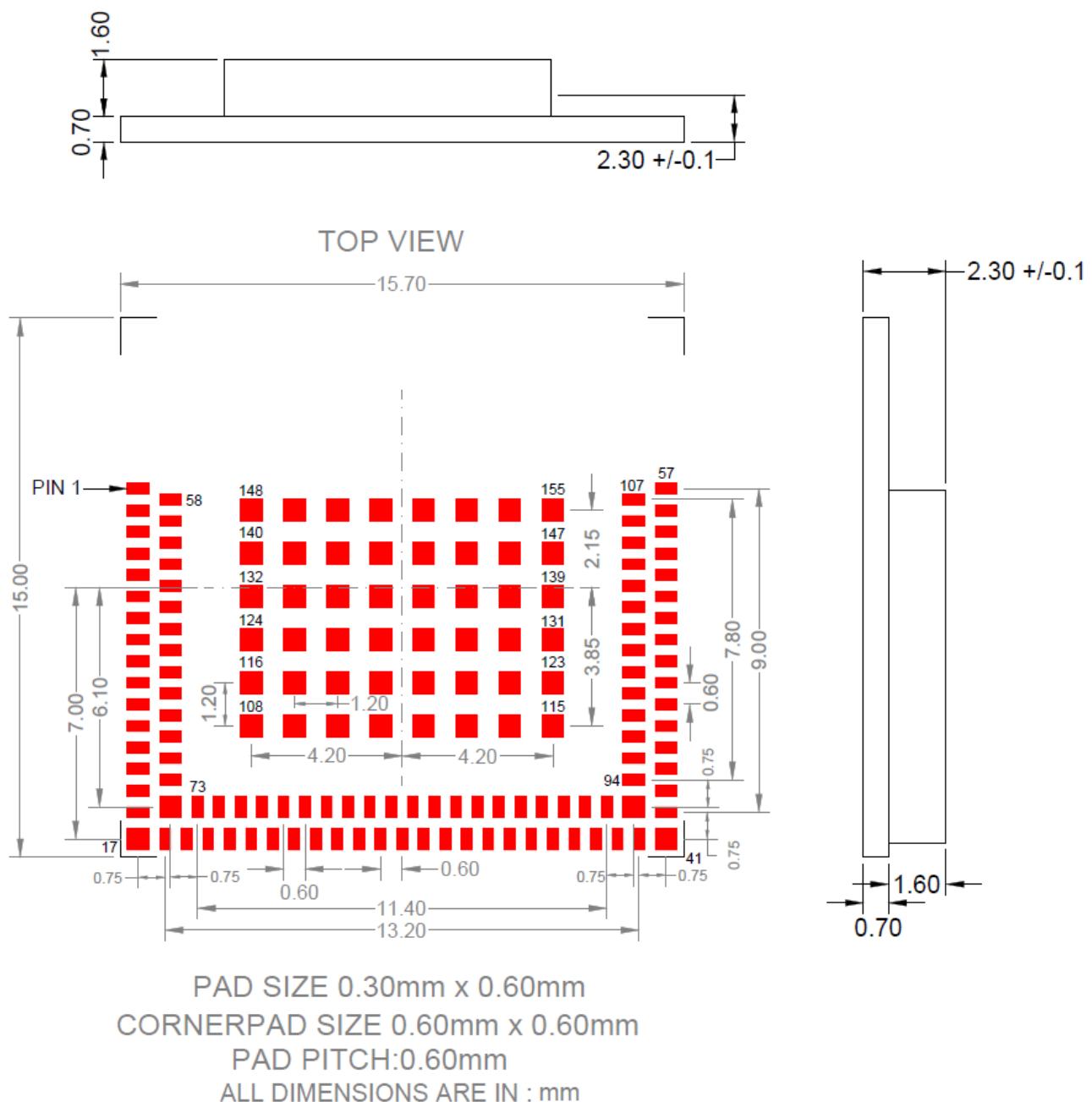
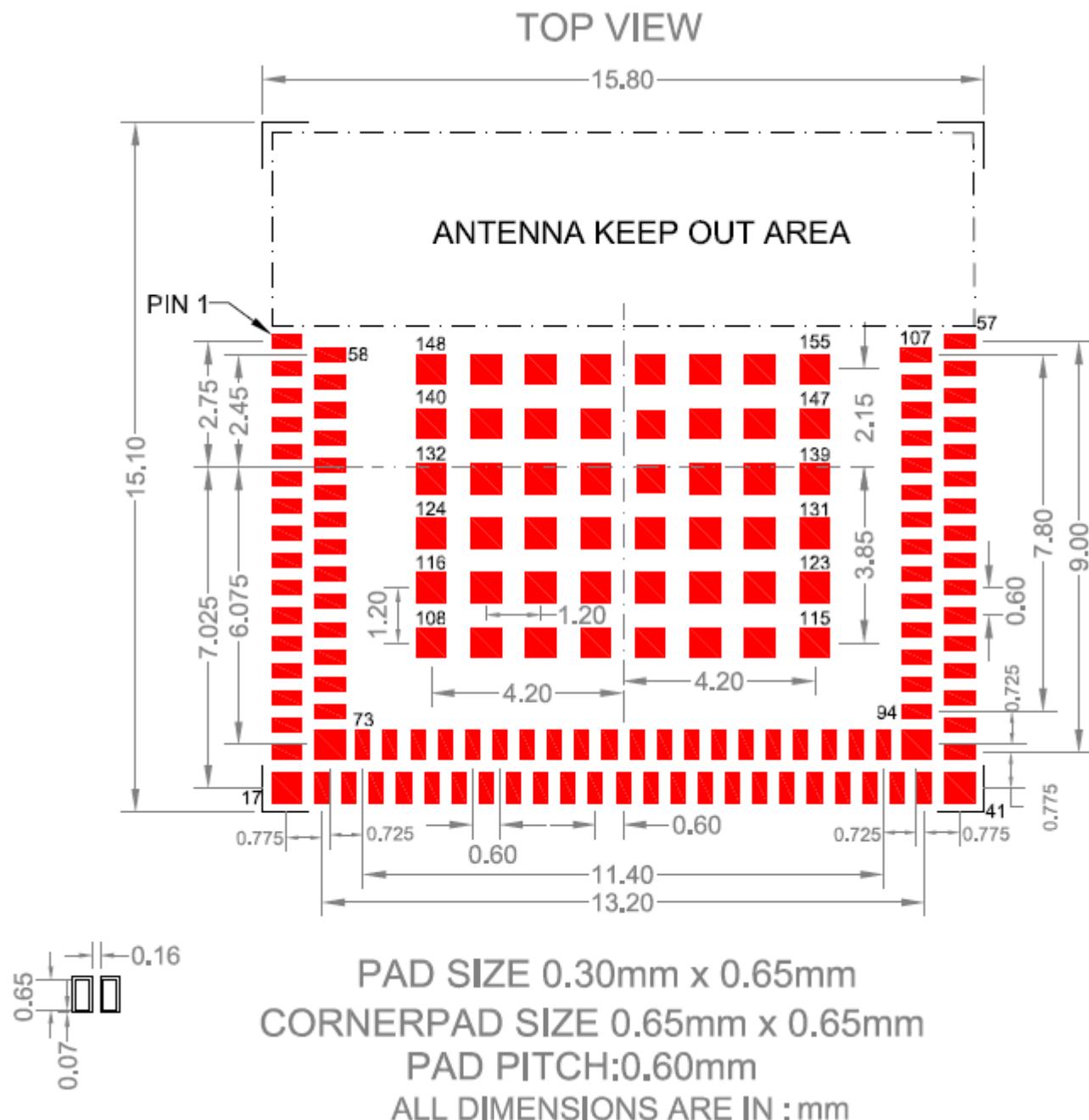


Figure 54 Package Outline

8.4 PCB Landing Pattern



9 RS14100 CA1/CC1 module Certification and Ordering Information

9.1 Certification Information

This section will outline the regulatory certification information for the RS14100 modules for the countries listed below. This information will be updated when available.

1. United States
2. Canada
3. Europe
4. Japan
5. Other Regulatory Jurisdictions

The RS14100 Single band CA1 and Dual band CC1 modules from Redpine Signals have undergone modular certification for FCC, IC and CE/ETSI. Note that any changes to the module's configuration including (but not limited to) the programming values of the RF Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh. The table below lists the details of the regulatory certifications. The certification for geographies not listed in the table is in progress.

- RF Testing Software is provided for any end product certification requirements.

9.1.1 Federal Communication Commission Statement

Any changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

Note

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

9.1.1.1 RF exposure statements

1. This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
2. This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body or nearby persons.

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XF6-M7DB6" or "Contains FCC ID: XF6-M7DB6" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

9.1.1.2 Labeling and User Information

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause undesired operation.

9.1.2 Industry Canada / ISED Statement

This product meets the applicable Innovation, Science and Economic Development Canada technical specifications.

Ce produit répond aux spécifications techniques applicables à l'Innovation, Science et Développement économique Canada.

9.1.2.1 Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes :

1. l'appareil ne doit pas produire de brouillage;
2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

9.1.2.2 Labeling and User Information

Innovation, Science and Economic Development Canada ICES003 Compliance Label: CAN ICES-3 (B)/NMB-3(B)

The M7DB6 module has been labeled with its own IC ID number (8407A-M7DB6) and if the IC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must also display a label referring to the enclosed module. This exterior label can use following wording: Contains Transmitter Module IC ID: 8407A-M7DB6 or Contains IC ID: 8407A-M7DB6 User manuals for license-exempt radio apparatus shall contain the above mentioned statement or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both

Warning:

1. The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
2. For devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;
3. For devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate; and

The high-power radars are allocated as primary users (i.e. priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

DFS (Dynamic Frequency Selection) products that operate in the bands 5250- 5350 MHz, 5470-5600MHz, and 5650-5725MHz.

This device is not capable of transmitting in the band 5600-5650 MHz in Canada.

Avertissement:

1. Le dispositif fonctionnant dans la bande 5150-5250 MHz est réservé uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;
2. Le gain maximal d'antenne permis pour les dispositifs avec antenne(s) amovible(s) utilisant les bandes 5250-5350 MHz et 5470-5725 MHz doit se conformer à la limitation P.I.R.E.;
3. Le gain maximal d'antenne permis pour les dispositifs avec antenne(s) amovible(s) utilisant la bande 5725-5850 MHz doit se conformer à la limitation P.I.R.E spécifiée pour l'exploitation point à point et non point à point, selon le cas.

En outre, les utilisateurs devraient aussi être avisés que les utilisateurs de radars de haute puissance sont désignés utilisateurs principaux (c.-à-d., qu'ils ont la priorité) pour les bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer du brouillage et/ou des dommages aux dispositifs LAN-EL.

Les produits utilisant la technique d'atténuation DFS (sélection dynamique des fréquences) sur les bandes 5250- 5350 MHz, 5470-5600MHz et 5650-5725MHz.

Cet appareil ne peut pas émettre dans la bande 5600-5650 MHz au Canada.

9.1.3 CE

M7DB6 is in conformity with the essential requirements and other relevant requirements of the R&TTE Directive (1999/5/EC). The product is conformity with the following standards and/or normative documents.

- EMC (immunity only) EN 301 489-17 V.2.2.1 in accordance with EN 301 489-1 V1.9.2
- Radiated emissions EN 300 328 V1.9.1
- Safety standards: EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2:2013

9.1.4 Qualified Antenna Types for M7DB6

This device has been designed to operate with the antennas listed below. Antennas not included in this list or having a gain greater than listed gains in each region are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Antenna Model	Antenna Type	Gain	Qualified Region
RSIA7	PCB Trace Antenna	0.712 dBi (2.4GHz)	FCC/IC, CE
		1.25 dBi (5GHz)	
GW.71.5153	Dipole Antenna	3.3 dBi (Straight)	FCC/IC
		3.8 dBi (Bent)	

Table 91 Qualified Antenna List

Any antenna that is of the same type and of equal or less directional gain can be used without a need for retesting. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication. Using an antenna of a different type or gain more than certified gain will require additional testing.

9.1.5 Module Marking Information

The figure and table below illustrates the marking on the Single band CA1, Dual band CC1 modules and explains the marking on the module



Marking	Description	
Model	M7DB6	Model Number for Single band and Dual-band modules
Firmware	RSXXXXX-CXX	Software/Firmware supported – refer to the Part Ordering Section for more details.
FCC	XF6-M7DB6	FCC Grant ID for Dual-band modules.
IC	8407A-M7DB6	IC Grant ID for Dual-band modules.

Marking		Description
Lot Code Information	XXX-WWYY	XXX – Internal usage WW – Week of manufacture YY – Year of manufacture
Compliance Marks		FCC Compliance Mark
		CE Compliance Mark

Table 92 Dual Band Module Marking Information

9.2 Module Package

Package Code	Package Type, Pins	Dimensions (mm)	Frequency Band	Integrated Antenna
CA1	LGA,155	15 x 15.7 x 2.2	Single Band (2.4 GHz)	Yes
CC1	LGA,155	15 x 15.7 x 2.2	Dual Band (2.4 GHz/5 GHz)	Yes

Table 93 CA1 and CC1 Module Packages

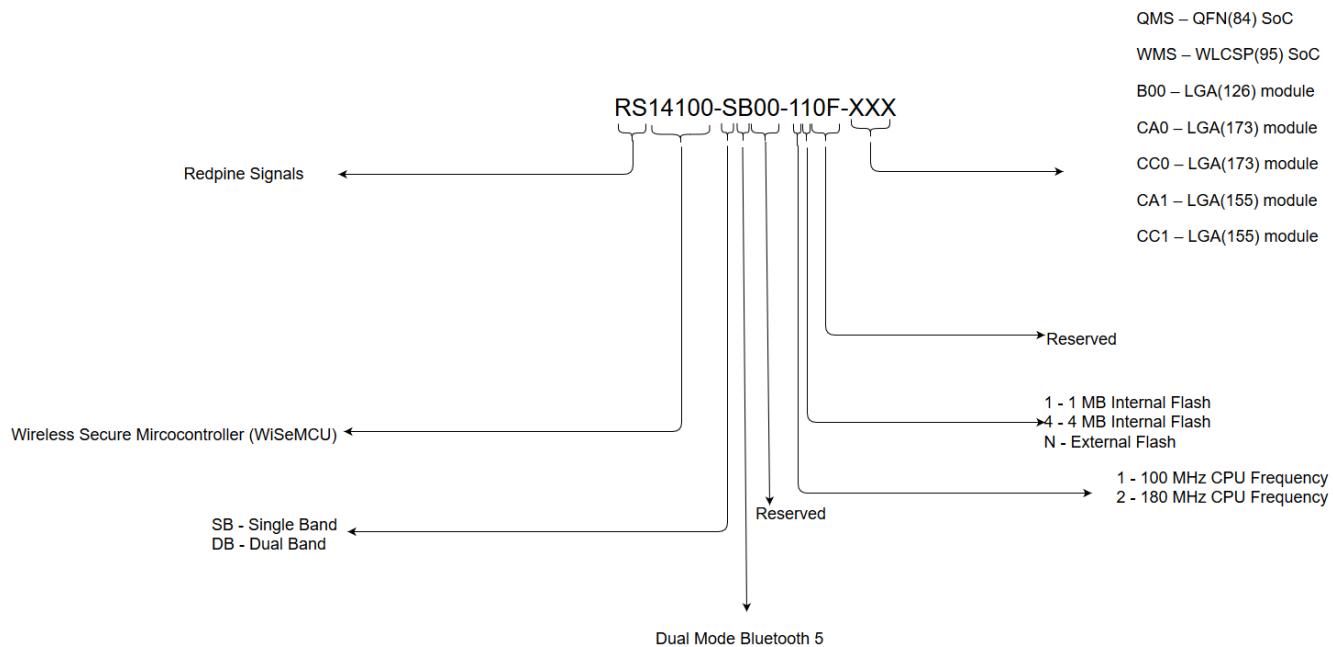
9.3 Ordering Information

Part Number	Wireless	CPU Freq	Flash+RAM
RS14100-SB00-140F-CA1	SBW+BT5	100 MHz	4 MB+208 KB
RS14100-SB00-240F-CA1	SBW+BT5	180 MHz	4 MB+208 KB
RS14100-DB00-140F-CC1	DBW+BT5	100 MHz	4 MB+208 KB
RS14100-DB00-240F-CC1	DBW+BT5	180 MHz	4 MB+208 KB

Table 94 Part Ordering Options

Note: SBW: Single Band Wi-Fi (2.4 GHz); DBW: Dual Band Wi-Fi (2.4/5 GHz)

9.3.1 Device Nomenclature

**Figure 55 RS14100 Device Nomenclature**

10 RS14100 CA1/CC1 module Documentation and Support

Category	Name
Product Brief	RS14100 Product Brief
Datasheet	RS14100 CA1/CC1 Datasheet
EVK Resources	RS14100 EVK Demo Guide RS14100 EVK User Guide
Hardware Resources	RS14100 CA1/CC1 Package dimensions and 3D models RS14100 CA1 Symbols RS14100 CC1 Symbols
Software Resources	WiSeMCU WLAN Software Reference Manual WiSeMCU BT Classic Software Reference Manual WiSeMCU BLE Software Reference Manual Redpine Hardware Reference Manual RS14100 Wireless SAPI Examples RS14100 Wireless SAPI Manual RS14100 TCP/IP Feature Selection Tool Redpine MCU SAPI Manual
Certifications	CE ETSI RED Certificate FCC Certificate IC Certificate RoHS Certificate
Software Tools	SmartStudio IDE and SDK
Support	Redpine Forum Technical Support Sales Support

11 RS14100 CA1/CC1 module Revision History

Revision No.	Version No.	Date	Changes
1	1.0	May, 2019	Initial version
2	1.0.1	May, 2019	Updated 32 Khz external oscillator specifications
3	1.0.2	May, 2019	<ul style="list-style-type: none"> • Removed AVDD_1P3 from the Reference schematics, Pinout Diagram, Moved the pin from Power section to NC list. • Removed 32KHz XTAL Pins and used UULP GPIO for feeding in the External Clock. Updated the below sections for the same <ul style="list-style-type: none"> ○ Pinout Description. ○ System Block Diagram ○ Detailed Description ○ Specifications ○ Reference Schematics

Table 95 Revision History

Disclaimer

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