AR5416 802.11n MAC/BB Processor for 2.4/5 GHz WLANs

General Description

The Atheros AR5416 MAC/BB processor is part of the AR5008 chip set solutions for IEEE 802.11n-confirmed draft compliant ready wireless local area networks (WLAN) applications.

The AR5416 integrates a multi-protocol media access control (MAC), a baseband processor, a PCI/CardBus host interface, and an analog-to-digital and digital-to-analog (ADC/DAC) converter.

Together with the AR2133 for 2.4 GHz, or AR5133 for 2.4/5 GHz, multiple input, multiple output (MIMO) radio chip, the AR5008 chip sets support up to a 3 Tx chain, 3 Rx chain, and 2 stream MIMO configuration. The AR5008 chipsets enable WLAN access point (AP) and client solutions that demand robust link quality with maximum throughput and range.

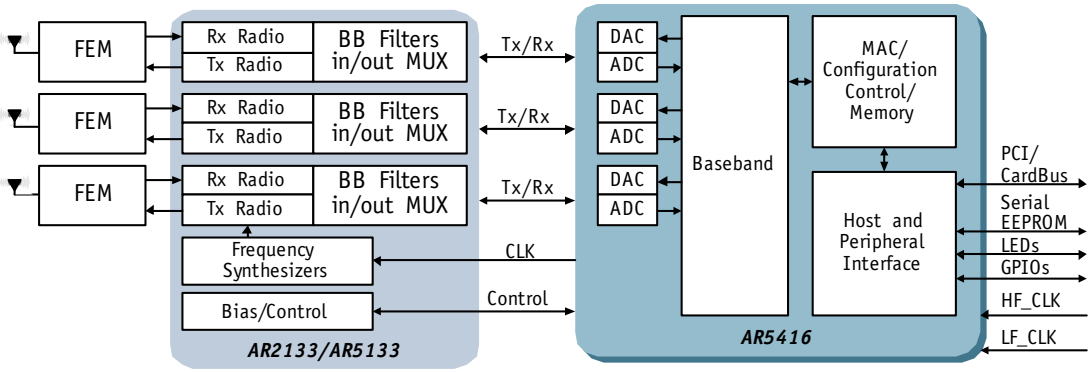
The AR5416 implements half-duplex OFDM, CCK, and DSSS baseband processing, supporting 130 Mbps and 300 Mbps for 20 MHz and 40 MHz channel operations respectively, and all IEEE 802.11a/b/g data rates. Additional features include signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. The AR5416 MAC supports the 802.11 wireless MAC protocol, 802.11i security, receive and transmit filtering, error recovery, and quality of service (QoS).

The AR5416 supports frame data transfer to and from the host using a PCI/CardBus interface, which also provides interrupt generation and reporting, power save, and status reporting. Other external interfaces include serial EEPROM, GPIOs, and LEDs.

Features

- All-CMOS MIMO solution interoperable with legacy IEEE 802.11a/b/g compatible WLANs
- 3x3 MIMO technology improves effective throughput and range over existing 802.11a/b/g products
- Supports spatial multiplexing, cyclic-delay diversity (CDD), and maximal ratio combining (MRC)
- 2.4/5 GHz WLAN MAC/BB processing engine
- BPSK, QPSK, 16 QAM, 64 QAM, DBPSK, DQPSK, and CCK modulation schemes
- Data rates of up to 130 Mbps for 20 MHz channels and 300 Mbps for 40 MHz channels
- Wireless multimedia enhancements quality of service support (QoS)
- 802.11e-compatible bursting
- Support for the IEEE 802.11e, h, i, and j standards
- WEP, TKIP, and AES hardware encryption
- 32-bit and 0–33-MHz PCI 2.3 interface
- PC Card 7.1 (CardBus) interface
- No external linear regulator needed, but can support an external switching regulator
- 32 KHz low frequency crystal for low power sleep mode
- Reduced (short) guard interval
- Frame aggregation with A-MPDU
- Block ACK
- Wake-on-Wireless feature supported
- Support for Bluetooth coexistence
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- 304-pin, 14 mm x 14 mm BGA package

System Block Diagram



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1. Pin Descriptions

This section contains both a package pinout (see Table 1-1 through Table 1-4) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Table 1-1. **AR5416 Pin Assignments (1–10)**

	1	2	3	4	5	6	7	8	9	10
A	RFRESET_L	RFLOAD	RFDATAOUT5	RFDATAOUT3	RFDATAOUT1	RFSHIFT	AGND	TX0_RX1_IN	TX0_RX1_QN	TX1_RX2_IN
B	SWCOM3	GND	RFDATAIN	RFDATAOUT4	RFDATAOUT2	RFDATAOUT0	AGND	TX0_RX1_IP	TX0_RX1_QP	TX1_RX2_IP
C	SWCOM1	SWCOM2	GND	DVDD18	DVDD18	AGND	AVDD18	AVDD18	AVDD18	AGND
D	SW1_1	SWCOM0	DVDD18							
E	SW1_0	SW2_1	DVDD18							
F	SW0_0	SW0_1	SW2_0			GND	GND	GND	GND	GND
G	PCI_AD31	PCI_CLKRUN_L	DVDD33			GND	GND	GND	GND	GND
H	PCI_AD29	PCI_AD30	DVDD33			GND	GND	GND	GND	GND
J	PCI_AD27	PCI_AD28	DVDD18			GND	GND	GND	GND	GND
K	PCI_AD25	PCI_AD26	NC			GND	GND	GND	GND	GND
L	PCI_CBE3_L	PCI_AD24	PCI_PME_L			GND	GND	GND	GND	GND
M	PCI_REQ_L	PCI_AD23	DVDD18			GND	GND	GND	GND	GND
N	PCI_SERR_L	PCI_AD22	DVDD33			GND	GND	GND	GND	GND
P	PCI_RST_L	PCI_AD21	DVDD33			GND	GND	GND	GND	GND
R	PCI_MODE	PCI_IDSEL	POWER_RST_L			GND	GND	GND	GND	GND
T	PCI_AD20	PCI_AD19	DVDD18							
U	PCI_AD18	PCI_AD17	DVDD18							
V	PCI_CBE2_L	PCI_FRAME_L	GND	DVDD18	DVDD18	PCI_AD16	DVDD33	DVDD33	DVDD18	PCI_AD8
W	PCI_IRDY_L	GND	PCI_DEVSEL_L	PCI_STOP_L	PCI_PERR_L	PCI_CBE1_L	PCI_AD14	PCI_AD12	PCI_AD10	PCI_CBE0_L
Y	PCI_TRDY_L	PCI_CLK	PCI_INT_L	PCI_GNT_L	PCI_PAR	PCI_AD15	PCI_AD13	PCI_AD11	PCI_AD9	PCI_AD7

Table 1-2. **AR5416 Pin Assignments (11–20)**

	11	12	13	14	15	16	17	18	19	20
A	TX1_RX2_QN	TX2_RX0_IN	TX2_RX0_QN	PDET_0	XPA5BIAS_0	XPA5BIAS_1	XPA2BIAS_2	VREFSEL_0	PWD_REGS	COMP_ANA
B	TX1_RX2_QP	TX2_RX0_IP	TX2_RX0_QP	PDET_1	XPA2BIAS_0	XPA2BIAS_1	BIASREF	VREFSEL_1	AGND	VREG_ANA
C	AGND	AVDD18	AVDD33	PDET_2	AGND	XPA5BIAS_2	AVDD33	AGND	COMP_DIG	VREG_DIG
D								AVDD18	AGND	AGND
E								AVDD33	CLKN	CLKP
F	GND	GND	GND	GND	GND			AGND	XTALI	XTALO
G	GND	GND	GND	GND	GND			DVDD33	LFXTALI	LFXTALO
H	GND	GND	GND	GND	GND			DVDD33	TDI	TDO
J	GND	GND	GND	GND	GND			DVDD18	TCK	TMS
K	GND	GND	GND	GND	GND			TRST_L	EPRM_SDA	EPRM_SCK
L	GND	GND	GND	GND	GND			GND	GND	GPIO13
M	GND	GND	GND	GND	GND			DVDD18	GPIO12	GPIO11
N	GND	GND	GND	GND	GND			DVDD33	GPIO10	GPIO9
P	GND	GND	GND	GND	GND			DVDD33	GPIO8	GPIO7
R	GND	GND	GND	GND	GND			GPIO6	GPIO5	GPIO4
T								DVDD18	GPIO3	GPIO2
U								DVDD18	GPIO1	GPIO0
V	PCI_AD6	DVDD18	DVDD33	DVDD33	GND	DVDD18	DVDD18	GND	GND	DVDD33
W	PCI_AD4	PCI_AD2	PCI_AD0	GND	GND	GND	DVDD18	DVDD18	GND	DVDD33
Y	PCI_AD5	PCI_AD3	PCI_AD1	GND	GND	GND	GND	NC	NC	GND

Table 1-3 and Table 1-4 provide the signal-to-pin relationship information for the AR5416.

Table 1-3. **Signal to Pin Relationships and Descriptions**

Signal Name	Pin	Direction	Description
PCI			
PCI_CLK	Y2	I	PCI clock, input for target, output for master
PCI_AD31	G1	I/O	Multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contains a physical byte address. During subsequent clocks, it contains data.
PCI_AD30	H2	I/O	
PCI_AD29	H1	I/O	
PCI_AD28	J2	I/O	
PCI_AD27	J1	I/O	
PCI_AD26	K2	I/O	
PCI_AD25	K1	I/O	
PCI_AD24	L2	I/O	
PCI_AD23	M2	I/O	
PCI_AD22	N2	I/O	
PCI_AD21	P2	I/O	
PCI_AD20	T1	I/O	
PCI_AD19	T2	I/O	
PCI_AD18	U1	I/O	
PCI_AD17	U2	I/O	
PCI_AD16	V6	I/O	
PCI_AD15	Y6	I/O	
PCI_AD14	W7	I/O	
PCI_AD13	Y7	I/O	
PCI_AD12	W8	I/O	
PCI_AD11	Y8	I/O	
PCI_AD10	W9	I/O	
PCI_AD9	Y9	I/O	
PCI_AD8	V10	I/O	
PCI_AD7	Y10	I/O	
PCI_AD6	V11	I/O	
PCI_AD5	Y11	I/O	
PCI_AD4	W11	I/O	
PCI_AD3	Y12	I/O	
PCI_AD2	W12	I/O	
PCI_AD1	Y13	I/O	
PCI_AD0	W13	I/O	

Table 1-3. **Signal to Pin Relationships and Descriptions (continued)**

Signal Name	Pin	Direction	Description
PCI_CBE3_L	L1	I/O	PCI multiplexed bus command and byte enables. During a transaction address phase, these signals define the bus command. During the data phase, they are used as byte enables.
PCI_CBE2_L	V1	I/O	
PCI_CBE1_L	W6	I/O	
PCI_CBE0_L	W10	I/O	
PCI_CLKRUN_L	G2	O	Provides for starting and stopping the PCI clock
PCI_DEVSEL_L	W3	I/O	PCI device select
PCI_FRAME_L	V2	I/O	PCI frame
PCI_GNT_L	Y4	I	PCI grant
PCI_IDSEL	R2	I	PCI ID select
PCI_INT_L	Y3	O	PCI interrupt
PCI_IRDY_L	W1	I/O	PCI initiator ready
PCI_PAR	Y5	I/O	PCI parity
PCI_PERR_L	W5	I/O	PCI parity error
PCI_PME_L	L3	O	PCI power management
PCI_REQ_L	M1	O	PCI request
PCI_RST_L	P1	I	PCI reset
PCI_SERR_L	N1	I/O	PCI system error
PCI_STOP_L	W4	I/O	PCI stop
PCI_TRDY_L	Y1	I/O	PCI target ready
General			
POWER_RST_L	R3	I	Reset entire chip
XTALI	F19	I	40 MHz crystal
XTALO	F20	O	
LFXTALI	G19	I	32 KHz clock for low power mode
LFXTALO	G20	O	

Table 1-3. **Signal to Pin Relationships and Descriptions (continued)**

Signal Name	Pin	Direction	Description
GPIO			
GPIO_0	U20	I/O	General purpose GPIO pins
GPIO_1	U19	I/O	
GPIO_2	T20	I/O	
GPIO_3	T19	I/O	
GPIO_4	R20	I/O	
GPIO_5	R19	I/O	
GPIO_6	R18	I/O	
GPIO_7	P20	I/O	
GPIO_8	P19	I/O	
GPIO_9	N20	I/O	
GPIO_10	N19	I/O	
GPIO_11	M20	I/O	
GPIO_12	M19	I/O	
GPIO_13	L20	I/O	
External Switch Control			
SW0_0	F1	O	Switch control for chain 0
SW0_1	F2	O	
SW1_0	E1	O	Switch control for chain 1
SW1_1	D1	O	
SW2_0	F3	O	Switch control for chain 2
SW2_1	E2	O	
SWCOM0	D2	O	Common switch control
SWCOM1	C1	O	
SWCOM2	C2	O	
SWCOM3	B1	O	
JTAG Interface			
TCK	J19	I	JTAG test clock
TDI	H19	I	JTAG data input
TDO	H20	O	JTAG data output
TMS	J20	I	JTAG test mode
TRST_L	K18	I	JTAG test reset
Mode Selection			
PCI_MODE	R1	I	Selects between PCI and CardBus interface ■ 0 = CardBus ■ 1 = PCI

Table 1-3. **Signal to Pin Relationships and Descriptions (continued)**

Signal Name	Pin	Direction	Description
Analog Interface			
BIASREF	B17	IA	BIASREF voltage is 620 mV; connects a 6.19 KΩ ± 1% resistor to ground
CLKN	E19	OA	Reference clock to the radio chip
CLKP	E20	OA	
PWD_REGS	A19	I	Selects external analog and digital voltage regulators. Connects to ground through a 0 Ω resistor to enable internal regulators. When external regulators are used, PWD_REGS, VREFSEL_0, VFRESEL_1, VREG_ANA, and VREG_DIG should be open. COMP_ANA and COMP_DIG connect to AVDD33 and DVDD33, respectively, or they can be left open.
VREFSEL_0	A18	I	Inputs for controlling internal linear regulators. Connects both pins to ground through 0 Ω resistor for 1.8 V. When external regulators are used, these pins should be open.
VREFSEL_1	B18	I	
COMP_ANA	A20	IA	Compensation for analog LDO, connects to external RC compensation network. See "Low Dropout Regulator" on page 139 for additional information. When an external regulator is used, this pin should be tied to AVDD33, or left open.
COMP_DIG	C19	IA	Compensation for digital LDO, connects to external RC compensation network. See "Low Dropout Regulator" on page 139 for additional information. When an external regulator is used, this pin should be tied to DVDD33, or left open.
VREG_ANA	B20	OA	Controls external PNP device to drive analog LDO for the internal analog regulator. When an external regulator is used, this pin should be open.
VREG_DIG	C20	OA	Controls external PNP device to drive digital LDO for the internal digital regulator. When an external regulator is used, this pin should be open.
PDET0	A14	IA	Power detector
PDET1	B14	IA	
PDET2	C14	IA	
TX0_RX1_IN	A8	IA/OA	Differential control for transmit chain 0 and receive chain 1
TX0_RX1_IP	B8	IA/OA	
TX0_RX1_QN	A9	IA/OA	
TX0_RX1_QP	B9	IA/OA	
TX1_RX2_IN	A10	IA/OA	Differential control for transmit chain 1and receive chain 2
TX1_RX2_IP	B10	IA/OA	
TX1_RX2_QN	A11	IA/OA	
TX1_RX2_QP	B11	IA/OA	

Table 1-3. **Signal to Pin Relationships and Descriptions (continued)**

Signal Name	Pin	Direction	Description
TX2_RX0_IN	A12	IA/OA	Differential control for transmit chain 2 and receive chain 0
TX2_RX0_IP	B12	IA/OA	
TX2_RX0_QN	A13	IA/OA	
TX2_RX0_QP	B13	IA/OA	
XPA2BIAS_0	B15	OA	External bias for 2.4 GHz
XPA2BIAS_1	B16	OA	
XPA2BIAS_2	A17	OA	
XPA5BIAS_0	A15	OA	External bias for 5 GHz
XPA5BIAS_1	A16	OA	
XPA5BIAS_2	C16	OA	
Analog Control			
RFDATAOUT0	B6	O	Data out to radio chip
RFDATAOUT1	A5	O	
RFDATAOUT2	B5	O	
RFDATAOUT3	A4	O	
RFDATAOUT4	B4	O	
RFDATAOUT5	A3	O	
RFDATAIN	B3	I	Data in from radio chip
RFSHIFT	A6	O	Controls to the radio chip
RFLOAD	A2	O	
RFRESET_L	A1	O	Reset to the radio chip
Serial EEPROM			
EPRM_SDA	K19	I/O	Serial EEPROM data
EPRM_SCK	K20	O	Serial EERPOM clock

Table 1-4. **Signal-to-Pin Relationships**

Signal Name	Pin	Description
Power		
AGND	A7, B7, B19, C6, C10, C11, C15, C18, D19, D20, F18	Analog ground
AVDD18	C7, C8, C9, C12, D18	Analog 1.8V supply
AVDD33	C13, C17, E18	Analog 3.3V supply
GND	B2, C3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L18, L19, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, V3, V15, V18, V19, W2, W14, W15, W16, W19, Y14, Y15, Y16, Y17, Y20	Digital ground
DVDD18	C4, C5, D3, E3, J3, J18, M3, M18, T3, T18 U3, U18, V4, V5, V9, V12, V16, V17, W17, W18	Digital 1.8V
DVDD33	G3, G18, H3, H18, N3, N18, P3, P18, V7, V8, V13, V14, V20, W20	Digital 3.3V
No Connection		
NC	K3, Y18, Y19	No connection, must be open

2. Functional Description

2.1 Overview

The AR5416 consists of the host interface, MAC, and digital PHY with baseband processor. IEEE 802.11 MAC functionality is partitioned between the host and the AR5416. The MAC provides the data service while the host software, with the aid of the MAC, controls transmit (Tx) and receive (Rx) queue processing.

The physical layer (PHY) is partitioned between the AR5416 and the AR5133/AR2133. See the *AR5133/AR2133 802.11n MIMO Radio for 2.4/5 GHz WLANs* data sheets for more information. The digital PHY implements the baseband digital processing functions. The radio frequency (RF) and baseband analog processing are provided by the AR5133/AR2133.

The ADC/DAC, interface to the AR5133/AR2133, EEPROM interface, GPIO, LED control complete AR5416 functionality. Figure 2-1 shows the system architecture.

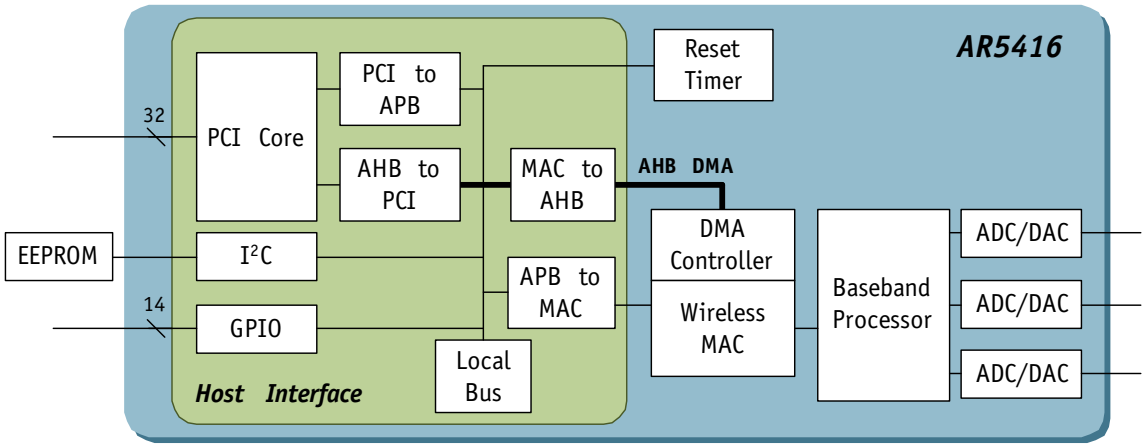


Figure 2-1. **AR5416 System Architecture**

2.2 Address MAP

Internal registers of the functional blocks and the peripheral interface are accessible by the host using the PCI/CardBus interface. The locations of these registers are defined as offset addresses. The host memory is mapped to the AR5416 address space by specifying the base address location in the PCI base address register. The combination of the host address base and the offset address allows access to a particular AR5416 internal register. Table 2-1 lists the offset addresses for the AR5416 internal registers and peripheral interface.

Table 2-1. **Offset Addresses**

Offset Location	Usage	Description
0x0000–0x07FC	MAC DMA general	DMA access
0x0800–0x0FFC	MAC DMA QCU registers	Control and status register for QCU
0x1000–0x1FFC	DCU registers	Control and status register for DCU
0x2000–0x3FFC	EEPROM access register	Memory location of EEPROM are mapped to this address range and allow access to EEPROM
0x4000–0x4FFC	Host interface	Control and status register for host interface
0x6000–0x6FFC	PCI configuration	Control and status register format for host PCI
0x8000–0x98FC	PCU registers	Control and status register for PCU

2.2.1 Serial EEPROM Interface

The AR5416 provides a serial interface to access an external EEPROM. The EEPROM interface modifies configuration space registers and configuration- and vendor-specific information.

The off-chip EEPROM can be:

- A 32-Kb device, organized as 2,048 entries of 16 bits each (2,048x16)
- An 64-Kb device, organized as 4,096 entries of 16 bits each (4,096x16)

The hardware automatically detects EEPROM size. The EEPROM addressing is 16 bits wide, with each 16-bit EEPROM mapped into the AR5416's register space. Each 32-bit aligned address corresponds to a unique EEPROM location. Because the host interface supports 32-bit register accesses and ignores the two least significant address bits, the address offset provided by the host interface corresponds to four times the EEPROM location.

At reset, some PCI/CardBus configuration registers load from the EEPROM while others are programmed by the host or initialized by AR5416 hardware. To ensure that the EEPROM contents are valid, a 16-bit word at address offset 0x2000 is checked. If the values do not match 0xA55A, the EEPROM contents are ignored and the default values loaded. More information is provided in "Host PCI Configuration Space Registers" on page 85.

2.2.1 EEPROM Auto-Sizing Mechanism

The first procedure after reset is to read the offset address 0x2000 to check for the content 0xA55A. The EEPROM physical presence, programmed state, and size are determined automatically. If the offset address 0x2000 contents do not match the 0xA55A value for any supported EEPROM sizes, the AR5416 assumes the EEPROM is not present on the PCB, or is present but not programmed. In either case, the logic uses the default values as described in "Serial EEPROM Interface".

2.2.2 EEPROM Read/Write Protection Mechanism

The EEPROM contains a 16-bit word protect mask value at address location 0x2010H that prevents software from accessing certain regions. The mask is 16 bits wide and contains eight sub-masks that are 2 bits wide.

The sub-mask can have four values that determine the access types permitted to the associated protection region:

- 00: read and write access allowed
- 01: write-only access allowed
- 10: read-only access allowed
- 11: no access allowed

2.3 Reset

The POWER_RST_L pin controls the AR5416 chip reset. The AR5416 host interface receives two reset signals as below:

- POWER_RST_L pin
  Controls the AR5416 power reset
- PCI_RST_L
  Controls the PCI core reset

In addition, the RTC_RESET Register provide software control of warm reset for the MAC/baseband and PCU blocks. See the register "RTC Reset and Force Sleep and Force Wakeup (RTC_RESET)" on page 95.

2.4 GPIO

The AR5416 provides fourteen configurable bi-directional general purpose I/O ports. Each GPIO can be independently configured as input or output using the GPIO control register. Information presented at the GPIO inputs and outputs can be read from the GPIO input and output register (H_GPIO_IN_OUT) (see the GPIO registers on page 79 through page 83).

2.5 LED

The AR5416 provides GPIO pins to configure for LED output. Control for LED output is provided by the "MAC LED Control (MAC_LED)" on page 98 register.

2.6 PCI/CardBus Host Interface

This section provides a summary of the AR5416 PCI/CardBus interface. This interface is compatible with PCI 2.3 and PC Card 7.1 standards and functions as the host interface for the AR5416, providing data and command transfer between the host software, the MAC, and the configuration registers. For details, refer to the PCI 2.3 and CardBus 7.1 standards specifications.

2.6.1 PCI/ CardBus Registers

At system boot, the host uses the PCI/CardBus configuration registers to detect the type of device present and to perform low level PCI/ CardBus configuration (e.g., assigning a base address to the device).

An external serial EEPROM provides device configuration information. At reset, some PCI/ CardBus configuration registers load from the off-chip serial EEPROM, whereas the host must program the others. Configuration, control, and status registers for the various functional blocks of the AR5416 map to the memory space of the PCI/CardBus interface and thus can be accessed by the host. PCI configuration register details are provided in "Host PCI Configuration Space Registers" on page 85.

2.7 Signal Description

The AR5416 PCI/CardBus interface pins are described in "Pin Descriptions" on page 9. Table 2-2 shows the interface pins grouped by functional type.

Table 2-2. **Types of PCI Interface Signals**

Type	Pin
Address and Data	PCI_AD[31:0]
	PCI_CBE[3:0]_L
	PCI_PAR
System	PCI_RST_L
	PCI_CLK
	PCI_CLKRUN_L
Interface Control	PCI_IDSEL
	PCI_DEVSEL_L
	PCI_FRAME_L
	PCI_IRDY_L
	PCI_STOP_L
	PCI_TRDY_L
Arbitration	PCI_GNT_L
	PCI_REQ_L
Interrupt	PCI_INT_L
PCI Error Reporting	PCI_SERR_L
	PCI_PERR_L
Power Management	PCI_PME_L
Mode Selection	PCI_MODE

2.8 Host Interface Unit Interrupts

The AR5416 host interface unit supports:

- Asynchronous mode interrupt
- Synchronous mode interrupt
  Handles interrupts generated from GPIO, peripheral devices such as the EEPROM
  Synchronous mode interrupts are controlled and monitor by the registers "Synchronous Interrupt (H_INTR_SYNC_CAUS)", "Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)" and "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" on page 79.

Table 2-3 describes interrupt signals from various different blocks on the AR5416. The signal/bits are the same for asynchronous and synchronous interrupts (see Table 5-8 on page 75 for more details).

Table 2-3. **Interrupt Registers**

Bit	Name
0	RTC_IRQ
1	MAC_IRQ
2	EEPROM_ILLEGAL_ACCESS
3	APB_TIMEOUT
4	PCI_MODE_DBI_ACCESS
5	HOST1_FATAL
6	HOST1_PERR
7	TRCV_FIFO_PERR
12:8	RES
13	LOCAL_TIMEOUT
14	PM_ACCESS
15	MAC_AWAKE
16	MAC_ASLEEP
17	MAC_SLEEP_ACCESS
31:18	GPIO_INTR

Software can control and program both the "Synchronous Interrupt (H_INTR_SYNC_CAUS)" and the "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" registers. Because both registers contain similar bits, software should keep the synchronous and asynchronous interrupt enable registers mutually exclusive.

2.9 PCI Clkrun

The AR5416 supports the optional PCI clkrun capability as described in the PCI Mobile Design Guide, Version 1.1.

The pin PCI_CLKRUN_L is a PCI interface signal that controls the state of the PCI clock as supplied by the PCI host. Both the PCI host and the PCI device use the pin to signal that a PCI transaction is starting. This signal forces the host to maintain the PCI clock if it is running, or to start the PCI clock if is halted, allowing either the PCI host or PCI device to start the PCI clock prior to each PCI transaction and to stop the clock when the transaction is completed.

PCI_CLKRUN_L usage is transparent to AR5416 operation and can be enabled or disabled at any time. When enabled, impact on system performance is negligible but power savings can be significant.

Bit [0] in the register "PCI CLKRUN Registers (H_CLKRUN)" on page 83 controls the pin PCI_CLKRUN_L. When cleared, PCI_CLKRUN_L is forced to high-impedance state and the AR5416 forces the PCI clock to stop. When set, PCI_CLKRUN_L is set low and the AR5416 requests the PCI clock to run.

3. Medium Access Control (MAC)

The MAC consists of the following major functional blocks: 10 queue control units (QCUs), 10 distributed coordination function (DCF) control units (DCUs), a single DMA Rx unit (DRU), and a single protocol control unit (PCU). See Figure 3-1.

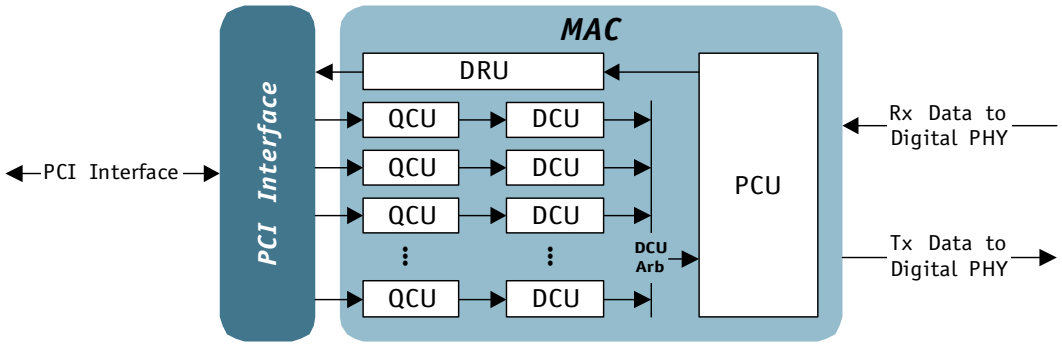


Figure 3-1. **MAC Block Diagram**

3.1 Overview

The MAC block supports full bus-mastering descriptor-based scatter/gather DMA. Frame transmission begins with the QCUs. QCUs manage the DMA of frame data from the host through the PCI/CardBus interface, and determine when a frame is available for transmission.

Each QCU targets exactly one DCU. Ready frames are passed from a QCU to its targeted DCU. The DCU manages the enhanced distributed coordination function (EDCF) channel access procedure on behalf of the QCUs associated with it.

Functionality of the MAC block includes:

- Tx frame data transfer from the host to the AR2133/AR5133 using the PCI bus
- Rx frame data transfer from the AR2133/AR5133 to host using the PCI bus
- Register access to all AR5416/AR2133/AR5133 registers
- Interrupt generation and reporting
- Sleep-mode sequencing
- Miscellaneous error and status reporting functions

Once the DCU gains access to the channel, it passes the frame to the PCU, which encrypts the frame and sends it to the baseband logic. The PCU handles both processing responses to the transmitted frame, and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bitstream from the digital PHY. The PCU decrypts the frame and passes it to the DRU, which manages Rx descriptors and writes the incoming frame data and status to the host memory through the PCI/CardBus interface.

3.2 Descriptor

The MAC is responsible for transferring frames between the host memory (accessed using the PCI/CardBus interface) and the AR5416. For all normal frame transmit/receive activity, the host provides a series of descriptors to the MAC, and the MAC then parses the descriptors and performs the required set of data transfers.

3.3 Descriptor Format

The transmit (Tx) descriptor format contains fourteen 32-bit words and the receive (Rx) descriptor ten 32-bit words (see Table 3-1).

The first two words of the descriptor point to the next descriptor in the linked list and to the data buffer associated with the descriptor. The next 12 (for Tx) or 2 (for Rx) words carry additional control information that affects how the MAC processes the frame and its data.

A descriptor is required to be aligned on a 32-bit boundary in host memory, although best performance is achieved if the descriptor is aligned on a cache-line boundary. The MAC uses the final two words to report status information back to the host. See the tables:

Table	Description
Table 3-2	Tx descriptor format for words 2–13
Table 3-3	Completion status of the Tx and Rx descriptors, words 14–23
Table 3-4	Rx descriptor format for words 2–3
Table 3-5	Rx descriptor format for words 4–12

Table 3-1. **DMA Descriptor Format**

Word	Bits	Name	Description
0	31:0	LinkPtr	Link pointer. Contains the address of the next descriptor to be used. Must be 32-bit aligned (bits 1:0 must be 0).
1	31:0	BufPtr	Data buffer pointer. Contains the starting address of the data buffer associated with this descriptor. A Tx data buffer can begin at any byte address. A Rx data buffer must be aligned on a 32-bit boundary in host memory, although best performance is achieved if the Rx data buffer is cache-line aligned. (Cache-line size varies from system to system)
2–13 (Tx) 2–3 (Rx)	31:0	Host-to-DMA engine control information	Additional control information is passed from host to DMA engine. The format of these words varies depending on whether the descriptor is being used to Tx a frame from host to PCU, or Rx a frame from PCU to host. (See Table 3-2 on page 24 and Table 3-4 on page 33 for details)
14–23 (Tx) 4–12 (Rx)	31:0	DMA completion status information	Status information reported by the DMA engine when it has finished processing a descriptor. As with the control information, the format of the status information differs between Tx and Rx descriptors. (See Table 3-3 on page 30 and Table 3-5 on page 33 for details)

The Tx descriptor format for words 2 through 13 is described in Table 3-2.

Table 3-2. **DMA Tx Descriptor Format for Words 2–13**

Word	Bits	Name	Description
2	11:0	frame_length	Frame length. Specifies the length, in bytes, of the entire MAC frame, including the frame check sequence (FCS), initialization vector (IV), and integrity check value (ICV). This field must appear in the descriptor for the first segment of a frame, and is ignored for all following descriptors of that frame.
	12	vmf	Virtual more fragment. If this bit is set, bursting is enabled for this frame. If no burst is in progress, it initiates a CTS-protected burst if CTSEn is set. If a previous burst is in progress, it ignores the CTSEn bit and assumes the burst is protected.
	15:13	RES	Reserved
	21:16	tpc_0	Tx power control These bits are passed unchanged to the baseband, where they are used to control the Tx power for the frame.

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

Word	Bits	Name	Description
2 (cont.)	22	rts_enable	Request to send (RTS) enable. If set, the PCU transmits the frame using the RTS/CTS protocol. If clear, the PCU transmits the frame using the contention/backoff protocol. At most, one of the "rts_enable" and "cts_enable" bits may be set; it is illegal to set both.
	23	veol	Virtual end-of-list flag. When set, indicates that the QCU should act as though the descriptor had a NULL LinkPtr, even if the LinkPtr is not NULL. Must be valid in the final descriptor of a frame and must be clear for all other descriptors of the frame.
	24	clear_dest_mask	Clear destination mask bit flag. If set, instructs the PCU and DCU to clear the destination mask bit at the index specified by the DestIdx field.
	28:25	RES	Reserved
	29	int_req	Interrupt request flag. Set to one by the driver to request that the DMA engine generate an interrupt upon completion of the frame to which this descriptor belongs. Note that this field must be valid and identical for all descriptors of the frame; that is, all descriptors for the frame must have this flag set, or all descriptors for the frame must have this flag clear.
	30	dest_index_valid	Destination index valid flag. Specifies whether the contents of the DestIdx field are valid.
	31	cts_enable	Proceed frame with CTS flag. If set, the PCU first sends a CTS before sending the frame described by the descriptor. Used for 802.11g and Atheros XR frames to quiet legacy stations before sending a frame the legacy stations cannot interpret (even at the PHY level). At most, one of the "rts_enable" and "cts_enable" bits may be set; it is illegal to set both bits.
3	11:0	buf_len	Data buffer length. Specifies the length, in bytes, of the data buffer associated with this descriptor. Tx data buffers may be any non-zero length buffers. This field must be valid for all descriptors.
	12	more	More descriptors in this frame flag. Set to one by the driver to indicate additional descriptors (DMA fragments) exist in the current frame. This field must be valid for all descriptors. 0 — No more descriptors for the current frame 1 — The current frame is continued in the next descriptor
	19:13	dest_index	Destination table index. Specifies an index to an on-chip table of per-destination information. The PCU fetches the encryption key from the specified index in this table and uses the key to encrypt the frame. DMA logic uses the index to maintain per-destination Tx filtering status and other related information.
	23:20	frame_type	Frame type indication. Indicates to the PCU what type of frame is being sent. Supported values: 0 — Normal frame 1 — Announcement traffic indication message (ATIM) frame 2 — PS poll frame 3 — Beacon 4 — Probe response frame 15:5 — Reserved

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

Word	Bits	Name	Description
3 (cont.)	24	no_ack	No ACK flag Must be set for any frame that has the 802.11 NoAck bit set in the QoS field and for all other frame types (e.g., beacons) that do not receive ACKs. 1 — Do not wait for ACK
	26:25	RES	Reserved
	27	ext_only	For 20–40 mode
	28	ext_and_ctl	For 20–40 mode
	29	more_agg	Indicates aggregate boundaries
	30	is_agg	Set for all descriptors for an aggregate
	31	RES	Reserved
4	14:0	burst_duration	Burst duration value (in µs). If this frame is not part of a burst or the last frame in a burst, the value should be zero. In a burst, the value is the amount of time to reserve (via NAV) after completing the current Tx packet sequence (after the ACK if applicable).
	15	dur_update_en	Frame duration update control. If set, the MAC updates (overwrites) the Duration field in the frame based on the current Tx rate. If clear, the MAC does not alter the contents of the frame's Duration field. Note that the MAC changes only the frame's Duration field. It does not alter the Duration field in the RTS/CTS that precedes the frame itself if "rts_enable" or "cts_enable" is set.
	19:16	tx_tries0	Number of frame data exchange attempts permitted for transmission series 0. A "frame data exchange attempt" means a transmission attempt in which the actual frame is sent on the air (in contrast to the case in which the frame has RTS enabled and the RTS fails to receive a CTS). In this case, the actual frame is not sent on the air, so this does not count as a frame data exchange attempt. A value of zero is illegal for the TXDataTries0 field.
	23:20	tx_tries1	Number of frame data exchange attempts permitted for transmission series 1. A value of zero means skip this transmission series.
	27:24	tx_tries2	Number of frame data exchange attempts permitted for transmission series 2. A value of zero means skip this transmission series.
	31:28	tx_tries3	Number of frame data exchange attempts permitted for transmission series 3. A value of zero means skip this transmission series.

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

<table>
<tr><th>Word</th><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>5</td><td>7:0</td><td>tx_rate0</td><td>Tx rate for transmission series 0.
<table>
<tr><th>MAC Rate Encoding</th><th>Protocol</th><th>Link Rate (Mbps)</th></tr>
<tr><td>0x0B</td><td rowspan="8">802.11g (OFDM)</td><td>6</td></tr>
<tr><td>0x0F</td><td>9</td></tr>
<tr><td>0x0A</td><td>12</td></tr>
<tr><td>0x0E</td><td>18</td></tr>
<tr><td>0x09</td><td>24</td></tr>
<tr><td>0x0D</td><td>36</td></tr>
<tr><td>0x08</td><td>48</td></tr>
<tr><td>0x0C</td><td>54</td></tr>
<tr><td>0x1B</td><td rowspan="8">802.11b (CCK)</td><td>1 L[1]</td></tr>
<tr><td>0x1A</td><td>2 L</td></tr>
<tr><td>0x1E</td><td>2 S</td></tr>
<tr><td>0x19</td><td>5.5 L</td></tr>
<tr><td>0x1D</td><td>5.5 S</td></tr>
<tr><td>0x18</td><td>11 L</td></tr>
<tr><td>0x1C</td><td>11 S</td></tr>
<tr><td>0x03</td><td rowspan="5">Reserved</td><td rowspan="5">Reserved</td></tr>
<tr><td>0x07</td></tr>
<tr><td>0x02</td></tr>
<tr><td>0x06</td></tr>
<tr><td>0x01</td></tr>
<tr><td>0x00, 0x04, 0x05, 0x010–0x17, 0x1F</td><td>Reserved</td><td>Reserved</td></tr>
</table>
[1]L = with long preamble; S = with short preamble.
<table>
<tr><th>Rate</th><th>Desc</th><th>Stream</th><th>HT20; GI=0 Mbps[1]</th><th>HT40; GI=0 Mbps</th><th>HT40; GI=1 Mbps</th></tr>
<tr><td>0x80</td><td>MCS 0</td><td>1</td><td>6.5</td><td>13.5</td><td>15</td></tr>
<tr><td>0x81</td><td>MCS 1</td><td>1</td><td>13</td><td>27</td><td>30</td></tr>
<tr><td>0x82</td><td>MCS 2</td><td>1</td><td>19.5</td><td>40.5</td><td>45</td></tr>
<tr><td>0x83</td><td>MCS 3</td><td>1</td><td>26</td><td>54</td><td>60</td></tr>
<tr><td>0x84</td><td>MCS 4</td><td>1</td><td>39</td><td>81</td><td>90</td></tr>
<tr><td>0x85</td><td>MCS 5</td><td>1</td><td>52</td><td>108</td><td>120</td></tr>
<tr><td>0x86</td><td>MCS 6</td><td>1</td><td>58.5</td><td>121.5</td><td>135</td></tr>
<tr><td>0x87</td><td>MCS 7</td><td>1</td><td>65</td><td>135</td><td>150</td></tr>
<tr><td>0x88</td><td>MCS 8</td><td>2</td><td>13</td><td>27</td><td>30</td></tr>
<tr><td>0x89</td><td>MCS 9</td><td>2</td><td>26</td><td>54</td><td>60</td></tr>
<tr><td>0x8A</td><td>MCS 10</td><td>2</td><td>39</td><td>81</td><td>90</td></tr>
<tr><td>0x8B</td><td>MCS 11</td><td>2</td><td>52</td><td>108</td><td>120</td></tr>
<tr><td>0x8C</td><td>MCS 12</td><td>2</td><td>78</td><td>162</td><td>180</td></tr>
<tr><td>0x8D</td><td>MCS 13</td><td>2</td><td>104</td><td>216</td><td>240</td></tr>
<tr><td>0x8E</td><td>MCS 14</td><td>2</td><td>117</td><td>243</td><td>270</td></tr>
<tr><td>0x8F</td><td>MCS 15</td><td>2</td><td>130</td><td>270</td><td>300</td></tr>
</table>
[1]For short guard interval (GI=1), HT20 mode is not allowed.</td></tr>
<tr><td></td><td>15:8</td><td>tx_rate1</td><td>Tx rate for transmission series 1; see the rate table in “tx_rate0”</td></tr>
<tr><td></td><td>23:16</td><td>tx_rate2</td><td>Tx rate for transmission series 2; see the rate table in “tx_rate0”</td></tr>
<tr><td></td><td>31:24</td><td>tx_rate3</td><td>Tx rate for transmission series 3; see the rate table in “tx_rate0”</td></tr>
</table>

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

Word	Bits	Name	Description	
6	14:0	packet_duration0	Packet duration 0 (in µs) Duration of the actual Tx frame associated with TXRate0. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	rts_cts_qual0	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 0.	
			1	Default behavior with respect to "rts_enable" and "cts_enable"
	30:16	packet_duration1	Packet duration 1 (in µs) Duration of the actual Tx frame associated with TXRate1. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	31	rts_cts_qual1	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 1.	
			1	Default behavior with respect to "rts_enable" and "cts_enable"
7	14:0	packet_duration2	Packet duration 2 (in µs) Duration of the actual Tx frame associated with TXRate2. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	15	rts_cts_qual2	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 2.	
			1	Default behavior with respect to"rts_enable" and "cts_enable"
	30:16	packet_duration3	Packet duration 3 (in µs) Duration of the actual Tx frame associated with TXRate3. This time does not include RTS, CTS, ACK, or any associated SIFS.	
	31	rts_cts_qual3	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 3.	
			1	Default behavior with respect to "rts_enable" and "cts_enable"
8	15:0	agg_length	Aggregate length	
	17:16	RES	Reserved	
	25:18	pad_delim	Number of delimiters to add at the end of a packet For AES, set to a minimum of 10. For packets under 256 bytes, add enough delimiters to make the packet 256 bytes. Each pad-delimit adds 4 bytes.	
	27:26	encrypt_type	Encryption type; the encryption field must be valid for all descriptions	
			0	None; 0 pad bytes
			1	WEP or TKIP (no MIC); 4 pad bytes
			2	AES; 8 pad bytes
			3	TKIP; 12 pad bytes
	31:28	RES	Reserved	

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

Word	Bits	Name	Description	
9	0	20_40_0	20_40 control for Tx series 0	
			0	HT20 Tx packet
			1	HT40 Tx packet
	1	GI_0	Guard interval control for Tx series 0	
			0	Normal guard interval
			1	Short guard interval
	4:2	chain_sel_0	Chain select for Tx series 0; 1, 5, and 7 are the only valid values	
			bit 0	Chain 0 is active
			bit 1	Chain 1 is active
			bit 2	Chain 2 is active
	5	20_40_1	20_40 control for Tx series 1	
			0	HT20 Tx packet
			1	HT40 Tx packet
	6	GI_1	Guard interval control for Tx series 1	
			0	Normal guard interval
			1	Short guard interval
	9:7	chain_sel_1	Chain select for Tx series 1; 1, 5, and 7 are the only valid values	
			bit 0	Chain 0 is active
			bit 1	Chain 1 is active
			bit 2	Chain 2 is active
	10	20_40_2	20_40 control for Tx series 2	
			0	HT20 Tx packet
			1	HT40 Tx packet
	11	GI_2	Guard interval control for Tx series 2	
			0	Normal guard interval
			1	Short guard interval
	14:12	chain_sel_2	Chain select for Tx series 2; 1, 5, and 7 are the only valid values	
			bit 0	Chain 0 is active
			bit 1	Chain 1 is active
			bit 2	Chain 2 is active
	15	20_40_3	20_40 control for Tx series 3	
			0	HT20 Tx packet
			1	HT40 Tx packet
	16	GI_3	Guard interval control for Tx series 3	
			0	Normal guard interval
			1	Short guard interval
	19:17	chain_sel_3	Chain select for Tx series 3. 1, 5, and 7 are the only valid values.	
			bit 0	Chain 0 is active
			bit 1	Chain 1 is active
			bit 2	Chain 2 is active
	27:20	rts_cts_rate	RTS or self-CTS rate selection. Specifies the rate the RTS sends at if rts_enable is set, or self CTS sends at if cts_enable is set. See the rate table in "tx_rate0".	
	31:28	RES	Reserved	

Table 3-2. **DMA Tx Descriptor Format for Words 2–13 (continued)**

Word	Bits	Name	Description
10	31:0	RES	Reserved
11	23:0	RES	Reserved
	29:24	tpc_1	Tx power control (TPC) for Tx series 1. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	31:30	RES	Reserved
12	23:0	RES	Reserved
	29:24	tpc_2	Tx power control (TPC) for Tx series 2. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	31:30	RES	Reserved
13	23:0	RES	Reserved
	29:24	tpc_3	Tx power control (TPC) for Tx series 3. These bits pass unchanged to the baseband, where they control Tx power for the frame.
	31:30	RES	Reserved

The Tx descriptor format for words 14 through 23 is described in Table 3-3.

Table 3-3. **DMA Tx Descriptor Completion Status Format for Words 14–23**

Word	Bits	Name	Description
14	7:0	rssi_ant00	Rx ACK signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.
	15:8	rssi_ant01	Rx ACK signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	23:16	rssi_ant02	Rx ACK signal strength indicator of control channel chain 2 A value of 0x80 (–128) indicates an invalid number.
	29:24	RES	Reserved
	30	BA_STATUS	If set, the BA_BITMAP values are valid
	31	RES	Reserved
15	0	frm_xmit_ok	Frame transmission success ■ If set, the frame was transmitted successfully ■ If clear, no ACK or BA was received during frame transmission
	1	excessive_retries	Excessive tries If set, transmission of the frame failed because the try limit was reached before the frame was transmitted successfully. Valid only for the final descriptor of a frame, and only if "frm_xmit_ok" is clear.
	2	fifo_underrun	Tx FIFO underrun flag If set, frame transmission failed because the DMA engine was not able to supply the PCU with data as quickly as the baseband was requesting data. Valid only for non-aggregate or non-RIFS underrun conditions unless the underrun occurred on the first packet of the aggregate or RIFS burst. See also the description for "tx_dlmtr_ underrun_err" and "tx_data_ underrun_err". Valid only if "frm_xmit_ok" is clear.
	3	filtered	Frame transmission filter indication If set, indicates that frame was not transmitted because the corresponding destination mask bit was set when the frame reached the PCU, or the frame violated TXOP on the first packet of a burst. Valid if "frm_xmit_ok" is clear.

Table 3-3. **DMA Tx Descriptor Completion Status Format for Words 14–23 (continued)**

Word	Bits	Name	Description
15 (cont.)	7:4	rts_fail_cnt	RTS failure count Reports the number of times an RTS was sent but no CTS received for the final transmission series (see "final_tx_index"). For frames with "rts_enable" clear, this count is always zero. Note that this count increments only when the RTS/CTS exchange fails and, in particular, does not increment if the RTS/CTS exchange succeeds but the frame fails because no ACK was received. Valid only for the final descriptor of a frame, regardless of "frm_xmit_ok" state.
	11:8	data_fail_cnt	Data failure count Reports the number of times the actual frame (as opposed to the RTS) was sent but no ACK received for the final transmission series (see "final_tx_index"). Valid only for the final descriptor of a frame, regardless of "frm_xmit_ok" state.
	15:12	virtual_retry_cnt	Virtual collision count Reports the number of virtual collisions that occurred before transmission of the frame ended. The counter value saturates at 0xF. A virtual collision refers to the case as described in the 802.11e QoS specification, in which two or more output queues simultaneously contend for a TXOP. In such cases, all lower-priority output queues experience a virtual collision in which the frame is treated as though it was sent on the air but failed to receive an ACK.
	16	tx_dlmtr_ underrun_err	Tx delimiter underrun error This error only occurs on aggregate frames when the underrun conditions happens while the MAC is sending delimiters.
	17	tx_data_ underrun_err	Tx data underrun error Only occurs on aggregate frames when the underrun condition happens while the MAC is sending the data portion of the frame or delimiters.
	18	desc_config_error	Descriptor configuration error This error occurs if the "ext_only", "ext_and_ctl", and current 20_40 values are not among the four valid combinations, or if "tx_dlmtr_ underrun_err" or "tx_data_ underrun_err" are set. See the description under "ext_and_ctl".
	19	tx_timer_expired	Tx timer expired This bit is set when the Tx frame takes longer to send to the baseband than is allowed based on the TX_TIMER register. Some regulatory domains require that Tx packets may not exceed a certain amount of transmit time.
	31:20	RES	Reserved
16	31:0	send_timestamp	Timestamp at the start of transmit A snapshot of the lower 32 bits of PCU's timestamp (TSF value). This field can aid the software driver in implementing requirements associated with the aMaxTransmitMSDULifetime MAC attribute. The Tx timestamp is sampled upon tx_frame signal rising that goes from the MAC to the baseband. This value corresponds to the last attempt at packet transmission (not the first attempt).
17	31:0	ba_bitmap_0-31	Block ACK bitmap 0 to 31 The values from the block that ACK received after successful transmission of an aggregate frame. Bit 0 if set represents the successful reception of the packet with the sequence number matching the seq_num value.
18	31:0	ba_bitmap_32-63	Block ACK bitmap 32 to 63 The values from the block that ACK received after successful transmission of an aggregate frame. Bit 0 if set represents the successful reception of the packet with the sequence number matching seq_num + 32.

Table 3-3. **DMA Tx Descriptor Completion Status Format for Words 14–23 (continued)**

Word	Bits	Name	Description
19	7:0	rssi_ant10	Receive ACK signal strength indicator of extension channel chain 0. A value of 0x80 (–128) indicates an invalid number.
	15:8	rssi_ant11	Receive ACK signal strength indicator of extension channel chain 1. A value of 0x80 (–128) indicates an invalid number.
	23:16	rssi_ant12	Receive ACK signal strength indicator of extension channel chain 2. A value of 0x80 (–128) indicates an invalid number.
20	31:0	EVM	Error vector magnitude 0 EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.
21	31:0	EVM	Error vector magnitude 1 EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.
22	31:0	EVM	Error vector magnitude 2 EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.
23	0	done	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid only for the final descriptor of a frame, regardless of the state of "frm_xmit_ok". The driver is responsible for tracking what descriptors are associated with a frame. When the DMA engine sets the Done flag in the final descriptor of a frame, the driver must be able to determine what other descriptors belong to the same frame and thus also have been consumed.
	12:1	SeqNum	Tx sequence number Indicates the sequence number from the response block ACK. This field should only be consulted if the Tx frame was an aggregate. Because hardware does not update the sequence number, this field does not need to be consulted for non-aggregate frames. For aggregates, this sequence number may not be the sequence number of the first Tx frame of the aggregate. More than likely has an older sequence number if the hardware of the other side keeps track of prior sequence numbers. It may sometimes have a newer sequence number if the first packet of the aggregate failed.
	16:13	RES	Reserved
	17	txop_exceeded	TXOP has been exceeded Indicates that this Tx frame had to be filtered because the amount of time to transmit this packet sequence would exceed the TXOP limit (which should only occur when software programs the TXOP limit improperly).
	20:18	RES	Reserved
	22:21	final_tx_index	Final transmission attempt series index Specifies the number of the Tx series that caused frame transmission to terminate.
	24:23	RES	Reserved
	25	pwr_mgmt	Power management state Indicates the value of the power management bit in the frame control field of the response ACK frame.
	31:25	RES	Reserved
31:24	31:0	TID	Traffic identifier of the block ACK

The DMA Rx logic (the DRU block) manages Rx descriptors and transfers the incoming frame data and status to the host through the PCI Interface. The Rx descriptor format for words 2 and 3 is described in Table 3-4.

Table 3-4. **DMA Rx Descriptor Format for Words 2 and 3**

Word	Bits	Name	Description
2	31:0	RES	Reserved
3	11:0	buf_len	Data buffer length (in bytes). Specifies the length of the data buffer associated with this descriptor. Rx data buffers must have a length that is an integral multiple of four bytes.
	12	RES	Reserved
	13	int_req	Interrupt request flag. Indicates whether the DMA engine should generate an interrupt upon frame completion. 0 – Do not generate an InterReq interrupt upon frame completion 1 – Generate an InterReq interrupt upon frame completion
	31:14	RES	Reserved

The Rx descriptor format for words 4 through 13 is described in Table 3-5.

Table 3-5. **DMA Rx Descriptor Completion Status Format for Words 4–13**

Word	Bits	Name	Description
4	7:0	rssi_ant00	Receive signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.
	15:8	rssi_ant01	Receive signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	23:16	rssi_ant02	Receive signal strength indicator of control channel chain 2 A value of 0x80 (–128) indicates an invalid number.
	31:24	rx_rate	Rx rate indication Indicates the rate this frame was transmitted from the source. Encodings match those used for the tx_rate_* field in word 5 of the Tx descriptor. Valid only if "frame_rx_ok" is set, or if it is clear and the "phy_error" flag is clear.
5	11:0	data_len	Received data length Specifies the length, in bytes, of the data actually received into the data buffer associated with this descriptor. The actual received data length is between zero and the total size of the data buffer, as specified originally in this field (see the description for "buf_len"). Valid for all descriptors.
	12	more	More descriptors in this frame flag If set, then this is not the final descriptor of the frame. If clear, this descriptor is the final one of the frame. Valid for all descriptors. 0 – No more descriptors for the current frame 1 – The current frame is continued in the next descriptor
	13	RES	Reserved
	21:14	num_delim	Number of zero length pad delimiters after current packet Does not include the start delimiter required between each packet in an aggregate; only valid for aggregate packets except for the last packet of an aggregate.
	31:22	RES	Reserved

Table 3-5. **DMA Rx Descriptor Completion Status Format for Words 4–13 (continued)**

Word	Bits	Name	Description
6	31:0	rcv_timestamp	A snapshot of the PCU's timestamp (TSF value) (in ms) Bits [31:0] of the PCU's 64-bit TSF. Intended for packet logging and packet sniffing. The timestamp is sampled on the rising edge of rx_clear, which goes from the baseband to the MAC.
7	0	gi	Rx packet guard interval. If this value is clear, the Rx frame used a long guard interval. If this value is set, the receive frame used a short guard interval.
	1	20_40	Rx packet 20 or 40 MHz bandwidth indicator. If this value is clear, the Rx frame was a HT20 packet (20 MHz bandwidth). If this value is set, then the receive frame was a HT40 packet (40 MHz bandwidth).
	2	duplicate	Rx packet duplicate indicator. If this value is set, the baseband has determined that this packet is a duplicate packet.
	31:3	RES	Reserved
8	7:0	rssi_ant10	Receive signal strength indicator of control channel chain 0 A value of 0x80 (–128) indicates an invalid number.
	15:8	rssi_ant11	Receive signal strength indicator of control channel chain 1 A value of 0x80 (–128) indicates an invalid number.
	23:16	rssi_ant12	Receive signal strength indicator of control channel chain 2 A value of 0x80 (–128) indicates an invalid number.
	31:24	rssi_combined	Rx signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (-128) indicates an invalid number.
9	31:0	EVM	Rx packet error vector magnitude 0
10	31:0	EVM	Rx packet error vector magnitude 1
11	31:0	EVM	Rx packet error vector magnitude 2
12	0	done	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information.Valid for all descriptors. 0: The MAC has not finished processing the descriptor. Valid only for the final descriptor of a frame. 1: The MAC has finished processing the descriptor and has updated the status information
	1	frame_rx_ok	Frame reception success flag If set, the frame was received successfully. If clear, an error occurred during frame reception. 0: An error occurred during frame reception 1: Frame received successfully
	2	crc_error	Cyclic redundancy code (CRC) error flag Valid only for the final descriptor of a frame, and only if the "frame_rx_ok" flag is clear. 0: Frame received without a CRC error 1: Reception of frame failed because of an incorrect CRC value
	3	decrypt_crc_err	Decryption CRC failure flag Valid only for the final descriptor of a frame, if the FrmRcvOK flag is clear.
	4	phy_error	PHY error flag If set, then reception of the frame failed because the PHY encountered an error. In this case, bits [15:8] of this word indicate the specific type of PHY error; see the baseband specification for details. Valid only if the 'frame_rx_ok' flag is clear.

Table 3-5. **DMA Rx Descriptor Completion Status Format for Words 4–13 (continued)**

Word	Bits	Name	Description
12 (cont.)	5	mic_error	Michael integrity check error flag If set, then the frame's TKIP Michael integrity check value did not verify correctly. Valid only when all of the following are true: ■ The "frame_rx_ok" bit is clear ■ The frame was decrypted using TKIP ■ The frame is not a fragment
	6	pre_delim_crc_err	Delimiter CRC error detected before this current frame
	7	RES	Reserved
	8	key_idx_valid	■ If "frame_rx_ok" is set, then this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the KeyIdx field reflects the table index at which the destination address was found. If clear, indicates that the PCU failed to locate the destination address in the key table and that the contents of KeyIdx field are undefined. ■ If "frame_rx_ok" is clear and the "phy_error" bit is set, then this field contains bit [0] of the PHY error code. In both cases, this field is valid only for the final descriptor of a frame.
	15:9	key_idx	■ If "frame_rx_ok" is set, then this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the KeyIdx field reflects the table index at which the destination address was found. If clear, indicates that the PCU failed to locate the destination address in the key table and that the contents of KeyIdx field are undefined. ■ If "frame_rx_ok" is clear and the "phy_error" bit is set, then this field contains bits [4:1] of the PHY error code, the upper three bits are zero. In both cases, this field is valid only for the final descriptor of a frame.
	16	more_agg	More aggregate flag This bit is only set for the last descriptor of the last packet of an aggregate.
	17	aggregate	Aggregate flag If set indicates that this packet is part of an aggregate.
	18	post_delim_crc_err	Delimiter CRC error detected after this current frame Only occurs when the start delimiter of the last frame in an aggregate is bad.
	29:19	RES	Reserved
	30	decrypt_busy_err	Decrypt busy error If set it indicates new frame arrived before decryption completed for the previous frame.
	31	key_miss	Key cache miss indication If set, indicates that the PCU could not locate a valid description key for the frame. Valid only if the "frame_rx_ok" is clear.

3.4 Queue Control Unit (QCU)

The queue control unit performs two tasks:

- Managing the Tx descriptor chain processing for frames pushed to the QCU from the host by traversing the linked list of Tx descriptors and transferring frame data from the host to the targeted DCU.
- Managing the queue transmission policy to determine when the frame at the head of the queue should be marked as available for transmission.

The MAC contains ten QCUs. Each QCU contains all the logic and state registers needed to manage a single queue (linked list) of Tx descriptors. A QCU is associated with exactly one DCU. When a QCU prepares a new frame, it signals ready to the DCU. When the DCU accepts the frame, the QCU responds by getting the frame data and passing it to the DCU for eventual transmission to the PCU and on to the air.

The host controls how the QCU performs these tasks by writing to various QCU configuration registers (see "QCU Registers" on page 60).

3.5 DCF Control Unit (DCU)

Collectively, the ten DCUs implement the EDCF channel access arbitration mechanism defined in the Task Group E (TGe) QoS extension to the 802.11 specification. Each DCU is associated with one of the eight EDCF priority levels and arbitrates with the other DCUs on behalf of all QCUs associated with it. A central DCU arbiter monitors the state of all DCUs and grants one the next access to the PCU (that is, access to the channel).

Because the EDCF standard defines eight priority levels, the first eight DCUs (DCUs 0–7) map directly to the eight EDCF priority levels. The two additional DCUs handle beacons and beacon-gated frames for a total of ten DCUs.

The mapping of physical DCUs to absolute channel access priorities is fixed and cannot be altered by software:

The highest-priority DCU is DCU 9. Typically, this DCU is the one associated with beacons.

The next highest priority DCU is DCU 8. Typically, this DCU is the one associated with beacon-gated frames.

The remaining eight DCUs priority levels are filled with DCUs 7 through 0. Among these 8 DCUs, DCU 7 has highest priority, DCU 6 the next highest priority, and so on through DCU 0, which has the lowest priority. Typically, these DCUs are associated with EDCF priorities seven through zero, respectively.

3.5.1 DCU State Information

Each DCU maintains sufficient state information to implement EDCF channel arbitration. Table 3-6 lists basic DCU state registers. (See "DCF Control Unit (DCU)" on page 36).

Table 3-6. **DCU Registers**

Register	Size	Description
D_QCUMASK	32	QCU mask
D_RETRY_LIMIT	32	Retry Limits
D_CHNTIME	32	ChannelTime settings
D_MISC	32	DCU-specific settings
D_SEQNUM	32	Frame sequence number control/status
D_GBL_IFS_SIFS	32	DCU-global IFS settings: SIFS duration
D_GBL_IFS_SLOT	32	DCU-global IFS settings: slot duration
D_GBL_IFS_EIFS	32	DCU-global IFS settings: EIFS duration
D_GBL_IFS_MISC	32	DCU-global IFS settings: misc. parameters
D_FPCTL	32	DCU frame prefetch settings
D_TXPSE	32	DCU Tx pause control/status
D_TXSLOTMASK	32	DCU transmission slot mask

3.6 Protocol Control Unit (PCU)

The PCU is responsible for the details of sending a frame to the baseband logic for transmission, for receiving frames from the baseband logic and passing the frame data to the DRU, including:

- Buffering Tx and Rx frames
- Encrypting and decrypting
- Generating ACK, RTS, and CTS frames
- Maintaining the timing synchronization function (TSF)
- Inserting and verifying FCS
- Generating virtual clear channel assessment (CCA)
- Updating and parsing beacons
- The PCU is primarily responsible for buffering outgoing and incoming frames and conducting medium access compatible with the IEEE 802.11 DCF protocol.

Figure 3-2 shows the PCU functional block diagram.

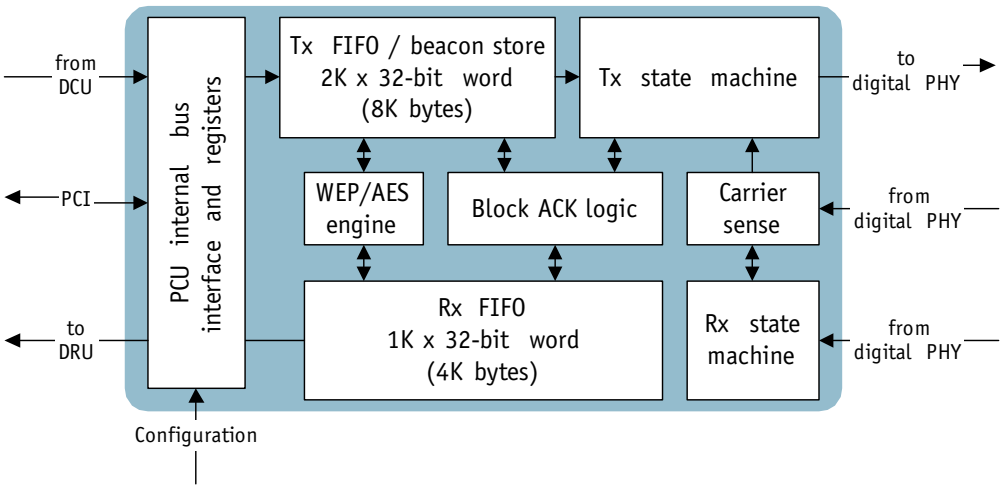


Figure 3-2. **PCU Functional Block Diagram**

4. Digital PHY Block

The digital physical layer (PHY) block is described in 802.11 draft-n mode and 802.11 a/b/g legacy mode. Transmit and receive paths are provided and shown as block diagrams for 802.11 draft-n mode.

4.1 Overview

The digital PHY block is a half-duplex, OFDM, CCK, DSSS baseband processor compatible with IEEE 802.11n and 802.11a/b/g. The AR5416 supports PHY data rates up to 300 Mbps in 20- and 40-MHz channel mode and all data rates defined by the IEEE 802.11a/b/g standard (1–54Mbps). Modulation schemes include BPSK, QPSK, 16-QAM, 64-QAM and forward error correction coding with rates of 1/2, 2/3, 3/4, 5/6.

4.2 802.11n (MIMO) Mode

Frames beginning with training symbols are used for signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. This process uses 56 sub-carriers for 20-MHz HT mode: 52 for data transmission and 4 for pilots. It uses 114 sub-carriers for 40-MHz HT mode: 108 for data transmission and 6 for pilots.

4.2.1 Transmitter (Tx)

Figure 4-1 shows the Tx path digital PHY 802.11n (MIMO mode) block diagram.

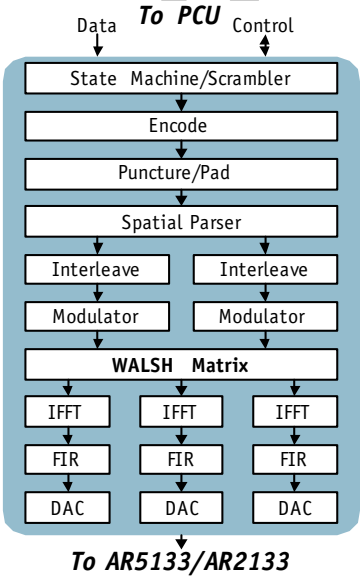


Figure 4-1. **Digital PHY 802.11n Tx**

The PCU block initiates transmission. The digital PHY powers on the digital to analog converter (DAC) and transmit portions of the AR5416. The training symbols are a fixed waveform and are generated within the digital PHY in parallel with the PCU sending the Tx header (frame length, data rate, etc.). The PCU must send transmitted data quickly enough to prevent buffers in the digital PHY from becoming empty. The PCU is prevented from sending data too quickly by pauses generated within the digital PHY.

Figure 4-1 shows a 3x3 MIMO system with two spatial data streams. The spatial parser splits the coded data into multiple data streams by allocating the proper number of bits to each data stream so that the number of data symbols resulted in each stream is the same. Then it interleaves coded bits across different data sub-carriers followed by the modulation. To achieve the maximum spatial diversity, the Walsh matrix orthogonally separates the two modulated streams into three before the streams undergo IFFT processing to produce time domain signals.

4.2.2 Receiver (Rx)

Figure 4-2 shows the Rx path digital PHY 802.11n (MIMO mode) block diagram.

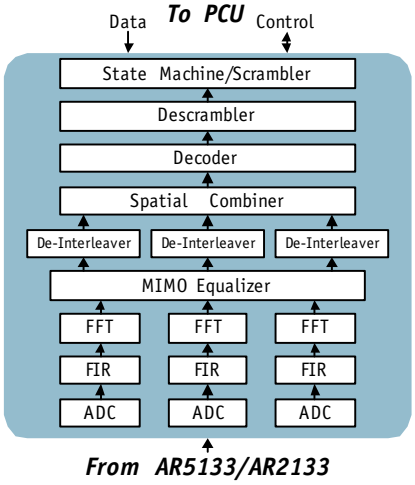


Figure 4-2. **Digital PHY 802.11n Rx**

The receiver inverts the transmitter's steps, performing a fast fourier transform (FFT), extracting bits from received constellations, de-interleaving, accounting for puncturing, decoding, and descrambling. The Rx block shows 3x3 MIMO configuration. The equalizer shown in Figure 4-2 is a frequency-domain equalizer handling degradation due to multi-path.

4.3 802.11 a/b/g Legacy Mode

4.3.1 Transmitter

The AR5416 digital PHY incorporates an OFDM and DSSS transceiver that supports all data rates defined by IEEE 802.11a/b/g. Legacy mode is detected on per-frame basis. PLCP frames are detected for legacy network information. The transmitter switches dynamically to generate legacy signals (802.11b/g in 2.4 GHz and 802.11a in 5 GHz).

4.3.2 Receiver

The receiver is capable of dynamically detecting legacy, HT 20MHz or 40 MHz frames and will demodulate the frame according to the detected frame type.

5. Register Descriptions

5.1 Beacon Handling

Table 5-1 describes sending a beacon and content after beacon (CAB).

Table 5-1. **Sending a Beacon and Content After Beacon**

	QCU/DCU	Description	See Register
AP in a BSS	QCU 9	QCU 9 is used only for beacons. It is the only queue control unit (QCU) that feeds into distributed coordination function (DCF) control unit (DCU) DCU 9.	
		■ Set FSP to DBA-gated	Bits [3:0] of the "Miscellaneous QCU Settings (Q_MISC)" register
		■ Set bit saying QCU is used to send beacons	Bit 7 of the Q_MISC register
		■ Set bit to disable CBRExpired counter increment if the local queue has no frames	Bit 5 of the Q_MISC register
	DCU 9	■ Set bit saying DCU is being used to send beacons	Bit 16 of the "Miscellaneous DCU-Specific Settings (D_MISC)" register
		■ Set bit to enable global lockout	Set bits [18:17] of the D_MISC register to 0x2
		■ Set both CW_MIN and CW_MAX to zero	D_LCL_IFS
	QCU 8	QCU 8 is used for CAB. For a basic service set (BSS), CAB is broadcast, uni-, and multi-cast frames. QCU 8 is the only QCU to feed into DCU 8.	
		■ Set FSP to DBA-gated	
		■ Set ReadyTimeEn bit and set the ReadyTimeDuration to: RTD = BeaconInterval – (SBA – DBA)	
		BeaconInterval	Interval between target beacon transmission time (TBTTs)
		SBA	Amount of time before TBTT that an SBA is generated
		DBA	Amount of time before TBTT that DBA is generated
		■ Set bit to disable CBRExpired counter increment if the beacon queue has no frames	Bit 6 of the Q_MISC register
		■ Set bit to disable CBRExpired counter increment if the local queue has no frames	Bit 5 of the Q_MISC register
	DCU 8	■ Set bit to enable global lockout	
	Software tasks at SBA (all of these must occur before DBA):		
	■ Build beacon and pass it to QCU 9		
	■ Build CAB and pass it to QCU 8		
	■ Clear all Tx filter bits for DCU 9 and DCU 8		

Table 5-1. **Sending a Beacon and Content After Beacon (continued)**

	QCU/DCU	Description	See Register
STA in an IBSS	QCU 9	QCU 9 is used only for beacons. It is the only queue control unit (QCU) that feeds into distributed coordination function (DCF) control unit (DCU) DCU 9.	
		■ Set FSP to DBA-gated	Bits [3:0] of the Q_MISC register
		■ Set bit saying QCU is used to send beacons	Bit 7 of the Q_MISC register
	DCU 9	■ Set bit saying DCU is being used to send beacons	Bit 16 of the D_MISC register
		■ Set bit to enable global lockout	Set bits [18:17] of the D_MISC register to 0x2
		■ Set both CW_MIN and CW_MAX to twice the usual CW_MIN value	See 802.11 specifications section 11.1.2.2
	QCU 8	QCU 8 is used for CAB. For an independent basic service set (IBSS), CAB is announcement traffic indication messages (ATIMs) followed by data frames that require preceding ATIM reception. QCU 8 is the only QCU to feed into DCU 8.	
		■ Set FSP to DBA-gated	
		■ Set ReadyTimeEn bit and set the ReadyTimeDuration to: RTD = BeaconInterval – (SBA – DBA)	
		BeaconInterval — Interval between TBTTs	
		SBA — Amount of time before TBTT that an SBA is generated	
		DBA — Amount of time before TBTT that DBA is generated	
		■ Set bit to disable CBRExpired counter increment if the beacon queue has no frames	Bit 6 of the Q_MISC register
		■ Set bit to disable CBRExpired counter increment if the local queue has no frames	Bit 5 of the Q_MISC register
		■ Set bit to clear TXE if ReadyTime expires	Bit 9 of the Q_MISC register
	DCU 8	■ Set bit to enable global lockout	
	Software tasks at SBA (all of these must occur before DBA):		
	■ Build beacon and pass it to QCU 9		
	■ Build CAB and pass it to QCU 8		
	■ Clear all Tx filter bits for DCU 9 and DCU 8		

5.2 General DMA and Rx-Related Registers

Table 5-2. **General DMA and Rx-Related Registers**

Offset	Access	Name	Description	Page
0x0008	R/W	CR	Command	page 44
0x000C	R/W	RXDP	Receive (Rx) queue descriptor pointer	page 44
0x0014	R/W	CFG	Configuration and status	page 44
0x0020	R/W	MIRT	Maximum interrupt rate threshold	page 45
0x0024	R/W	IER	Interrupt global enable	page 45
0x0028	R/W	TIMT	Transmit interrupt mitigation thresholds	page 46
0x0030	R/W	TXCFG	Tx configuration	page 46
0x0034	R/W	RXCFG	Rx configuration	page 47
0x0040	R/W	MIBC	MIB control	page 47
0x0044	R/W	TOPS	Timeout prescale	page 48
0x0048	R/W	RXNF	RXNOFR timeout	page 48
0x004C	R/W	TXNF	TXNOFR timeout	page 48
0x0050	R/W	RFGTO	Rx frame gap timeout	page 48
0x0054	R/W	RFCNT	Rx frame count limit	page 49
0x0064	R/W	GTT	Global Tx timeout	page 49
0x0068	R/W	GTTM	Global Tx timeout mode	page 49
0x006C	R/W	CST	Carrier sense timeout	page 50
0x0080	R	ISR_P	Primary interrupt status	page 50
0x0084	R	ISR_S0	Secondary interrupt status register 0	page 52
0x0088	R	ISR_S1	Secondary interrupt status register 1	page 52
0x008C	R	ISR_S2	Secondary interrupt status register 2	page 53
0x0090	R	ISR_S3	Secondary interrupt status register 3	page 54
0x0094	R	ISR_S4	Secondary interrupt status register 4	page 54
0x0098	R	ISR_S5	Secondary interrupt status register 5	page 54
0x00A0	R/W	IMR_P	Primary interrupt mask	page 55
0x00A4	R/W	IMR_S0	Secondary interrupt mask register 0	page 56
0x00A8	R/W	IMR_S1	Secondary interrupt mask register 1	page 56
0x00AC	R/W	IMR_S2	Secondary interrupt mask register 2	page 57
0x00B0	R/W	IMR_S3	Secondary interrupt mask register 3	page 57
0x00B4	R/W	IMR_S4	Secondary interrupt mask register 4	page 58
0x00B8	R/W	IMR_S5	Secondary interrupt mask register 5	page 58
0x00C0	R/W	ISR_P_RAC	Primary interrupt status register, read-and-clear access	page 58
0x00C4	R	ISR_S0_S	Secondary interrupt status register 0, shadow copy	page 58
0x00C8	R	ISR_S1_S	Secondary interrupt status register 1, shadow copy	page 59
0x00CC	R	ISR_S2_S	Secondary interrupt status register 2, shadow copy	page 59
0x00D0	R	ISR_S3_S	Secondary interrupt status register 3, shadow copy	page 59
0x00D4	R	ISR_S4_S	Secondary interrupt status register 4, shadow copy	page 59
0x00D8	R	ISR_S5_S	Secondary interrupt status register 5, shadow copy	page 59

5.2.1 Command (CR)

Offset: 0x0008
Access: Read/Write
Reset: (See field descriptions)

Bit	Name	Description
1:0	RES	Reserved
2	RXE	Rx enable; resets to 0x0
4:3	RES	Reserved
5	RXD	Rx disable; resets to 0x0
6	SWI	Software interrupt; one-shot/auto-cleared, always reads as 0
31:7	RES	Reserved

5.2.2 Receive Queue Descriptor Pointer (RXE)

Offset: 0x000C
Access: Read/Write
Cold reset: (Undefined)
Warm reset: (Unaffected)

Bit	Name	Description
1:0	RES	Reserved
31:2	RXDP	Rx descriptor pointer

5.2.3 Configuration and Status (CFG)

Offset: 0x0014
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Not reset on warm reset)

Bit		Description
0	Byteswap Tx descriptor words; resets to 0x0	
1	Byteswap Tx data buffer words; resets to 0x0	
2	Byteswap Rx descriptor words; resets to 0x0	
3	Byteswap Rx data buffer words; resets to 0x0	
4	Byteswap register access (MMR) data words; resets to 0x0	
5	Access point (AP) / ad hoc indication; resets to 0x0	
	0	AP mode; the MAC is operating either as an AP or as a station (STA) in a BSS
	1	Ad hoc mode; the MAC is operating as a STA in an IBSS
9:7	Reserved	
10	Clock gating disable; resets to 0x0	
	0	Allow clock gating in all DMA blocks to operate normally
	1	Reserved
11	DMA halt in preparation for reset request; resets to 0x0	
	0	DMA logic operates normally
	1	Requests that DMA logic stop immediately so software can reset the MAC. Bit [12] of this register indicates when the halt has taken effect. The DMA halt is not recoverable; once software sets bit [11] to request a DMA halt, software must wait for bit [12] to become set and reset the MAC. Any other operation yields unpredictable results.
12	DMA halt status; read-only.	
	0	DMA has not yet halted
	1	DMA has halted
31:13	Reserved	

5.2.4 Maximum Interrupt Rate Threshold (MIRT)

Offset: 0x0020
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
15:0	Maximum interrupt rate threshold Resets to 0x0. This register is described in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The maximum interrupt rate timer starts when either the TXINTM or RXIMTM status bits are set. TXMINTR or RXMINTR asserts at this time; no future TXINTM or RXINTM events can cause the TXMINTR or TXMINTR to assert until this timer has expired. If both the TXINTM and RXINTM status bits are set while the timer is expired then TXMINTR and RXMINTR round robin between the two.
31:16	Reserved

5.2.5 Interrupt Global Enable (IER)

Offset: 0x0024
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
0	Enable hardware signalling of interrupts; resets to 0x0
31:1	Reserved

5.2.6 Transmit Interrupt Mitigation Thresholds (TIMT)

Offset: 0x0028
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
15:0	Transmit last packet threshold Resets to 0x0. This register is described in µs up to a maximum of 65.535 ms. If this register is 0x0, this interrupt mitigation mechanism is disabled. The transmit last packet timer starts counting any time there is a transmit completion. If the timer is still counting when the next transmit completion occurs it resets and starts over. The last transmit packet timer expires when either the last transmit packet threshold equal the last transmit packet timer count or the first transmit packet threshold equals the first transmit packet timer count.
31:16	Transmit first packet threshold Resets to 0x0. This register is described in µs up to a maximum of 65.535 ms. If this register is 0x0, this interrupt mitigation mechanism is disabled. The transmit first packet timer starts counting when a transmit completion occurs. All further transmit completions are ignored until the timer expires by reaching the threshold. The first transmit packet timer expires when either the last transmit packet threshold equal the last transmit packet timer count or the first transmit packet threshold equals the first transmit packet timer count.

5.2.7 Transmit Configuration (TXCFG)

Offset: 0x0030
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Not reset on warm reset)

Bit	Description	
2:0	Maximum DMA request size for master reads; resets to 0x5.	
	0	4 B
	1	8 B
	2	16 B
	3	32 B
	4	64 B
	5	128 B
	6	256 B
	7	Reserved
3	Reserved	
9:4	Frame trigger level. Specifies the minimum number of bytes, in units of 64 bytes, that must be DMAed into the PCU TXFIFO before the PCU initiates sending the frame on the air; resets to 0x1 (i.e., 64 B or a full frame, whichever occurs first).	
31:10	Reserved	

5.2.8 Receive Configuration (RXCFG)

Offset: 0x0034
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Not reset on warm reset)

Bit	Description	
2:0	Maximum DMA size for master writes; resets to 0x4	
	0	4 B
	1	8 B
	2	16 B
	3	32 B
	4	64 B
	5	128 B
	6	256 B
	7	Reserved
4:3	Zero-length frame DMA enable; resets to 0x0	
	0	Disable DMA of all zero-length frames. In this mode, the DMA logic suppresses all zero-length frames. Reception of zero-length frames is invisible to the host (they neither appear in host memory nor consume an Rx descriptor)
	1	Reserved
	2	Enable DMA of all zero-length frames. In this mode, all zero-length frames (chirps, double-chirps, and non-chirps) DMA into host memory just like normal (non-zero-length) frames.
	3	Reserved
31:5	Reserved	

5.2.9 MIB Control (MIBC)

Offset: 0x0040
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Not reset on warm reset)

Bit	Description	
0	Warning test indicator; resets to 0x0. Read Only	
1	Freeze all counters; resets to 0x1.	
2	Clear all counters; resets to 0x1.	
3	MIB counter strobe. This bit is a one-shot and always reads as zero. For writes:	
	0	No effect
	1	Causes every MIB counter to increment by one
31:4	Reserved	

5.2.10 Timeout Prescale (TOPS)

Offset: 0x0044
Access: Read/Write
Reset: (See field descriptions)

NOTE: Controls the prescale for interrupt-related timeouts. Set to 0 to disable.

Bit	Description
15:0	Timeout prescale count; resets to 0x0000
31:16	Reserved

5.2.11 RXNOFR Timeout (RXNF)

Offset: 0x0048
Access: Read/Write
Reset: (See field descriptions)

NOTE: Set to 0 to disable.

Bit	Description
9:0	Timeout count limit; resets to 0x000
31:10	Reserved

5.2.12 TXNOFR Timeout (TXNF)

Offset: 0x004C
Access: Read/Write
Reset: (See field descriptions)

NOTE: Set to 0 to disable.

Bit	Description
9:0	Timeout count limit; resets to 0x000
14:10	QCU mask. Specifies the set of QCUs for which frame completions causes a reset of the TXNOFR timeout; resets to 0x0000.
31:15	Reserved

5.2.13 Receive Frame Gap Timeout (RFGTO)

Offset: 0x0050
Access: Read/Write
Reset: (See field descriptions)

NOTE: Set to 0 to disable.

Bit	Description
9:0	Timeout count limit; resets to 0x000
31:10	Reserved

5.2.14 Receive Frame Count Limit (RFCNT)

Offset: 0x0054
Access: Read/Write
Reset: (See field descriptions)

NOTE: Set to 0x1F (decimal 31) to disable.

Bit	Description
4:0	Frame count limit; resets to 0x1F
31:5	Reserved

5.2.15 Global Transmit Timeout (GTT)

Offset: 0x0064
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
15:0	Timeout counter in time units (TU = 1024 µs). This current value of the timeout counter resets on every transmit. If no Tx frame is queued up and ready to transmit, then the timeout counter stays at 0. Otherwise the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit, the global Tx timeout interrupt is set in the interrupt service register (ISR). This mechanism can be used to detect whether a Tx frame is ready and unable to be transmitted for some reason (e.g., NAV, carrier sense, quiet collision, etc.).
31:16	Timeout limit (TU = 1024 µs). On reset this value is set to 25 TU.

5.2.16 Global Transmit Timeout Mode (GTTM)

Offset: 0x0068
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
0	USEC strobe. If this bit is set then the GTT timer will not use the TU based strobe but rather use a µs strobe to increment the timeout counter.
1	Ignore channel idle. If this bit is set then the GTT timer will not increment if the channel idle indicates the air is busy or NAV is still counting down.
2	Reset count on channel idle low. Reset count every time channel idle is low.
3	CST USEC strobe. If this bit is set then the CST timer will not use the TU based strobe but rather use the µs strobe to increment the timeout counter.
31:4	Reserved

5.2.17 Carrier Sense Timeout (CST)

Offset: 0x006C
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
15:0	Timeout counter (TU = 1024 µs). This current value of the timeout counter resets on every transmit. If no Tx frame is queued up and ready to transmit, then the timeout counter stays at 0. Otherwise the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit, the carrier sense timeout (CST) interrupt is set in the ISR. This mechanism can be used to detect whether transmit is stuck (if RX_CLEAR remains low for an extended period of time). This counter starts counting if there are any queues ready to transmit. It continues counting when RX_CLEAR is low.
31:16	Timeout limit (TU = 1024 µs). On reset this value is set to 16 TU.

5.2.18 Primary Interrupt Status (ISR_P)

Offset: 0x0080
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

NOTE:

- The bits that are logical ORs of bits in the secondary ISRs are generated by logically ORing the secondary ISR bits after the secondary ISR bits have been masked with the appropriate bits from the corresponding secondary interrupt mask register.
- A write of one to a bit that is a logical OR of bits in a secondary ISR clears the secondary ISR bits from which the primary ISR bit is generated. For example: A write of a one to the TXOK bit (bit 6) in ISR_P clears all 10 TXOK bits in ISR_S0 (bits 9:0 of ISR_S0).
- Only the bits in this register (ISR_P) and the "Primary Interrupt Mask (IMR_P)" register control whether the MAC's interrupt output is asserted. Bits in the secondary interrupt status/mask registers control which bits are set in the primary ISR; however, the IMR_S* registers do not determine whether INTA# is asserted. That is, INTA# is asserted only when the logical AND of ISR_P and IMR_P is non-zero. The secondary interrupt mask/status registers affect which bits are set in ISR_P, but they do not directly affect whether interrupt is asserted.

Bit	Name	Description
0	RXOK	Frame was received with no errors
1	RXDESC	Frame was received and the desc_InterReq field was such that an interrupt was generated
2	RXERR	Frame was received with errors
3	RXNOFR	No frame received for RXNOFR timeout clocks
4	RXEOL	RXDESC fetch logic has no more RXDESC available
5	RXORN	Rxfifo overrun
6	TXOK	Logical OR of all TXOK bits in secondary ISR 0. Indicates that at least one frame was completed with no errors and at the requested rate, regardless of whether the InterReq bit was set)
7	TXDESC	Logical OR of all TXDESC bits in secondary ISR 0. Indicates that at least one frame was sent and last descriptor had the InterReq bit set.

Bit	Name	Description
8	TXERR	Logical OR of all TXERR bits in secondary ISR 1. Indicates that at least one frame was completed with an error, regardless of whether the InterReq bit was set.
9	TXNOFR	Has not transmitted a frame in TXNOFR timeout clocks. Only one TXNOFR bit exists for all QCUs; see the "TXNOFR Timeout (TXNF)" register for more information.
10	TXEOL	Logical OR of all TXEOL bits in secondary ISR 1. Indicates that at least one Tx descriptor fetch state machine has no more Tx descriptors available.
11	TXURN	Logical OR of all TXURN bits in secondary ISR 2. Indicates that the PCU reported a Txfifo underrun for at least one QCU's frame.
12	MIB	One of the MIB regs has reached its threshold
13	SWI	Software interrupt signalled. See the "Command (CR)" register.
14	RXPHY	The PHY signalled an error on a received frame
15	RXKCM	Key cache miss. A frame was received with the Key Cache Miss Rx status bit set.
16	SWBA	PCU has signalled a software beacon alert
17	BRSSI	PCU indicates that the RSSI of a beacon it has received has fallen below a programmable threshold
18	BMISS	PCU indicates that is has not received a beacon during the previous *N* beacon periods (*N* is programmable)
19	TXMINTR	TXMINTR Maximum transmit interrupt rate Same as TXINTM with the added requirement that maximum interrupt rate count has reached its threshold. This interrupt will alternate with RXMINTR.
20	BNR	Beacon Not Ready. Indicates that the QCU marked as being used for beacons (see the "Miscellaneous QCU Settings (Q_MISC)" register) received a DMA beacon alert when the queue contained no frames.
21	RXCHIRP	Indicates that the PHY reported that a chirp was received
22	RES	Reserved.
23	BCNMISC	Miscellaneous beacon-related interrupts. This bit is the logical OR of the CST, GTT, TIM, CABEND, DTIMSYNC, BCNTO, CABTO, TSFOOR, DTIM, and TBTT_TIME bits in the "Secondary Interrupt Status 2 (ISR_S2)" register.
24	RXMINTR	Maximum receive interrupt rate. Same as RXINTM with the added requirement that maximum interrupt rate count has reached its threshold. This interrupt will alternate with TXMINTR.
25	QCBROVF	Logical OR of all QCBROVF bits in the "Secondary Interrupt Status 3 (ISR_S3)" register. Indicates that at least one QCU's CBR expired counter has reached the value of the QCU's CBR_OVF_THRESH parameter.
26	QCBRURN	Logical OR of all QCBRURN bits in the "Secondary Interrupt Status 3 (ISR_S3)" register. Indicates that at least one QCU's frame scheduling trigger event occurred when no frames were present on the queue.
27	QTRIG	Logical OR of all QTRIG bits in the "Secondary Interrupt Status 4 (ISR_S4)" register. Indicates that at least one QCU's frame scheduling trigger event has occurred.
28	GENTMR	Logical OR of all GENERIC TIMER bits in the "Secondary Interrupt Status 4 (ISR_S4)" register, which include the GENERIC_TIMER_TRIGGER[7:0], GENERIC_TIMER_THRESH[7:0], and GENERIC_TIMER_OVERFLOW.
29	RES	Reserved.

Bit	Name	Description
30	TXINTM	Transmit completion interrupt after mitigation. Either the first tx packet or last tx packet interrupt mitigation count has reached its threshold. See TIMT register definition.
31	RXINTM	Receive completion interrupt after mitigation. Either the first rx packet or last rx packet interrupt mitigation count has reached its threshold. See RIMT register definition.

5.2.19 Secondary Interrupt Status 0 (ISR_S0)

Offset: 0x0084
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

Bit	Description
0	TXOK for QCU 0
1	TXOK for QCU 1
...	...
9	TXOK for QCU 9
15:10	Reserved
16	TXDESC for QCU 0
17	TXDESC for QCU 1
...	...
25	TXDESC for QCU 9
31:26	Reserved

5.2.20 Secondary Interrupt Status 1 (ISR_S1)

Offset: 0x0088
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

Bit	Description
0	TXERR for QCU 0
1	TXERR for QCU 1
...	...
9	TXERR for QCU 9
15:10	Reserved
16	TXEOL for QCU 0
17	TXEOL for QCU 1
...	...
25	TXEOL for QCU 9
31:26	Reserved

5.2.21 Secondary Interrupt Status 2 (ISR_S2)

Offset: 0x008C
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

Bit	Name	Description	
0	TXURN	TXURN for QCU 0	
1	TXURN	TXURN for QCU 1	
...	...	...	
9	TXURN	TXURN for QCU 9	
15:10	RES	Reserved	
16	MCABT_SI	Set if the PCI bus signals a master cycle abort. During a MAC-initiated master read or write cycle, the PCI/CardBus Interface received either a Target Abort on the PCI bus because the target explicitly aborted the transaction, or the PCI/CardBus Interface received a Master Abort on the PCI bus because no target ever responded to the transaction.	
		0	No interrupt
		1	PCI master cycle abort
17	SSERR_SI	Signalled system error. Set if a parity error is detected on a PCI address cycle	
		0	No interrupt
		1	PCI system error
18	DPERR_SI	Detected parity error. Set if a parity error is detected on a PCI data cycle	
		0	No interrupt
		1	PCI system error
23:19	RES	Reserved	
22	CST	Carrier sense timeout. Indicates that the CST count is equal to or greater than the CST limit.	
23	GTT	Global Tx timeout indicates that the GTT count became equal to or greater than the GTT limit	
24	TIM	A beacon was received with the local STA's bit set in the traffic indication map (TIM) element	
25	CABEND	End of CAB traffic. A CAB frame was received with the more data bit clear in the frame control field.	
26	DTIMSYNC	Delivery traffic indication message (DTIM) synchronization lost. A beacon was received that was expected to be a DTIM but was not, or a beacon was received that was not expected to be a DTIM but was.	
27	BCNTO	Beacon timeout. TBTT occurred and the STA began waiting to receive a beacon, but no beacon was received before the PCU's beacon timeout expired.	
28	CABTO	CAB timeout. A beacon was received that indicated that the STA should expect to receive CAB traffic. However, the PCU's CAB timeout expired either because the STA received no CAB traffic, or because the STA received some CAB traffic but never received a CAB frame with the more data bit clear in the frame control field, which would indicate the final CAB frame.	
29	DTIM	A beacon was received with the DTIM bit set and a DTIM count value of zero. Beacons that have the DTIM bit set but a non-zero DTIM count do not generate this interrupt.	
30	TSFOOR	TSF out of range. Indicates that the corrected TSF received from a beacon differs from the PCU's internal TSF by more than a (programmable) threshold.	
31	TBTT_TIME	TBTT-referenced timer interrupt. Indicates that the PCU's TBTT-referenced timer has elapsed.	

5.2.22 Secondary Interrupt Status 3 (ISR_S3)

Offset: 0x0090
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

Bit	Description
0	QCBROVF for QCU 0
1	QCBROVF for QCU 1
...	...
9	QCBROVF for QCU 9
15:10	Reserved
16	QCBRURN for QCU 0
17	QCBRURN for QCU 1
...	...
25	QCBRURN for QCU 9
31:26	Reserved

5.2.23 Secondary Interrupt Status 4 (ISR_S4)

Offset: 0x0094
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

Bit	Description
0	QTRIG for QCU 0
1	QTRIG for QCU 1
...	...
9	QTRIG for QCU 9
31:10	Reserved

5.2.24 Secondary Interrupt Status 5 (ISR_S5)

Offset: 0x0098
Access: Read; Write-one-to-clear
Reset: All bits reset to 0x0

NOTE:

- Trigger indicates that the TSF matched or exceeded the timer. See "Generic Timers (MAC_PCU_GENERIC_TIMERS[0:15])" and "Generic Timers Mode (MAC_PCU_GENERIC_TIMERS_MODE)".
- The threshold is set when the TSF exceeds the timer by the value GENERIC_TIMER_THRESH. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ timer + period, which indicates incorrect software programming.

Bit	Description
0	GENERIC_TIMER 0 trigger
1	GENERIC_TIMER 1 trigger
...	...
7	GENERIC_TIMER 7 trigger
8	Reserved
9	GENERIC_TIMER 1 threshold
...	...
15	GENERIC_TIMER 7 threshold
16	GENERIC_TIMER overflow
31:17	Reserved

5.2.25 Primary Interrupt Mask (IMR_P)

Offset: 0x00A0
Access: Read/Write
Reset: All bits reset to 0x0

NOTE: Only the bits in this register control whether the PCI_INT_L output will be asserted by the MAC. The bits in the secondary interrupt mask registers control which bits are set in the primary ISR. However, the IMR_S0 to IMR_S5 registers (see "Secondary Interrupt Mask 0 (IMR_S0)" to "Secondary Interrupt Mask 5 (IMR_S5)") do not determine whether INTA# is asserted.

Bit	Description
0	RXOK interrupt enable
1	RXDESC interrupt enable
2	RXERR interrupt enable
3	RXNOFR interrupt enable
4	RXEOL interrupt enable
5	RXORN interrupt enable
6	TXOK interrupt enable
7	TXDESC interrupt enable
8	TXERR interrupt enable
9	TXNOFR interrupt enable
10	TXEOL interrupt enable
11	TXURN interrupt enable
12	MIB interrupt enable
13	SWI interrupt enable
14	RXPHY interrupt enable
15	RXKCM interrupt enable
16	SWBA interrupt enable
17	BRSSI interrupt enable
18	BMISS interrupt enable
19	TXMINTR interrupt enable
20	BNR interrupt enable
21	RXCHIRP interrupt enable
22	HCFPOLL interrupt enable
23	BCNMISC interrupt enable
24	RXMINTR interrupt enable
25	QCBROVF interrupt enable
26	QCBRURN interrupt enable
27	QTRIG interrupt enable
28	GENTMR interrupt enable
29	HCFTO interrupt enable
30	TXINTM interrupt enable
31	RXINTM interrupt enable

5.2.26 Secondary Interrupt Mask 0 (IMR_S0)

Offset: 0x00A4
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	TXOK for QCU 0 interrupt enable
1	TXOK for QCU 1 interrupt enable
...	...
9	TXOK for QCU 9 interrupt enable
15:10	Reserved
16	TXDESC for QCU 0 interrupt enable
17	TXDESC for QCU 1 interrupt enable
...	...
25	TXDESC for QCU 9 interrupt enable
31:26	Reserved

5.2.27 Secondary Interrupt Mask 1 (IMR_S1)

Offset: 0x00A8
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	TXERR for QCU 0 interrupt enable
1	TXERR for QCU 1 interrupt enable
...	...
9	TXERR for QCU 9 interrupt enable
15:10	Reserved
16	TXEOL for QCU 0 interrupt enable
17	TXEOL for QCU 1 interrupt enable
...	...
25	TXEOL for QCU 9 interrupt enable
31:26	Reserved

5.2.28 Secondary Interrupt Mask 2 (IMR_S2)

Offset: 0x00AC
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	TXURN for QCU 0 interrupt enable
1	TXURN for QCU 1 interrupt enable
...	...
9	TXURN for QCU 9 interrupt enable
15:10	Reserved
16	MCABT interrupt enable
17	SSERR interrupt enable
18	DPERR interrupt enable
21:19	Reserved
22	CST interrupt enable
23	GTT interrupt enable
24	TIM interrupt enable
25	CABEND interrupt enable
26	DTIMSYNC interrupt enable
27	BCNTO interrupt enable
28	CABTO interrupt enable
29	DTIM interrupt enable
30	TSFOOR interrupt enable
31	TBTT_TIME interrupt enable

5.2.29 Secondary Interrupt Mask 3 (IMR_S3)

Offset: 0x00B0
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	QCBROVF for QCU 0 interrupt enable
1	QCBROVF for QCU 1 interrupt enable
...	...
9	QCBROVF for QCU 9 interrupt enable
15:10	Reserved
16	QCBRURN for QCU 0 interrupt enable
17	QCBRURN for QCU 1 interrupt enable
...	...
25	QCBRURN for QCU 9 interrupt enable
31:26	Reserved

5.2.30 Secondary Interrupt Mask 4 (IMR_S4)

Offset: 0x00B4
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	QTRIG for QCU 0 interrupt enable
1	QTRIG for QCU 1 interrupt enable
...	...
9	QTRIG for QCU 9 interrupt enable
31:10	Reserved

5.2.31 Secondary Interrupt Mask 5 (IMR_S5)

Offset: 0x00B8
Access: Read/Write
Reset: All bits reset to 0x0

Bit	Description
0	GENERIC_TIMER 0 trigger enable
1	GENERIC_TIMER 1 trigger enable
...	...
7	GENERIC_TIMER 7 trigger enable
8	GENERIC_TIMER 0 threshold enable
9	GENERIC_TIMER 1 threshold enable
...	...
15	GENERIC_TIMER 7 threshold enable
16	GENERIC_TIMER overflow enable
31:17	Reserved

5.2.32 Primary Interrupt Status, Read-and-Clear Access (ISR_P_RAC)

Offset: 0x00C0
Access: Read-and-clear/no write access
Reset: (Undefined)

NOTE: A read from this location atomically:

- Copies all secondary ISRs into the corresponding secondary ISR shadow registers (ISR_S0 is copied to ISR_S0_S, etc.)
- Clears all bits of the primary ISR (ISR_P) as well as all bits of all secondary ISRs (ISR_S0 through ISR_S4)
- Returns the contents of the primary ISR ("Primary Interrupt Status (ISR_P)")

Bit	Description
31:0	Same format as primary ISR ("Primary Interrupt Status (ISR_P)")

5.2.33 Secondary Interrupt Status 0, Shadow Copy (ISR_S0_S)

Offset: 0x00C4
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 0 ("Secondary Interrupt Status 0 (ISR_S0)")

5.2.34 Secondary Interrupt Status 1, Shadow Copy (ISR_S1_S)

Offset: 0x00C8
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 1 (“Secondary Interrupt Status 1 (ISR_S1)”)

5.2.35 Secondary Interrupt Status 2, Shadow Copy (ISR_S2_S)

Offset: 0x00CC
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 2 (“Secondary Interrupt Status 2 (ISR_S2)”)

5.2.36 Secondary Interrupt Status 3, Shadow Copy (ISR_S3_S)

Offset: 0x00D0
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 3 (“Secondary Interrupt Status 3 (ISR_S3)”)

5.2.37 Secondary Interrupt Status 4, Shadow Copy (ISR_S4_S)

Offset: 0x00D4
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 4 (“Secondary Interrupt Status 4 (ISR_S4)”)

5.2.38 Secondary Interrupt Status 5, Shadow Copy (ISR_S5_S)

Offset: 0x00D8
Access: Read-only
Reset: (Undefined)

Bit	Description
31:0	Same format as secondary ISR 5 (“Secondary Interrupt Status 5 (ISR_S5)”)

5.3 QCU Registers

Table 5-3. **QCU Registers**

Offset	Access	Name	Description	Page
0x0800 + (Q << 2)[1]	R/W	Q_TXDP	Tx queue descriptor pointer	page 60
0x0840	R/W	Q_TXE	Tx queue enable	page 60
0x0880	R/W	Q_TXD	Tx queue disable	page 61
0x08C0 + (Q << 2)[1]	R/W	Q_CBRCFG	CBR configuration	page 61
0x0900 + (Q << 2)[1]	R/W	Q_RDYTIMECFG	ReadyTime configuration	page 61
0x0940	R/W	Q_ONESHOTARM_SC	OneShotArm set control	page 62
0x0980	R/W	Q_ONESHOTARM_CC	OneShotArm clear control	page 62
0x09C0 + (Q << 2)[1]	R/W	Q_MISC	Miscellaneous QCU settings	page 63
0x0A00 + (Q << 2)[1]	R	Q_STS	Miscellaneous QCU status	page 64
0x0A40	R/W	Q_RDYTIMESHDN	ReadyTimeShutdown status	page 64

[1]Ten QCUs exist, numbered from 0 to 9. The variable *Q* in these register addresses refers to the QCU number.

5.3.1 Transmit Queue Descriptor Pointer (Q_TXDP)

Offset: 0x0800 + (*Q* << 2)[1]
Access: Read/Write
Cold reset: (Undefined)
Warm reset: (Unaffected)

Bit	Description
1:0	Reserved
31:2	Tx descriptor pointer

5.3.2 Transmit Queue Enable (Q_TXE)

Offset: 0x0840
Access: Read/Write
Reset: (See field descriptions)

NOTE: Writing a 1 in bit position *N* sets the TXE bit for QCU *N*. Writing a 0 in bit position *N* has no effect; in particular, it does not clear the TXE bit for the QCU

Bit	Description
0	Enable QCU 0; resets to 0x0
1	Enable QCU 1; resets to 0x0
...	...
9	Enable QCU 9; resets to 0x0
31:10	Reserved

5.3.3 Transmit Queue Disable (Q_TXD)

Offset: 0x0880
Access: Read/Write
Reset: (See field descriptions)

NOTE:

- To stop transmission for QCU Q:
  - Write a 1 to QCU Q's TXD bit
  - Poll the Q_TXE register until QCU Q's TXE bit is clear
  - Poll QCU Q's Q_STS register until its pending frame count (bits [1:0] of Q_STS) is zero
  - Write a 0 to QCU Q's TXD bit. At this point, QCU Q has shut down and has no frames pending in its associated DCU.
- Software must not write a 1 to a QCU's TXE bit when that QCU's TXD bit is set. Undefined operation will result.
- Software must ensure that it sets a QCU's TXE bit only when the QCU's TXD bit is clear. Writing a 0 to TXE when TXD is set is fine, but has no effect on the QCU.

Bit	Description
0	Disable QCU 0; resets to 0x0
1	Disable QCU 1; resets to 0x0
...	...
9	Disable QCU 9; resets to 0x0
31:10	Reserved

5.3.4 CBR Configuration (Q_CBRCFG)

Offset: 0x08C0 + (*Q* << 2)[1]
Access: Read/Write
Reset: (See field descriptions)

Bit	Description
23:0	CBR interval in µs; resets to 0x0
31:24	CBR overflow threshold. Determines the value of the CBR expired counter at which a CBROVF interrupt will be generated; resets to 0x0.

5.3.5 ReadyTime Configuration (Q_RDYTIMECFG)

Offset: 0x0900 + (*Q* << 2)[1]
Access: Read/Write
Reset: (See field descriptions)

Bit	Description	
23:0	ReadyTime duration in µs; resets to 0x0	
24	ReadyTime enable; resets to 0x0	
	0	Disable ReadyTime use
	1	Enable ReadyTime use
31:25	Reserved	

5.3.6 OneShotArm Set Control (Q_ONESHOTARM_SC)

Offset: 0x0940
Access: Read/Write
Reset: (See field descriptions)

NOTE: A read to this register returns the current state of all OneShotArm bits (QCU Q's OneShotArm bit is returned in bit position Q).

Bit	Description	
0	0	No effect
	1	Set OneShot arm bit for QCU 0
1	0	No effect
	1	Set OneShot arm bit for QCU 1
...	...	
9	0	No effect
	1	Set OneShot arm bit for QCU 10
31:10	Reserved	

5.3.7 OneShotArm Clear Control (Q_ONESHOTARM_CC)

Offset: 0x0980
Access: Read/Write
Reset: (See field descriptions)

NOTE: A read to this register returns the current state of all OneShotArm bits (QCU Q's OneShotArm bit is returned in bit position Q).

Bit	Description	
0	0	No effect
	1	Set OneShot arm bit for QCU 0
1	0	No effect
	1	Clear OneShot arm bit for QCU 1
...	...	
9	0	No effect
	1	Clear OneShot arm bit for QCU 9
31:10	Reserved	

5.3.8 Miscellaneous QCU Settings (Q_MISC)

Offset: 0x09C0 + (Q << 2)[1]
Access: Read/Write
Reset: (See field descriptions)

Bit	Description	
3:0	Frame scheduling policy setting; resets to 0x0.	
	0	ASAP. The QCU is enabled continuously.
	1	CBR. The QCU will be enabled under control of the settings in the Q_CBRCFG register.
	2	DBA-gated. The QCU will be enabled at each occurrence of a DMA beacon alert.
	3	TIM-gated. The QCU will be enabled whenever: ■ In STA mode, the PCU indicates that a beacon frame has been received with the local STA's bit set in the TIM element. ■ In IBSS mode, the PCU indicates that an ATIM frame has been received.
	4	Beacon-sent-gated. The QCU will be enabled when the DCU that is marked as being used for beacon transmission (see bit 16 of the "Miscellaneous DCU-Specific Settings (D_MISC)" register) indicates that it has sent the beacon frame on the air
	5	Beacon-received-gated. The QCU is enabled when the PCU indicates it has received a beacon.
	6	HCF Poll gated. The QCU will be enabled whenever the receive HCF poll event occurs. This signal comes from the PCU when a directed HCF poll frame type is received with valid FCS.
	15:7	Reserved
4	OneShot enable; resets to 0x0.	
	0	Disable OneShot function
	1	Enable OneShot function. Note that OneShot must not be enabled when the QCU is set to an ASAP frame scheduling policy.
5	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the queue contains no frames; resets to 0x0.	
	0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the queue contains frames
	1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the queue is valid (the queue is valid whenever TXE is asserted)
6	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the QCU marked as being used for beacon transmission (that is, the QCU that has bit 7 set in its Q_MISC register) contains no frames; resets to 0x0.	
	0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the beacon queue contains frames
	1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the beacon queue is valid (the beacon queue is valid whenever its TXE is asserted)
7	Beacon use indication. Indicates whether the QCU is being used for beacons; resets to 0x0.	
	0	QCU is being used for non-beacon frames only
	1	QCU is being used for beacon frames (and possibly for non-beacon frames as well)
8	CBR expired counter limit enable; resets to 0x0.	
	0	Maximum CBR expired counter value is 255, but a CBROVF interrupt will be generated when the counter reaches the value set in the CBR overflow threshold field of the Q_CBRCFG register.
	1	The maximum CBR expired counter is limited to the value of the CBR overflow threshold field of the Q_CBRCFG register. Note that in addition to limiting the maximum CBR expired counter to this value, a CBROVF interrupt also will be generated when the CBR expired counter reaches the CBR overflow threshold.

Bit	Description	
9	ReadyTime expiration and VEOL handling policy; resets to 0x0.	
	0	On expiration of ReadyTime or on VEOL, the TXE bit is not cleared. Only reaching the physical end-of-queue (that is, a NULL LinkPtr) will clear TXE.
	1	The TXE bit IS cleared on expiration of ReadyTime, on VEOL, and on reaching the physical end-of-queue.
10	CBR expired counter force-clear control. Write-only (always reads as zero). Write of:	
	0	No effect
	1	Resets the CBR expired counter to zero
11	DCU frame early termination request control; resets to 0x1.	
	0	Never request early frame termination. Once a frame enters the DCU, it will remain active until its normal retry count has been reached or the frame succeeds.
	1	Allow this QCU to request early frame termination. When requested, the DCU will try to complete processing the frame more quickly than it normally would.
31:12	Reserved	

5.3.9 Miscellaneous QCU Status (Q_STS)

Offset: 0x0A00 + (*Q* << 2)[1]
Access: Read-only
Reset: (See field descriptions)

Bit	Description
1:0	Pending frame count. Indicates the number of frames this QCU presently has pending in its associated DCU; resets to 0x0.
7:2	Reserved
15:8	Current value of CBR expired counter; resets to 0x0.
31:16	Reserved

5.3.10 ReadyTimeShutdown Status (Q_RDYTIMESHDN)

Offset: 0x0A40
Access: Read/Write
Reset: (See field descriptions)

Bit	Description	
0	ReadyTimeShutdown status for QCU 0; resets to 0x0. On read, returns ReadyTimeShutdown indication. Write of:	
	0	No effect
	1	Clears the ReadyTimeShutdown status bit
1	ReadyTimeShutdown status for QCU 1; resets to 0x0.	
...	...	
9	ReadyTimeShutdown status for QCU 9; resets to 0x0.	
31:10	Reserved	

5.4 DCU Registers

Table 5-4. **DCU Registers**

Offset	Access	Name	Description	Page
0x1000+ (*D* << 2)[2]	R/W	D_QCUMASK	QCU mask	page 65
0x1080 + (*D* << 2)[2]	R/W	D_RETRY_LIMIT	Retry limits	page 66
0x10C0 + (*D* << 2)[2]	R/W	D_CHNTIME	ChannelTime settings	page 66
0x1100 + (*D* << 2)[2]	R/W	D_MISC	Miscellaneous DCU-specific settings	page 67
0x1030	R/W	D_GBL_IFS_SIFS	DCU-global IFS settings: SIFS duration	page 69
0x1070	R/W	D_GBL_IFS_SLOT	DCU-global IFS settings: slot duration	page 69
0x10B0	R/W	D_GBL_IFS_EIFS	DCU-global IFS settings: EIFS duration	page 69
0x10F0	R/W	D_GBL_IFS_MISC	DCU-global IFS settings: miscellaneous parameters	page 70
0x1230	R/W	D_FPCTL	DCU frame prefetch settings	page 70
0x1270	R/W	D_TXPSE	DCU Tx pause control/status	page 71
0x12F0	R/W	D_TXSLOTMASK	DCU transmission slot mask	page 72
(Varies)	R/W	D_TXBLK	DCU Tx filter bits	page 73

[2]Ten DCUs exist, numbered from 0 to 9. The variable *D* in these register addresses refers to the DCU number.

5.4.1 QCU Mask (D_QCUMASK)

Offset: 0x1000 + (*D* << 2)[2]
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
9:0	QCU mask. Setting bit Q means that QCU Q is associated with (i.e., feeds into) this DCU. These registers have reset values that correspond to a 1-to-1 mapping between QCUs and DCUs. For example 0x1000 will reset to 0x1, 0x1004 maps to 0x2, 0x1008 maps to 0x4, etc.
31:10	Reserved

5.4.2 DCU-Specific IFS Settings (D_LCL_IFS)

Offset: 0x1040 + (*D* << 2)[2]
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
9:0	CW_MIN value. Must be equal to a power of 2, minus 1; resets to 0xF
19:10	CW_MAX value. Must be equal to a power of 2, minus 1; resets to 0x3FF
27:20	AIFS value, in slots beyond SIFS. For example, a setting of 2 (the reset value) indicates AIFS is equal to DIFS; resets to 0x2
31:28	Reserved

5.4.3 Retry Limits (D_RETRY_LIMIT)

Offset: 0x1080 + (*D* << 2)[2]
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
3:0	Frame RTS failure limit. Specifies the number of times a frame's RTS exchange may fail before the current transmission series is terminated. An RTS exchange fails if RTS is enabled for the frame, but when the MAC sends the RTS on the air, no CTS is received; resets to 0x4; a value of 0x0 is unsupported.
7:4	Reserved
13:8	STA RTS failure limit. Specifies the number of times a frame's RTS exchange may fail before the CW is reset to CW_MIN; resets to 0x20. A value of 0x0 is unsupported.
19:14	STA data failure limit. Specifies the number of times a frame's data exchange may fail before CW is reset to CW_MIN; resets to 0x20. A value of 0x0 is unsupported.
31:20	Reserved

5.4.4 ChannelTime Settings (D_CHNTIME)

Offset: 0x10C0 + (*D* << 2)[2]
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description	
19:0	ChannelTime duration in µs; resets to 0x0.	
20	ChannelTime enable	
	0	Disable ChannelTime function
	1	Enable ChannelTime function
31:21	Reserved	

5.4.5 Miscellaneous DCU-Specific Settings (D_MISC)

Offset: 0x1100 + (*D* << 2)[2]
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description	
5:0	Backoff threshold setting. Determines the backoff count at which the DCU initiates arbitration for access to the PCU and commit to sending the frame; resets to 0x2.	
6	End of transmission series STA RTS/data failure count reset policy. This bit controls only whether the two STA failure counts are reset when transitioning from one transmission series to the next within a single frame. The counts are reset per 802.11 specifications when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed); resets to 0x0.	
	0	Do not reset the STA RTS failure count or the STA data failure count at the end of each transmission series.
	1	Reset both the STA RTS failure count and the STA data failure count at the end of each transmission series.
7	End of transmission series CW reset policy. This bit controls only whether the contention window is reset when transitioning from one transmission series to the next within a single frame. The CW is reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed); resets to 0x0.	
	0	Reset the CW to CW_MIN at the end of each intraframe transmission series.
	1	Do not reset the CW at the end of each intraframe transmission series.
8	Fragment burst frame starvation handling policy. This bit controls the DCU operation when the DCU is in the middle of a fragment burst and finds that the QCU sourcing the fragments does not have the next fragment available; resets to 0x0.	
	0	The DCU terminates the fragment burst. When this occurs, the remaining fragments (when the QCU has them available) are sent as a separate fragment burst with a different sequence number.
	1	The DCU waits for the QCU to have the next fragment available. While doing so, all other DCUs are unable to transmit frames.
9	Fragment burst backoff policy. This bit controls whether the DCU performs a backoff after each transmission of a fragment (that is, a frame with the MoreFrag bit set in the frame control field); resets to 0x0.	
	0	The DCU handles fragment bursts normally. No backoff is performed after a successful transmission, and the next fragment is sent at SIFS.
	1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully. In addition, after the backoff count reaches zero, the DCU then follows the normal channel access procedure and sends at AIFS rather than at SIFS. This setting is intended to ease the use of fragment bursts.
11:10	Reserved	
12	Backoff persistence factor setting; resets to 0x1.	
	0	New CW equals old CW
	1	Use binary-exponential CW progression
13	Reserved	

Bit	Description	
15:14	Virtual collision handling policy; resets to 0x0.	
	0	Default handling. A virtual collision is processed like a collision on the air except that the retry count for the frame is not incremented (i.e., just do the backoff)
	1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately re-arbitrates for access to the PCU without doing a backoff and without incrementing the retry count)
	3:2	Reserved
16	Beacon use indication. Indicates whether the DCU is being used for beacons; resets to 0x0.	
	0	DCU is being used for non-beacon frames only
	1	DCU is being used for beacon frames only
18:17	DCU arbiter lockout control; resets to 0x0.	
	0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU
	1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU is either arbitrating for access to the PCU or performing an intra-frame backoff
	2	Global lockout. Forces all lower-priority DCUs to defer arbitrating for access to the PCU whenever: ■ At least one of the QCUs that feed into the current DCU has a frame ready ■ The current DCU is actively processing a frame (i.e., is not idle). This includes arbitrating for access to the PCU, performing an intra-frame or post-frame backoff, DMA'ing frame data to the PCU, or waiting for the PCU to complete the frame.
	3	Reserved
19	DCU arbiter lockout ignore control; resets to 0x0.	
	0	Obey DCU arbiter lockouts from higher-priority DCUs
	1	Ignore DCU arbiter lockouts from higher-priority DCUs (i.e., allow the current DCU to arbitrate for access to the PCU even if one or more higher-priority DCUs is asserting a DCU arbiter lockout)
20	Sequence number increment disable; resets to 0x0.	
	0	Allow the DCU to use a normal sequence number progression (the DCU increments the sequence number for each new frame)
	1	Force the sequence number to be frozen at its current value
21	Post-frame backoff disable; resets to 0x0.	
	0	DCU performs a backoff after each frame finishes, per the 802.11a specification
	1	DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
22	Virtual collision CW increment policy; resets to 0x0.	
	0	Virtual collisions do not increment (advance) the frame's contention window (CW)
	1	Virtual collisions do increment the frame's CW
23	Blown IFS handling policy. This setting controls how the DCU handles a DMA of a frame taking so long that the IFS spacing is met before the frame trigger level is reached; resets to 0x0.	
	0	Send the frame on the air anyway (i.e., ignore the IFS violation), causing the frame to be sent on the air at a time that is later than called for in the 802.11 specification
	1	Do not send the frame on the air. Instead, act as if the frame had been sent on the air but failed and initiate the retry procedure. A retry will be charged against the frame. If more retries are permitted, the frame will be retried. If the retry limit has been reached, the frame will fail.
31:24	Reserved	

5.4.6 DCU-Global IFS Settings: SIFS Duration (D_GBL_IFS_SIFS)

Offset: 0x1030
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
15:0	SIFS duration in core clocks; resets to 640, which is 16 µs at 40 MHz
31:16	Reserved

5.4.7 DCU-Global IFS Settings: Slot Duration (D_GBL_IFS_SLOT)

Offset: 0x1070
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
15:0	Slot duration in core clocks; resets to 360, which is 9 µs at 40 MHz
31:16	Reserved

5.4.8 DCU-Global IFS Settings: EIFS Duration (D_GBL_IFS_EIFS)

Offset: 0x10B0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description
15:0	EIFS duration in core clocks; resets to 3480, which is 87us at 40 MHz
31:16	Reserved

5.4.9 DCU-Global IFS Settings: Miscellaneous Parameters (D_GBL_IFS_MISC)

Offset: 0x10F0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description	
2:0	LFSR slice select. Determines which slice of the internal LFSR is used to generate the random sequence that determines backoff counts in the DCUs and scrambler seeds in the PCU. Thus different STAs have different LFSR slice values to minimize the random sequence correlations among STAs in the same BSS/IBSS; resets to 0x0. **NOTE:** This field affects the MAC only when the random LFSR slice selection disable bit (bit 24) is set. When random LFSR slice selection is enabled (the default), this field is ignored.	
3	Turbo mode indication Software must keep this register consistent with the Turbo/non-Turbo state of the overall system. It must be set or cleared by software to indicate whether the system is in Turbo state; resets to 0x0.	
9:4	Reserved	
19:10	Microsecond duration, in core clocks; resets to 40.	
23:20	Reserved	
24	Random LFSR slice selection disable; resets to 0x0.	
	0	Allow the IFS logic to randomly generate the LFSR slice select value (see bits [2:0] of this register).
	1	Disable random LFSR slice selection. Instead, the value programmed into the LFSR slice select field (bits [2:0] of this register) will be used
26:25	Slot transmission window length.	
27	Force transmission always on slot boundaries. When bits [26:25] of this register are non-zero, the MAC transmits on slot boundaries when the 802.11 spec requires it to do so. When bits [26:25] are not equal to 0x0 and this bit is non-zero, the MAC attempts to transmit on slot boundaries all the time, not just when the specification requires, thus affecting the case in which a frame becomes available when the channel has been idle for an AIFS. If this bit is clear in this case, then the MAC transmits immediately. If this bit is set, then the MAC waits for the next slot boundary before transmitting. Resets to 0x0. **NOTE:** The setting of this bit has no effect unless bits [26:25] are non-zero.	
28	Ignore Back Off. Setting this bit will allow the DCU to ignore any backoff as well as EIFS. Should be set during fast channel change to guarantee low latency to flush the transmit pipe.	
31:29	Reserved	

5.4.10 DCU Frame Prefetch Settings (D_FPCTL)

Offset: 0x1230
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description	
3:0	DCU for which normal (non-burst) frame prefetching should be performed; resets to 0x0	
4	Normal (non-burst) frame prefetch enable; resets to 0x0	
	0	Do not perform non-burst frame prefetches
	1	Perform non-burst frame prefetches when able to do so, but only on behalf of the DCU specified in bits [3:0] of this register.
14:5	Burst frame prefetch enable. Setting bit *D* ($4 \geq D \geq 0$) of this field enables burst frame prefetching for DCU *D*; resets to 0x0, disabling burst frame prefetching for all DCUs.	
31:15	Reserved	

5.4.11 DCU Transmit Pause Control/Status (D_TXPSE)

Offset: 0x1270
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

Bit	Description	
4:0	Request that a subset of the DCUs pause transmission; resets to 0x0. For bit *D* of this field ($4 \geq D \geq 0$):	
	0	Allow DCU *D* to continue to transmit normally
	1	Request that DCU *D* pause transmission as soon as it is able to do so.
15:5	Reserved	
16	Transmit pause status; resets to 0x1.	
	0	Transmit pause request has not yet taken effect, so that some of the DCUs for which a transmission pause request has been issued via bits [4:0] of this register still are transmitting and have not yet paused.
	1	Any DCUs for which a transmission pause request has been issued via bits [4:0] of this register have paused their transmissions. If no transmission pause request is pending (i.e., bits [4:0] of this register are all set to 0), then this transmit pause status bit will be set to one.
31:17	Reserved	

5.4.12 DCU Transmission Slot Mask (D_TXSLOTMASK)

Offset: 0x12F0
Access: Read/Write
Cold reset: (See field descriptions)
Warm reset: (Does not reset on warm reset)

NOTE: If bits [26:25] of "DCU-Global IFS Settings: Miscellaneous Parameters (D_GBL_IFS_MISC)" are non-zero, this register controls which slots the DCUs may start a frame transmission on.

The slot that occurs coincident with SIFS elapsing is slot 0, and slot numbers increase after this point regardless of whether the channel was idle or busy during the slot.

If bits [26:25] of D_GBL_IFS_MISC are zero, then this register has no effect.

Bit	Description	
0	Specifies whether transmission may start on slot numbers that are congruent to 0 (mod 16); resets to 0x0.	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots
1	Specifies whether transmission may start on slot numbers that are congruent to 1 (mod 16); resets to 0x0.	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots
...	...	
15	Specifies whether transmission may start on slot numbers that are congruent to 15 (mod 16); resets to 0x0.	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots
31:16	Reserved	

5.4.13 DCU Transmit Filter Bits (D_TXBLK)

Offset: Varies
Access: Read/Write
Reset: All bits cleared

Each DCU has 128 Tx filter bits, for a total of 10*128=1280 Tx filter bits for all 10 DCUs.

- For reads of the Tx filter bits, the 1280 bits are accessed via reads within a range of 64 32-bit register locations
- For writes of the Tx filter bits, only three of the 64 register locations are used.

  One location allows specific bits of a specific DCU's Tx filter bits to be set or cleared. Two other locations allow all 128 Tx filter bits for any subset of the 10 DCUs to be set or cleared atomically.
- For both reads and writes, the PCI offset issued by the host is mapped to one of the 64 register locations.

  The 6-bit internal address that results from this mapping is called mmr_addr, and its value controls what portion of the Tx filter bits is affected by the host's register read or write. In general, the PCI offset that maps to the internal mmr_addr is given by:

  PCI offset = 0x1038 +
  ((mmr_addr & 0x1F) << 6) +
  ((mmr_addr & 0x20) >> 3)

Table 5-5 shows PCI offsets.

Table 5-5. **PCI Offsets**

mmr_addr	PCI Offset
0	0x1038
1	0x1078
2	0x10B8
3	0x10F8
4	0x1138
5	0x1178
6	0x11B8
7	0x11F8
8	0x1238
9	0x1278
10	0x12B8
11	0x12F8
12	0x1338
13	0x1378
14	0x13B8
15	0x13F8
16	0x1438
17	0x1478

Table 5-5. **PCI Offsets**

mmr_addr	PCI Offset
18	0x14B8
19	0x14F8
20	0x1538
21	0x1578
22	0x15B8
23	0x15F8
24	0x1638
25	0x1678
26	0x16B8
27	0x16F8
28	0x1738
29	0x1778
30	0x17B8
31	0x17F8
32	0x103C
33	0x107C
34	0x10BC
35	0x10FC
36	0x113C
37	0x117C
38	0x11BC
39	0x11FC
...	...
48	0x143C
49	0x147C

MMR Address (mmr_addr) Usage for the Transmit Filter Bits

Writes

Only three register locations (mmr_addr values) are supported for writes. Writes to mmr_addr values other than these yield undefined results and may corrupt the Tx filter bits. Table 5-6 shows write examples.

Table 5-6. **Write Examples**

Write Data	Effect
0x00130404	Clears bits 50 and 58 of DCU 1's Tx filter bits
0x00978001	Clears bits 127 and 112 of DCU 9's Tx filter bits
0x01978001	Sets bits 127 and 112 of DCU 9's Tx filter bits

Table 5-7 describes mmr_addr usage for writes.

Table 5-7. **MMR_ADDR Usage**

mmr_addr	Description		
0	Allows individual bits of a particular DCU's 128 Tx filter bits to be modified. The write data determines which bits are affected and which operation is performed. Table 5-6 shows write examples. Write data is split into several fields:		
	15:0	Bitmask. Controls which bits within the selected bitslice are affected. Bit *N* ($15 \geq N \geq 0$) of the bitmask affects bit *N* of the selected bitslice:	
		0	Bit *N* will be unchanged
		1	Bit *N* of the selected bitslice is modified per the command field (see bits 27:24)
	19:16	Slice number. Selects a 16-bit bitslice from the selected DCU's 128 Tx filter bits to be affected by the write:	
		0	Filter bits [15:0] are affected
		1	Filter bits [31:16] are affected
		...	...
		7	Filter bits [127:112] are affected
		15:8	Reserved
	23:20	DCU number. Determines which DCU's Tx filter bits are affected by the write. Setting this field to a value of D ($9 \geq D \geq 0$) causes DCU D's Tx filter bits to be affected by the write.	
	27:24	Command. Determines what operation will be performed on the selected filter bits:	
		0	Clear the selected bits
		1	Set the selected bits
		15:2	Reserved
	31:28	Reserved	
48	Clears all 128 filter bits for each DCU that has a 1 in bits [9:0] of the write data (e.g., a write of 0x5 to address 48 will cause all 128 filter bits for DCUs 0 and 2 to be cleared)		
49	Sets all 128 filter bits for each DCU that has a 1 in bits [9:0] of the write data (for example, a write of 0x5 to address 49 will cause all 128 filter bits for DCUs 0 and 2 to be set)		

Reads

Table 5-8 describes mmr_addr usage for reads.

mmr_addr	Description
0	Returns filter bits for DCU[0] bits[31:0]
1	Returns filter bits for DCU[0], bits[63:32]
2	Returns filter bits for DCU[0], bits[95:64]
3	Returns filter bits for DCU[0], bits[127:96]
4–7	Returns filter bits for DCU[1], bits[31:0] ... [127:96]
36–39	Returns filter bits for DCU[9], bits[31:0] ... [127:96]
48–49	No effect

5.5 Host Interface Registers

The host occupies a 4 Kb block of address space in the range of 0x04000–0x04FFC. The registers that control the host interface behavior are shown in Table 5-8.

Table 5-8. **Host Interface Registers**

Offset	Access	Name	Description	Page
0x04000	RW	H_RC	Reset the MAC AHB/APB interface	page 76
0x04018	RW	H_TIMEOUT	Host timeout registers	page 76
0x0401C	RW	H_EEPROM_CTRL	EEPROM control	page 76
0x04020	R	H_SREV_ID	MAC silicon revision ID	page 77
0x04028	W	H_INTR_CAUSE_CLR	Interrupt cause clear	page 77
0x0402C	RW	H_INTR_SYNC_ENAB	Synchronous interrupt enable	page 78
0x04030	RW	H_INTR_ASYN_MASK	Asynchronous interrupt mask	page 78
0x04034	RW	H_INTR_SYN_MASK	Synchronous interrupt mask	page 79
0x04038	R	H_INTR_ASYN_CAUS	Asynchronous interrupt cause	page 79
0x0403C	RW	H_INTR_ASYN_ENAB	Asynchronous interrupt enable	page 79
0x04048	RW	H_GPIO_IN_OUT	GPIO input and output	page 79
0x0404C	RW	H_GPIO_OE_BITS	GPIO output enable bits	page 80
0x04050	RW	H_GPIO_IRQ_POLAR	GPIO IRQ polarity	page 80
0x04054	RW	H_GP_INPT_EN_VAL	GPIO input enable and value	page 80
0x04058	RW	H_GP_INPT_MUX1	GPIO input MUX1	page 81
0x0405C	RW	H_GP_INPT_MUX2	GPIO input MUX2	page 81
0x04060	RW	H_GP_OUTPT_MUX1	GPIO output MUX1	page 82
0x04064	RW	H_GP_OUTPT_MUX2	GPIO output MUX2	page 82
0x04068	RW	H_GP_OUTPT_MUX3	GPIO output MUX3	page 83
0x0406C	R	H_INPUT_STATE	Input values	page 83
0x04078	RW	H_CLKRUN	PCI clkrun registers	page 83
0x0407C	R	H_EEP_STS_DATA	EEPROM status and read data	page 84
0x04084	RW	H_RFSILENT	RFSILENT-related registers	page 84
0x04088	RW	H_GPIO_PDPU	GPIO pull-up/pull-down registers	page 84
0x0408C	RW	H_GPIO_DS	GPIO drive strength registers	page 84

5.5.1 Reset the MAC AHB/APB Interface (H_RC)

Offset: 0x04000
Access: Read/Write
Reset Value: 0

Bit	Description	
0	0	Normal operation of the MAC AHB Interface
	1	Hold the MAC AHB Interface in Reset
1	0	Normal operation of the MAC APB Interface
	1	Hold the MAC APB Interface in Reset

5.5.2 Host Power Management State (H_PCIE_PM)

Offset: 0x04008
Reset Value: N/A
Access: Read-only

Bit	Description
14:0	Reserved
16:15	POWER_STATE
17	PME_ENABLE
31:18	Reserved

5.5.3 Host Timeout Registers (H_TIMEOUT)

Offset: 0x04018
Access: Read/Write
Reset Value: 1000_1000h

Bit	Description
15:0	APB Bus timeout counter for register access
31:16	Reserved

5.5.4 EEPROM Control (H_EEPROM_CTRL)

Offset: 0x0401C
Access: Read/Write (bits 7:0)
Read Only (bit 25:8)
Reset Value: 0x0

Bit	Description	
0	0	Normal operation of the APB
	1	Fast mode operation of the APB
1	0	Normal operation of the APB
	1	Hold the APB
7:2	CLKDIV value for the APB	
8	EEPROM is not present	
9	EEPROM is corrupt	
25:10	EEPROM protect mask	

5.5.5 MAC Silicon Revision ID (H_SREV_ID)

Offset: 0x04020
Access: Read-only
Reset Value: N/A

Bit	Description
7:0	MAC silicon revision ID

5.5.6 Interrupt Cause Clear (H_INTR_CAUSE_CLR)

Offset: 0x04028
Access: Write-Only
Reset Value: N/A

Bit	Description
31:0	Writing a 1 to any bit in this register clears the corresponding bit in the register "Synchronous Interrupt (H_INTR_SYNC_CAUS)". See Table 5-9 for bit descriptions.

Table 5-9. **H_INT_CAUSE_CLR Bit Descriptions**

Bit	Name	Description
0	RTC_IRQ	RTC is in shutdown state
1	MAC_IRQ	The MAC has requested an interrupt
2	EEPROM_ILLEGAL_ACCESS	Software attempted to either access a protected area within the EEPROM, or access the EEPROM while it is busy or absent
3	APB_TIMEOUT	No response from an AR5416 module block within the programmed timeout period during a register access
4	PCI_MODE_DBI_ACCESS	Software attempted to access an illegal address
5	HOST1_FATAL	HOST1_FATAL signal from PCI core during a DMA transfer
6	HOST1_PERR	HOST1_PERR signal from PCI core during a DMA transfer
7	TRCV_FIFO_PERR	Indicates a data parity error during a PCI target write cycle. The PCI core asserted TRCV_FIFO_PERR.
12:8	RES	Reserved
13	LOCAL_TIMEOUT	A local bus timeout has occurred
14	PM_ACCESS	The AHB master is requesting a DMA transfer to the core while it is asleep
15	MAC_AWAKE	MAC has become awake
16	MAC_ASLEEP	MAC has gone to sleep
17	MAC_SLEEP_ACCESS	Software is trying to access a register within the MAC while it is asleep
31:18	GPIO_INTR	GPIO interrupts

5.5.7 Synchronous Interrupt (H_INTR_SYNC_CAUS)

Offset: 0x04028
Access: Read-only
Reset Value: N/A

Bit	Description
31:0	Any bit set to 1 in this register indicates that the corresponding interrupt has been triggered in synchronous mode. For any bit to be to set in this register, the corresponding bit in the "Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)" register must also be set. See Table 5-9 for bit descriptions.

5.5.8 Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)

Offset: 0x0402C
Access: Read/Write
Reset Value: 0

Bit	Description
31:0	Any bit set to 1 allows the corresponding interrupt signal to set its corresponding bit in the "Synchronous Interrupt (H_INTR_SYNC_CAUS)" register. See Table 5-9 for bit descriptions.

5.5.9 Asynchronous Interrupt Mask (H_INTR_ASYN_MASK)

Offset: 0x04030
Access: Read/Write
Reset Value: 0

Bit	Description
31:0	Any bit set to 1 allows the corresponding interrupt signal to trigger a PCI interrupt provided that the corresponding "Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)" register bit is set. Note that for the asynchronous interrupt cause register bit to be set, the corresponding "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" register bit must also be set by software. See Table 5-9 for bit descriptions.

5.5.10 Synchronous Interrupt Mask (H_INTR_SYN_MASK)

Offset: 0x04034
Access: Read/Write
Reset Value: 0

Bit	Description
31:0	Any bit set to 1 allows the corresponding interrupt signal to trigger a PCI interrupt provided that the corresponding "Synchronous Interrupt (H_INTR_SYNC_CAUS)" register bit is set. Note that for the interrupt cause register bit to be set, the corresponding "Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)" register bit must also be set by system software. See Table 5-9 for bit descriptions.

5.5.11 Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)

Offset: 0x04038
Access: Read/Write
Reset Value: N/A

Bit	Description
31:0	Any bit set to 1 indicates that the corresponding interrupt has been triggered in asynchronous mode. For any bit to be to set in this register, the corresponding bit in the "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" register must also be set. See Table 5-9 for bit descriptions.

5.5.12 Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)

Offset: 0x0403C
Access: Read/Write
Reset Value: 0

Bit	Description
31:0	Any bit set to 1 in this register allows the corresponding interrupt signal to set its corresponding bit in the "Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)" register. See Table 5-9 for bit descriptions.

5.5.13 GPIO Input and Output (H_GPIO_IN_OUT)

Offset: 0x04048
Access: Read/Write
Reset Value: 0

Bit	Description
13:0	Output value of each GPIO. This value is only used the corresponding GPIO enable bits and GPIO output MUX registers are set correctly. (Read/Write)
27:14	Actual value of each GPIO signal (Read only)

5.5.14 GPIO Output Enable Bits (H_GPIO_OE_BITS)

Offset: 0x0404C
Access: Read/Write
Reset Value: 0

Bit	Description	
2*N*+1:2*N*	Each two-bit field controls the drive mechanism for each GPIO. The mapping for this two-bit field is:	
	0	Never drive output
	1	Drive if the output is low
	2	Drive if the output is high
	3	Always drive output

5.5.15 GPIO IRQ Polarity (H_GPIO_IRQ_POLAR)

Offset: 0x04050
Access: Read/Write
Reset Value: 0

Bit	Description	
13:0	GPIO interrupt polarity	
	0	Corresponding GPIO can interrupt if it is high
	1	Corresponding GPIO can interrupt system if it is low

5.5.16 GPIO Input Enable and Value (H_GP_INPT_EN_VAL)

Offset: 0x04054
Access: Read/Write
Reset Value: 0

Bit	Description	
1:0	Reserved	
2	Default value of BT_PRIORITY input	
3	Default value of BT_FREQUENCY input	
4	Default value of BT_ACTIVE input	
6:5	Reserved	
7	Default value of RFSILENT input to the baseband	
9:8	Reserved	
10	0	Set BT_PRIORITY to default
	1	Connect BT_PRIORITY to a GPIO input
11	0	Set BT_FREQUENCY to default
	1	Connect BT_FREQUENCY to a GPIO input

Bit	Description	
12	0	Set BT_ACTIVE to default
	1	Connect BT_ACTIVE to a GPIO input
14:13	Reserved	
15	0	Set RFSILENT to default
	1	Connect RFSILENT to a GPIO input
16	0	Set RTC Reset controlled entirely by software
	1	RTC Reset controllable through a GPIO pin as well as software

5.5.17 GPIO Input MUX1 (H_GP_INPT_MUX1)

Offset: 0x04058
Access: Read/Write
Reset Value: 0

NOTE: Each 4-bit field corresponds to a particular input and sets the GPIO that connects to it.

Bit	Description
7:0	Reserved
11:8	Input MUX for BT_PRIORITY input
15:12	Input MUX for BT_FREQUENCY input
19:16	Input MUX for BT_ACTIVE input
23:20	Reserved

5.5.18 GPIO Input MUX2 (H_GP_INPT_MUX2)

Offset: 0x0405C
Access: Read/Write
Reset Value: 0

NOTE: Each 4-bit field corresponds to a particular input and sets the GPIO that connects to it.

Bit	Description
3:0	Reserved
7:4	Input MUX for RFSILENT input
11:8	Input MUX for RTC Reset input
23:12	Reserved

5.5.19 GPIO Output MUX1 (H_GP_OUTPT_MUX1)

Offset: 0x04060
Access: Read/Write
Reset Value: 0

NOTE: Each 5-bit field corresponds to a particular GPIO and selects if the output is a fixed value or is connected an output signals Each field is only relevant if the corresponding "GPIO Output Enable Bits (H_GPIO_OE_BITS)" are set appropriately.

Bit	Description
4:0	Output MUX for GPIO 0
9:5	Output MUX for GPIO 1
14:10	Output MUX for GPIO 2
19:15	Output MUX for GPIO 3
24:20	Output MUX for GPIO 4
29:25	Output MUX for GPIO 5

This table describes the mapping of possible output MUX values for each GPIO.

MUX Value	Description
0	Set GPIO output to value set in the GPIO output register
2:1	Reserved
3	Set GPIO to Tx-frame signal
4	Set GPIO to Rx-clear signal
5	Set GPIO to MAC network signal
6	Set GPIO to MAC power LED signal
31:7	Reserved

5.5.20 GPIO Output MUX2 (H_GP_OUTPT_MUX2)

Offset: 0x04064
Access: Read/Write
Reset Value: 0

Bit	Description
4:0	Output MUX for GPIO 6
9:5	Output MUX for GPIO 7
14:10	Output MUX for GPIO 8
19:15	Output MUX for GPIO 9
24:20	Output MUX for GPIO 10
29:25	Output MUX for GPIO 11

5.5.21 GPIO Output MUX3 (H_GP_OUTPT_MUX3)

Offset: 0x04068
Access: Read/Write
Reset Value: 0

Bit	Description
4:0	Output MUX for GPIO12
9:5	Output MUX for GPIO 13

5.5.22 Input Values (H_INPUT_STATE)

Offset: 0x0406C
Access: Read-only
Reset Value: N/A

Bit	Description
3:0	Reserved
3	Status of network LED from MAC
4	Status of power LED from MAC
5	Status of RX_CLEAR from MAC
6	Status of TX_FRAME from MAC

5.5.23 PCI CLKRUN Registers (H_CLKRUN)

Offset: 0x04078
Access: Read/Write
Reset Value: 0

Bit	Description	
0	0	Allow PCI Core to de-assert clkrun and stop the clock
	1	Force the PCI core to assert clkrun and keep running the clock
31:1	clkrun delay parameter	

5.5.24 EEPROM Status and Read Data (H_EEP_STS_DATA)

Offset: 0x0407C
Access: Read/Write
Reset Value: 0

Bit	Description	
15:0	Results of the last EEPROM read transfer	
16	0	EEPROM is idle
	1	EEPROM is busy
17	Indicates that the last software access to the EEPROM occurred when it was busy and was therefore not forwarded to the EEPROM	
18	Indicates that the last software access to the EEPROM occurred to a protected area within the EEPROM and was therefore not forwarded to the EEPROM	
19	Indicates that software attempted to access the EEPROM even though it is not present	

5.5.25 RFSILENT Related (H_RFSILENT)

Offset: 0x04084
Access: Read/Write
Reset Value: 0

Bit	Description	
0	RFSILENT_POLARITY	
	0	Do not invert the RFSILENT signal to the baseband
	1	Invert the RFSILENT signal to the baseband
1	RFSILENT_FORCE signal to the baseband	

5.5.26 GPIO Pull-Up/Pull-Down (H_GPIO_PDPU)

Offset: 0x04088
Access: Read/Write
Reset Value: 0

Bit	Description	
2*N*+1:2*N*	Each two-bit field controls the pull up or pull down of each GPIO. The mapping for this two-bit field is:	
	0	No pull-up or pull down
	1	Pull-down
	2	Pull-up
	3	Pull-up and pull-down

5.5.27 GPIO Drive Strength (H_GPIO_DS)

Offset: 0x0408C
Access: Read/Write
Reset Value: 0

Bit	Description	
2*N*+1:2*N*	Each two-bit field controls the drive strength of each GPIO. The mapping for this two-bit field is:	
	0	Default drive strength = 6 mA
	1	Drive strength = 12 mA
	2	Drive strength = 18 mA
	3	Drive strength = 24 mA

5.6 Host PCI Configuration Space Registers

Table 5-2 summarizes the AR5416 host PCI Configuration Space registers. These registers are accessed by the host using PCI configure operations and are used at boot time by the host to detect the type of card present and to perform low-level configuration, such as assigning base addresses to the card.

At reset, some of these registers are hard coded on the chip but new values can be loaded from an off-chip serial EEPROM, while others must be programmed by the host or are initialized by the AR5416 hardware. Refer to "EEPROM Interface Region" on page 92 for register values that are loaded from the EEPROM upon reset.

Registers that are loaded by the host or initialized by the AR5416 are identified in Table 5-10.

Refer to version 2.3 of the PCI bus standard for detailed information on these registers.

Table 5-10. **Host PCI Configuration Space Registers**

Offset	Name	Description	Initialized By	Page
0x00	Vendor ID	Identification of the manufacturer	EEPROM	page 86
0x02	Device ID	Identification of the device type	EEPROM	page 86
0x04	Command	Controls accessibility of the device	Host	page 86
0x06	Status	Provides status of the device's functionality	AR5416/EEPROM	page 87
0x08	Revision ID	Identification of the device's revision	EEPROM	page 88
0x09	Class Code	Identification of the device's basic function	EEPROM	page 88
0x0C	Cache Line Size	Specifies system cache line size	Host	page 89
0x0D	Latency Timer	Defines the minimum time (in PCI bus cycles) the bus master can retain ownership of the PCI bus	Host	page 89
0x0E	Header Type	Defines device's configuration header format	EEPROM	page 89
0x10	Base Address	Base address for accessing the WLAN memory mapped registers	Host	page 90
0x2C	Subsystem Vendor ID	Identification of the subsystem manufacturer	EEPROM	page 90
0x2E	Subsystem ID	Identification of the subsystem device type	EEPROM	page 90
0x34	Capabilities Pointer	Pointer to the device's list of capabilities	EEPROM	page 91
0x3C	Interrupt Line	Defines if the device's interrupts are generated using the PCI interrupt pins, or using message signaled interrupts (MSI) capability	Host	page 91
0x3D	Interrupt Pin	Defines specific PCI interrupt pins that are associated with particular functions of the device	EEPROM	page 91
0x3E	MinGnt	Indicates how long the device retains the PCI bus ownership	EEPROM	page 92
0x3F	MaxLat	Indicates how often the device accesses the PCI bus	EEPROM	page 92

5.6.1 Vendor ID

Contains the vendor identification number. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0x168C returns when read from the register.

Offset: 0x00
Access: Read Only
Size: 16 bits

Bit	Name	Description
15:0	VENDOR_ID	Vendor identification

5.6.2 Device ID

This register identifies the device type. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0xFF1D returns when read from the register.

Offset: 0x02
Access: Read Only
Size: 16 bits

Bit	Name	Description
15:0	DEVICE_ID	Device identification

5.6.3 Command

This register provides access control of the AR5416 PCI interface. The register is controlled by the host.

Offset: 0x04
Access: Read/Write
Size: 16 bits
Reset Value: Undefined

Bit	Name	Description
0	IO_SPACE	I/O Space
		0 Disable
		1 Enable
1	MEM_SPACE	Memory space
2	BUS_MSTR	Bus master
3	SPEC_CYCLES	Special cycles
4	MEM_WR_INV	Memory write and invalidate enable
5	VGA_SNOOP	VGA palette snoop
6	PAR_ERR_RESP	Parity error response
7	STEP_CNTL	Stepping control
8	SERR_EN	System error enable
9	FAST_BB_EN	Fast back-to-back enable
15:10	RES	Reserved. Must be written with zero. On read, can contain any value.

5.6.4 Status

This register provides status of the functionality provided by the AR5416 PCI interface. This register is mostly controlled by the AR5007AP-NG.

Offset: 0x06
Access: Read/Write, except as noted
Size: 16 bits
Reset Value: 0x0290

Bit	Name	Description	
3:0	RES	Reserved. Must be written with zero. On read, can contain any value.	
4	CAP_LIST	Capabilities list. Read only.	
5	66MHZ_EN	66 MHz capable. Read only.	
6	RES	Reserved. Must be written with zero. On read, can contain any value.	
7	FAST_BB	Fast back-to-back capable. Read-only.	
		0	Disabled
		1	Enabled
8	MD_PAR_ERR	Master data parity error	
		On Read:	
		0	No error
		1	Error
		On Write:	
		0	Do not clear bit
		1	Clear error bit
10:9	DEVSEL_TIMING	Device Select Timing. Read only.	
		01	Medium
11	SIG_TARG_ABORT	Signaled Target Abort	
		On Read:	
		0	No abort
		1	Abort
		On Write:	
		0	Do not clear bit
		1	Clear abort bit
12	RX_TARG_ABORT	Received target abort	
13	RX_MAS_ABORT	Received master abort	
14	SIG_SYS_ERR	Signaled system error	
		On Read:	
		0	No error
		1	Error
		On Write:	
		0	Do not clear bit
		1	Clear error bit
15	DETECT_PAR_ERR	Detected parity error	

5.6.5 Revision ID

This register contains the device revision identification number. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0x1 returns when read from the register.

Offset: 0x08
Access: Read/Write
Size: 8 bits

Bit	Name	Description
7:0	REVISION_ID	Revision identification

5.6.6 Class Code

This register contains the class code identification number that identifies the basic function of the device. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0x0D8000 returns when read from the register.

Offset: 0x09
Access: Read only
Size: 24 bits

Bit	Name	Description
23:0	CLASS_CODE	Class code identification value

5.6.7 Cache Line Size

This register contains the size of the system cache line. This register is controlled by the host.

Offset: 0x0C
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	CACHE_SZ	Cache line size, in units of 32-bit words (4 bytes)

5.6.8 Latency Timer

This register provides the minimum amount of time, in PCI clock cycles, that the bus master can retain ownership of the bus whenever it initiates a new transaction. This register is controlled by the host.

Offset: 0x0D
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	LATENCY_TMR	Latency timer

5.6.9 Header Type

This register contains the header type information. Value can be loaded from the EEPROM.

Offset: 0x0E
Access: Read Only
Size: 8 bits

Bit	Name	Description	
7:0	HDR_TYPE	Header type	
		0	Nonbridge PCI device

5.6.10 Base Address

This register contains the base address for accessing the AR5007AP-NG WLAN memory mapped registers. This register is controlled by the host.

Offset: 0x10
Access: Bits [15:0] are Read Only (always return 0)
Bits [31:16} are Read/Write
Size: 32 bits
Reset Value: Undefined

Bit	Name	Description
31:0	BASE_ADDR	Base address

5.6.11 Subsystem Vendor ID

This register contains the subsystem vendor identification number. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0x168C returns when read from the register.

Offset: 0x2C
Access: Read Only
Size: 16 bits

Bit	Name	Description
15:0	SSYS_VEND_ID	Subsystem vendor ID

5.6.12 Subsystem ID

This register contains the subsystem device identification number. Value of this register can be loaded from the EEPROM when the EEPROM is attached, or if the EEPROM content is not valid, a value of 0xEE1C returns when read from the register.

Offset: 0x2E
Access: Read Only
Size: 16 bits

Bit	Name	Description
15:0	SSYS_ID	Subsystem ID

5.6.13 Capabilities Pointer (CAP_PTR)

This register contains the value of the capabilities pointer. Default value is provided by the AR5007AP-NG.

Offset: 0x34
Access: Read Only
Size: 8 bits
Reset Value: 0x40

Bit	Name	Description
7:0	CAP_PTR	Capabilities pointer value

5.6.14 Interrupt Line (INT_LINE)

This register contains the host interrupt controller's interrupt line value that the device's interrupt pin is connected to. This register is controlled by the host.

Offset: 0x3C
Access: Read/Write
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	INT_LINE	Interrupt line value

5.6.15 Interrupt Pin (INT_PIN)

This register defines which of the four PCI interrupt request pins, a PCI function is connected to. Value can be loaded from the EEPROM.

Offset: 0x3D
Access: Read only
Size: 8 bits
Reset Value: 0x01

Bit	Name	Description
7:0	INT_PIN	Interrupt pin value

5.6.16 MinGnt

This register contains a value that indicates how long the device (bus-master) retains PCI bus ownership. Value can be loaded from the EEPROM.

Offset: 0x3E
Access: Read only
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	MIN_GNT	Minimum grant value

5.6.17 MaxLat

This register contains the maximum latency value. Value can be loaded from the EEPROM.

Offset: 0x3F
Access: Read only
Size: 8 bits
Reset Value: 0x00

Bit	Name	Description
7:0	MAX_LAT	Maximum latency value

5.7 EEPROM Interface Region

The EEPROM interface region (0x02000 – 0x03FFC) accesses the external EEPROM. Upon power reset, a state machine inside the host interface reads the EEPROM and writes registers within the AR5416.

Each EEPROM location is 16 bits wide. The first location must contain the 16-bit word A55A, indicating that the EEPROM is valid. If the first location is not this value, the state machine assumes that the EEPROM contents have been corrupted. The state machine immediately stops running in this case.

The next EEPROM location contains the mask word. Location (2) contains an address pointer to the next valid data segment. Each data segment consists of three locations: a 16-bit address location and two locations for the 32-bit write data. The state machine reads each data segment and then writes to the corresponding register. The state machine stops when it comes across an address equal to 0x0FFFF.

5.7.1 EEPROM PCI Configuration Interface Registers

This region maps to the PCI core configuration registers accessible by the EEPROM using the memory space. The locations and bit-fields of most of these registers match with the PCI specification.

Address	Name	Description	Page
0x06000	VENDOR_DEVICE	Vendor ID and Device ID	page 93
0x06004	STATUS_4_5	Bits 4 and 5 of the status register (capability 66 MHz)	page 93
0x06008	REV_CLASS	Revision ID and class code	page 93
0x0600C	HEADER	Header type	page 93
0x0602C	SUBSYS_VENDOR_DEVICE	Subsystem vendor ID and device ID	page 94
0x06034	CAP_PTR	Capabilities pointer	page 94
0x0603C	LAT_GNT_PIN	Maximum latency, minimum grant, and interrupt pin	page 94

5.7.2 Vendor ID and Device ID (VENDOR_DEVICE)

Offset: 0x06000
Default Values:
Vendor ID = 0x0168C
Device ID = 0x0FF1C

Bit	Description
15:0	Vendor ID
31:16	Device ID

5.7.3 Status Register, Bits 4 and 5 (STATUS_4_5)

Offset: 0x06004
Default Value: 3

Bit	Description	
16	Bit 4 of the Status register	
	0	No additional capabilities
	1	Additional capabilities
17	Bit 5 of the Status register	
	0	No 66 MHz capable
	1	66 MHz capable

5.7.4 Revision ID and Class Code (REV_CLASS)

Offset: 0x06008
Default Value:
Class Code = 0x0D8000
Rev ID = 0x06001

Bit	Description
7:0	Revision ID
31:8	Class code

5.7.5 Header Type (HEADER)

Offset: 0x0600C
Default Value: 0

Bit	Description
23:16	Header

5.7.6 Subsystem Vendor ID and Device ID (SUBSYS_VENDOR_DEVICE)

Offset: 0x0602C
Default Value:
Subsystem Vendor ID = 0x0168C
Subsystem Device ID = 0x0EE1C

Bit	Description
15:0	Subsystem vendor ID
31:16	Subsystem device ID

5.7.7 Capabilities Pointer (CAP_PTR)

Offset: 0x06034
Default Value: 0x06040

Bit	Description
7:0	Capabilities pointer

5.7.8 Maximum Latency, Minimum Grant, and Interrupt Pin (LAT_GNT_PIN)

Offset: 0x0603C
Default Value:
Max Latency = 0
Min Grant = 0
Interrupt Pin = 1

Bit	Description
15:8	Interrupt pin
23:16	Min grant
31:24	Max latency

5.8 RTC Interface Registers

The RTC occupies offset range 0x07000 – 0x07FFC in the address space. Within this 4 Kb range the address range 0x00040 – 0x0005C range consists of always on registers available for software access regardless of whether the RTC is asleep.

Table 5-11 shows the mapping of these registers.

Table 5-11. **RTC Interface Registers**

Address	Access	Name	Description	Page
0x07040	RW	RTC_RESET	RTC reset and force sleep and force wakeup	page 95
0x07044	R	RTC_STATUS	RTC sleep status	page 95
0x07048	RW	RTC_DERIVED	RTC force derived RTC and bypass derived RTC	page 96
0x0704C	R	RTC_FORCE_WAKE	RTC force wake	page 96
0x07050	R	RTC_INT_CAUSE	RTC interrupt cause	page 96
0x07050	W	RTC_CAUSE_CLR	RTC interrupt cause clear	page 96
0x07054	RW	RTC_INT_ENABLE	RTC interrupt enable	page 97
0x07058	RW	RTC_INT_MASK	RTC interrupt mask	page 97

5.8.1 RTC Reset and Force Sleep and Force Wakeup (RTC_RESET)

Offset: 0x07040
Access: Read/Write
Default Value: 0

Bit	Description
0	RTC reset (active low)

5.8.2 RTC Sleep Status (RTC_STATUS)

Offset: 0x07044
Access: Read-only
Default Value: 0

Bit	Description
0	RTC in SHUTDOWN state
1	RTC in ON state
2	RTC in SLEEP state
3	RTC in WAKEUP state
4	RTC in cold reset (active high)
5	PLL changing signal from RTC

5.8.3 RTC Force Derived RTC and Bypass Derived RTC (RTC_DERIVED)

Offset: 0x07048
Access: Read/Write
Default Value: 0

Bit	Description
0	Bypass derived RTC
1	Force derived RTC

5.8.4 RTC FORCE WAKE (RTC_FORCE_WAKE)

Offset: 0x0704C
Access: Read/Write
Default Value: 3

Bit		Description
0	FORCE_WAKE signal to the MAC	
1	0	Do not assert FORCE_WAKE on MAC interrupt
	1	Assert FORCE_WAKE on MAC interrupt

5.8.5 RTC Interrupt Cause (RTC_INT_CAUSE)

Offset: 0x07050
Access: Read-only
Default Value: 0

Bit	Description
0	RTC in SHUTDOWN state
1	RTC in ON state
2	RTC in SLEEP state
3	RTC in WAKEUP state
4	Software access of an RTC register when it is not in the ON state
5	PLL changing

5.8.6 RTC Interrupt Cause Clear (RTC_CAUSE_CLR)

Offset: 0x07050
Access: Write-only
Default Value: 0

Bit	Description
5:0	A write of 1 to any bit in this register clears that bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" register until the corresponding event occurs again

5.8.7 RTC Interrupt Enable (RTC_INT_ENABLE)

Offset: 0x07054
Access: Read/Write
Default Value: 0

Bit	Description	
5:0	0	Writing a 0 to any bit in this register automatically clears the corresponding bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" register regardless of the corresponding event
	1	Writing a 1 to any bit in this register allows that bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" register to be set when the corresponding event occurs.

5.8.8 RTC Interrupt Mask (RTC_INT_MASK)

Offset: 0x07058
Access: Read/Write
Default Value: 0

Bit	Description
5:0	Writing a 1 to any bit in this register allows the corresponding event to generate an RTC interrupt to the host interface, which can in-turn be programmed to generate a system interrupt. The corresponding bit in the "RTC Interrupt Enable (RTC_INT_ENABLE)" register must also be set.

5.9 MAC Interface Registers

The MAC DMA occupies offset range 0x00000 – 0x01FFC in the address space. Within this 8-Kb range the address range 0x01F00 – 0x1FFFC consists of always on registers available for software access regardless of whether the MAC is asleep.

Table 5-12 shows the mapping of these registers.

Table 5-12. **MAC Interface Registers**

Address	Access	Name	Description	Page
0x01F00	R	MAC_SLEEP	MAC sleep status	page 98
0x01F04	R/W	MAC_LED	MAC LED control	page 98

5.9.1 MAC Sleep Status (MAC_SLEEP)

Offset: 0x01F00
Access: Read-only
Default Value: N/A

Bit	Description	
0	0	MAC is awake
	1	MAC is asleep

5.9.2 MAC LED Control (MAC_LED)

Offset: 0x01F04
Access: Read-only
Default Value: 0

Bit	Description
1:0	Sleep clock rate
2	LED hysteresis disable
3	LED slowest blink rate mode
6:4	LED blink threshold select
9:7	LED mode select
10	Association active
11	Association pending

5.10 MAC PCU Registers

Table 5-13 shows the mapping of these registers.

Table 5-13. **MAC PCU Registers**

Address	Name	Description	Page
0x08000	MAC_PCU_STA_ADDR_L32	STA address lower 32 bits	page 102
0x08004	MAC_PCU_STA_ADDR_U16	STA address upper 16 bits	page 102
0x08008	MAC_PCU_BSSID_L32	BSSID lower 32 bits	page 103
0x0800C	MAC_PCU_BSSID_U16	BSSID upper 16 bits	page 103
0x08010	MAC_PCU_BCN_RSSI_AVE	Beacon RSSI average	page 103
0x08014	MAC_PCU_ACK_CTS_TIMEOUT	ACK and CTS timeout	page 104
0x08018	MAC_PCU_BCN_RSSI_CTL	Beacon RSSI control	page 104
0x0801C	MAC_PCU_USEC_LATENCY	Millisecond counter and Rx/Tx latency	page 104
0x08020	MAC_PCU_RESET_TSF	Reset TSF	page 104
0x08038	MAC_PCU_MAX_CFP_DUR	Maximum CFP duration	page 105
0x0803C	MAC_PCU_RX_FILTER	Rx filter	page 105
0x08040	MAC_PCU_MCAST_FILTER_L32	Multicast filter mask lower 32 bits	page 105
0x08044	MAC_PCU_MCAST_FILTER_U32	Multicast filter mask upper 32 bits	page 106
0x08048	MAC_PCU_DIAG_SW	Diagnostic switches	page 106
0x0804C	MAC_PCU_TSF_L32	TSF lower 32 bits	page 107
0x08050	MAC_PCU_TSF_U32	TSF upper 32 bits	page 107
0x08058	MAC_PCU_DEF_ANTENNA	Default antenna	page 108
0x0805C	MAC_PCU_AES_MUTE_MASK_0	AES mute mask 0	page 108
0x08060	MAC_PCU_AES_MUTE_MASK_1	AES mute mask 1	page 108
0x08080	MAC_PCU_LAST_BEACON_TSF	Last receive beacon TSF	page 108
0x08084	MAC_PCU_NAV	Current NAV	page 109
0x08088	MAC_PCU_RTS_SUCCESS_CNT	Successful RTS count	page 109
0x0808C	MAC_PCU_RTS_FAIL_CNT	Failed RTS count	page 109
0x08090	MAC_PCU_ACK_FAIL_CNT	FAIL ACK count	page 109
0x08094	MAC_PCU_FCS_FAIL_CNT	Failed FCS count	page 110
0x08098	MAC_PCU_BEACON_CNT	Beacon count	page 110
0x080D4	MAC_PCU_SLP1	Sleep 1	page 110
0x080D8	MAC_PCU_SLP2	Sleep 2	page 111
0x080E0	MAC_PCU_ADDR1_MASK_L32	Address 1 mask lower 32 bits	page 111
0x080E4	MAC_PCU_ADDR1_MASK_U16	Address 1 mask upper 16 bits	page 111
0x080E8	MAC_PCU_TPC	Tx power control	page 112
0x080EC	MAC_PCU_TX_FRAME_CNT	Tx frame counter	page 112
0x080F0	MAC_PCU_RX_FRAME_CNT	Rx frame counter	page 112
0x080F4	MAC_PCU_RX_CLEAR_CNT	Rx clear counter	page 113
0x080F8	MAC_PCU_CYCLE_CNT	Cycle counter	page 113
0x080FC	MAC_PCU_QUIET_TIME_1	Quiet time 1	page 113
0x08100	MAC_PCU_QUIET_TIME_2	Quiet time 2	page 114
0x08108	MAC_PCU_QOS_NO_ACK	QoS no ACK	page 114

Table 5-13. **MAC PCU Registers**

Address	Name	Description	Page
0x0810C	MAC_PCU_PHY_ERROR_MASK	PHY error mask	page 115
0x08114	MAC_PCU_RXBUF_THRESHOLD	Rx buffer threshold	page 115
0x08118	MAC_PCU_MIC_QOS_CONTROL	QoS control	page 116
0x0811C	MAC_PCU_MIC_QOS_SELECT	Michael QoS select	page 116
0x08120	MAC_PCU_MISC_MODE	Miscellaneous mode	page 117
0x08124	MAC_PCU_FILTER_OFDM_CNT	Filtered OFDM counter	page 118
0x08128	MAC_PCU_FILTER_CCK_CNT	Filtered CCK counter	page 119
0x0812C	MAC_PCU_PHY_ERR_CNT_1	PHY error counter 1	page 119
0x08130	MAC_PCU_PHY_ERR_CNT_1_MASK	PHY error counter 1 mask	page 120
0x08134	MAC_PCU_PHY_ERR_CNT_2	PHY error counter 2	page 120
0x08138	MAC_PCU_PHY_ERR_CNT_2_MASK	PHY error counter 2 mask	page 121
0x0813C	MAC_PCU_TSF_THRESHOLD	TSF threshold	page 121
0x08144	MAC_PCU_PHY_ERROR_EIFS_MASK	PHY error EIFS mask	page 121
0x08168	MAC_PCU_PHY_ERR_CNT_3	PHY error counter 3	page 122
0x0816C	MAC_PCU_PHY_ERR_CNT_3_MASK	PHY error counter 3 mask	page 122
0x08170	MAC_PCU_BLUETOOTH_MODE	Bluetooth mode	page 123
0x08174	MAC_PCU_BLUETOOTH_WEIGHTS	Bluetooth weight	page 124
0x08178	MAC_PCU_HCF_TIMEOUT	HCF timeout	page 125
0x0817C	MAC_PCU_BLUETOOTH_MODE2	Bluetooth mode 2	page 125
0x081D0	MAC_PCU_TXSIFS	SIFS, Tx latency and ACK shift	page 126
0x081EC	MAC_PCU_TXOP_X	TXOP for non-QoS frames	page 126
0x081F0	MAC_PCU_TXOP_0_3	TXOP for TID 0 to 3	page 126
0x081F4	MAC_PCU_TXOP_4_7	TXOP for TID 4 to 7	page 127
0x081F8	MAC_PCU_TXOP_8_11	TXOP for TID 8 to 11	page 127
0x081FC	MAC_PCU_TXOP_12_15	TXOP for TID 0 to 3	page 127
0x08200	MAC_PCU_GENERIC_TIMERS[0:15]	Generic timers	page 128
0x08240	MAC_PCU_GENERIC_TIMERS_MODE	Generic timers mode	page 128
0x08244	MAC_PCU_SLP32_MODE	32 KHz sleep mode	page 128
0x08248	MAC_PCU_SLP32_WAKE	32 KHz sleep wake	page 129
0x0824C	MAC_PCU_SLP32_INC	32 KHz sleep increment	page 129
0x08250	MAC_PCU_SLP_MIB1	Sleep MIB sleep count	page 129
0x08254	MAC_PCU_SLP_MIB2	Sleep MIB cycle count	page 130
0x08258	MAC_PCU_SLP_MIB3	Sleep MIB control status	page 130
0x0825C	MAC_PCU_WOW1	MAC PCU wake on wireless (WoW) 1	page 130
0x08260	MAC_PCU_WOW2	MAC PCU WoW 2	page 131
0x08270	MAC_PCU_WOW3_BEACON_FAIL	WoW 3 beacon fail	page 131
0x08274	MAC_PCU_WOW3_BEACON	WoW 3 beacon timeout	page 131
0x08278	MAC_PCU_WOW3_BEACON_KEEP_ALIVE	WoW 3 keep-alive timeout	page 131
0x087C	MAC_PCU_WOW_KA	MAC PCU WoW keep-alive disable bit	page 132
0x08284	PCU_1US	Number of clocks in one microsecond	page 132
0x08288	PCU_KA	Delay between WoW keep-alive	page 132

Table 5-13. **MAC PCU Registers**

Address	Name	Description	Page
0x0828C	WOW_EXACT	Exact length and offset equipment flag for WoW patterns	page 132
0x08294	PCU_WOW4	WoW offset register 1	page 133
0x08298	PCU_WOW5	WoW offset register 2	page 133
0x08318	MAC_PCU_20_40_MODE	Global mode register	page 133
0x08328	MAC_PCU_RX_CLEAR_DIFF_CNT	Difference Rx_Clear counter	page 133
0x0832C	MAC_PCU_SELF_GEN_ANTENNA_MASK	Antenna mask for self-generated files	page 134
0x08330	MAC_PCU_BA_BAR_CONTROL	Control registers for block BA control fields	page 134
0x08334	MAC_PCU_LEGACY_PLCP_SPOOF	Legacy PLCP spoof	page 134
0x08338	MAC_PCU_PHY_ERROR_MASK_CONT	PHY error mask and EIFS mask	page 135
0x0833C	MAC_PCU_TX_TIMER	Tx timer	page 135
0x08800	MAC_PCU_KEY_CACHE[0:1023]	Key cache lower half	page 136

5.10.1 STA Address Lower 32 Bits (MAC_PCU_STA_ADDR_L32)

This register contains the lower 32 bits of the STA address.

Offset: 0x08000
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	ADDR_31_0	Lower 32 bits of STA MAC address (PCU_STA_ADDR[31:0])

5.10.2 STA Address Upper 16 Bits (MAC_PCU_STA_ADDR_U16)

This register contains the lower 32 bits of the STA address.

Offset: 0x08004
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
15:0	PCU_STA_ADDR[47:32]	Upper 16 bits of station MAC address
16	PCU_AP	Set if STA is an AP
17	PCU_ADHOC	Set if STA is in an ad hoc network
18	PCU_PSMODE	Set if STA is in power-save mode
19	PCU_NO_KEYSEARCH	Disable key search
20	PCU_PCF	Set if associated AP is PCF capable
21	PCU_USE_DEFANT	When a descriptor chosen in auto-select mode (0000), use default antenna to transmit
22	PCU_DEFANT_TX	Update default antenna with Tx antenna
23	PCU_DEFANT_RTS	Use default antenna to send RTS
24	PCU_ACKCTS_6MB	Use 6 Mbps rate for ACK and CTS
25	PCU_BSRATE_11B	802.11b base rate 0 Use all rates 1 Use only 1–2 Mbps
26	REG_SECTOR_SELF_GEN	Use default antenna for self generated frames
27	REG_CRPT_MIC_ENABLE	Enables the checking and insertion of MIC in TKIP
28	PCU_KSRCH_MODE	Search key cache first. If not, match use offset for IV = 0, 1, 2, 3. ■ If KSRCH_MODE = 0 then do not search ■ If IV = 1, 2, or 3, then search ■ If IV = 0, do not search
29	REG_PRESERVE_SEQNUM	Stops PCU from replacing the sequence number
30	PCU_CBCIV_ENDIAN	Endianess of IV in CBC nonce
31	REG_ADHOC_MCAST_SEARCH	Enables the key cache search for ad hoc MCAST packets

5.10.3 BSSID Lower 32 Bits (MAC_PCU_BSSID_L32)

This register contains the lower 32 bits of the BSS identification information.

Offset: 0x08008
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_BSSID[31:0]	Lower 32 bits of BSSID

5.10.4 BSSID Upper 16 Bits (MAC_PCU_BSSID_U16)

This register contains the upper 32 bits of the BSS identification information.

Offset: 0x0800C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
15:0	PCU_BSSID[47:32]	Upper 16 bits of BSSID
26:16	PCU_AID	Association ID

5.10.5 Beacon RSSI Average (MAC_PCU_BCN_RSSI_AVE)

Offset: 0x08010
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x800

Bit	Name	Description
11:0	REG_BCN_RSSI_AVE	Holds the average RSSI with 1/16 dB resolution. The RSSI is averaged over multiple beacons which matched our BSSID. AVE_VALUE is 12 bits with 4 bits below the normal 8 bits. These lowest 4 bits provide for a resolution of 1/16 dB. The averaging function is depends on the BCN_RSSI_WEIGHT; determines the ratio of weight given to the current RSSI value compared to the average accumulated value.

5.10.6 ACK and CTS Timeout (MAC_PCU_ACK_CTS_TIMEOUT)

Offset: 0x08014
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
13:0	PCU_ACK_TIMEOUT	Timeout while waiting for ACK
29:16	PCU_CTS_TIMEOUT	Timeout while waiting for CTS

5.10.7 Beacon RSSI Control (MAC_PCU_BCN_RSSI_CTL)

Offset: 0x08018
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	PCU_RSSI_THR	The threshold at which the beacon low RSSI interrupt is asserted when the average RSSI ("BCN_RSSI_AVE") below this level
15:8	PCU_BCN_MISS_THR	Threshold at which the beacon miss interrupt asserts. Because the beacon miss counter increments at TBTT, it increments to 1 before the first beacon.
28:24	REG_BCN_RSSI_WEIGHT	Used to calculate "BCN_RSSI_AVE"
29	REG_BCN_RSSI_RST_ STROBE	The BCN_RSSI_RESET clears "BCN_RSSI_AVE" to aid in changing channels

5.10.8 Millisecond Counter and Rx/Tx Latency (MAC_PCU_USEC_LATENCY)

Offset: 0x0801C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
6:0	PCU_1US_SCALER	clk cycle in 1 µs
22:14	PCU_TXDELAY	Baseband Tx latency to start of timestamp in µs
28:23	PCU_RXDELAY	Baseband Rx latency to start of SIGNAL in µs

5.10.9 Reset TSF (MAC_PCU_RESET_TSF)

Controls beacon operation by the PCU.

Offset: 0x08020
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	RES	Reserved
24	ONE_SHOT	Setting this bit causes the TSF to reset. This register clears immediately after being reset.
31:25	RES	Reserved

5.10.10 Maximum CFP Duration (MAC_PCU_MAX_CFP_DUR)

Contains the maximum time for a CFP.

Offset: 0x08038
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
15:0	PCU_MAX_CFPDUR	Maximum contention free period duration in µs
31:16	RES	Reserved.

5.10.11Rx Filter (MAC_PCU_RX_FILTER)

This register determines Rx frame filtering.
Offset: 0x0803C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

NOTE: If any bit is set, the corresponding packet types pass the filter and are DMAed. All filter conditions except the promiscuous setting rely on the no early PHY error and protocol version being checked to ensure it is version 0.

Bit	Name	Description	
0	UNICAST	Unicast frame Enable. Enable reception of unicast (directed) frames that match the STA address.	
		0	Disable. No ACK will return.
		1	Enable
1	MULTICAST	Multicast frame Enable. Enable reception of multicast frames that match the multicast filter.	
2	BROADCAST	Broadcast frame Enable. Enable reception of non beacon broadcast frames that originate from the BSS whose ID matches BSSID.	
3	CONTROL	Control frame Enable. Enable reception of control frames.	
4	BEACON	Beacon frame Enable. Enable reception of beacon frames.	
5	PROMISCUOUS	Promiscuous Receive Enable. Enable reception of all frames, including errors.	
6	RES	Reserved.	
7	PROBE_REQ	Probe request enable. Enables reception of all probe request frames.	
8	RES	Reserved.	
9	MY_BEACON	Retrieves any beacon frame with matching SSID.	
31:10	RES	Reserved.	

5.10.12Multicast Filter Mask Lower 32 Bits (MAC_PCU_MCAST_FILTER_L32)

This register contains the lower 32 bits of the multicast filter mask.

Offset: 0x08040
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask low. Lower 32 bits of multicast filter mask.

5.10.13Multicast Filter Mask Upper 32 Bits (MAC_PCU_MCAST_FILTER_U32)

This register contains the upper 32 bits of the multicast filter mask.

Offset: 0x08044
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask high. Upper 32 bits of multicast filter mask.

5.10.14 Diagnostic Switches (MAC_PCU_DIAG_SW)

Controls the operation of the PCU, including enabling/disabling acknowledgements, CTS, transmission, reception, encryption, loopback, FCS, channel information, and scrambler seeds.

Offset: 0x08048
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
0	PCU_INVALKEY_NOACK	Enable or disable acknowledgement when a valid key is not found for the received frames in the key cache.
1	NO_ACK	Enable or disable acknowledgement generation for all frames
2	NO_CTS	Enable or disable CTS generation
3	NO_ENCRYPT	Enable or disable encryption
4	NO_DECRYPT	Enable or disable decryption
5	HALT_RX	Enable or disable reception
6	LOOP_BACK	Enable or disable Tx data loopback
7	CORRUPT_FCS	Enable or disable corrupt FCS. Enabling this bit causes an invalid FCS to be appended to a frame during transmission.
8	DUMP_CHAN_INFO	Enable or disable channel information. Enabling this bit stores 56 bytes of channel information in the Rx buffer before frame data is stored.
16:9	RES	Reserved
17	ACCEPT_NON_V0	Enable or disable protocol field
19:18	RES	Reserved
20	RX_CLEAR_HIGH	Force RX_CLEAR high
21	IGNORE_NAV	Ignore virtual carrier sense (NAV)
22	CHAN_IDLE_HIGH	Force channel idle high
23	PHYERR_ENABLE_EIFS_CTL	Uses framed and wait_wep in the pcu_rx_err logic if bits is set to 0
24	DUAL_CHAIN_CHAN_INFO	Dual chain channel info (extra 62 bytes)
25	FORCE_RX_ABORT	Force Rx abort bit in conjunction with Rx block aids quick channel change to shut down Rx. The force Rx abort bit kills with the Rx_abort any frame currently transferring between the MAC and baseband. while the RX block bit prevents any new frames from getting started.
26	SATURATE_CYCLE_CNT	The saturate cycle count bit, if set, causes the "Cycle Counter (MAC_PCU_CYCLE_CNT)" register to saturate instead of shifting to the right by 1 every time the count reaches 0xFFFFFFFF. This saturate condition also holds the rx_clear, rx_frame, and tx_frame counts.
27	RES	Reserved
28	RX_CLEAR_CTL_LOW	Force the RX_CLEAR_CTL signal to appear to the MAC as being low
29	RX_CLEAR_EXT_LOW	Force the RX_CLEAR_EXT signal to appear to the MAC as being low
31:30	RES	Reserved

5.10.15TSF Lower 32 Bits (MAC_PCU_TSF_L32)

Offset: 0x0804C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs. Writes to this register do not cause the TSF to change. Rather, the value is held in a temporary staging area until this register is written, at which point both the lower and upper parts of the TSF are loaded. A read result of 0xFFFFFFFF indicates that the read occurred before TSF logic came out of sleep. It may take up to 45 µs after the chip is brought out of sleep for the TSF logic to wake.

5.10.16TSF Upper 32 Bits (MAC_PCU_TSF_U32)

Offset: 0x08050
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs

5.10.17Default Antenna (MAC_PCU_DEF_ANTENNA)

Offset: 0x08058
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	DEFANT	Anytime transmit is about to start, the 24 bits of transmit antenna of the selected series in the Tx descriptor is sent serially to the serial GPIO interface. When no active transmit is in progress and the Rx_Clear is high, the default antenna register value is serially sent to the GPIO interface.
31:24	RES	Reserved

5.10.18AES Mute Mask 0 (MAC_PCU_AES_MUTE_MASK_0)

Offset: 0x0805C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0xC7FF

Bit	Name	Description
15:0	FC_MUTEMASK	AES mute mask for frame control field
31:16	QOS_MUTEMASK	AES mute mask for TID field

5.10.19AES Mute Mask 1 (MAC_PCU_AES_MUTE_MASK_1)

Offset: 0x08060
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x000F

Bit	Name	Description
15:0	SEQ_MUTEMASK	AES mute mask for sequence number field

5.10.20Last Rx Beacon TSF (MAC_PCU_LAST_BEACON_TSF)

This threshold register indicates the minimum amount of data required before initiating a transmission.

Offset: 0x08080
Access: Hardware = Write-only
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
31:0	LAST_TSTP	Beacon timestamp. Lower 32 bits of timestamp of the last beacon received.

5.10.21Current NAV (MAC_PCU_NAV)

Offset: 0x08084
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
25:0	CS_NAV	Current NAV value in µs
31:26	RES	Reserved.

5.10.22Successful RTS Count (MAC_PCU_RTS_SUCCESS_CNT)

This register counts the number of successful RTS exchanges. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Offset: 0x08088
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
15:0	RTS_OK	RTS/CTS exchange success counter
31:16	RES	Reserved

5.10.23Failed RTS Count (MAC_PCU_RTS_FAIL_CNT)

This register counts the number of failed RTS exchanges. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Offset: 0x0808C
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
15:0	RTS_FAIL	RTS/CTS exchange failure counter
31:16	RES	Reserved

5.10.24FAIL ACK Count (MAC_PCU_ACK_FAIL_CNT)

This register counts the number of failed acknowledgements. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Offset: 0x08090
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
15:0	ACK_FAIL	DATA/ACK failure counter
31:16	RES	Reserved

5.10.25Failed FCS Count (MAC_PCU_FCS_FAIL_CNT)

This register counts the number of failed frame check sequences. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Offset: 0x08094
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
15:0	FCS_FAIL	FCS failure counter
31:16	RES	Reserved

5.10.26Beacon Count (MAC_PCU_BEACON_CNT)

This register counts the number of valid beacon frames received. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Offset: 0x08098
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
15:0	BEACONCNT	Valid beacon counter
31:16	RES	Reserved

5.10.27Sleep 1 (MAC_PCU_SLP1)

The Sleep 1 register in conjunction with the "Sleep 2 (MAC_PCU_SLP2)" register, controls when the AR5007AP-NG should wake when waiting for AP Rx traffic. Sleep registers are only used when the AR5007AP-NG is in STA mode.

Offset: 0x080D4
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
18:0	RES	Reserved
19	ASSUME_DTIM	A mode bit which indicates whether to assume a beacon was missed when the SLP_BEACON_TIMEOUT occurs with no received beacons, in which case is assumes the DTIM was missed, and waits for CAB.
23:20	RES	Reserved
31:24	CAB_TIMEOUT	Time in TU that the PCU waits for CAB after receiving the beacon or the previous CAB, insuring that if no CAB is received after the beacon is received or if a long gap occurs between CABs, the CAB powersave state returns to idle.

5.10.28Sleep 2 (MAC_PCU_SLP2)

Offset: 0x080D8
Access: Hardware = Read/Write
Software = Read-only
Reset Value: 0x0

Bit	Name	Description
23:0	RES	Reserved
31:24	BEACON_TIMEOUT	Time in TU that the PCU waits for a beacon after waking up. If this time expires, the PCU woke due to SLP_NEXT_DTIM, and SLP_ASSUME_DTIM is active, then it assumes the beacon was missed and goes directly to watching for CAB. Otherwise when this time expires, the beacon powersave state returns to idle.

5.10.29Address 1 Mask Lower 32 Bits (MAC_PCU_ADDR1_MASK_L32)

This STA register provides multiple BSSID support when the AR5007AP-NG is in AP mode.

Offset: 0x080E0
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0xFFFFFFFF

Bit	Name	Description
31:0	STA_MASK_L	STA address mask lower 32-bit register. Provides multiple BSSID support.

5.10.30Address 1 Mask Upper 16 Bits (MAC_PCU_ADDR1_MASK_U16)

This STA register provides multiple BSSID support when the AR5007AP-NG is in AP mode.

Offset: 0x080E4
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0xFFFF

Bit	Name	Description
31:0	STA_MASK_L	STA address mask upper 16-bit register. Provides multiple BSSID support.

5.10.31Tx Power Control (MAC_PCU_TPC)

This register set the transmit power for self-generated response frames.

Offset: 0x080E8
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x3F

Bit	Name	Description
5:0	ACK_PWR	ACK self-generated response frames
7:6	RES	Reserved
13:8	CTS_PWR	CTS self-generated response frames
15:14	RES	Reserved
21:16	CHIRP_PWR	Chirp self-generated response frames
31:22	RES	Reserved

5.10.32Tx Frame Counter (MAC_PCU_TX_FRAME_CNT)

The Tx frame counter counts the number of cycles the tx_frame signal is active.

Offset: 0x080EC
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	TX_FRAME_CNT	Counts the number of cycles the tx_frame signal is active

5.10.33Rx Frame Counter (MAC_PCU_RX_FRAME_CNT)

The receive frame counter counts the number of cycles the rx_frame signal is active.

Offset: 0x080F0
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	RX_FRAME_CNT	Counts the number of cycles the rx_frame signal is active

5.10.34Rx Clear Counter (MAC_PCU_RX_CLEAR_CNT)

The receive clear counter counts the number of cycles the rx_clear signal is not active.

Offset: 0x080F4
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_CNT	Counts the number of cycles the rx_clear signal is active

5.10.35Cycle Counter (MAC_PCU_CYCLE_CNT)

The cycle counter counts the number of clock cycles.

Offset: 0x080F8
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	CYCLE_CNT	Counts the number of clock cycles

5.10.36Quiet Time 1 (MAC_PCU_QUIET_TIME_1)

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

Offset: 0x080FC
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

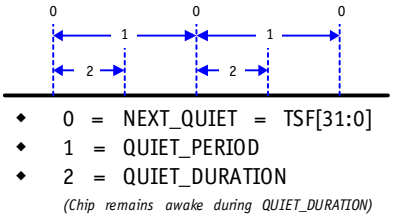
Bit	Name	Description
16:0	RES	Reserved
17	QUIET_ACK_CTS_ENABLE	If set, then the MAC sends an ACK or CTS in response to a received frame
31:18	RES	Reserved.

5.10.37Quiet Time 2 (MAC_PCU_QUIET_TIME_2)

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

Offset: 0x080FC
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

NOTE: QUIET_ENABLE is implemented as GENERIC_TIMER_ENABLE and NEXT_QUIET as GENERIC_TIMER_NEXT. QUIET_PERIOD is implemented as GENERIC_TIMER_PERIOD.



Bit	Name	Description
15:0	RES	Reserved
31:16	QUIET_DURATION	The length of time in TUs that the chip is required to be quiet

5.10.38QoS No ACK (MAC_PCU_QOS_NO_ACK)

This register provides a mechanism to locate the NoACK information in the QoS field and determine which encoding means NOACK.

Offset: 0x08108
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x2

Bit	Name	Description	
3:0	NOACK_2_BIT_VALUES	These values are of a two bit field that indicate No ACK	
		NOACK_2_BIT_VALUE	**Encoding Matching No ACK**
		xxx1	00
		xx1x	01
		x1xx	10
		1xxx	11
6:4	NOACK_BIT_OFFSET	Offsets from the byte where the No Ack information should be stored; offset can range from 0 to 6 only	
8:7	NOACK_BYTE_OFFSET	Number of bytes from the byte after end of the header of a data packet to the byte location where No Ack information is stored. (The end of the header is at byte offset 25 for 3-address packets and 31 for 4-address packets.)	
31:9	RES	Reserved.	

5.10.39PHY Error Mask (MAC_PCU_PHY_ERROR_MASK)

Offset: 0x0810C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x2

NOTE: Provides the ability to choose which PHY errors from the baseband to filter. The error number offsets into this register. If the mask value at the offset is 0, this error filters and does not show up on the Rx queue. Only the first 32 of the possible 256 PHY errors have a mask; all others are filtered.

Bit	Name	Description
0	ERROR TRANSMIT_UNDERRUN	Transmit underrun error
3:1	RES	Reserved.
4	ERROR PANIC	Panic error
5	ERROR RADAR_DETECT	Radar detect error
6	ERROR ABORT	Abort error
7	ERROR TX_INTERRUPT_RX	Transmit interrupt
16:8	RES	Reserved
17	ERROR OFDM TIMING	False detection for OFDM
18	ERROR OFDM SIGNAL_PARITY	OFDM signal parity error
19	ERROR OFDM RATE_ILLEGAL	OFDM illegal rate error
20	ERROR OFDM LENGTH_ILLEGAL	OFDM illegal length error
21	ERROR OFDM POWER_DROP	OFDM power drop error
22	ERROR OFDM SERVICE	OFDM service error
23	ERROR OFDM RESTART	OFDM restart error
24	RES	Reserved.
25	ERROR CCK TIMING	False detection for CCK
26	ERROR CCK HEADER_CRC	CCK CRC header error
27	ERROR CCK RATE_ILLEGAL	CCK illegal rate error
29:28	RES	Reserved.
30	ERROR CCK SERVICE	CCK service error
31	ERROR CCK RESTART	CCK restart error

5.10.40Rx Buffer Threshold (MAC_PCU_RXBUF_THRESHOLD)

Offset: 0x08114
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x400

Bit	Name	Description
10:0	RXBUF_THRSHD	When the number of valid entries in the Rx buffer is larger than this threshold, host interface logic gives higher priority to the Rx side to prevent Rx buffer overflow.
31:11	RES	Reserved.

5.10.41 QoS Control (MAC_PCU_MIC_QOS_CONTROL)

Offset: 0x08118
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0xAA

Bit	Name	Description	
1:0	MIC_QOS_CONTROL [0]	MIC QOS control [0]	
		0	Use 0 when calculating Michael
		1	Use 1 when calculating Michael
		2	Use MIC_QOS_SELECT when calculating Michael
		3	Use inverse of MIC_QOS_SELECT when calculating Michael
3:2	MIC_QOS_CONTROL [1]	MIC QOS control [1]. See options for "MIC_QOS_CONTROL [0]".	
5:4	MIC_QOS_CONTROL [2]	MIC QOS control [2]. See options for "MIC_QOS_CONTROL [0]".	
7:6	MIC_QOS_CONTROL [3]	MIC QOS control [3]. See options for "MIC_QOS_CONTROL [0]".	
9:8	MIC_QOS_CONTROL [4]	MIC QOS control [4]. See options for "MIC_QOS_CONTROL [0]".	
11:10	MIC_QOS_CONTROL [5]	MIC QOS control [5]. See options for "MIC_QOS_CONTROL [0]".	
13:12	MIC_QOS_CONTROL [6]	MIC QOS control [6]. See options for "MIC_QOS_CONTROL [0]".	
15:14	MIC_QOS_CONTROL [7]	MIC QOS control [7]. See options for "MIC_QOS_CONTROL [0]".	
16	MIC_QOS_ENABLE	Enable MIC QOS control	
		0	Disable hardware Michael
		1	Enable hardware Michael

5.10.42 Michael QoS Select (MAC_PCU_MIC_QOS_SELECT)

Offset: 0x0811C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x3210

Bit	Name	Description
3:0	MIC_QOS_SELECT [0]	MIC QOS select [0]. Select the OOS TID bit when calculating Michael.
7:4	MIC_QOS_SELECT [1]	MIC QOS select [1]. Select the OOS TID bit when calculating Michael.
11:8	MIC_QOS_SELECT [2]	MIC QOS select [2]. Select the OOS TID bit when calculating Michael.
15:12	MIC_QOS_SELECT [3]	MIC QOS select [3]. Select the OOS TID bit when calculating Michael.
19:16	MIC_QOS_SELECT [4]	MIC QOS select [4]. Select the OOS TID bit when calculating Michael.
23:20	MIC_QOS_SELECT [5]	MIC QOS select [5]. Select the OOS TID bit when calculating Michael.
27:24	MIC_QOS_SELECT [6]	MIC QOS select [6]. Select the OOS TID bit when calculating Michael.
31:28	MIC_QOS_SELECT [7]	MIC QOS select [7]. Select the OOS TID bit when calculating Michael.

5.10.43Miscellaneous Mode (MAC_PCU_MISC_MODE)

The internal address for this register is 048, and the clock is system_clk.

Offset: 0x08120
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
0	BSSID_MATCH_FORCE	If the BSSID_MATCH_FORCE bit is set, all logic based on matching the BSSID thinks that the BSSID matches.
1	RES	Reserved.
2	MIC_NEW_LOCATION_ ENABLE	If the MIC_NEW_LOCATION_ENABLE is set, the transmit Michael Key is assumed to be co-located in the same entry that the receive Michael key is located.
3	TX_ADD_TSF	If the TX_ADD_TSF bit is set, the TSF in the transmit packet will be added to the internal TSF value for transmit beacons and prob_response frames.
4	CCK_SIFS_MODE	If the CCK_SIFS_MODE is set, the chip assumes that it is using 802.11g mode where SIFS is set to 10 µs and non-CCK frames must add 6 to SIFS to make it CCK frames. This bit is needed in the duration calculation, which also needs the SIFS_TIME register.
11:5	RES	Reserved.
12	TXOP_TBTT_LIMIT_ ENABLE	If this limit is set, then logic to limit the value of the duration to fit the time remaining in TXOP and time remaining until TBTT is turned on. This logic will also filter frames, which will exceed TXOP.
17:13	RES	Reserved.
18	FORCE_QUIET_ COLLISION	If the FORCE_QUIET_COLLISION bit is set, the PCU thinks that it is in quiet collision period, kills any transmit frame in progress, and prevents any new frame from starting.
19	RES	Reserved.
20	BT_ANT_PREVENT	If this bit is set, the Rx state machine does now allow any new receive frames into the Rx buffer while the BT_ANT signal is asserted, thus preventing receives of new frames when Bluetooth has control over the antenna. When the antenna switches over to the Bluetooth device, if the WLAN Rx frame RSSI is strong, it may still be received although attenuated. Setting this bit prevents the frame from entering the Rx path.
21	TBTT_PROTECT	If the TBTT_PROTECT bit is set, then the time from TBTT to 20 µs after TBTT is protected from transmit. Turn this off in ad hoc mode or if this MAC is used in the AP.
22	HCF_POLL_CANCELS_ NAV	If the HCF_POLL_CANCELS_NAV bit is set when a directed HCF poll is received, the current NAV is cancelled and HCF data burst can proceed at SIFS.
23	RX_HCF_POLL_ENABLE	If the RX_HCF_POLL_ENABLE bit is set, then the MAC is enabled to receive directed HCF polls. If this bit is not set the receive state machine does not tell the rest of the MAC that it has received a directed HCF poll.
24	CLEAR_VMF	If the CLEAR_VMF bit is set, then the VMF mode in the transmit state machine will be cleared. Set this bit to enter fast channel change mode and clear it once fast channel change is over.

Bit	Name	Description
25	CLEAR_FIRST_HCF	If the CLEAR_FIRST_HCF bit is set, then the first_hcf state will be cleared. Set this bit to enter fast channel change mode and clear the bit once fast channel change is over.
26	CLEAR_BA_VALID	If the CLEAR_BA_VALID bit is set, the state of the block ACK storage is invalidated.
27	SEL_EVM	If the SEL_EVM bit is set, the evm field of the Rx descriptor status contains the EVM data received from the baseband. If this bit is cleared, the evm field of the Rx descriptor status contains 3 bytes of Legacy PLCP, 2 service bytes, and 6 bytes of HP PLCP.
28	ALWAYS_PERFORM_ KEY_SEARCH	If this bit is set, key search is performed for every frame in an aggregate. If this bit is cleared, key search is only performed for the first frame of an aggregate. Unless the transmitter address is different between the frames in an aggregate. This bit has no effect on non-aggregate frame packets.

5.10.44Filtered OFDM Counter (MAC_PCU_FILTER_OFDM_CNT)

The filtered OFDM counters use the MIB control signals. The internal address for this register is 049, and the clock is system_clk.

Offset: 0x08124
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	FILTOFDM_CNT	Counts the OFDM frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

5.10.45Filtered CCK Counter (MAC_PCU_Filter_CCK_CNT)

The internal address for this register is 04A, and the clock is system_clk.

Offset: 0x08128
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	FILTCCK_CNT	Counts the CCK frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

5.10.46PHY Error Counter 1 (MAC_PCU_PHY_ERR_CNT_1)

The PHY error counters count any PHY error matching the respective mask. The bits of 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FF, then all PHY errors from 0–7 and 24–31 are counted.

The internal address for this register is 04B, and the clock is system_clk.

Offset: 0x0812C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	PHY_ERROR_CNT1	Counts any PHY error1 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

5.10.47PHY Error Counter 1 Mask (MAC_PCU_PHY_ERR_CNT_1_MASK)

The internal address for this register is 04C, and the clock is system_clk.

Offset: 0x08130
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	PHY_ERROR_CNT_MASK1	Counts any error that matches the PHY error1 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

5.10.48PHY Error Counter 2 (MAC_PCU_PHY_ERR_CNT_2)

The internal address for this register is 04E, and the clock is system_clk.

Offset: 0x08134
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	PHY_ERROR_CNT_MASK2	Counts any error that matches the PHY error2 mask. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

5.10.49PHY Error Counter 2 Mask (MAC_PCU_PHY_ERR_CNT_2_MASK)

The internal address for this register is 04D, and the clock is system_clk.

Offset: 0x08138
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	PHY_ERROR_CNT2	Counts any PHY error2 using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. PIB MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

5.10.50TSF Threshold (MAC_PCU_TSF_THRESHOLD)

The internal address for this register is 04F, and the clock is system_clk.

Offset: 0x0813C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
15:0	TSF_THRESHOLD	Asserts the PCU_TSF_OUT_OF_RANGE_INTER if the corrected receive TSF in a beacon is different from the internal TSF by more than this threshold.

5.10.51PHY Error EIFS Mask (MAC_PCU_PHY_ERROR_EIFS_MASK)

Offset: 0x08144
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	VALUE	This mask provides the ability to choose which PHY errors from the baseband cause EIFS delay. The error number is used as an offset into this mask. If the mask value at the offset is 1, then this error will not cause EIFS delay.

5.10.52PHY Error Counter 3 (MAC_PCU_PHY_ERR_CNT_3)

Offset: 0x08168
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	VALUE	Count of PHY errors that pass the PHY_ERR_CNT_3_MASK filter

5.10.53PHY Error Counter 3 Mask (MAC_PCU_PHY_ERR_CNT_3_MASK)

Offset: 0x0816C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
23:0	VALUE	Mask of the PHY error number allowed to be counted

5.10.54Bluetooth Mode (MAC_PCU_BLUETOOTH_MODE)

Offset: 0x08170
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

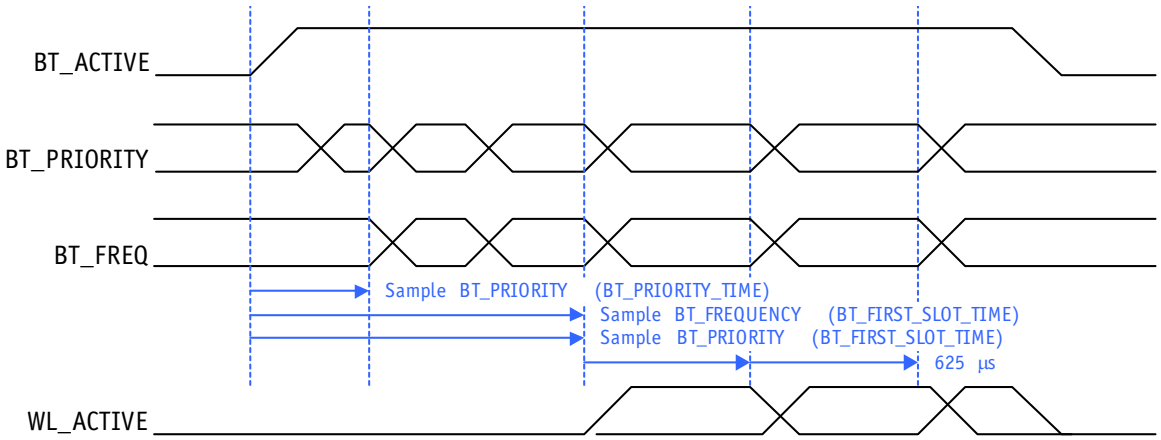


Figure 5-1. **Bluetooth Mode**

Bit	Name	Description	
7:0	TIME_EXTEND	Extends the rx_clear after the transmit or receive of a frame so that bursts are protected; value in µs	
8	TX_STATE_EXTEND	Extends the rx_clear as long as TXSM transmits or waits for a response	
9	TX_FRAME_EXTEND	Extends the rx_clear so that as soon as the tx_frame asserts at the MAC the rx_clear drops	
11:10	BT_MODE	0x0	The device is in legacy rx_clear mode
		0x1	The device is in un-timed mode (three-wire mode)
		0x2	The device is in slotted mode (four-wire mode)
		0x3	The device does not support Bluetooth coexistence
12	QUIET	Causes a quiet collision on transmit if the Bluetooth device has higher priority	
16:13	QCU_THRESH	Indicates which QCUs are high priority. Any QCU number that is greater than or equal to the QCU_THRESH is treated as high priority.	
17	RX_CLEAR_POLARITY	If high	If this bit is high then the output polarity of the RX_CLEAR is inverted, thus when RX_CLEAR is high the WLAN is active.
		If low	If this bit is low when RX_CLEAR is low, then WLAN is active.
23:18	PRIORITY_TIME	Used in the slotted mode (BT_MODE = 0x2) to indicate the time in µs from the rising edge or BT_ACTIVE to when the BT_PRIORITY pin can be sampled to indicate priority	
31:24	FIRST_SLOT_TIME	The time from the rising edge of BT_ACTIVE to the time in µs when the BT_PRIORITY signal is sampled as the Tx/Rx and BT_FREQ is sampled. Based on this information the BT_ACTIVE signal is driven on the RX_CLEAR pin.	

5.10.55MAC PCU Bluetooth Coexistence Weights (BT_WEIGHT)

Offset: 0x08174
Access: Hardware = Read-only
Software = Read/Write
Reset Value: See field descriptions

WL_LEVEL is compared to BT_LEVEL. If WL_LEVEL is equal to or greater than BT_LEVEL, WLAN is given priority and has control over the antenna.

Bit	Name	Description			
15:0	BT_WEIGHT	Resets to 0xFA50. Input condition:			
		BT_PRIORITY	**BT_FREQ**	**BT_TX_RX**	**BT_LEVEL**
		0	0	0	BT_BT_WEIGHT[1:0]
		0	0	1	BT_BT_WEIGHT[3:2]
		0	1	0	BT_BT_WEIGHT[5:4]
		0	1	1	BT_BT_WEIGHT[7:6]
		1	0	0	BT_BT_WEIGHT[9:8]
		1	0	1	BT_BT_WEIGHT[11:10]
		1	1	0	BT_BT_WEIGHT[13:12]
		1	1	1	BT_BT_WEIGHT[15:14]
		Resets to 0xFA50. In un-slotted mode:			
		BT_PRIORITY	**BT_FREQ**	**BT_ACTIVE**	**BT_LEVEL**
		0	0	0	BT_BT_WEIGHT[1:0]
		0	0	1	BT_BT_WEIGHT[3:2]
		0	1	0	BT_BT_WEIGHT[5:4]
		0	1	1	BT_BT_WEIGHT[7:6]
		1	0	0	BT_BT_WEIGHT[9:8]
		1	0	1	BT_BT_WEIGHT[11:10]
		1	1	0	BT_BT_WEIGHT[13:12]
		1	1	1	BT_BT_WEIGHT[15:14]
31:16	WL_WEIGHT	Resets to 0xFAA4. Input condition:			
		WL_WAIT_BEACON	**QCU_PRIORITY**	**WL_RX_CLEAR**	**WL_LEVEL**
		0	0	0	BT_WL_WEIGHT[1:0]
		0	0	1	BT_WL_WEIGHT[3:2]
		0	1	0	BT_WL_WEIGHT[5:4]
		0	1	1	BT_WL_WEIGHT[7:6]
		1	0	0	BT_WL_WEIGHT[9:8]
		1	0	1	BT_WL_WEIGHT[11:10]
		1	1	0	BT_WL_WEIGHT[13:12]
		1	1	1	BT_WL_WEIGHT[15:14]

5.10.56HCF Timeout (MAC_PCU_HCF_TIMEOUT)

Offset: 0x08178
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
15:0	VALUE	The time the PCU waits after the HCF trigger timer occurs before the PCU returns to sleep mode, unless the HCF poll has been detected. An interrupt is generated if the timeout occurs before a HCF poll is detected.

5.10.57Bluetooth Mode 2 (MAC_PCU_BLUETOOTH_MODE2)

Offset: 0x0817C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
7:0	BCN_MISS_THRESH	>1	This threshold is compared to the beacon miss count If the beacon miss count is greater than BT_BCN_MISS_THRESH, the MAC switches BT_ANT to listen for beacons until a beacon is received or a beacon timeout occurs. If the beacon timeout occurs, BT_ANT can resume normal behavior until the next time the MAC waits for a beacon.
		0	Logic is disabled. This register applies to both slotted and un-slotted modes.
15:8	BCN_MISS_CNT	The BCN_MISS_CNT is a read only register of the current count of consecutive missed beacons.	
16	HOLD_RX_CLEAR	If high	The external RX_CLEAR and the BT_ANT decision are held the entire time that BT_ACTIVE is asserted
		If low	The external RX_CLEAR and the BT_ANT decision are made before every slot boundary. This register applies only to the slotted mode.

5.10.58SIFS, Tx Latency and ACK Shift (MAC_PCU_TXSIFS)

Offset: 0x081D0
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
7:0	SIFS_TIME	SIFS_TIME is the number of µs in SIFS. For example, in 802.11a, SIFS_TIME would be set to 16. This value is used to determine quiet collision and filtering due to TBTT and TXOP limits.	
11:8	TX_LATENCY	TX_LATENCY is the latency in µs from tx_frame being asserted by the MAC to when the energy of the frame is on the air. This value is used to decrease the time to TBTT and time remaining in TXOP in the calculation to determine quiet collision.	
14:12	ACK_SHIFT	ACK_SHIFT register is used to generate the ACK_TIME, which is used to generate the ACK_SIFS_TIME. The ACK_TIME table in the hardware assumes a channel width of 2.5 MHz. This value should be 3 for CCK rates.	
		0	2.5 MHz
		1	5 Mhz

5.10.59TxOP for Non-QoS Frames (MAC_PCU_TXOP_X)

Offset: 0x081EC
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	SIFS_TIME	TXOP in units of 32 µs. A TXOP value exists for each QOS TID value. When a new burst starts, the TID is used to select one of the 16 TXOP values. This TXOP decrements until the end of the burst to make sure that the packets are not sent out by the time TXOP expires. TXOPX is used for legacy non QOS bursting.

5.10.60TxOP for TID 0 to 3 (MAC_PCU_TXOP_0_3)

Offset: 0x081F0
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	VALUE_0	Value in units of 32 µs
15:8	VALUE_1	Value in units of 32 µs
23:16	VALUE_2	Value in units of 32 µs
31:24	VALUE_3	Value in units of 32 µs

5.10.61TXOP for TID 4 to 7 (MAC_PCU_TXOP_4_7)

Offset: 0x081F4
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	VALUE_4	Value in units of 32 µs
15:8	VALUE_5	Value in units of 32 µs
23:16	VALUE_6	Value in units of 32 µs
31:24	VALUE_7	Value in units of 32 µs

5.10.62TXOP for TID 8 to 11 (MAC_PCU_TXOP_8_11)

Offset: 0x081F8
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	VALUE_8	Value in units of 32 µs
15:8	VALUE_9	Value in units of 32 µs
23:16	VALUE_10	Value in units of 32 µs
31:24	VALUE_11	Value in units of 32 µs

5.10.63TXOP for TID 0 to 3 (MAC_PCU_TXOP_12_15)

Offset: 0x081FC
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	VALUE_12	Value in units of 32 µs
15:8	VALUE_13	Value in units of 32 µs
23:16	VALUE_14	Value in units of 32 µs
31:24	VALUE_15	Value in units of 32 µs

5.10.64Generic Timers (MAC_PCU_GENERIC_TIMERS[0:15])

Offset: 0x08200
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Address	Default	Description
0x0200–0x021C	0x0	GENERIC_TIMER_NEXT
0x0220–0x023C	0x0	GENERIC_TIMER_PERIOD
0x0240	GENERIC_TIMER_MODE	
	0x0	ENABLE[7:0]
	0x0	OVERFLOW_INDEX[10:8] Indicates the last generic timer that overflowed.
	0x100	GENERIC_TIMER_THRESH [31:11] Number of µs that, if exceeded in the TSF comparison, will generate a threshold interrupt. Threshold interrupts correspond to these timers.

Generic Timer	Function
0	TBTT
1	DMA beacon alert
2	SW beacon alert
3	HCF trigger timer
4	NEXT_TIM
5	NEXT_DTIM
6	Quiet time trigger
7	No dedicated function

NOTE: GENERIC _TIMER_0, unlike other generic timers, does not wake the MAC before timer expiration and its overflow mechanism does not generate an interrupt. Instead, it silently adds this period repeatedly until the next timer has advanced past the TSF. Thus when MAC wakes after sleeping for multiple TBTTs, the TGBTT does not assert repeatedly or cause the beacon miss count to jump.

5.10.65Generic Timers Mode (MAC_PCU_GENERIC_TIMERS_MODE)

Offset: 0x08240
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	ENABLE	
10:8	OVERFLOW_INDEX	Indicates the last generic timer that overflowed
31:11	THRESH	Number of µs that generate a threshold interrupt if exceeded in TSF comparison

5.10.6632 KHz Sleep Mode (MAC_PCU_SLP32_MODE)

Offset: 0x08244
Access: Hardware = Read-only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
19:0	HALF_CLK_LATENCY	Time in µs from the detection of the falling edge of the 32 KHz clk to the rising edge of the 32 KHz clk. Reset Value: 0xF424
20	ENABLE	When set, indicates that the TSF should be allowed to increment on its own. Reset Value: 0x1
21	TSF_WRITE_STATUS	The TSF write status. Reset Value: 0x1
22	DISABLE_32KHZ	Indicates the 32 KHz clock is not used to control the TSF, but the MAC clock increments the TSF. Only used on AP class devices that do not go to sleep. Reset Value: 0x0

5.10.6732 KHz Sleep Wake (MAC_PCU_SLP32_WAKE)

Offset: 0x08248
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x800

Bit	Name	Description
15:0	XTL_TIME	Time in µs before a generic timer should expire that the wake signal asserts to the crystal wake logic. Add an extra 31 µs due to 32 KHz clock resolution.

5.10.6832 KHz Sleep Increment (MAC_PCU_SLP32_INC)

Offset: 0x0824C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x1E848

Bit	Name	Description
19:0	TSF_INC	Time in $1/2^{12}$ of a µs the TSF increments on the rising edge of the 32 KHz clk (30.5176 µs period). The upper 8 bits are at µs resolution. The lower 12 bits are the fractional portion. $\frac{1 \text{ unit}}{1/212 \text{ ms}} = \frac{X}{30.5176 \text{ ms}}$ Where *X* = 125000, or 0x1E848 is the default setting for 32.768 MHz clock.

5.10.69Sleep MIB Sleep Count (MAC_PCU_SLP_MIB1)

Offset: 0x08250
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	SLEEP_CNT	Counts the number of 32 KHz clock cycles that the MAC has been asleep

5.10.70Sleep MIB Cycle Count (MAC_PCU_SLP_MIB2)

Offset: 0x08254
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	CYCLE_CNT	Counts the absolute number of 32KHz clock cycles. When CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing.

5.10.71Sleep MIB Control Status (MAC_PCU_SLP_MIB3)

Offset: 0x08258
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
0	CLR_CNT	CLR_CNT clears both SLEEP_CNT and CYCLE_CNT. Pending is asserted while the clearing of these registers is pending.
1	PENDING	SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the pending bit should be polled to verify any pending write has cleared.

5.10.72MAC PCU Wake on Wireless 1 (MAC_PCU_WOW1)

Offset: 0x0825C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
7:0	PATTERN_ENABLE	Indicates which of the eight patterns are enabled for compare; resets to 0xFF
15:8	PATTERN_DETECT	Indicates which of the eight patterns are matched for a Rx packet; resets to 0x0
16	MAGIC_ENABLE	When set, indicates that magic packet detection has been enabled; resets to 0x0
17	MAGIC_DETECT	Set when a magic packet has been detected; resets to 0x0
18	INTR_ENABLE	When set, indicates that unmasked MAC interrupts cause WOW detection; resets to 0x0
19	INTR_DETECT	Set when an interrupt is detected; resets to 0x0
20	KEEP_ALIVE_FAIL	Indicates excessive retry or other problems that cause the keep-alive packet from successful transmission; resets to 0x0
21	BEACON_FAIL	Indicates the beacon receive timeout; resets to 0x0
31:28	CW_BITS	Indicates the number of bits used in the contention window; resets to 0x4 If CW_BITS = N, the random backoff is selected between 0 and (2^N–1). E.g., if CS_BITS = 4, the random backoff will be selected between 0 and 15. Values larger than 10 are assumed to be 10.

5.10.73MAC PCU Wake on Wireless 2 (MAC_PCU_WOW2)

Offset: 0x08260
Access: Hardware = Read/Write
Software = Write-only
Reset Value: See field description

Bit	Name	Description
7:0	AIFS	The time in µs for AIFS; resets to 34
15:8	SLOT	The time in µs for SLOT; resets to 9
23:16	TRY_CNT	Reset value = 8

5.10.74Wake on Wireless 3 Beacon Fail (MAC_PCU_WOW3_BEACON_FAIL)

Offset: 0x08270
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
0	ENABLE	Enable wake-on-wireless if the AP fails to send a beacon

5.10.75Wake on Wireless 3 Beacon Timeout (MAC_PCU_WOW3_BEACON)

Offset: 0x08274
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x40000000

Bit	Name	Description
31:0	TIMEOUT	WoW beacon fail timeout value (refclk cycles)

5.10.76Wake on Wireless 3 Keep-Alive Timeout (MAC_PCU_WOW3_KEEP_ALIVE)

Reset Value: 0x3E4180

Offset: 0x08278
Access: Hardware = Read/Write
Software = Read/Write

Bit	Name	Description
31:0	TIMEOUT	WoW keep-alive timeout value (refclk cycles)

5.10.77MAC PCU WoW Keep-Alive Disable Bit (MAC_PCU_WOW_KA)

Offset: 0x0827C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
0	AUTO_DISABLE	Disable automatic transmission of keep-alive frames
1	FAIL_DISABLE	Disable WoW if there is a failure sending keep-alive frames

5.10.78Number of Clocks in One Microsecond (PCU_1US)

Offset: 0x08284
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x2C

Bit	Name	Description
6:0	SCALER	Number of MAC clocks in one µs

5.10.79Delay Between WoW Keep-Alive Frames (PCU_KA)

Offset: 0x08288
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x2C

Bit	Name	Description
11:0	DEL	Delay between WoW keep-alive frames

5.10.80Exact Length and Offset Requirement Flag for WoW Patterns (WOW_EXACT)

Offset: 0x0828C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	LENGTH	Exact length requirement flag for WoW patterns; 1 bit for each pattern
15:8	OFFSET	Exact offset requirement flag for WoW patterns; 1 bit for each pattern

5.10.81WoW Offset 1 (PCU_WOW4)

Offset: 0x08294
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	OFFSET4	Offset for pattern 4
15:8	OFFSET5	Offset for pattern 5
23:16	OFFSET6	Offset for pattern 6
31:24	OFFSET7	Offset for pattern 7

5.10.82WoW Offset 2 (PCU_WOW5)

Offset: 0x08298
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
7:0	OFFSET4	Offset for pattern 4
15:8	OFFSET5	Offset for pattern 5
23:16	OFFSET6	Offset for pattern 6
31:24	OFFSET7	Offset for pattern 7

5.10.83Global Mode (MAC_PCU_20_40_MODE)

Reset Value: 0x0

Offset: 0x08318
Access: Hardware = Read-only
Software = Read/Write

Bit	Name	Description
0	JOINED_RX_CLEAR	Setting this bit causes the rx_clear used in the MAC to be the AND of the control channel rx_clear and the extension channel rx_clear. If this bit is clear then the MAC will use only the control channel rx_clear.

5.10.84Difference Rx_Clear Counter (MAC_PCU_RX_CLEAR_DIFF_CNT)

Offset: 0x08328
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_DIFF_CNT	A cycle counter MIB register. On every cycle of the MAC clock, this counter increments every time the extension channel rx_clear is low when the MAC is not actively transmitting or receiving. Due to a small lag between tx_frame and rx_clear as well as between rx_clear and rx_frame, the count may have some residual value even when no activity is on the extension channel.

5.10.85Antenna Mask for Self-Generated Files (MAC_PCU_SELF_GEN_ANTENNA_MASK)

Offset: 0x0832C
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x7

Bit	Name	Description
2:0	VALUE	The antenna mask normally comes from the transmit descriptor. For self generated frames, this register provides the antenna mask to the baseband via the MAC/baseband interface.

5.10.86Control Registers for Block BA Control Fields (MAC_PCU_BA_BAR_CONTROL)

Offset: 0x08330
Access: Hardware = Read-only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
3:0	COMPRESSED_OFFSET	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the COMPRESSED bit. Reset Value: 0x2
7:4	ACK_POLICY_OFFSET	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the ACK policy bit. Reset Value: 0x0
8	COMPRESSED_VALUE	The value of the compressed bit. Reset Value: 0x1
9	ACK_POLICY_VALUE	The value of the ACK policy bit. Reset Value: 0x1

5.10.87Legacy PLCP Spoof (MAC_PCU_LEGACY_PLCP_SPOOF)

Offset: 0x08334
Access: Hardware = Read-only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
7:0	EIFS_MINUS_DIFS	Defines the number of µs to be subtracted from the transmit packet duration to provide fairness for legacy devices as well as HT devices. Reset Value: 0x0
4:0	MIN_LENGTH	This register defines the minimum spoofed legacy PLCP length. Reset Value: 0xE

5.10.88PHY Error Mask and EIFS Mask (MAC_PCU_PHY_ERROR_MASK_CONT)

Offset: 0x08338
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
2:0	MASK_VALUE	Continuation of register MAC_PCU_PHY_ERROR_MASK_VALUE. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All others PHY errors above 34 will be filtered.
18:16	EIFS_VALUE	Continuation of register MAC_PCU_PHY_ERROR_MASK_VALUE. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All others PHY errors above 34 cause EIFS delay.

5.10.89Tx Timer (MAC_PCU_TX_TIMER)

Offset: 0x0833C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
14:0	TX_TIMER	Guarantees the transmit frame does not take more time than the values programmed in this timer. The unit for this timer is in µs.
15	TX_TIMER_ENABLE	Enabled when this bit is set to 1.

5.10.90Key Cache (MAC_PCU_KEY_CACHE[0:1023])

Offset: 0x08800
Access: Hardware = Read-only
Software = Read/Write
Reset Value: 0x0

Table 5-14. **Offset to First Dword of *N*th Key [1]**

Intra Key	Offset Bits	Description	
8*N + 00	31:0	key[31:0]	
8*N + 04	15:0	key[47:32]	
8*N + 08	31:0	key[79:48]	
8*N + 0C	15:0	key[95:79]	
8*N + 10	31:0	key[127:96]	
8*N + 14	2:0	key type:	
		0	40b
		1	104b
		2	TKIP without MIC
		3	128b
		4	TKIP
		5	AES_OCB
		6	AES_CCM
		7	Do nothing
8*N + 14	14:3	Reserved	
8*N + 18	31:0	Addr[32:1]	
8*N + 1C	14:0	Addr[47:33]	
	15	Key valid	

[1]key = (int addr: 200 + 8*N)
(PCI Address: 8800 + 20*N)

The key cache contains sensitive information that normally is not accessible via the host interface. A bit loaded by the EEPROM indicates whether the key cache is readable. In either mode the keycache accesses return the last Tx.

When the key type is 4 (TKIP) and key is valid, this entry + 64 contains the Michael key.

Table 5-15. **Offset to First Dword of *N*th Key (continued)**

Intra Key	Offset Bits	Description
8*N + 800	31:0	Rx Michael key 0
8*N + 804	15:0	Tx Michael key 0 [31:16]
8*N + 808	31:0	Rx Michael key 1
8*N + 80C	15:0	Tx Michael key 0 [15:0]
8*N + 810	31:0	Tx Michael key 1
8*N + 814	RES	Reserved
8*N + 818	RES	Reserved
8*N + 81C	RES	Reserved
	15	Key Valid = 0

TKIP keys are not allowed to reside in the entries 64–127 because they require the Michael key. Entries 64–67 are always reserved for Michael.

NOTE: Internally this memory is 48 bits wide, thus to write a line of the memory requires two 32-bit writes. All writes to registers with an offset of 0x0 or 0x8 actually write to a temporary holding register. A write to register with an offset of 0x4 or 0xC writes to the memory with the current write value concatenated with the temporary holding register.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1 summarizes the absolute maximum ratings and Table 6-2 lists the recommended operating conditions for the AR5416 solution. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 6-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{dd18}	Supply voltage	–0.3 to 2.5	V
V_{dd33}	Maximum I/O supply voltage	–0.3 to 4.0	V
T_{store}	Storage temperature	–60 to 150	°C
ESD	Electrostatic discharge tolerance	2000	V

6.2 Recommended Operating Conditions

Table 6-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{dd18}	Supply voltage	±5%	1.71	1.8	1.89	V
V_{dd33}	I/O voltage	±10%	2.97	3.3	3.63	V
T_{case}	Case temperature	—	0	25	95	°C
$T_{industrial}$	Industrial case temperature	—	–40	25	95	°C
T_j	Junction temperature	—	–40	50	120	°C

6.3 Power Consumption

These conditions apply to the following typical characteristics unless otherwise specified:

V_{dd18} = 1.8 V
V_{dd33} = 3.3 V, T_{amb} = 25 °C

Table 6-3 depicts typical power drain on each of the two on-chip power supply domains as a function of the AR5416's operating mode.

Table 6-3. **Power Consumption**

Operating Mode	3.3 V Supply (mA)	1.8 V Supply (mA)
Sleep	6.8	4
Idle (One-stream Rx)	15	85
Idle (Two-stream Rx)	23	245
Idle (Three-stream Rx)	32	310
Tx (One-stream)	29.4	255.8
Tx (Two-stream)	39.5	402.3
Tx (Three-stream)	54	518.3
Rx (One-stream)	18.6	336
Rx (Two-stream)	31.6	542.3
Rx (Three-stream)	31.8	708.27

7. Low Dropout Regulator

The AR5416 can be powered by external regulators or on-chip analog and digital regulators. The pin PWD_REGS controls selection of external or internal voltage regulators. Connect this pin to ground through a 0 Ω resistor to enable the internal regulators. When external regulators are used, this pin should be left open (NC).

Along with external PNP and compensation network, the internal digital and analog voltage regulator blocks provide a regulated 1.8 V power supply for the AR5416, and analog 1.8 V power supply to the AR2133/AR5133, respectively.

7.1 Digital Low Dropout Regulator

Figure 7-1 displays a diagram with recommended components for the AR5416 digital low dropout regulator. If the on-chip regulator is not used, the COMP_DIG pin should be shorted to DVDD33, and the VREG_DIG pin should be left open (NC).

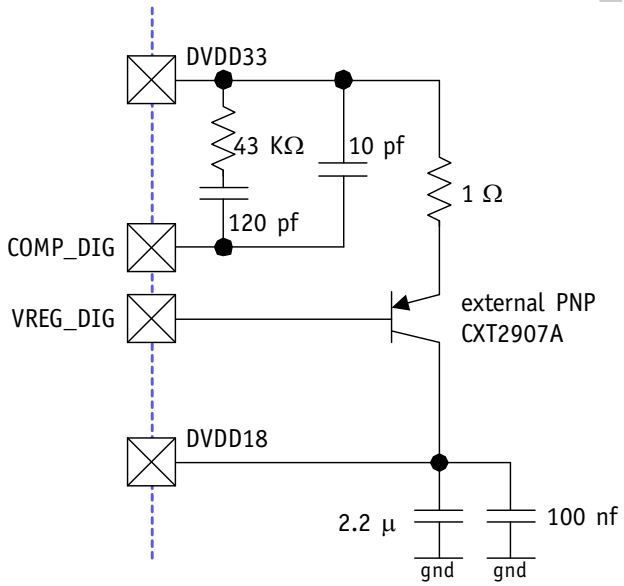


Figure 7-1. **Digital Low Dropout Regulator**

7.1.1 Compensation Network

The on-chip regulator must be compensated with the series-parallel combination of resistors and capacitors as shown in Figure 7-1. It is also important to ensure that bypass capacitance at the output of the regulator does not exceed 4.7 µF. A 1 Ω resistor must be inserted between the emitter of the external PNP and the 3.3 V supply. Five percent components are sufficient.

7.1.2 PNP Transistor

For the PNP transistor, use a transistor with strong current gain at 250 mA; a transistor with a beta of at least 35 is sufficient.

7.2 Analog Low Dropout Regulator

Figure 7-2 displays a diagram with recommended components for the AR5416 analog low dropout regulator. If the on-chip regulator is not used, the COMP_ANA pin should be shorted to AVDD33 or left open, and the VREG_ANA pin should be left open (NC).

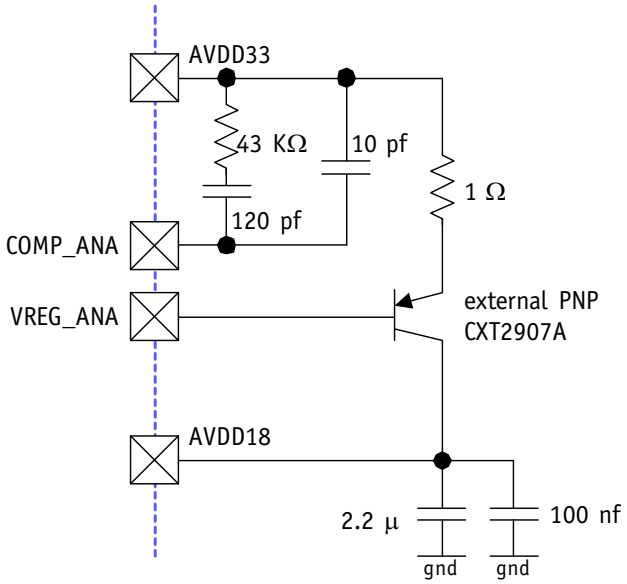


Figure 7-2. **Analog Low Dropout Regulator**

7.2.1 Compensation Network

The on-chip regulator must be compensated with the series-parallel combination of resistors and capacitors as shown in Figure 7-2. It is also important to ensure that the bypass capacitance at the output of the regulator does not exceed 4.7 µF. A 1 Ω resistor must be inserted between the emitter of the external PNP and the 3.3 V supply. Five percent components are sufficient.

7.2.2 PNP Transistor

For the PNP transistor, use a transistor with strong current gain at 250 mA; a transistor with a beta of at least 35 is sufficient.

The LDO powers analog circuits on the AR5416 and the AR2133/AR5133.

8. Package Dimensions

The AR5416 is packaged in a 304-pin JEDEC MO-207 compliant BGA package. The body size is 14 mm by 14 mm.

The BGA package drawings and dimensions are provided in Figure 8-1 and Table 8-1.

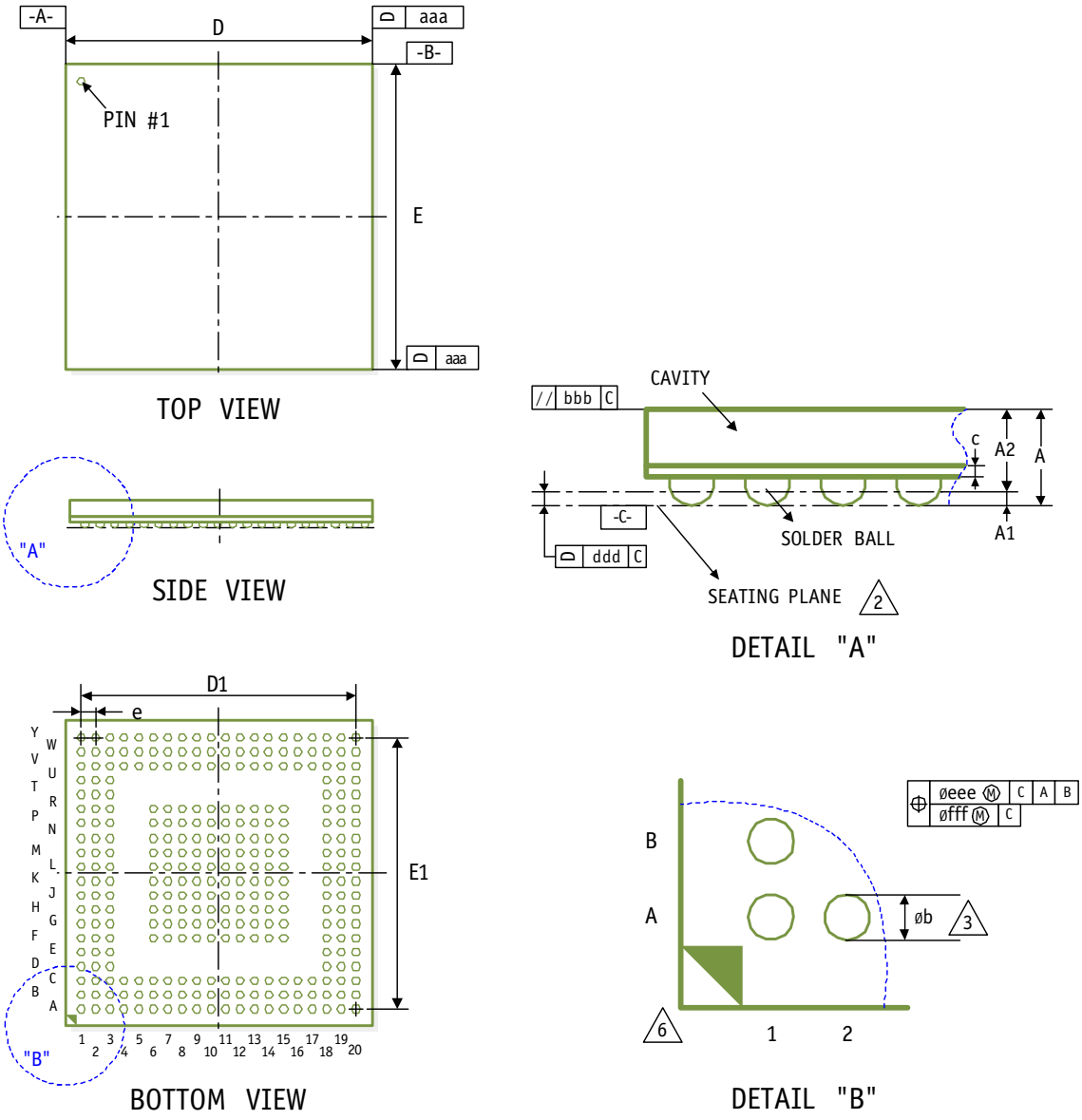


Figure 8-1. **Package Drawing**

Table 8-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.00	mm	—	—	0.039	inches
A1	0.16	0.21	0.26	mm	0.006	0.008	0.010	inches
A2	0.61	0.66	0.71	mm	0.024	0.026	0.028	inches
c	0.17	0.21	0.25	mm	0.007	0.008	0.010	inches
D	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
E	13.90	14.00	14.10	mm	0.547	0.551	0.555	inches
D1	—	12.35	—	mm	—	0.486	—	inches
E1	—	12.35	—	mm	—	0.486	—	inches
e	—	0.65	—	mm	—	0.026	—	inches
b	0.25	0.30	0.35	mm	0.010	0.012	0.014	inches
aaa	0.15			mm	0.006			inches
bbb	0.20			mm	0.008			inches
ccc	0.08			mm	0.003			inches
ddd	0.15			mm	0.006			inches
eee	0.08			mm	0.003			inches
MD/ME	20/20				20/20			

Notes:

1. Controlling dimension: Millimeters.
2. Primary DATUM C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary DATUM C.
4. A minimum clearance of 0.25 mm is required between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO–207.
6. The pattern of Pin 1 fiducial is for reference only.
7. Special characteristics of class C: bbb, ccc.

9. Ordering Information

The order number is determined by the selection of these options.

The order number AR5416-*AC0A* specifies a BGA standard temperature leaded version of the AR5416.

The order number AR5416-*AC1A* specifies a BGA standard temperature lead-free version of the AR5416.

Document Number: 981-00045-001 MKG-0273 Rev. 3

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