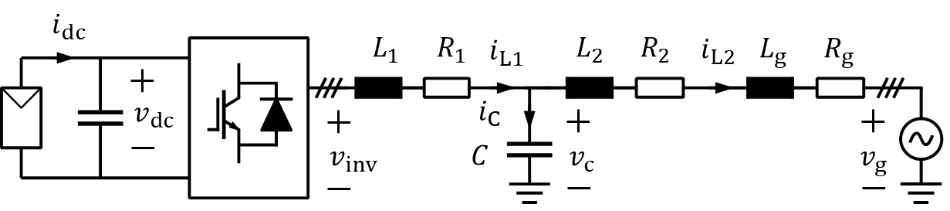
## **Impedance Model for Inverter with ACCPR-PLL-DVC**

## **System Configuration**



In the following, the superscript ‘’s’’ stands variables in system frame, while ‘’c’’ represents variables in control frame synchronized by PLL.

## **Current Control**

**Controller output**

(1)

**Modulator delay**

Pade1 formula is considered.

(2)

Where

**PR Controller**

Complex transfer function of PR controller in the -frame

(3)

Based on the frequency translation, complex transfer function of PR controller in the -frame

(4)

Equivalent transfer matrix of PR controller in the -frame

(5)

**Active damping**

(6)

## **LCL Filter**

(7)

(8)

## **Phase-Locked Loop (PLL)**

**PI Controller of PLL**

(9)

**Small-signal model of PLL**

(10)

**PLL effect**

(11)

## **DC-link**

Power balance constraint between dc and ac side can be given by

(12)

(13)

The dynamic equation of the dc-link voltage

(14)

With

The current reference can be given by

(15)

Linearizing (13) – (15)

(16)

(17)

(18)

Combining (16) and (17)

(19)

Inserting (19) to (18)

(20)

## **Substitution**

**Current controller**

Linearizing (1)

(21)

Substituting (11) to (21)

(22)

Substituting (20) to (22)

(23)

Rearranging (23)

(24)

(25)

(26)

(27)

Defined the modulation index at operating point

(28)

Substituting (19)(28) to (24)

(29)

Rearranging (29)

(30)

(31)

**LCL filter**

Linearizing (7)

(32)

Substituting (24) to (32)

(33)

Substituting (30) to (33)

(34)

## **Impedance model**

Rearranging (34)

(35)

(36)