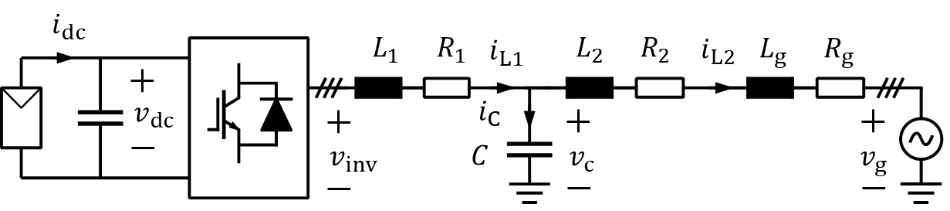
## **Impedance Model for Inverter with ACC-PLL-DVC**

## **System Configuration**



In the following, the superscript ‘’s’’ stands variables in system frame, while ‘’c’’ represents variables in control frame synchronized by PLL.

## **Impedance model**

## **Current Control**

**Controller output**

(1)

**Voltage feed forward (VFF) filter**

(2)

**Modulator delay**

Pade1 formula is considered.

(3)

Where

**PI Controller**

(4)

**Decoupling**

(5)

**Active damping**

(6)

## **LCL Filter**

(7)

(8)

## **Phase-Locked Loop (PLL)**

**PI Controller of PLL**

(9)

**Small-signal model of PLL**

(10)

**PLL effect**

(11)

(12)

(13)

(14)

## **Substitution**

Linearizing (1) and (7)

(15)

(16)

**expressed as a function of , or**

Power balance constraint between dc and ac side can be given by

(17)

(18)

The dynamic equation of the dc-link voltage

(19)

With

The current reference can be given by

(20)

Linearizing (18) – (20)

(21)

(22)

(23)

Combining (21) and (22)

(24)

**expressed as a function of and**

Inserting (24) to (23)

(25)

Inserting (8), (11) – (14), (24) and (25) to (15)

(26)

Rearranging

(27)

Where

(28)

(29)

(30)

(31)

Inserting (24) to (16)

(32)

Rearranging (32)

(33)

Inserting (27) to (33)

(34)

Rearranging (34)

(35)

PCC impedance

(36)