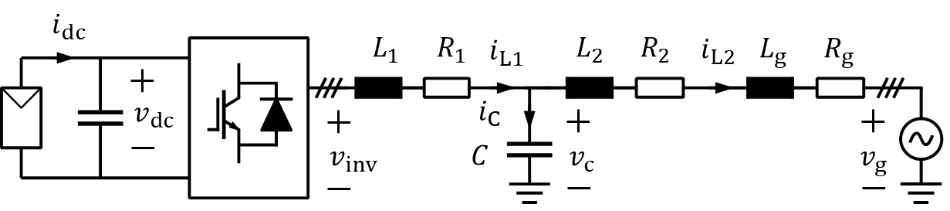
## **Impedance Model for Inverter with ACC-PLL-DVC-MBC**

## **System Configuration**



In the following, the superscript ‘’s’’ stands variables in system frame, while ‘’c’’ represents variables in control frame synchronized by PLL.

## **Impedance model**

## **Current Control**

**Controller output**

(1)

**Voltage feed forward (VFF) filter**

(2)

**Phase correction**

(3)

Where

**Modulator delay**

Pade1 formula is considered.

(4)

Where

**PI Controller**

(5)

**Decoupling**

(6)

**Active damping**

(7)

## **LCL Filter**

(8)

(9)

## **Phase-Locked Loop (PLL)**

**PI Controller of PLL**

(10)

**Small-signal model of PLL**

(11)

**PLL effect**

(12)

(13)

(14)

(15)

## **Substitution**

Linearizing (1) and (8)

(16)

(17)

**expressed as a function of , or is needed to solve (17)**

Power balance constraint between dc and ac side can be given by

(18)

(19)

The dynamic equation of the dc-link voltage

(20)

With

The current reference can be given by

(21)

Linearizing (19) – (21)

(22)

(23)

(24)

Combining (22) and (23)

(25)

**expressed as a function of and is needed to solve (10)**

Inserting (25) to (24)

(26)

Inserting (9), (12) – (15), (25) and (26) to (16)

(27)

Rearranging

(28)

Where

(29)

(30)

(31)

(32)

## **Solving (17)**

Inserting (25) to (17)

(33)

Rearranging (33)

(34)

Inserting (28) to (34)

(35)

Rearranging (35)

(36)