Technical Explanation 3L SKiiP28MLI07E3V1 Evaluation Inverter

Revision:	05
Issue date:	2018-12-12
Prepared by:	Ingo Rabl
Reviewed by:	-
Approved by:	Ulrich Nicolai

Keyword: 3L NPC Inverter, Multilevel, MiniSKiiP, Application Sample

This Technical Explanation (TE) describes the SEMIKRON three level (3L) evaluation inverter; a three phase inverter based on 3L NPC (Neutral Point Clamped) MiniSKiiP modules. The TE explains the functionality of the inverter and provides information on technical details as well as a step-by-step instruction of how to set the inverter in operation.
However, the information given may not be exhaustive and the responsibility for a proper and save setup remains with the user.

1. Introduction

SEMIKRON set up a three level (3L) evaluation inverter (in the following "EVA Inverter") for evaluation purposes. It is able to carry a maximum current of $100A_{RMS}$ at a DC-link voltage of up to $750V_{DC}$. Drivers and sensors (voltage, current, temperature) are on board. The user only needs to supply the EVA Inverter with power (DC-link voltage and auxiliary power) and PWM control signals. The inverter is designed to offer a high degree of self-protection: overvoltage, overcurrent, overtemperature and desaturation events are monitored and lead to a safe shut down.
However, the special feature is the implemented check for harmful switching patterns: a phase leg shoot through (all IGBTs of one phase leg switched on simultaneously) will be recognized and blocked by the driver. That way the inverter becomes very robust.

Figure 1: SEMIKRON Evaluation Inverter

The very compact EVA Inverter (w x l x h: 304mm x 320mm x 185mm; weight ca. 12kg) is dedicated to both universities and professional development engineers. It offers an easy way to learn about the basic functionality of a 3L inverter, to try different control algorithms, and to run performance tests without bearing the risk of destroying the device.

1.1 Ordering the EVA Inverter

The MiniSKiiP MLI EVA Inverter has a unique item number and can be ordered directly at SEMIKRON Sales (please contact your sales partner).
The order number is: **91 28 70 01**

2. Safety Instructions

The EVA Inverter bares risks when put in operation. Please carefully read and obey the following safety instructions to avoid harm or damage to persons or gear.

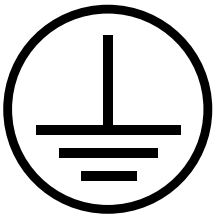
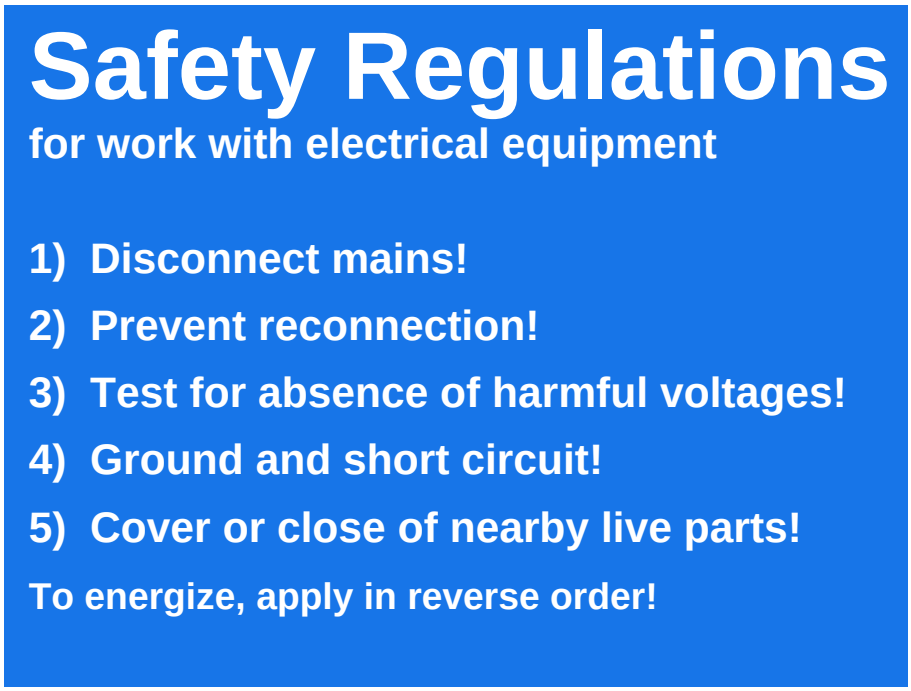
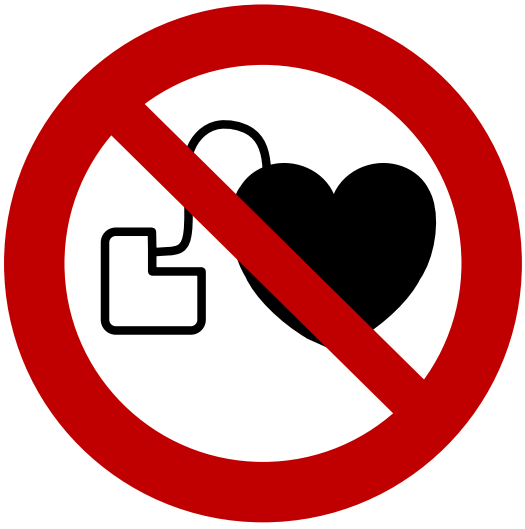
Table 1: Safety instructions	
	**In operation the EVA Inverter inherits high voltages that are dangerous to life!** **Only qualified personnel should work with the Kit.**
	**After disabling the DC supply the built-in resistors are able to reduce the DC-link voltage below 30V in a time greater than 3 minutes!**
	**Some parts of the EVA Inverter or connected devices (e.g. heatsink) may reach high temperatures that might lead to burns when touched.**
	**When connected to DC-link capacitors it must be made sure that the DC-link voltage is reduced to values below 30V before touching the system.**
	**The M5 mounting hole marked with the PE symbol provides a PE connecting point. The PE connection is mandatory! The minimum cross section of the PE connection is 16mm² (AWG5).**

Table 2: Safety regulations for work with electrical equipment



Please follow the safety regulations for working safe with the EVA Inverter.

Table 3: No access for people with active implanted cardiac devices!



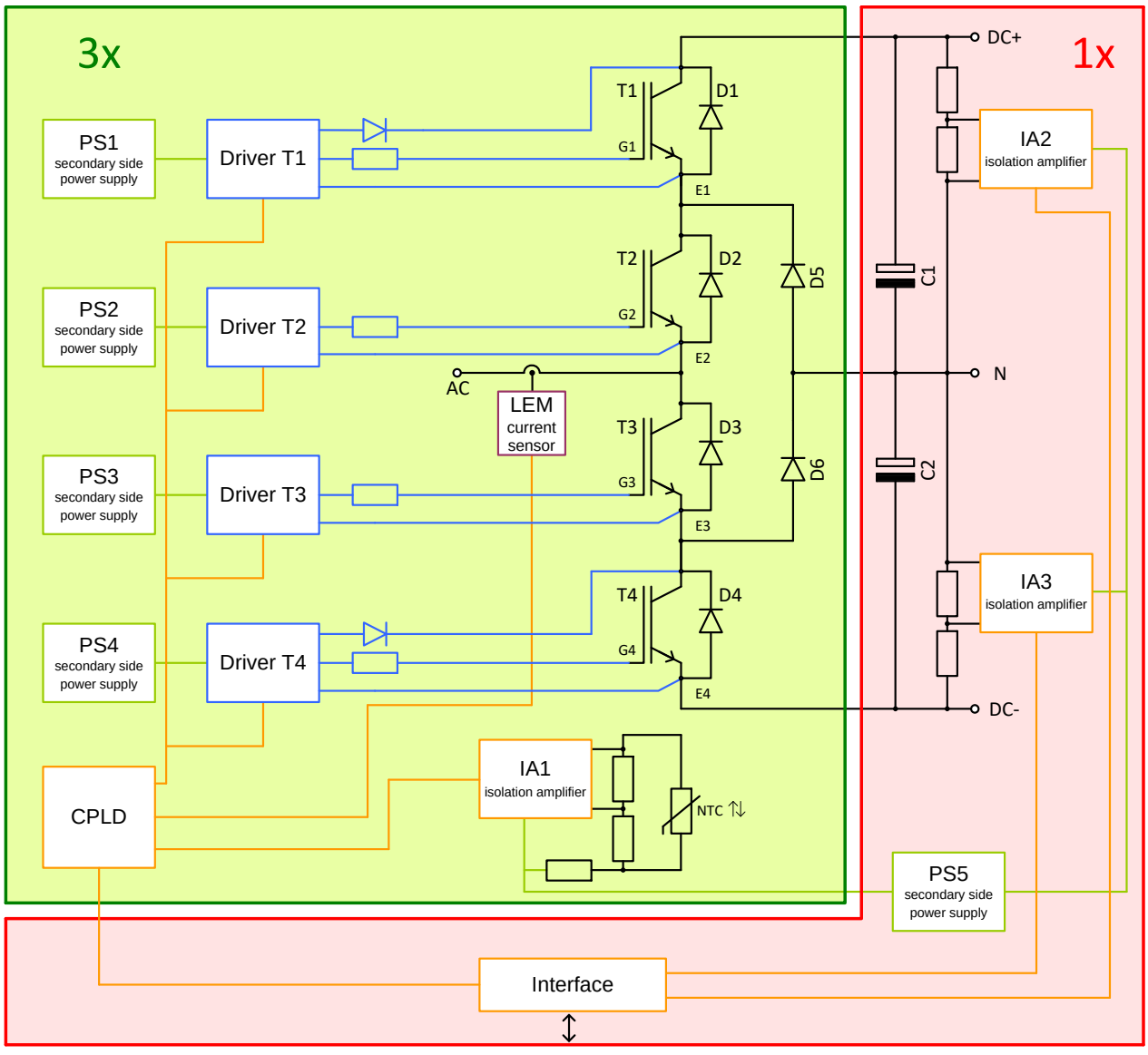
Operating the Application Sample may go along with electromagnetic fields which may disturb cardiac devices.
People with cardiac devices shall not operate the device.

3. Technical Data

3.1 EVA Inverter block diagram

The electrical block diagram in Figure 2 shows two parts: the red marked part (existing once) is responsible for the measurement of the DC-link voltages (upper and lower half), inherits the DC-link capacitors and the customer interface.

Figure 2: EVA Inverter block diagram



The green marked part exemplarily shows one of the three phase legs of the EVA Inverter (i.e. the green marked part exists three times). It inherits the power module and all required circuitry like driver circuits, galvanically isolated power supplies per IGBT, the current sensor, temperature measurement, and a programmable device (CPLD) that accounts for the correct switching pattern, correct switch-on and switch-off sequences, and the correct electrical limits (voltage, current, etc.).

3.2 Electrical and mechanical characteristics

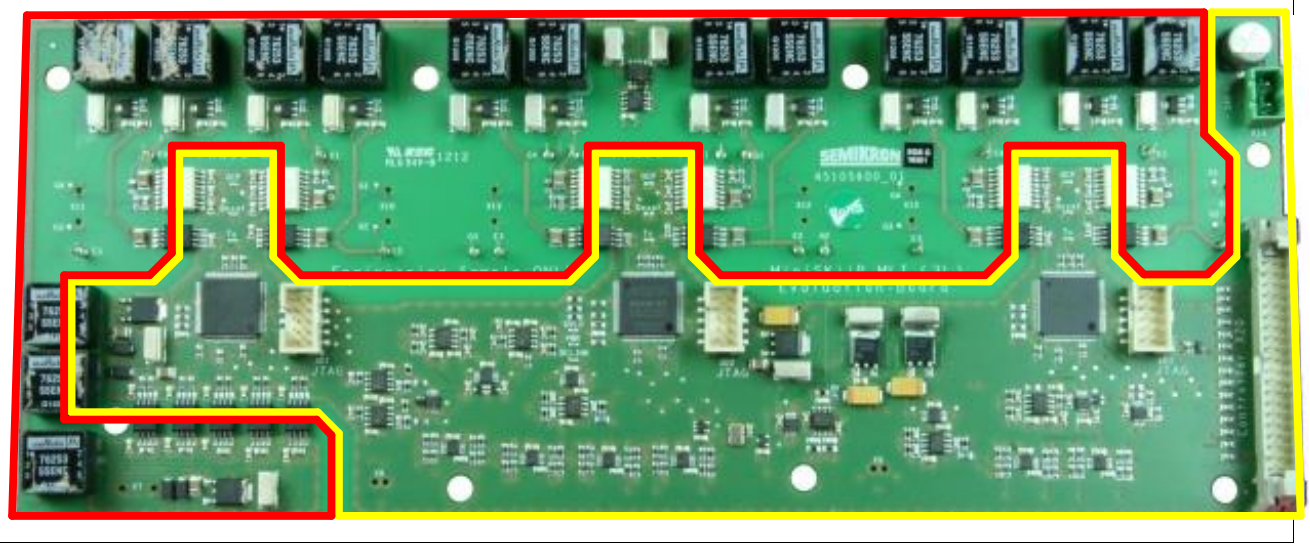
With regard to the requirement specification the EVA Inverter allows for operation within the following boundaries:

- Max. DC-link voltage — V_{DC} = 750V in total, max. 400V per individual DC-link half
- Max. AC voltage (line to line) — V_{AC} = 480V
- Max. AC current — I_{AC} = 100A_{RMS} (see chapter 6.2 for further restrictions)
- Max. Switching frequency — f_{sw} = 20kHz
- Ambient temperature — T_a = 0°C…40°C (see chapter 6.2 for further restrictions)
- Max. Heatsink temperature — T_s = 80°C
- Installation altitude — ≤ 2000m above sea level
- IP rating — IP 00
- Pollution Degree — PD 2
- Climatic conditions — 1K1, 2K2, 3K3 (3Z1)

Neglecting the above mentioned boundaries may lead to malfunction or damage of the EVA Inverter.

Concerning insulation coordination the EVA Inverter has been developed with respect to EN50178 and EN61800-5-1. An electrically protective separation is implemented between the customer interface (SELV – Safety Extra Low Voltage; framed in yellow color in Figure 3) and the high voltage connections (framed in red color in Figure 3). Basic insulation separates the heatsink from the high voltage connections.

Figure 3: Protective separation between high voltage (red marked area) and SELV (yellow marked area)



3.3 Integrated Functions

The EVA Inverter has many integrated functions to ensure safe operation and to provide a maximum feedback to the user.

3.3.1 AC phase current measurement / overcurrent protection (OCP)

The EVA Inverter measures the AC currents of all three phase legs with galvanically isolated current transducers. The measured values are available at the corresponding control interface pins (see chapter 4.3) and are also used for the onboard overcurrent protection. The overcurrent protection (OCP) level is set to 25% overload in regards to the nominal chip current ($150A_{nom} \cdot 1.25 = 187.5A \pm 8A$) where the EVA Inverter is switched off in order to protect the modules. Only affected modules are switched off. An overcurrent shutdown can be reset by clearing the fault latches (see chapter 4.3).

3.3.2 Module temperature measurement / overtemperature protection

The EVA Inverter measures the sensor temperatures of the three modules via galvanically isolated ΣΔ-optocouplers. The measured values are available at the corresponding control interface pins (see chapter 4.3).
At a sensor temperature of 115°C ± 4°C the affected module is switched off to avoid damage due to temperature overload. An overtemperature shutdown can be reset by clearing the fault latches (see chapter 4.3).

3.3.3 DC-link voltage measurement / overvoltage protection

The EVA Inverter measures the voltages of the two DC-link halves via galvanically isolated ΣΔ-optocouplers. The measured values are available at the corresponding control interface pins (see chapter 4.3).
As soon as one or both DC-link halves exceed a voltage of $465V_{DC} \pm 14V_{DC}$ the EVA Inverter is switched off to avoid damage to the chips due to dynamic voltage overshoots during switching.
However, the EVA Inverter is not able to reduce the DC-link voltage in lack of a brake chopper. SEMIKRON recommends to make sure that the DC-link voltage does not exceed $750V_{DC}$ at any time!
An overvoltage shutdown can be reset by clearing the fault latches (see chapter 4.3).

3.3.4 Additional protection circuitry – Desaturation Detection

To protect the EVA Inverter from damage due to hard short circuits, the IGBTs T1 and T4 of each phase are provided with a desaturation detection. Whenever one of the mentioned IGBTs is switched on and the forward voltage drop rises above 3V (normal operation voltage drop is around 1V), the respective IGBT is switched off by the driver immediately. Subsequently, the driver shuts down the malfunctioning phase and the DESAT LED flashes.
A desaturation event can be reset by clearing the fault latches (see chapter 4.3).

3.3.5 Additional protection circuitry – Active Clamping

To make the EVA Inverter even more robust, it comes with an active clamping circuitry at every IGBT of each phase. A low reverse current through the clamping diodes arises at a V_{CE} voltage across any IGBT of 430V…475V (depending on the ambient temperature and device tolerance). With rising V_{CE} voltage the reverse current also increases until the affected IGBT starts conducting at $V_{CE} \leq 600V$, which leaves a sufficient margin to the IGBT's blocking voltage of 650V.

3.3.6 CPLD

The driver board of the EVA Inverter comes with three CPLDs, one for each phase leg. The CPLDs supervise the switch-on and switch-off sequences of the IGBTs, the dead times, and the PWM sequences. All analogue signals are monitored and emergency procedures are implemented. That allows to identify if safe operating area is left.

Switching sequence: The software makes sure that inner switches (T2, T3) are switched on before outer switches (T1, T4) and outer switches are switched off before inner switches.

Dead times: All dead times are set to 3µs. If the user dead time is set to 5µs, the EVA Inverter will run with this dead time. If the user dead time is set to <3µs, the CPLDs will extend the dead times to the minimum value of 3µs. Dead times below 3µs are not possible.

PWM sequences: The PWM signals from the control interface have to take their way through the CPLDs where they are compared to a table of switching states (see Figure 4). If the delivered PWM pattern can be found in the area marked green in Figure 4 (allowed switching states), the pattern will be put through to the driver output stages. If the PWM pattern inherits a potentially destructive (Figure 4, marked orange) or destructive (Figure 4, marked red) state, the CPLD will shut down the phase leg with the correct switch-off sequence. As soon as the pattern is back to green, the phase leg resumes operation.

Figure 4: NPC switching states

T1	0	0	0	1	0	0	1	0	1	1	0	1	1	1	0	1
T2	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1
T3	0	0	1	0	1	1	0	0	0	1	0	1	0	1	1	1
T4	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1
state	**allowed**						**potentially destructive**					**destructive**				

Analogue signal processing: Every analogue measured signal is compared with the maximum allowed values (current, temperature, voltage) and the result is processed by the CPLDs. If any of these values leaves the defined safe operation area, the affected phase leg of the EVA Inverter will be shut down and a warning LED will be activated. To reactivate the device, the user needs to clear the fault latches after eliminating the root cause of the fault.

3.4 Driver Board Description

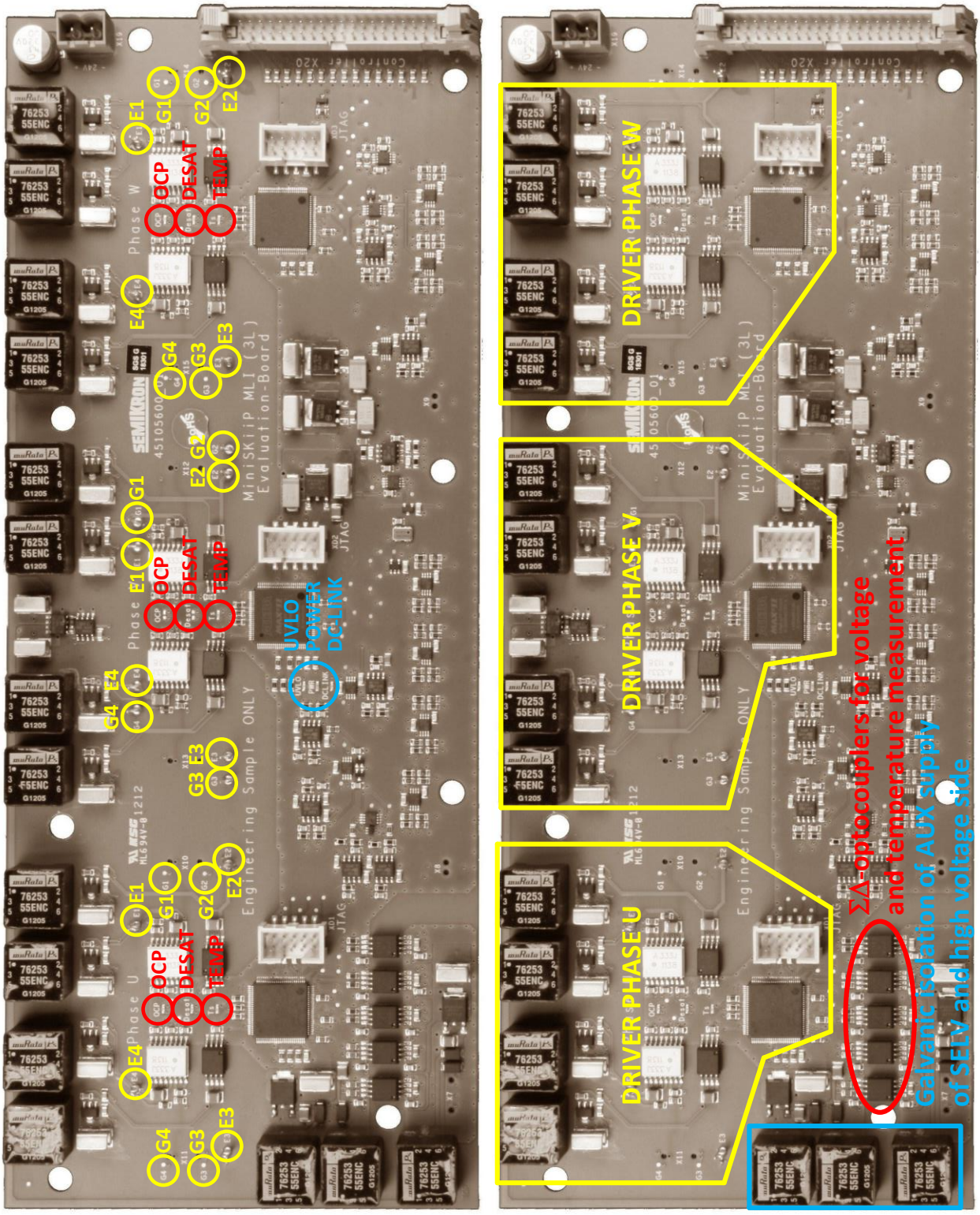
The driver board can be separated in several functional groups as shown in Figure 5 (right image): three more or less identical groups for the driver stages of phases U, V and W (marked yellow), five ΣΔ-optocouplers (two for the DC-link voltage and three for the temperature measurement) marked red, and the galvanic isolation (blue) represent the main functional groups. The board further inherits several voltage regulators and operational amplifiers for signal matching.

In the center of the driver board (Figure 5, left image) three LEDs (marked blue) inform the user about the status of the EVA Inverter. As soon as the auxiliary power supply is applied, the POWER LED flashes. The UVLO LED shows if the power supply has fallen below a critical value. Then the inverter is deactivated and the summing faults of all three phases go to 0V. The DC-link LED warns about too high DC-link voltage.

Per phase leg three LEDs (Figure 5, left image, marked red) show the status: OCP flashes when the current exceeds the limit, DESAT flashes in case of a desaturation event, and TEMP flashes when the module gets too hot.

Furthermore the driver board offers points of measurement for the gate and emitter potentials of all IGBTs of the three phase legs. The location of those points are highlighted in Figure 5 (left image, marked yellow).

Figure 5: Description driver board: points of measurement, status LEDs, functional groups



4. User Interface

4.1 Power connection

The location of the power terminals is shown in Figure 6. The signal names (U, V, W, DC+, N, DC-, PE) are also printed on the board / the heatsink.

Figure 6: Position of power terminals

Table 4: Mounting instruction for power terminals

	Mounting with:	Mounting torque	Cross-section area*
DC-link (DC+, N, DC-)	M6 cable shoe & M6 washer, snap ring, and nut	3.9Nm	35mm² or AWG2**
AC connection (U, V, W)	M6 cable shoe & M6 washer, snap ring, and nut	3.9Nm	35mm² or AWG2**
PE connection	M5 cable shoe & M5 bolt, snap ring, and washer	2.2Nm	16mm² or AWG5

*(at I_{AC} = 100A_{RMS} and $THD_{DC\text{-}supply}$ = 0%);
**(required cross-section area may differ depending on type of wire and allowed cable temperature)

In order to reduce mechanical stress on the power terminals, the user is asked to provide appropriate laying of the cables.

4.2 Supply Connection

The location of the supply plug is shown below (see Figure 7). The correct polarity is also printed on the PCB.
EVA Inverter operation with switched-off fans (V_{FAN} < 5V) is possible, however, SEMIKRON recommends a minimum fan supply of $5V_{DC}$ to guarantee a minimum air flow. Please refer to chapter 6.1 for further information about cooling limits.

Figure 7: Position of supply connectors

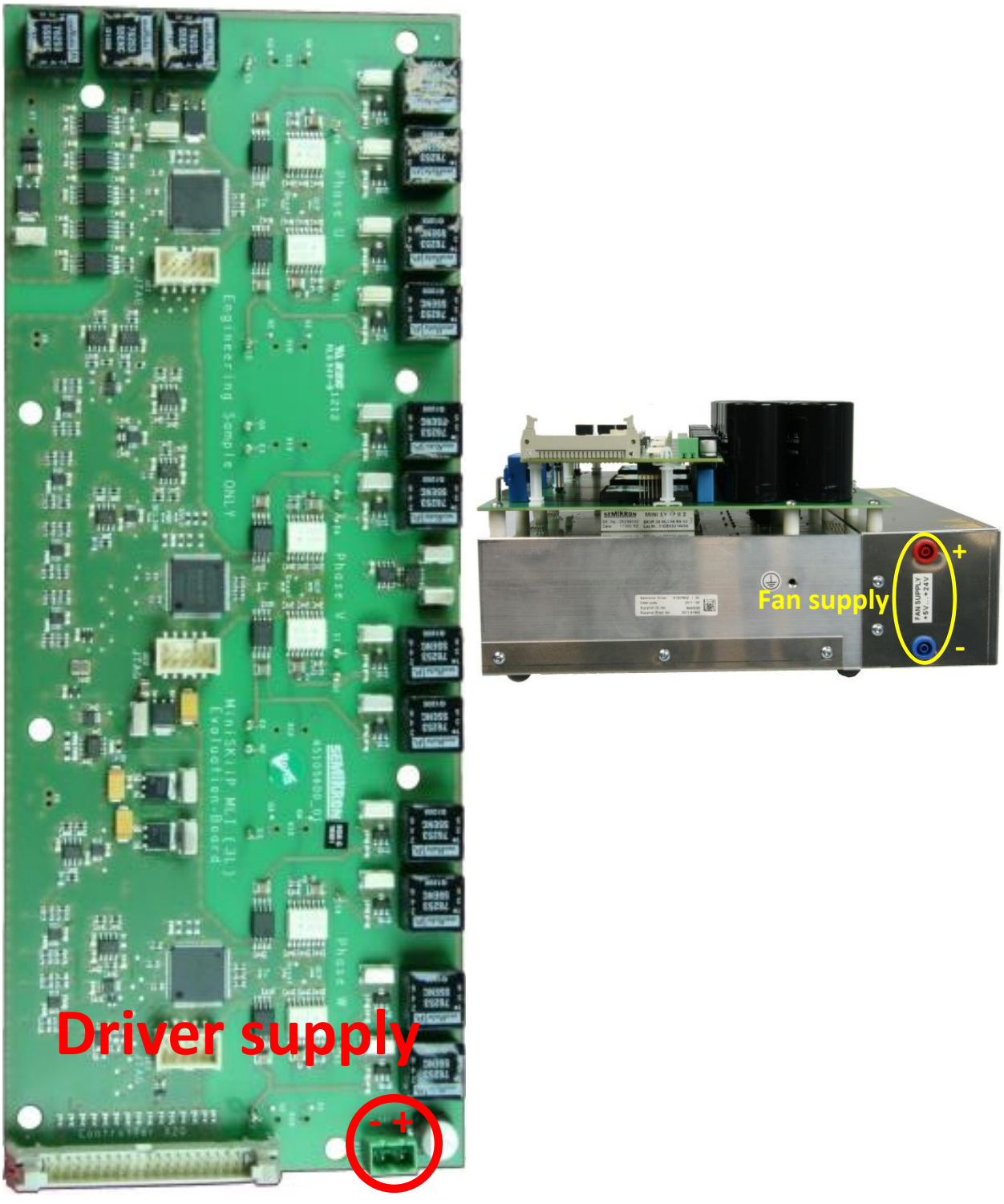


Table 5: Supply connection			
	Connector	**Voltage**	**Current**
Fan supply	4mm banana jack	$5V_{DC}$…$24V_{DC}$	max. 1A
Driver supply	Phoenix MSTB 2.5/2-ST-5.08	$24V_{DC}$ ±10%	max. 1A

4.3 Control interface

The control interface is a 40-pin ribbon cable plug located on the driver board (see Figure 8). The maximum allowed length of the ribbon cable is 1m, based on an input threshold voltage of $V_{ref\_in} = 15V$. At lower voltage levels correct functionality cannot be guaranteed. Higher levels do not increase the maximum cable length.
The user needs to make sure that the EVA Inverter is supplied with proper signals.

Figure 8: Position of the 40-pin control interface

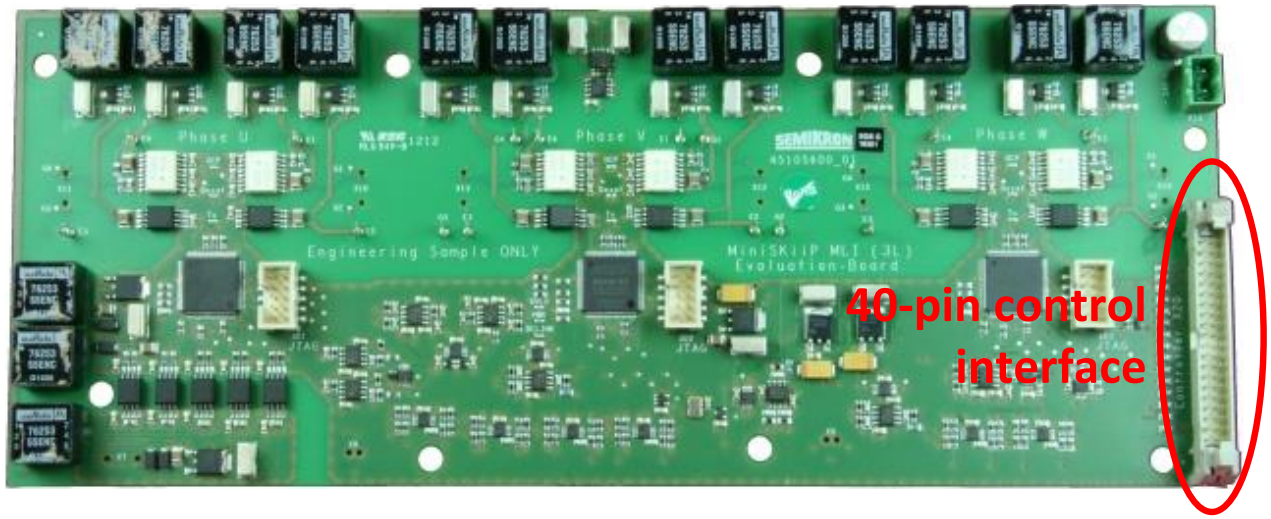


Table 6: Pin assignment of the 40-pin control interface			
Pin	**Signal name**	**Description**	**Voltage level**
1	GND	Ground	0V
2	T1_Phase_U	PWM pattern IGBT T1 of phase U	Off = 0V / On = Vref_In; R_{in} = 12kΩ / 1nF
3	T2_Phase_U	PWM pattern IGBT T2 of phase U	
4	T3_Phase_U	PWM pattern IGBT T3 of phase U	
5	T4_Phase_U	PWM pattern IGBT T4 of phase U	
6	GND	Ground	0V
7	T1_Phase_V	PWM pattern IGBT T1 of phase V	Off = 0V / On = Vref_In; R_{in} = 12kΩ / 1nF
8	T2_Phase_V	PWM pattern IGBT T2 of phase V	
9	T3_Phase_V	PWM pattern IGBT T3 of phase V	
10	T4_Phase_V	PWM pattern IGBT T4 of phase V	
11	GND	Ground	0V
12	T1_Phase_W	PWM pattern IGBT T1 of phase W	Off = 0V / On = Vref_In; R_{in} = 12kΩ / 1nF
13	T2_Phase_W	PWM pattern IGBT T2 of phase W	
14	T3_Phase_W	PWM pattern IGBT T3 of phase W	
15	T4_Phase_W	PWM pattern IGBT T4 of phase W	
16	GND	Ground	0V
17	RESERVE	Reserved pins, DO NOT CONNECT!	Reserved pins, DO NOT CONNECT!
18	RESERVE		
19	RESERVE		
20	_ΣFault_U	Summing fault phase U	Fault = 0V / ready-for-operation = Vref_In (Pull-Up to Vref_In on user side; $R_{pull-up}$ = 1kΩ)
21	_ΣFault_V	Summing fault phase V	
22	_ΣFault_W	Summing fault phase W	
23	_Clear_Faults	Input for resetting /clearing fault latches	Clear = 0V (Pull-Up to Vref_In on user side; $R_{pull-up}$ = 1kΩ; R_{in} = 12kΩ / 1nF)
24	_POR	Output of local power-on-reset	POR = 0V / ready = Vref_In (Pull-Up to Vref_In on user side; $R_{pull-up}$ = 1kΩ)
25	Vref_In	Setting of input threshold	Vref_In = +3.3…+24V; R_{in} = 12kΩ /1nF
26	GND	Ground	0V
27	GND	Ground	0V
28	$V_{DC,TOP}$	Voltage DC+ to N	0V…10V ≙ 0V…500V; I_{out} ≤ 5mA
29	$V_{DC,BOT}$	Voltage N to DC-	

30	GND	Ground	0V
31	$I_{AC,U}$	Phase current U	0V…±10V ≙ 0A…±187.5A; I_{out} ≤ ±5mA
32	GND	Ground	0V
33	$I_{AC,V}$	Phase current V	0V…±10V ≙ 0A…±187.5A; I_{out} ≤ ±5mA
34	GND	Ground	0V
35	$I_{AC,W}$	Phase current W	0V…±10V ≙ 0A…±187.5A; I_{out} ≤ ±5mA
36	GND	Ground	0V
37	$T_{sense,U}$	Temperature power module U	0V…10V ≙ 0°C…130°C; I_{out} ≤ 5mA
38	$T_{Sense,V}$	Temperature power module V	
39	$T_{Sense,W}$	Temperature power module W	
40	GND	Ground	0V

Shorting output signals to each other or to supply pins may damage the driver board!

TY_Phase_X (Y = 1..4, X = U, V, W)

Table 7: TY_Phase_X

Signal type	Signal function	Pin	Voltage levels
digital input	PWM pattern for IGBT Y of phase X	3-5, 7-10, 12-15	0V vs. GND (logic low) → off Vref_In vs. GND (logic high) → on

_ΣFault_X (X = U, V, W)

Table 8: _ΣFault_X

Signal type	Signal function	Pin	Voltage levels
digital output	Summing error of phase X	20-22	0V vs. GND (logic low) → fault state, phase X switches off regardless of input PWM Vref_In vs. GND (logic high) → EVA Inverter ready for operation

The maximum output current of _ΣFault_X may not exceed 50mA. As soon as the fault is no longer present, the fault state can be reset with the _Clear_Faults signal. The user needs to provide a 1kΩ pull-up resistor to Vref_In.

_Clear_Faults

Table 9: _Clear_Faults

Signal type	Signal function	Pin	Voltage levels
digital input	Reset input	23	0V vs. GND (logic low) → fault latches are cleared, no further errors can occur Vref_In vs. GND (logic high) → fault latches can be set

The user needs to provide a 1kΩ pull-up resistor to Vref_In. Dragging the _Clear_Faults input to GND clears the fault latches and resets the EVA Inverter to operational mode. As long as _Clear_Faults is set to 0V, the inverter is operational, but without protection!
ATTENTION: The EVA Inverter can be operated with permanent connection of _Clear_Faults to GND. If this mode is chosen the inverter will not have any protection (temperature, current, etc.) at all!
SEMIKRON recommends not to use this mode.

_POR

Table 10: _POR			
Signal type	**Signal function**	**Pin**	**Voltage levels**
digital output	Power-on-reset	24	0V vs. GND (logic low) → power-on reset, EVA Inverter not yet ready for operation Vref_In vs. GND (logic high) → EVA Inverter ready for operation

The maximum output current of _POR may not exceed 50mA. The user needs to provide a 1kΩ pull-up resistor to Vref_In.

Vref_In

Table 11: Vref_In			
Signal type	**Signal function**	**Pin**	**Voltage levels**
reference input	Setting of the logic high voltage level	25	+3.3V ≤ Vref_In ≤ +24V

Vref_In is to be chosen by the user; it is the voltage value for the logic high level. It may be chosen between 3.3V and 24V vs. GND. The voltage level of Vref_In is the level that is set for all digital high levels of input and output signals.
The tolerance thresholds of logic high and low level are set according to Vref_In as follows:

- $0V < V_{I/O} < \frac{1}{3}$ Vref_In → logic **low** level
- $\frac{2}{3}$Vref_In $< V_{I/O} <$ Vref_In → logic **high** level

($V_{I/O}$ stands for the voltage of the digital input or output signals.)

SEMIKRON recommends high values for high immunity.

$V_{DC,XXX}$ (XXX = TOP, BOT)

Table 12: $V_{DC,XXX}$			
Signal type	**Signal function**	**Pin**	**Voltage levels**
analogue output	Voltage measurement of DC-link half TOP / BOT	28, 29	0V vs. GND → 0V DC+ vs. N / 0V N vs. DC- 10V vs. GND → 500V DC+ vs. N / 500V N vs. DC- Linear gradient between 0V (0V) and 10V (500V)

The maximum output current of $V_{DC,XXX}$ may not exceed 5mA.
The tolerance of the voltage measurement is ±2% with regard to the maximum measurable voltage of $500V_{DC}$ at an ambient temperature of 25°C. The additional temperature dependent tolerance is ±0.85% at an ambient temperature of 0°C. The overvoltage protection intervenes at $465V_{DC}$ $\pm 14V_{DC}$. This refers to 9.3V at the corresponding control interface pins.

$I_{AC,X}$ (X = U, V, W)

Table 13: $I_{AC,X}$			
Signal type	**Signal function**	**Pin**	**Voltage levels**
analogue output	Current measurement of phase X	31, 33, 35	±0V vs. GND → ±0A at phase U/V/W ±10V vs. GND → ±187.5A at phase U/V/W Linear gradient between 0V and ±10V (±187.5A)

The maximum output current of $I_{AC,X}$ may not exceed ±5mA.
A positive measurement of the current refers to a positive technical current; a positive technical current represents the current flow away from the EVA Inverter towards the load.
The tolerance of the current measurement is ±3% with regard to the peak current of ±187.5A at an ambient temperature of 25°C. The additional temperature dependent tolerance is ±1.25% at an ambient temperature of 0°C and linearly degrades to ±0.75% at an ambient temperature of 40°C. The overcurrent protection (OCP) trip level is ±187.5A. That refers to ±10V at the corresponding control interface pins.

$T_{Sense,X}$ (X = U, V, W)

Table 14: $T_{Sense,X}$			
Signal type	**Signal function**	**Pin**	**Voltage levels**
analogue output	Temperature measurement of module X	37-39	0V vs. GND → 0°C at sensor of module X 10V vs. GND → 130°C at sensor of module X Non-linear gradient between 0V (0°C) and 10V (130°C)

The maximum output current of $T_{Sense,X}$ may not exceed 5mA.
A ±0,3V measurement tolerance needs to be taken into account. That refers to ±4°C.
The non-linear temperature/voltage gradient is shown in Figure 9. Figure 10 exemplarily shows some temperatures and the according voltages at the corresponding control interface pins.

Figure 9: Temperature/voltage gradient of $T_{Sense,X}$ –measurement vs. sensor temperature

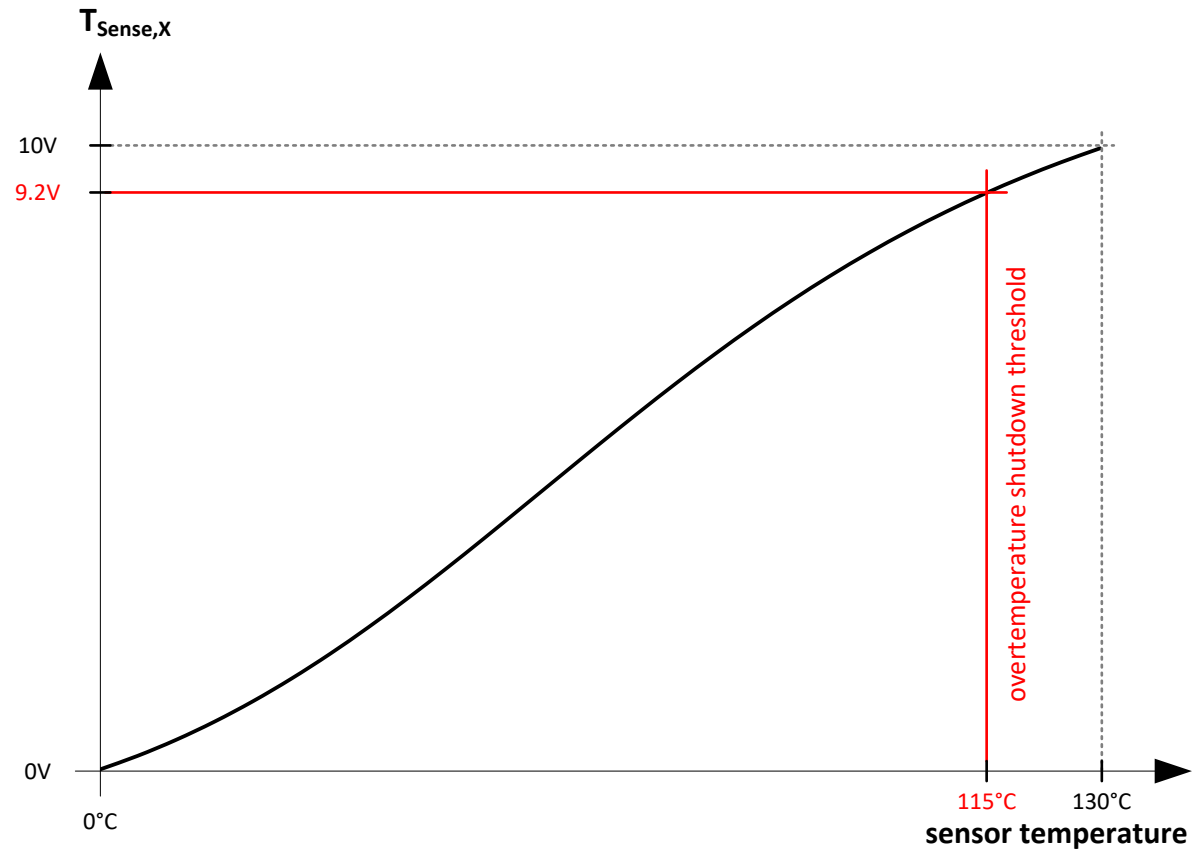


Figure 10: Sensor temperatures and according voltages

Sensor temperature	0°C	25°C	50°C	75°C	100°C	115°C	130°C
Measured voltage	0V	1.35V	3.65V	6.12V	8.25V	9.2V	10V

GND

Table 15: GND

Signal type	Signal function	Pin	Voltage levels
GND / ground	GND / ground	1, 6, 11, 16, 26, 27, 30, 32, 34, 36, 40	±0V, GND, ground

No difference has been made between the ground potentials of analogue and digital signals.

5. Getting Started

To set the EVA Inverter in operation only a view handles are necessary.

5.1 Connecting the EVA Inverter

For safe and proper operation the following connections need to be made:

- PE connection
- Fan supply
- Driver supply
- DC-link connection (DC+, N, DC-)
- AC connection (U, V, W)
- Logic interface connection

Figure 11: Connecting the EVA Inverter

Please refer to chapters 4.1 and 4.2 for cross section areas, mounting torques, and the correct voltage levels.

5.2 Minimum connection

- For operation at low loads the fan supply is not absolutely necessary. However, SEMIKRON recommends a minimum fan supply of $5V_{DC}$ during operation (please refer to chapter 6.1).
- If N is not externally controlled, the user will have to make sure that the DC-link halves stay voltage-balanced by using adequate PWM patterns.
- The minimum required connections in the logic interface (40pin connector) are pins 1-16 (PWM signals of all IGBTs and digital ground), pin 23 (_Clear_Faults, pull-up to pin 25, Vref_In mandatory), pin 25 (Vref_In), and pin 26 (digital ground). The other pins may be left out. However, SEMIKRON recommends the connection of all digital logic signals in order to be able to monitor errors.

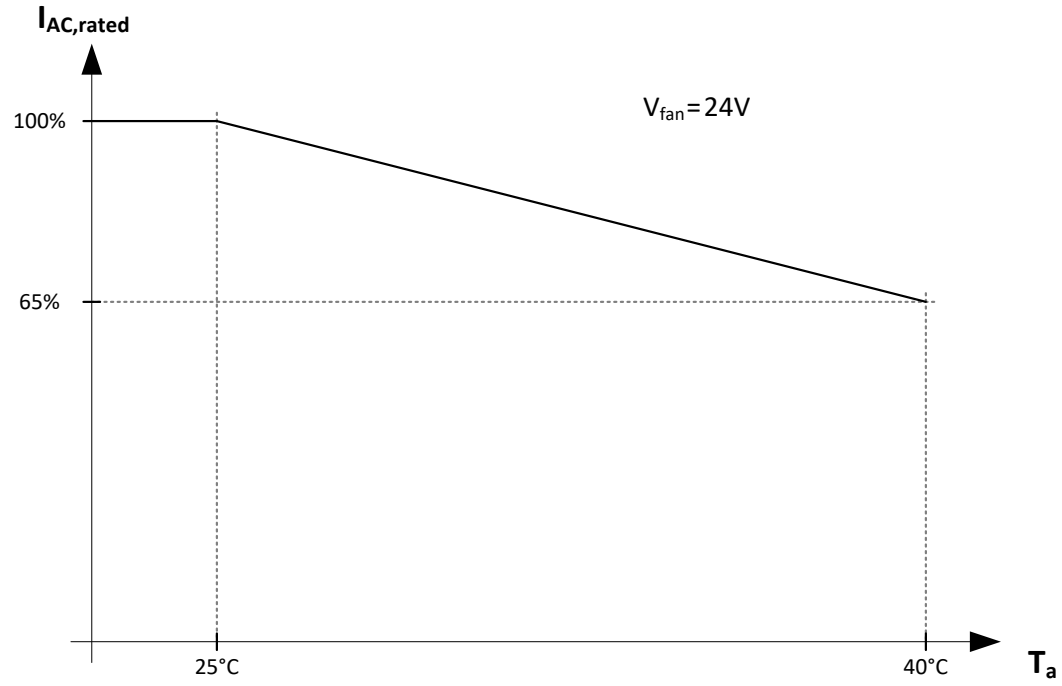
6. Design Limits

The design limits of the EVA Inverter allow for a maximum heatsink temperature of 80°C and an AC output current of $100A_{RMS}$ at certain operating conditions. The restrictions, maximum values, and derating curves are shown and explained below.

6.1 Cooling limits

The SEMIKRON standard heatsink P21 provides an $R_{th} = 0.06K/W$ at an airflow of 5m/s. To reach that flow the three fans need to provide an air volume of $85m^3/h$ each. That can be realized by operating the fans at $24V_{DC}$.
At a switching frequency of 3kHz, AC current of $100A_{RMS}$, and DC-link voltage of $750V_{DC}$ the power loss per module is approx. 300W. Given the thermal resistance of $R_{th} = 0.06K/W$ and a total power loss of 900W the temperature rise of the heatsink is 55K. At 25°C ambient temperature the heatsink reaches 80°C, which is the defined design limit.
Staying within the design limit requires a derating of the rated AC current that is related to the ambient temperature (T_a).

Figure 12: Derating of rated AC current vs. ambient temperature

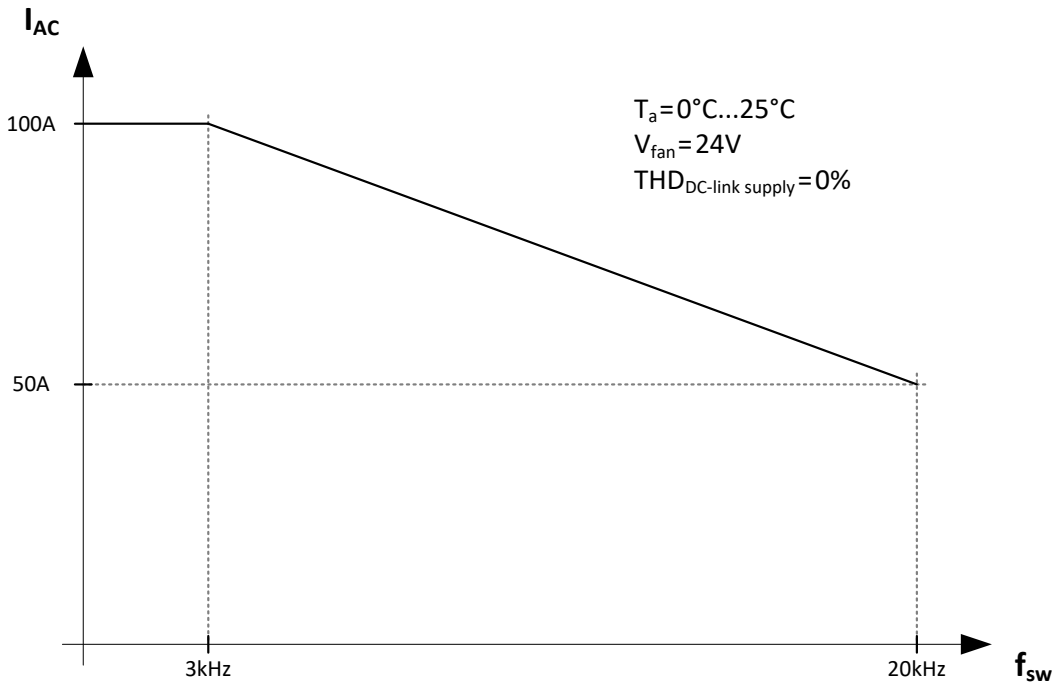


Please refer to chapter 6.2 for the AC current.
Example: The AC current at 20kHz and 25°C is $50A_{RMS}$. At an ambient temperature of 40°C the maximum rated AC current is 75% of $50A_{RMS}$ ⇒ $37,5A_{RMS}$.
It is also possible to reduce the supply voltage of the fans (voltage range 5V…24V). Please make sure that the heatsink temperature does not exceed 80°C at any time.

6.2 Output Current Limits

The maximum AC output current is $100A_{RMS}$. This value will be able to be reached at 0°C…25°C ambient temperature, if the fans are operated with $24V_{DC}$ at a switching frequency of 3kHz, and if the DC-link is supplied by pure DC current (no AC component; $THD_{DC\text{-link supply}} = 0\%$).
At higher switching frequencies the power modules produce higher losses so that the output AC current needs to be reduced. At 20kHz (maximum switching frequency) the limit is $50A_{RMS}$.
The derating curve for values between 3kHz and 20kHz is shown below.

Figure 13: Derating of AC current vs. switching frequency



Please refer to chapter 6.1 for higher ambient temperatures.
If the DC-link is fed with something else than DC current with THD = 0%, please refer to chapter 6.3 for derating curves.

6.3 DC-link Limits

The installed DC-link capacitors can handle AC current up to 9.3A per capacitor at 300Hz and up to 10.3A per capacitor at a switching frequency of 3kHz (61.8A total). A higher frequency does not increase the AC current capability.
If the EVA Inverter is operated at $100A_{RMS}$ output current (at $\cos\varphi = 1$), the corresponding AC load at the DC-link will be $60A_{RMS}$. To permit that operating point it is necessary to feed the DC-link without an additional AC current component to avoid damaging the capacitors, e.g. a DC power supply.

If the DC-link is fed by a B6 bridge rectifier, the DC capacitors will be exposed to an additional 300Hz AC current component. At $100A_{RMS}$ output current the 300Hz ripple current is 93A. There are two possibilities to handle the additional AC load: either by paralleling 10 additional DC capacitors of the same type (per half DC-link ⇒ 20 capacitors in total required) or by inserting a supply line inductance (L_{supply}).
Using an inductor with 100µH in the supply line reduces the AC ripple current to 70A, 1.6mH to 10A, which would require only one additional capacitor per DC-link half (see Figure 14). Moreover a combination of both methods may be considered.

At pure active power ($\cos\varphi = 1$), the 300Hz ripple is 93A, the less active and the more reactive power the EVA Inverter provides, the lower the 300Hz ripple becomes. At pure reactive power ($\cos\varphi = 1$), the 300Hz AC ripple current is approximately 3A. This value is dependent on the magnetic and resistive losses in the load and on the losses in the EVA Inverter (see Figure 15).

Figure 14: Dependency of DC-link supply ripple vs. DC-link supply line inductance

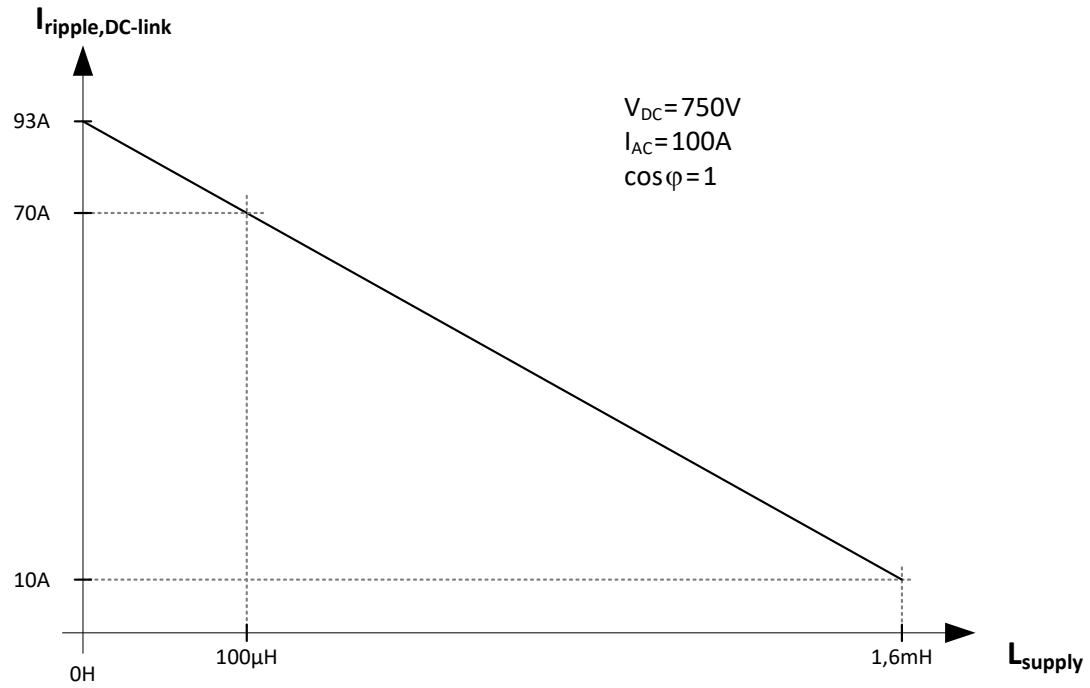
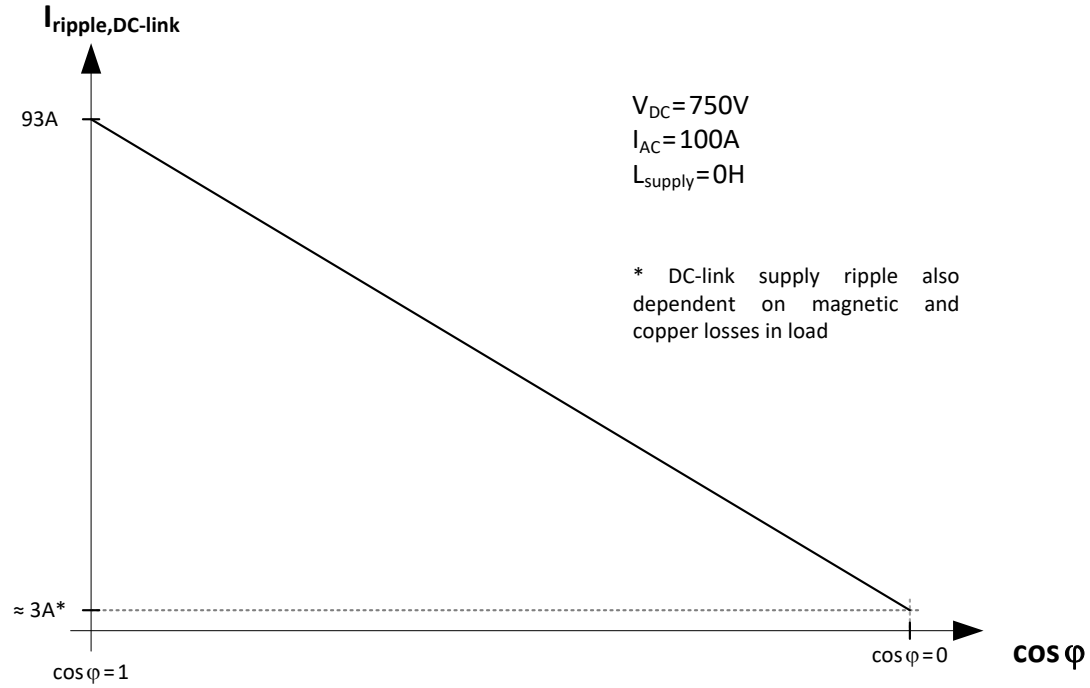


Figure 15: Dependency of DC-link supply ripple vs. power factor



Symbols and Terms

Letter Symbol	Term
2L	Two level
3L	Three level
CD	Clamping Diode
cos φ	Power factor
DC	Direct Current
DC+	Positive potential (terminal) of a direct voltage source
DC-	Negative potential (terminal) of a direct voltage source
DESAT	Desaturation
f_{SW}	Switching frequency
FWD	Free Wheeling Diode
IGBT	Insulated Gate Bipolar Transistor
I_{RMS}	AC terminal current
LED	Light Emitting Diode
N	Neutral potential (terminal) of a DC voltage source; midpoint between DC+ and DC-
NPC	Neutral Point Clamped
NTC	Temperature sensor with negative temperature coefficient
OCP	Overcurrent protection
PE	Power Earth
PWM	Pulse Width Modulation
R_{th}	Thermal resistance
SELV	Safety Extra Low Voltage
T_a	Ambient temperature
THD	Total Harmonic Distortion
T_s	Heatsink temperature
UVLO	Under-voltage lock-out
V_{DC}	Total supply voltage (DC+ to DC-)

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3
[3] I. Staudt, "3L NPC & TNPC Topology", SEMIKRON Application Note, AN-11001 - rev05, 2015

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SEMIKRON INTERNATIONAL GmbH
Sigmundstrasse 200, 90431 Nuremberg, Germany
Tel: +49 911 6559 6663, Fax: +49 911 6559 262
sales@semikron.com, www.semikron.com