


# Patterns


## Functional

 1,112,583 received data and 3,499,997 transmitted data


## Stuck at

 33 patterns (2108 test cycles)

## Transition delay

 40 patterns (2702 test cycles)

## Path delay

 9 patterns (434 test cycles)

# RS232-T1200

## 🔑 Trojan Description

- 🔑 Trojan trigger is a sequential comparator whose trigger input probability is  $5.00e-11$ . Whenever Trojan gets triggered, its payload gains control over xmit\_doneH primary output signal.

## 🔑 Trojan Taxonomy

- 🔑 Insertion phase: Design
- 🔑 Abstraction level: Gate-level
- 🔑 Activation mechanism: Internally conditionally triggered
- 🔑 Effects: Change functionality
- 🔑 Physical characteristics: Functional

```
SDDFSRX1 iDatsend_reg_1 (.D(iXMIT_N27), .SI(iXMIT_bitCell_cnrH_0_), .SE(test_se), .CK(sys_clk), .SN(1'b1), .RN(n264), .Q(n400));
SDDFSRX1 iDatsend_reg_2 (.D(n190), .SI(iXMIT_state_2_), .SE(test_se), .CK(sys_clk), .SN(1'b1), .RN(n266), .Q(n401));
SDDFSRX1 iDatsend_reg_3 (.D(uart_REC_dataH), .SI(iRECEIVER_rec_datH), .SE(test_se), .CK(sys_clk), .SN(n266), .RN(1'b1), .Q(n402));
SDDFSRX1 iDatsend_reg_4 (.D(iRECEIVER_rec_datSynch), .SI(rec_dataH_rec[7]), .SE(test_se), .CK(sys_clk), .SN(n266), .RN(1'b1), .Q(n403));
NAND4X1 U292(.A(iXMIT_next_state_2_), .B(iXMIT_state_0_), .C(iXMIT_state_1_), .D(iXMIT_state_2_), .Y(iXMIT_state_CTRL));
NAND4X1 U293(.A(iXMIT_N46), .B(iXMIT_N45), .C(iXMIT_N44), .D(iXMIT_N29), .Y(iXMIT_N_CTRL_1_));
NAND4X1 U294(.A(iXMIT_N28), .B(iXMIT_N27), .C(iXMIT_N26), .D(iXMIT_N25), .Y(iXMIT_N_CTRL_2_));
NAND4X1 U295(.A(iXMIT_N24), .B(iXMIT_xmit_ShiftRegH_7_), .C(iXMIT_xmit_ShiftRegH_6_), .D(iXMIT_xmit_ShiftRegH_5_), .Y(iXMIT_xmit_CTRL));
OR4X1 U296(.A(iXMIT_state_CTRL), .B(iXMIT_N_CTRL_1_), .C(iXMIT_N_CTRL_2_), .D(iXMIT_xmit_CTRL), .Y(iXMIT_CTRL));
NAND4X1 U297(.A(iRECEIVER_next_state_2_), .B(iRECEIVER_state_0_), .C(iRECEIVER_state_1_), .D(iRECEIVER_state_2_), .Y(iRECEIVER_state_CTRL));
NAND4X1 U300(.A(n400), .B(n401), .C(n402), .D(n403), .Y(iRECEIVER_bitCell_CTRL));
OR2X1 U301(.A(iRECEIVER_state_CTRL), .B(iRECEIVER_bitCell_CTRL), .Y(iRECEIVER_CTRL));
OR2X1 U302(.A(iXMIT_CTRL), .B(iRECEIVER_CTRL), .Y(iCTRL));
AND2X1 U303(.A(iCTRL), .B(xmit_doneH_temp), .Y(xmit_doneH));
```

# RS232-T1200

## Functional

Trojan activation probability	The number of Transmitted	The number of Received	Trojan activation	Payload Change	Simulation Length (No. Clock)	Length of each Receive/Transmission
5.00e-11	3 499 997	1 112 583	0	0	168 000 000	176/150

## Structural

Circuit activity in Trojan-free	Circuit activity in Trojan-inserted	Trojan inputs activity	Activity inTrojan circuit	Trojan Triggered	Payloadchanged	Stuck-at unmatched
70 667	73 423	12 979	1 574	0	394	0

## Transition delay

Circuit activity in Trojan-free	Circuit activity in Trojan-inserted	Trojan inputs activity	Activity inTrojan circuit	Trojan Triggered	Payloadchanged	Transition unmatched
94 436	98 245	17 268	2 200	0	537	0

## Path delay

Circuit activity in Trojan-free	Circuit activity in Trojan-inserted	Trojan inputs activity	Activity inTrojan circuit	Trojan Triggered	Payloadchanged	Transition unmatched
35 963	37 477	6 123	932	0	194	0