8M-BIT
SERIAL FLASH MEMORY WITH
DUAL AND QUAD SPI

winbond

Table of Contents

1. GENERAL DESCRIPTION 5
2. FEATURES 5
3. PACKAGE TYPES AND PIN CONFIGURATIONS 6
   - 3.1 Pin Configuration SOIC / VSOP 150 / 208-mil 6
   - 3.2 Pad Configuration WSON 6x5-mm / USON 2x3-mm 6
   - 3.3 Pin Configuration PDIP 300-mil 7
   - 3.4 Pin Description SOIC, VSOP, WSON, USON & PDIP 300-mil 7
   - 3.5 Ball Configuration TFBGA 8x6-mm 8
   - 3.6 Ball Description TFBGA 8x6-mm 8
4. PIN DESCRIPTIONS 9
   - 4.1 Chip Select (/CS) 9
   - 4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3) 9
   - 4.3 Write Protect (/WP) 9
   - 4.4 HOLD (/HOLD) 9
   - 4.5 Serial Clock (CLK) 9
5. BLOCK DIAGRAM 10
6. FUNCTIONAL DESCRIPTION 11
   - 6.1 SPI OPERATIONS 11
     - 6.1.1 Standard SPI Instructions 11
     - 6.1.2 Dual SPI Instructions 11
     - 6.1.3 Quad SPI Instructions 11
     - 6.1.4 Hold Function 11
   - 6.2 WRITE PROTECTION 12
     - 6.2.1 Write Protect Features 12
7. CONTROL AND STATUS REGISTERS 13
   - 7.1 STATUS REGISTER 13
     - 7.1.1 BUSY 13
     - 7.1.2 Write Enable Latch (WEL) 13
     - 7.1.3 Block Protect Bits (BP2, BP1, BP0) 13
     - 7.1.4 Top/Bottom Block Protect (TB) 13
     - 7.1.5 Sector/Block Protect (SEC) 13
     - 7.1.6 Complement Protect (CMP) 14
     - 7.1.7 Status Register Protect (SRP1, SRP0) 14
     - 7.1.8 Erase/Program Suspend Status (SUS) 14
     - 7.1.9 Security Register Lock Bits (LB3, LB2, LB1) 14
     - 7.1.10 Quad Enable (QE) 15
     - 7.1.11 Status Register Memory Protection (CMP = 0) 16
     - 7.1.12 Status Register Memory Protection (CMP = 1) 17

7.2 INSTRUCTIONS 18
7.2.1 Manufacturer and Device Identification 18
7.2.2 Instruction Set Table 1 (Erase, Program Instructions) 19
7.2.3 Instruction Set Table 2 (Read Instructions) 20
7.2.4 Instruction Set Table 3 (ID, Security Instructions) 21
7.2.5 Write Enable (06h) 22
7.2.6 Write Enable for Volatile Status Register (50h) 22
7.2.7 Write Disable (04h) 23
7.2.8 Read Status Register-1 (05h) and Read Status Register-2 (35h) 24
7.2.9 Write Status Register (01h) 24
7.2.10 Read Data (03h) 26
7.2.11 Fast Read (0Bh) 27
7.2.12 Fast Read Dual Output (3Bh) 28
7.2.13 Fast Read Quad Output (6Bh) 29
7.2.14 Fast Read Dual I/O (BBh) 30
7.2.15 Fast Read Quad I/O (EBh) 32
7.2.16 Word Read Quad I/O (E7h) 34
7.2.17 Octal Word Read Quad I/O (E3h) 36
7.2.18 Set Burst with Wrap (77h) 38
7.2.19 Continuous Read Mode Bits (M7-0) 39
7.2.20 Continuous Read Mode Reset (FFh or FFFFh) 39
7.2.21 Page Program (02h) 40
7.2.22 Quad Input Page Program (32h) 41
7.2.23 Sector Erase (20h) 42
7.2.24 32KB Block Erase (52h) 43
7.2.25 64KB Block Erase (D8h) 44
7.2.26 Chip Erase (C7h / 60h) 45
7.2.27 Erase / Program Suspend (75h) 46
7.2.28 Erase / Program Resume (7Ah) 47
7.2.29 Power-down (B9h) 48
7.2.30 Release Power-down / Device ID (ABh) 49
7.2.31 Read Manufacturer / Device ID (90h) 51
7.2.32 Read Manufacturer / Device ID Dual I/O (92h) 52
7.2.33 Read Manufacturer / Device ID Quad I/O (94h) 53
7.2.34 Read Unique ID Number (4Bh) 54
7.2.35 Read JEDEC ID (9Fh) 55
7.2.36 Read SFDP Register (5Ah) 56
7.2.37 Erase Security Registers (44h) 57
7.2.38 Program Security Registers (42h) 58
7.2.39 Read Security Registers (48h) 59
8. ELECTRICAL CHARACTERISTICS 60
8.1 Absolute Maximum Ratings 60

8.2 Operating Ranges 60
8.3 Power-up Timing and Write Inhibit Threshold 61
8.4 DC Electrical Characteristics 62
8.5 AC Measurement Conditions 63
8.6 AC Electrical Characteristics 64
8.7 AC Electrical Characteristics (cont'd) 65
8.8 Serial Output Timing 66
8.9 Serial Input Timing 66
8.10 HOLD Timing 66
8.11 WP Timing 66
9. PACKAGE SPECIFICATION 67
9.1 8-Pin SOIC 150-mil (Package Code SN) 67
9.2 8-Pin VSOP 150-mil (Package Code SV) 68
9.3 8-Pin SOIC 208-mil (Package Code SS) 69
9.4 8-Pin VSOP 208-mil (Package Code ST) 70
9.5 8-Pin PDIP 300-mil (Package Code DA) 71
9.6 8-Pad WSON 6x5mm (Package Code ZP) 72
9.7 8-Pad USON 2x3-mm (Package Code UX) 74
9.8 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 ball array) 75
9.9 24-Ball TFBGA 8x6-mm (Package Code TC, 6x4 ball array) 76
10. ORDERING INFORMATION 77
10.1 Valid Part Numbers and Top Side Marking 78
11. REVISION HISTORY 80

1. GENERAL DESCRIPTION

The W25Q80BV (8M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1µA for power-down.

The W25Q80BV array is organized into 4,096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q80BV has 256 erasable sectors and 16 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q80BV supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of SpiFlash Memories**
  - W25Q80BV: 8M-bit/1M-byte (1,048,576)
  - 256-byte per programmable page
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- **Highest Performance Serial Flash**
  - 104MHz Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Up to 8X that of ordinary Serial Flash
  - More than 100,000 erase/program cycles(1)
  - More than 20-year data retention
- **Efficient "Continuous Read Mode"**
  - Low Instruction overhead
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1µA Power-down current
  - -40°C to +85/105°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4/32/64K-bytes)
  - Program one to 256 bytes
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Top/Bottom, 4KB complement array protection
  - Lock-Down and OTP array protection
  - 64-Bit Unique Serial Number for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Byte Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging(2)**
  - 8-pin SOIC/VSOP 150/208-mil
  - 8-pad USON 2x3-mm
  - 8-pad WSON 6x5-mm
  - 8-pin PDIP 300-mil
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGD and other options

Note 1. More than 100,000 Block Erase/Program cycles for Industrial and Automotive temperature; more than 10,000 full chip Erase/Program cycles tested in compliance with AEC-Q100.
2. Some package types are special orders, please contact Winbond for ordering information.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25Q80BV is offered in an 8-pin SOIC 150-mil or 208-mil (package code SN & SS), an 8-pin VSOP 150-mil or 208-mil (package code SV & ST), an 8-pad WSON 6x5-mm (package code ZP), an 8-pad USON 2x3-mm (package code UX), an 8-pin PDIP 300-mil (package code DA) and a 24-ball 8x6-mm TFBGA (5x5 ball array - package code TB, 6x4 ball array – package code TC) as shown in Figure 1a-d respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pin Configuration SOIC / VSOP 150 / 208-mil

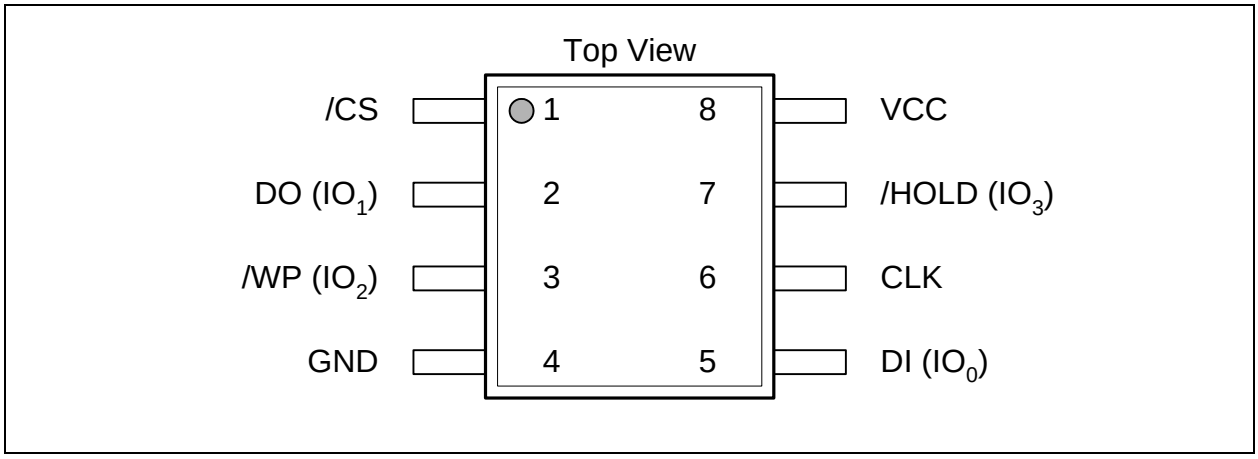

Figure 1a. W25Q80BV Pin Assignments, 8-pin SOIC / VSOP 150 / 208-mil (Package Code SN, SS, SV, ST)

3.2 Pad Configuration WSON 6x5-mm / USON 2x3-mm

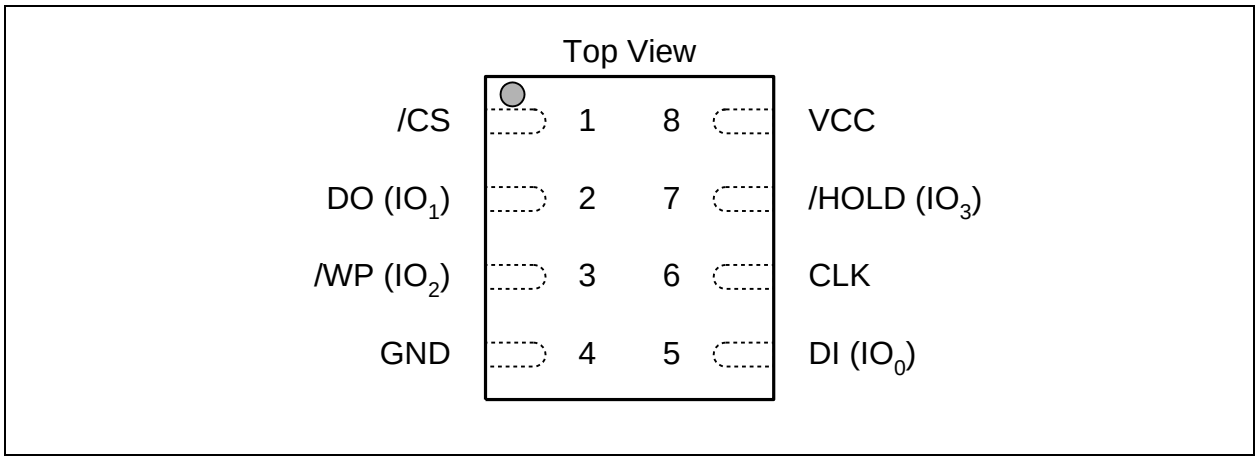

Figure 1b. W25Q80BV Pad Assignments, 8-pad WSON 6x5-mm, USON 2x3-mm (Package Code ZP, UX)

3.3 Pin Configuration PDIP 300-mil

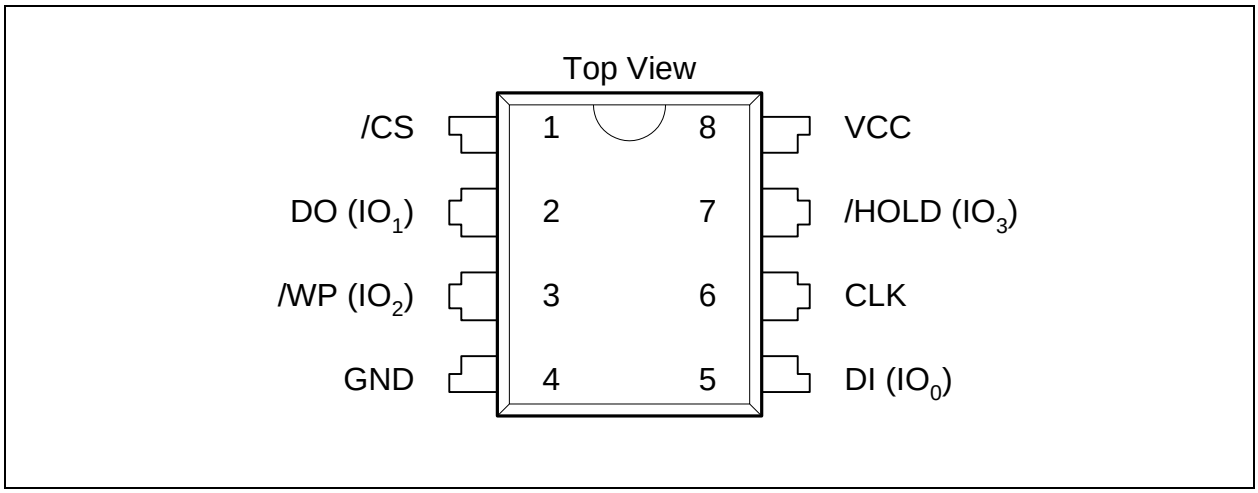

Figure 1c. W25Q80BV Pin Assignments, 8-pin PDIP (Package Code DA)

3.4 Pin Description SOIC, VSOP, WSON, USON & PDIP 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

3.5 Ball Configuration TFBGA 8x6-mm

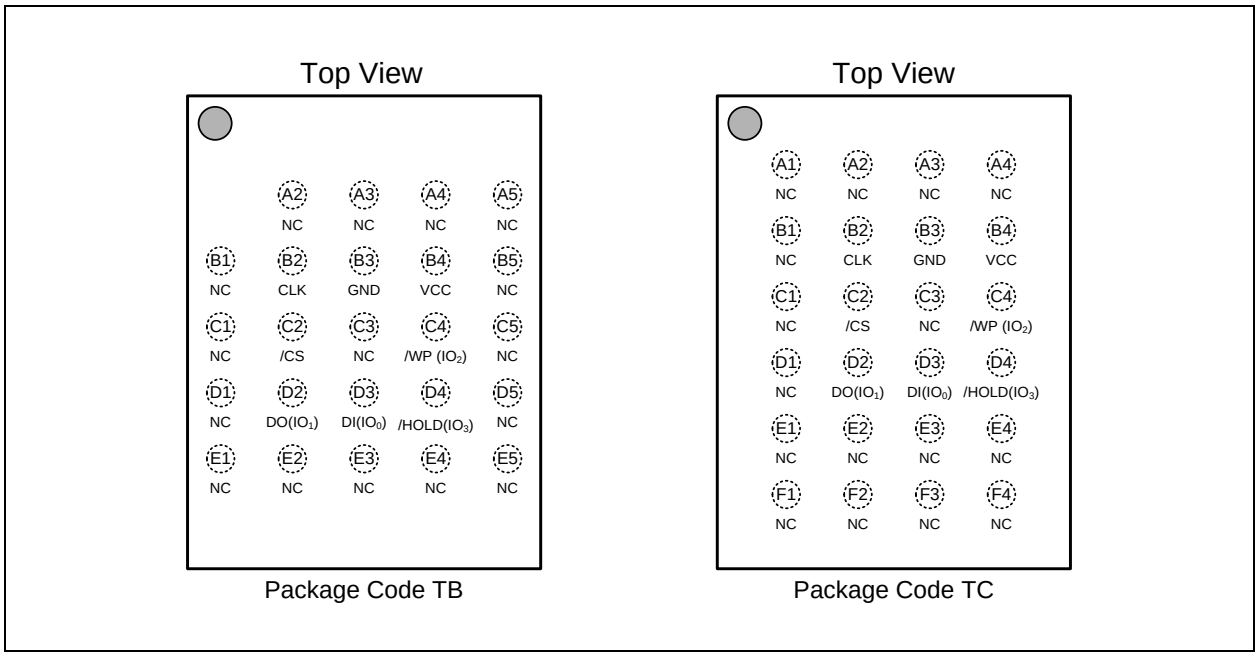

Figure 1d. W25Q80BV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB or TC)

3.6 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)*2
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)*1
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)*1
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)*2
Multiple	NC		No Connect

*1 IO0 and IO1 are used for Standard and Dual SPI instructions
*2 IO0 – IO3 are used for Quad SPI instructions

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 38). If needed a pull-up resister on /CS can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q80BV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See figure 1a-c for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See figure 1a-c for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

5. BLOCK DIAGRAM

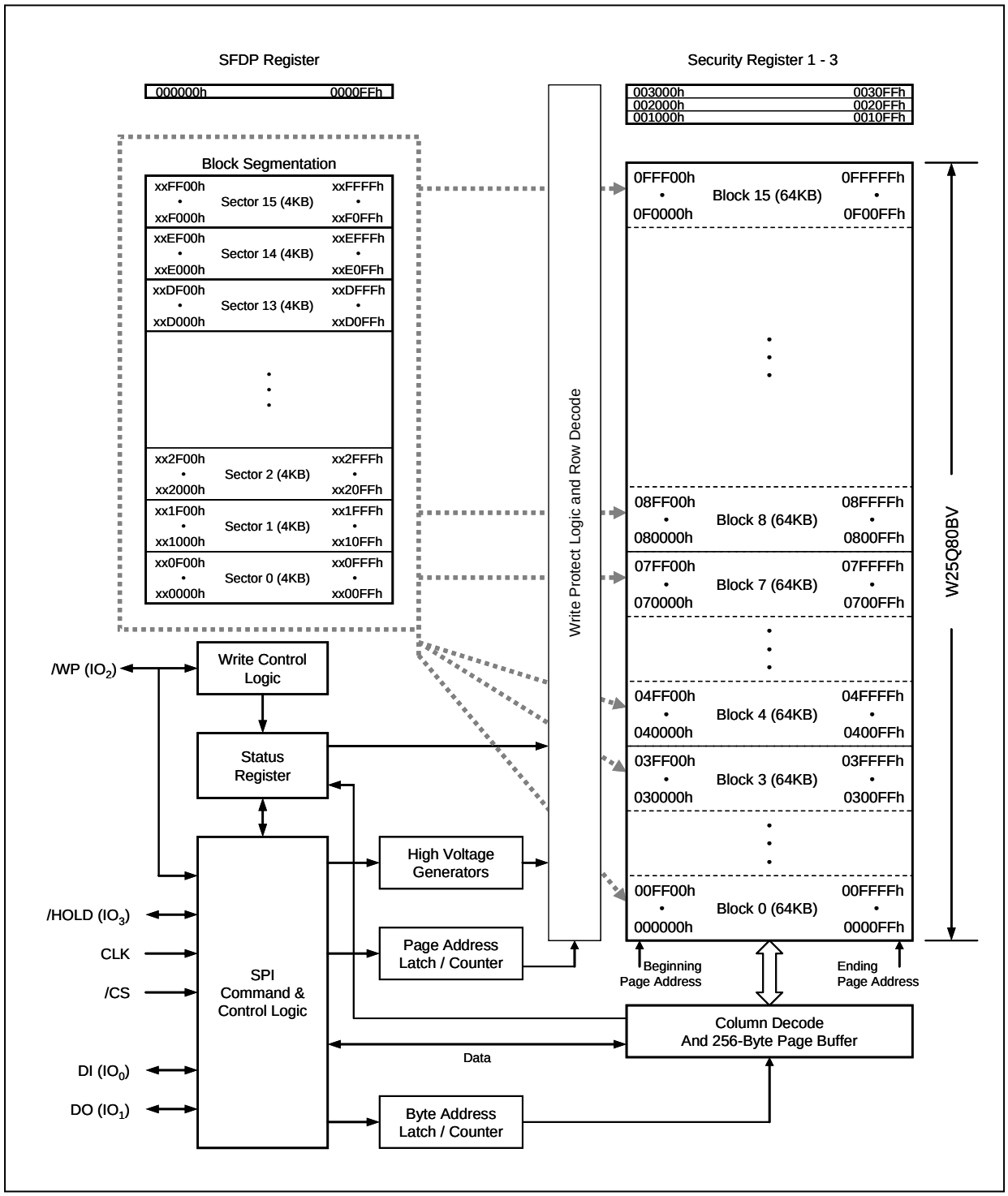

Figure 2. W25Q80BV Serial Flash Memory Block Diagram

分销商库存信息:		
WINBOND		
W25Q80BVSSIG	W25Q80BVSNIG	W25Q80BVDAIG
W25Q80BVZPIG		