
STM32
CubeMX

1. Description

1.1. Project

Project Name	program
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/19/2021

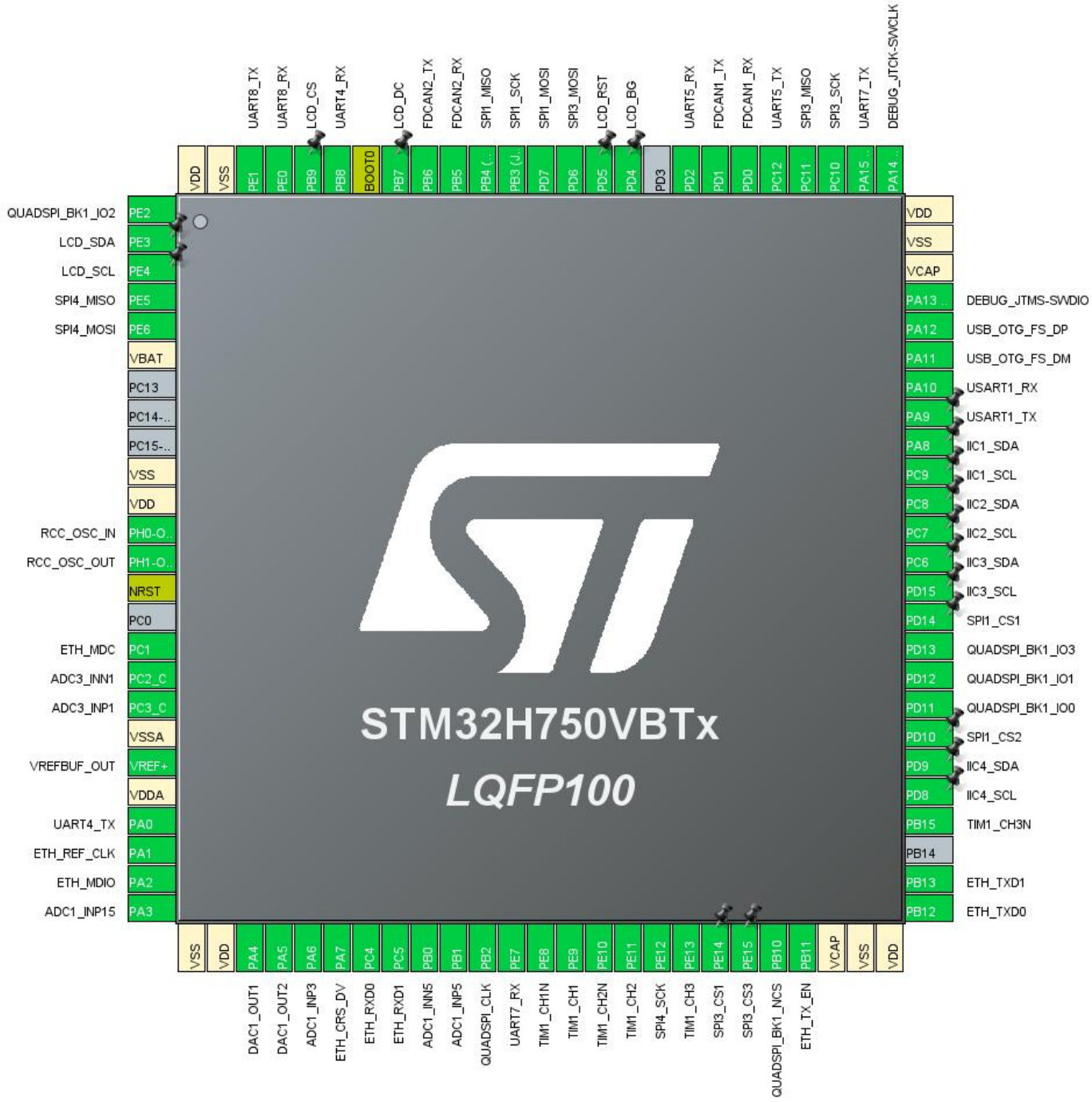
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

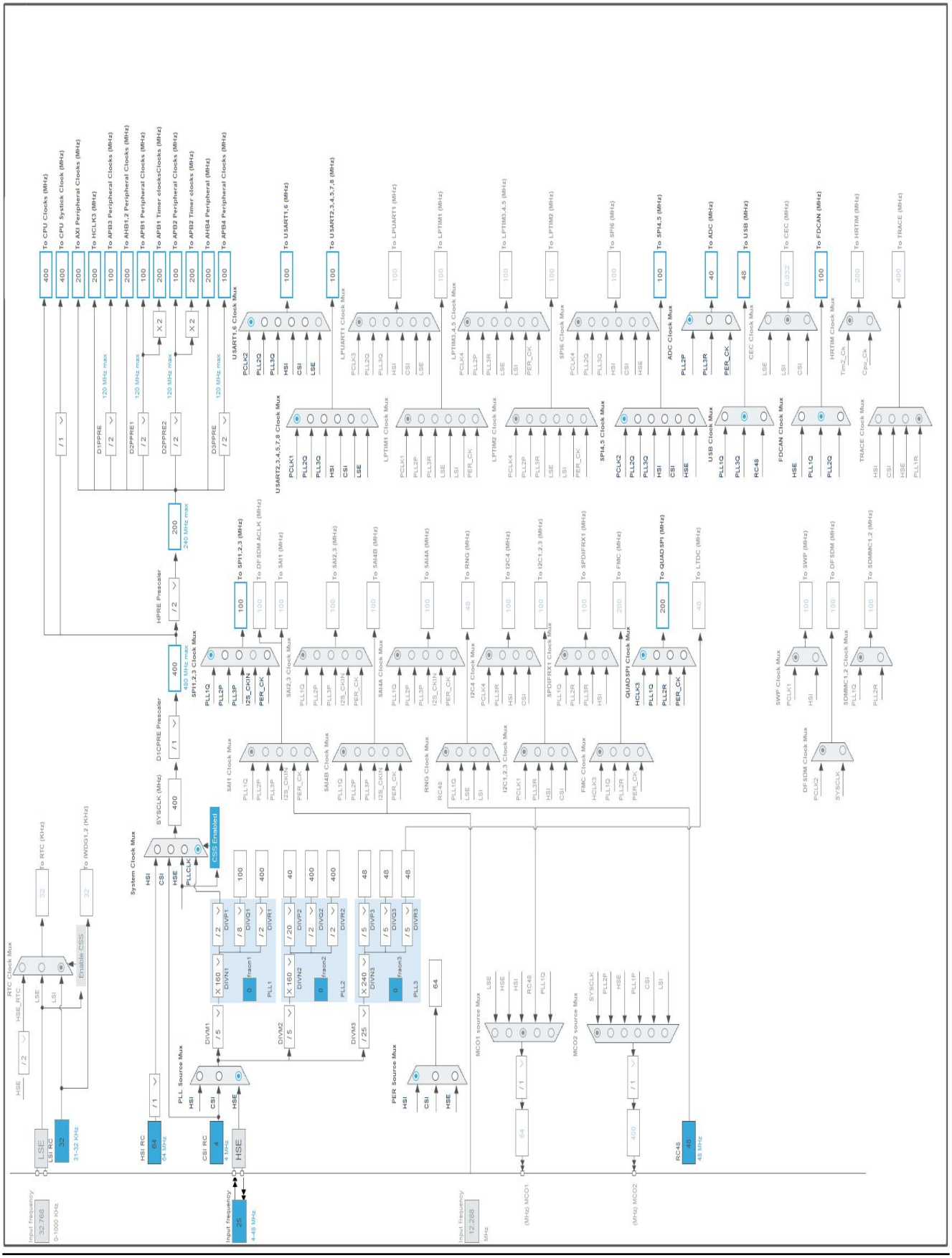
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
2	PE3 *	I/O	GPIO_Output	LCD_SDA
3	PE4 *	I/O	GPIO_Output	LCD_SCL
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	ETH_MDC	
17	PC2_C	I/O	ADC3_INN1	
18	PC3_C	I/O	ADC3_INP1	
19	VSSA	Power		
20	VREF+	MonoIO	VREFBUF_OUT	
21	VDDA	Power		
22	PA0	I/O	UART4_TX	
23	PA1	I/O	ETH_REF_CLK	
24	PA2	I/O	ETH_MDIO	
25	PA3	I/O	ADC1_INP15	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC1_OUT1	
29	PA5	I/O	DAC1_OUT2	
30	PA6	I/O	ADC1_INP3	
31	PA7	I/O	ETH_CRS_DV	
32	PC4	I/O	ETH_RXD0	
33	PC5	I/O	ETH_RXD1	
34	PB0	I/O	ADC1_INN5	
35	PB1	I/O	ADC1_INP5	
36	PB2	I/O	QUADSPI_CLK	
37	PE7	I/O	UART7_RX	
38	PE8	I/O	TIM1_CH1N	
39	PE9	I/O	TIM1_CH1	
40	PE10	I/O	TIM1_CH2N	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PE11	I/O	TIM1_CH2	
42	PE12	I/O	SPI4_SCK	
43	PE13	I/O	TIM1_CH3	
44	PE14 *	I/O	GPIO_Output	SPI3_CS1
45	PE15 *	I/O	GPIO_Output	SPI3_CS3
46	PB10	I/O	QUADSPI_BK1_NCS	
47	PB11	I/O	ETH_TX_EN	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
54	PB15	I/O	TIM1_CH3N	
55	PD8 *	I/O	GPIO_Output	IIC4_SCL
56	PD9 *	I/O	GPIO_Output	IIC4_SDA
57	PD10 *	I/O	GPIO_Output	SPI1_CS2
58	PD11	I/O	QUADSPI_BK1_IO0	
59	PD12	I/O	QUADSPI_BK1_IO1	
60	PD13	I/O	QUADSPI_BK1_IO3	
61	PD14 *	I/O	GPIO_Output	SPI1_CS1
62	PD15 *	I/O	GPIO_Output	IIC3_SCL
63	PC6 *	I/O	GPIO_Output	IIC3_SDA
64	PC7 *	I/O	GPIO_Output	IIC2_SCL
65	PC8 *	I/O	GPIO_Output	IIC2_SDA
66	PC9 *	I/O	GPIO_Output	IIC1_SCL
67	PA8 *	I/O	GPIO_Output	IIC1_SDA
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	UART7_TX	
78	PC10	I/O	SPI3_SCK	
79	PC11	I/O	SPI3_MISO	
80	PC12	I/O	UART5_TX	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
81	PD0	I/O	FDCAN1_RX	
82	PD1	I/O	FDCAN1_TX	
83	PD2	I/O	UART5_RX	
85	PD4 *	I/O	GPIO_Output	LCD_BG
86	PD5 *	I/O	GPIO_Output	LCD_RST
87	PD6	I/O	SPI3_MOSI	
88	PD7	I/O	SPI1_MOSI	
89	PB3 (JTDO/TRACESWO)	I/O	SPI1_SCK	
90	PB4 (NJTRST)	I/O	SPI1_MISO	
91	PB5	I/O	FDCAN2_RX	
92	PB6	I/O	FDCAN2_TX	
93	PB7 *	I/O	GPIO_Output	LCD_DC
94	BOOT0	Boot		
95	PB8	I/O	UART4_RX	
96	PB9 *	I/O	GPIO_Output	LCD_CS
97	PE0	I/O	UART8_RX	
98	PE1	I/O	UART8_TX	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	program
Project Folder	D:\Desktop\Files\iugandi\program
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x1000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_ADC3_Init	ADC3
5	MX_DAC1_Init	DAC1
6	MX_ETH_Init	ETH
7	MX_FDCAN1_Init	FDCAN1
8	MX_FDCAN2_Init	FDCAN2
9	MX_QUADSPI_Init	QUADSPI
10	MX_SPI1_Init	SPI1
11	MX_SPI3_Init	SPI3

Rank	Function Name	Peripheral Instance Name
12	MX_SPI4_Init	SPI4
13	MX_UART4_Init	UART4
14	MX_UART5_Init	UART5
15	MX_UART7_Init	UART7
16	MX_DMA_Init	DMA
17	MX_TIM1_Init	TIM1
18	MX_USB_DEVICE_Init	USB_DEVICE
19	MX_BDMA_Init	BDMA
20	MX_UART8_Init	UART8
21	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

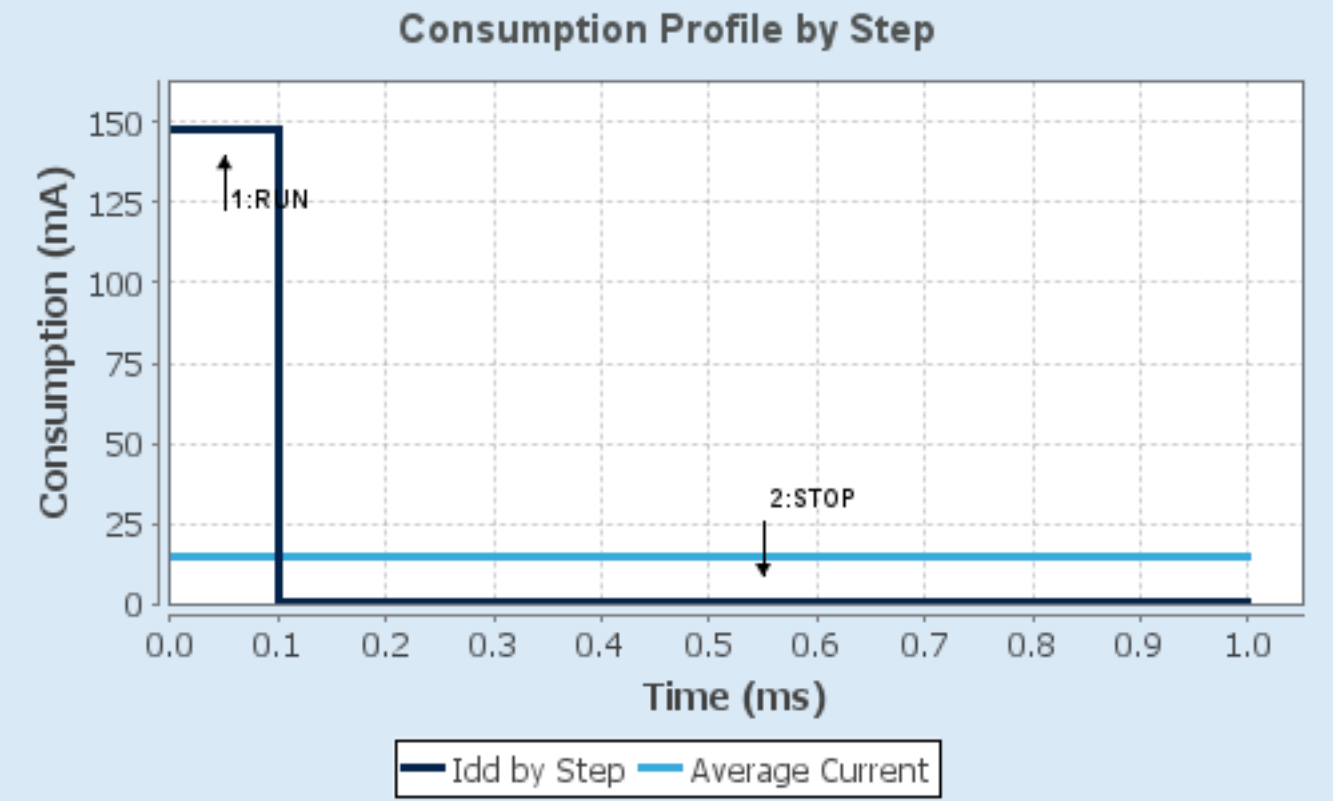
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.02	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN3: IN3 Single-ended

IN5: IN5 Differential

mode: IN15

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	**Channel 15 ***

Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC3

IN1: IN1 Differential

7.2.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. DAC1

OUT1 connected to: only external pin

OUT2 connected to: only external pin

7.3.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

DAC Out2 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

7.4. DEBUG

Debug: Serial Wire

7.5. ETH

Mode: RMII

7.5.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4

First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.6. FDCAN1

mode: Activated

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

7.7. FDCAN2

mode: Activated

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

7.8. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.8.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.9.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL3 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

7.10. SPI1

Mode: Full-Duplex Master

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.11. SPI3

Mode: Full-Duplex Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled

NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.12. SPI4

Mode: Full-Duplex Master

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.13. SYS

Timebase Source: TIM7

7.14. TIM1

Channel1: Output Compare CH1 CH1N

Channel2: Output Compare CH2 CH2N

Channel3: Output Compare CH3 CH3N

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
Output compare preload	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

7.15. UART4

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. UART5

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.17. UART7

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. UART8

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. USART1

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration

Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. USB_OTG_FS

Mode: Device_Only

7.20.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.21. VREFBUF

VREFBUF Mode: Internal voltage reference

7.21.1. Parameter Settings:

Voltage_Reference_Buffer_Settings:

Trimming Mode	Factory Trimming
Internal Voltage reference scale	SCALE 0: around 2.5 V

7.22. USB_DEVICE

Class For FS IP: Mass Storage Class

7.22.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

MSC_MEDIA_PACKET (Media I/O buffer Size)	512

7.22.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22314
PRODUCT_STRING (Product Identifier)	STM32 Mass Storage
CONFIGURATION_STRING (Configuration Identifier)	MSC Config
INTERFACE_STRING (Interface Identifier)	MSC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INN5	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC2_C	ADC3_INN1	Analog mode	No pull-up and no pull-down	n/a	
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN1	PD0	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN2	PB5	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15 (JTDI)	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
VREFBUF	VREF+	VREFBUF_OUT	n/a	n/a	n/a	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_SDA
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	LCD_SCL

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_CS1
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_CS3
	PD8	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC4_SCL
	PD9	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC4_SDA
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_CS2
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_CS1
	PD15	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC3_SCL
	PC6	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC3_SDA
	PC7	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC2_SCL
	PC8	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC2_SDA
	PC9	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC1_SCL
	PA8	GPIO_Output	**Output Open Drain ***	**Pull-up ***	**Very High ***	IIC1_SDA
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_BG
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_RST
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_DC
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LCD_CS

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	Low

ADC1: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. BDMA configuration

DMA request	Stream	Direction	Priority
ADC3	BDMA_Channel0	Peripheral To Memory	Low

ADC3: BDMA_Channel0 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	Disable
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
FDCAN1 interrupt 0	true	0	0
FDCAN2 interrupt 0	true	0	0
FDCAN1 interrupt 1	true	0	0
FDCAN2 interrupt 1	true	0	0
USART1 global interrupt	true	0	0
UART4 global interrupt	true	0	0
UART5 global interrupt	true	0	0
TIM7 global interrupt	true	15	0
UART7 global interrupt	true	0	0
UART8 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
ADC3 global interrupt	true	0	0
BDMA channel0 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
SPI1 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FDCAN calibration unit interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
FPU global interrupt	unused		
SPI4 global interrupt	unused		
QUADSPI global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

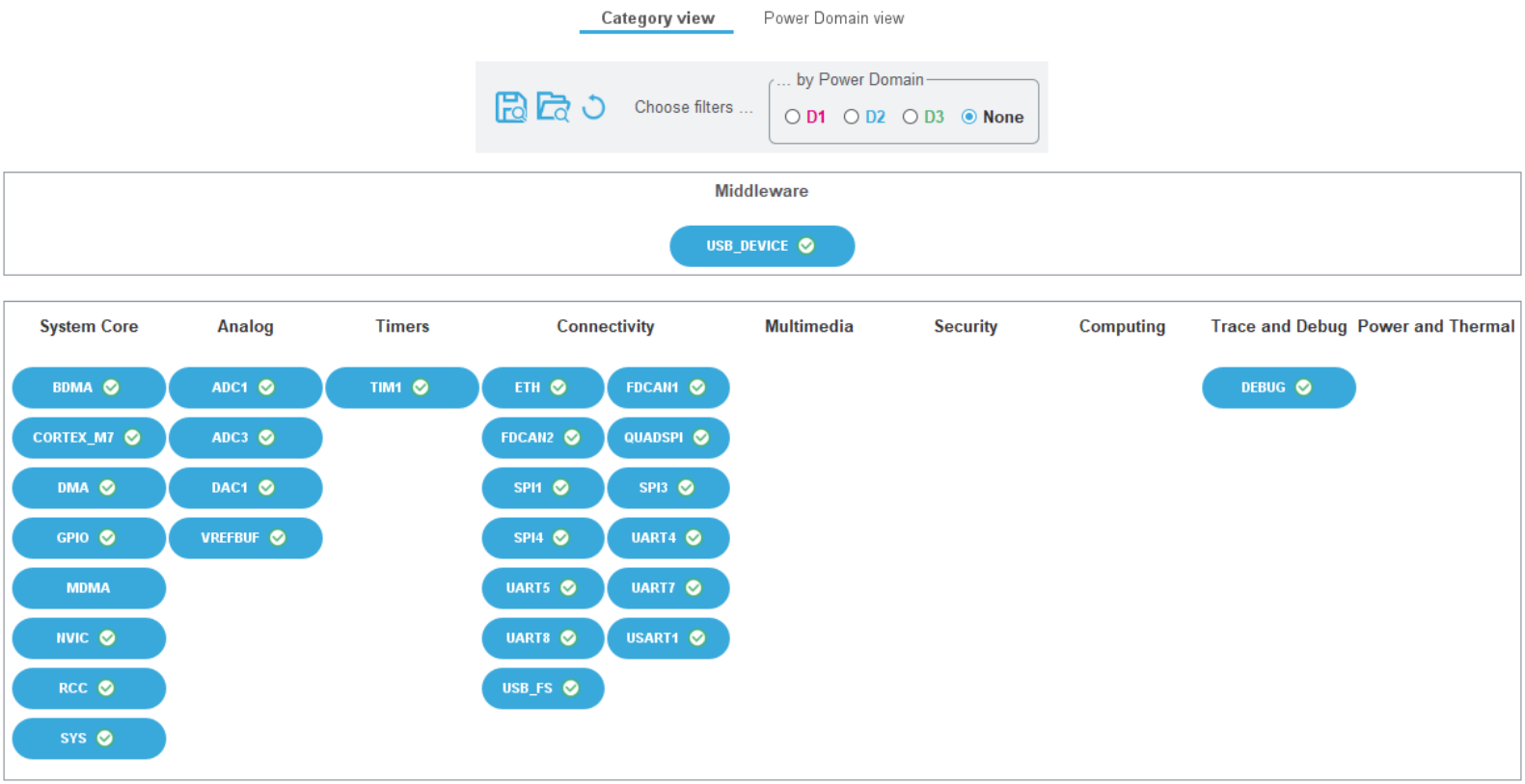
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	true
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
FDCAN1 interrupt 0	false	true	true
FDCAN2 interrupt 0	false	true	true
FDCAN1 interrupt 1	false	true	true
FDCAN2 interrupt 1	false	true	true
USART1 global interrupt	false	true	true
UART4 global interrupt	false	true	true
UART5 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
UART7 global interrupt	false	true	true
UART8 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
ADC3 global interrupt	false	true	true
BDMA channel0 global interrupt	false	true	true

*** User modified value**

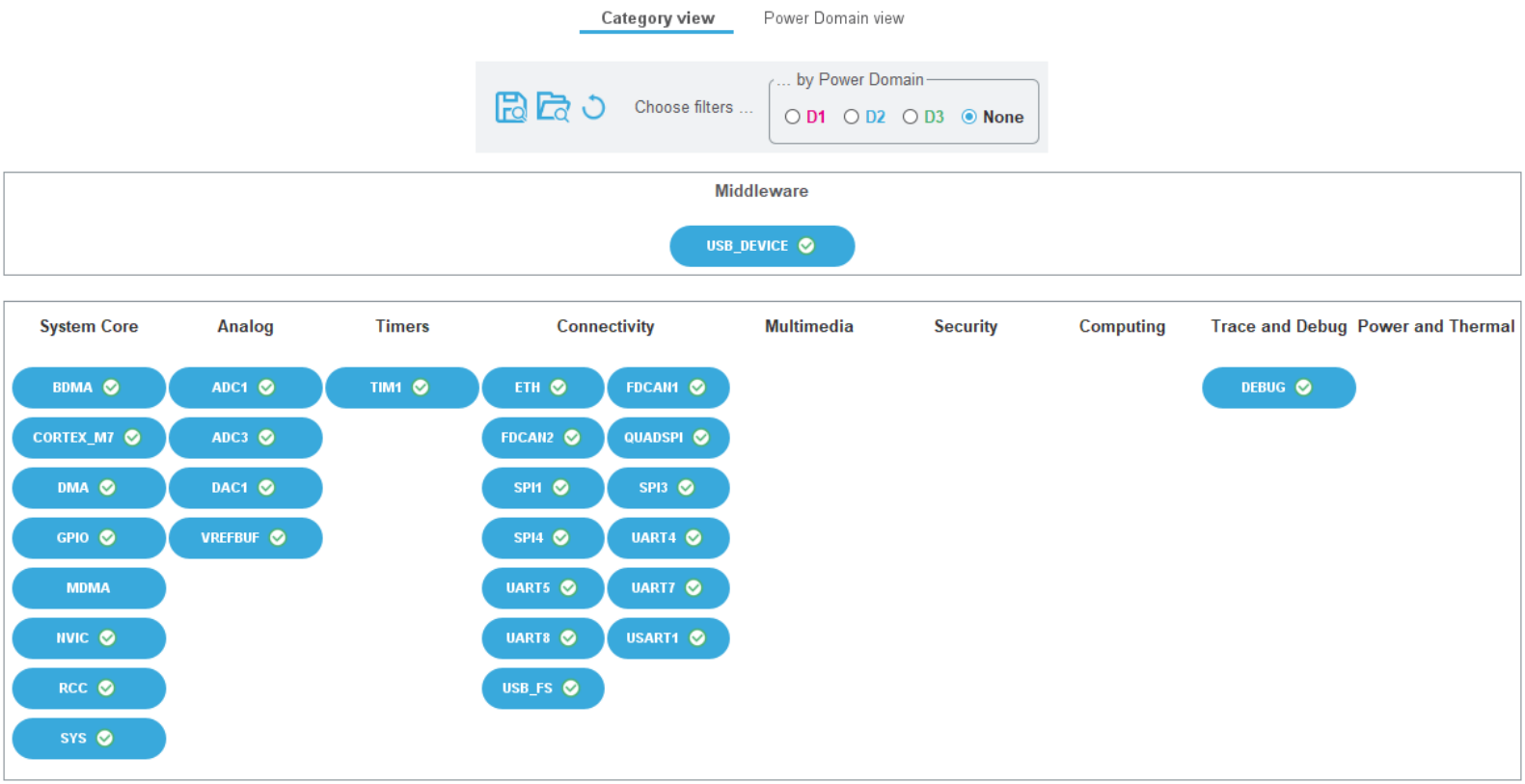
9. System Views

9.1. Category view

9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00496677.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00399555.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf

Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00514974.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf