4.1 a. Refer to control signals in Figure 4.2 in the text.

REGWRITE = 1,

MEMREAD = 0,

MEMWRITE = 0,

ALU Input Mux: selects register file data (0 –defined in Figure 4.15)

ALU Operation: AND (control format not defined)

Branch = 0

Register Input Mux: selects ALU (1 –defined in Figure 4.15)

b. The registers that perform a useful function are:

Program Counter (PC);

Instruction Memory;

Register File: both read ports, write port;

ALU;

PC + 4 Adder

c. The Branch Adder and Data Memory produce outputs that are not used. All resources produce outputs.

4.2 a. LWI leads the contents of a memory allocation that is the sum of two registry values. REGISTER, Mux, ALU, MEM.

b. nothing. (other reasonable answers are also okay)

c. nothing. (other reasonable answers are also okay)

4.5 lw+sw=25%+10%=35%

Addi + beq+lw+sw =20%+25%+25%+10%=80%

4.8 a. pipelined: 350 ps; non-pipelined: 250+350+150+300+200 = 1250 ps.

b. pipelined: 350 x 5 = 1750 ps; non-pipelined: 1250 ps.

c. ID; 300 ps. c. ID; 300 ps.

d. 30%（LD） + 20%(SW) = 50%

e. 40%（ALU） + 30%(LD) = 70%

f. cycle time:

single-cycle: 1250 ps.

multi-cycle: 350 ps.

pipelined: 350 ps.

execution time ratio:

single-cycle / pipelined = 1250 / 350 = 3.57

multi-cycle / pipelined = (20% x 5 + 80% x 4) = 4.2

execution time:

pipelined: 350 ps

single-cycle: 1250 ps

multi-cycle: 350 x 4.2 = 1470 ps (1400 is also okay)

NOTICE: ALU has no MEM stage, SW has no WB stage, BEQ has no WB (or MEM+WB) stage.