

# Digital Integrated Circuits

## Lab 1: Device Simulations

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# ***Outline***

- Lab Contents
- Report Requirements

# Models for DC Simulation

- ❑ Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 16nm bulk Si-MOSFETs and 10nm multi-gate (MG) FinFETs

- PTM link:  
<http://ptm.asu.edu/>
- Use the high-performance (HP) models
- For both n-channel and p-channel devices

**Predictive Technology Model**

**Introduction**  
**Latest Models**  
**Nano-CMOS**  
**Post-Silicon**  
**Interconnect**  
**Reliability**  
**Contact**

**LATEST MODELS**

Typical SPICE model files for each future generation are available here.

**Attention:** By using a **PTM** file, you agree to acknowledge both the URL.

**New!**  
**June 01, 2012:**  
PTM releases a new set of models for multi-gate technology (MG) FinFETs.  
Acknowledgement: PTM-MG is developed in collaboration with ASU.

Please start from [models](#) and [param.inc](#).

- 7nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 10nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 14nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 16nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 20nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)

The entire package is also available here: [PTM-MG](#)

November 15, 2008:  
PTM releases a new set of models for low-power applications (PTM LP), incorporating 16nm, 22nm, 32nm, and 45nm technology nodes.

- 16nm PTM LP model: [V2.1](#)
- 22nm PTM LP model: [V2.1](#)
- 32nm PTM LP model: [V2.1](#)
- 45nm PTM LP model: [V2.1](#)

September 30, 2008:  
PTM releases a new set of models for high-performance applications (PTM HP), incorporating 16nm, 22nm, 32nm, and 45nm technology nodes.

- 16nm PTM HP model: [V2.1](#)
- 22nm PTM HP model: [V2.1](#)
- 32nm PTM HP model: [V2.1](#)
- 45nm PTM HP model: [V2.1](#)

**ASU**

# *Simulation Settings*

- ❑  $L_g = 14\text{nm}$  for FinFETs while  $L_g = 16\text{nm}$  for bulk Si-MOSFETs
- ❑ Supply voltage ( $V_{DD}$ ) is  $0.65\text{V}$  for  $10\text{nm}$  FinFETs and  $0.7\text{V}$  for  $16\text{nm}$  bulk Si-MOSFETs
- ❑ Simulation temperature
  - $T = 25^\circ\text{C}$
  - $T = 90^\circ\text{C}$

# ***Task 1: Plot I-V Curves***

□ For bulk Si-MOSFETs and FinFETs

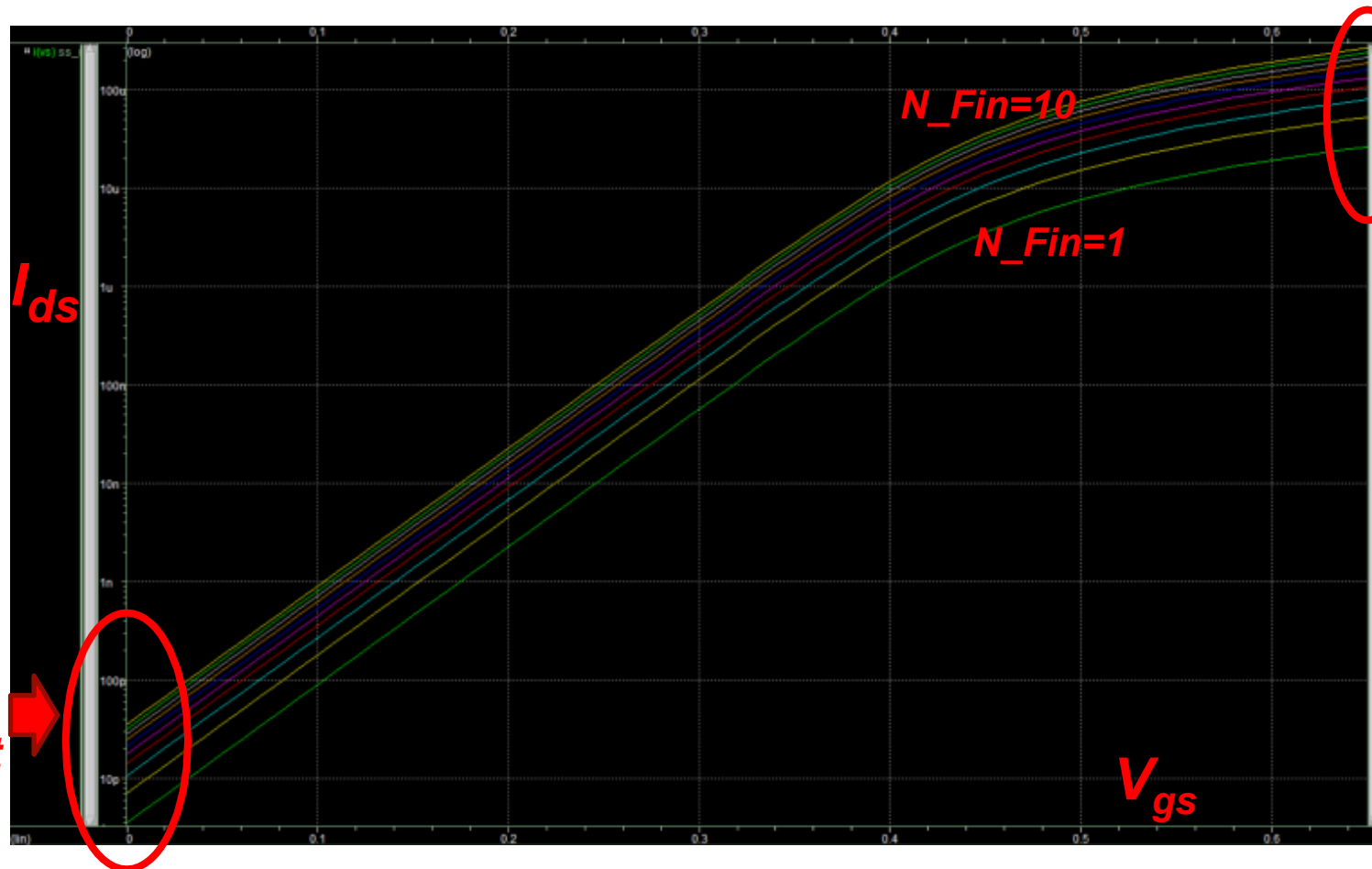
➤ Plot  $I_{ds}$ - $V_{ds}$  (@ $V_{gs} = V_{DD}$ ) curves

➤ Plot  $I_{ds}$ - $V_{gs}$  (@ $V_{ds} = V_{DD}$ ) curves

- For both n-channel and p-channel devices
- FinFETs: fin number is increased from 1 to 10 with a step of 1
- Bulk Si-MOSFETs: width is increased from  $3\lambda$  to  $15\lambda$  with a step of  $3\lambda$

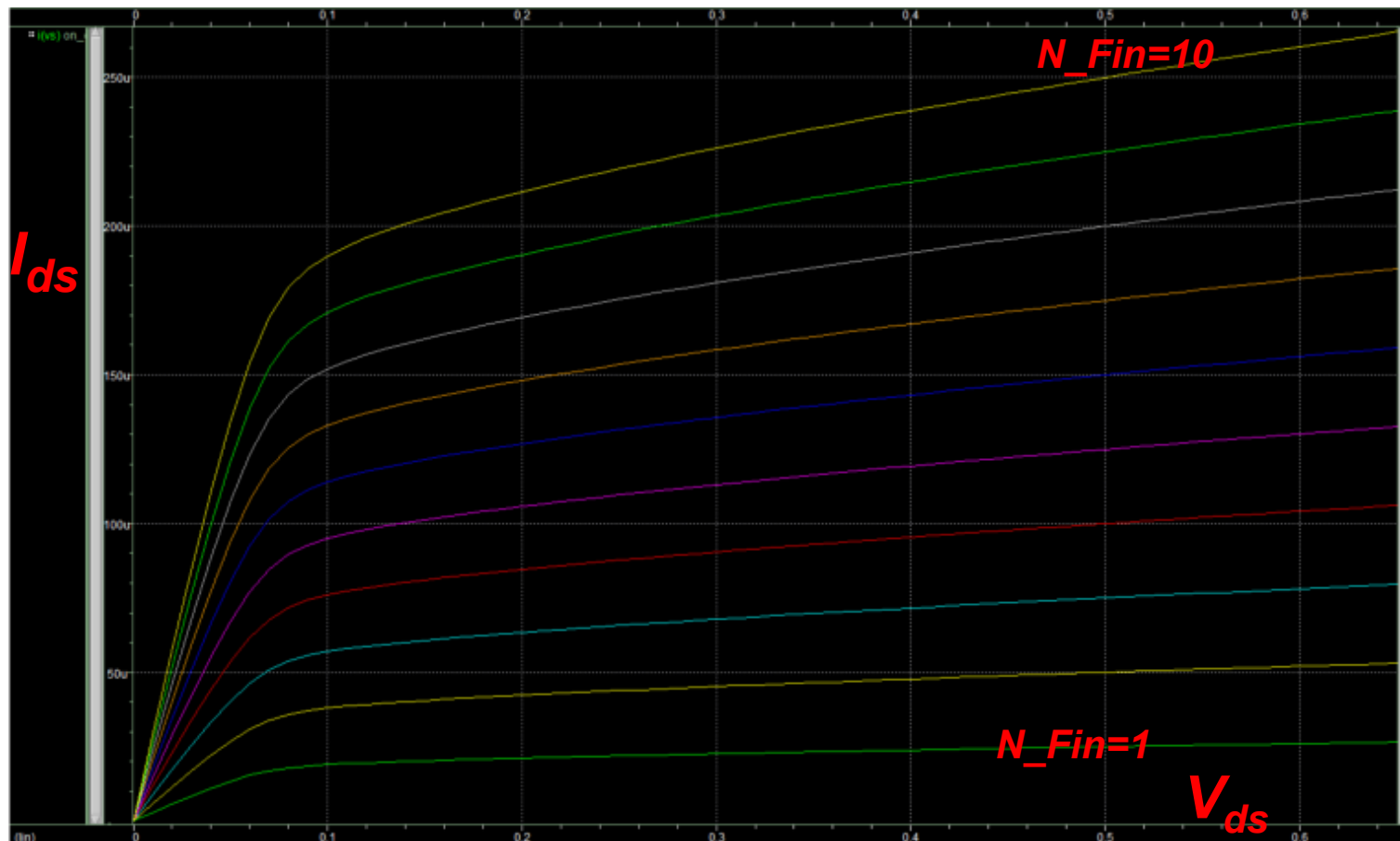
# $I_{ds}$ - $V_{gs}$ Curve of N-Channel FinFETs

- $I_{ds}$  versus  $V_{gs}$  in logarithmic coordinate ( $V_{ds}=V_{DD}$ )



# $I_{ds}$ - $V_{ds}$ Curve of N-Channel FinFETs

- $I_{ds}$  versus  $V_{ds}$  in linear coordinate ( $V_{gs} = V_{DD}$ )



## ***Task 2: Metrics to be Measured***

- ❑ On-state current ( $I_{on}$ )
- ❑ Off-state current ( $I_{off}$ )
- ❑ On-state to off-state current ratio ( $I_{on}/I_{off}$ )
- ❑ Equivalent resistance ( $R_{on}$  &  $R_{off}$ )
- ❑ Subthreshold Swing (SS)



# Measurement Methods — $I_{on}$ & $I_{off}$

□ Take the n-channel device as an example

- The on-state current ( $I_{on}$ ) is measured when

- $V_{gs} = V_{DD}$

- $V_{ds} = V_{DD}$

- The off-state current ( $I_{off}$ ) is measured when

- $V_{gs} = 0$

- $V_{ds} = V_{DD}$

# Measurement Methods — Ron & Roff

## □ Take the n-channel device as an example

- $R_{on}$ : According to Fig. 1, set  $V_g = V_{DD}$ , conduct simulation and get the curve shown in Fig. 2. Then use equation (1) to estimate Roff value.
- $R_{off}$ : Set  $V_g=0V$  and repeat the above process.

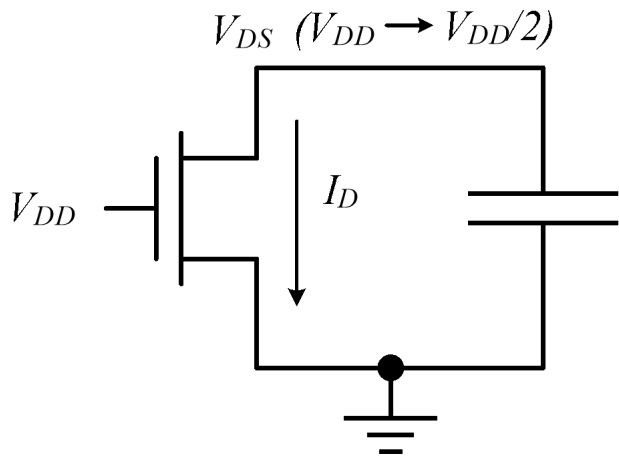


Fig. 1

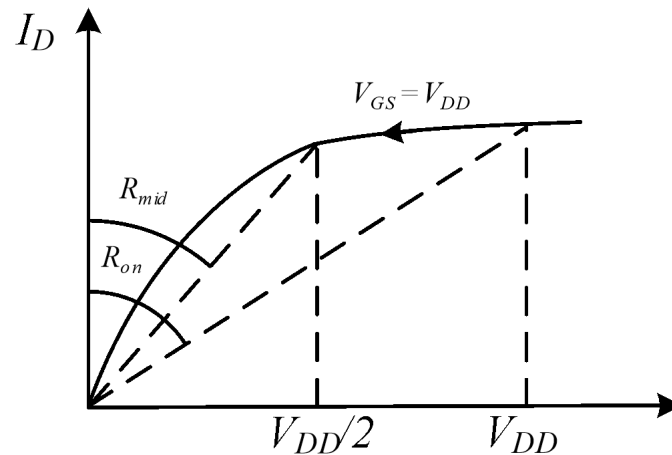


Fig. 2

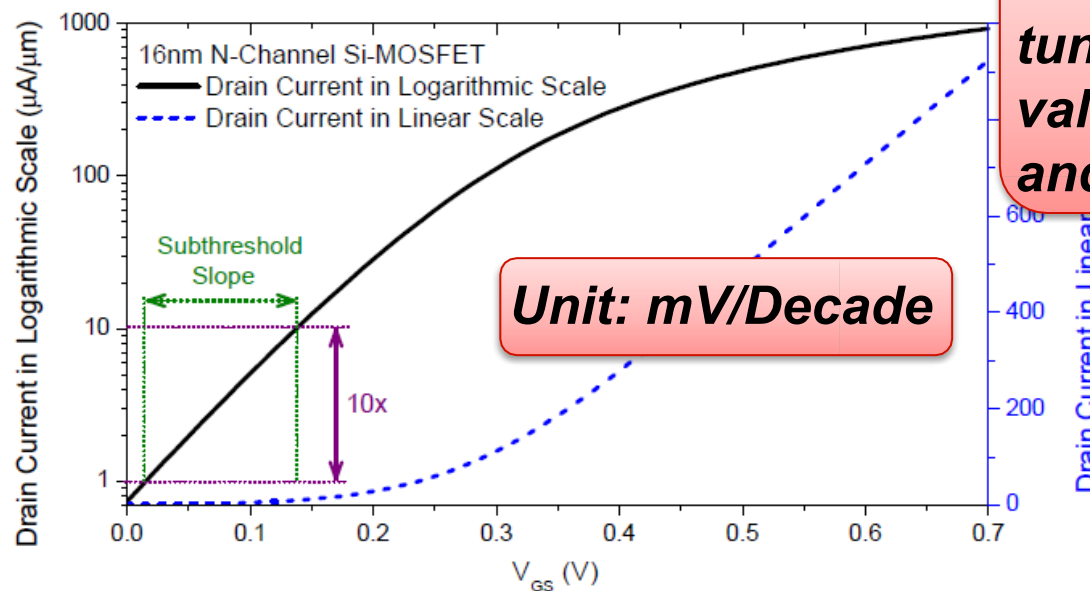
$$R_{eq} = \text{average}_{t=t_1 \dots t_2} (R_{on}(t)) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} R_{on}(t) dt = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)} dt \approx \frac{1}{2} (R_{on}(t_1) + R_{on}(t_2)) \quad (1)$$

# Measurement Methods — Subthreshold Slope (SS)

□ According to the definition, you can use the following way

- Find the  $V_{gs}$  when  $I_{ds} = 0.1 \mu A \times (W/L)$ , denoted by  $V_1$
- Find the  $V_{gs}$  when  $I_{ds} = 0.01 \mu A \times (W/L)$ , denoted by  $V_2$
- The subthreshold slope (SS) =  $V_1 - V_2$

**You may need to tune the current values to get  $V_1$  and  $V_2$**



## ***Task 3 (optional): TFET***

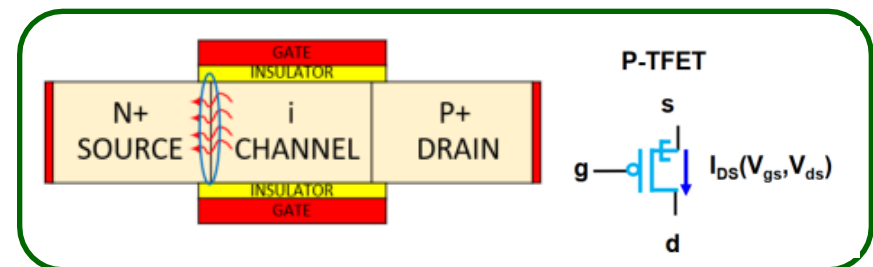
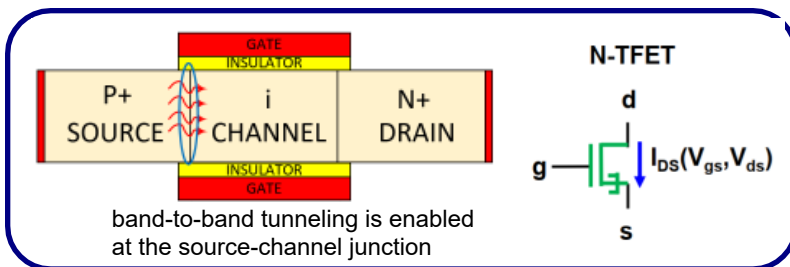
- ☐ I-V Curve
- ☐ On-state current ( $I_{on}$ )
- ☐ Off-state current ( $I_{off}$ )
- ☐ On-state to off-state current ratio ( $I_{on}/I_{off}$ )
- ☐ Equivalent resistance ( $R_{on}$  &  $R_{off}$ )
- ☐ Subthreshold Swing (SS)

# Models for TFET

- Use the Penn State III-V Tunnel FET Model Manual Version 1.0.1 for task 3 (optional).
  - Download the from models and manual from Canvas
  - Models are available for both n-channel and p-channel devices
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- The diagram illustrates the setup for using the Penn State III-V Tunnel FET Model Manual. It shows a Verilog-A file named `.hdl` and a model path `"../heterotfet.va"`. Below this, a Verilog-A code snippet is shown: `x1 d1 gate s1 tfet type=1 w=width`. Red arrows point to specific parts of the code with annotations: `d1` is labeled "Drain", `gate` is labeled "Gate", `s1` is labeled "Source", `tfet` is labeled "tfet type (no need to change)", `type=1` is labeled "1: n-channel TFET -1: p-channel TFET", and `w=width` is labeled "Tune width with a fixed length of 20nm".

# Simulation Settings for TFET

- ❑  $L_g$  is fixed at 20nm for both n-channel and p-channel TFETs while  $W_g$  is changed from  $3\lambda$  to  $15\lambda$  with a step of  $3\lambda$
- ❑ Supply voltage ( $V_{DD}$ ) is 0.3V for 20nm TFETs
- ❑ Simulation temperature
  - $T = 25^\circ\text{C}$



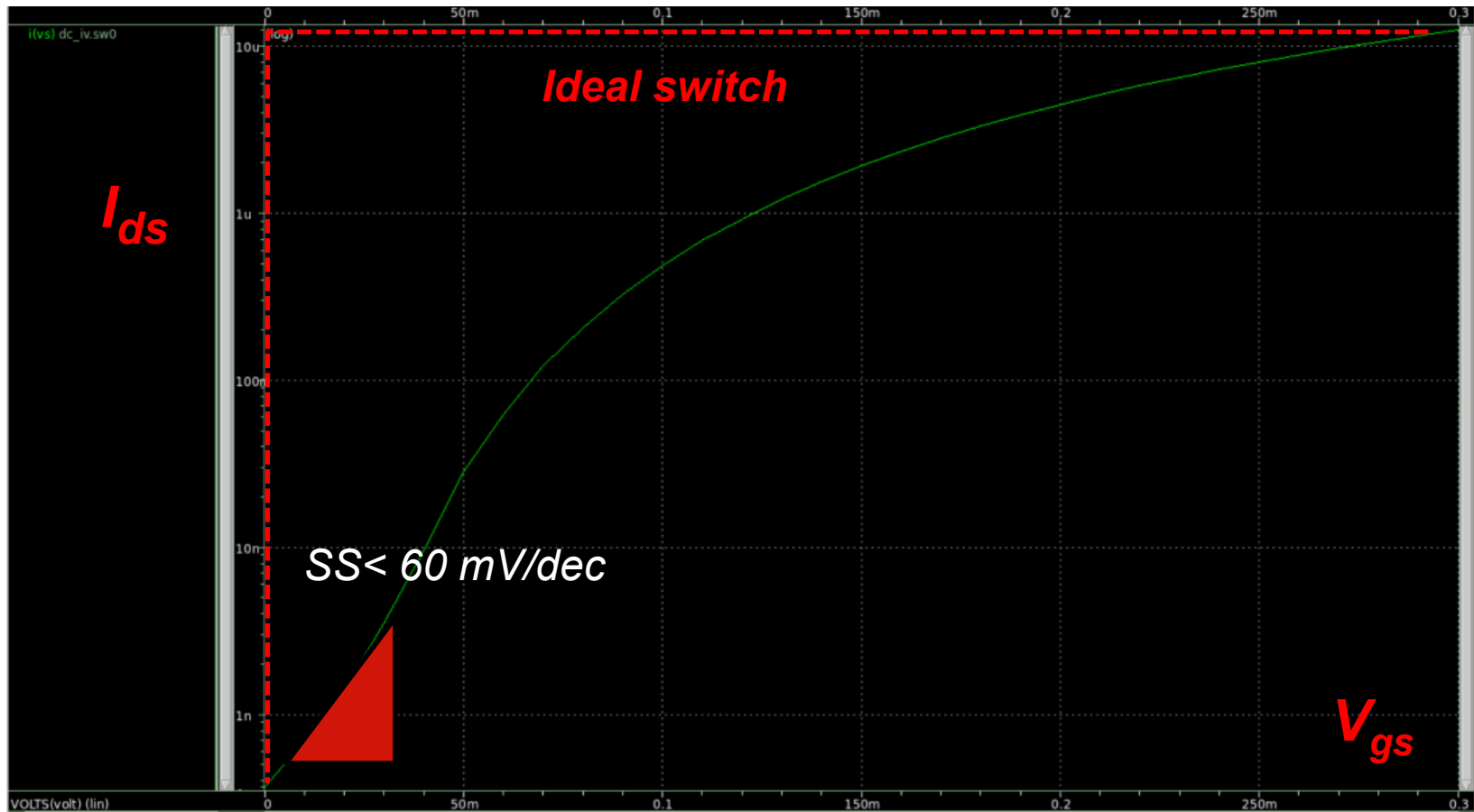
# $I_{ds}$ - $V_{ds}$ Curve of N-Channel TFETs

- $I_{ds}$  versus  $V_{ds}$  in linear coordinate ( $V_{gs}$  sweep from 0 to  $V_{DD}$ )



# $I_{ds}$ - $V_{gs}$ Curve of N-Channel TFETs

- $I_{ds}$  versus  $V_{gs}$  in logarithmic coordinate ( $V_{ds}=V_{DD}$ )





# ***Outline***

- Lab Contents
- Report Requirements

# ***Report Requirement***

- ❑ Write your lab report like writing a technical document (readable, comprehensive analysis, no typo...)
- ❑ You may include
  - Introduction/background
  - Lab procedures
  - Lab results
    - Widths/lengths of transistors, I-V curves, result tables of metrics...
  - **Technical analysis of the simulation results**
  - Observations and conclusions
    - You can also add some comments on how this lab can be helpful to your understanding of the class material

# ***Submission***

- ❑ You need to submit your **report** and **code**
  - Name of report (in PDF format):  
**lab1\_report\_[Name]\_[Student No.].pdf**
  - Name of code (compressing the files):  
**lab1\_code\_\_[Name]\_[Student No.].zip**
  
- ❑ Please upload your report to Canvas course website
  
- ❑ Submission of lab1 report and code will be due on  
**13<sup>th</sup> October 2021**

# Q & A

- If you have any technical problem, you may contact TA through

*TA: 汪登峰*

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