Digital Integrated Circuits

YuZhuo Fu

contact:fuyuzhuo@ic.sjtu.edu.cn

Office location：417 room

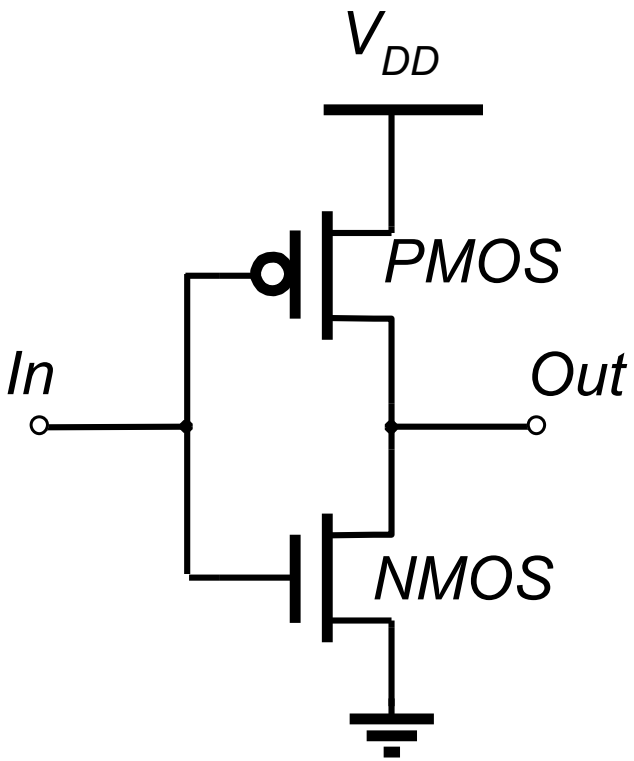
WeiDianZi building,No 800 DongChuan road,MinHang Campus

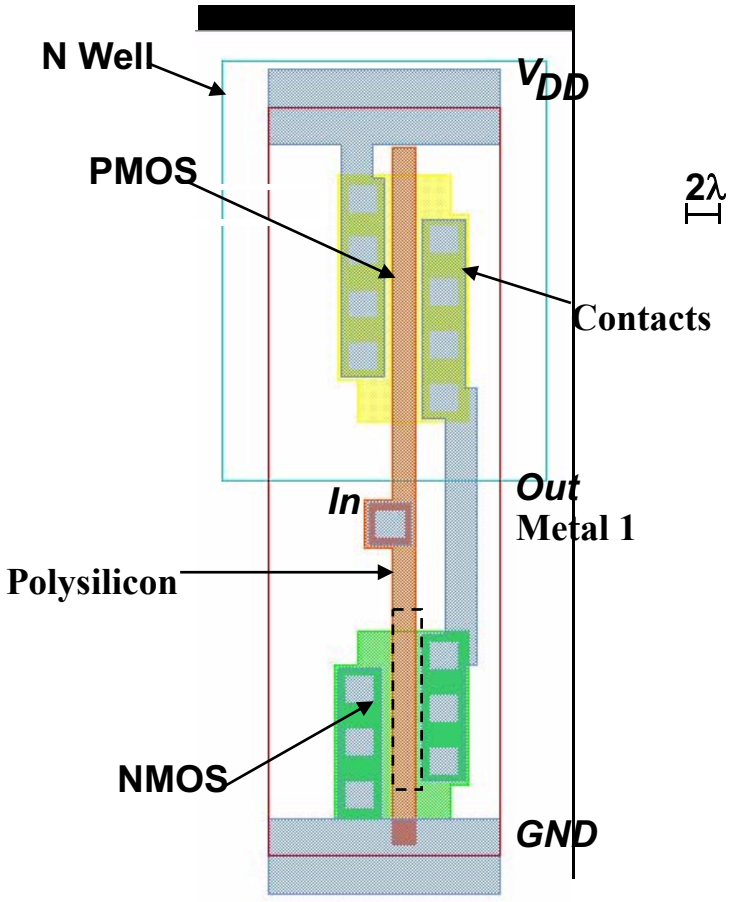
Chapter 3 Inverter

CMOS Inverter

- ***At a glance***
- Static behavior
- Dynamic behavior
- Power, Energy, and Energy Delay
- Perspective tech.

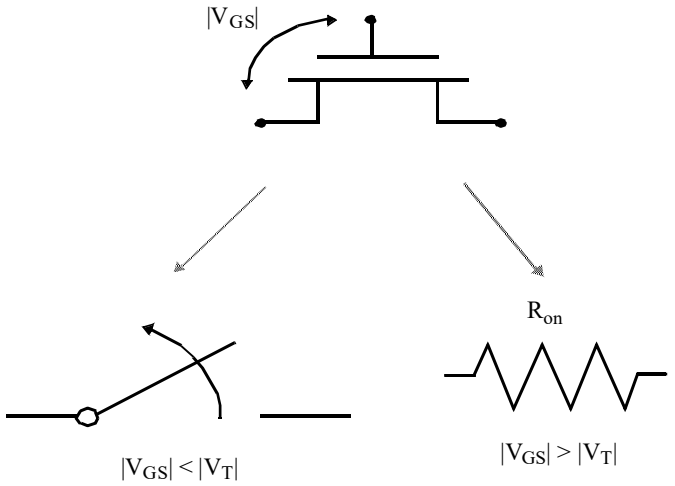
CMOS Inverter



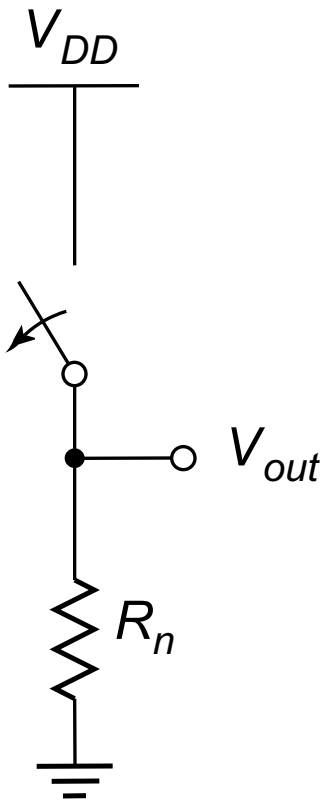


A First Glance of CMOS

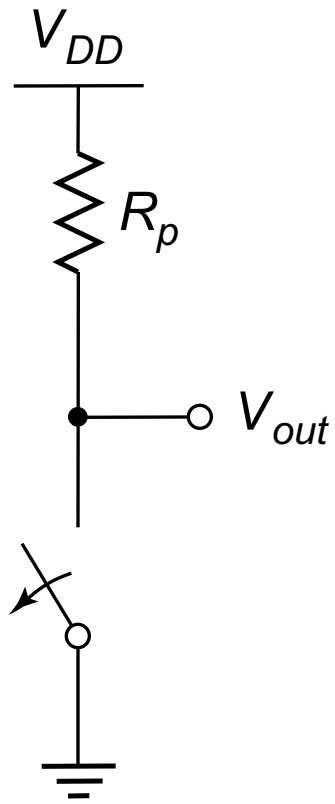
- A switch with infinite off-resistance and a finite on-resistance
  - When $V_{gs}<V_t$，MOS is off
  - when$V_{gs}>V_t$，MOS is on just like a resistance R_{on}
- whenV_{in}=Vdd，nMOS on，pMOS off
- When V_{in}=0，pMOS off，nMOS on



CMOS Inverter First-Order DC Analysis



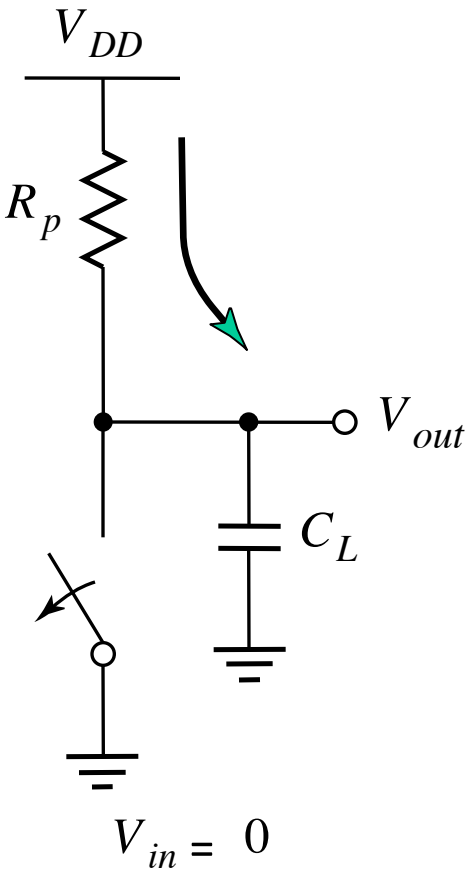
$V_{in} = V_{DD}$



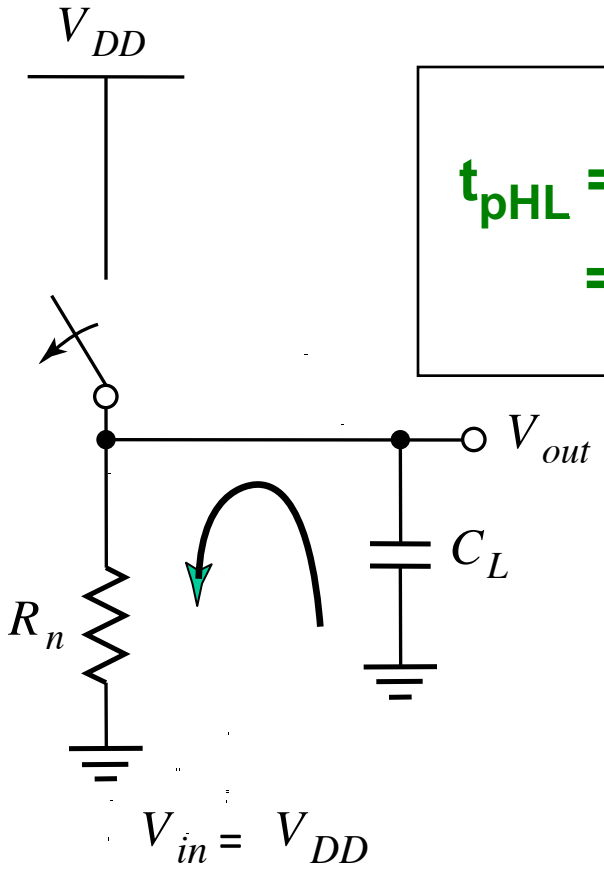
$V_{in} = 0$

$$V_{OL} = 0$$
$$V_{OH} = V_{DD}$$
$$V_M = f(R_n, R_p)$$

CMOS Inverter: Transient Response



(a) Low-to-high



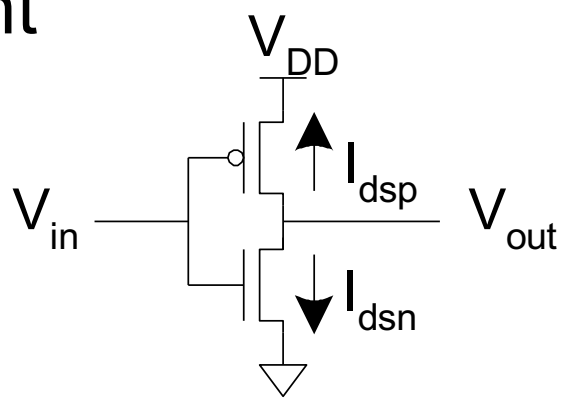
(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$

$= 0.69\ R_{on}C_L$

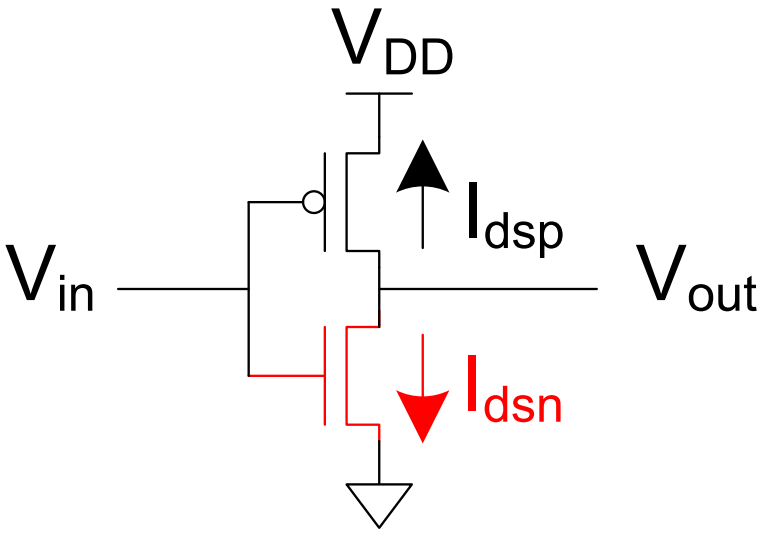
DC Response

- When $V_{in} = 0$ => $V_{out} = V_{DD}$
- When $V_{in} = V_{DD}$ => $V_{out} = 0$
- In between
  - V_{out} depends on transistor size and current
  - ***By KCL, must settle such that $I_{dsn} = |I_{dsp}|$***
  - We could solve equations，But graphical solution gives more insight



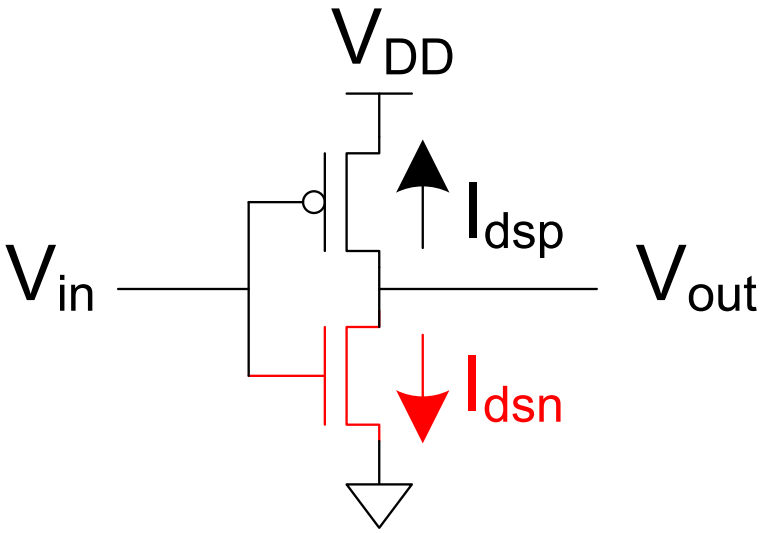
nMOS Operation

Cutoff	**Linear**	**Saturated/VS**
$V_{gsn} < ?$	$V_{gsn} > ?$	$V_{gsn} > ?$
	$V_{dsn} < ?$	$V_{dsn} > ?$



nMOS Operation

Cutoff	Linear	Saturated/VS
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{dsn} < V_{gsn}–V_{tn}/V_{dsatn}$	$V_{dsn} > V_{gsn}–V_{tn}/V_{dsatn}$

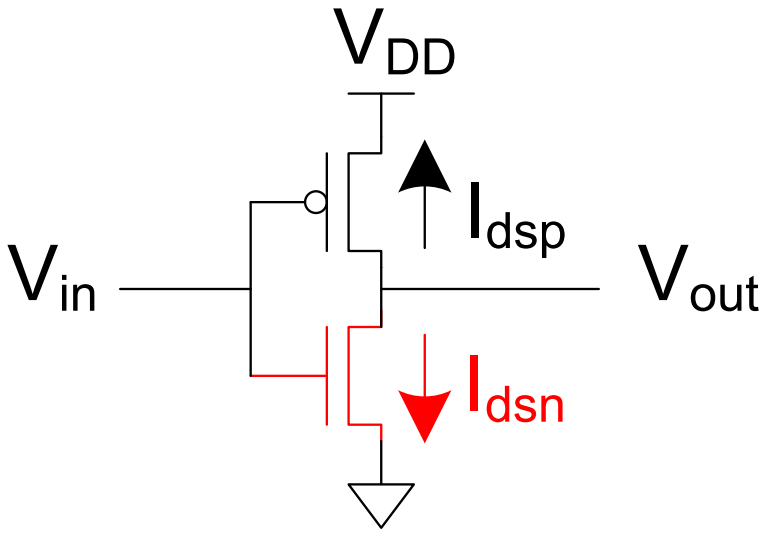


nMOS Operation

Cutoff	Linear	Saturated/VS
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{dsn} < V_{gsn} - V_{tn} / V_{dsatn}$	$V_{dsn} > V_{gsn} - V_{tn} / V_{dsatn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

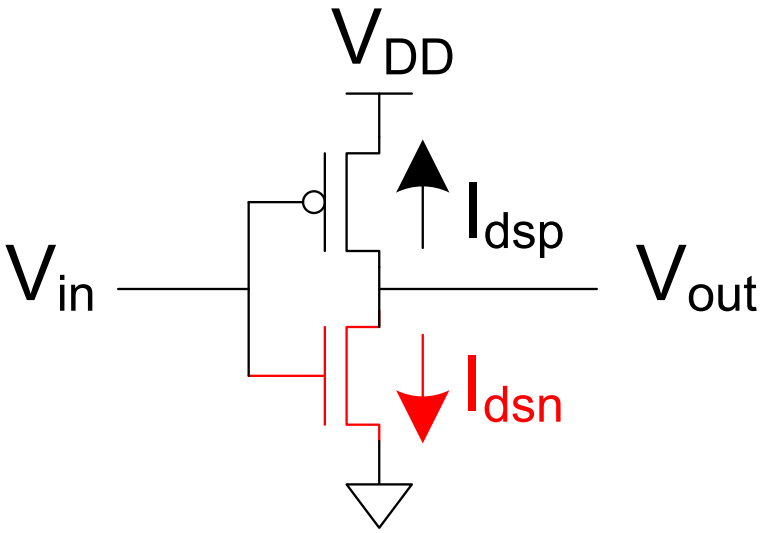


nMOS Operation

Cutoff	Linear	Saturated/VS
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
	$V_{dsn} < V_{gsn}–V_{tn}/V_{dsatn}$	$V_{dsn} > V_{gsn}–V_{tn}/V_{dsatn}$
	$V_{out} < V_{gsn}–V_{tn}/V_{dsatn}$	$V_{out} > V_{gsn}–V_{tn}/V_{dsatn}$

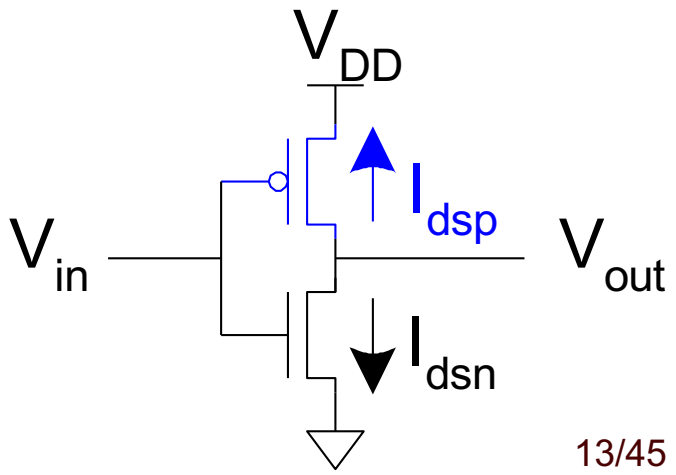
$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



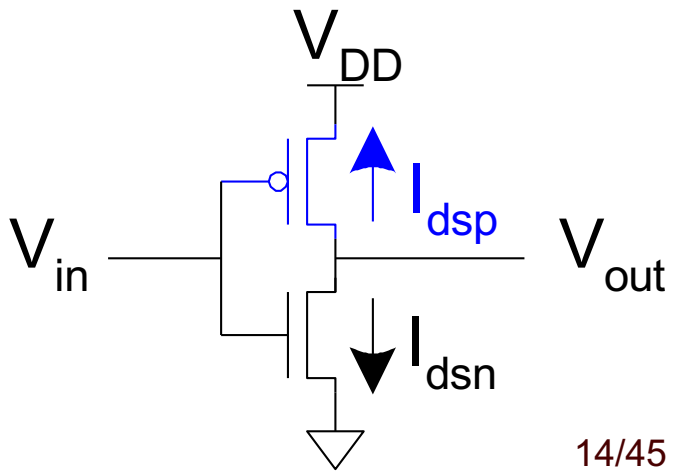
pMOS Operation

Cutoff	Linear	Saturated/VS
$V_{gsp} > ?$	$V_{gsp} < ?$	$V_{gsp} < ?$
	$V_{dsp} > ?$	$V_{dsp} < ?$



pMOS Operation

Cutoff	Linear	Saturated/VS
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{dsp} > V_{gsp}–V_{tp}/V_{DSATp}$	$V_{dsp} < V_{gsp}–V_{tp}/V_{DSATp}$

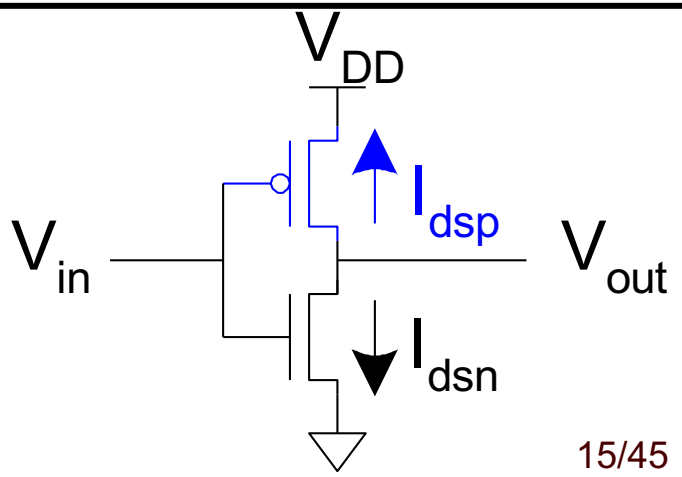


pMOS Operation

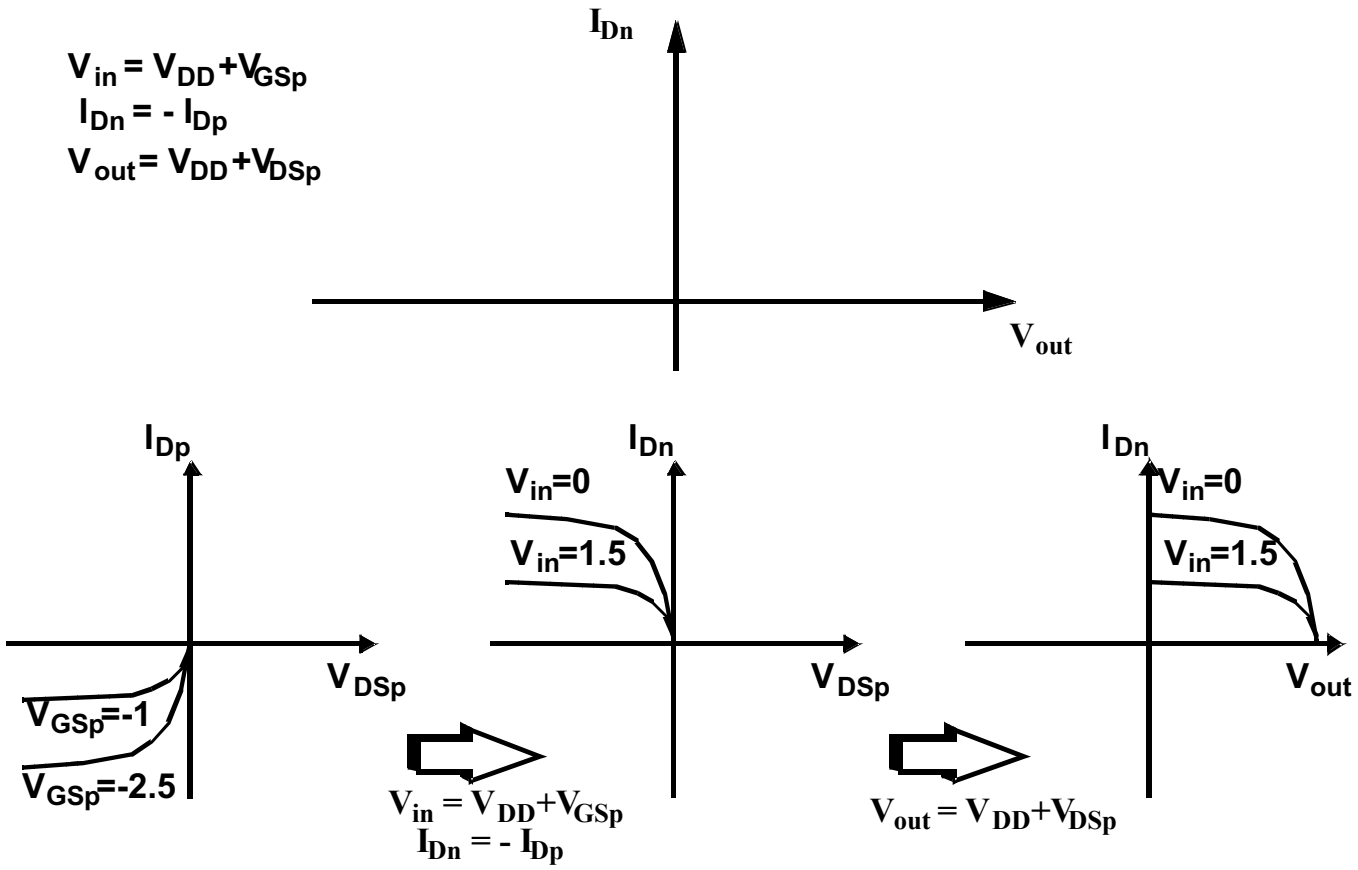
Cutoff	Linear	Saturated/VS
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
$V_{in} > V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$
	$V_{dsp} > V_{gsp} - V_{tp} / V_{DSATp}$	$V_{dsp} < V_{gsp} - V_{tp} / V_{DSATp}$
	$V_{out} > V_{in} - V_{tp} / V_{DSATp}$	$V_{out} < V_{in} - V_{tp} / V_{DSATp}$

$$V_{gsp} = V_{in} - V_{DD}$$

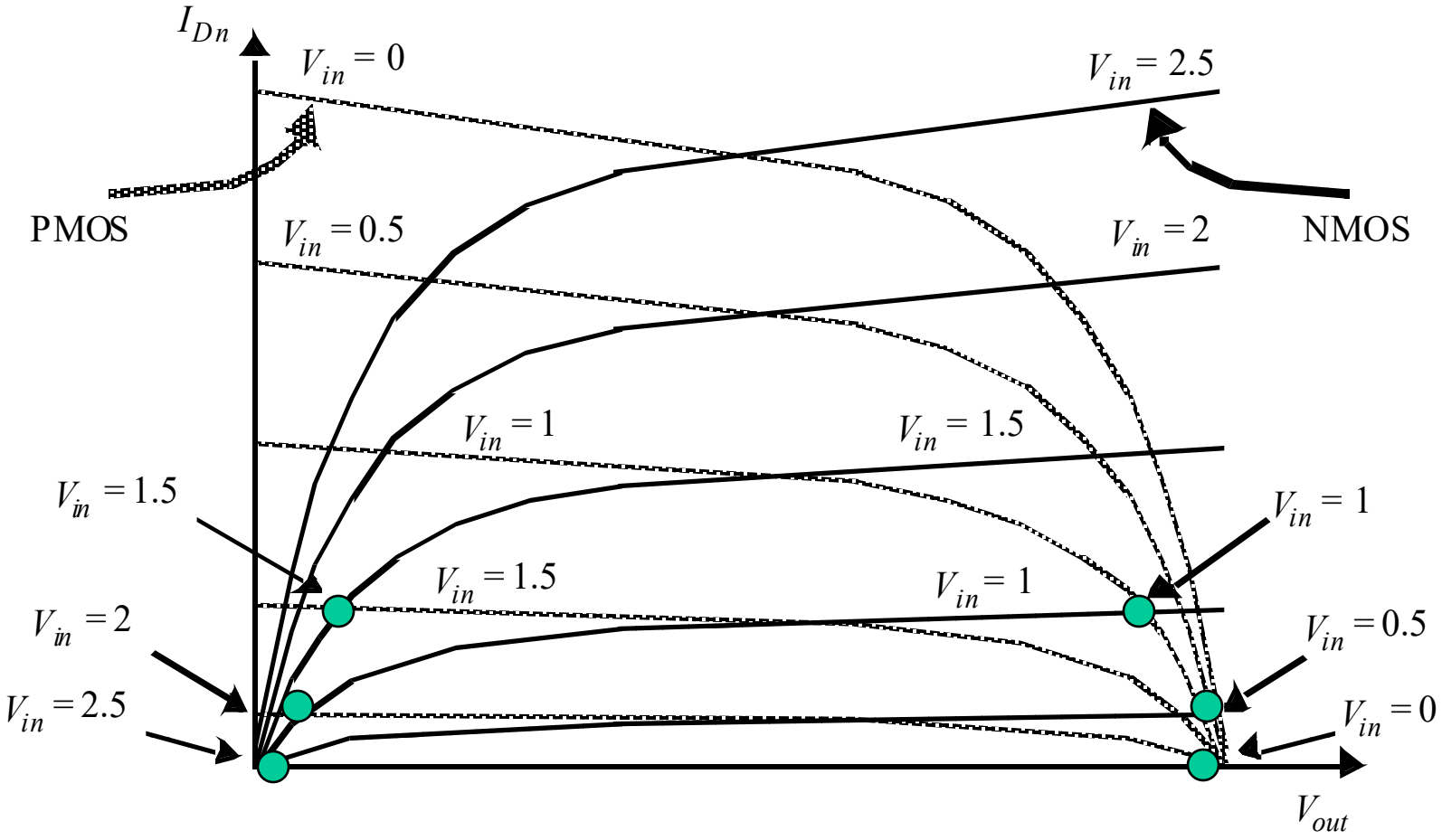
$$V_{dsp} = V_{out} - V_{DD}$$



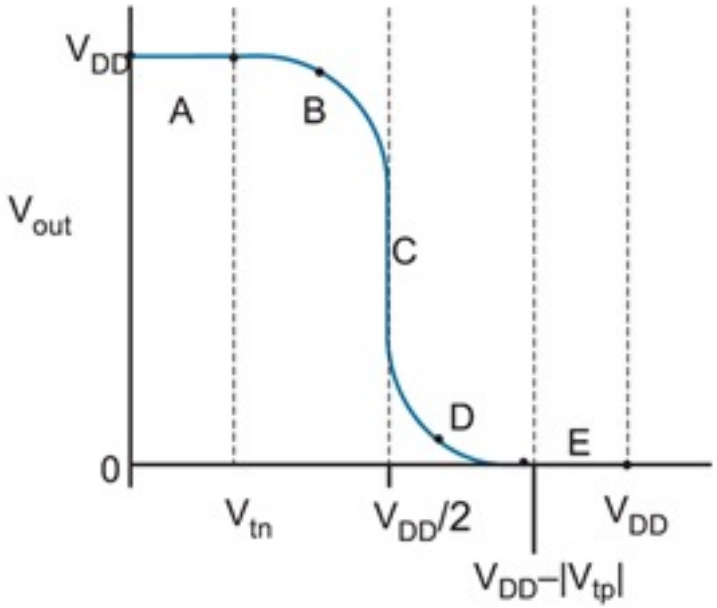
PMOS Load Lines

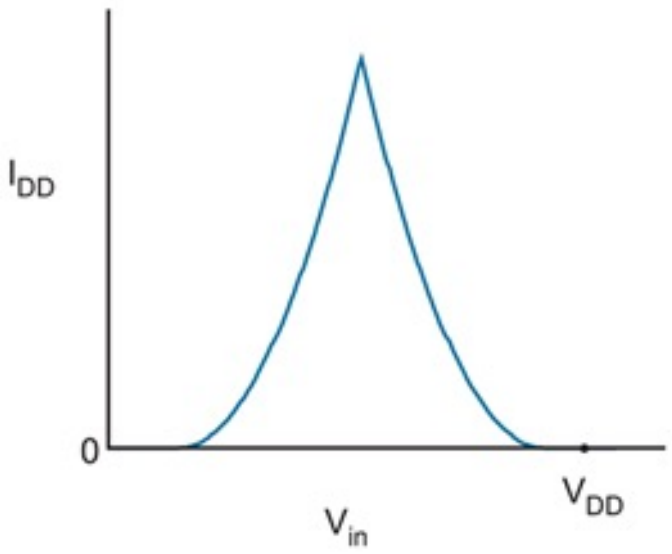


CMOS Inverter Load Characteristics



CMOS Inverter VTC





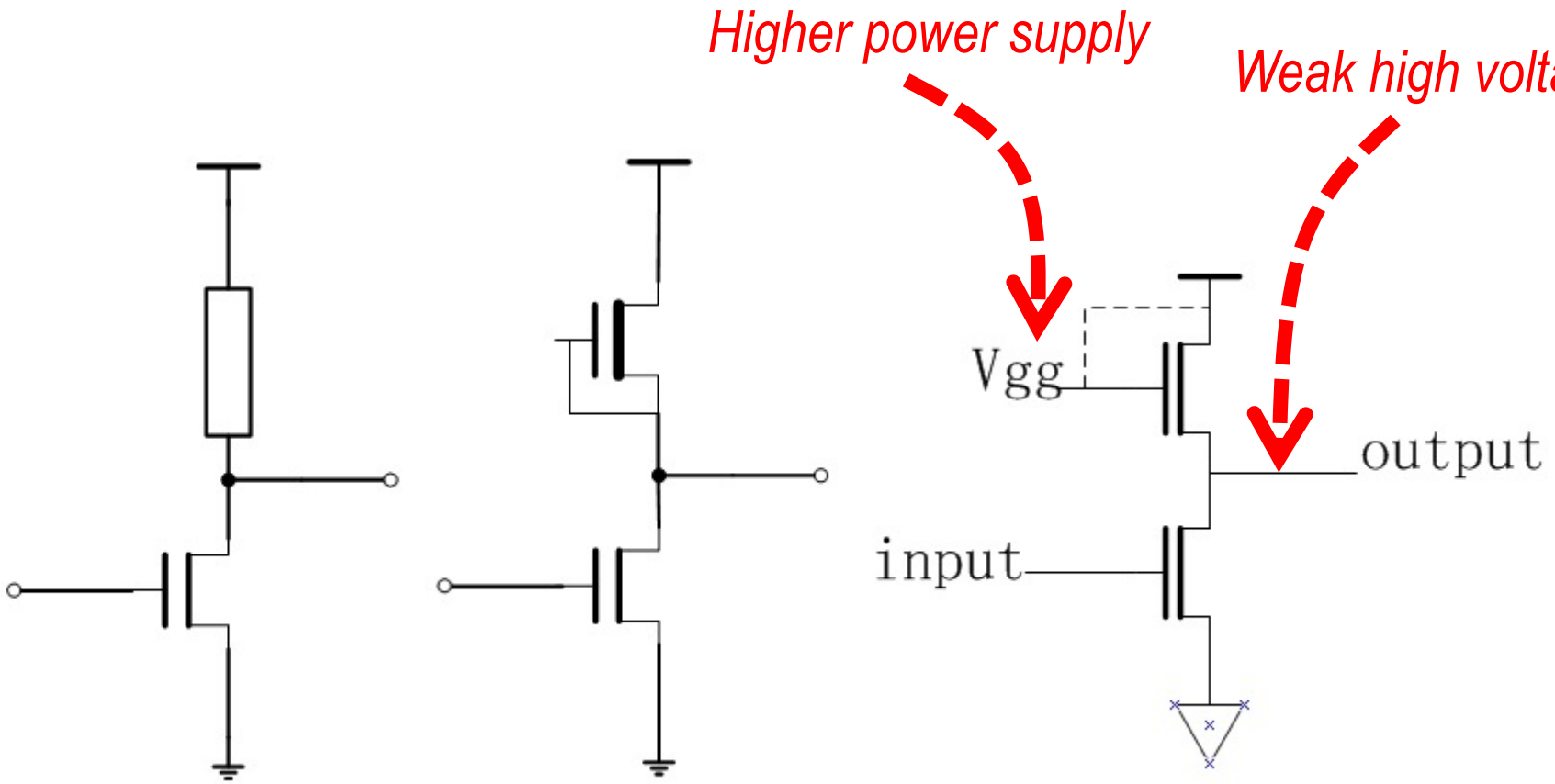
Summary of CMOS inverter operation				
Region	Condition	P-device	N-device	output
A	$[0,V_{tn}]$	**linear**	cutoff	V_{DD}
B	$[V_{tn},V_{DD}/2]$	linear	saturated	$V_{DD}/2$
C	$=V_{DD}/2$	**saturated**	**saturated**	X drop
D	$[V_{DD}/2,V_{DD}-\|V_{TP}\|]$	saturated	linear	$<V_{DD}/2$
E	$[V_{DD}-\|V_{TP}\|, V_{DD}]$	cutoff	**linear**	0

cmosinverter - 记事本

文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

```
* cmos.sp

*********************************************************************************
* Parameters and models
*********************************************************************************
.param SUPPLY=1.8
.option scale=90n
.param N1=4
.include '../models/mosistsmc180/mosistsmc180.sp'
.temp 70
.option post

*********************************************************************************
* Simulation netlist
*********************************************************************************
Vdd     vdd     gnd     'SUPPLY'
Vin     a       gnd
M1      y       a       gnd     gnd     NMOS    W=4     L=2

M2      y       a       vdd     vdd     PMOS    W='N1*4' L=2


*********************************************************************************
* Stimulus
*********************************************************************************
.DC Vin 0 SUPPLY 0.01 sweep N1 2  20  2
.end
```

Other inverters



Source: Carriers from

CMOS properties

- High noise margins, the voltage swing is equal to the supply voltage
- Ratioless circuit structure
- Low output impedance
- High input resistance
- Low power Static power is low

CMOS Inverter

- At a glance
- ***Static behavior***
- Dynamic behavior
- Power, Energy, and Energy Delay
- Perspective tech.

CMOS inverter static behavior

- ***Threshold Voltage***
- Noise Margin
- Gain
- DC robust

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right) \qquad k_n = \beta_n = \mu_n C_{ox}\frac{W}{L}$$

I_n + I_p

$$k_n\left((V_{gsn} - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_{gsp} - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) = 0$$

$V_{gsn} \to V_{in}$, $V_{gsp} \to V_{in} - V_{DD}$

$$k_n\left((V_M - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_M - V_D - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) =$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{dsat_n}}{2}\right) + \gamma\left(V_{DD} + V_{Tp} + \frac{V_{dsat_p}}{2}\right)}{1+\gamma} \approx \frac{\gamma V_{DD}}{1+\gamma}$$

$$\gamma = \frac{k_p V_{dsat_p}}{k_n V_{dsat_n}} = \frac{W_p v_{dsat_p}}{W_n v_{dsat_n}}$$

$$V_{sat} \approx V_c = LE_c = L\frac{2v_{sat}}{\mu_{eff}}$$

$P/n \uparrow \Rightarrow V_M \uparrow$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right) \qquad k_n = \beta_n = \mu_n C_{ox}\frac{W}{L}$$

$$k_n\left((V_{gsn} - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_{gsp} - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) = 0$$

$$k_n\left((V_M - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_M - V_D - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) =$$

$$\frac{W_p/L_p}{W_n/L_n} = = \approx \frac{k_n' V_{dsat_n}\left(V_M - V_{Tn} - \frac{V_{dsat_n}}{2}\right)}{k_p' V_{dsat_p}\left(V_{DD} - V_M + V_{Tp} + \frac{V_{dsat_p}}{2}\right)}$$

$V_M = \frac{V_{dd}}{2}$

Switching threshold of CMOS inverter

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

Assuming $W_p/W_n=8$, calculating V_M=?

$L_p = L_n =$

$$r = \frac{k_p' \frac{W_p}{L_p} V_{DSAT_p}}{k_n' \frac{W_n}{L_n} V_{DSAT_n}} = \frac{-30*(-1)}{115*0.63} * 8 = 3.3$$

2.5

$$V_M = \frac{(V_{Tn} + \frac{V_{DSAT_n}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSAT_p}}{2})}{1+r}$$

$$= \frac{(0.43 + \frac{0.63}{2}) + 3.3(2.5 - 0.4 - \frac{0.4}{2})}{1+3.3} = \frac{0.75 + 3.3*1.9}{1+3.3} = 1.63V$$

Switching threshold of CMOS inverter

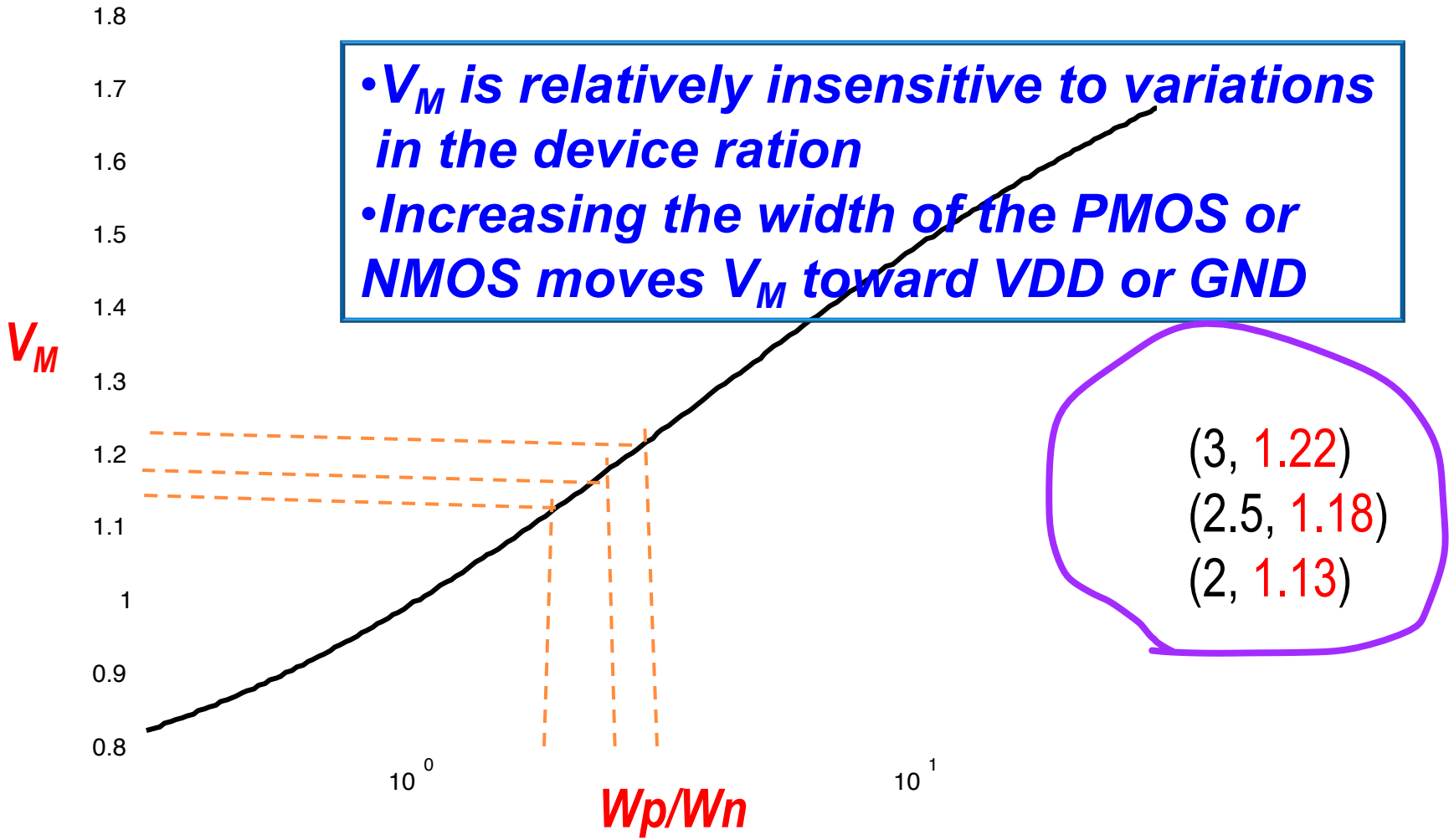
Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})}{-k_p' V_{DSAT_p}(V_{DD} - V_M + V_{Tp} + \frac{V_{DSAT_p}}{2})} = \frac{115\times10^{-6}\times0.63\times(1.25-0.43-\frac{0.63}{2})}{30\times10^{-6}\times1\times(1.25-0.4-\frac{1}{2})} = 3.5$$

This rate let $V_M=V_{dd}/2$!

Switching Threshold as a function of Transistor Ratio



CMOS inverter static behavior

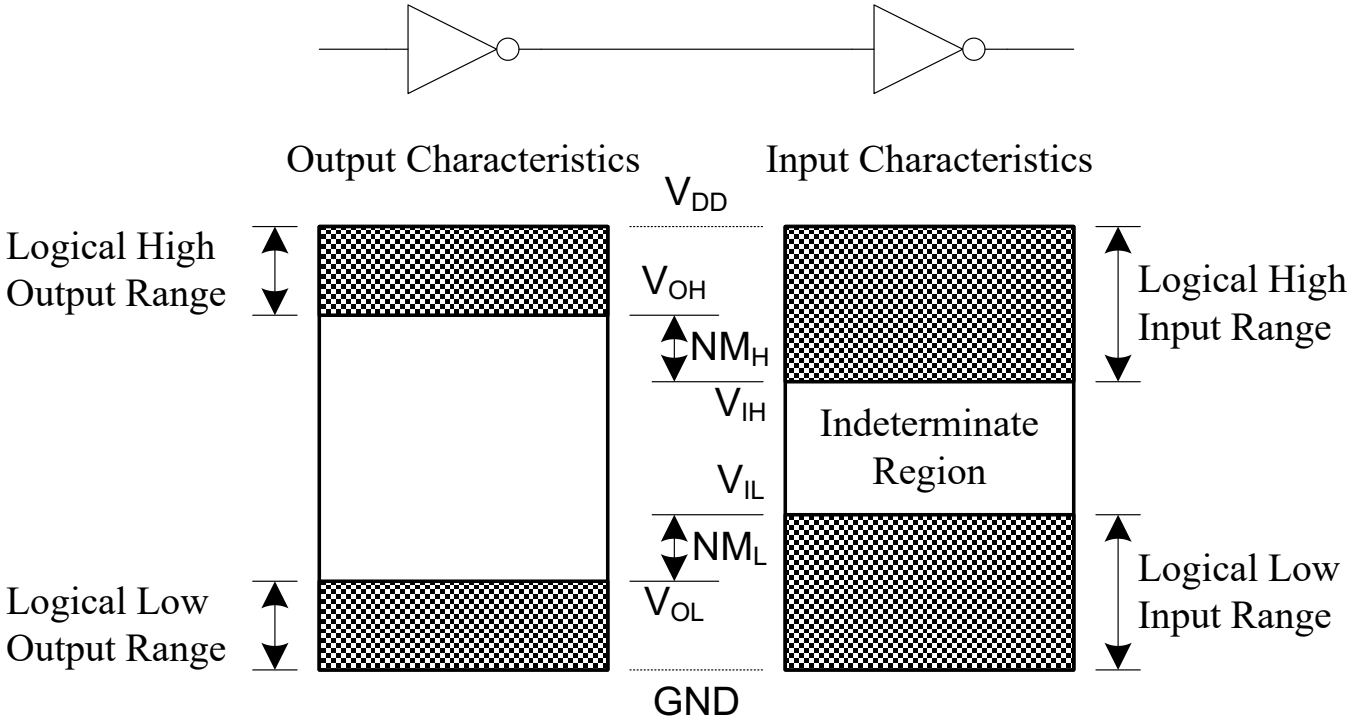
- Threshold Voltage
- ***Noise Margin***
- Gain
- DC robust

Noise Margin

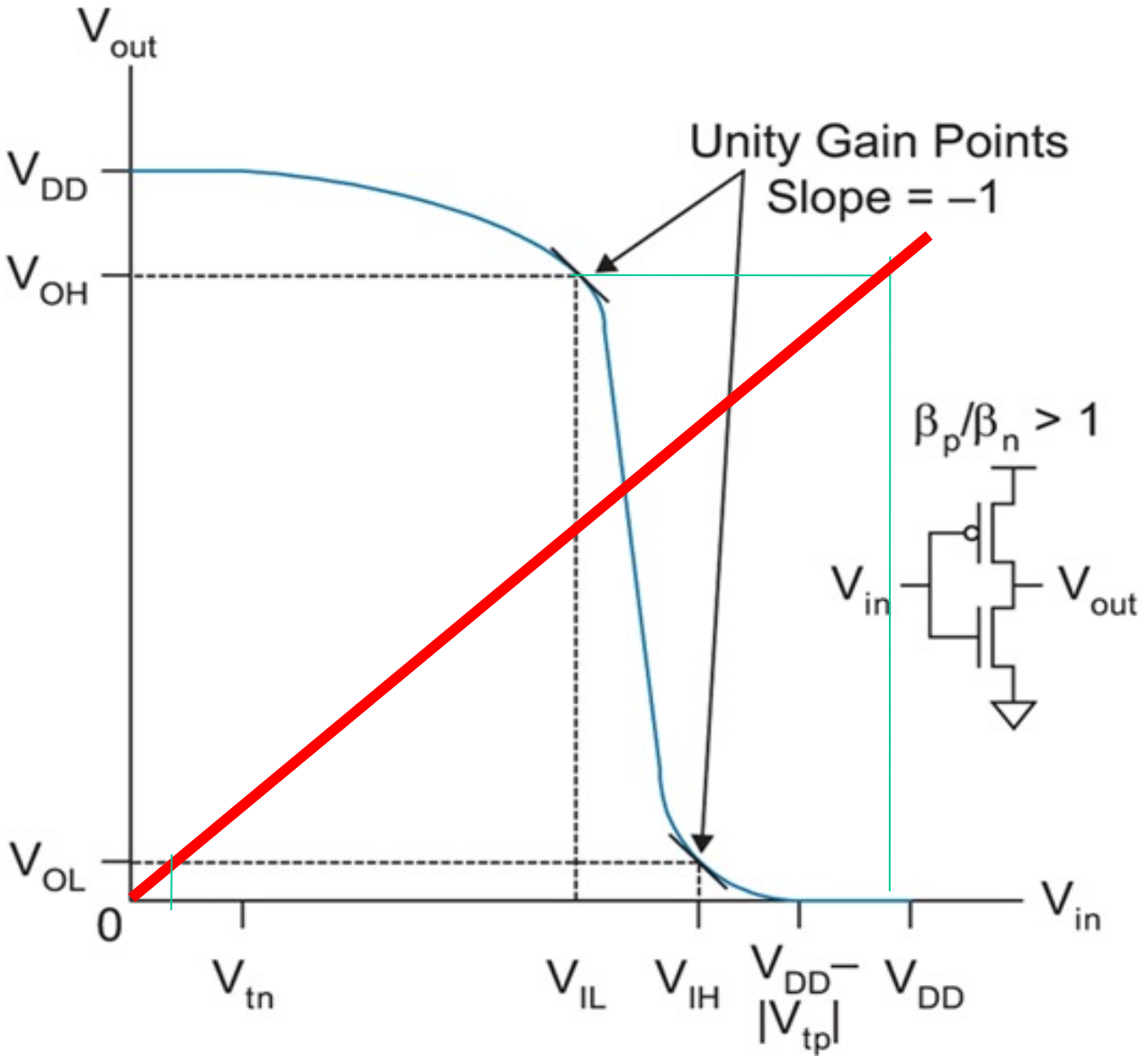
- NM_L
  - The difference in maximum **LOW** input voltage recognized by the receiving gate and the maximum **LOW** output voltage produced by the driving gate
  - $NM_L = V_{IL} - V_{OL}$
- NM_H
  - The difference in minimum **HIGH** input voltage recognized by the receiving gate and the minimum **HIGH** output voltage produced by the driving gate
  - $NM_H = V_{OH} - V_{IH}$

Noise Margin

- VIH=minimum HIGH input voltage
- VIL=maximum LOW input voltage
- VOH=minimum HIGH output voltage
- VOL=maximum LOW output voltage

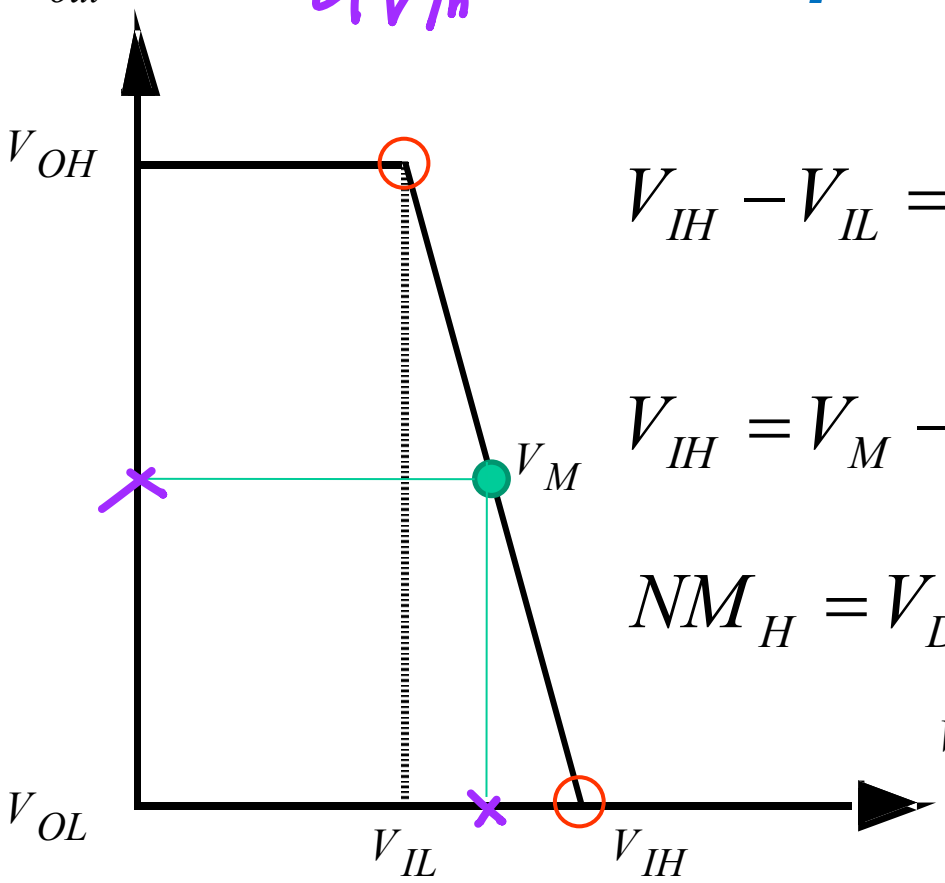


Determining V_{IH} and V_{IL}



Determining V_{IH} and V_{IL}

$g = \frac{dV_{out}}{dV_{in}}$



A simplified approach!

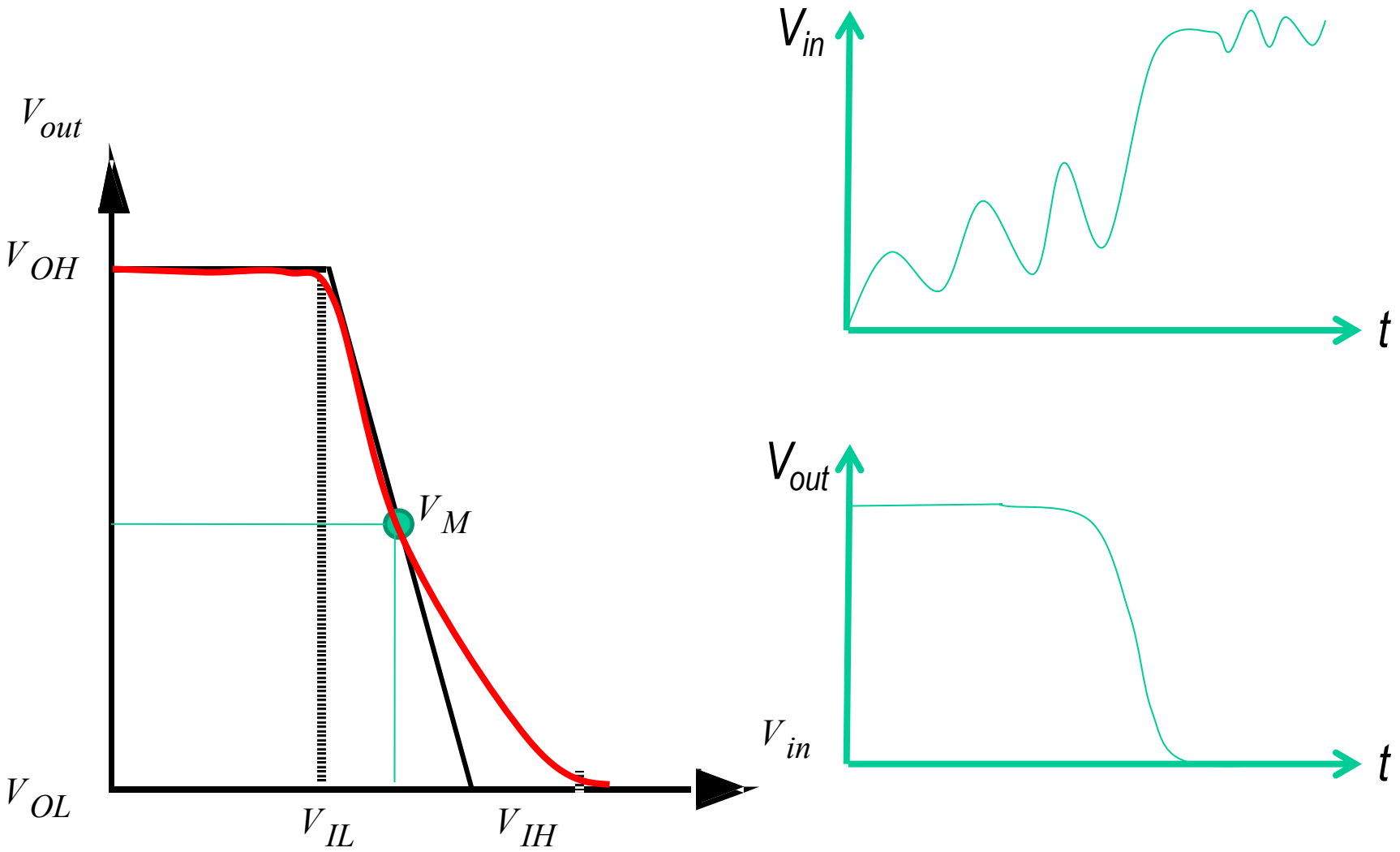
$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g}, V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH}, NM_L = V_{IL}$$

V_M increase, NM_H decrease, NM_L increase

Determining V_{IH} and V_{IL}



Example

g=-30, V_{dd}=2.5V, V_M=1.0V Please estimate NM_H and NM_L

$V_{IH}=V_M-V_M/g=1.0*(1+1/30)=1.03V$

$V_{IL}=(V_{DD}-V_M)/g+V_M=-1.5/30+1.0=0.95V$

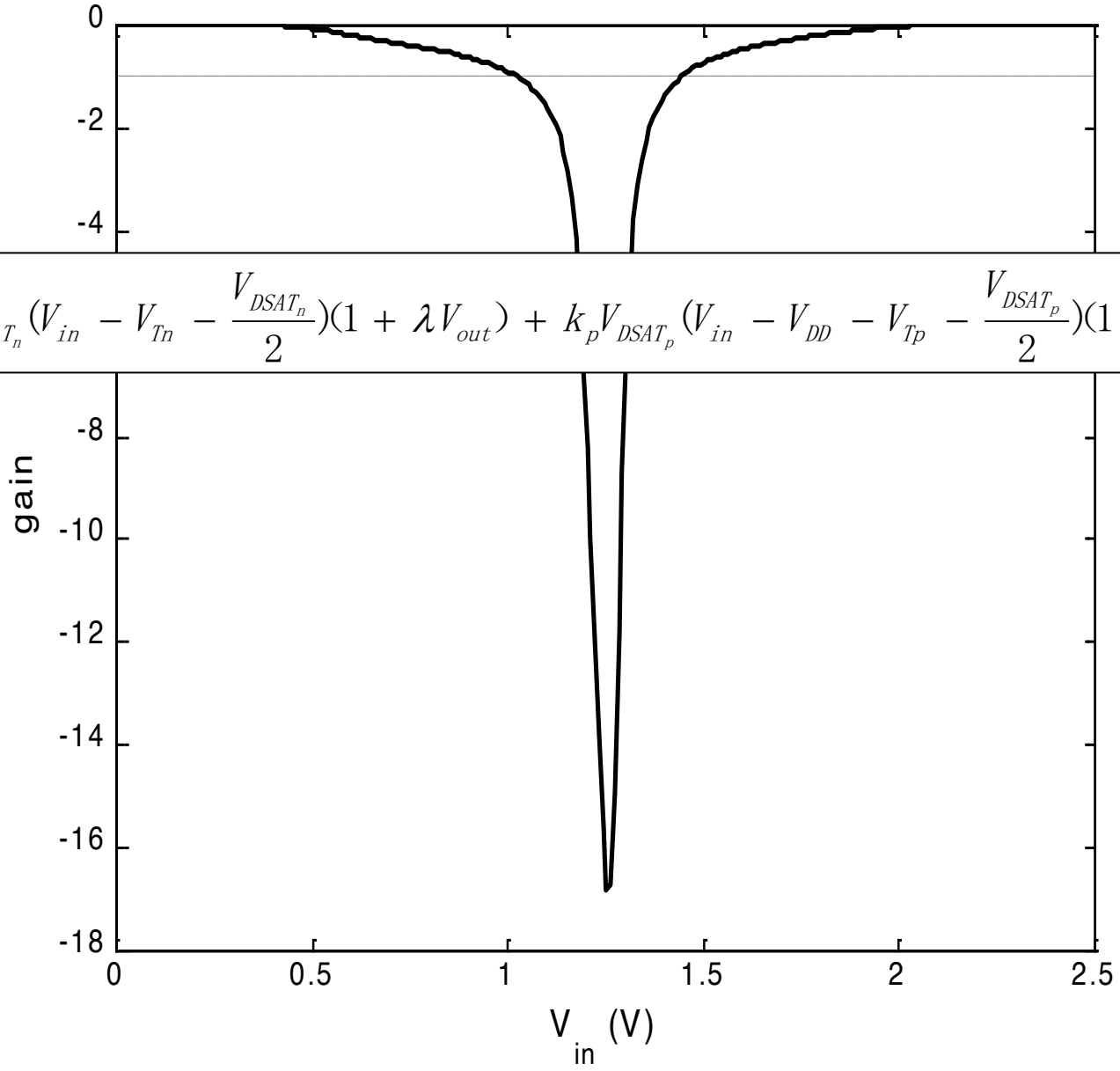
$NM_H=V_{OH}-V_{IH}=2.5-1.03=1.47V$

$NM_L=V_{IL}-V_{OL}=0.95V$

CMOS inverter static behavior

- Threshold Voltage
- Noise Margin
- ***Gain***
- DC robust

Inverter Gain



$$k_n V_{DSAT_n}(V_{in} - V_{Tn} - \frac{V_{DSAT_n}}{2})(1 + \lambda V_{out}) + k_p V_{DSAT_p}(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSAT_p}}{2})(1 + \lambda(V_{DD} - V_{out})) = 0$$

Inverter Gain

$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M}$$

$$= -\left.\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}(1+\lambda_p V_{out} - \lambda_p V_{DD})}{\lambda_n k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right) + \lambda_p k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - {V_{DSATp}}/{2}\right)}\right|_{V_{in}=V}$$

$$\approx -\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}(1+\lambda_p V_{out} - \lambda_p V_{DD})}{k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

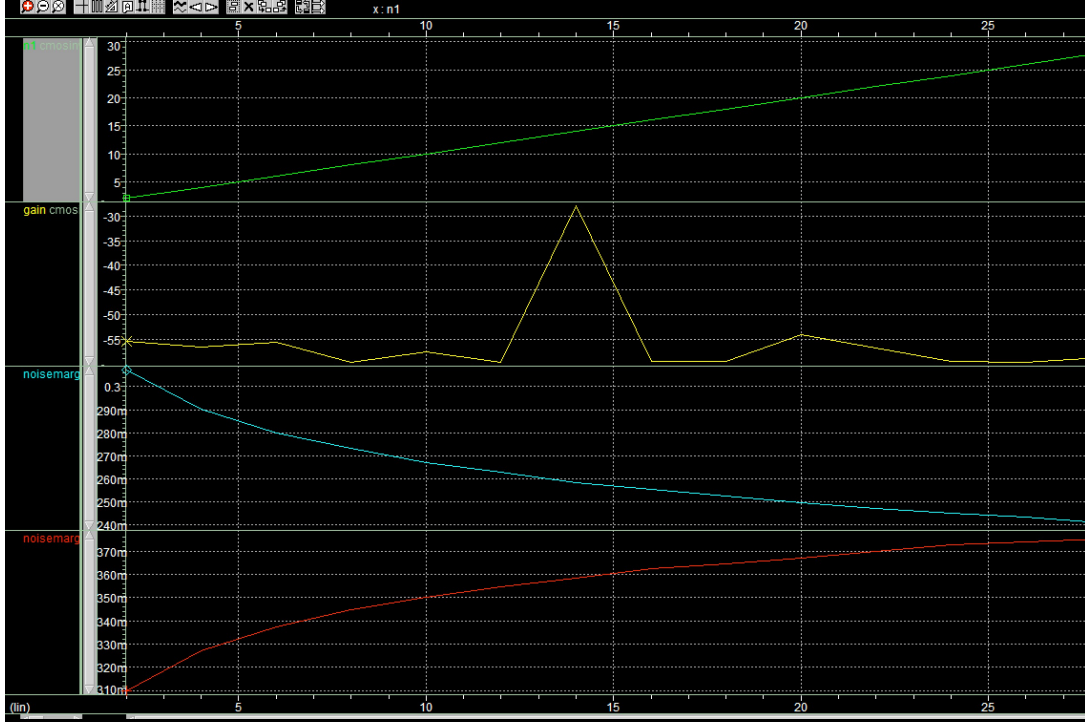
$$= -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

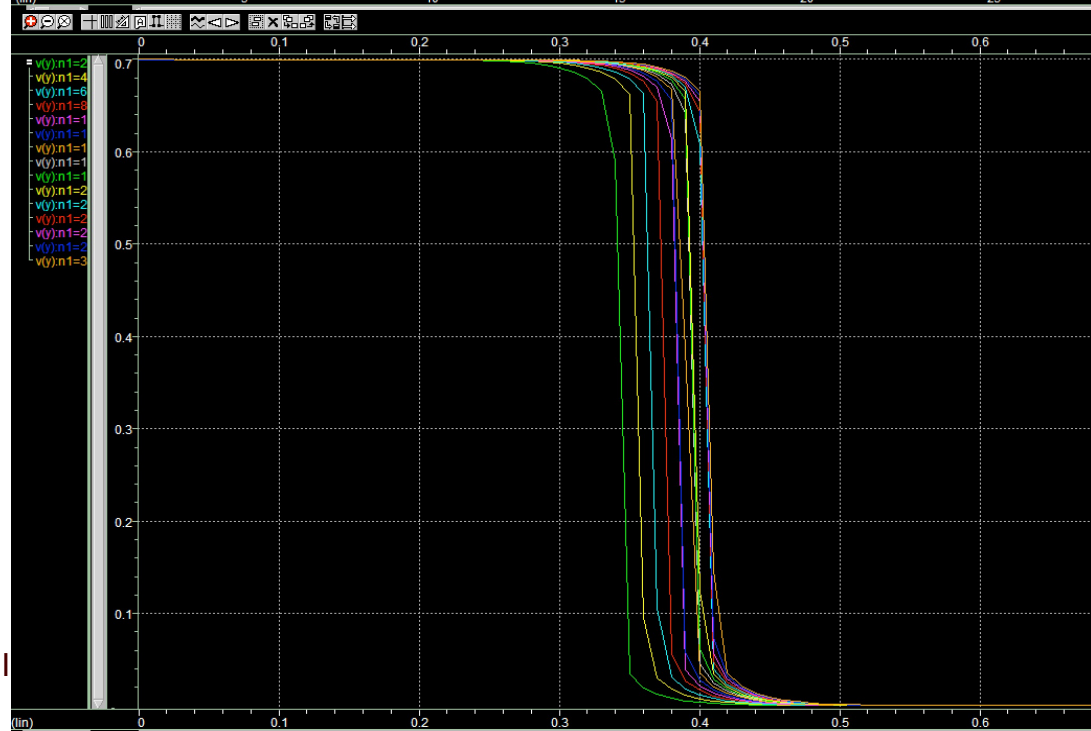
$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}}$$

$V \uparrow$. not sure $g \uparrow$

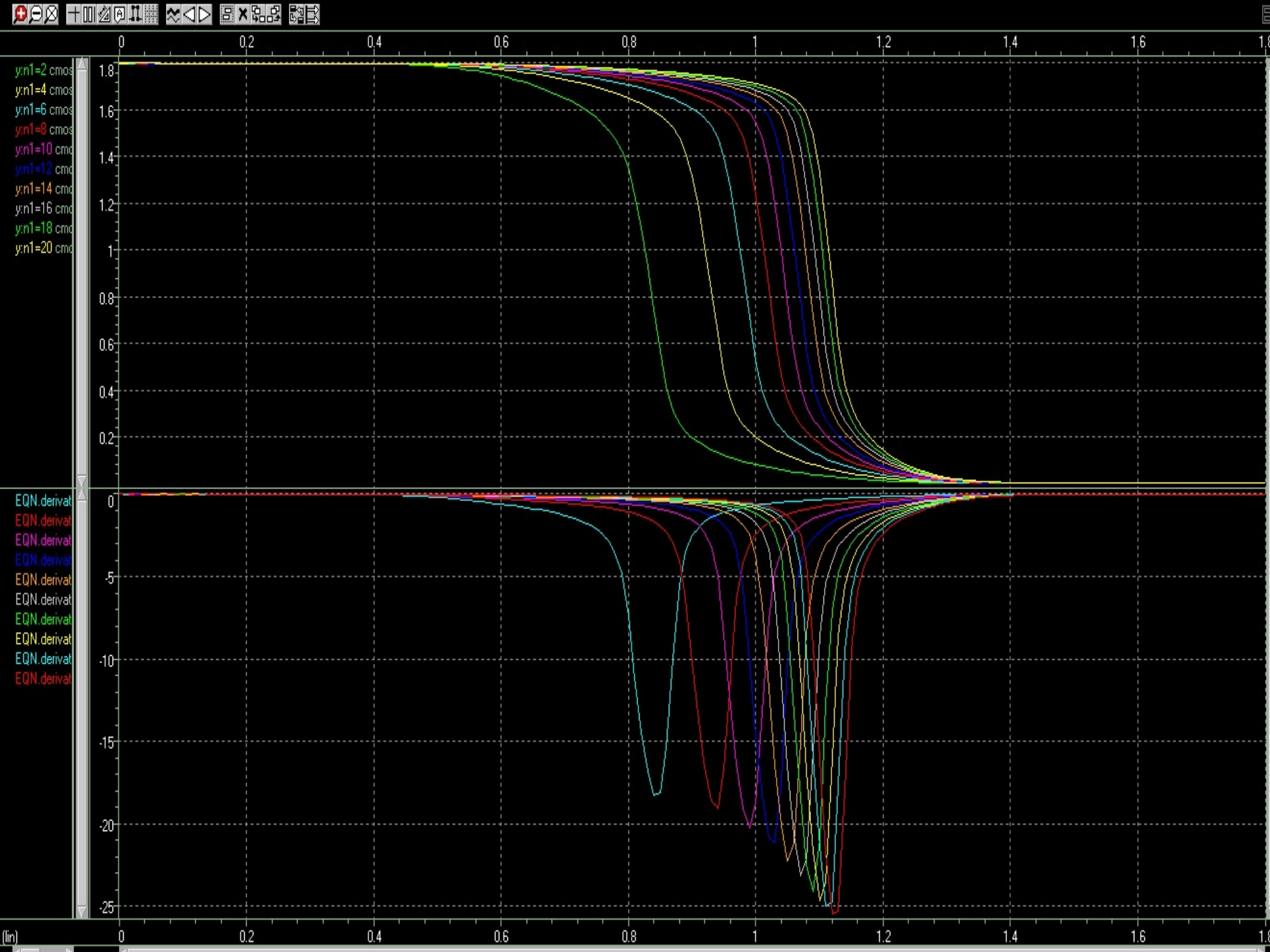
Ratio increase, Gain increase

```
**********************************************
* CMOS Inverter 直流特性
**********************************************
.param N1=4
.param SUPPLY=0.7
.option scale=125n
*.lib '../../lib/cmos25.lib' tt
.include '../../lib/16nm_HP.pm'
.temp 70
.option post
.probe I(*) V(*)
**********************************************
* Netlist
**********************************************
Vin a gnd
Vdd vdd gnd 'SUPPLY'
M1 y a gnd gnd NMOS W=4 L=2
M2 y a vdd  vdd PMOS W='N1*4' L=2
**********************************************
* 激励
**********************************************
.DC Vin 0 'SUPPLY' 0.01 sweep N1 2 30 2
**********************************************
* 测量
**********************************************
*噪声容限
.measure DC vm  FIND V(a) WHEN V(a)=V(y)
.measure DC vil FIND V(a) WHEN deriv('V(y)')=-1 cross=1
.measure DC vih FIND V(a) WHEN deriv('V(y)')=-1 cross=2

.measure DC voh FIND V(y) WHEN deriv('V(y)')=-1 cross=1
.measure DC vol FIND V(y) WHEN deriv('V(y)')=-1 cross=2
.measure noisemargin_H param=('voh-vih')
.measure noisemargin_L param=('vil-vol')
*增益
.measure DC gain deriv V(y) when V(y)=Vm
.end
```





Digital I


y:n1=2 cmos
y:n1=4 cmos
y:n1=6 cmos
y:n1=8 cmos
y:n1=10 cmo
y:n1=12 cmo
y:n1=14 cmo
y:n1=16 cmo
y:n1=18 cmo
y:n1=20 cmo
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
0
-5
-10
-15
-20
-25
(lin)

An example

An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of 3.4 and with the NMOS transistor minimum size (W=0.375um, L=0.25um,W/L=1.5),Vdd=2.5V,Please give the gain of V_M, and V_{IL},V_{IH},NM_L,NM_H, VTC curve

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}} = \frac{-30 * (-1)}{115 * 0.63} * 3.4 = 1.4$$

$$g = -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)} = -\frac{1+1.4}{\left(1.25 - 0.43 - \frac{0.63}{2}\right)(0.06+0.1)}$$

$$= -\frac{2.4}{0.505 * 0.16} = -30$$

An example:Inverter Gain

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$I_D(V_M) = k_n V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})(1+\lambda_n V_{out})$$

$$= 115\times10^{-6}\times\frac{0.375}{0.25}\times0.63\times(1.25-0.43-{}^{0.63}\!/_{2})\times(1+0.06\times1.25) = 59\times10^{-6}\,\text{A}$$

$$g = \frac{1}{I_D(V_M)}\frac{k_n V_{DSAT_n} + k_p V_{DSAT_p}}{\lambda_n - \lambda_p}$$

$$= \frac{1}{59\times10^{-6}}\frac{115\times10^{-6}\times{}^{0.375}\!/_{0.25}\times0.63 + 30\times10^{-6}\times3.4\times{}^{0.375}\!/_{0.25}\times1.0}{0.06+0.1} = -27.5$$

$$\gamma = \frac{k_p' \, W_p / L_p \, V_{DSATp}}{k_n' \, W_n / L_n \, V_{DSATn}} = \frac{-30 * (-1)}{115 * 0.63} * 3.4 = 1$$

$$g = -\frac{1+\gamma}{\left(V_M - V_{Tn} - V_{DSATn}/2\right)(\lambda_n - \lambda_p)} = \frac{2}{(1.25 - 0.43 - 0.63/2)(0.06+0.1)} = -24.75$$

$$g = \frac{dV_{out}}{dV_{in}}\Big|_{V_{in}=V_M} = -\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{\lambda_n k_n V_{DSATn}\left(V_{in} - V_{Tn} - V_{DSATn}/2\right) + \lambda_p k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2\right)} =$$

$$-\frac{(1+\lambda_n V_{out}) + \gamma\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{\lambda_n\left(V_{in} - V_{Tn} - V_{DSATn}/2\right) + \lambda_p \gamma\left(V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2\right)} =$$

$$-\frac{(1+0.6*1.25) + 1*(1-0.1*1.25)}{0.06*(1.25-0.43-0.315) - 0.1(-1.25+0.4+0.5)} = -40$$

An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of 3.4 and with the NMOS transistor minimum size (W=0.375um, L=0.25um,W/L=1.5),Vdd=2.5V,Please give the gain of V_M, and V_{IL},V_{IH},NM_L,NM_H, VTC curve

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$V_{IH}=V_M-V_M/g=1.25*(1+1/30)=1.29V$

$V_{IL}=(V_{DD}-V_M)/g+V_M=-1.25/30+1.25=1.21V$

$NM_H=V_{OH}-V_{IH}=2.5-1.29=1.21V$

$NM_L=V_{IL}-V_{OL}=1.21V$

An example

*An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of **16** and with the NMOS transistor minimum size (W=0.375um, L=0.25um,**W/L=1.5**) , Vdd=2.5V , Please give the gain of **V_M**, and **V_{IL},V_{IH},NM_L,NM_H,** **VTC** curve*

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}} = \frac{-30 * (-1)}{115 * 0.63} * 16 = 6.6$$

$$V_M = \frac{\left(V_{Tn} + {V_{DSATn}}/{2}\right) + \gamma(V_{DD} + V_{Tp} + {V_{DSATp}}/{2})}{1+\gamma}$$

$$= \frac{(0.43 + 0.63/2) + 6.6 * (2.5 - 0.4 - 1/2)}{1 + 6.6} = \frac{0.745 + 6.6 * 1.6}{1 + 6.6} = 1.49$$

An example

*An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of **16** and with the NMOS transistor minimum size (W=0.375um, L=0.25um,**W/L=1.5**) , Vdd=2.5V , Please give the gain of **V_M**, and **V_{IL}**,**V_{IH}**,**NM_L**,**NM_H**, **VTC** curve*

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$g = -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n + \lambda_p)} = -\frac{1+6.6}{\left(1.49 - 0.43 - \frac{0.63}{2}\right)(0.06+0.1)}$$

$$= -\frac{7.6}{0.745 * 0.16} = -64$$

An example

*An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of **16** and with the NMOS transistor minimum size (W=0.375um, L=0.25um,**W/L=1.5**) , Vdd=2.5V , Please give the gain of **V_M**, and **V_{IL}**,**V_{IH}**,**NM_L**,**NM_H**, **VTC** curve*

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$V_{IH}=V_M-V_M/g=1.49*(1+1/64)=1.51V$

$V_{IL}=(V_{DD}-V_M)/g+V_M=-1.25/30+1.25=1.47V$

$NM_H=V_{OH}-V_{IH}=2.5-1.51=0.99V$

$NM_L=V_{IL}-V_{OL}=1.47V$

A example : noise margin

$g=-V_M/(V_{IH}-V_M)$

$V_{IH}=V_M-V_M/g=1.25*(1+1/27.5)=1.3V$

$g=-(V_{DD}-V_M)/(V_M-V_{IL})$

$V_{IL}=(V_{DD}-V_M)/g+V_M=-1.25/27.5+1.25=1.2V$

$NM_H=V_{OH}-V_{IH}=2.5-1.3=1.2V$

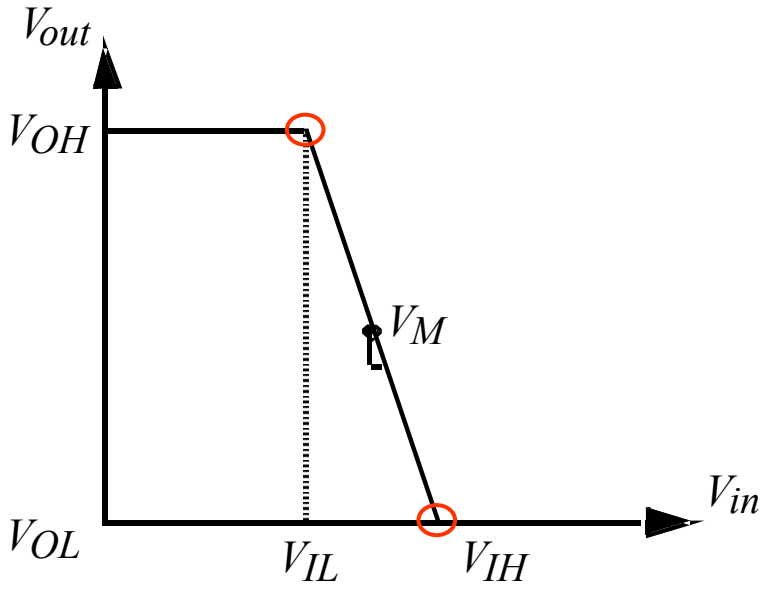
$NM_L=V_{IL}-V_{OL}=1.2V$

Simulated valued

$V_{IL}=1.03V$

$V_{IH}=1.45V$

- ***Gain is overestimated***
- ***Linear approximation of VTC***

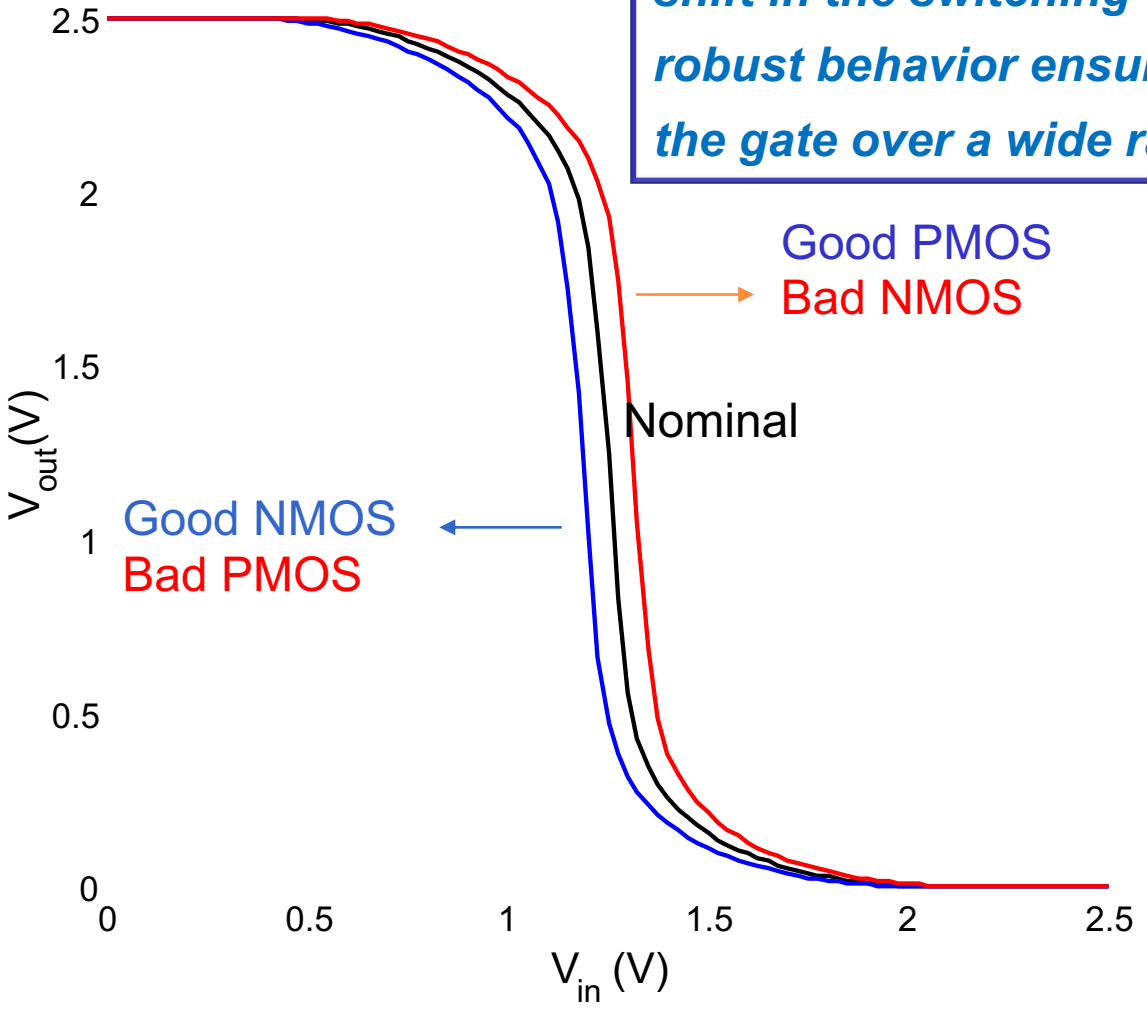


CMOS static behavior

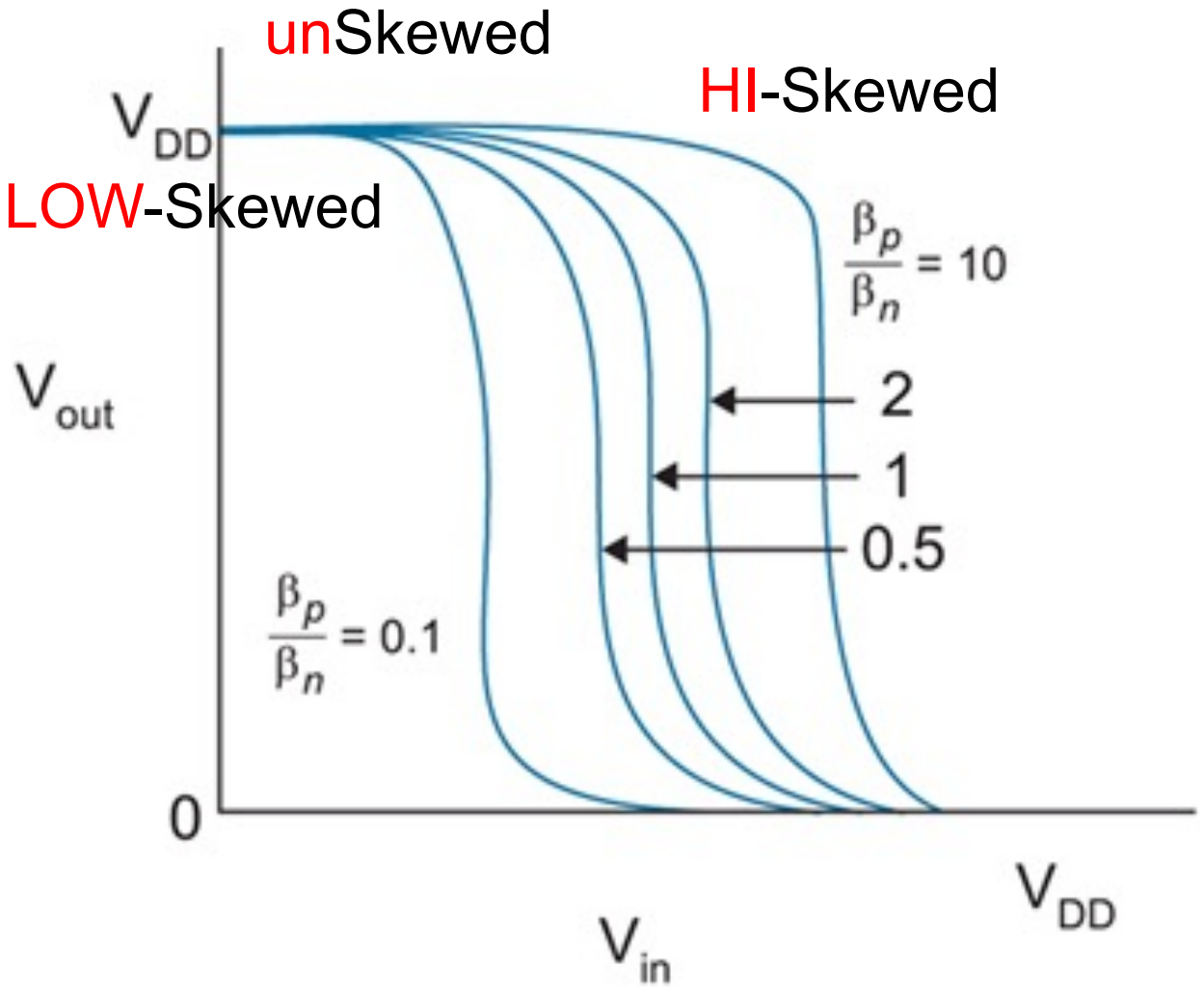
- CMOS threshold voltage
- CMOS noise margin
- CMOS gain
- ***DC robust***

Impact of Process Variations

The variations of device mainly cause a shift in the switching threshold, this robust behavior ensures functionality of the gate over a wide range of conditions

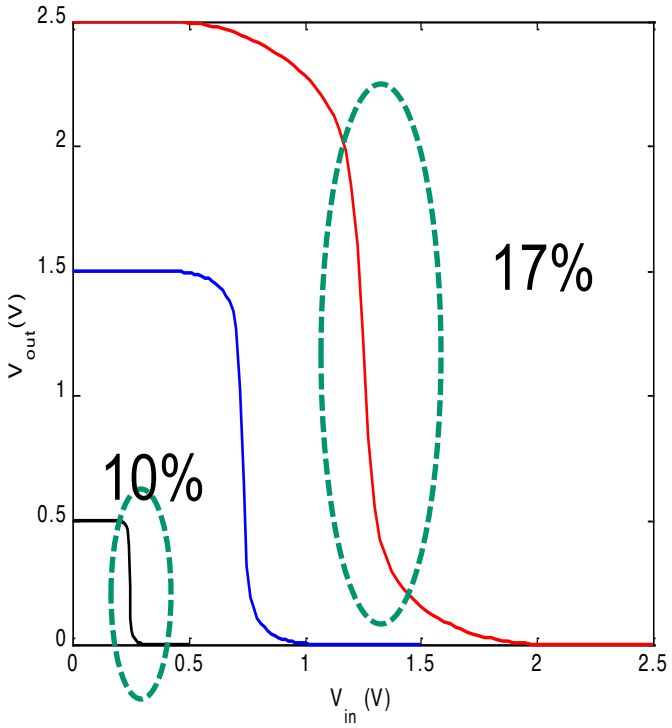


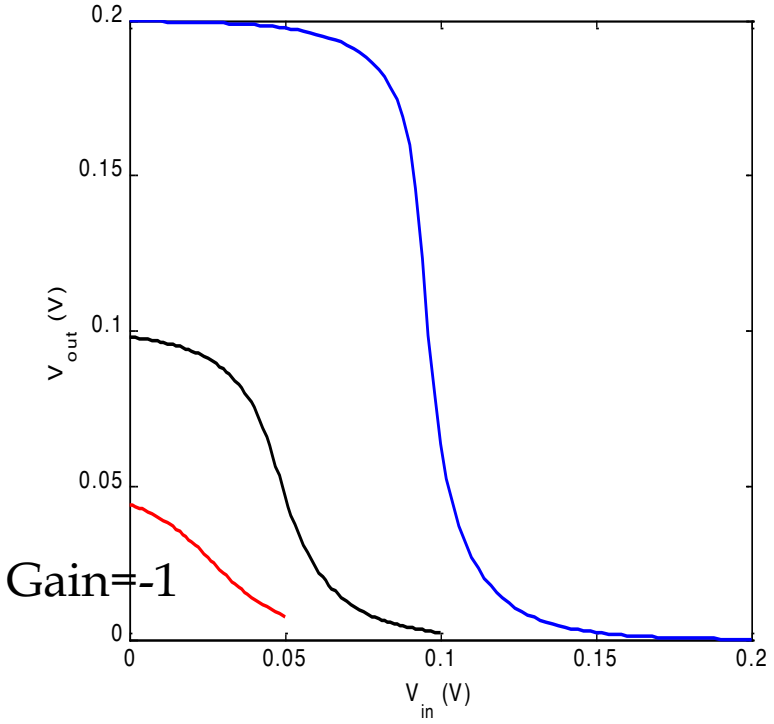
Transfer characteristics of skewed inverter



Gain as a function of V_{DD}

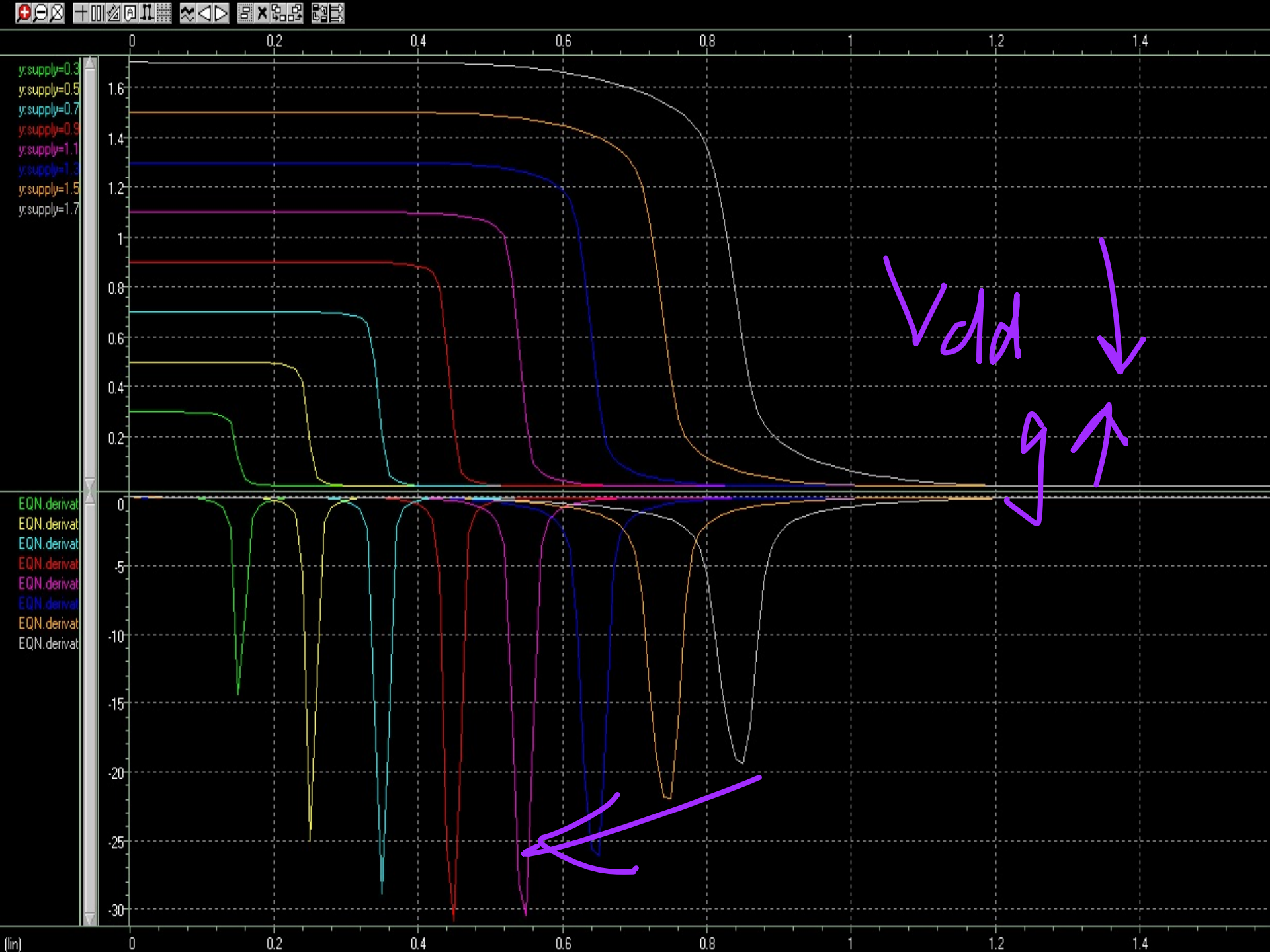
$$V_{DD\min} > 2 \sim 4 \frac{kT}{q} = 2 \sim 4 \;\; 25mV$$





$$g = -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)\left(\lambda_n + \lambda_p\right)}$$

Low power voltage is useful!
But not too low


y:supply=0.3
y:supply=0.5
y:supply=0.7
y:supply=0.9
y:supply=1.1
y:supply=1.3
y:supply=1.5
y:supply=1.7
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
-5
-10
-15
-20
-25
-30
(lin)
Vdd ↓
g ↑