# Digital Integrated Circuits

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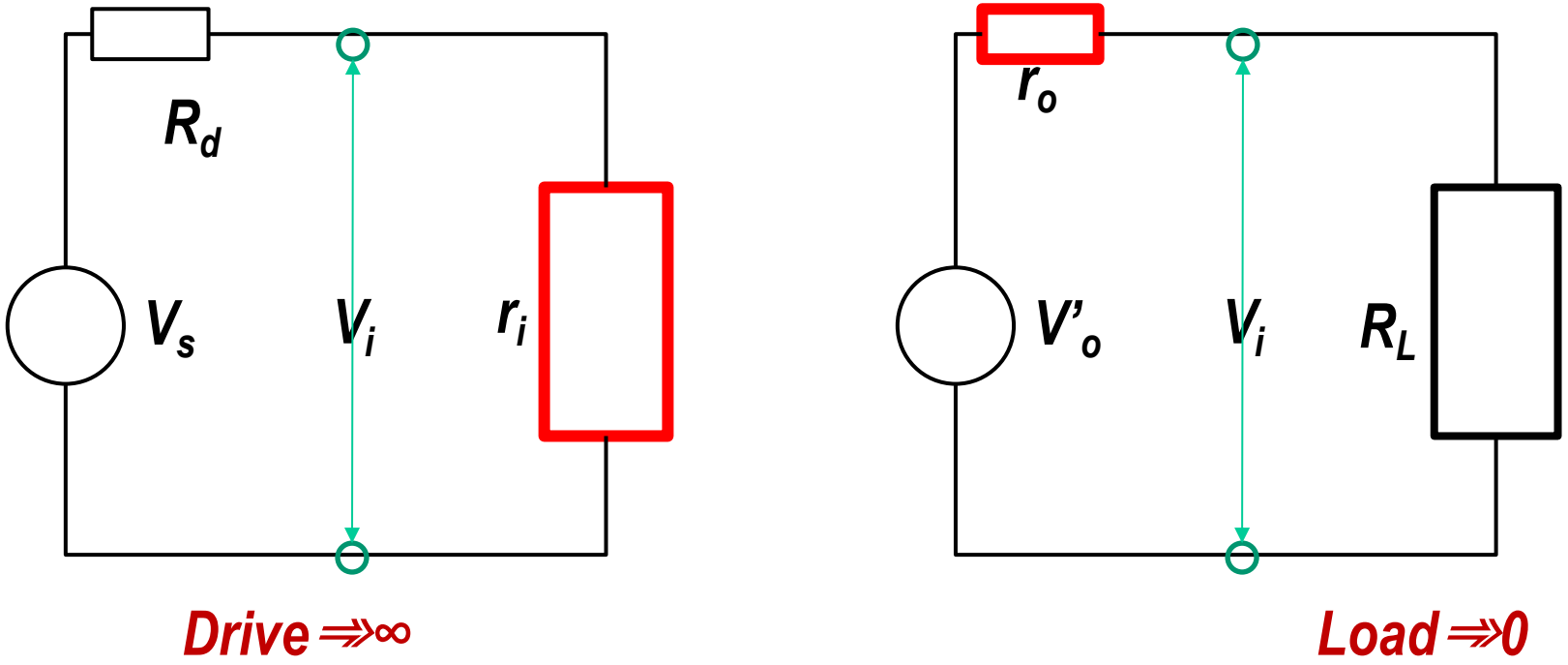
# Review content

- Format
  - Concept 40, Computing 60
  - 2++ hours
  - Mon. 8th 09:50-12:00
- Content
  - Introduction
  - Device
  - Inverter

# Input&output resistance



# Input&output resistance

- The voltage of the input signal comes,the gate could be regarded as load of front gate
- Set Empty load of current gate,calcutate VI rate
- Input resistance

$$V_i = \frac{r_i}{R_s + r_i} V_s$$

***Greater*** *input resistance, signal transfer ,less signal attenuation*

- Output resistance

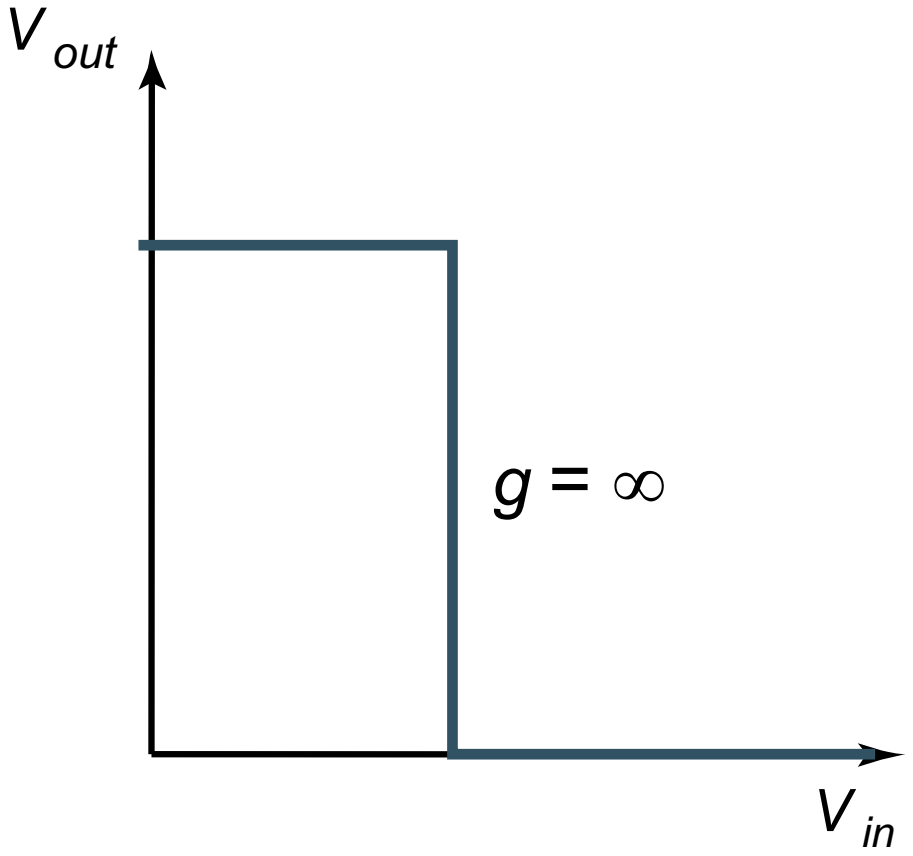
***What is its meaning?***

$$V_o = \frac{R_L}{r_o + R_L} V_o'$$

***Less*** *of the gate output resistance, smaller affect with load*

***Input(drive) re. is more greater than output(load)***

# The Ideal Gate




$R_i = \infty$

$R_o = 0$

$Fanout = \infty$

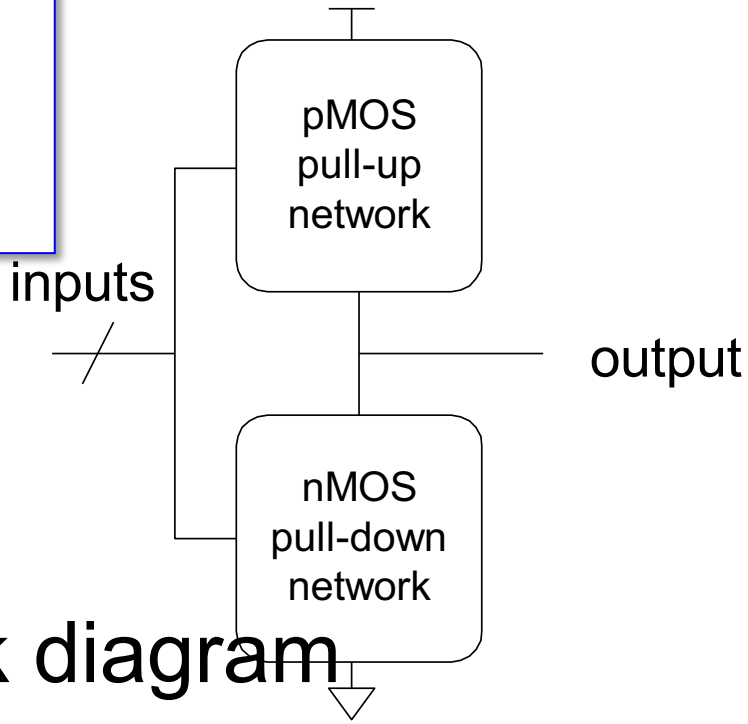
$NM_H = NM_L = V_{DD}/2$

# Complementary CMOS

nMOS pull-down network

pMOS pull-up network

a.k.a. static CMOS

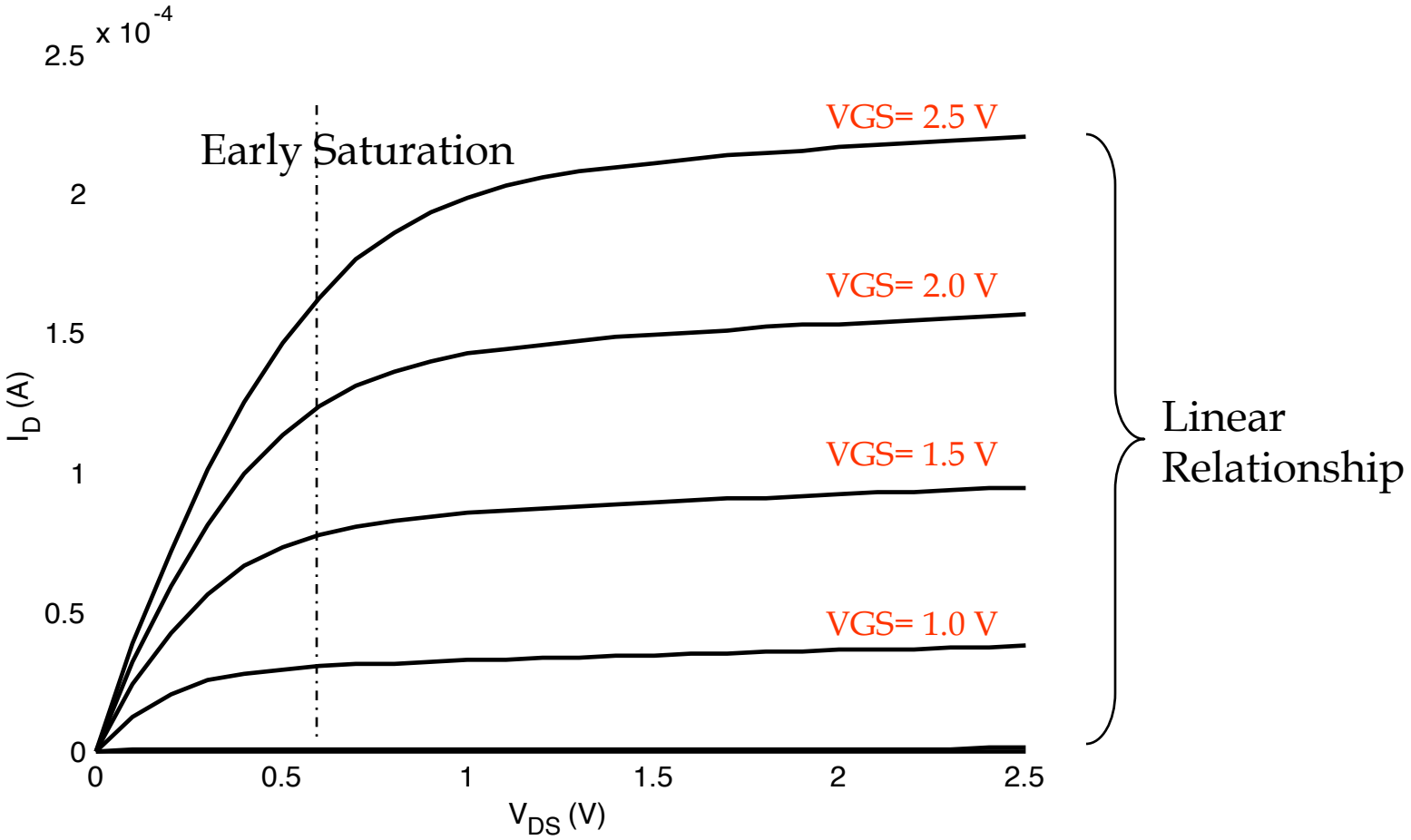



- CMOS circuit layout/stick diagram
- Why NMOS/PDN  PMOS/PUN

# Device

- All state and principle
- Velocity saturation
- I-V formula (Hight-K Low-K material )
- Gate Capacitance

# Current-Voltage Relations
# The Deep-Submicron Era



# Attention : velocity position

$$\mu_n = 3800\,\mathrm{cm}^2/\mathrm{v.s}, \mu_p = 1800\,\mathrm{cm}^2/\mathrm{v.s}$$

Charge per unit area: $$Q_i(x) = -C_{ox}[V_{gs} - V(x) - V_T]$$

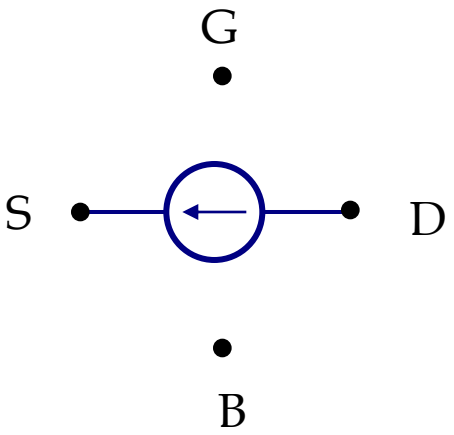
$$I_D = -v_n(x)Q_i(x)W \qquad v_n(x) = \mu_n E(x) = \mu_n \frac{dV}{dx}$$

$$I_D = \mu_n \frac{dV}{dx} C_{ox}[V_{gs} - V(x) - V_T]W$$

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{ox}[V_{gs} - V(x) - V_T]W dV$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]\kappa(V_{DSAT})$$

# A unified model for manual analysis




$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

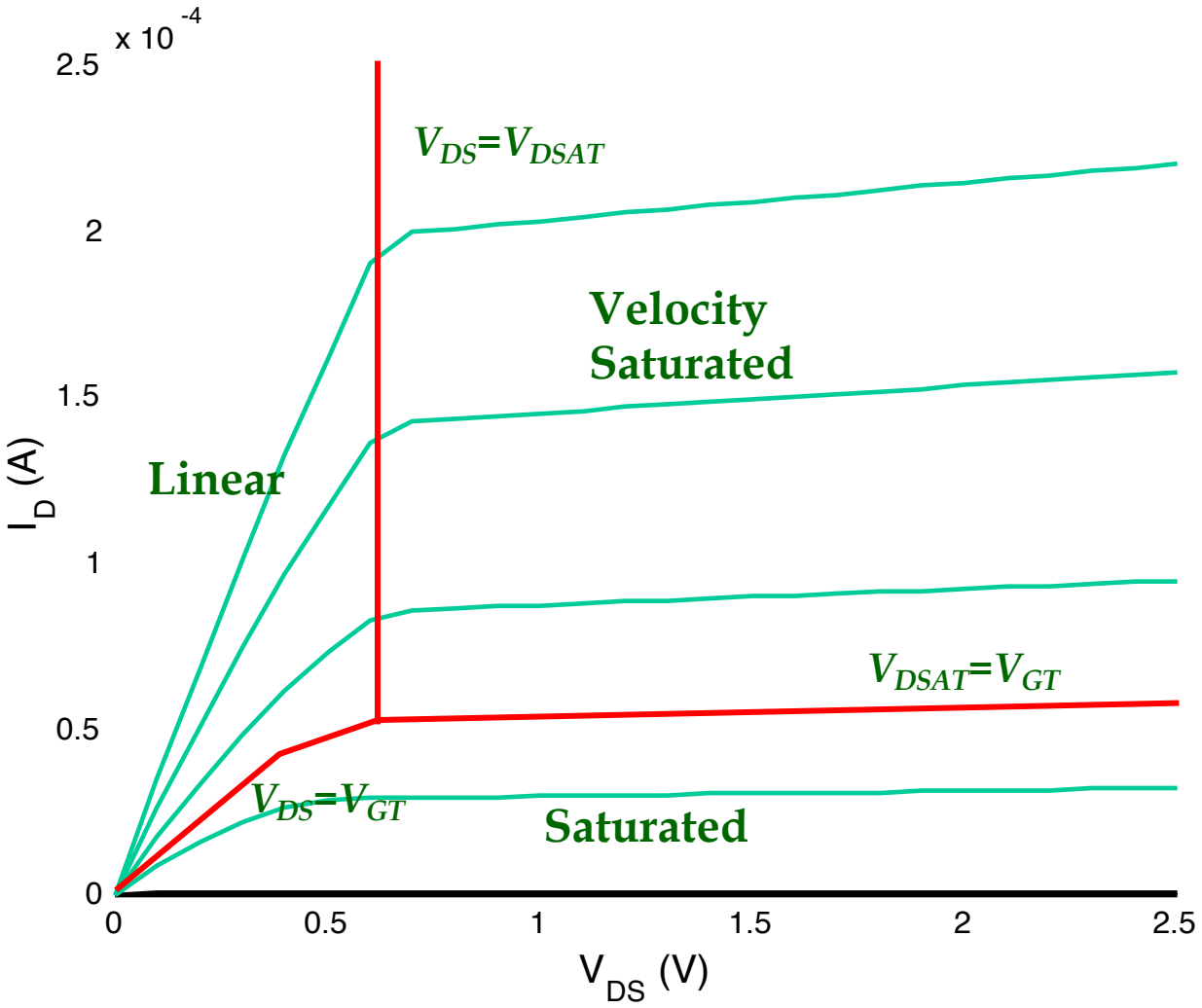
$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

**Table 3.2** Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

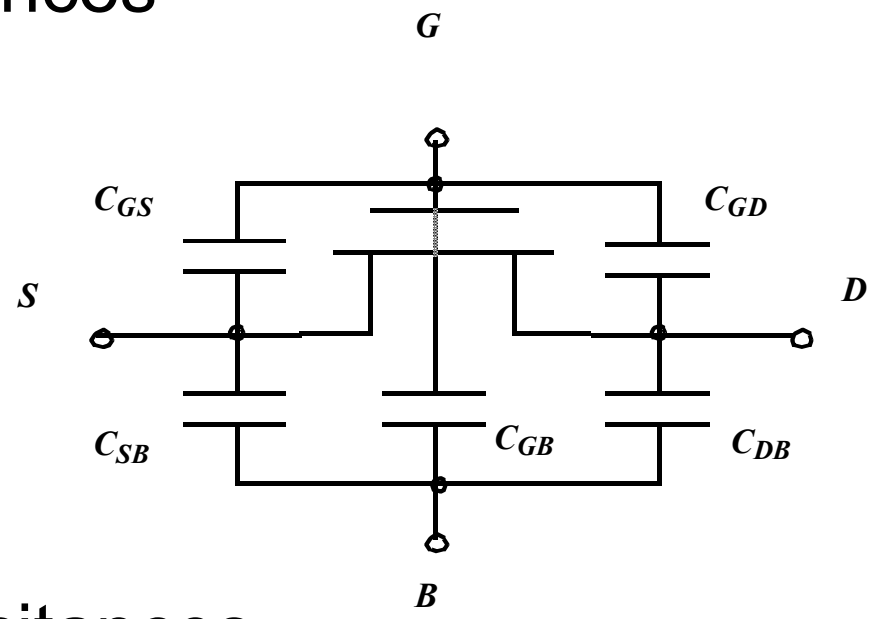
| | $V_{T0}$ (V) | $\gamma$ ($V^{0.5}$) | $V_{DSAT}$ (V) | $k'$ ($A/V^2$) | $\lambda$ ($V^{-1}$) |
|---|---|---|---|---|---|
| NMOS | 0.43 | 0.4 | 0.63 | $115 \times 10^{-6}$ | 0.06 |
| PMOS | −0.4 | -0.4 | -1 | $-30 \times 10^{-6}$ | -0.1 |

# Simple Model versus SPICE

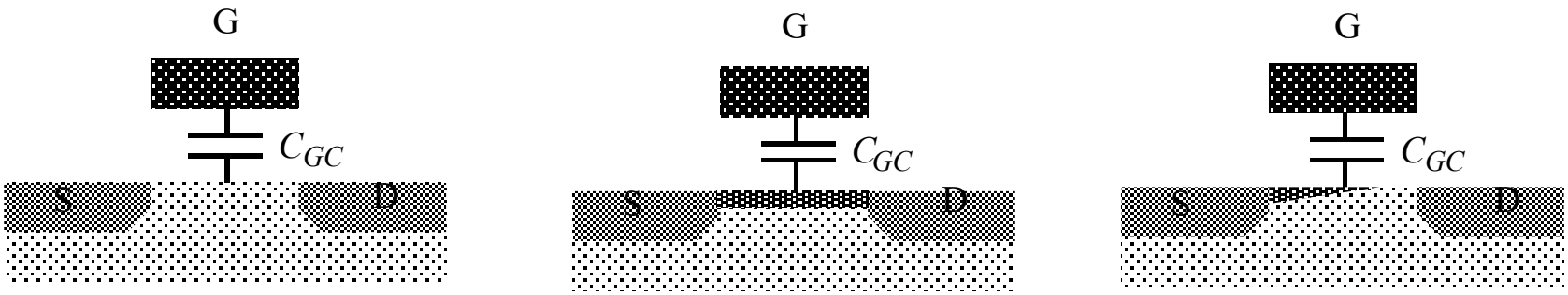


# Capacitance components

- MOS structure capacitances
  - Overlap cap.
- Channel capacitances
  - Gate-body cap.
  - Gate-source cap.
  - Gate-drain cap.
- Junction/diffusion capacitances
  - Bottom-plate cap.
  - Side-well cap.



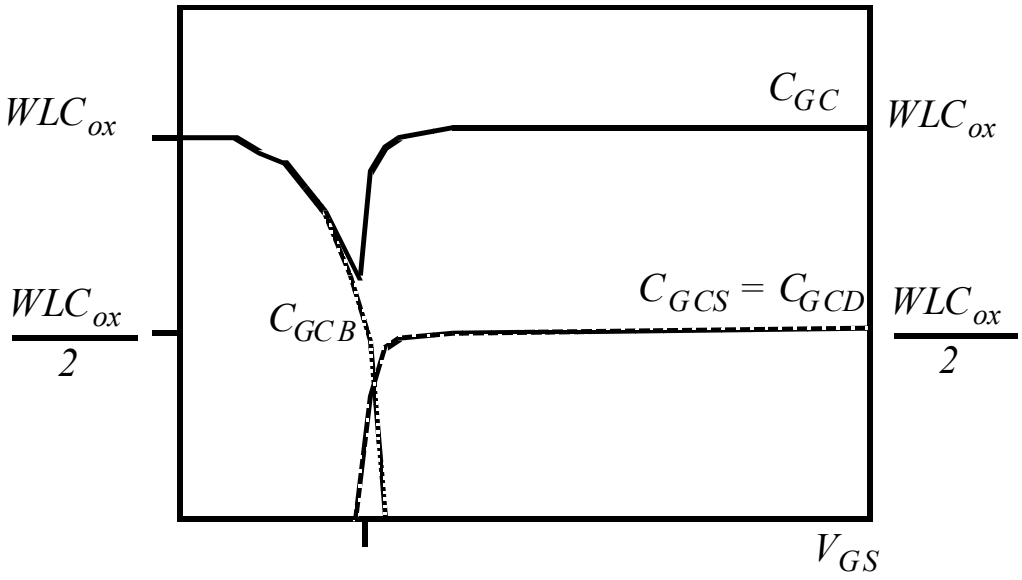
# Gate channel Capacitance



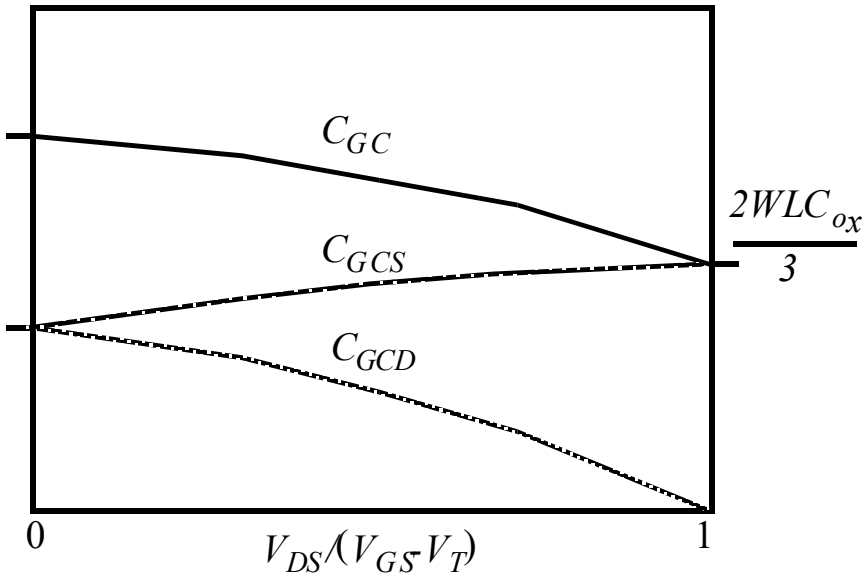

| Operation Region | $C_{gb}$ | $C_{gs}$ | $C_{gd}$ |
|---|---|---|---|
| Cutoff | $C_{ox}WL_{eff}$ | 0 | 0 |
| Triode | 0 | $C_{ox}WL_{eff}/2$ | $C_{ox}WL_{eff}/2$ |
| Saturation | 0 | $(2/3)C_{ox}WL_{eff}$ | 0 |

*Most important regions in digital design: saturation and cut-off*

# Gate Capacitance




Capacitance as a function of $V_{GS}$ (with $V_{DS} = 0$)

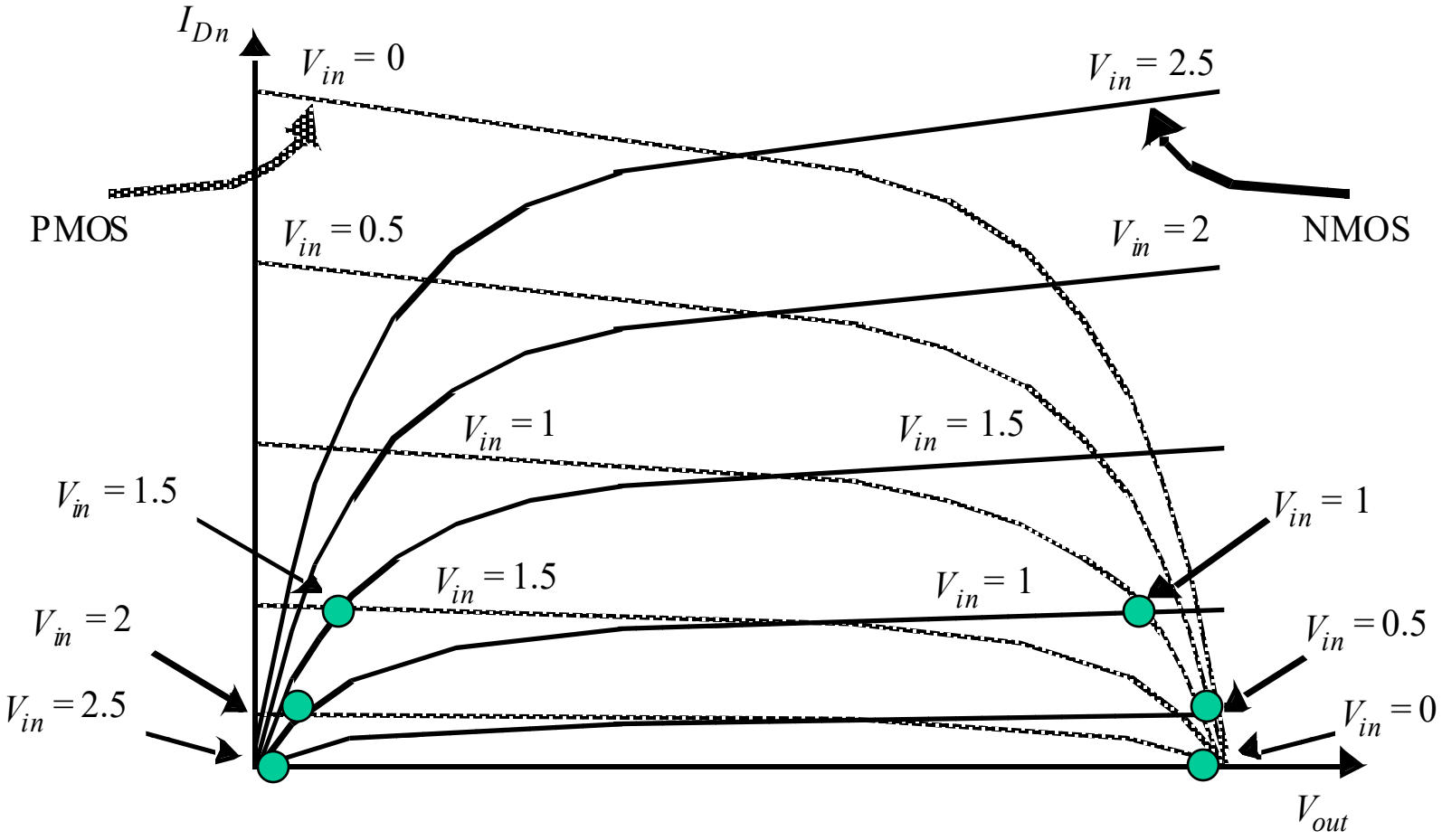



Capacitance as a function of the degree of saturation

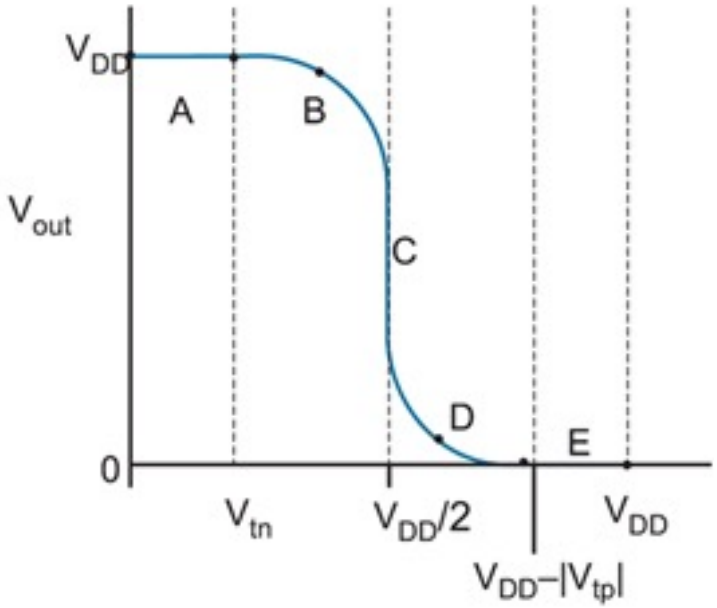
# CMOS static behavior

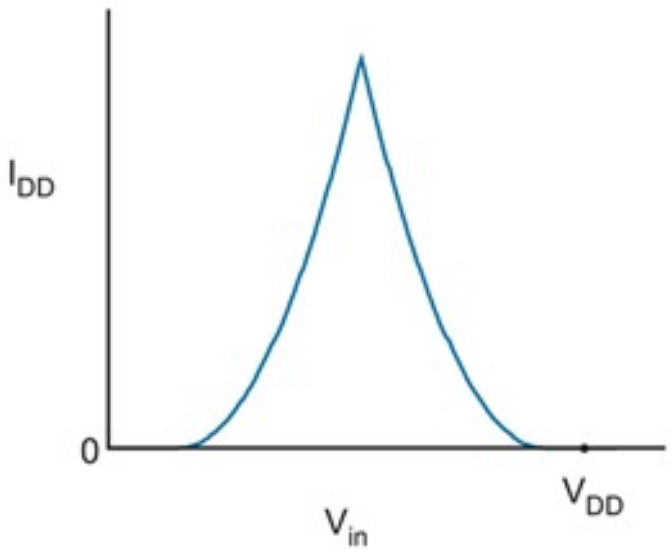
- *CMOS threshold voltage*
- *CMOS noise margin*
- *CMOS gain*
- *DC robust*
- *Inverter Chain*
- *Power*

# CMOS Inverter Load Characteristics



# CMOS Inverter VTC




| Summary of CMOS inverter operation | | | | |
|---|---|---|---|---|
| Region | Condition | P-device | N-device | output |
| A | [0,Vtn] | linear | cutoff | VDD |
| B | [Vtn,VDD/2] | linear | saturated | VDD/2 |
| C | =VDD/2 | saturated | saturated | X drop |
| D | [VDD/2,VDD-\|VTP\|] | saturated | linear | <VDD/2 |
| E | [VDD-\|VTP\|, VDD] | cutoff | linear | 0 |

# Switching Threshold as a function of Transistor Ratio

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right] = v_{sat} C_{ox} W\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]$$

$$k_n V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2}) + k_p V_{DSAT_p}(V_M - V_{DD} - V_{Tp} - \frac{V_{DSAT_p}}{2}) = 0$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSAT_n}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSAT_p}}{2})}{1 + r} \qquad r = \frac{k_p V_{DSAT_p}}{k_n V_{DSAT_n}}$$

$$V_M \approx \frac{r V_{DD}}{1 + r}$$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})}{k_p' V_{DSAT_p}(V_{DD} - V_M + V_{Tp} + \frac{V_{DSAT_p}}{2})}$$

# Switching threshold of CMOS inverter

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

| | $V_{T0}(V)$ | $\gamma(V^{0.5})$ | $V_{DSAT}(V)$ | $k'(A/V^2)$ | $\lambda(V^{-1})$ |
|---|---|---|---|---|---|
| *NMOS* | 0.43 | 0.4 | 0.63 | $115X10^{-6}$ | 0.06 |
| *PMOS* | -0.4 | -0.4 | -1 | $-30X10^{-6}$ | -0.1 |

***Assuming $W_p/W_n$=8, calculating $V_M$=?***

$$r = \frac{k_p' \, W_p/L_p \, V_{DSAT_p}}{k_n' \, W_n/L_n \, V_{DSAT_n}} = \frac{-30*(-1)}{115*0.63} * 8 = 3.3$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSAT_n}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSAT_p}}{2})}{1+r}$$

$$= \frac{(0.43 + \frac{0.63}{2}) + 3.3(2.5 - 0.4 - \frac{0.4}{2})}{1+3.3} = \frac{0.75 + 3.3*1.9}{1+3.3} = 1.63V$$

# Switching threshold of CMOS inverter

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

| | $V_{T0}(V)$ | $\gamma(V^{0.5})$ | $V_{DSAT}(V)$ | $k'(A/V^2)$ | $\lambda(V^{-1})$ |
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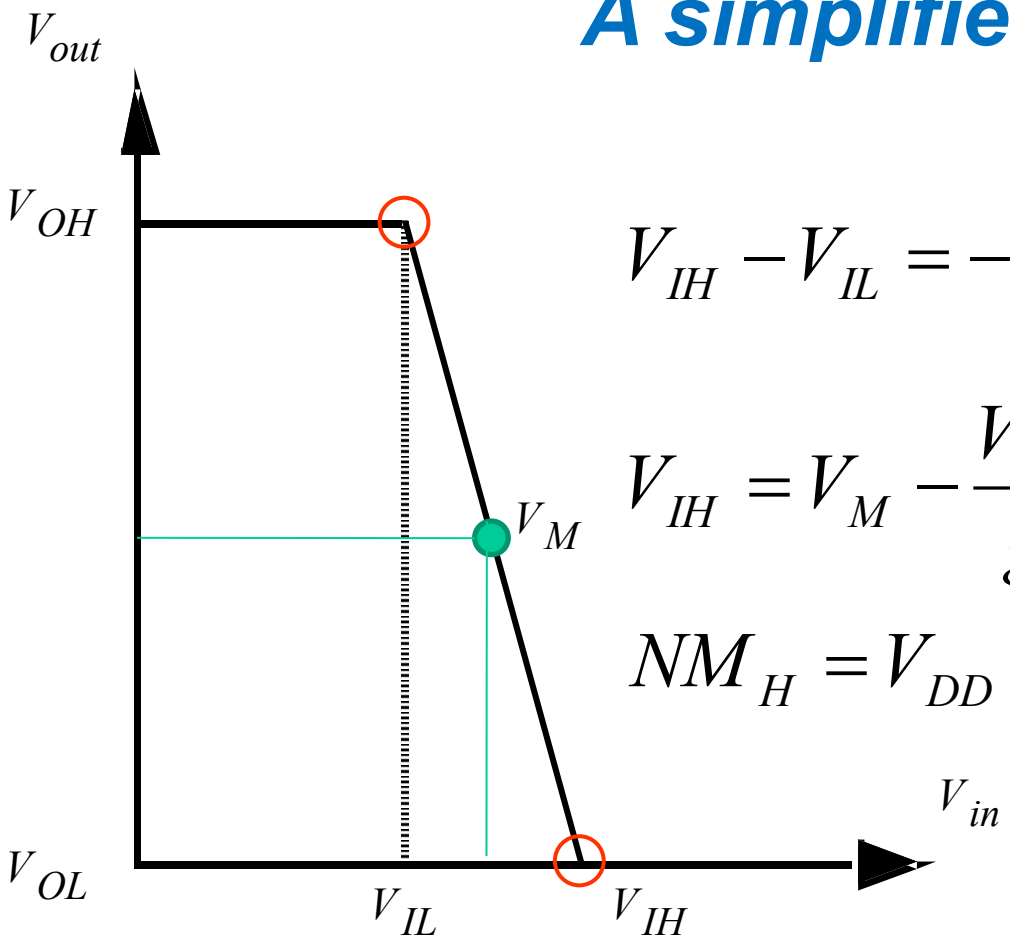
$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})}{-k_p' V_{DSAT_p}(V_{DD} - V_M + V_{Tp} + \frac{V_{DSAT_p}}{2})} = \frac{115\times10^{-6}\times0.63\times(1.25-0.43-\frac{0.63}{2})}{30\times10^{-6}\times1\times(1.25-0.4-\frac{1}{2})} = 3.5$$

***This rate let $V_M=V_{dd}/2$!***

# Determining $V_{IH}$ and $V_{IL}$




***A simplified approach!***

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g}, V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH}, NM_L = V_{IL}$$

# Example

***g=-30, $V_{dd}$=2.5V, $V_M$=1.0V Please estimate $NM_H$ and $NM_L$***

$V_{IH}=V_M-V_M/G=1.0*(1+1/30)=1.03V$

$V_{IL}=(V_{DD}-V_M)/G+V_M=-1.5/30+1.0=0.95V$

$NM_H=V_{OH}-V_{IH}=2.5-1.03=1.47V$

$NM_L=V_{IL}-V_{OL}=0.95V$

# Inverter Gain

$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M}$$

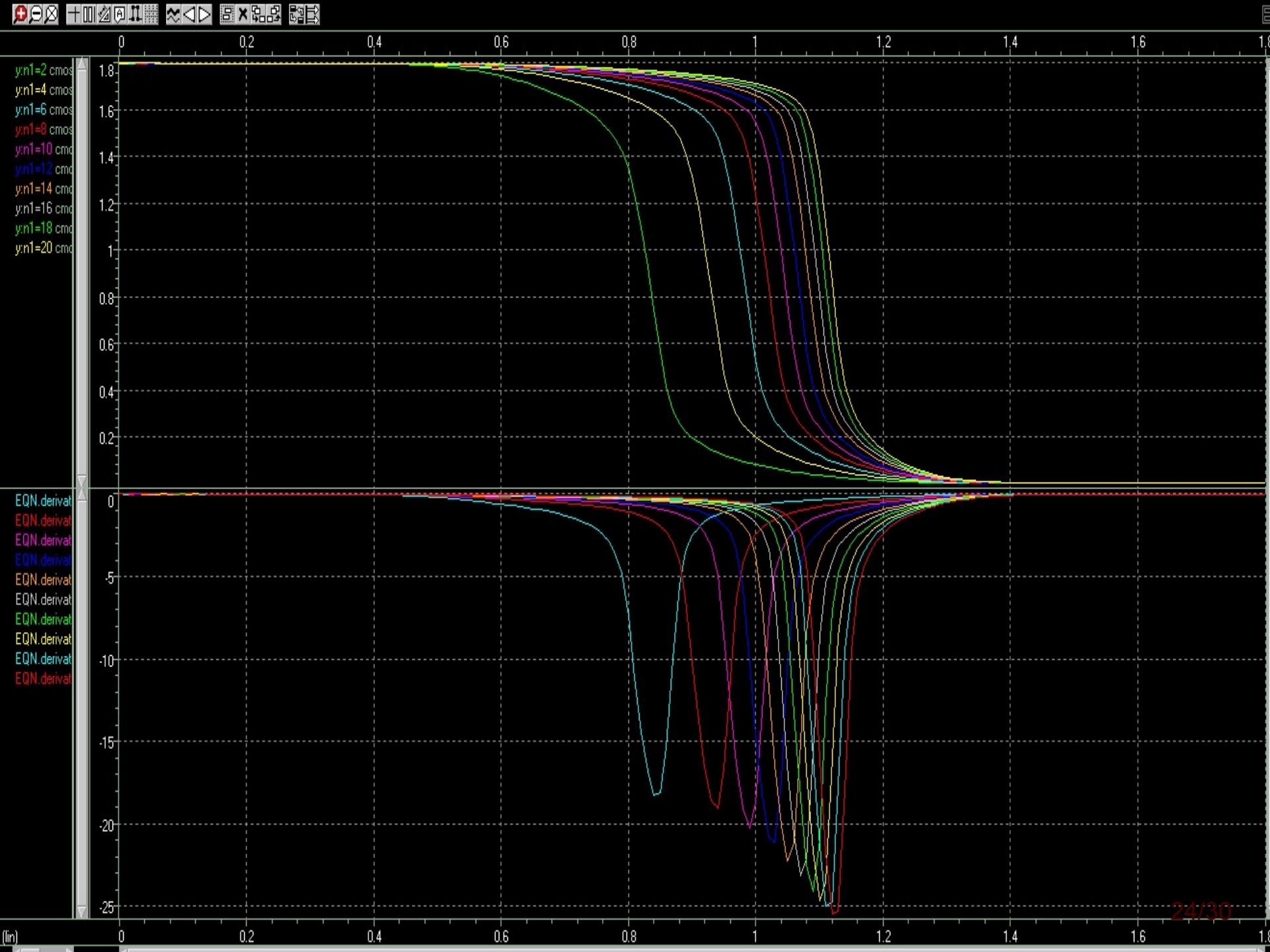
$$= -\left.\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{\lambda_n k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right) + \lambda_p k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - {V_{DSATp}}/{2}\right)}\right|_{V_{in}=V}$$

$$\approx -\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

$$= -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

**Ratio increase, Gain increase**

$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}}$$


y:n1=2 cmos
y:n1=4 cmos
y:n1=6 cmos
y:n1=8 cmos
y:n1=10 cmo
y:n1=12 cmo
y:n1=14 cmo
y:n1=16 cmo
y:n1=18 cmo
y:n1=20 cmo
EQN.derivat
EQN.derivat
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EQN.derivat
EQN.derivat
EQN.derivat
EQN.derivat
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
-5
-10
-15
-20
-25
(lin)
24/30

# An example

*An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of 3.4 and with the NMOS transistor minimum size (W=0.375um, L=0.25um,W/L=1.5),Vdd=2.5V,Please give the gain of $V_M$, and $V_{IL}$,$V_{IH}$,$NM_L$,$NM_H$, VTC curve*

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

| | $V_{T0}$(V) | $\gamma$($V^{0.5}$) | $V_{DSAT}$(V) | k'($A/V^2$)) | $\lambda$($V^{-1}$) |
|---|---|---|---|---|---|
| *NMOS* | 0.43 | 0.4 | 0.63 | $115X10^{-6}$ | 0.06 |
| *PMOS* | -0.4 | -0.4 | -1 | $-30X10^{-6}$ | -0.1 |

$$\gamma = \frac{k_p' \left. W_p \right/ L_p \, V_{DSATp}}{k_n' \left. W_n \right/ L_n \, V_{DSATn}} = \frac{-30 * (-1)}{115 * 0.63} * 3.4 = 1.4$$

$$g \approx -\frac{1+\gamma}{\left(V_M - V_{Tn} - \left. V_{DSATn} \right/ 2\right)(\lambda_n - \lambda_p)} = -\frac{1+1.4}{\left(1.25 - 0.43 - \frac{0.63}{2}\right)(0.06+0.1)}$$

$$= -\frac{2.4}{0.505 * 0.16} = -30$$

# tpHL/tpLH

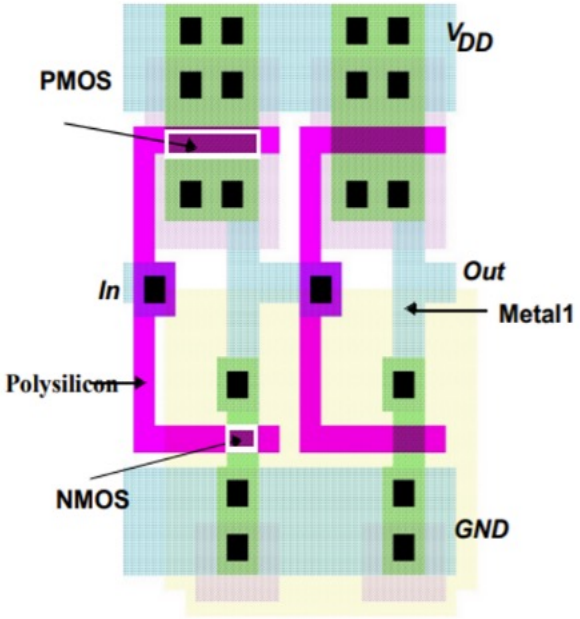


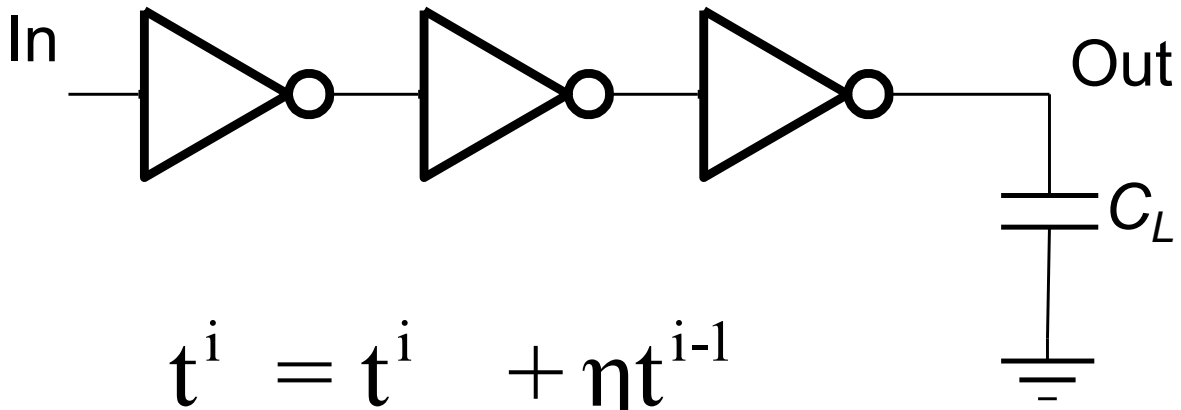

Figure 1

## Computing the Capacitances

| capacitor | expression | Value(fF) (H->L) | Value(fF) (L->H) |
|---|---|---|---|
| $C_{gd1}$ | $2C_{GD0_n}*W_n$ | 0.23 | 0.23 |
| $C_{gd2}$ | $2C_{GD0_p}*W_p$ | 0.61 | 0.61 |
| $C_{db1}$ | $K_{eqn}AD_nC_J+K_{eqwn}PD_nC_{JSW}$ | 0.66 | 0.90 |
| $C_{db2}$ | $K_{eqn}AD_nC_J+K_{eqwn}PD_nC_{JSW}$ | 1.5 | 1.15 |
| $C_{g3}$ | $(C_{GD0_n}+C_{GSO_n})W_n+C_{ox}W_nL_n$ | 0.76 | 0.76 |
| $C_{g4}$ | $(C_{GD0_p}+C_{GSO_p})W_p+C_{ox}W_pL_p$ | 2.28 | 2.28 |
| $C_w$ | | 0.12 | 0.12 |
| $C_L$ | | 6.1 | 6.0 |

Table 1

# Inverter Chain




$$t_p^i = t_{step}^i + \eta t_{step}^{i-1}$$

***If $C_L$ is given:***

***- How many stages are needed to minimize the delay?***

***- How to size the inverters?***

# CMOS Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage} 1/f_{clock}$$

$$f_{0\rightarrow1} = P_{0\rightarrow1} * f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage}$$

***Dynamic power*** ***Short-circuit power*** ***Leakage power***

# Lowering Dynamic Power

***Capacitance:***
***Function of fan-out, wire length, transistor sizes***

***Supply Voltage:***
***Has been dropping with successive generations***

$$P_{dyn} = C_L V_{DD}^2 P_{0\rightarrow1} f$$

***Activity factor:***
***How often, on average, do wires switch?***

***Clock frequency:***
***Increasing…***

| Parameter | Relation | Full Scaling | General Scaling | Fixed Voltage Scaling |
|---|---|---|---|---|
| $W, L, t_{ox}$ | | 1/S | 1/S | 1/S |
| $V_{DD}, V_T$ | | 1/S | 1/U | 1 |
| $N_{SUB}$ | $V/W_{depl}^2$ | S | $S^2/U$ | $S^2$ |
| Area/Device | WL | $1/S^2$ | $1/S^2$ | $1/S^2$ |
| $C_{ox}$ | $1/t_{ox}$ | S | S | S |
| $C_L$ | $C_{ox}WL$ | 1/S | 1/S | 1/S |
| $k_n, k_p$ | $C_{ox}W/L$ | S | S | S |
| $I_{av}$ | $k_{n,p} V^2$ | 1/S | $S/U^2$ | S |
| $t_p$ (intrinsic) | $C_L V / I_{av}$ | 1/S | $U/S^2$ | $1/S^2$ |
| $P_{av}$ | $C_L V^2 / t_p$ | $1/S^2$ | $S/U^3$ | S |
| PDP | $C_L V^2$ | $1/S^3$ | $1/SU^2$ | 1/S |