Evaluation of TFET and FinFET Devices and 32-Bit CLA Circuits Considering Work Function Variation and Line-Edge Roughness

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***Abstract*—In this paper, we comprehensively investigate the impacts of work function variation (WFV) and fin line-edge roughness (fin LER) on III-V homojunction tunnel FET (TFET) and FinFET devices and 32-bit carry-look-ahead adder (CLA) circuits operating in near-threshold region using atomistic 3D TCAD mixed-mode simulations and HSPICE simulations with look-up table based Verilog-A models calibrated with TCAD simulation results. The results indicate that at low operating voltage (< 0.3V), the CLA circuit delay and power-delay product (PDP) of TFET are significantly better than FinFET even with the impacts of random variations. As the operating voltage decreases, the performance advantage of TFET CLA becomes more significant due to its better I_{on} and $C_{g,ave}$ and their smaller variability. However, the leakage power of TFET CLA is larger than FinFET CLA due to the worse I_{off} variability of TFET devices.**

I. INTRODUCTION

Steep subthreshold slope TFET, which utilizes the band-to-band tunneling as the conduction mechanism, is one of the most promising candidates for ultra-low voltage/power applications [1]. Recent research works on TFET based circuits have shown significant performance improvement and power reduction at low operating voltage [2-4].

With device scaling, the impacts of random variations become more severe. Several studies on the variability of TFET devices have been reported [5-6], while other works on TFET circuits employed simple parameter sensitivity methods that neglect physical non-uniformities [2, 7], and a physics-based TFET performance and variability assessment for large logic circuits is lacking. Among all variation sources, the WFV and fin LER have the most significant impacts on TFET and FinFET devices. In this work, we provide an in-depth physics-based assessment on the impacts of WFV and fin LER on TFET and FinFET devices and 32-bit CLA circuits.

II. DEVICE STRUCTURES AND CHARACTERISTICS

The basic TFET structure under study comprises a gated p-i-n tunnel diode under reverse bias with asymmetrical source/drain doping. For n-type TFET, the source is p+ region with dominant electron conduction, the channel is gated intrinsic region, and the drain is n+ region. When N-TFET is "OFF" (V_{GS}=0), the valence band edge of the source is below the conduction band edge of the channel, and the band-to-band tunneling probability is low due to lack of available states in the channel region and wide barrier at source-channel junction. When N-TFET is "ON" (V_{GS}>0), the conduction band edge of the channel is pulled down below the valence band edge of the source, and carriers can tunnel into available empty states of the channel region. For P-TFET, the source is n+ region with dominant hole conduction, applying V_{GS}<0 turns P-TFET "ON". The band diagrams of TFET in ON/OFF states are shown in Fig. 1.

We consider the $In_{0.53}Ga_{0.47}As$ homojunction N-TFET and $Ge_{0.925}Sn_{0.075}$ homojunction P-TFET due to their high I_{on} and compatible I_{DS}-V_{GS} characteristic. $In_{0.53}Ga_{0.47}As$ N-FinFET and Ge P-FinFET are considered for comparison. Fig. 2 shows the 3D TFET and FinFET device structures constructed for atomistic TCAD simulations. The device parameters and doping are shown in TABLE I. We use the non-local band-to-band tunneling model which is applicable to arbitrary tunneling barrier with non-uniform electric field for TFET simulations [9], and the parameters used in the model are calibrated with [10-11]. Fig. 3 shows the I_{DS}-V_{GS} characteristics of TFETs and FinFETs with comparable I_{off} at V_{DS} = 0.3V.

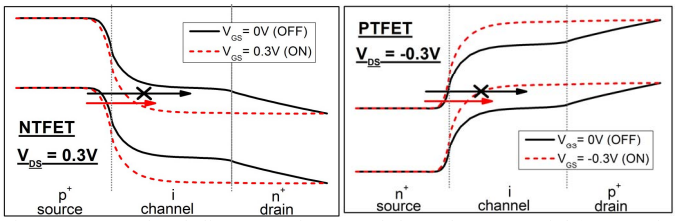

Fig. 1. Energy band diagrams of n-type (left) and p-type (right) TFET in ON/OFF state.

TABLE I. PARAMETERS OF TFET AND FINFET DEVICES

TFET and FinFET			
L_{eff} = 25nm	**W_{fin}** = 7nm	**H_{fin}** = 20nm	**EOT** = 0.65nm
	nTFET	***pTFET***	***FinFET***
Nch (cm^{-3})	undoped	undoped	1E17
Ns (cm^{-3})	4.5E19 (p-type)	1E20 (n-type)	1E20
Nd (cm^{-3})	2E17 (n-type)	2E17 (p-type)	1E20

III. SIMULATION METHODOLOGY

To assess WFV, we use the Vonoroi grain pattern [12] for TiN gate material, which has two different grain orientations <200> and <111> with the probability of 60% and 40%, respectively, as shown in Fig. 4(a) by the yellow and orange regions, and the relevant parameters are shown in TABLE II. To assess fin LER, the rough line edge patterns are generated by Fourier synthesis approach [13] with correlation length (Λ) =20nm and root-mean-square amplitude (Δ) =1.5nm as shown in Fig. 4(b). We analyze the impacts of WFV and fin LER on devices using 3D atomistic TCAD mixed-mode Monte-Carlo simulations with 100 samples, respectively.

TCAD mixed-mode simulations for complex circuits with large transistor counts face the challenges of computation resources, prohibitively long simulation times and convergence problems. To overcome these obstacles, look-up table based Verilog-A model has been employed for TFET circuit simulations in some studies [2, 4]. The approach, however, is not physics-based, and the Verilog-A model cannot accurately describe the physical non-uniformities and variability. In this work, the transfer characteristics of TFET and FinFET devices

and their variability with WFV and fin LER are extracted from atomistic 3D TCAD device simulations with $I_{ds}(V_{gs}, V_{ds})$, $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ characteristics across wide range of voltage to build two-dimensional Verilog-A look-up tables. The flow chart for small signal Verilog-A model generation is shown in Fig. 5. Finally, the Verilog-A models of devices with random variation are employed in HSPICE circuit simulations.

IV. Device Variability due to WFV and Fin LER

A. I_{off} and I_{on} Variability

Fig. 6 shows the impacts of WFV and fin LER on I_{DS}-V_{GS} dispersions of TFET and FinFET devices at V_{DS} = 0.3V. Fig. 7 illustrates the probability distributions of I_{on} (I_{DS} at $V_{DS} = V_{GS}$ = 0.3V) and I_{off} (I_{DS} at V_{DS} = 0.3V and V_{GS} = 0V). Note that, for TFET variability, the different structure constructs used for WFV and fin LER lead to slightly different nominal I_{DS}-V_{GS} curves. Therefore, the corresponding probability distributions show two nominal values. The mean values (μ), standard deviations (σ) and the ratio of the mean-to-standard deviation (μ/σ) are listed in the table with the figures.

For FinFETs, the V_t is a linear function of gate WF, WFV

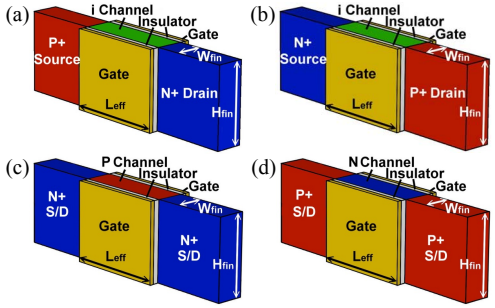

Fig. 2. Physical structures of (a) $In_{0.53}Ga_{0.47}As$ homojunction N-TFET, (b) $Ge_{0.925}Sn_{0.075}$ homojunction P-TFET, (c) $In_{0.53}Ga_{0.47}As$ N-FinFET and (d) Ge P-FinFET.

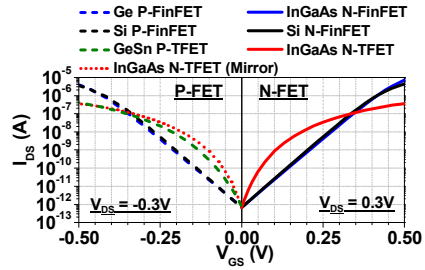

Fig. 3. I_{DS}-V_{GS} characteristics at V_{DS}=0.3V of $In_{0.53}Ga_{0.47}As$ N-TFET, $Ge_{0.925}Sn_{0.075}$ P-TFET, Si N/P-FinFET, $In_{0.53}Ga_{0.47}As$ N-FinFET and Ge P-FinFET.

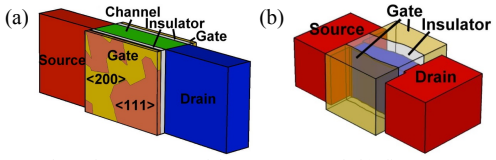

Fig. 4. Examples of structures with (a) WFV and (b) fin LER.

TABLE II. Parameters for WFV Simulations

Gate Material = TiN		**Grain Size** = 5nm	
Work function (eV)	***Nominal***	***<200> (60%)***	***<111> (40%)***
InGaAs N-TFET	4.53	4.61	4.41
GeSn P-TFET	4.82	4.9	4.7
InGaAs N-FinFET	4.88	4.96	4.76
Ge P-FinFET	4.27	4.35	4.15

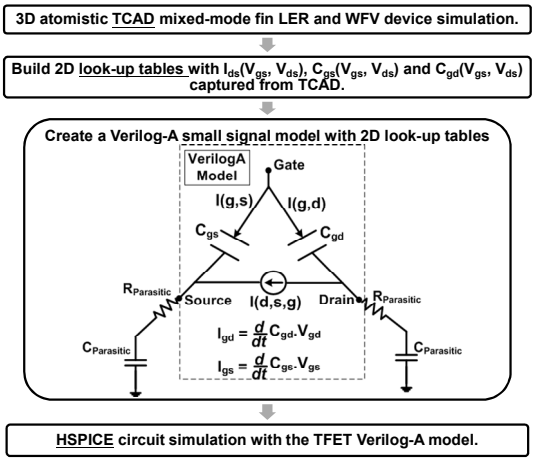

Fig. 5. Flowchart for HSPICE look-up table based Verilog-A model generation from atomistic 3D TCAD simulations [2, 4].

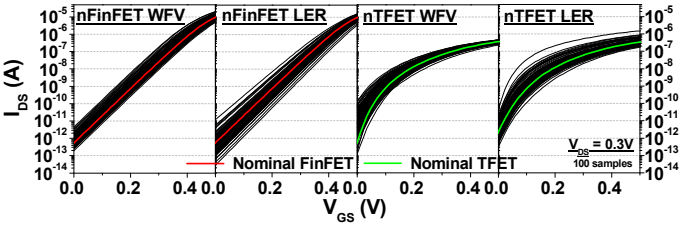

Fig. 6. Simulated I_{DS}-V_{GS} characteristics at V_{DS}=0.3V for TFET and FinFET with WFV and fin LER.

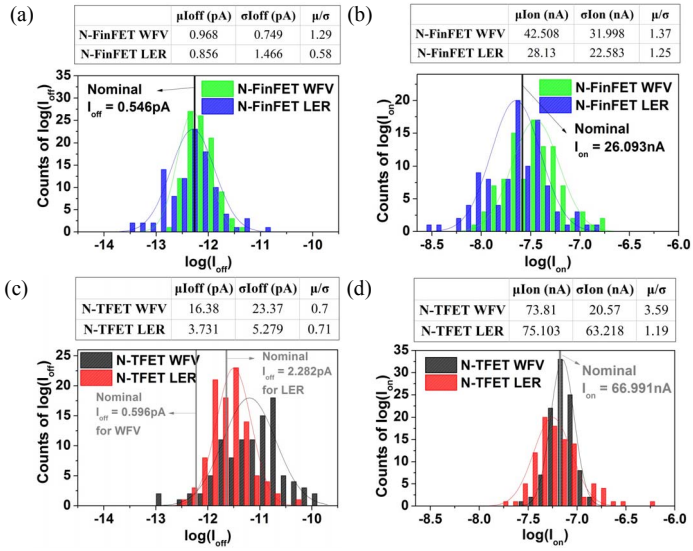

Fig. 7. Probability distribution of (a) log(I_{off}), (b) log(I_{on}) for FinFET and (c) log(I_{off}), (d) log(I_{on}) for TFET at V_{DS}=0.3V considering WFV and fin LER.

causes a V_t shift of I_{DS}-V_{GS} curves in subthreshold region with almost equal subthreshold swing (S.S.), therefore the I_{on} and I_{off} probability distributions are similar. On the other hand, fin LER influences the effective fin width and electrostatic integrity, thus impacting both V_t and S.S., so the I_{on} and I_{off} probability distributions are quite different. As can be seen, both the μ/σ of I_{on} and I_{off} are worse with fin LER than WFV, especially for I_{off}.

For TFETs, the I_{OFF} distribution with WFV is boarder (worse) than that with fin LER since WFV leads to fluctuation in the energy bands and alters the critical tunneling path, and the effect decreases with increasing V_{GS}. The metal grains with

various WF form the up and down energy bands that boost the band-to-band generation, resulting in large I_{off} distribution. Therefore, the variability of I_{OFF} is larger than I_{ON}, and the correlation between I_{ON} and I_{OFF} is weak. On the other hand, for fin LER, both I_{on} and I_{off} are degraded as fin width (W_{Fin}) increases due to the weaker electrostatic control of the channel from both gates, and the degradations of I_{on} and I_{off} track W_{Fin} with exponential-like behavior, especially for I_{off} which dramatically increases with decreasing W_{Fin}. Comparing with fin LER, the $\mu/\sigma(I_{on})$ of WFV is better, and the $\mu/\sigma(I_{off})$ of WFV is comparable to LER. In addition, WFV causes larger $\sigma(I_{off})$ than LER.

Overall, comparing FinFET and TFET, the impacts by WFV on I_{on} and I_{off} are quite different. The $\mu/\sigma(I_{off})$ of TFET is worse while $\mu/\sigma(I_{on})$ of TFET is better. In addition, the I_{off} distribution of TFET skews to high values, and not as symmetrical as the I_{off} distribution for FinFET, resulting in larger $\mu(I_{off})$. On the other hand, the variation of TFET considering fin LER is slight better than FinFET.

B. C_g Variability

Fig. 8 shows the impacts of WFV and fin LER on C_g-V_{GS} dispersions of TFET and FinFET devices at V_{DS} = 0.3V. Fig. 9 illustrates the probability distributions of $C_{g,ave}$ (the average capacitance across the gate-bias range from 0 to V_{DD}=0.3V) at V_{DS}=V_{DD}. For both TFET and FinFET, the C_g variation by WFV becomes more significant at larger V_{GS}. In contrast, the variation due to fin LER is more severe when V_{GS} is small. Note that $C_{g,ave}$ is extracted only for the range from V_{GS} =0V to 0.3V. The μ/σ (WFV) are much better compared with μ/σ(LER). For TFET with WFV and FinFET with fin LER, the $C_{g,ave}$ skews to high values, resulting in larger μ than the nominal cases.

V. Impacts of WFV and Fin LER on CLA Circuits

A. Delay Variability

The switching delay is commonly calculated as $\tau = (C_g V_{DD}/I_{on})$. Due to the strong bias dependence of gate capacitance (C_g), the average capacitance ($C_{g,ave}$) across the gate-bias range from 0 to V_{DD} (0.3V in this case) at V_{DS}=V_{DD} is determined for approximation : $\tau \approx (C_{g,ave} V_{DD}/I_{on})$.

The transient waveforms and the probability distributions of delays for 32-bit CLA of TFET and FinFET with WFV and fin LER are shown in Fig. 10 and Fig. 11. As can be seen, the μ/σ(Delay) of TFET is better than FinFET in both cases (with WFV and fin LER). For both TFET and FinFET, the μ/σ(WFV) is better than μ/σ(LER). The variability of delay correlates with aforementioned I_{on} and $C_{g,ave}$ variations in Section IV. The smaller I_{on} of FinFET significantly degrades its μ/σ(Delay).

Fig. 12 presents the delay for 32-bit CLA of TFET and Fin FET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV and fin LER (at 0.2V and 0.3V). The delay variability of all cases becomes worse with decreasing V_{DD} due to decreasing I_{DS}. The delay and its variability of TFET are significantly better than FinFET at low V_{DD} due to its larger I_{DS} and smaller $C_{g,ave}$ variation compared with FinFET.

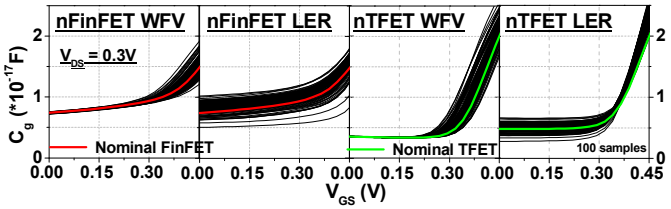

Fig. 8. Simulated C_g-V_{GS} characteristics at V_{DS}=0.3V for TFET and FinFET with WFV and fin LER.

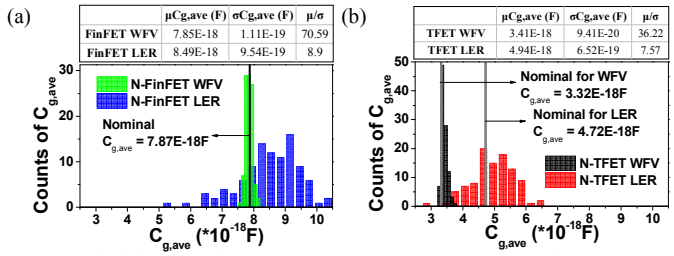

Fig. 9. Probability distribution of $C_{g,ave}$ for (a) FinFET and (b) TFET at V_{DS}=0.3V considering WFV and fin LER.

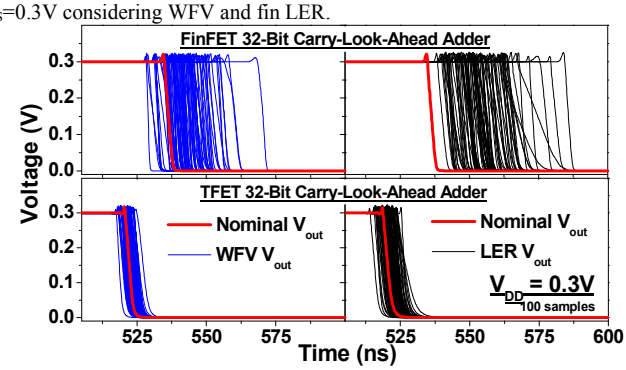

Fig. 10. Transient waveforms of 32-bit CLA for TFET and FinFET at V_{DD}=0.3V considering WFV and fin LER.

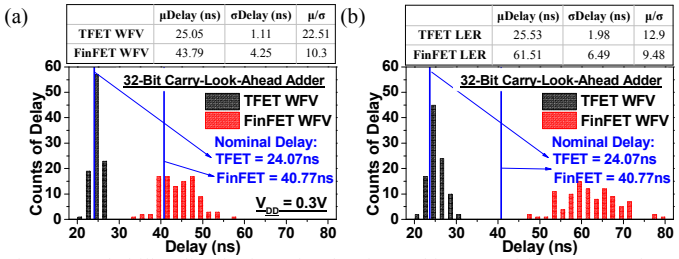

Fig. 11. Probability distribution of Delay for 32-bit CLA with (a) WFV, (b) fin LER for TFET and FinFET at V_{DD}=0.3V.

B. PDP Variability

PDP is a figure of merit to evaluate the energy efficiency of logic gates. It represents the energy dissipated during a switching event, and can be calculated as: $PDP = C_g V_{DD}^2 \approx C_{g,ave} V_{DD}^2$.

The probability distributions of PDP 32-bit CLA of TFET and FinFET for the nominal cases and the cases with WFV and fin LER are shown in Fig. 13. The μ/σ(WFV) is better than μ/σ(LER) for both TFET and FinFET, and the distributions of TFET with WFV and that of FinFET with fin LER skew to larger values.

Fig. 14 shows the PDP for 32-bit CLA of TFET and FinFET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV and fin LER (at 0.2V and 0.3V). As can be seen, TFET PDP is much better than FinFET

at low V_{DD} due to the fact that $C_{g,ave}$ variation of FinFET is larger and skewed to high values compared with TFET. Notice that the PDP of TFET is still better than FinFET considering random variations.

C. Leakage Power Variability

The probability distributions of leakage power for 32-bit CLA of TFET and FinFET for the nominal cases and the cases with WFV and fin LER at V_{DD}=0.3V are shown in Fig. 15. The leakage power variation of TFET with both variation sources are much worse than FinFET, and the distributions skew to larger values, especially under WFV. This correlates to aforementioned I_{off} variations in Section IV.

Fig. 16 shows the leakage power for 32-bit CLA of TFET and FinFET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV and fin LER (at 0.2V and 0.3V). As the operating voltage is reduced, the leakage power decreases. Notice that the increase of leakage power by random variations is more significant than the influence by operating voltage for TFET.

VI. Conclusion

We investigate and compare the impacts of WFV and fin LER on TFET and FinFET I_{on}, I_{off} and $C_{g,ave}$ using atomistic 3D TCAD simulations with calibrated model and device parameters. Our studies indicate that considering WFV, FinFET has comparable I_{on} and I_{off} variability while TFET has smaller I_{on} variability and larger I_{off} variability. In addition, the band diagram dispersion caused by WFV increases the band-to-band generation for TFET in "OFF" state, leading to skewed I_{off} distribution to larger values. On the other hand, the impact of fin LER is similar for TFET and FinFET, resulting in comparable I_{on} and I_{off} variability. The $C_{g,ave}$ variability is worse with fin LER compared with WFV for both TFET and FinFET.

Using Verilog-A device models extracted from atomistic 3D TCAD simulations to capture the physical non-uniformities and variability, HSPICE circuit simulations are performed to assess the impacts of WFV and fin LER on TFET and FinFET 32-bit CLA. The results show that at low operating voltage (< 0.3V), the delay and PDP of TFET CLA are significantly better than the FinFET counterparts, even under the impacts of WFV and LER. However, the variability of leakage power for TFET CLA is worse than FinFET CLA, especially with WFV. The leakage power distribution of TFET CLA skews to larger values due to its worse I_{off} variability.

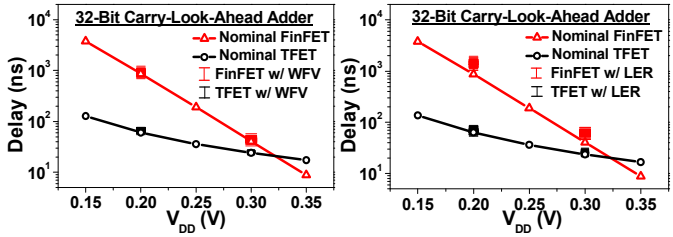

Fig. 12. Delay for 32-bit CLA of TFET and FinFET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV(left) and fin LER (right) (0.2V and 0.3V).

(a)

	μPDP (J)	σPDP (J)	μ/σ
TFET WFV	3.01E-17	2.05E-18	14.68
FinFET WFV	3.12E-17	3.03E-18	10.31

(b)

	μPDP (J)	σPDP (J)	μ/σ
TFET LER	3.14E-17	2.68E-18	11.7
FinFET LER	4.68E-17	5.22E-18	8.97

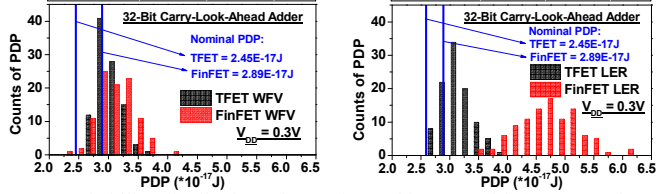

Fig. 13. Probability distribution of PDP for 32-bit CLA with (a) WFV, (b) fin LER for TFET and FinFET at V_{DD}=0.3V.

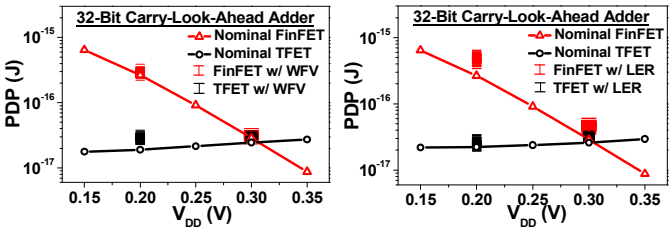

Fig. 14. PDP for 32-bit CLA of TFET and FinFET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV(left) and fin LER (right) (0.2V and 0.3V).

(a)

	μ(Leakage Power) (pW)	σ(Leakage Power) (pW)	μ/σ
TFET LER	219.12	15.48	14.16
FinFET LER	46.25	1.57	29.48

(b)

	μ(Leakage Power) (pW)	σ(Leakage Power) (pW)	μ/σ
TFET LER	558.94	97.33	5.74
FinFET LER	56.05	5.17	10.83

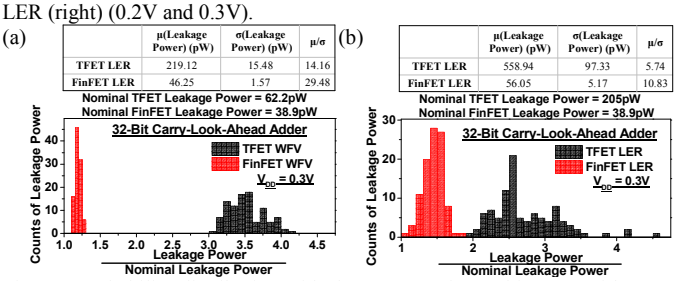

Fig. 15. Probability distribution of leakage power for 32-bit CLA with (a) WFV, (b) fin LER for TFET and FinFET at V_{DD}=0.3V.

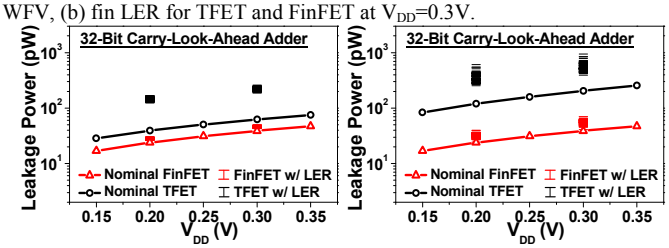

Fig. 16. Leakage power for 32-bit CLA of TFET and FinFET versus V_{DD} from 0.15V to 0.35V for the nominal cases and the cases considering WFV(left) and fin LER (right) (0.2V and 0.3V).

Acknowledgment

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