Digital Integrated Circuits

Designing Combinational Logic Circuits

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Dynamic Logic

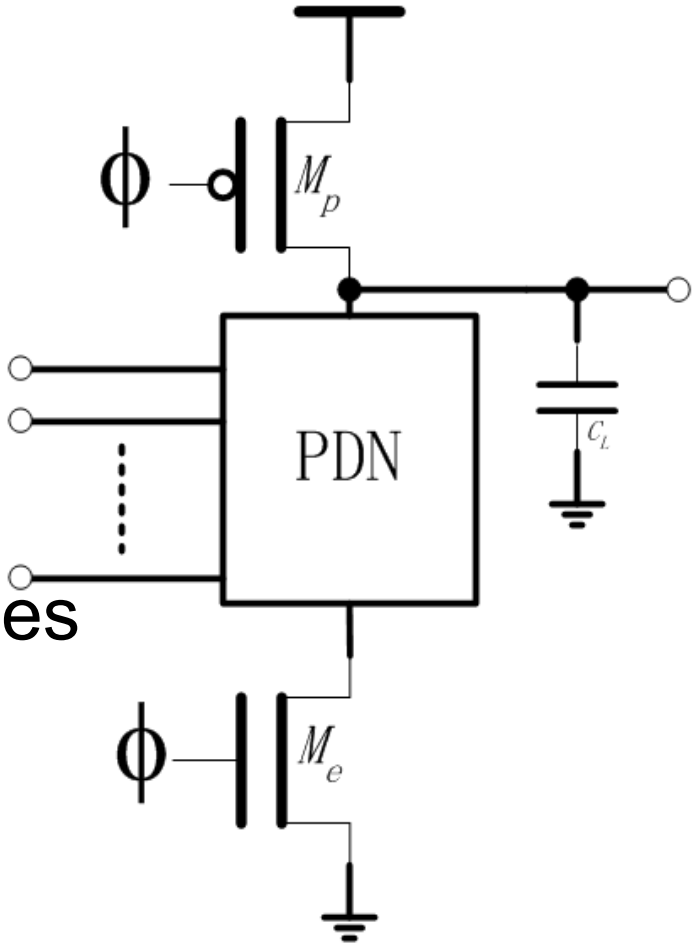
Dynamic logic outline

- ***Dynamic logic principle***
- **Dynamic logic properties**
- **Dynamic logic design issues**
- **Dynamic logic cascade solution**

Static or ***Dynamic***

A first glance of dynamic logic

- Basic components
  - PDN,just like CMOS and pseudo-NMOS
  - Clock control transistors，seperate circuit to two phases
- Dynamic logic’s two phases
  - precharge
  - evaluation

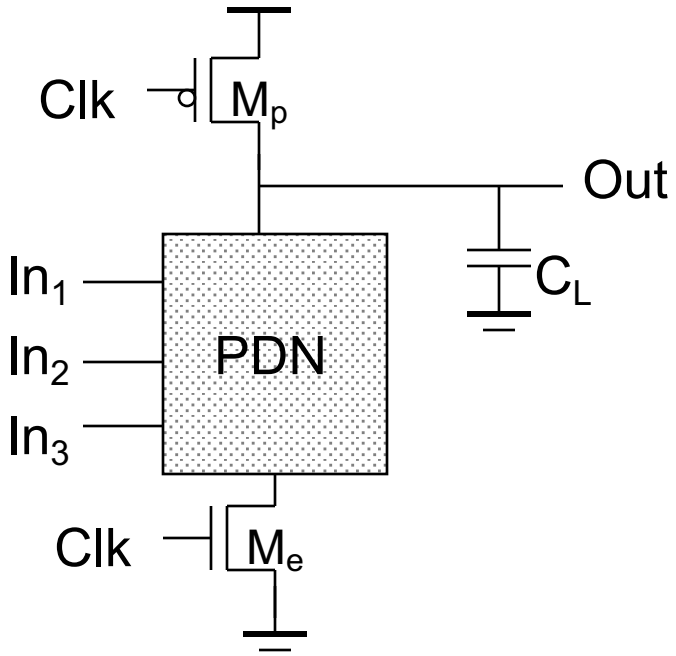


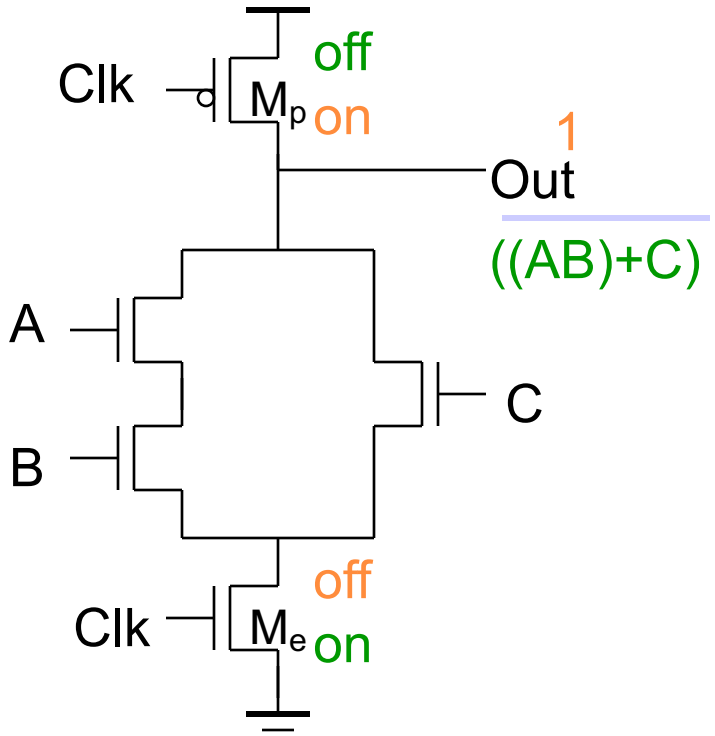
Dynamic CMOS

- ***Static*** circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices

- ***Dynamic*** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

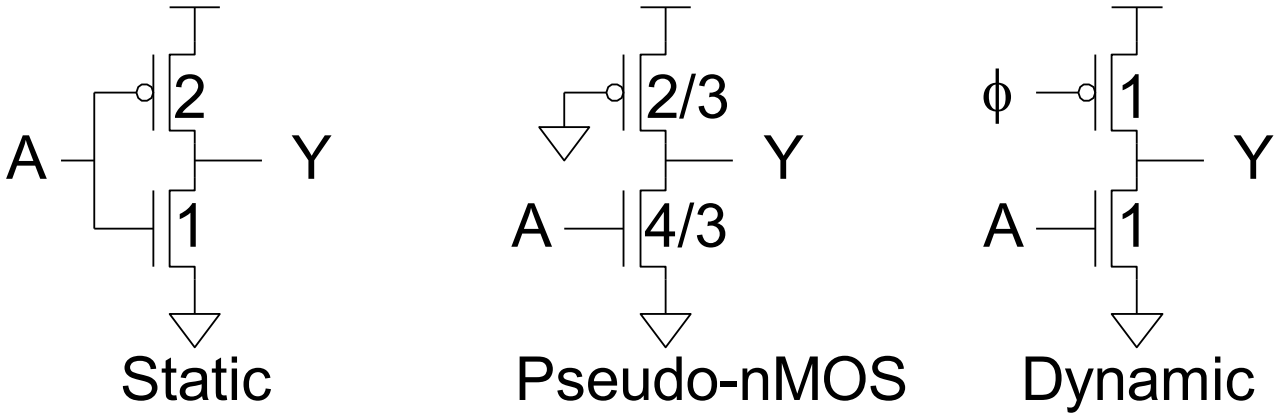
Evaluate(Clk = 1)

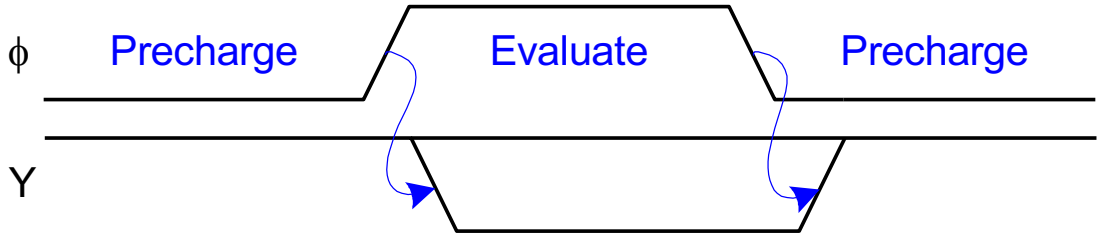
Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation
- Inputs to the gate can make ***at most*** one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

Dynamic Logic

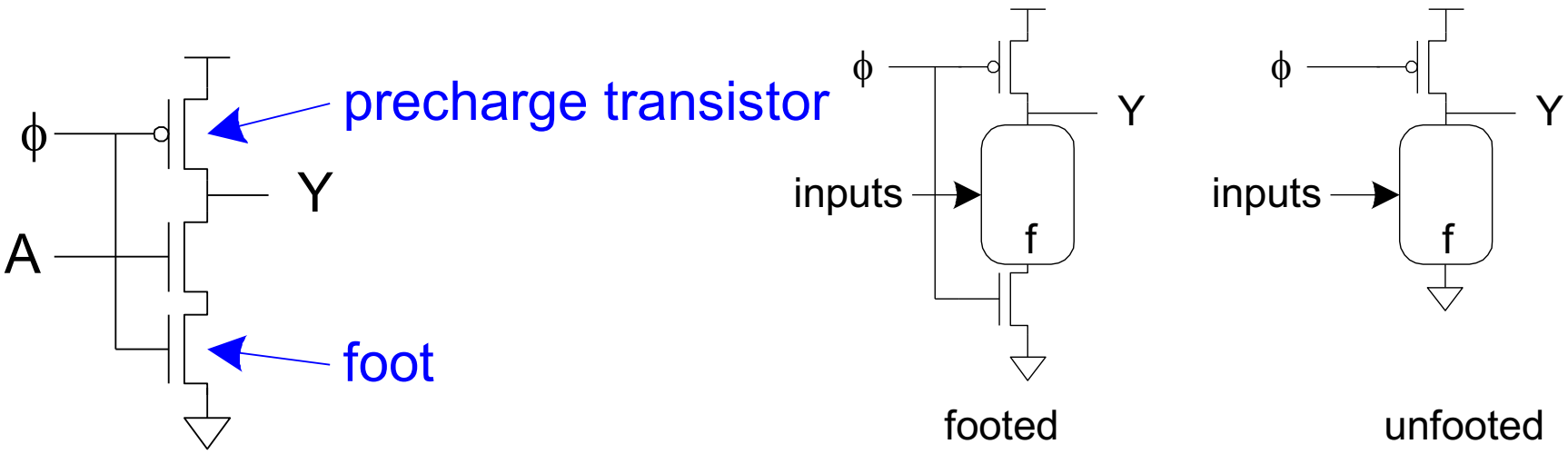
- *Dynamic* gates uses a clocked pMOS pullup
- Two modes: *precharge* and *evaluate*



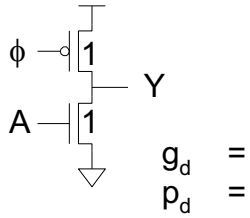
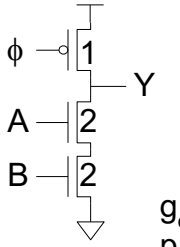
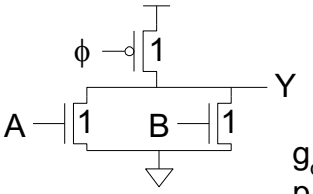
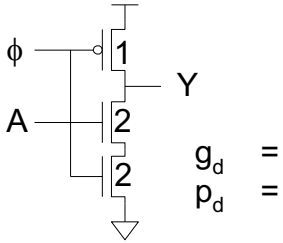
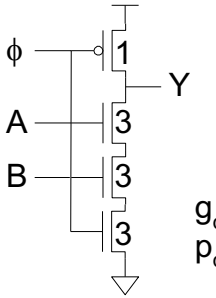
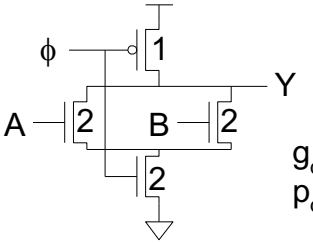


The Foot

- What if pulldown network is ON during precharge?
- Use series evaluation transistor to prevent fight.



Logical Effort

	Inverter	NAND2	NOR2
unfooted	 g_d = p_d =	 g_d = p_d =	 g_d = p_d =
footed	 g_d = p_d =	 g_d = p_d =	 g_d = p_d =

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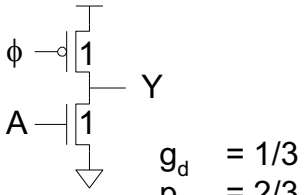
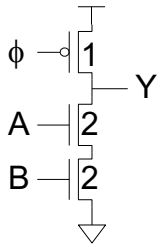
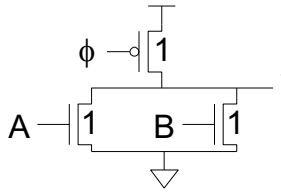
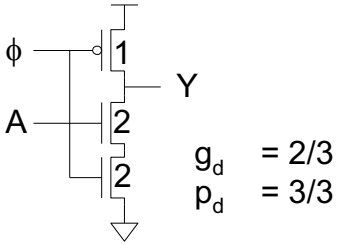
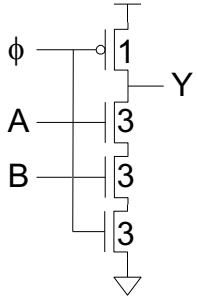
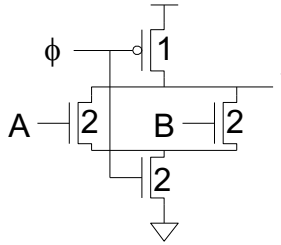
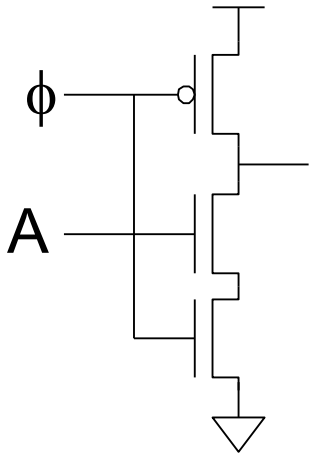
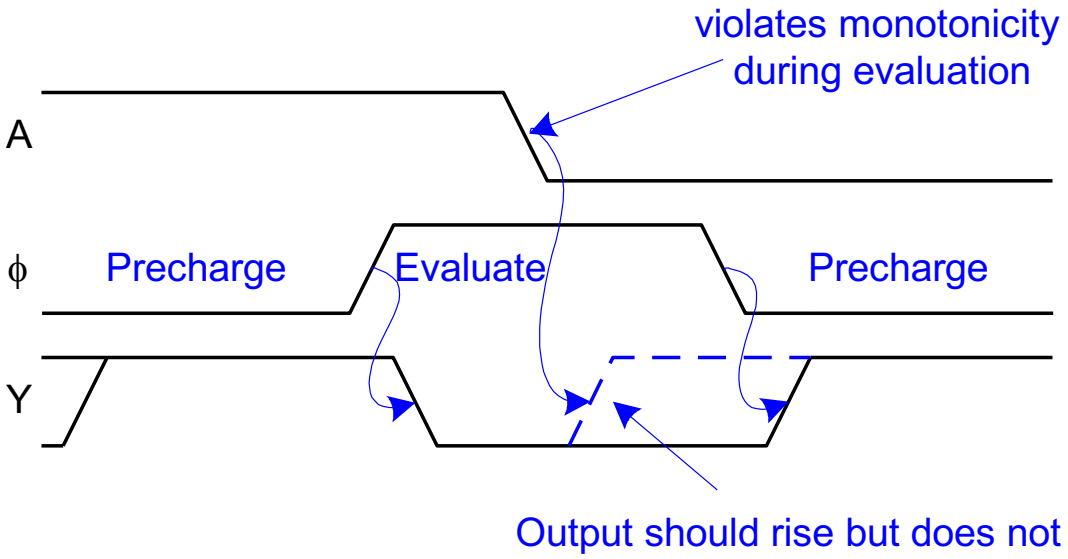
unfooted	 $g_d = 1/3$ $p_d = 2/3$	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 1/3$ $p_d = 3/3$
footed	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 3/3$ $p_d = 4/3$	 $g_d = 2/3$ $p_d = 5/3$

Monotonicity

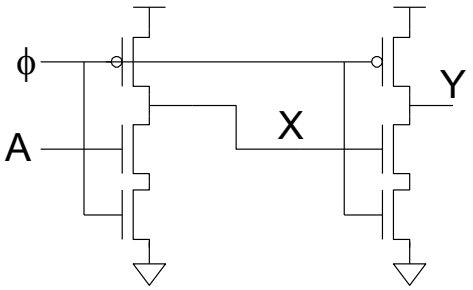
- Dynamic gates require ***monotonically rising*** inputs during evaluation
  - 0 -> 0
  - 0 -> 1
  - 1 -> 1
  - ***But not 1 -> 0***

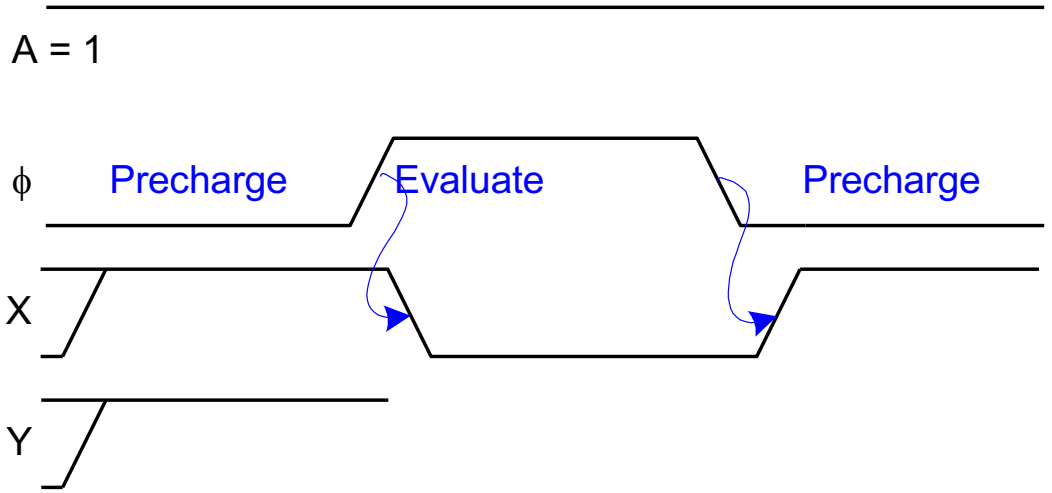




Monotonicity Woes

- But dynamic gates produce monotonically falling outputs during evaluation
- Illegal for one dynamic gate to drive another!





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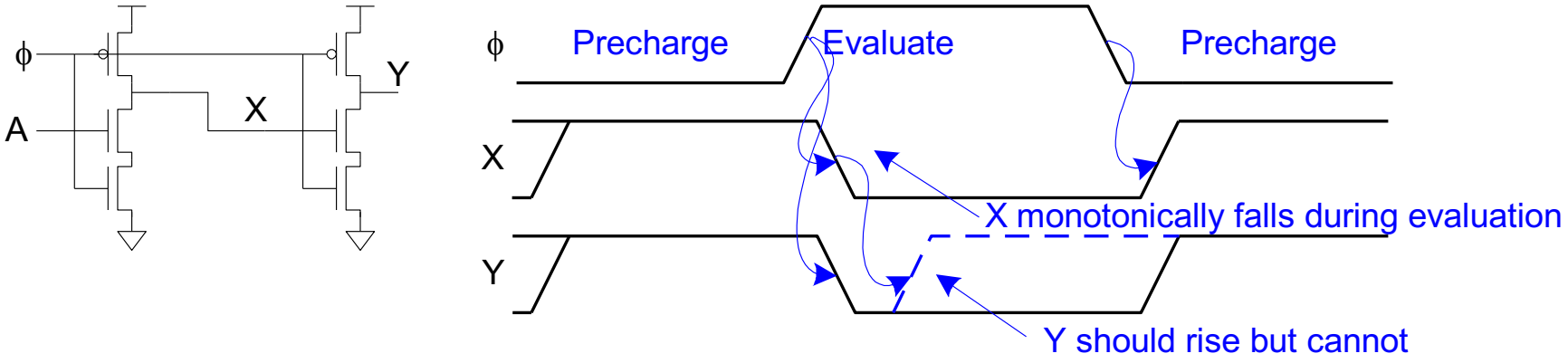


Dynamic logic outline

- Dynamic logic principle
- ***Dynamic logic properties***
- Dynamic logic design issues
- Dynamic logic cascade solution

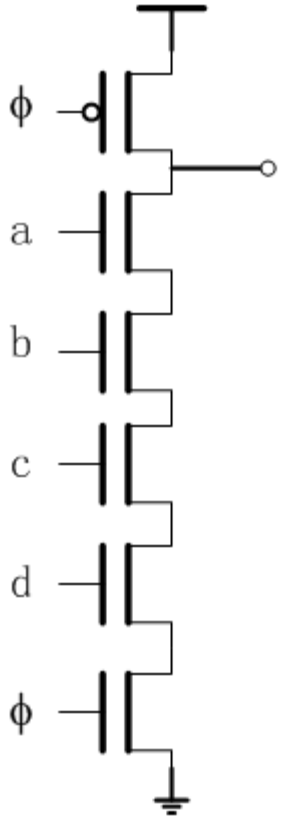
Properties of Dynamic Gates

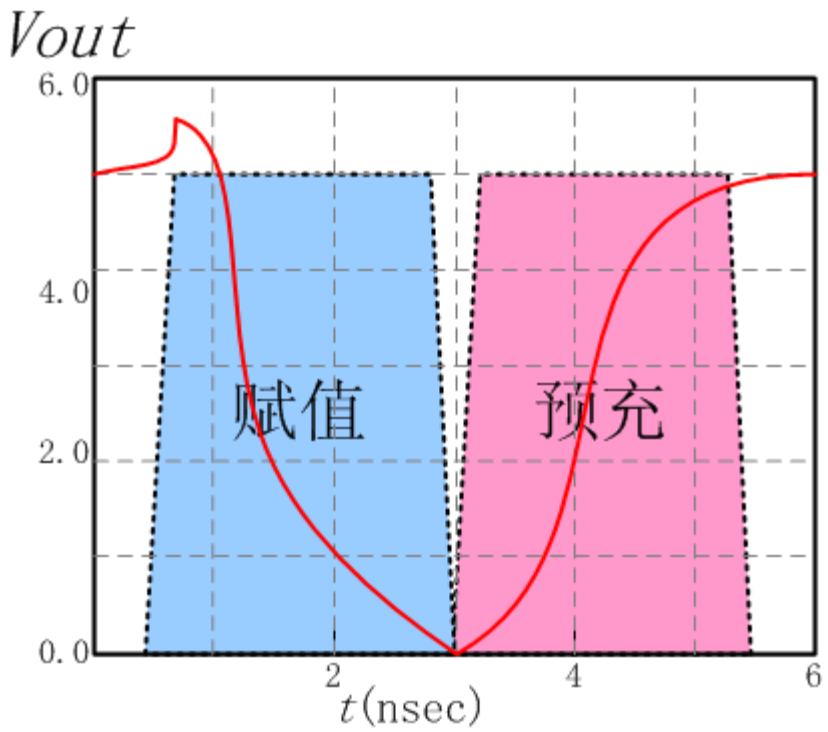
- ✓ Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- ✓ Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- ✓ Non-ratioed
  - sizing of the devices does not affect the logic levels
- ✓ Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (C_{out})

Properties of Dynamic Gates

Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - No glitching
  - *higher transition probabilities*
  - *extra load on Clk*
PDN starts to work when the input signals exceed V_{Tn}
  - V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
Needs a precharge/evaluate clock

A 4-NAND dynamic logic VTC

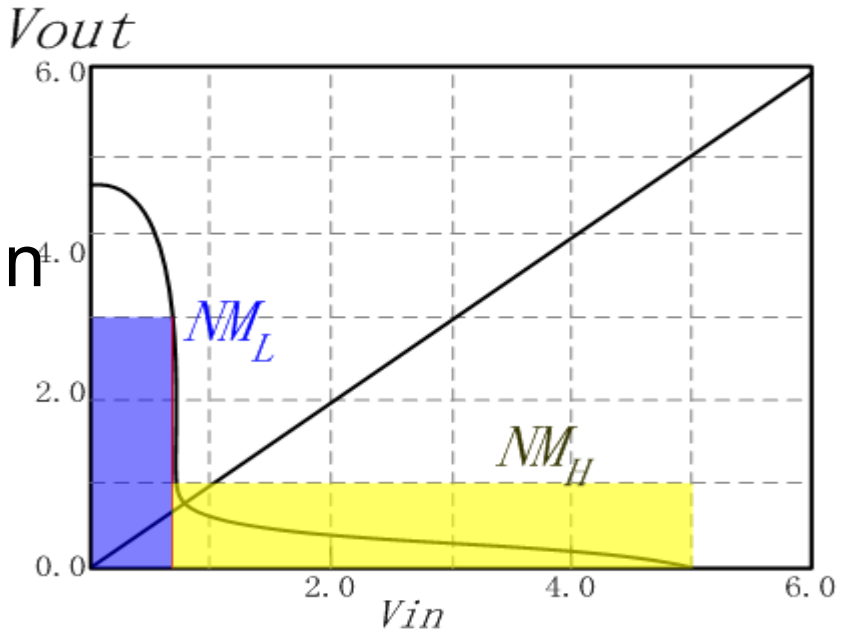




A 4-NAND dynamic logic V_{TC}

面积	静态电流	晶体管数目	V_{OH}	V_{OL}	V_M	NM_H	NM_L	t_{pHL}	t_{pLH}	t_p
212	0	6	5V	0V	0.75V	4.25V	0.75V	0.74nsec	0	0.37nsec

- Small load capacity
- Asymmetry of noise margin
- Small delay
- Fewer transistors



Dynamic logic outline

- Dynamic logic principle
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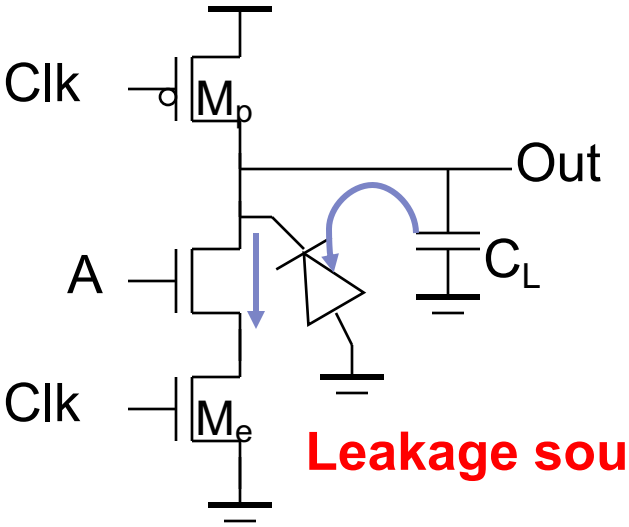
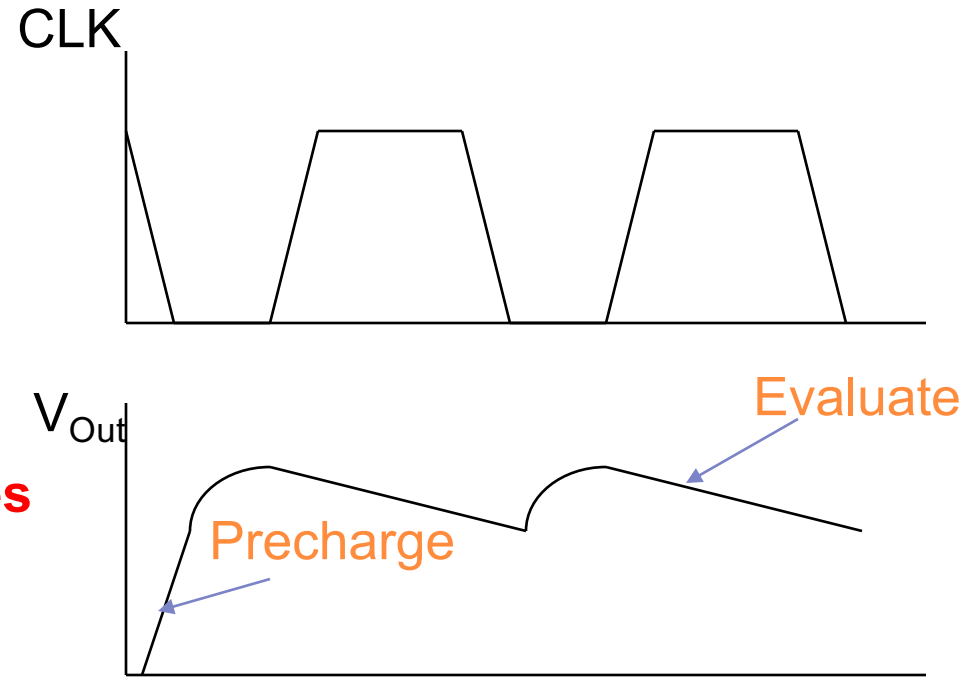
- ***Dynamic logic design issues***
  - ***Charge-leakage***
  - Charge-sharing
  - Backgate Coupling
  - Clock feedthrough
- Dynamic logic cascade solution

Issues in Dynamic Design 1: Charge Leakage

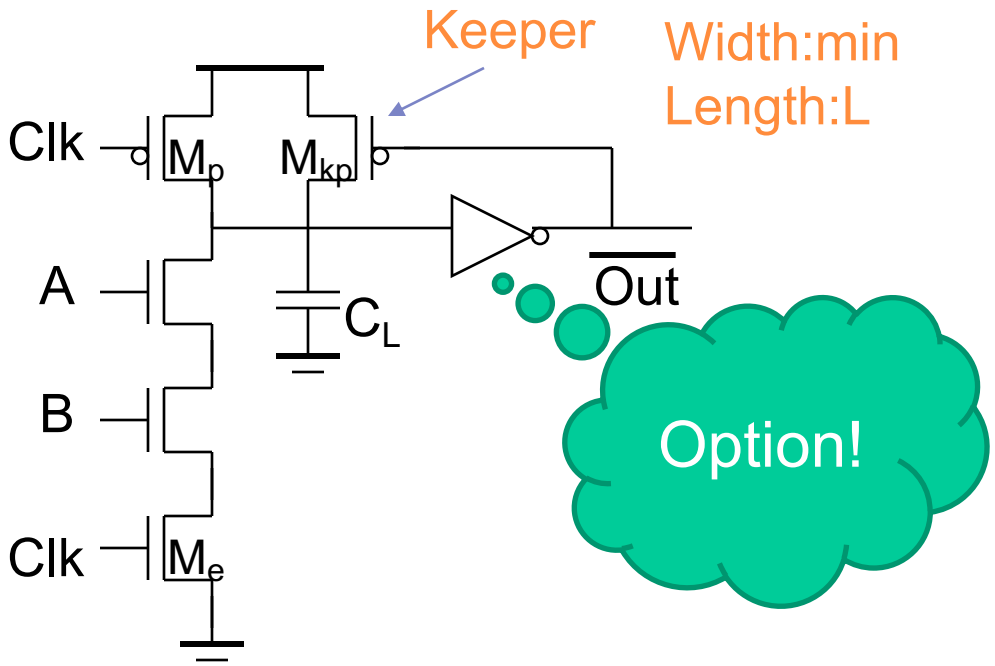


Leakage sources



Dominant component is subthreshold current

Solution to Charge Leakage



Same approach as level restorer for pass-transistor logic

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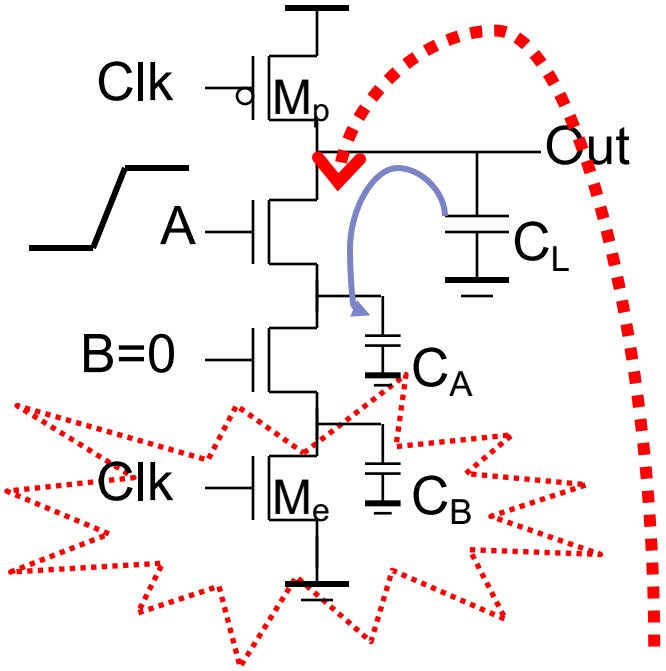
Issues in Dynamic Design 2: Charge Sharing

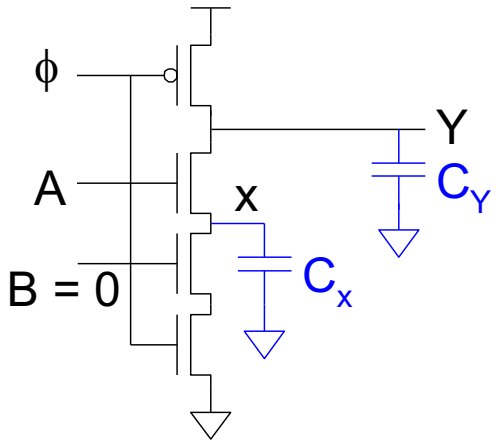


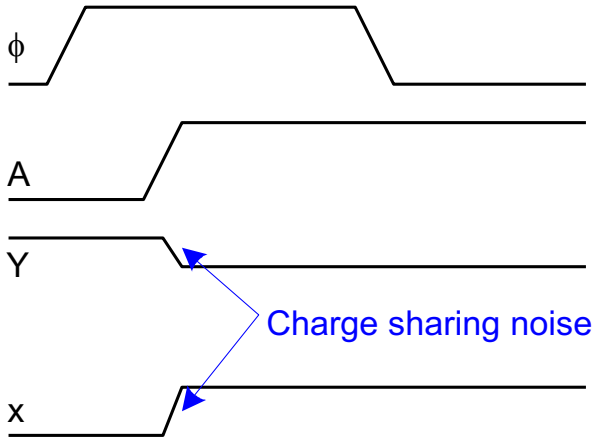
Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

Could we move it to there?

Charge Sharing

- Dynamic gates suffer from charge sharing





$$V_x = V_Y =$$

Charge Sharing

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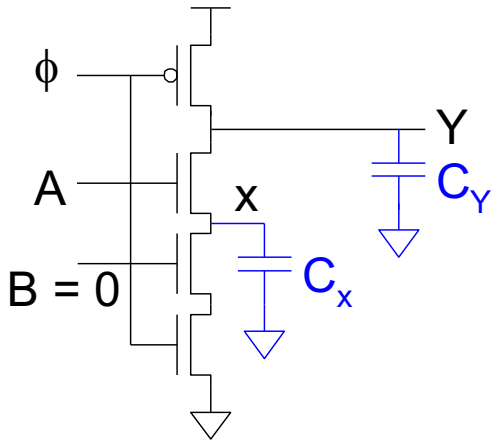
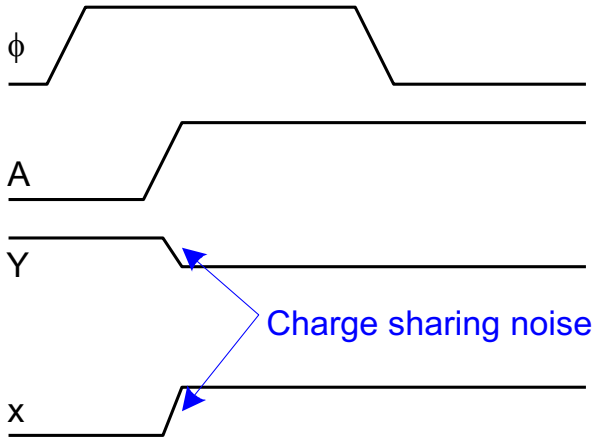
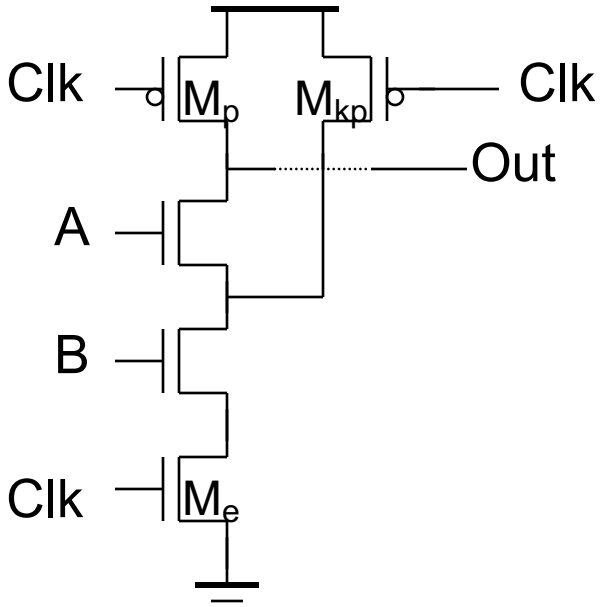




$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

Solution to Charge Redistribution

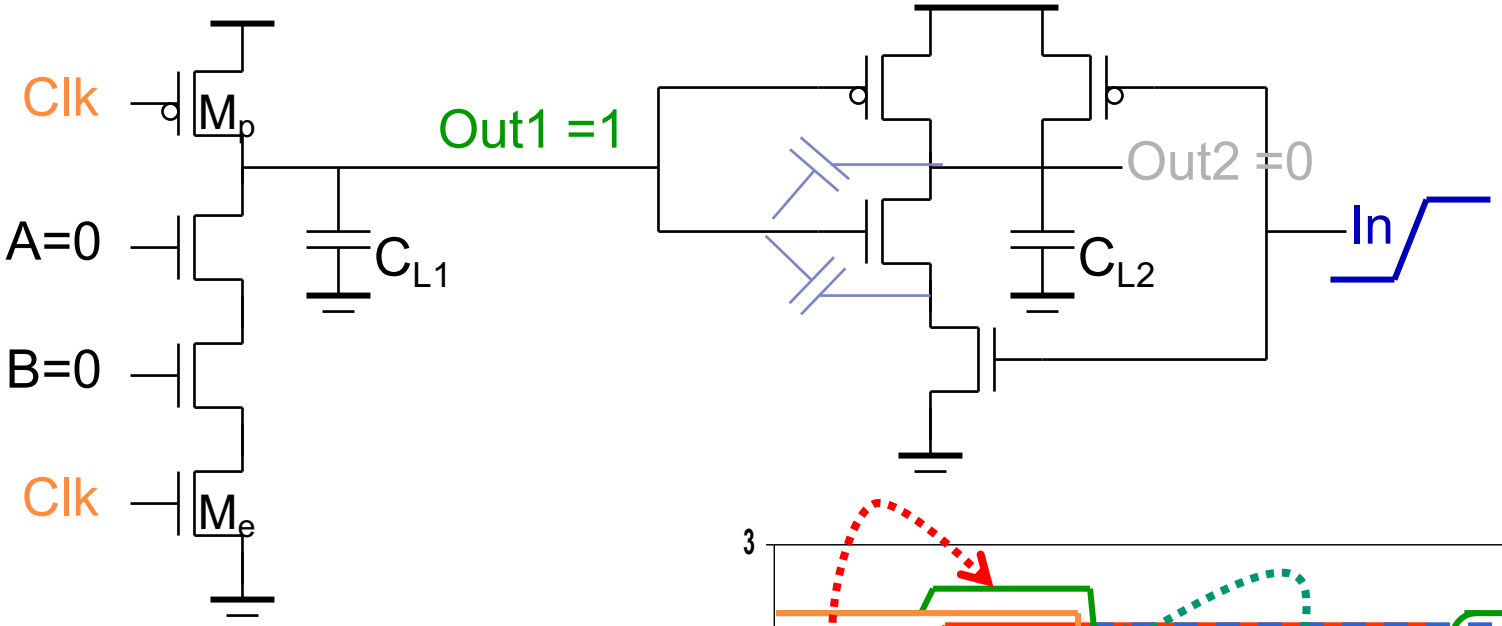


Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

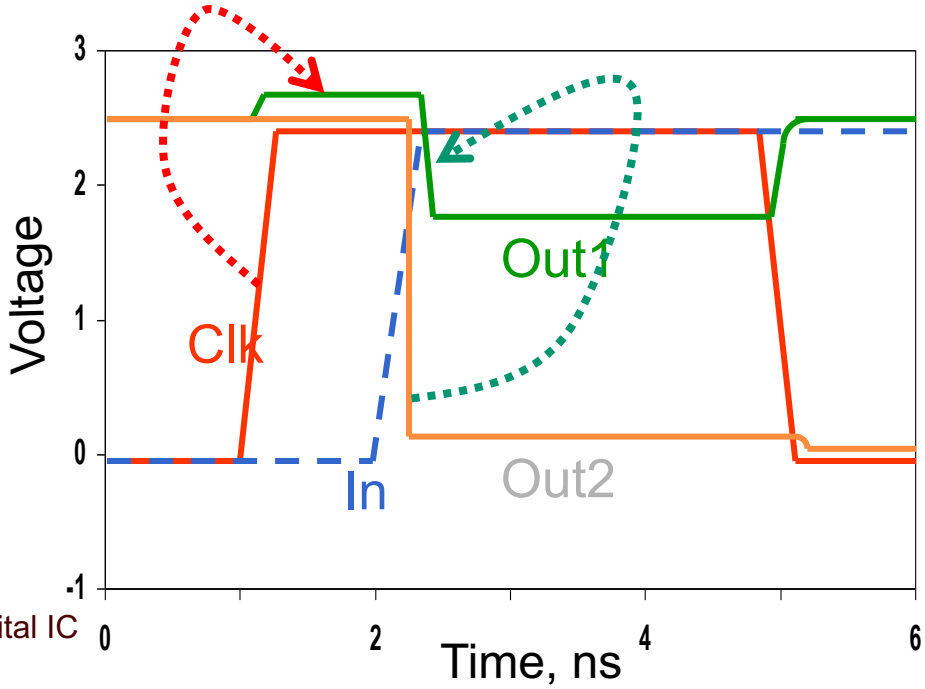
Dynamic logic outline

- Dynamic logic principle
- Dynamic logic properties
- ***Dynamic logic design issues***
  - Charge-leakage
  - Charge-sharing
  - ***Backgate Coupling***
  - Clock feedthrough
- Dynamic logic cascade solution

Issues in Dynamic Design 3: Backgate Coupling



Dynamic NAND



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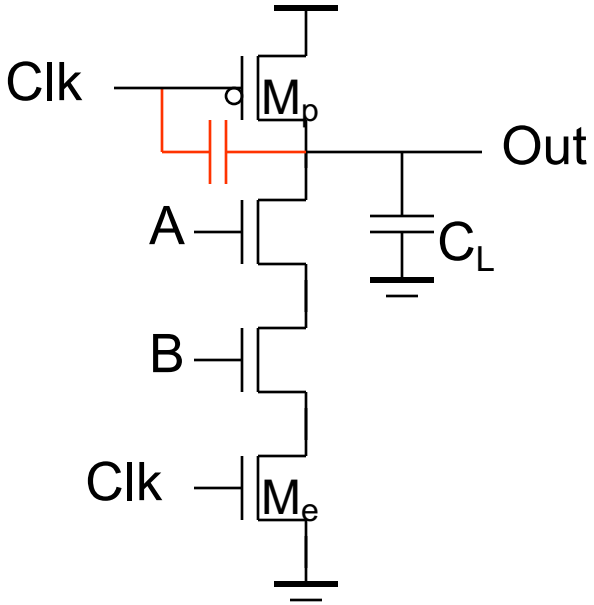
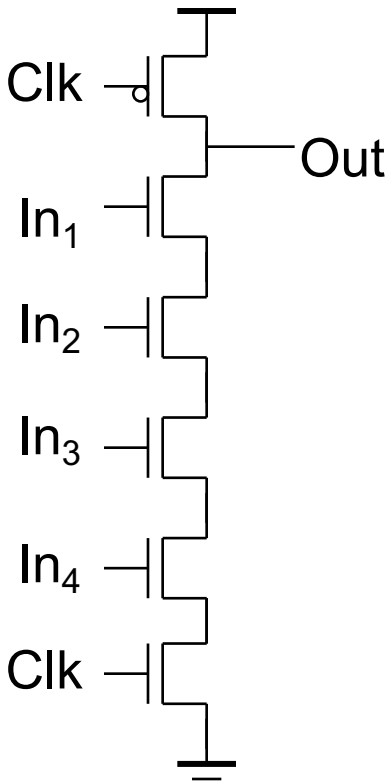
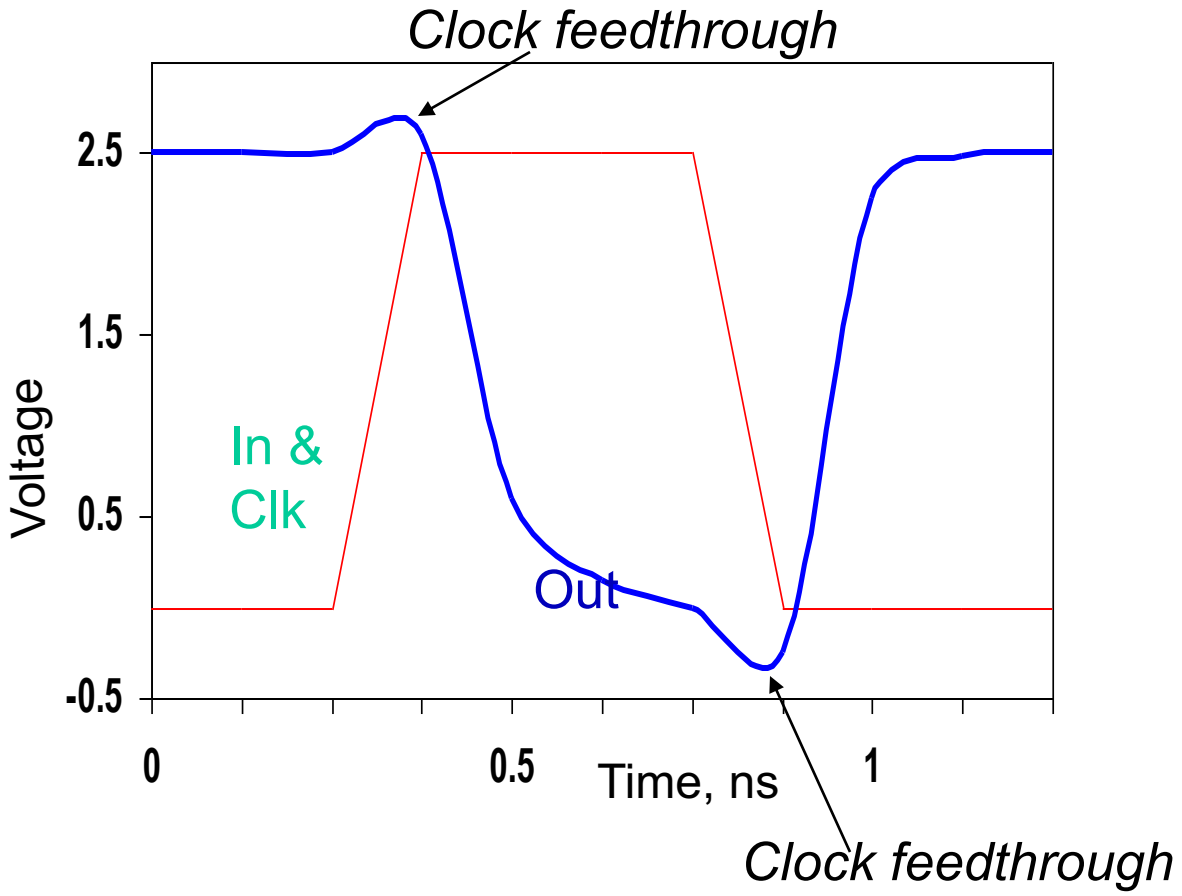
Issues in Dynamic Design 4: Clock Feedthrough



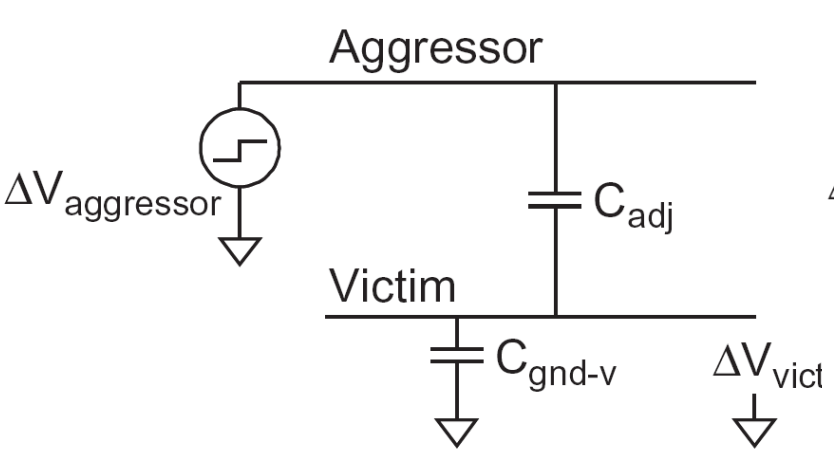
Coupling between **Out** and **Clk** input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

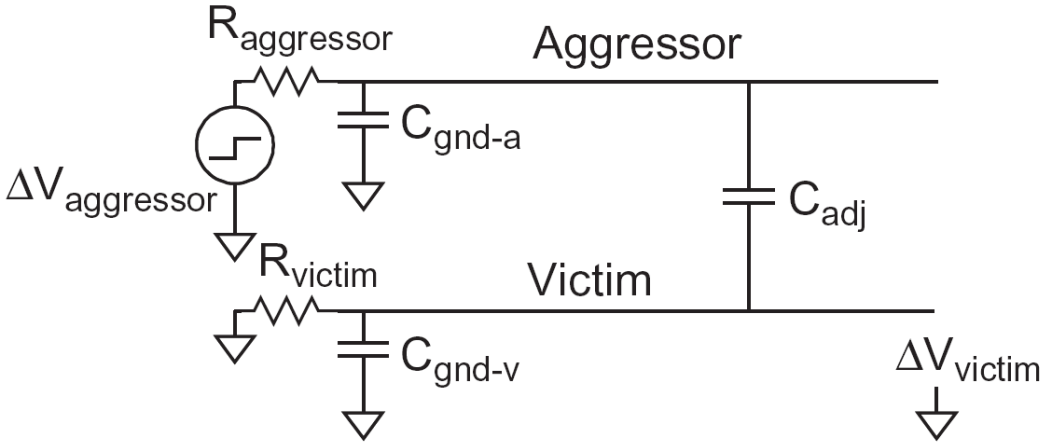
Clock Feedthrough





Crosstalk Noise Effects



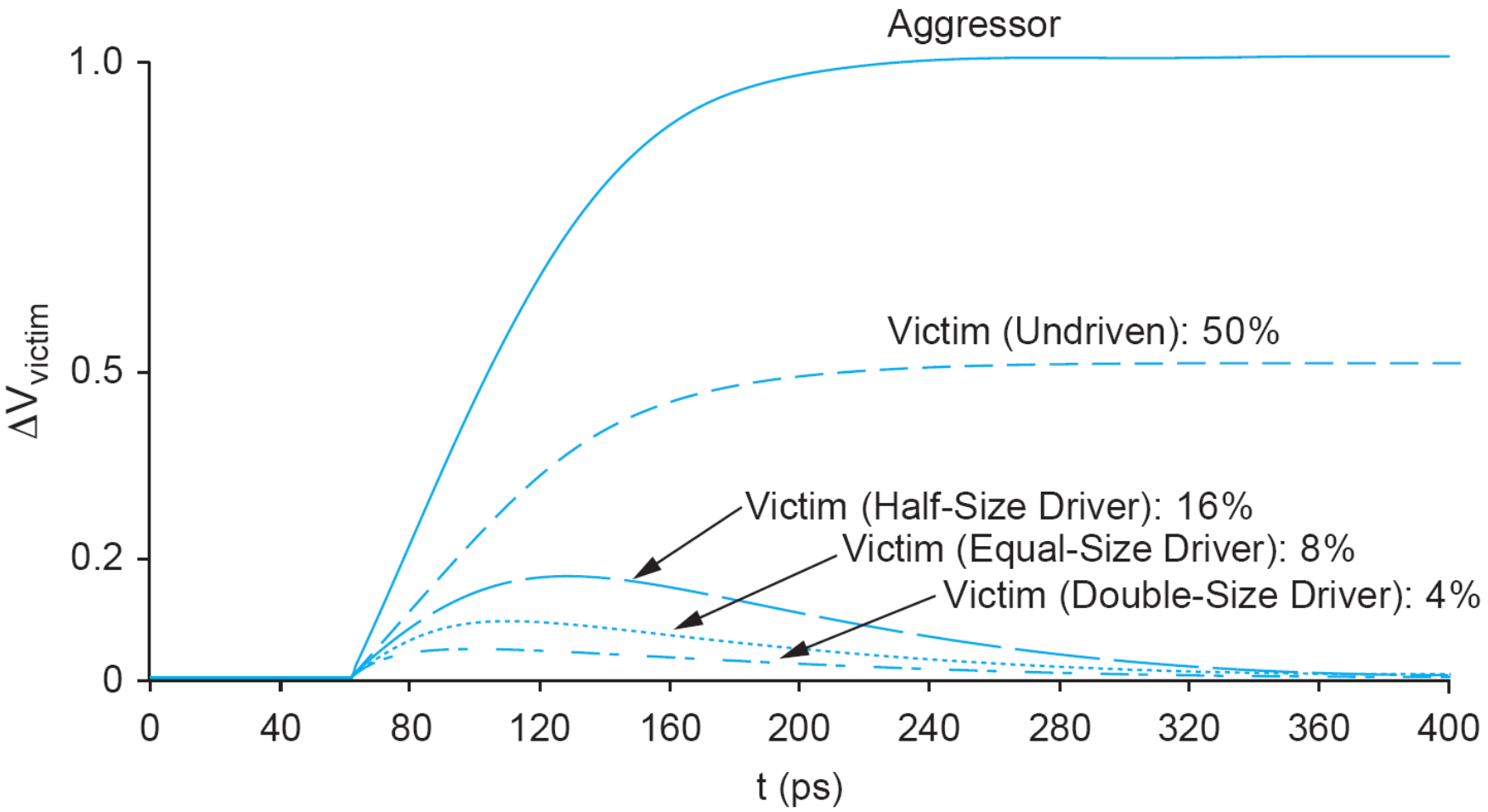


$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \Delta V_{aggressor}$$

$$k = \frac{\tau_{aggressor}}{\tau_{victim}} = \frac{R_{aggressor}(C_{gnd-a} + C_{adj})}{R_{victim}(C_{gnd-v} + C_{adj}))}$$

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \frac{1}{1+k} \Delta V_{aggressor}$$

Waveforms of coupling noise



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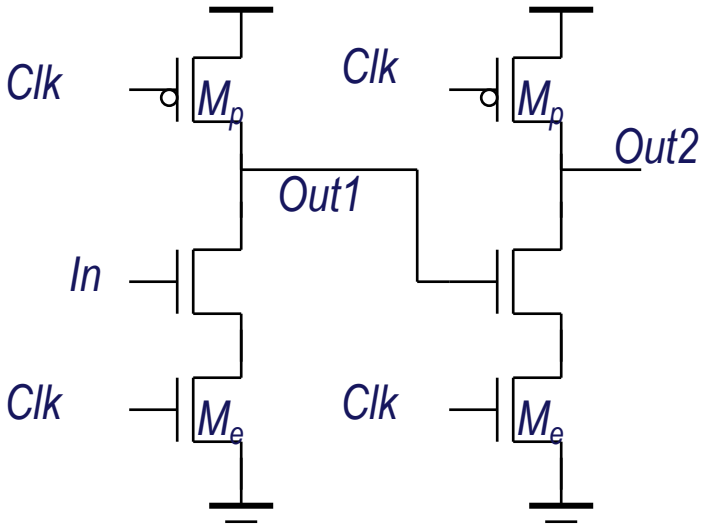
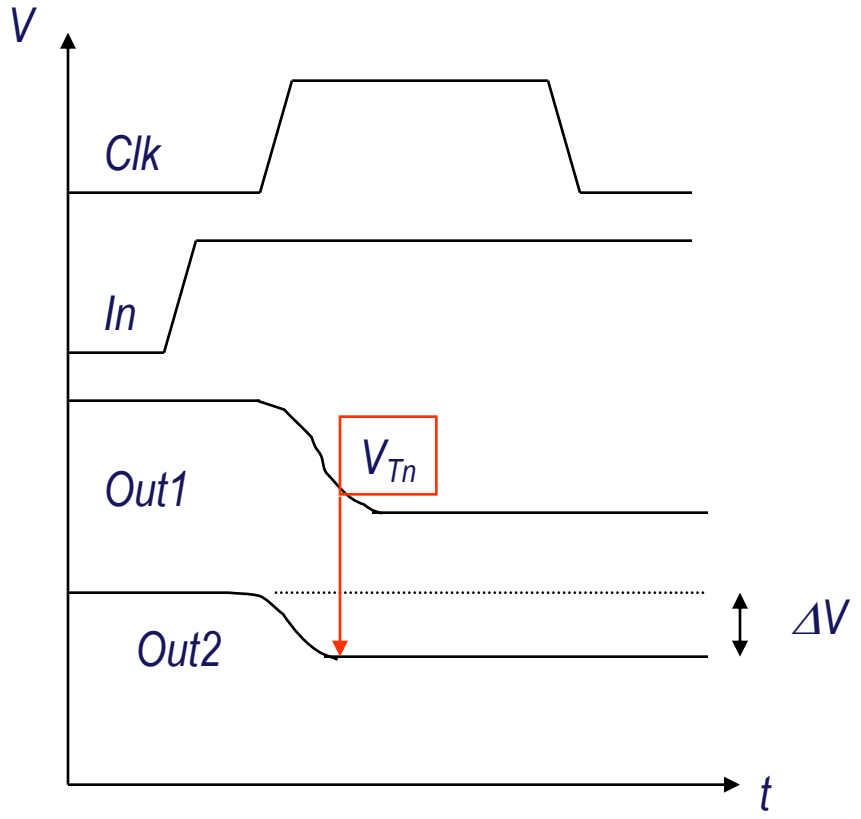
Cascading Dynamic Gates

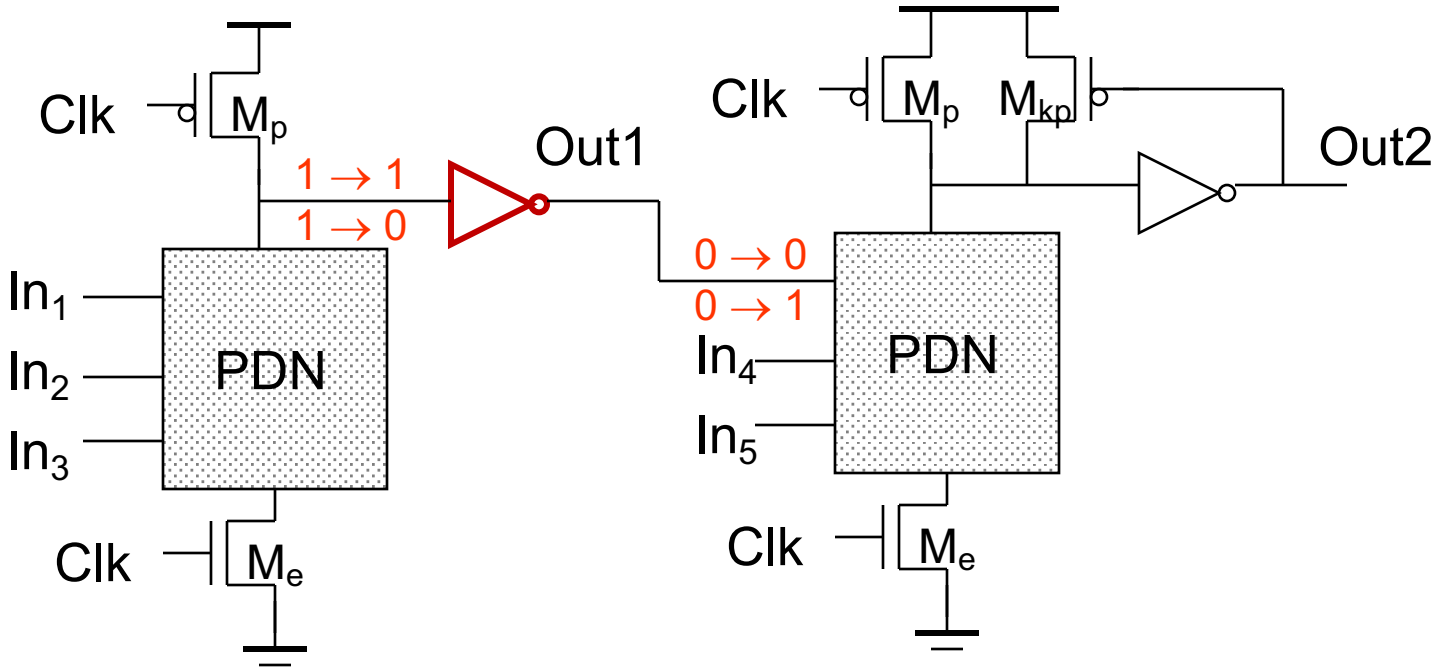




Only 0 → 1 transitions allowed at inputs!

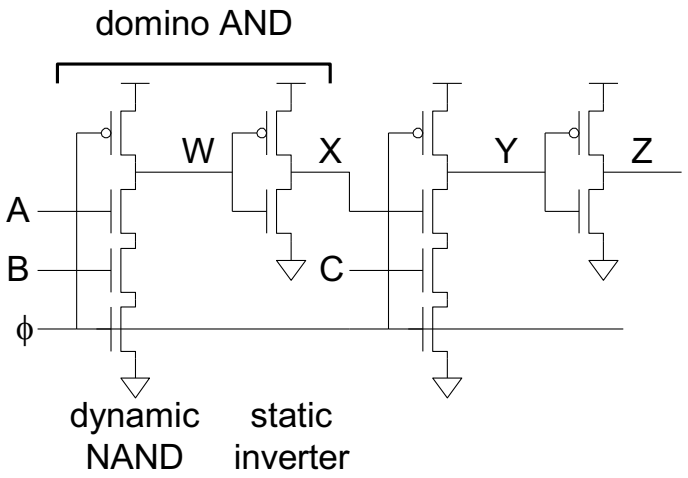
Not 1 → 0!

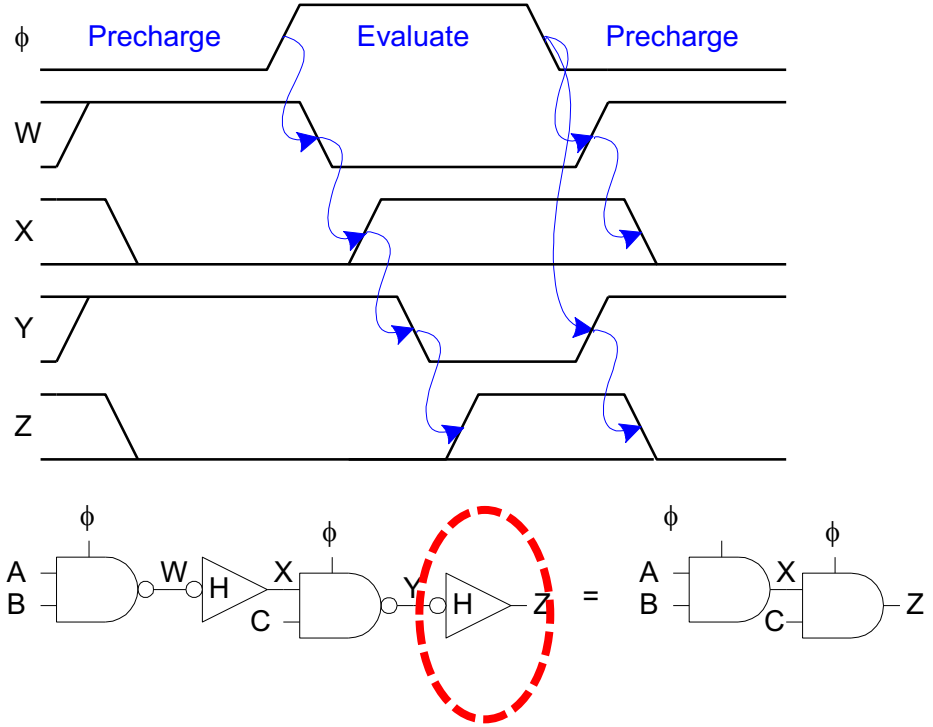
Domino Logic



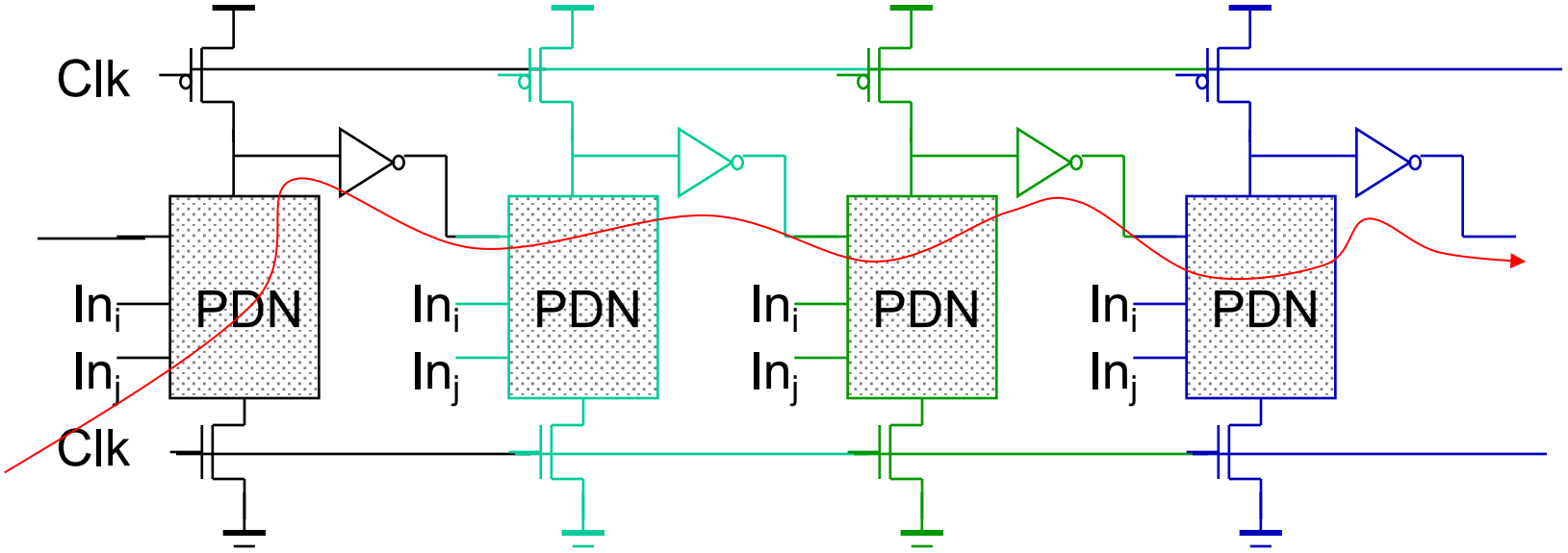
Domino Gates

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs



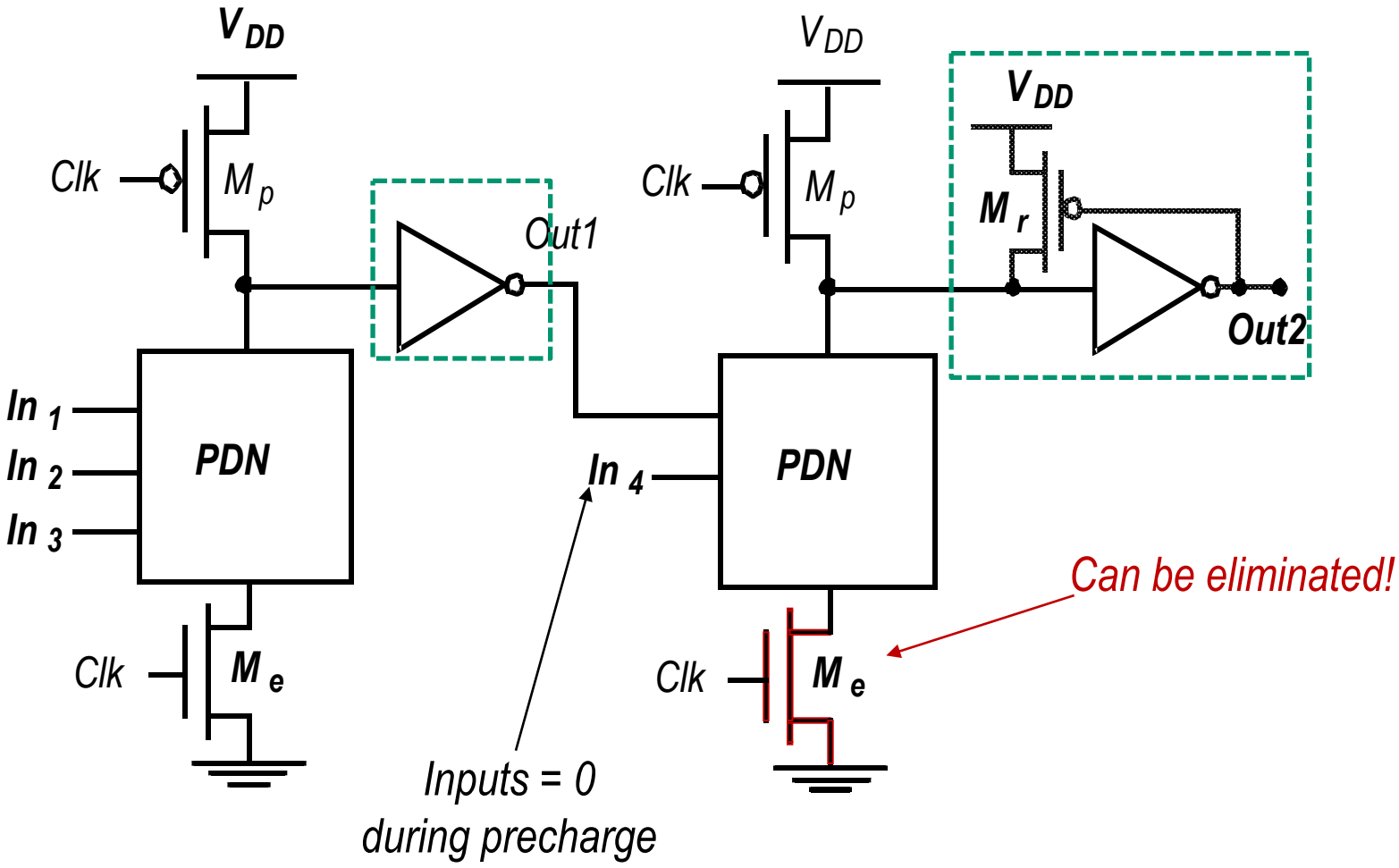


Why Domino?

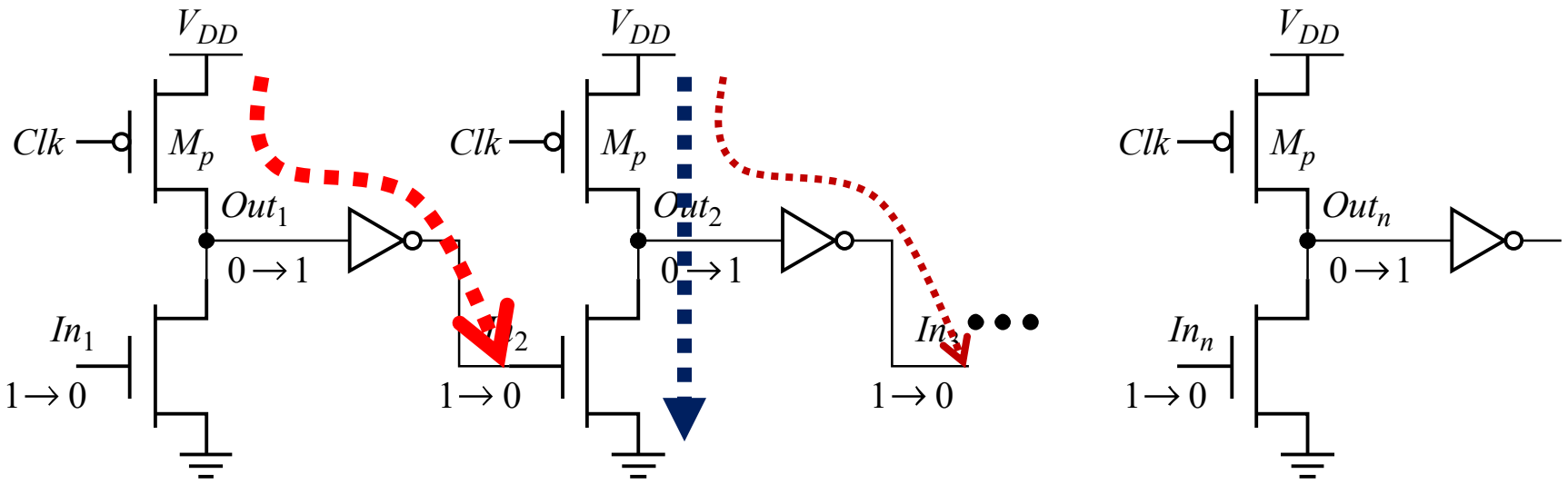


Like falling dominos!

Designing with Domino Logic

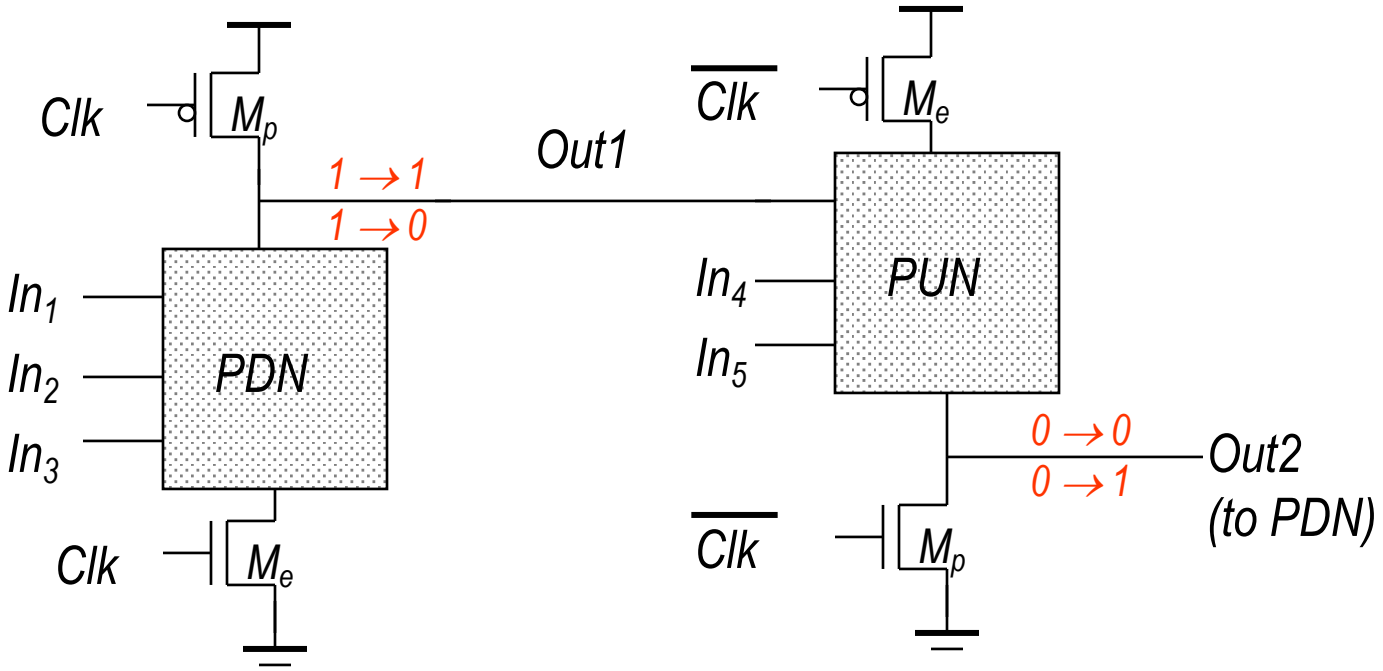


Footless Domino



- ***The first gate in the chain needs a foot switch***
- ***Precharge is rippling – short-circuit current***
- ***A solution is to delay the clock for each stage***

np-CMOS



Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN

Domino Summary

- Domino logic is attractive for high-speed circuits
  - 1.5 – 2x faster than static CMOS
  - But many challenges:
    - Monotonicity
    - Leakage
    - Charge sharing
    - Noise
- Widely used in high-performance microprocessors

Traditional Domino Circuits

- Ping-pang approach for overlapping the precharge time

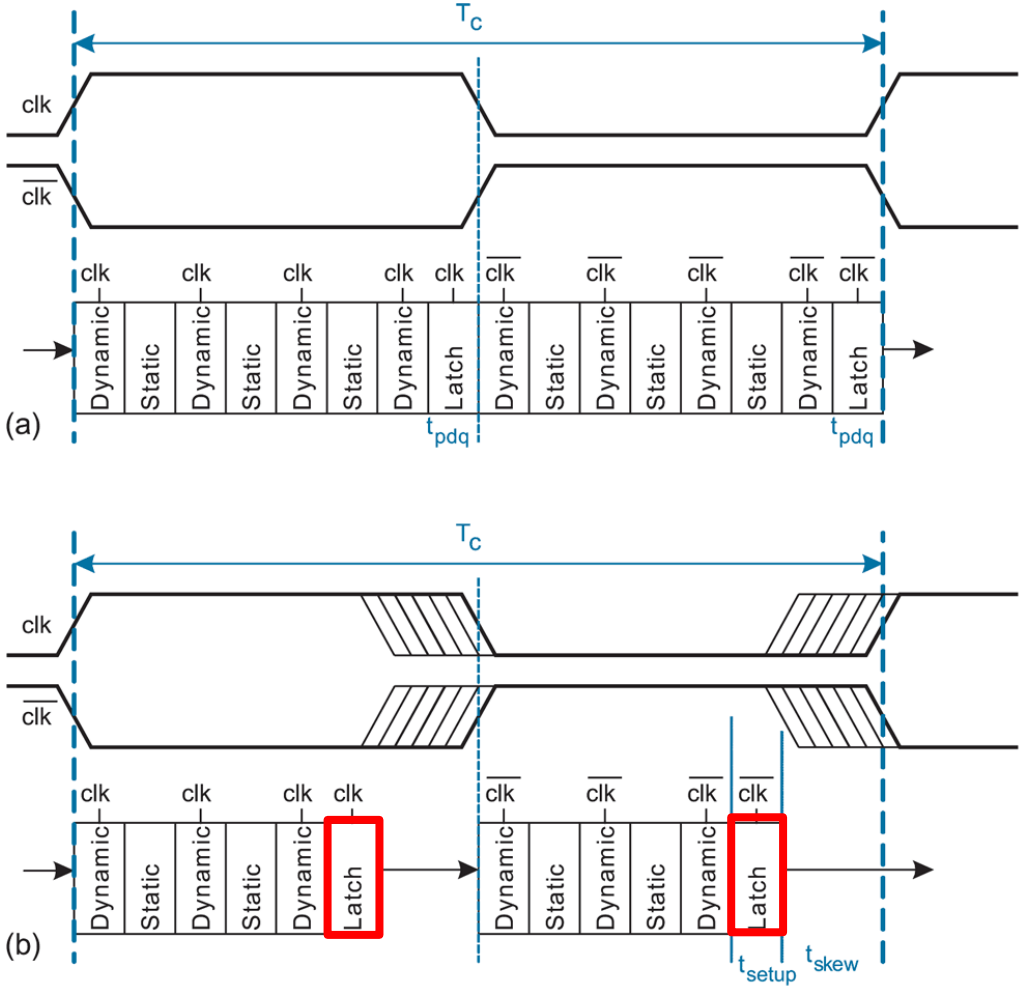


FIG 7.43 Traditional domino circuits

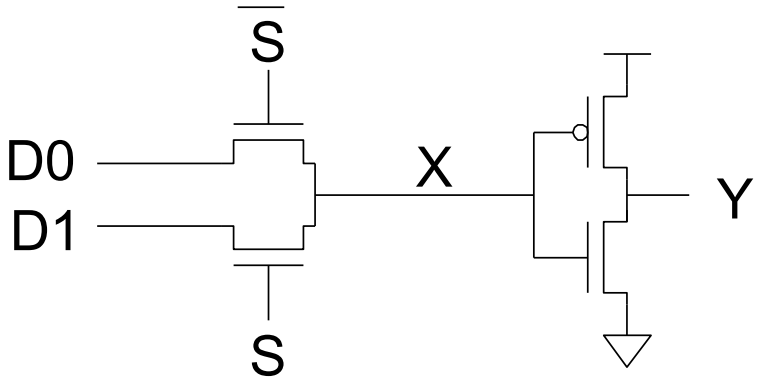
Some circuits pitfalls

Faults… …

Outline

- Circuit Pitfalls
  - Detective puzzle
  - Given circuit and symptom, diagnose cause and recommend solution
  - All these pitfalls have caused failures in real chips

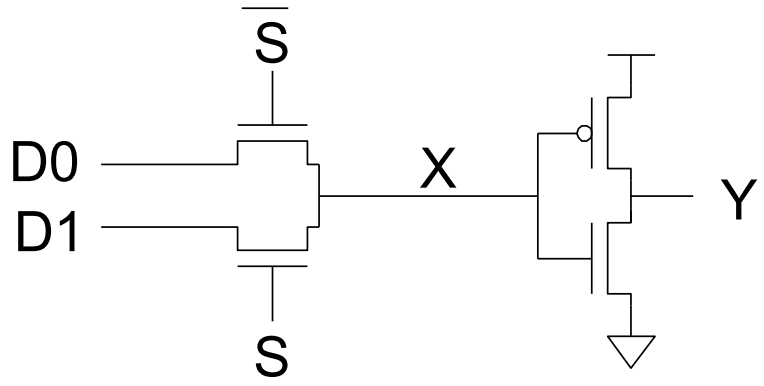
Bad Circuit 1



Symptom

Mux works Y=1 when selected =1 but D=1.

Bad Circuit 1

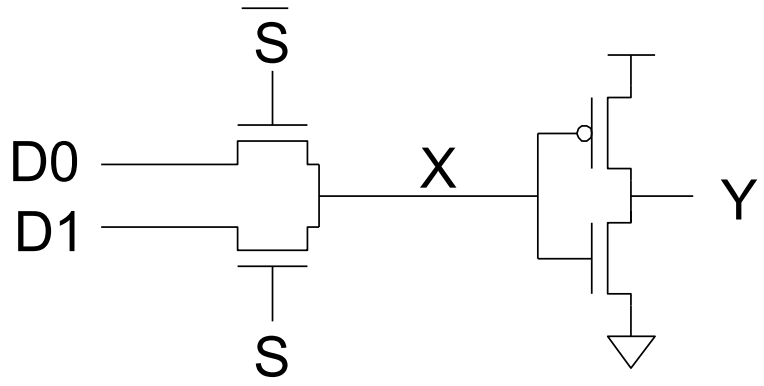


Symptom

Mux works Y=1 when selected =1 but D=1.

- Principle: Threshold drop
  - X never rises above V_{DD}-V_t
  - V_t is raised by the body effect $V_t = V_{t0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$
  - The threshold drop is most serious as V_t becomes a greater fraction of V_{DD}.

Bad Circuit 1



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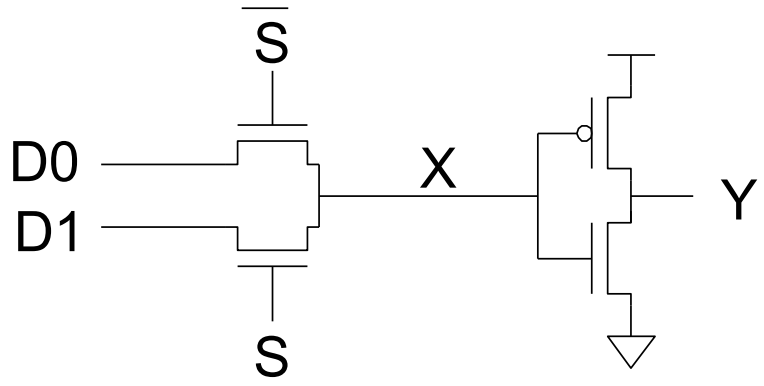
Bad Circuit 1

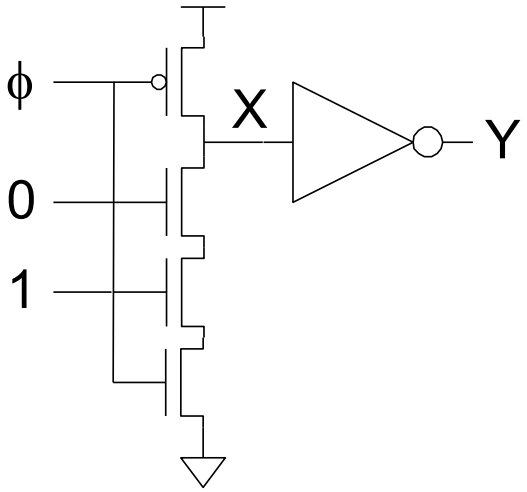


Symptom

Mux works Y=1 when selected =1 but D=1.

- Principle: Threshold drop $V_t = V_{t0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$
  - X never rises above V_{DD}-V_t
  - V_t is raised by the body effect
  - The threshold drop is most serious as V_t becomes a greater fraction of V_{DD}.
- Solution: Use transmission gates, not pass transistors

Bad Circuit 2



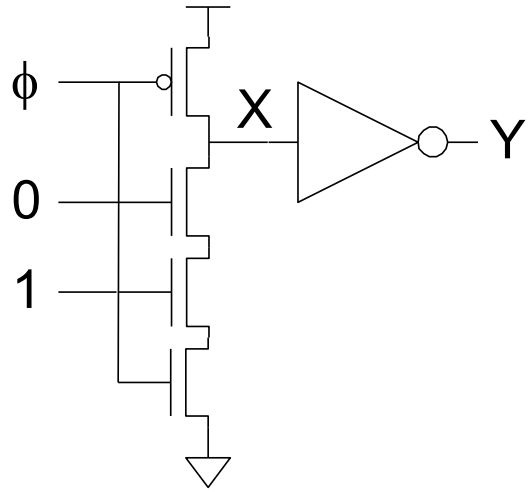
Symptom

Precharge gate (Y=0)

Then evaluate

Eventually Y spontaneously flips to 1

Bad Circuit 2



Symptom

Precharge gate (Y=0)

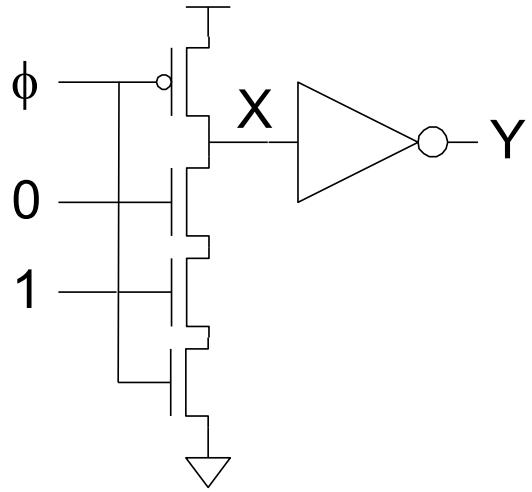
Then evaluate

Eventually Y

spontaneously flips to 1

- Principle: Leakage
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge
- Solution:

Bad Circuit 2



Symptom

Precharge gate (Y=0)

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- Principle: Leakage
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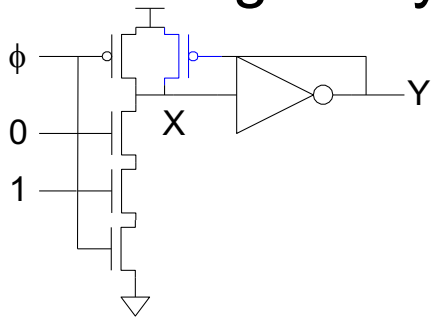
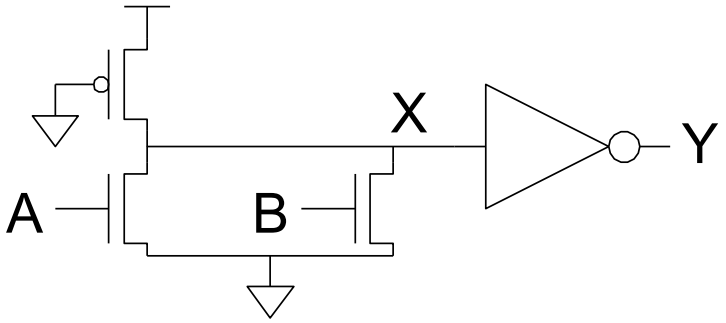


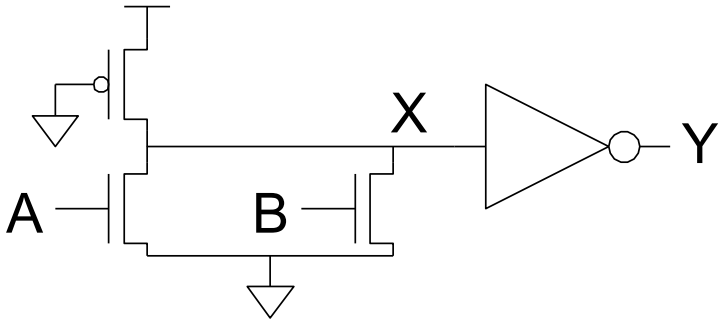
Bad Circuit 3



Symptom

When only one input is true, **Y = 0.**

Bad Circuit 3

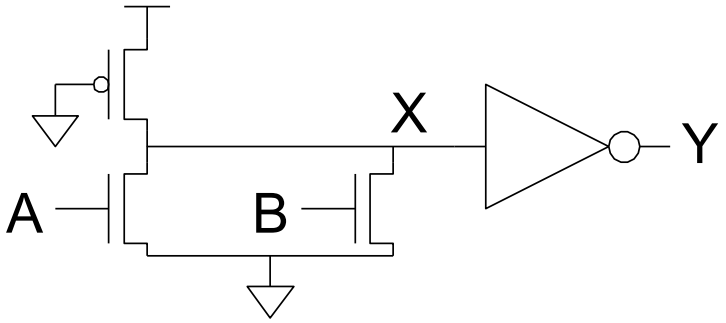


Symptom

When only one input is true, **Y = 0.**

- Principle: Ratio Failure
  - nMOS and pMOS fight each other.
  - If the pMOS is too strong, nMOS cannot pull X low enough.
- Solution:

Bad Circuit 3

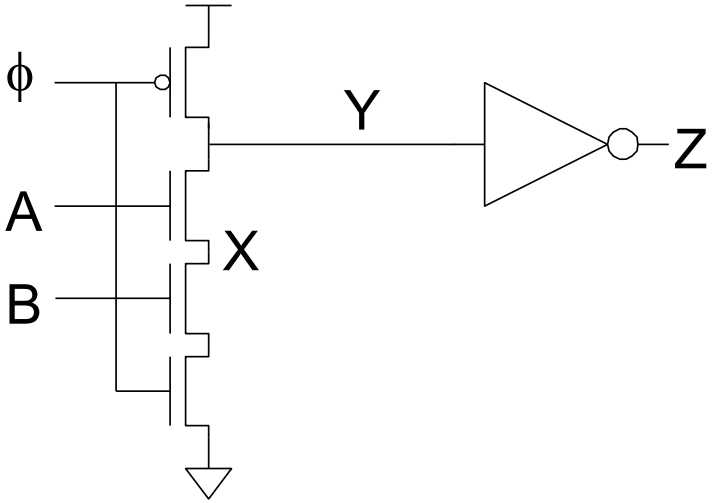


Symptom

When only one input is true, **Y = 0.**

- Principle: Ratio Failure
  - nMOS and pMOS fight each other.
  - If the pMOS is too strong, nMOS cannot pull X low enough.
- Solution:Check that ratio is satisfied in all corners

Bad Circuit 4



Symptom

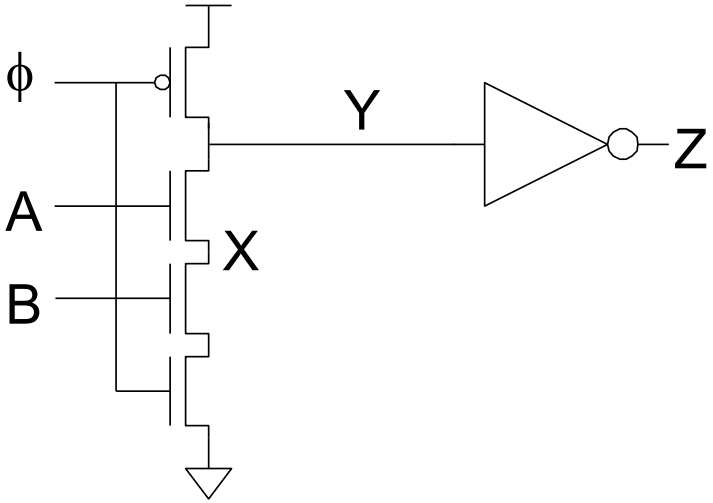
Precharge gate while

A = B = 0, so Z = 0 Set f = 1

A rises

Z is observed to sometimes rise

Bad Circuit 4



Symptom

Precharge gate while

A = B = 0, so Z = 0 Set f = 1

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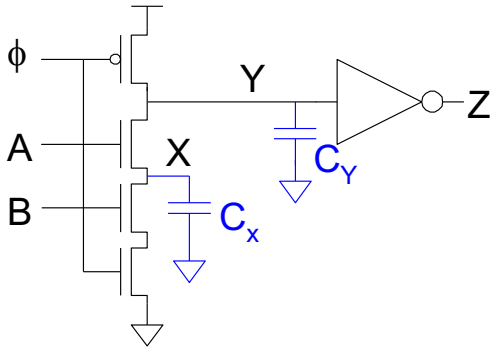
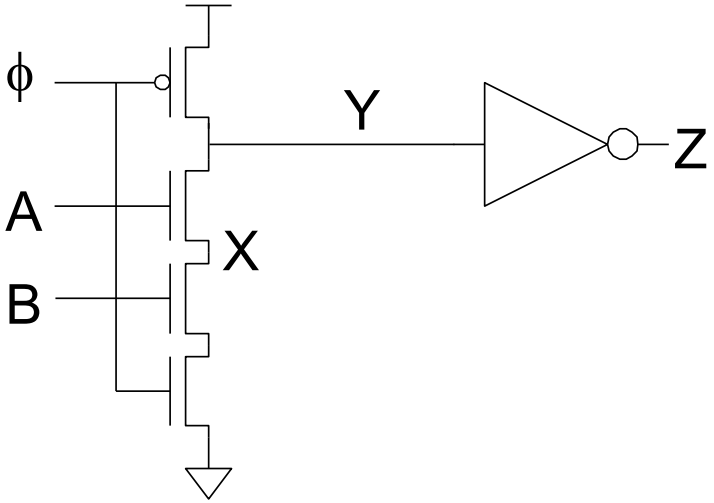
Z is observed to sometimes rise

- Principle: Charge Sharing
  - If X was low, it shares charge with Y



Bad Circuit 4



Symptom

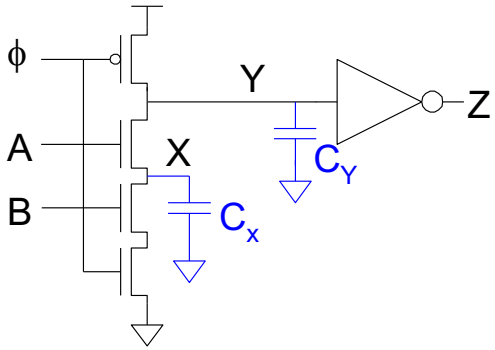
Precharge gate while

A = B = 0, so Z = 0 Set f = 1

A rises

Z is observed to sometimes rise

- Principle: Charge Sharing
  - If X was low, it shares charge with Y
- Solutions: Limit charge sharing
  - Safe if $C_Y >> C_X$ $V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$
  - Or precharge node X too



Summary

- Static CMOS gates are very robust
  - Logic effect/Fan-in relate to the delay/Power evalutation
- Other circuits suffer from a variety of pitfalls
  - Pseodu NMOS logic
  - Pass transistor
    - cascade problem ,restorer(keeper),some pass logic
  - Dynamic logic
    - Characteristic
    - Cascade issue
    - Domino logic
    - Some pitfalls of dynamic logic