Digital Integrated Circuits

Inverter

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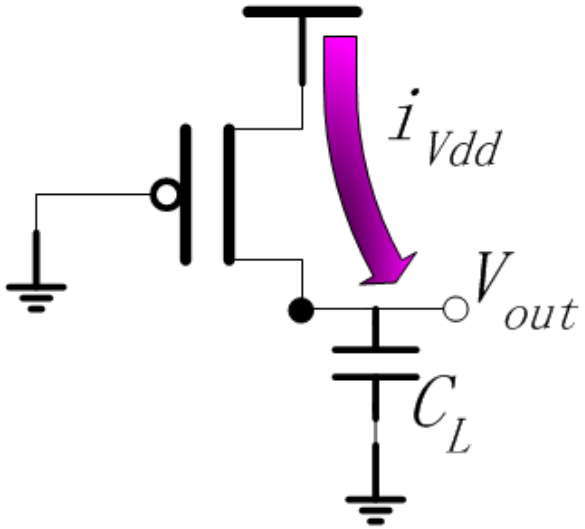
CMOS Inverter

- At a glance
- Static behavior
- Dynamic behavior
- ***Power, Energy, and Energy Delay***
- Perspective tech.

Dynamic Power Consumption

- (dis)charge process
  - C_L is charged through pMOS on-resistance
  - C_L is discharged through nMOS on-resistance
- Power distribution
  - Charge processing:One part of Supply power is dissipated in the pMOS transistor,another part is dissipated in the charge C_L
  - Discharge processing:all dissipated in the nMOS transistor

Precise measure of dynamic power consumption



$$E_{V_{dd}} = \int_0^\infty i_{V_{dd}}(t) V_{dd}\, dt = V_{dd} \int_0^\infty C_L \frac{dv_{out}}{dt} dt$$

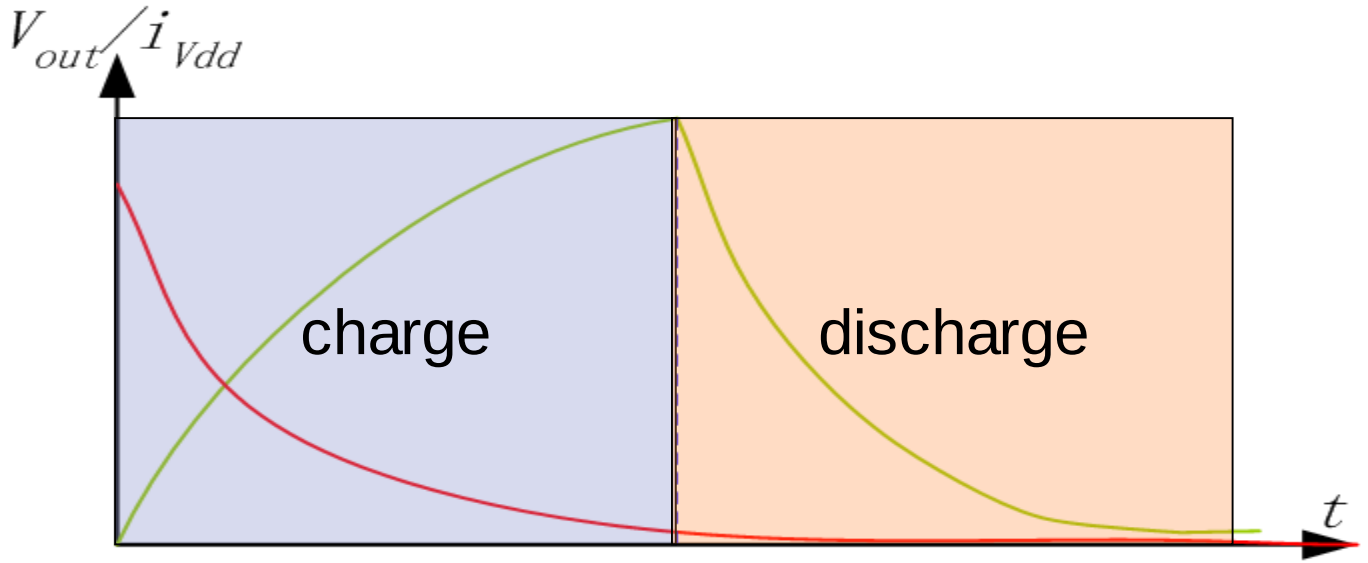
$$= C_L V_{dd} \int_0^{V_{dd}} dv_{out} = C_L V_{dd}^2$$

$$E_C = \int_0^\infty i_{V_{dd}}(t) v_{out}\, dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out}\, dt$$

$$= C_L \int_0^{V_{dd}} v_{out}\, dv_{out} = \frac{C_L V_{dd}^2}{2}$$

Output voltages and supply current during (dis)charge of C_L

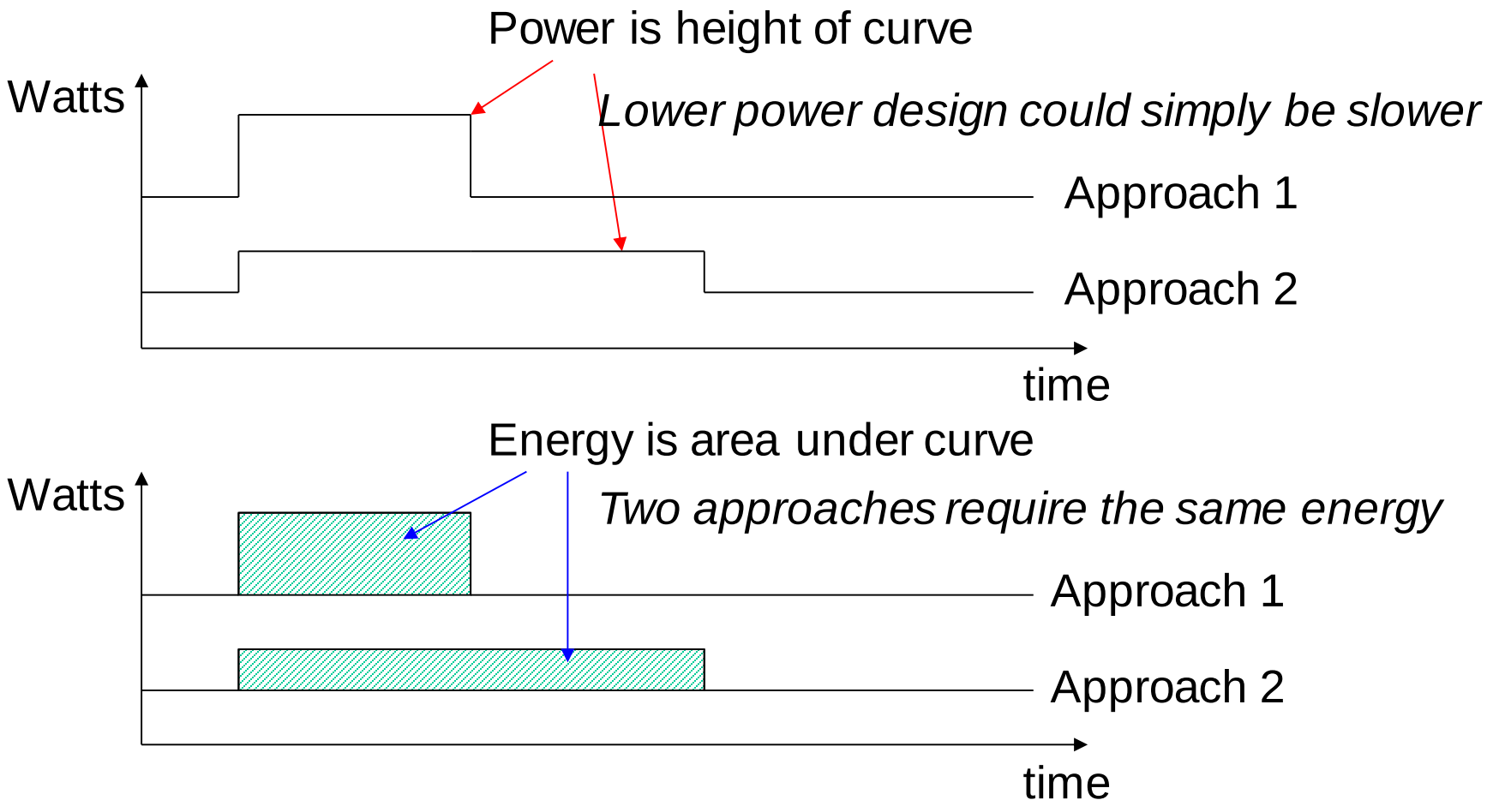
- Energy dissipation is independent of the size
- Power consumption is dependent of device switching number.



Power and Energy Figures of Merit

- Power consumption in Watts
  - determines battery life in hours
- Peak power
  - determines power ground wiring designs
  - sets packaging limits
  - impacts signal noise margin and reliability analysis
- Energy efficiency in Joules
  - rate at which power is consumed over time
- Energy = power * delay
  - Joules = Watts * seconds
  - lower energy number means less power to perform a computation at the same frequency

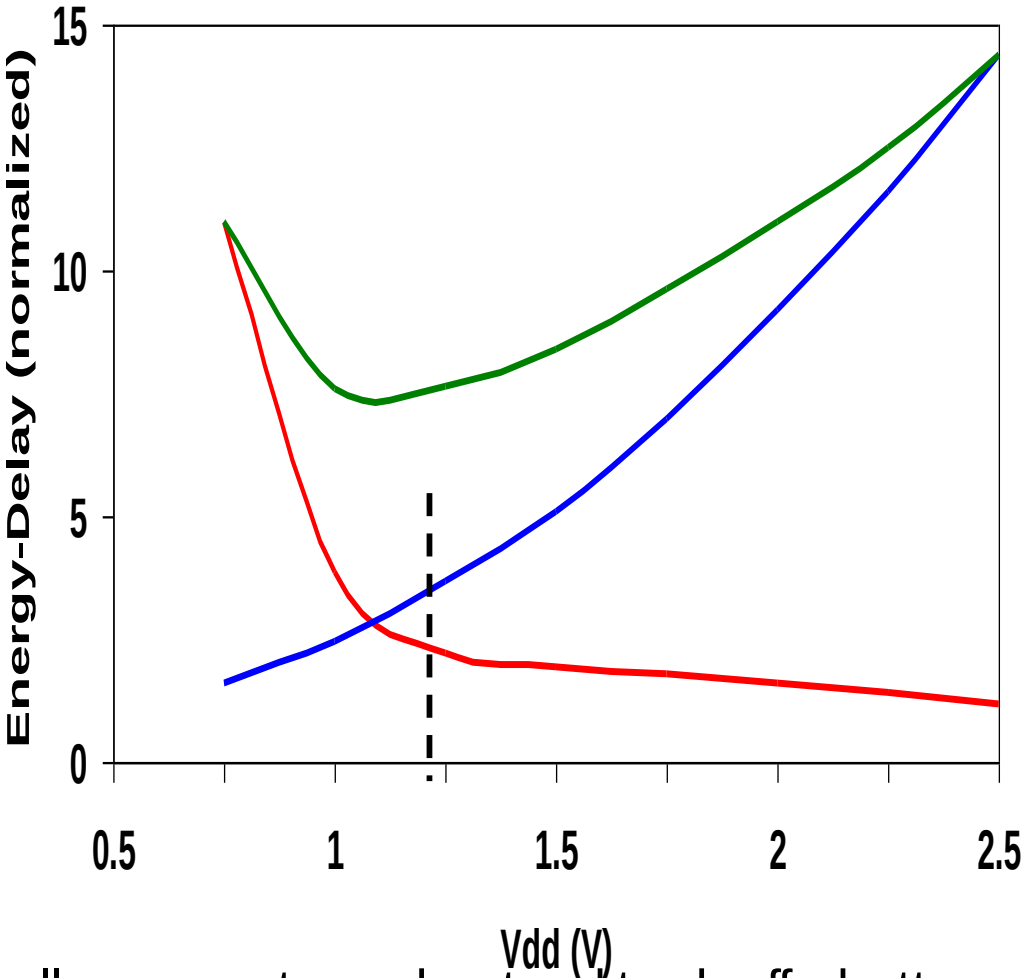
Power versus Energy



PDP and EDP

- Power-delay product (PDP) = $P_{av} * t_p = (C_L V_{DD}^2)/2$
  - PDP is the average energy consumed per switching event (Watts * sec = Joule)
  - lower power design could simply be a slower design
- Energy-delay product (EDP) = PDP * $t_p = P_{av} * t_p^2$
  - EDP is the average energy consumed multiplied by the computation time required
  - takes into account that one can trade increased delay for lower energy/operation(e.g.,via supply voltage scaling that increases delay,but decreases energy consumption)

PDP and EDP



energy-delay

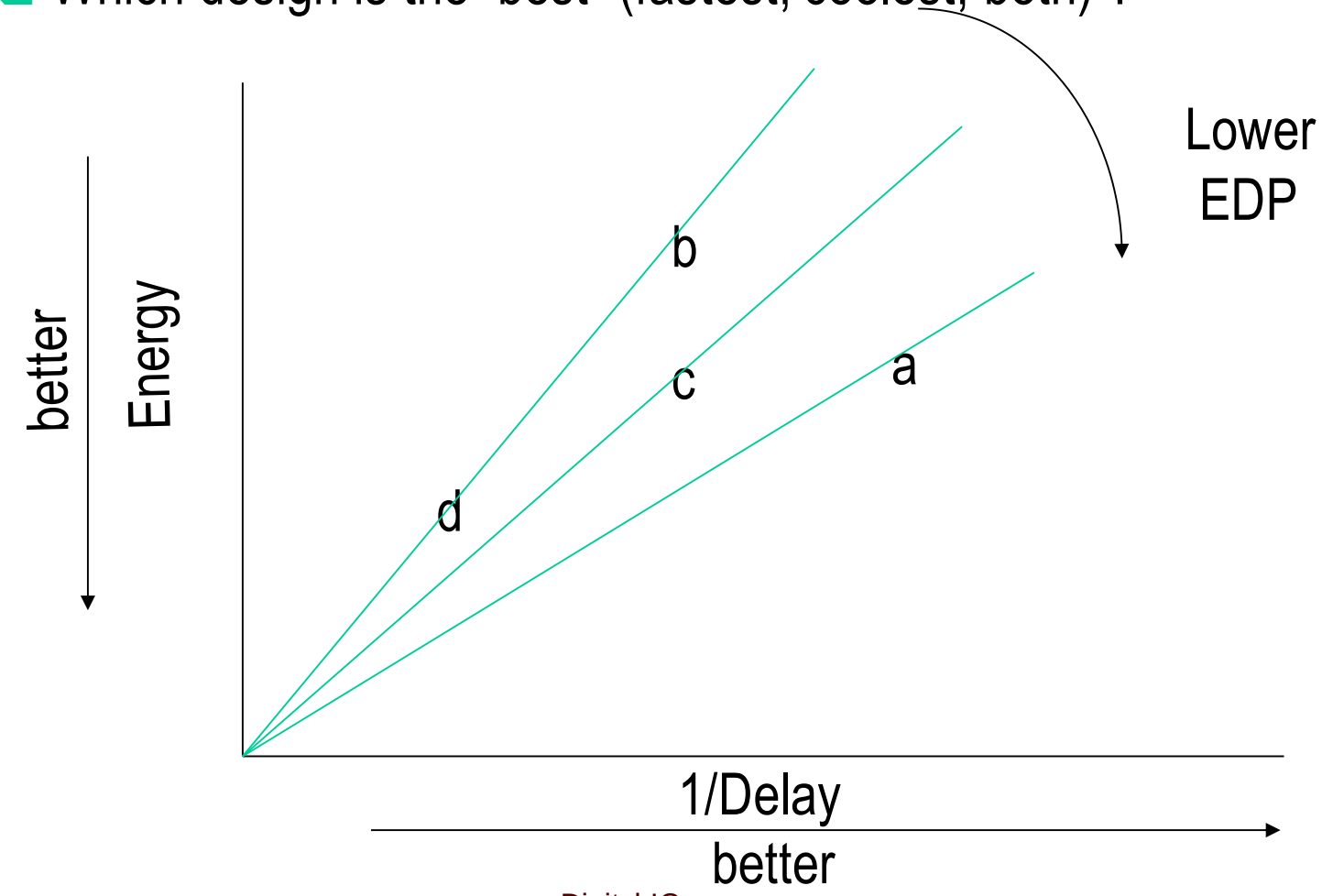
energy

delay

allows one to understand tradeoffs better

Understanding Tradeoffs

- Which design is the “best” (fastest, coolest, both) ?



Where Does Power Go in CMOS?

- Dynamic Power Consumption
  - Charging and Discharging Capacitors
- Short Circuit Currents
  - Short Circuit Path between Supply Rails during Switching
- Leakage
  - Leaking diodes and transistors

CMOS Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage} 1/f_{clock}$$

$$f_{0\rightarrow1} = P_{0\rightarrow1} * f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leakage}$$

Dynamic power ***Short-circuit power*** ***Leakage power***

Lowering Dynamic Power

Capacitance:
Function of fan-out, wire length, transistor sizes

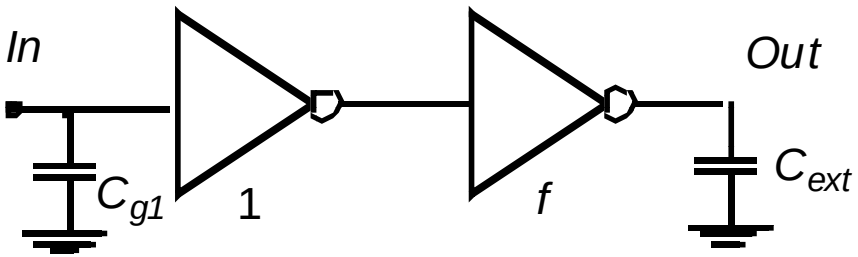
Supply Voltage:
Has been dropping with successive generations

$$P_{dyn} = C_L \, V_{DD}^2 \, P_{0\rightarrow1} \, f$$

Activity factor:
How often, on average, do wires switch?

Clock frequency:
Increasing…

Transistor Sizing for Minimum Energy



- *Goal: Minimize Energy of whole circuit*
  - Design parameters: *f* and V_{DD}
  - $t_p \le t_{pref}$ of circuit with *f*=1 and $V_{DD} = V_{ref}$

$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right) \qquad I_{DSAT} = k'\frac{W}{L}\left(V_{GT}V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$$

$$t_{p0} \propto \frac{V_{DD}}{V_{DD}-V_{TE}}$$

$$t_{pLH} = \ln(2)R_{eqn}C = 0.69 * \frac{3V_{DD}}{4I_{DSATn}}(1-\lambda V_{DD})C_L$$

Transistor Sizing (2)

- ***Performance Constraint (γ=1)***

$$\frac{t_p}{t_{pref}} = \frac{t_{p0}}{t_{p0ref}} \frac{\left(2+f+\frac{F}{f}\right)}{(3+F)} = \frac{V_{DD}}{V_{ref}} \frac{V_{ref}-V_{TE}}{V_{DD}-V_{TE}} \frac{\left(2+f+\frac{F}{f}\right)}{(3+F)} = 1$$

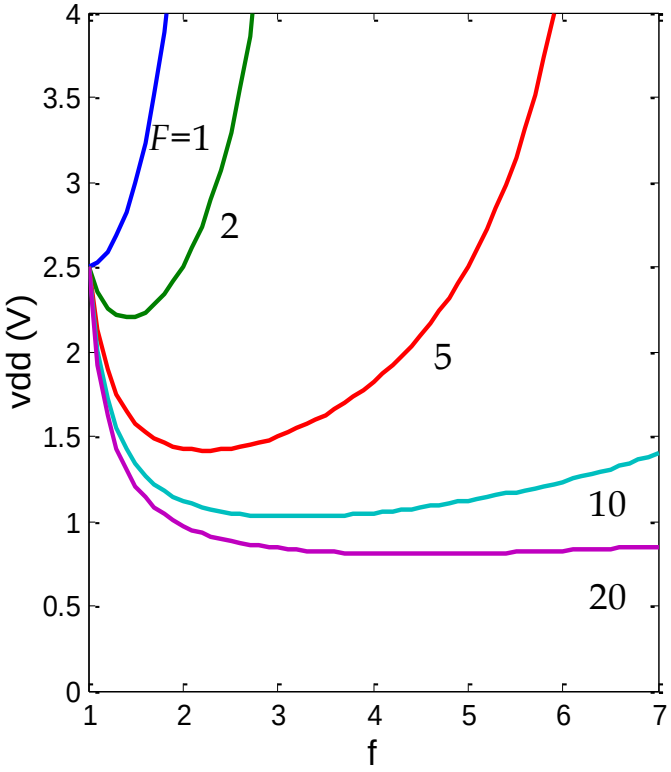
- ***Energy for single Transition***

$$E = V_{DD}^2 C_{g1}\left[(1+\gamma)(1+f)+F\right]$$

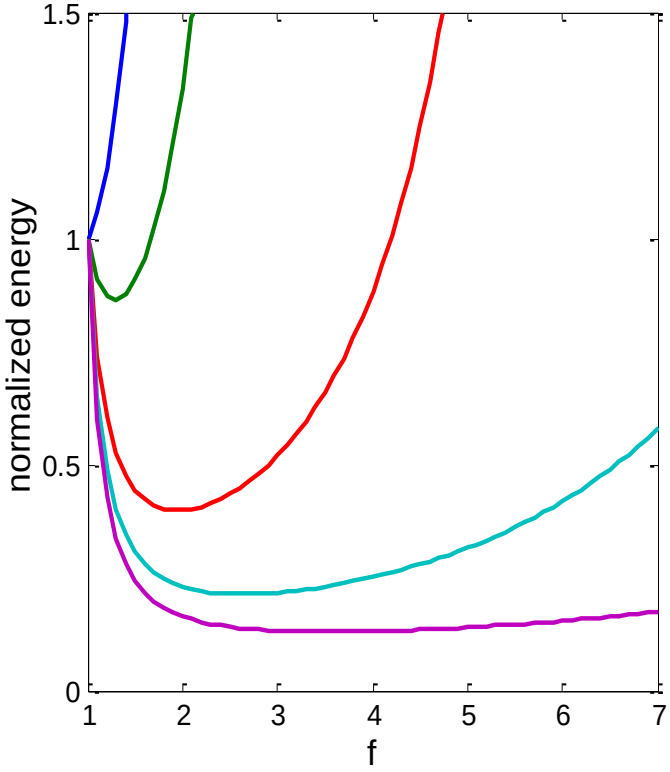
$$\frac{E}{E_{ref}} = \left(\frac{V_{DD}}{V_{ref}}\right)^2 \left(\frac{2+2f+F}{4+F}\right)$$

Transistor Sizing (3)

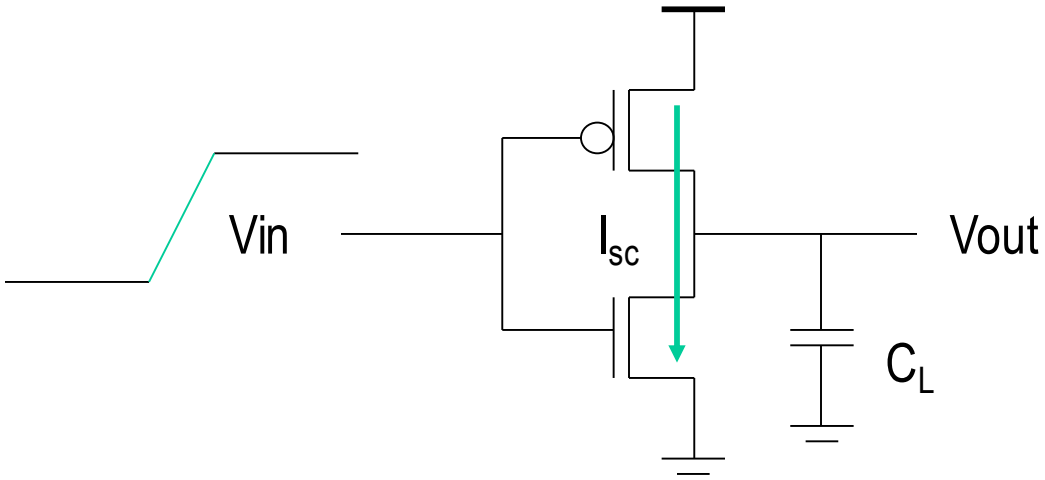
V_{DD}=f(f)

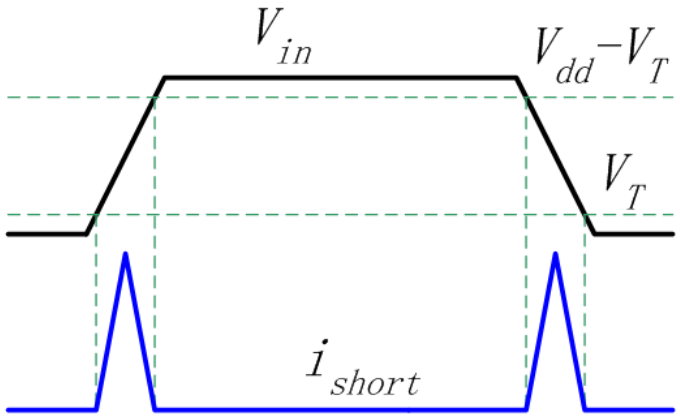


E/E_{ref}=f(f)



Short Circuit Power Consumption



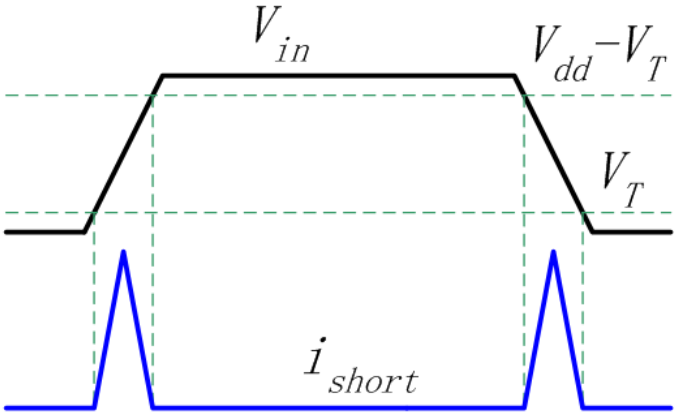


Finite slope of the input signal causes a direct current path between V_{DD} and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

Short Circuit power consumption

- Energy of ever switch activity

$$E_{dp} = V_{dd}\frac{I_{peak}}{2}t_{rise} + V_{dd}\frac{I_{peak}}{2}t_{fa}$$



- Average power

$$P_{dp} = \frac{t_{rise} + t_{fall}}{2} V_{dd} I_{peak} f$$

- ***Short circuit occupy no more than 20% of dynamic power***

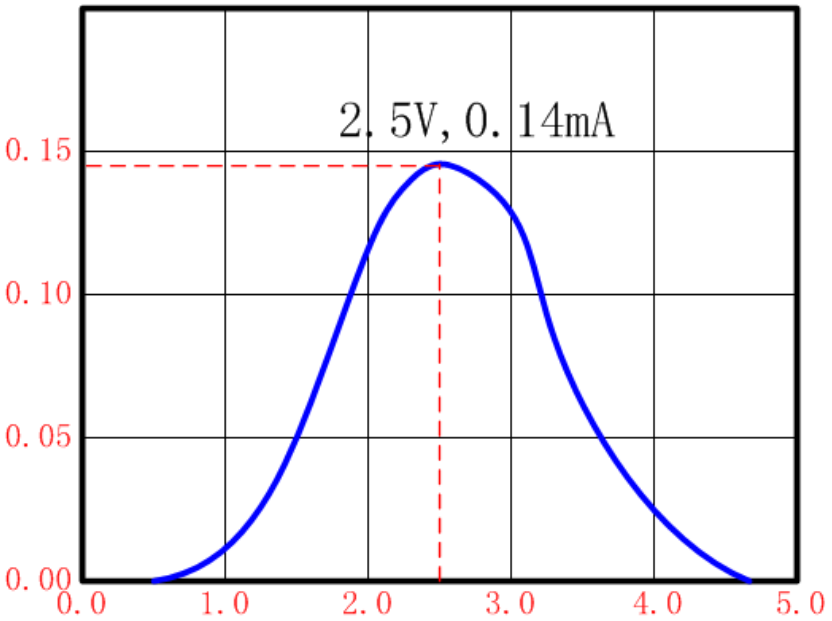
$$t_{sc} = \frac{V_{DD} - 2V_T}{V_{DD}} t_s \approx \frac{V_{DD} - 2V_T}{V_{DD}} \times \frac{t_{r(f)}}{0.8}$$

An example

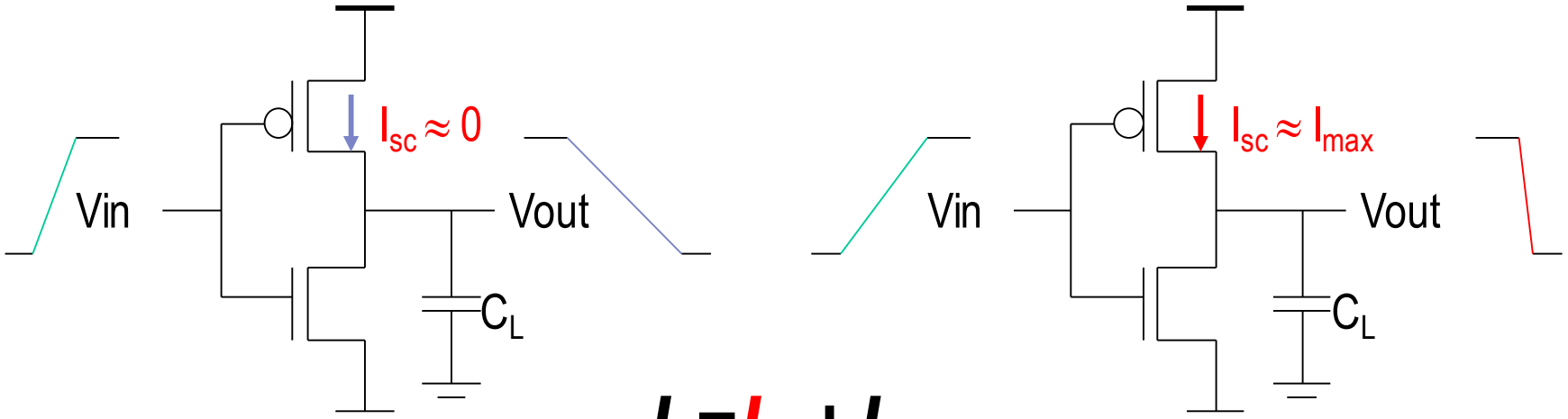
- Assume rise/fall time both are 300ps
- Short circuit power:

  300ps×5V × 0.14mA=0.21pJ
- Dynamic power

  30pF × 5V × 5V=0.75pJ



Impact of C_L on P_{sc}



$$I_n = I_{sc} + I_d$$

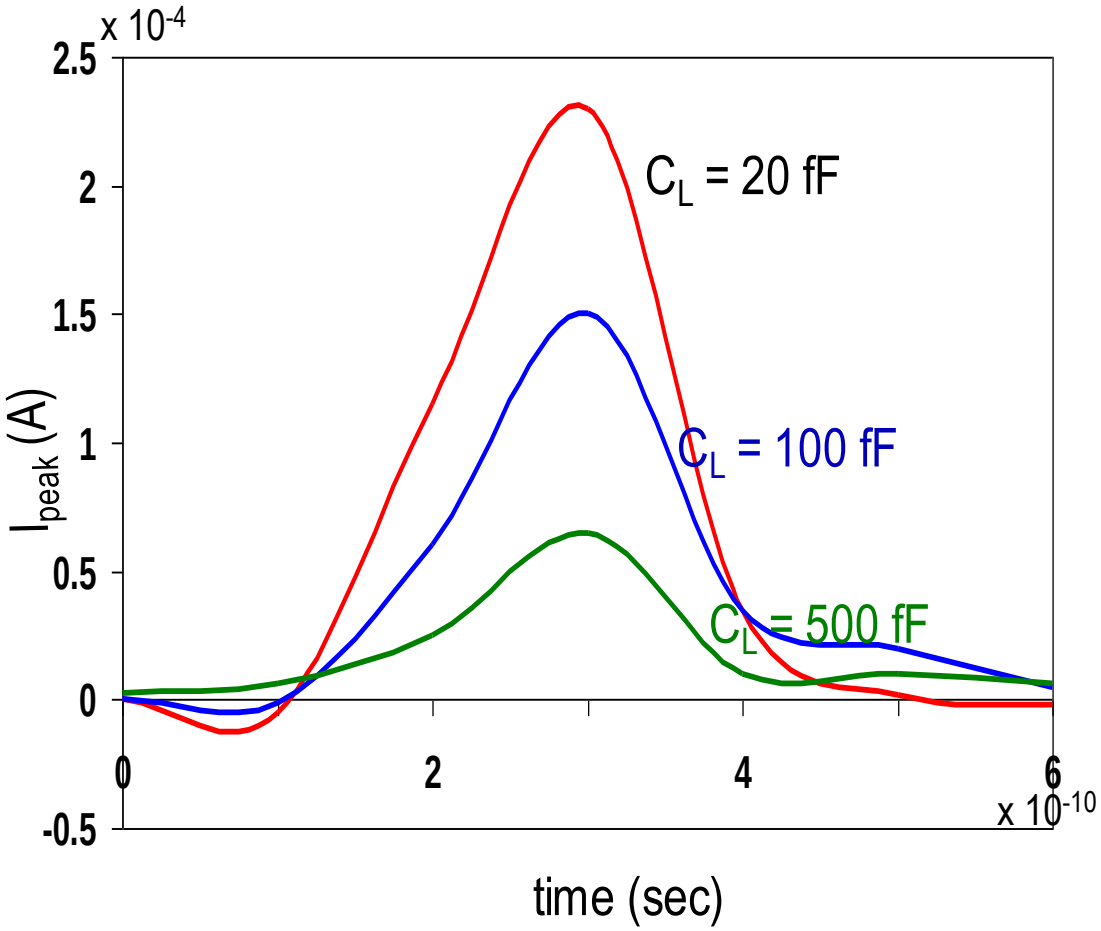
Large capacitive load

Output fall time significantly larger than input rise time.

Small capacitive load

Output fall time substantially smaller than the input rise time.

I_{peak} as a Function of C_L

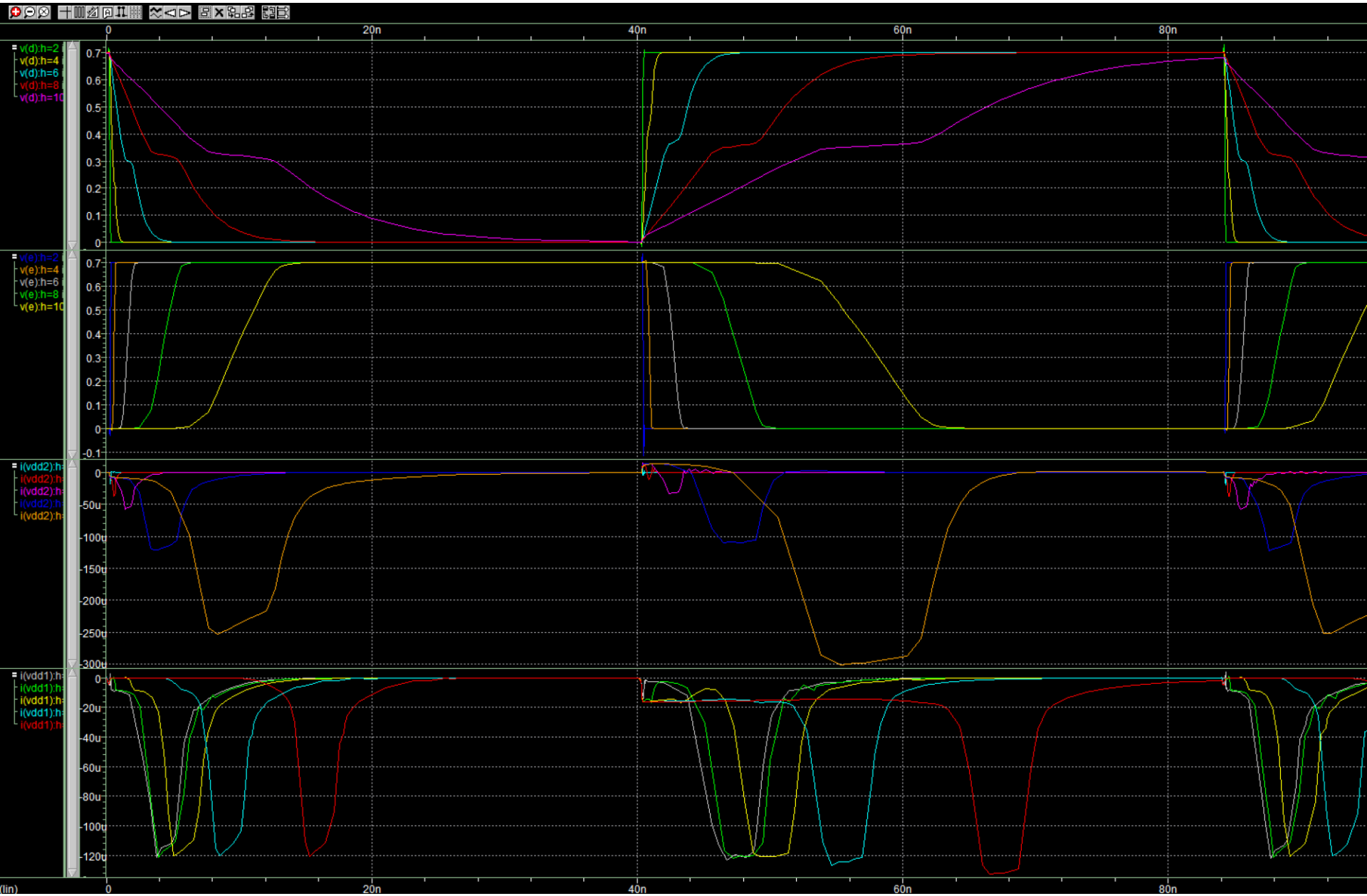


500 psec input slope

When load capacitance is small, I_{peak} is large.

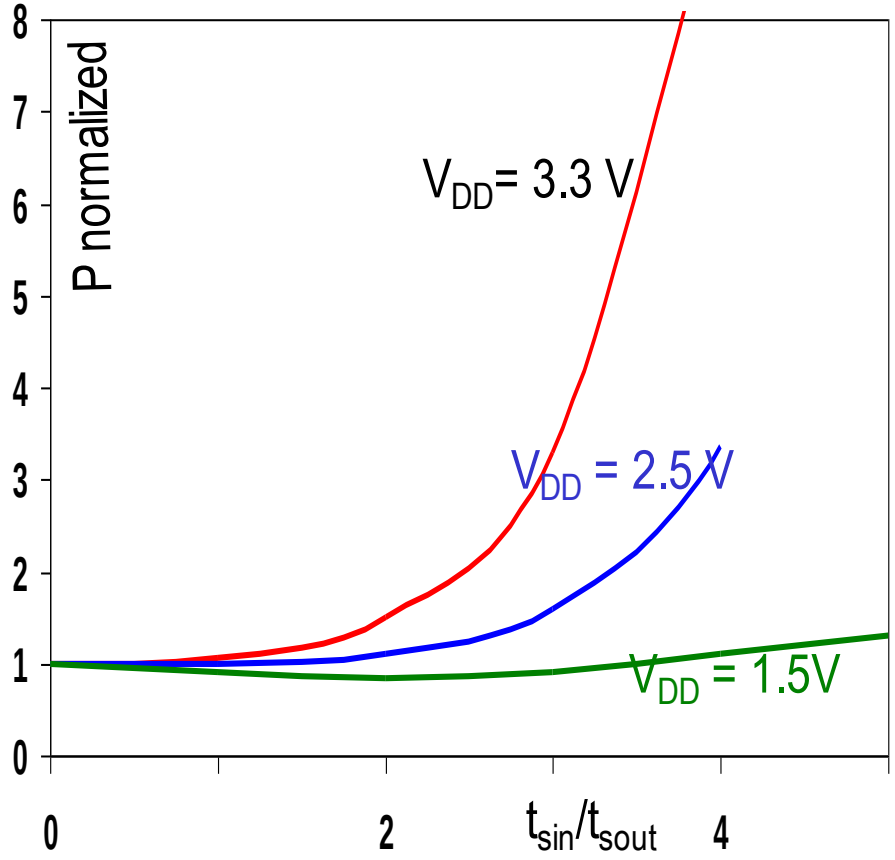
Short circuit dissipation is minimized by matching the rise/fall times of the input and output signals - slope engineering.

```
.global gnd
.subckt inv a y vdd1 N=4 P=8
M1 y a gnd gnd NMOS W=N L=2
+ AS=N+5 PS='2*N+10' AD='N+5' PD='2*N+10'
M2 y a vdd1 vdd1 PMOS W='2*N' L=2
+ AS='P+5' PS='2*P+10' AD='P+5' PD='2*P+10'
.ends
*---------------------------------------------------
*simulation netlist
*---------------------------------------------------
vdd1 vdd1 gnd 'SUPPLY'
vdd2 vdd2 gnd 'SUPPLY'
vin a gnd PULSE 0 'SUPPLY' 0ps 100ps 100ps 40000ps 84000ps
*shape input waveform
X1 a b vdd1 inv  N=2
*reshape input waveform
X2 b c vdd1 inv   N=2**2
*device under test
x3 c d vdd1 inv N=8
*load
x4 d e vdd2 inv  N=H**4
*load on load
x5 e f vdd1 inv   N=8
X6 f h vdd1 inv  N=4*1000
```


0
20n
40n
60n
80n
v(d):h=2
v(d):h=4
v(d):h=6
v(d):h=8
v(d):h=10
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
v(e):h=2
v(e):h=4
v(e):h=6
v(e):h=8
v(e):h=10
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
i(vdd2):h
i(vdd2):h
i(vdd2):h
i(vdd2):h
i(vdd2):h
0
-50u
-100u
-150u
-200u
-250u
-300u
i(vdd1):h
i(vdd1):h
i(vdd1):h
i(vdd1):h
i(vdd1):h
0
-20u
-40u
-60u
-80u
-100u
-120u
(lin)
0
20n
40n
60n
80n

Digital IC

P_{sc} as a Function of Rise/Fall Times



When load capacitance is small (t_{sin}/t_{sout} > 2 for V_{DD} > 2V) the power is dominated by P_{sc}

If $V_{DD} < V_{Tn} + |V_{Tp}|$ then P_{sc} is eliminated since both devices are never on at the same time.

W/L_p = 1.125 μm/0.25 μm
W/L_n = 0.375 μm/0.25 μm
C_L = 30 fF

normalized wrt zero input rise-time dissipation

Switching power

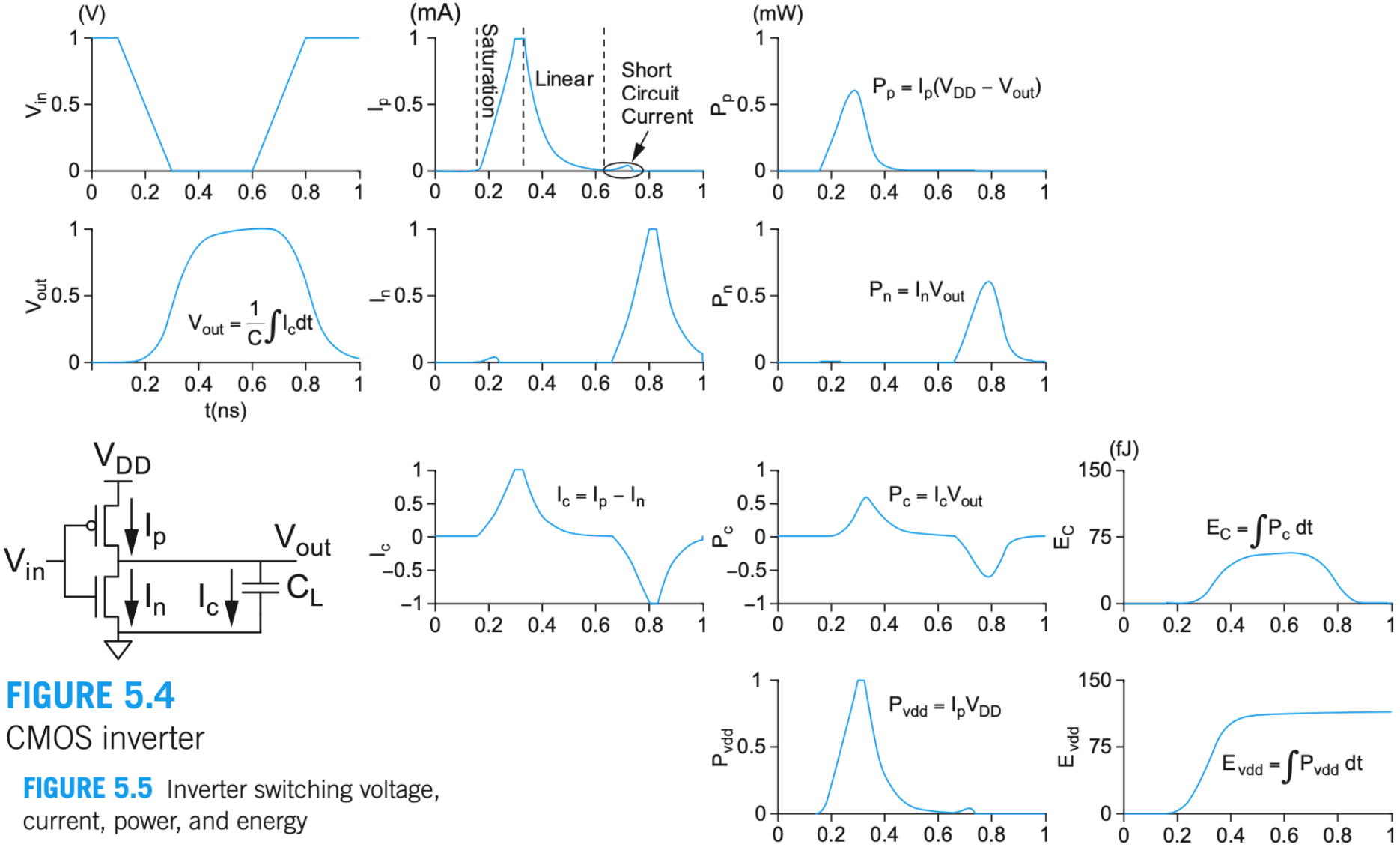


FIGURE 5.4
CMOS inverter

FIGURE 5.5 Inverter switching voltage, current, power, and energy

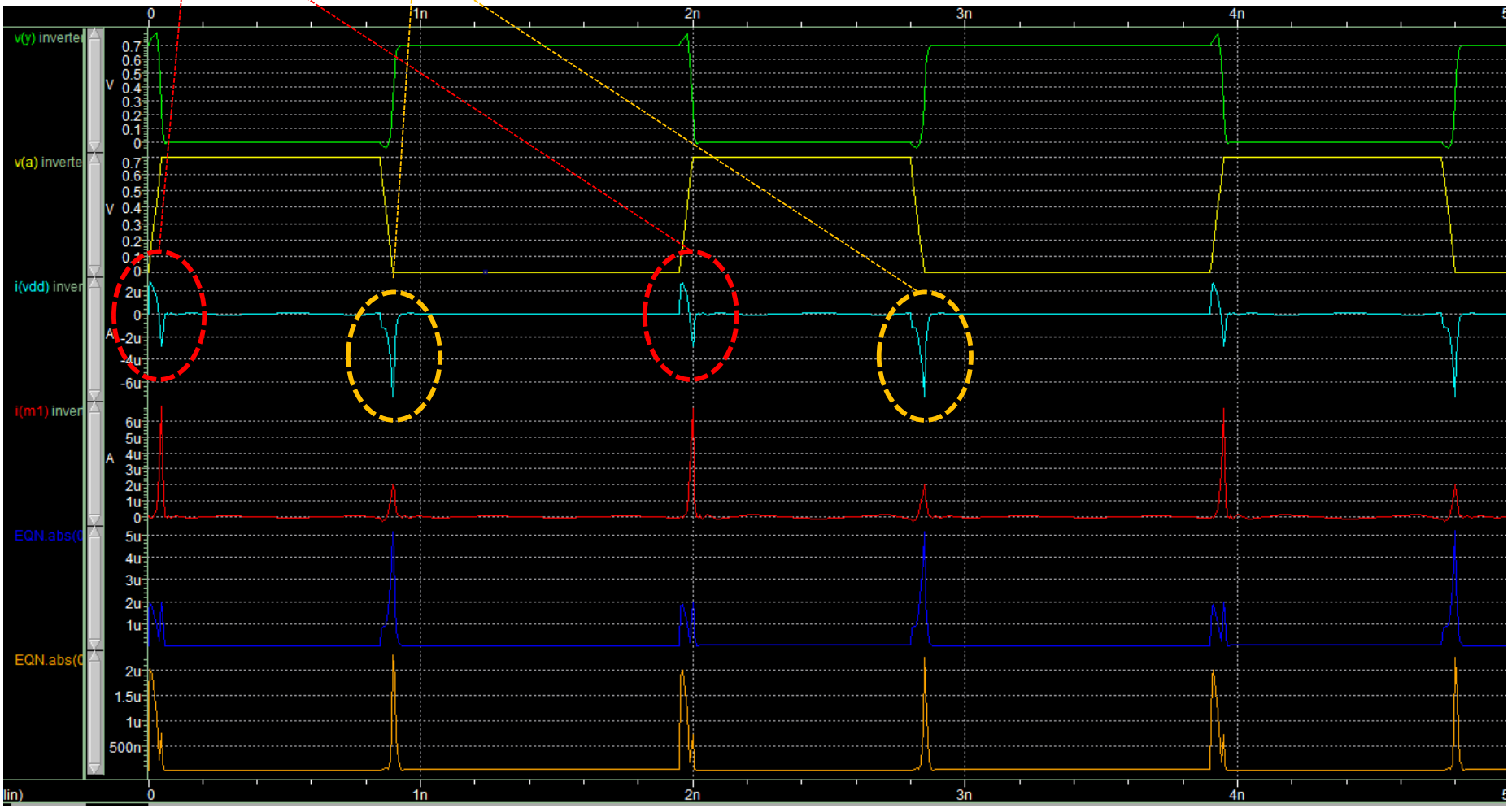
Power Testing

inverter - 记事本

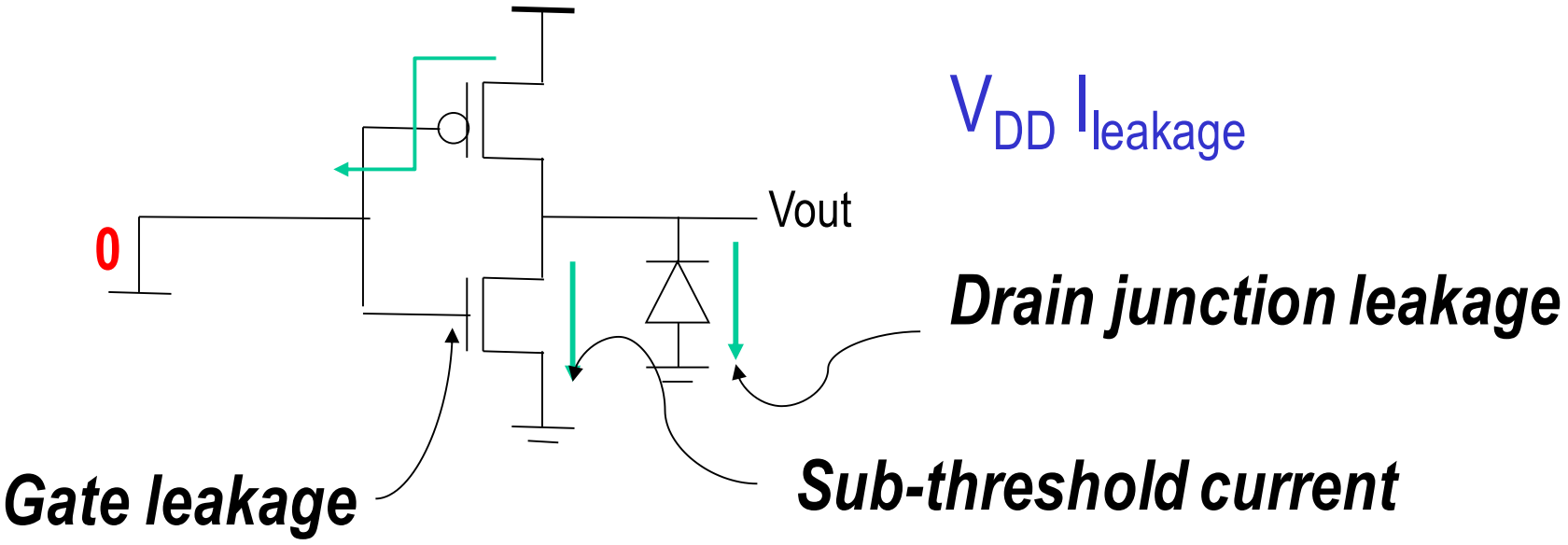
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

```
* cmos.sp
.option node
*.option list
.probe I(*) V(*)
********************************************************************************
* Parameters and models
********************************************************************************
.param SUPPLY=0.7
.option scale=16n
.param N1=3
.include '../LIB/16nm_HP.pm'

.temp 70
.option post

********************************************************************************
* Simulation netlist
********************************************************************************
Vdd     vdd     gnd     'SUPPLY'
Vin     a       gnd     PULSE(0 'SUPPLY' 0ps 50ps 50ps 800ps 1950ps
M1      y       a       gnd     gnd     NMOS    W=4     L=2
M2      y       a       vdd     vdd     PMOS    W=N1*3    L=2

*C1 y a 1f

********************************************************************************
* Stimulus
********************************************************************************

*.tran  100p 10n
*.plot i(y)
* sweep N1 2 30 2
.tran  10p 5n
*sweep supply 0.2 1.5 0.1
.MEASURE TRAN tdlay TRIG V(a) VAL = 'SUPPLY/2'  RISE = 1 TARG V(y) VAL = 'SUPPLY/2' FALL = 1
.end
```

Power Testing



Leakage (Static) Power Consumption



Sub-threshold current is the dominant factor.
All increase exponentially with temperature!

TSMC Processes Leakage and V_T

	CL018 G	CL018 LP	CL018 ULP	CL018 HS	CL015 HS	CL013 HS
V_{dd}	1.8 V	1.8 V	1.8 V	2 V	1.5 V	1.2 V
T_{ox} (effective)	42 Å	42 Å	42 Å	42 Å	29 Å	24 Å
L_{gate}	0.16 μm	0.16 μm	0.18 μm	0.13 μm	0.11 μm	0.08 μm
I_{DSat} (n/p) (μA/μm)	600/260	500/180	320/130	780/360	860/370	920/400
I_{off} (leakage) (ρA/μm)	20	1.60	0.15	300	1,800	13,00
V_{Tn}	0.42 V	0.63 V	0.73 V	0.40 V	0.29 V	0.25 V
FET Perf. (GHz)	30	22	14	43	52	80

From MPR, 2000

Principles for Power Reduction

- ***Prime choice: Reduce voltage!***
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question
- ***Reduce switching activity***
- ***Reduce physical capacitance***
  - Device Sizing: for F=20
    - f_{opt}(energy)=3.53, f_{opt}(performance)=4.47

Review: Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage} 1/f_{clock}$$

$$f_{0\rightarrow1} = P_{0\rightarrow1} * f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leakage}$$

Dynamic power (~90% today and decreasing relatively)

Short-circuit power (~8% today and decreasing absolutely)

Leakage power (~2% today and ***increasing***)

CMOS Inverter

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- Static behavior
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- Power, Energy, and Energy Delay
- ***Perspective tech.***

Technology Evolution

International Technology Roadmap for Semiconductors

Year of Introduction	1999	2000	2001	2004	2008	2011	2014
Technology node [nm]	180		130	90	60	40	30
Supply [V]	1.5-1.8	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	0.3-0.6
Wiring levels	6-7	6-7	7	8	9	9-10	10
Max frequency [GHz],Local-Global	1.2	1.6-1.4	2.1-1.6	3.5-2	7.1-2.5	11-3	14.9 -3.6
Max mP power [W]	90	106	130	160	171	177	186
Bat. power [W]	1.4	1.7	2.0	2.4	2.1	2.3	2.5

Node years: 2007/65nm, 2010/45nm, 2013/33nm, 2016/23nm

Technology Scaling Models

- ***Full scaling(constant electrical)***
  - Ideal model –dimensions and voltage scale together by the same factor S
- ***Fixed voltage scaling***
  - Most common model until recently- only dimensions scale, voltages remain constant
- ***General scaling***
  - Most realistic for today's situation-voltages and dimensions scale with different factors

Scaling Relationships for Long Channel Devices

Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
W, L, t_{ox}		1/S	1/S	1/S
V_{DD}, V_T		1/S	1/U	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_L	$C_{ox}WL$	1/S	1/S	1/S
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{av}	$k_{n,p} V^2$	1/S	S/U^2	S
t_p (intrinsic)	$C_L V / I_{av}$	1/S	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S
PDP	$C_L V^2$	$1/S^3$	$1/SU^2$	1/S

Difference between long and short channels

$$I_{Dsat} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$I_D\Big|_{V_{DS}=V_{DSAT}} = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

$$= v_{sat} C_{ox} W (V_{GT} - \frac{V_{DSAT}}{2})$$

Transistor Scaling (velocity-saturated devices)

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
√ *Area*/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	$1/S$	$1/U$	1
Current Density	$I_{sat}/Area$	S	S^2/U	S^2
Ron	V/I_{sat}	1	1	1
√ *Intrinsic Delay*	$R_{on}C_{gate}$	$1/S$	$1/S$	$1/S$
√ P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	$P/Area$	1	S^2/U^2	S^2

summary

- CMOS at a glance
- CMOS static behavior
  - VTC, noise margin, threshold voltage
- CMOS dynamic behavior
  - Capacitance mosaic, delay
  - Ratio pMOS/nMOS:3.5,2.4,1.6
  - Optimizing inverter sizing
- Power
  - Power mosaic
  - Optimizing dynamic power
  - Short power consideration