Digital Integrated Circuits

Lab 1: Device Simulations

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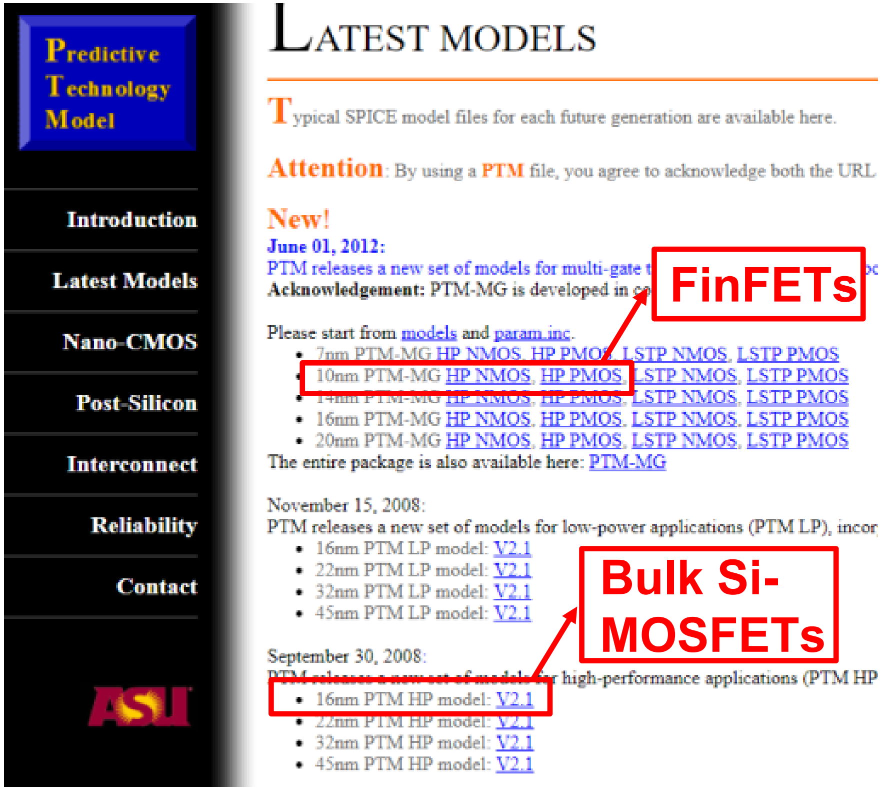
Outline

- Lab Contents
- Report Requirements

Models for DC Simulation

- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 16nm bulk Si-MOSFETs and 10nm multi-gate (MG) FinFETs
  - PTM link: http://ptm.asu.edu/
  - Use the high-performance (HP) models
  - For both n-channel and p-channel devices



Simulation Settings

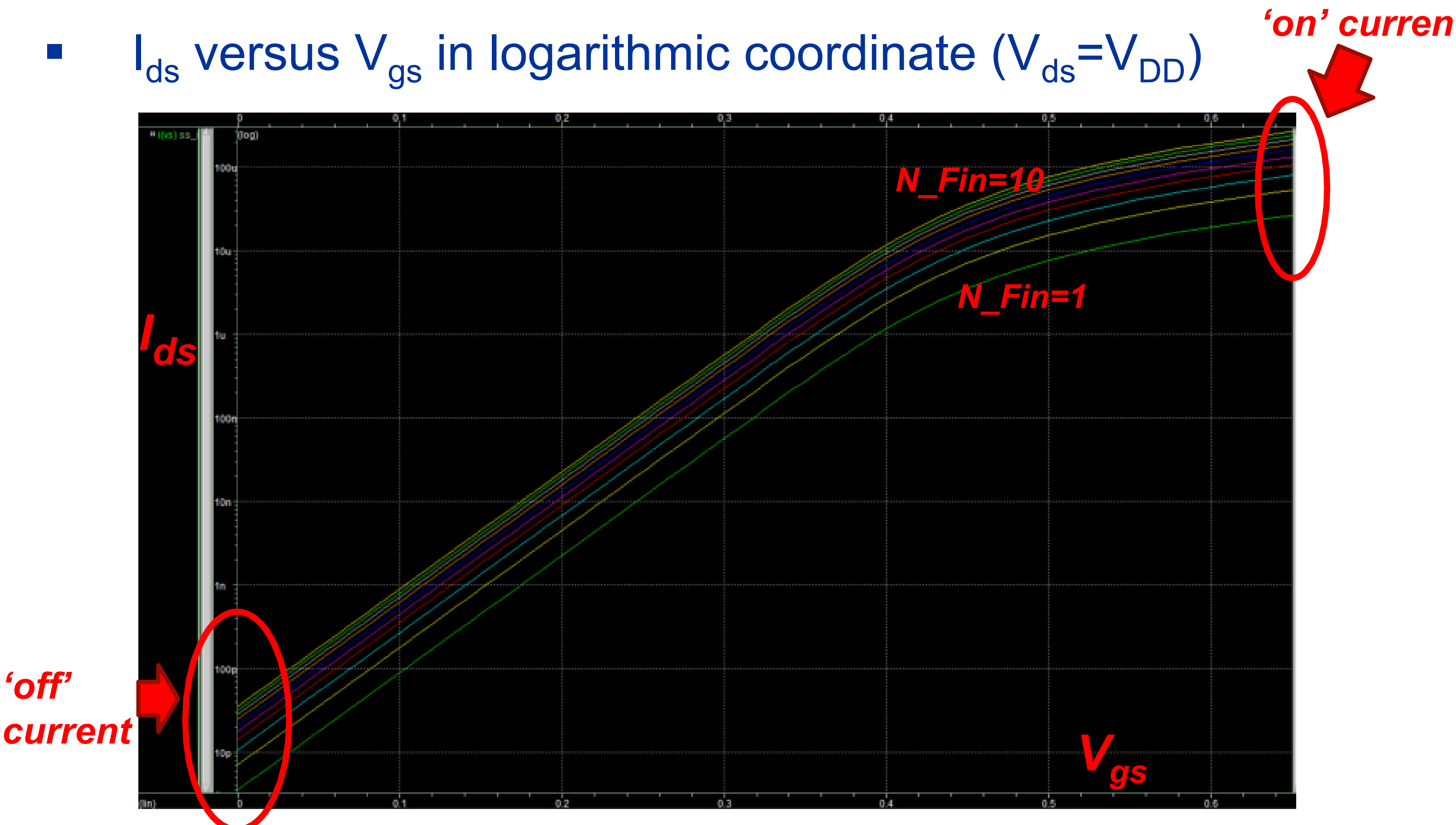
- L_g = 14nm for FinFETs while L_g = 16nm for bulk Si-MOSFETs
- Supply voltage (V_{DD}) is 0.65V for 10nm FinFETs and 0.7V for 16nm bulk Si-MOSFETs
- Simulation temperature
  - T = 25˚C
  - T = 90˚C

Task 1: Plot I-V Curves

- For bulk Si-MOSFETs and FinFETs
  - Plot I_{ds}-V_{ds} (@$V_{gs} = V_{DD}$) curves
  - Plot I_{ds}-V_{gs} (@$V_{ds} = V_{DD}$) curves
    - For both n-channel and p-channel devices
    - FinFETs: fin number is increased from 1 to 10 with a step of 1
    - Bulk Si-MOSFETs: width is increased from 3λ to 15λ with a step of 3λ

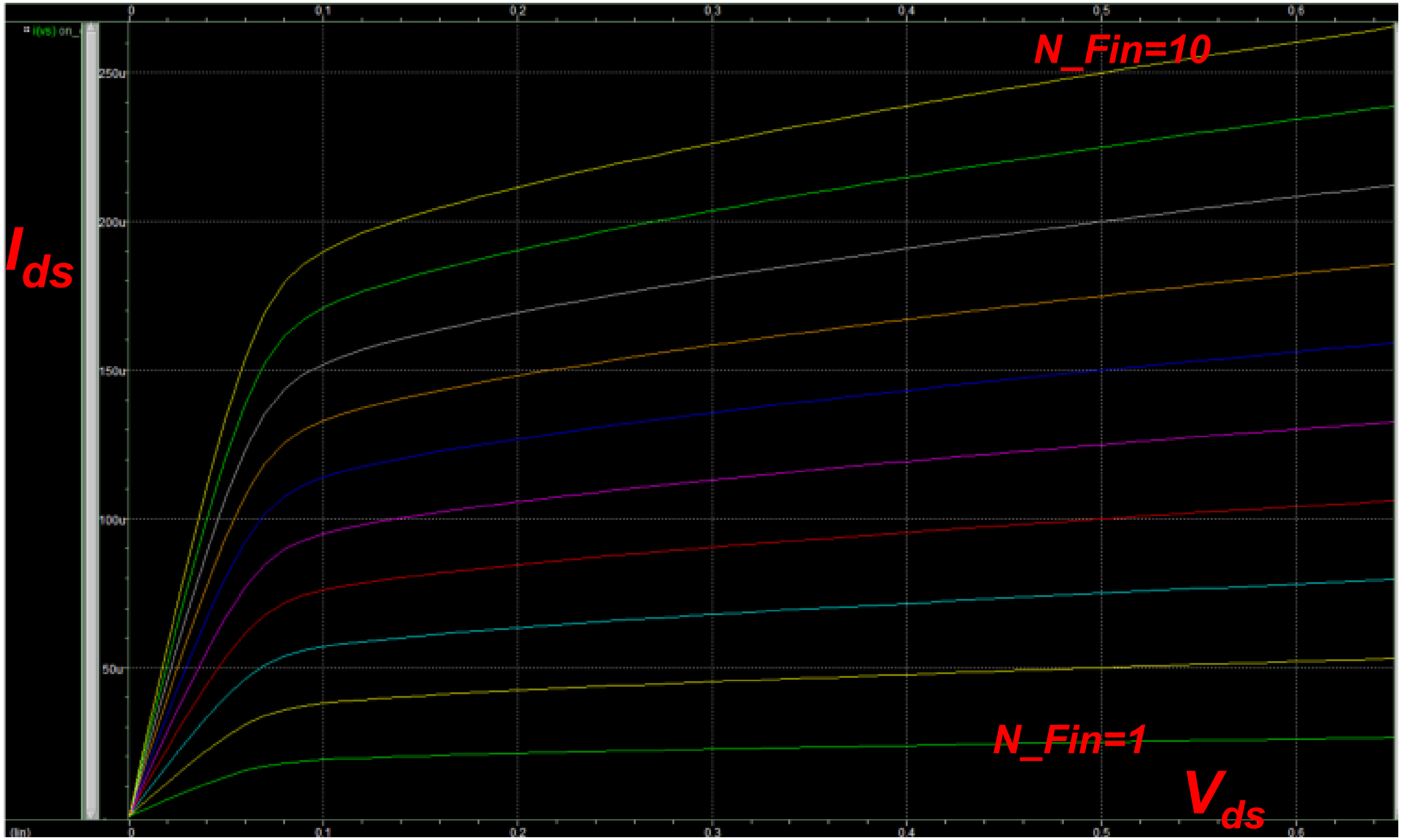
I_{ds}-V_{gs} Curve of N-Channel FinFETs

- I_{ds} versus V_{gs} in logarithmic coordinate (V_{ds}=V_{DD})



I_{ds}-V_{ds} Curve of N-Channel FinFETs

- I_{ds} versus V_{ds} in linear coordinate ($V_{gs} = V_{DD}$)



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Task 2: Metrics to be Measured

- On-state current (I_{on})
- Off-state current (I_{off})
- On-state to off-state current ratio (I_{on}/I_{off})
- Equivalent resistance (R_{on}&R_{off})
- Subthreshold Swing (SS)

Measurement Methods — I_{on} & I_{off}

- Take the n-channel device as an example
  - The on-state current (I_{on}) is measured when
    - $V_{gs} = V_{DD}$
    - $V_{ds} = V_{DD}$
  - The off-state current (I_{off}) is measured when
    - $V_{gs} = 0$
    - $V_{ds} = V_{DD}$

Measurement Methods — Ron & Roff

- Take the n-channel device as an example
  - R_{on} : According to Fig. 1, set Vg = V_{DD}, conduct simulation and get the curve shown in Fig. 2. Then use equation (1) to estimate Roff value.
  - R_{off} : Set Vg=0V and repeat the above process.

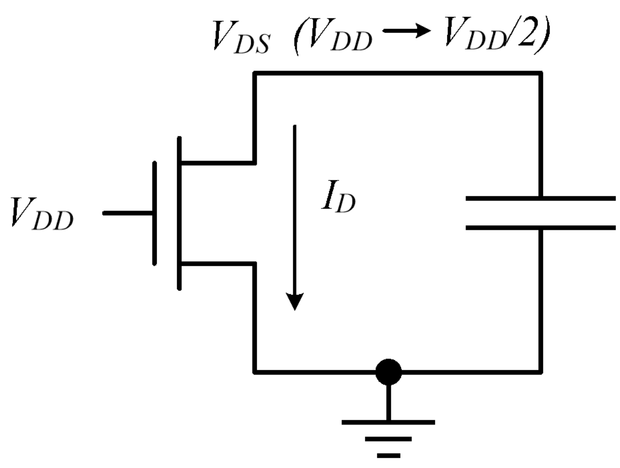


Fig. 1

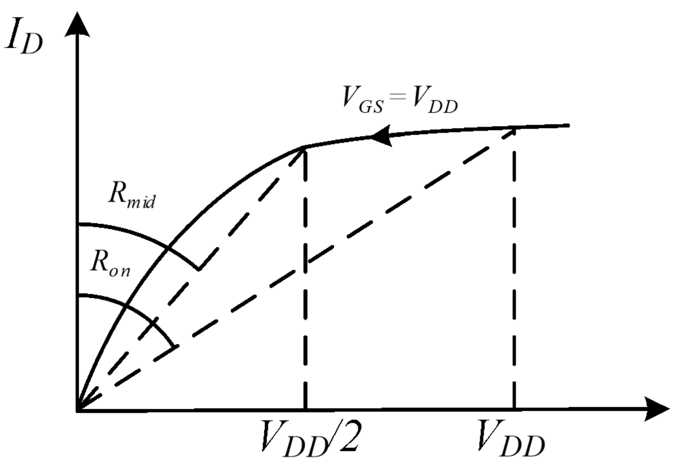


Fig. 2

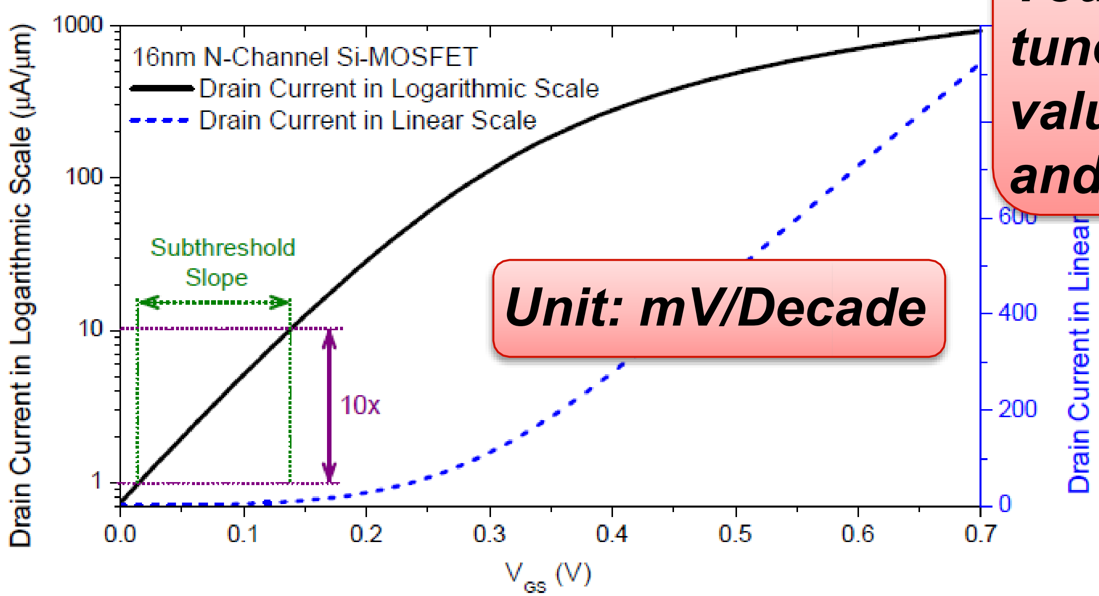
$$R_{eq} = average_{t=t_1 \ldots t_2}(R_{on}(t)) = \frac{1}{t_2-t_1}\int_{t_1}^{t_2} R_{on}(t)dt = \frac{1}{t_2-t_1}\int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}dt \approx \frac{1}{2}(R_{on}(t_1)+R_{on}(t_2)) \quad (1)$$

N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison-Wesley, 2010.

Measurement Methods — Subthrehold Slope (SS)

- According to the definition, you can use the following way
  - Find the V_{gs} when I_{ds} = $\boxed{0.1\ uA}$ × (W/L) ,denoted by V_1
  - Find the V_{gs} when I_{ds}= $\boxed{0.01\ uA}$ × (W/L) ,denoted by V_2
  - The subthreshold slope (SS) = V_1-V_2

You may need to tune the current values to get V1 and V2



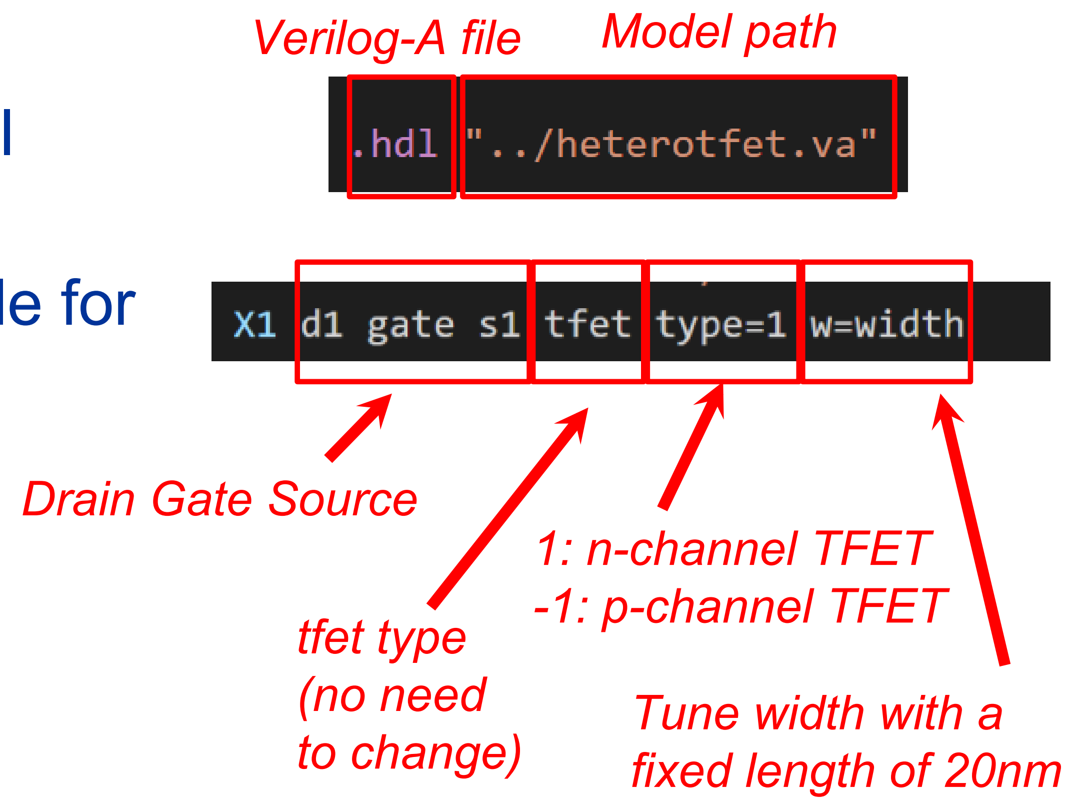
Unit: mV/Decade

Task 3 (optional): TFET

- I-V Curve
- On-state current (Ion)
- Off-state current (Ioff)
- On-state to off-state current ratio (Ion/Ioff)
- Equivalent resistance (Ron & Roff)
- Subthreshold Swing (SS)

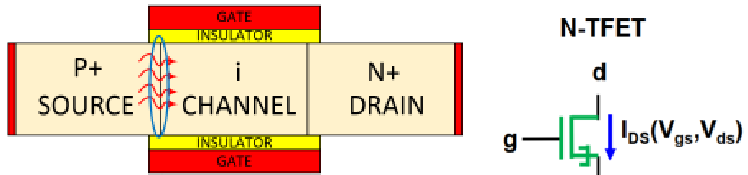
Models for TFET

- Use the Penn State III-V Tunnel FET Model Manual Version 1.0.1 for task 3 (optional).
  - Download the from models and manual from Canvas
  - Models are available for both n-channel and p-channel devices

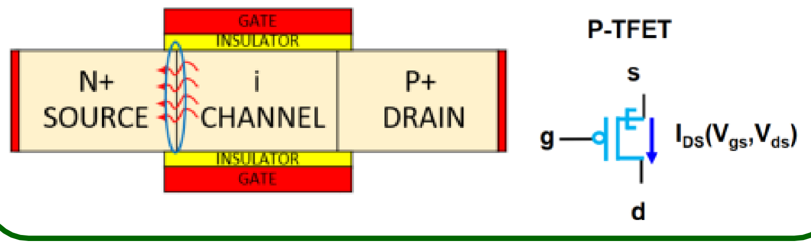


Simulation Settings for TFET

- L_g is fixed at 20nm for both n-channel and p-channel TFETs while W_g is changed from 3λ to 15λ with a step of 3λ
- Supply voltage (V_{DD}) is 0.3V for 20nm TFETs
- Simulation temperature
  - T = 25˚C



band-to-band tunneling is enabled at the source-channel junction

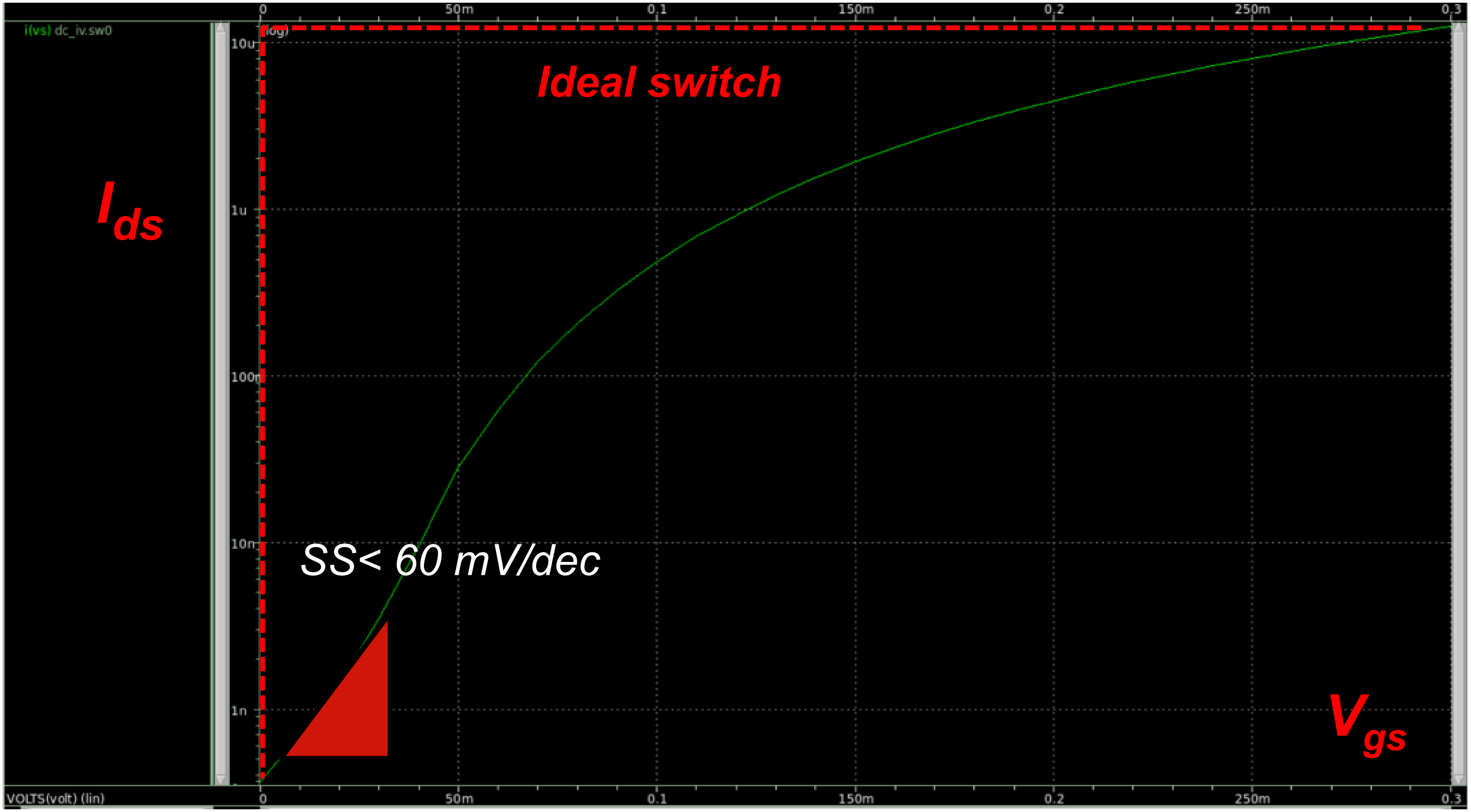


I_{ds}-V_{ds} Curve of N-Channel TFETs

- I_{ds} versus V_{ds} in linear coordinate (V_{gs} sweep from 0 to V_{DD})

I_{ds}-V_{gs} Curve of N-Channel TFETs

- I_{ds} versus V_{gs} in logarithmic coordinate (V_{ds}=V_{DD})



Outline

- Lab Contents
- Report Requirements

Report Requirement

- Write your lab report like writing a technical document (readable, comprehensive analysis, no typo…)
- You may include
  - Introduction/background
  - Lab procedures
  - Lab results
    - Widths/lengths of transistors, I-V curves, result tables of metrics…
  - Technical analysis of the simulation results
  - Observations and conclusions
    - You can also add some comments on how this lab can be helpful to your understanding of the class material

Submission

- You need to submit your report and code
  - Name of report (in PDF format):
    lab1_report_[Name]_[Student No.].pdf
  - Name of code (compressing the files):
    lab1_code__[Name]_[Student No.].zip

- Please upload your report to Canvas course website

- Submission of lab1 report and code will be due on **13th October 2021**

Q & A

- If you have any technical problem, you may contact TA through

  TA: 汪登峰

  E-mail: yungsk@sjtu.edu.cn

  Lab: Rm 208, Building of Microelectronics