CMOS VLSI Design

2.CMOS Transistor Theory

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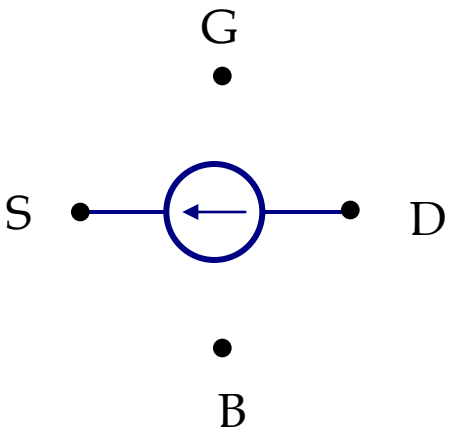
outline

- Ideal I-V characteristics under static conditions
- Velocity Saturation
- **Dynamic Characteristics**
- Nonideal I-V effects

A unified model for manual analysis



$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

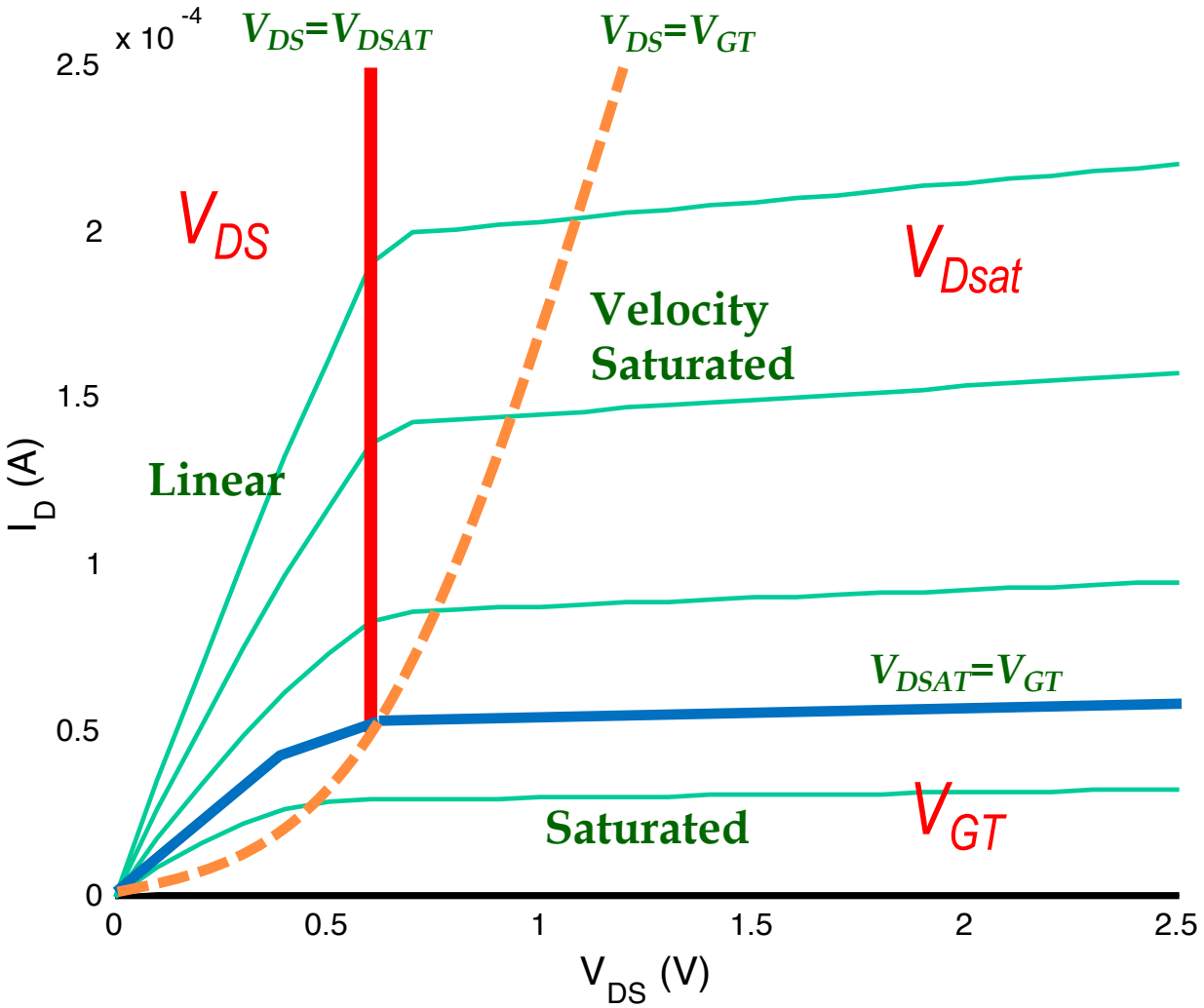
and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

$$\beta = k' \frac{W}{L}$$

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

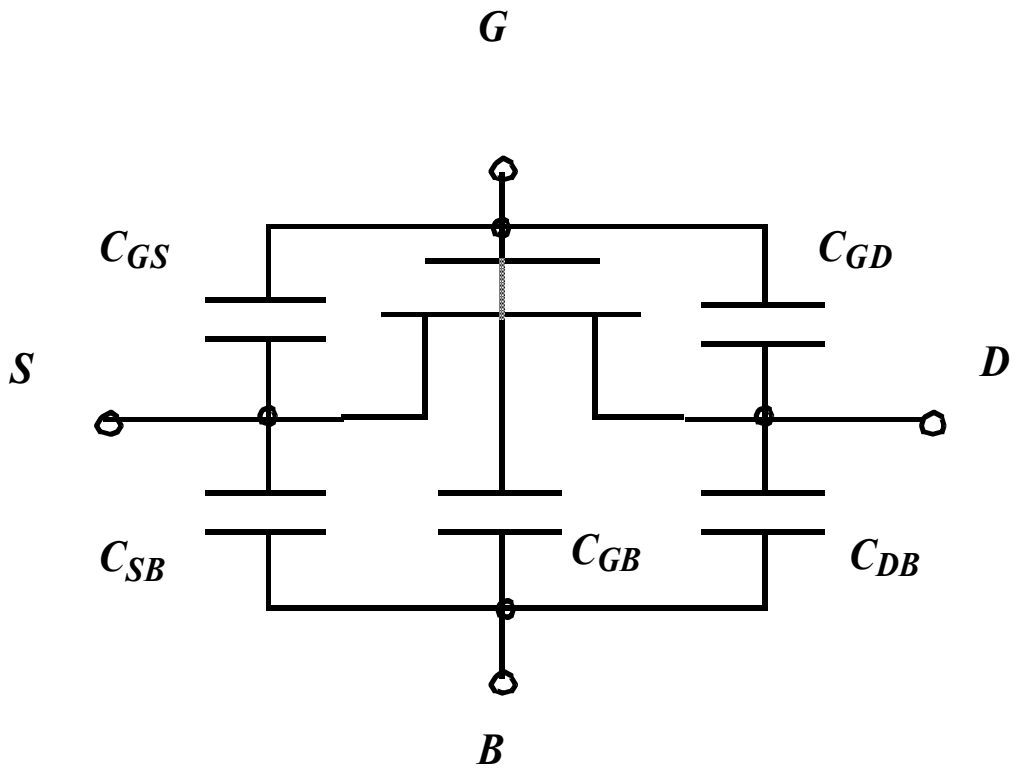
	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	115X10-8	0.06
PMOS	-0.4	-0.4	-1	-30X10-6	-0.1

Simple Model versus SPICE

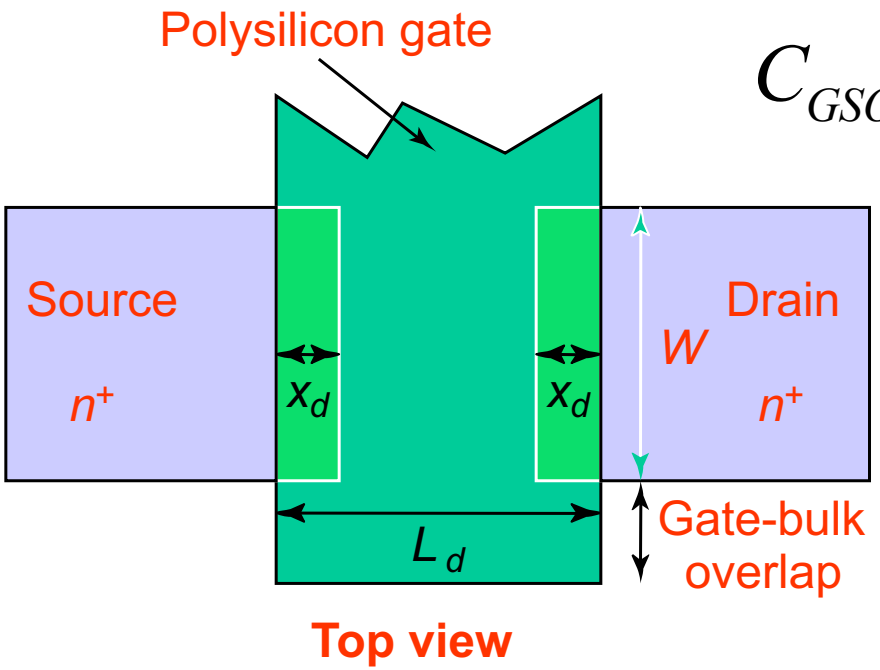


Capacitance model

$$C_{GS} = C_{GSO} + C_{GCS}$$
$$C_{GD} = C_{GDO} + C_{GCD}$$
$$C_{GB} = C_{GCB}$$
$$C_{SB} = C_{Sdiff}$$
$$C_{DB} = C_{Ddiff}$$



The Gate Capacitance



$$C_{GSO} = C_{GDO} = C_{ox} x_d W = C_o W$$

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

Gate channel Capacitance

TABLE 2.1 Approximation for intrinsic MOS gate capacitance

Parameter	Cutoff	Linear	Saturation
C_{gb}	$\leq C_0$	0	0
C_{gs}	0	$C_0/2$	$2/3\ C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gs} + C_{gd} + C_{gb}$	C_0	C_0	$2/3\ C_0$

$$C_0 = WLC_{ox}$$

$$C_g = C_{gs} + C_{gd} + C_{gb} \approx C_0 + 2C_{gol}W$$

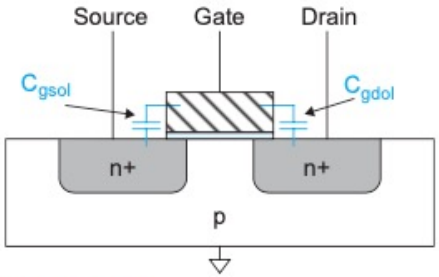


FIGURE 2.10 Overlap capacitance

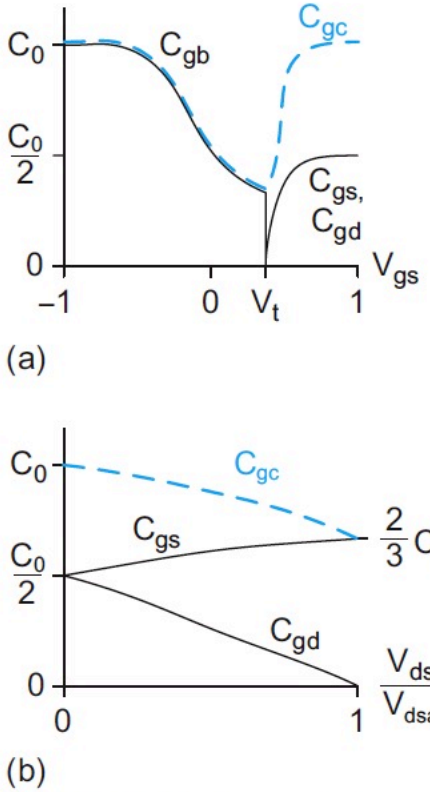


FIGURE 2.9 Intrinsic gate capacitance $C_{gc} = C_{gs} + C_{gd} + C_{gb}$ as a function of (a) V_{gs} and (b) V_{ds}

Most important regions in digital design: saturation and cut-off

Detail Diffusion Capacitance

$$C_{sb}=AS_sC_{jbs}+PS_sC_{jbssw}$$

面积电容+周长电容

$$C_{jbs} = C_J\left(1+\frac{V_{sb}}{\psi_0}\right)^{-M_J}$$

$$\psi_0 = \frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right) = 0.026\ln\left(\frac{N_D N_A}{n_i^2}\right)$$

$$C_{jbssw} = C_{JSW}\left(1+\frac{V_{sb}}{\psi_0}\right)^{-M_{JSW}}$$

$$C_{jbsswg} = C_{JSW}\left(1+\frac{V_{sb}}{\psi_0}\right)^{-M_{JSWG}}$$

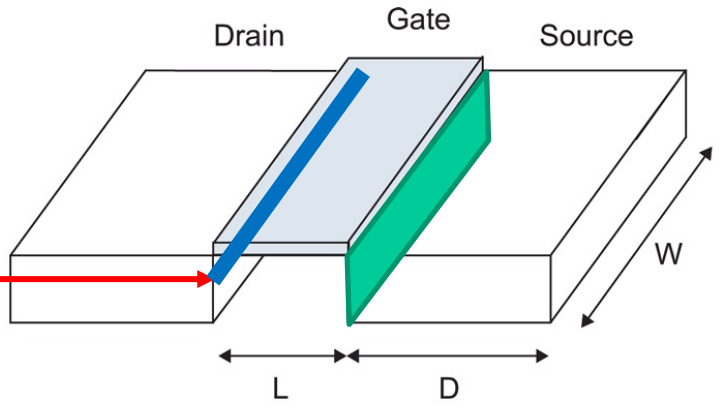


FIG 2.13 Diffusion region geometry

Example 2.2

Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted nMOS transistor in a 65nm process when the drain is at 0V and again at V_{DD}=1.0V. Assume the substrate is grounded. The diffusion region conforms to the design rules with λ=25nm. The transistor characteristics are C_J=1.2fF/μm^2, M_J=0.33,C_{JSW}=0.1fF/μm, C_{JSWG}=0.36 fF/μm, M_{JSW}=M_{JSWG}=0.10, and ψ_0=0.7V at room temperature.

SOLUTION: From Figure 2.8, we find a unit-size diffusion contact is $4 \times 5\ \lambda$, or $0.1 \times 0.125\ \mu$m. The area is 0.0125 μm^2 and perimeter is 0.35 μm plus 0.1 μm along the channel. At zero bias, $C_{jbd} = 1.2$ fF/μm^2, $C_{jbdsw} = 0.1$ fF/μm, and $C_{jbdswg} = 0.36$ fF/μm. Hence, the total capacitance is

AS PS1 PS2

$$C_{db}(0\text{ V}) = (0.0125\mu\text{m}^2)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right) + (0.35\mu\text{m})\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + (0.1\mu\text{m})\left(0.36\frac{\text{fF}}{\mu\text{m}}\right) = 0.086\text{ fF} \quad (2.21)$$

At a drain voltage of V_{DD}, the capacitance reduces to

$$C_{db}(1\text{ V}) = (0.0125\mu\text{m}^2)\left(1.2\frac{\text{fF}}{\mu\text{m}^2}\right)\left(1+\frac{1.0}{0.7}\right)^{-0.33} + \left[(0.35\mu\text{m})\left(0.1\frac{\text{fF}}{\mu\text{m}}\right) + (0.1\mu\text{m})\left(0.36\frac{\text{fF}}{\mu\text{m}}\right)\right]\left(1+\frac{1.0}{0.7}\right)^{-0.10} = 0.076\text{ fF} \quad (2.22)$$

An example of Diffusion Capacitance

NMOS:t_{ox}=6nm,L=0.24um,W=0.36um,L_D=L_S=0.625um, C_{OX}=5.7X10^{-3}F/m^2, C_O=3X10^{-10}F/m,C_{j0}=2X10^{-3}F/m^2, and C_{jsw0}=2.75X10^{-10}F/m, determine the zero-bias value of relevant capacitances

- $C_{gc}=WLC_{ox}=0.24*0.36*5.7=0.49fF$
- $C_{overlap}=2*C_o*W=2*0.3*0.36=0.216fF$
- $C_{diff\text{-}s}=WD_s*C_j+(2W+2D_s)C_{jsw}=$

$0.36*0.625*2+(0.36*2+0.625*2)*0.275=0.539fF$

1F=10^{15}fF

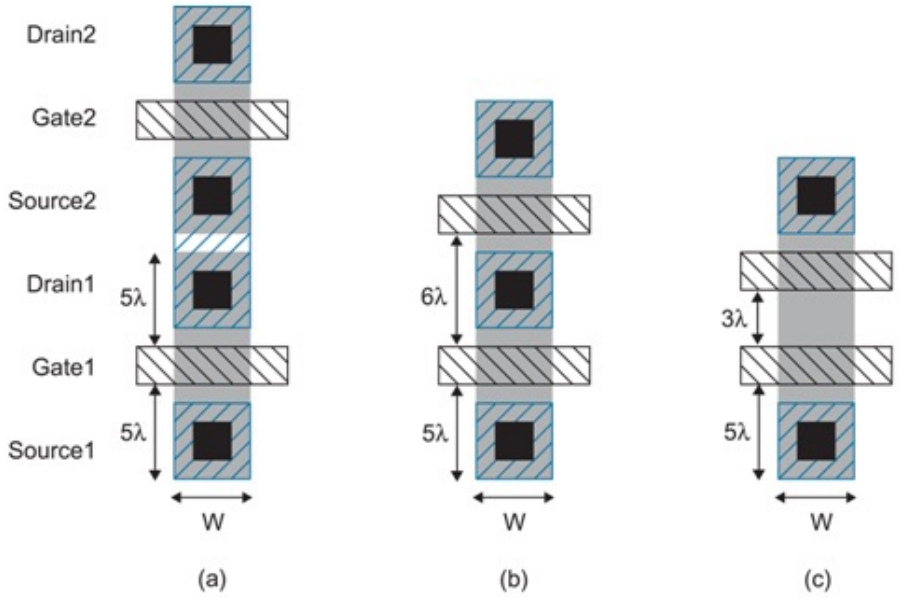
	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

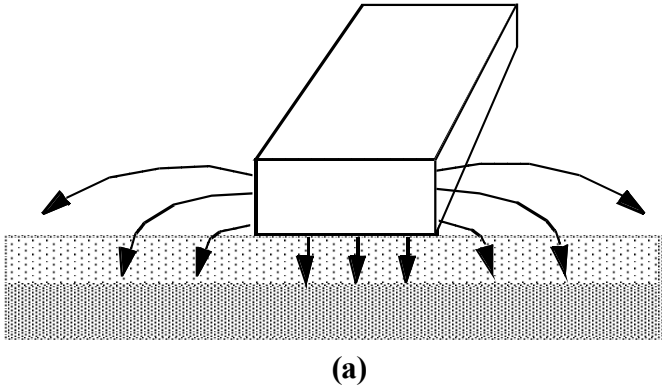
Diffusion Capacitance

- C_{sb}, C_{db}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_g for contacted diff
  - ½ C_g for uncontacted
  - Varies with process



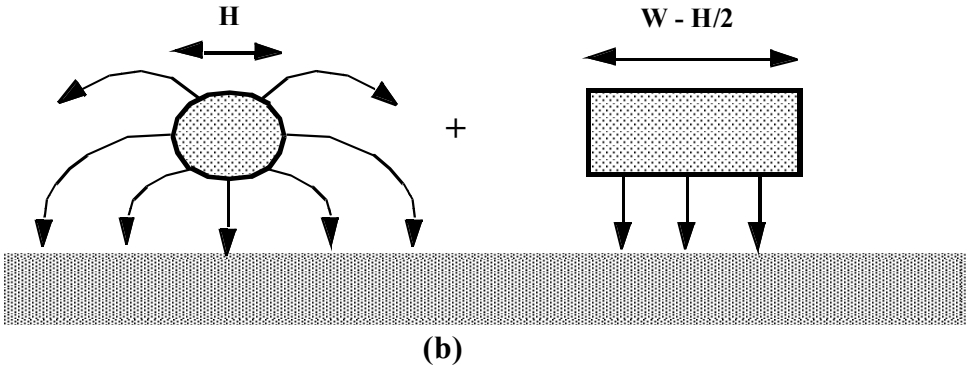
Fringing Capacitance

Over the years, a steady reduction in the W/H ratio which has even dropped below 1



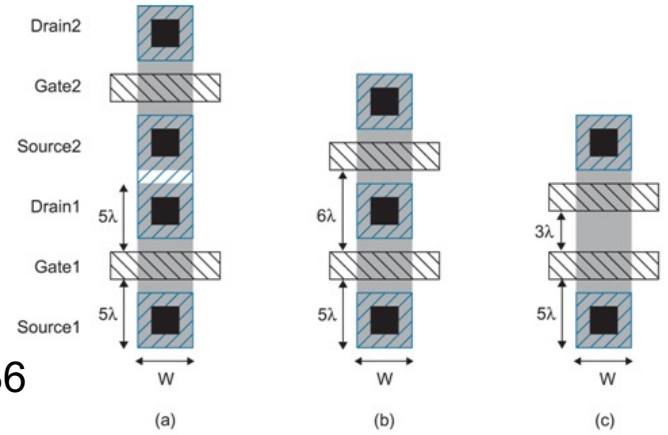
Perimeter?

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$



Another example

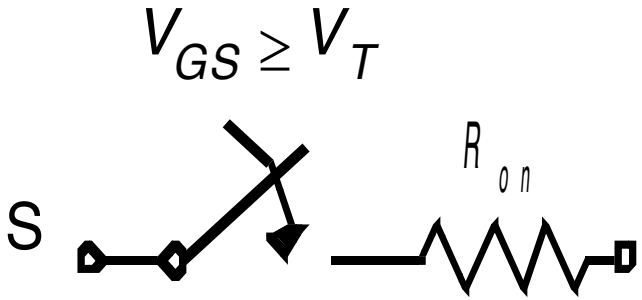
Calculate the diffusion parasitic C_{db} of the drain of a unit-sized contacted nMOS transistor in a 0.18um process when the drain is at 0 and at V_{dd}=1.8V, assume the substrate is grounded, the transistor characteristic are C_j=0.98fF/um^2,M_j=0.36, C_{JSW}=0.22fF/um,M_{JSW}=0.10, and ϕ_0=0.75V at room temperature

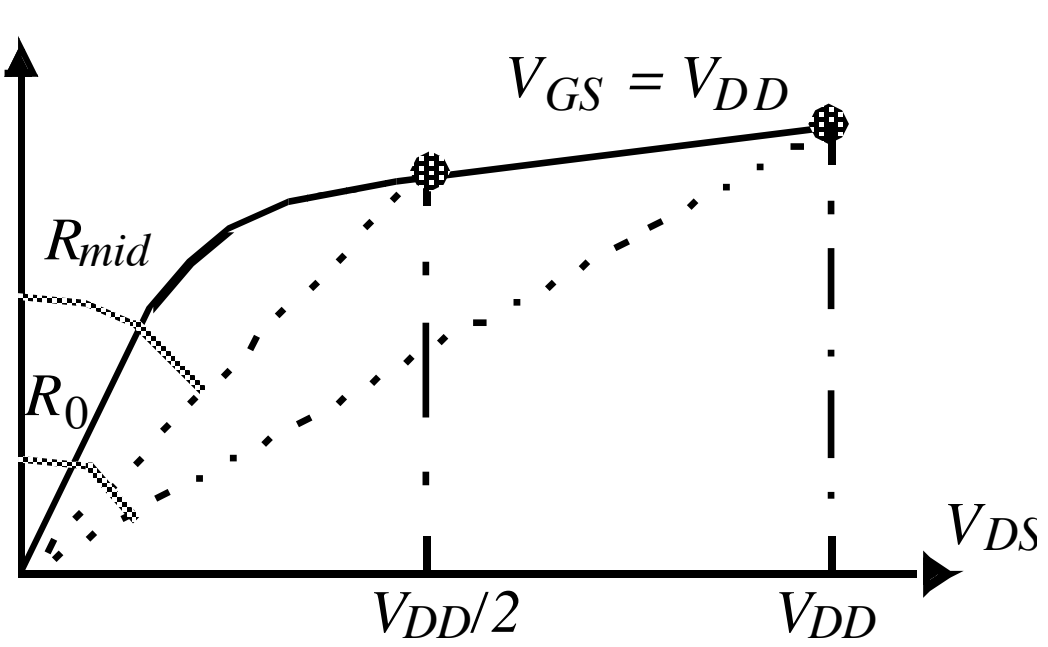


- AD=20unit^2=20*0.081=0.162um^2
- PD=10+4=14unit=14*0.09=1.26um
- C_{db}(0)=0.162*0.98+1.26*0.22=**0.43**
- C_{db}(1.8)=0.162*0.98*(1+1.8/0.75)$^{-0.36}$

+1.26*0.22*(1+1.8/0.75)$^{-0.10}$=0.1022+0.2788=**0.381**

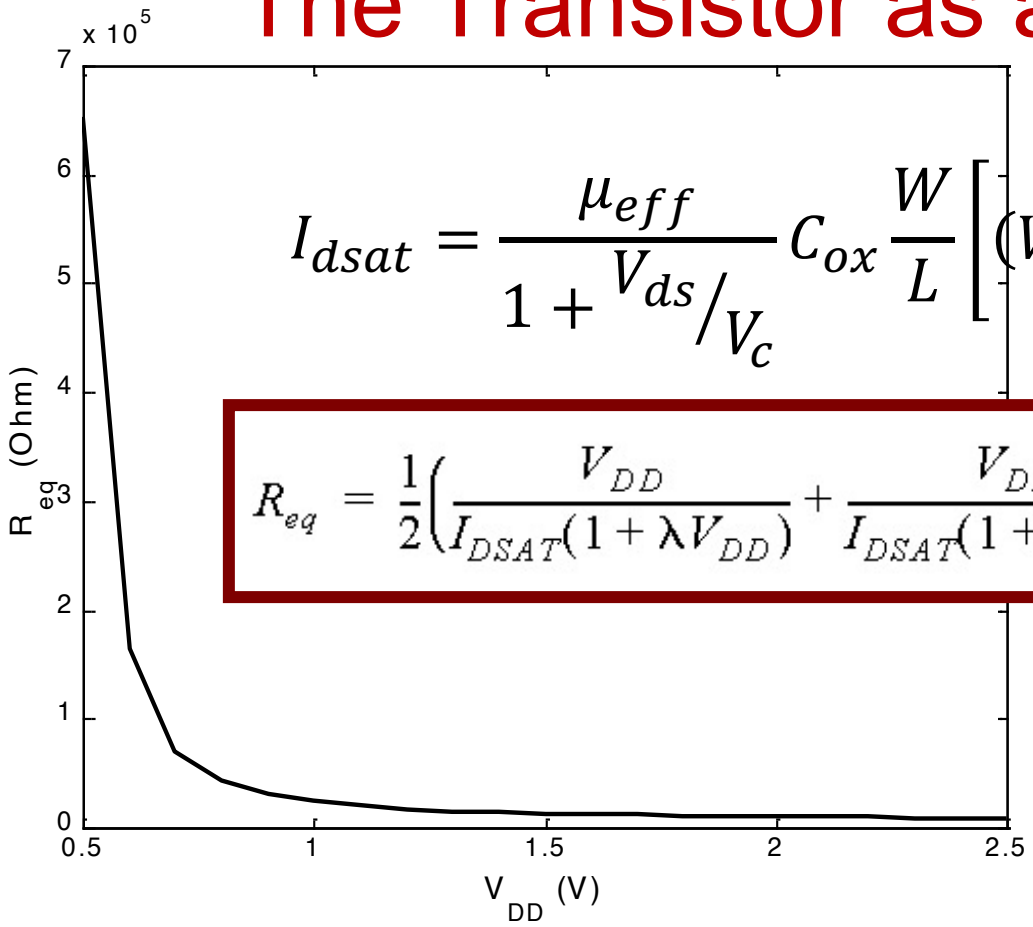
The Transistor as a Switch





$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

The Transistor as a Switch



$$I_{dsat} = \frac{\mu_{eff}}{1 + {V_{ds}}/{V_c}} C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right]$$

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

跨导g就是R的倒数

$$R_{eq} = \frac{3}{4}\frac{V_{dd}}{k'\frac{W}{L}\left[(V_{GS} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right]}\left(1 - \frac{5}{6}\lambda V_{dd}\right)$$

outline

- PN junction principle
- CMOS transistor introduction
- Ideal I-V characteristics under static conditions
- Velocity Saturation
- Dynamic Characteristics
- ***Nonideal I-V effects***

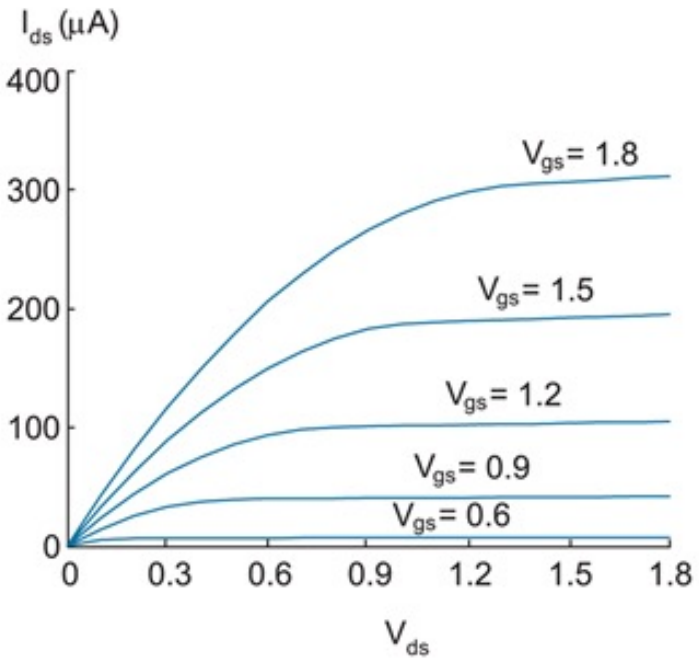
Nonideal characteristics

- *Velocity saturation*
- ***Channel length modulation***
- *Body effect*
- *Threshold Variations*
- *Parasitic Resistances*
- *Subthreshold Conduction*
- *Hot-carrier effects*
- *Latchup*
- *Process variations*

Channel length modulation

- Increasing V_{DS} decreases the effective channel length
- Λ is an empirical channel length, should not be confuse with the symbol used in layout design rules

$$I_D = I_D^{'}(1+\lambda V_{DS})$$



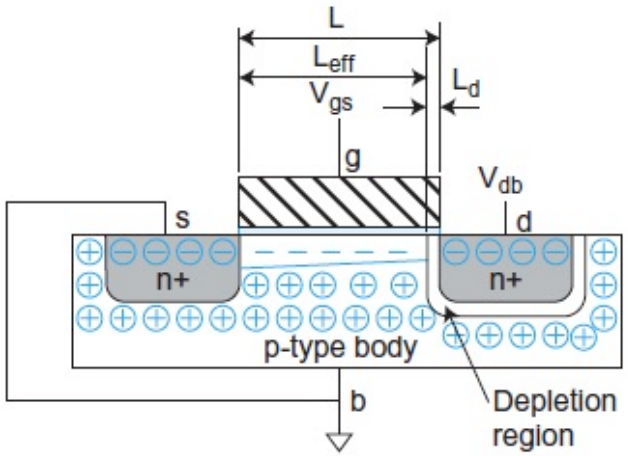


FIGURE 2.18 Depletion region shortens effective channel length

Nonideal characteristics

- *Velocity saturation*
- *Channel length modulation*
- ***Body effect***
- *Threshold Variations*
- *Parasitic Resistances*
- *Subthreshold Conduction*
- *Hot-carrier effects*
- *Latchup*
- *Process variations*

Body effect

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) \qquad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon N_A} = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}$$

$$\phi_S = \left|\frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right)\right| = \left|0.052 ln\left(\frac{N_A}{n_i}\right)\right|$$

nominal threshold voltage of 0.4V and doping level of $8*10^{17}cm^{-3}$,t_{ox}=4nm, the body is tied to ground with a substrate contact. how much does the threshold change at room temperature if the source is at 1.1V instead of 0,note, n_i= $1.45*10^{10}cm^{-3}$, $\varepsilon_0=8.85*10^{-14}$, $\varepsilon=11.7\varepsilon_0$, $\varepsilon_{ox}=3.9\varepsilon_0$, $q=1.6*10^{-10}C$

$$\gamma = \frac{40 * 10^{-8}}{3.9 * 8.85 * 10^{-14}}\sqrt{2 * (1.6 * 10^{-19}) * (11.7 * 8.85 * 10^{-14} * 8 * 10^{17}} = 0.6$$

$$V_t = 0.4 + 0.6 * (\sqrt{|0.92 + 1.1|} - \sqrt{|0.92|}) = 0.68$$

Body effect

Reverse bias voltage

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) \qquad \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon N_A} = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}$$

$$\phi_S = \left|\frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right)\right| = \left|0.052 ln\left(\frac{N_A}{n_i}\right)\right|$$

$$V_t = V_{t0} + k_\gamma V_{sb}$$

$$\phi_s = 2(0.026\ \text{V})\ln\frac{8\times10^{17}\ \text{cm}^{-3}}{1.45\times10^{10}\ \text{cm}^{-3}} = 0.93\ \text{V}$$

$$\gamma = \frac{10.5\times10^{-8}\ \text{cm}}{3.9\times8.85\times10^{-14}\ \frac{\text{F}}{\text{cm}}}\sqrt{2(1.6\times10^{-19}\ \text{C})(11.7\times8.85\times10^{-14}\ \frac{\text{F}}{\text{cm}})(8\times10^{17}\ \text{cm}^{-3})} = 0.16 \qquad (2.40)$$

$$V_t = 0.3 + \gamma\left(\sqrt{\phi_s + 0.6\ \text{V}} - \sqrt{\phi_s}\right) = 0.34\ \text{V}$$

Example 2.5

Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?

SOLUTION: At room temperature, the thermal voltage $v_T = kT/q = 26$ mV and $n_i = 1.45 \times 10^{10}$ cm^{-3}. The threshold increases by 0.04 V.

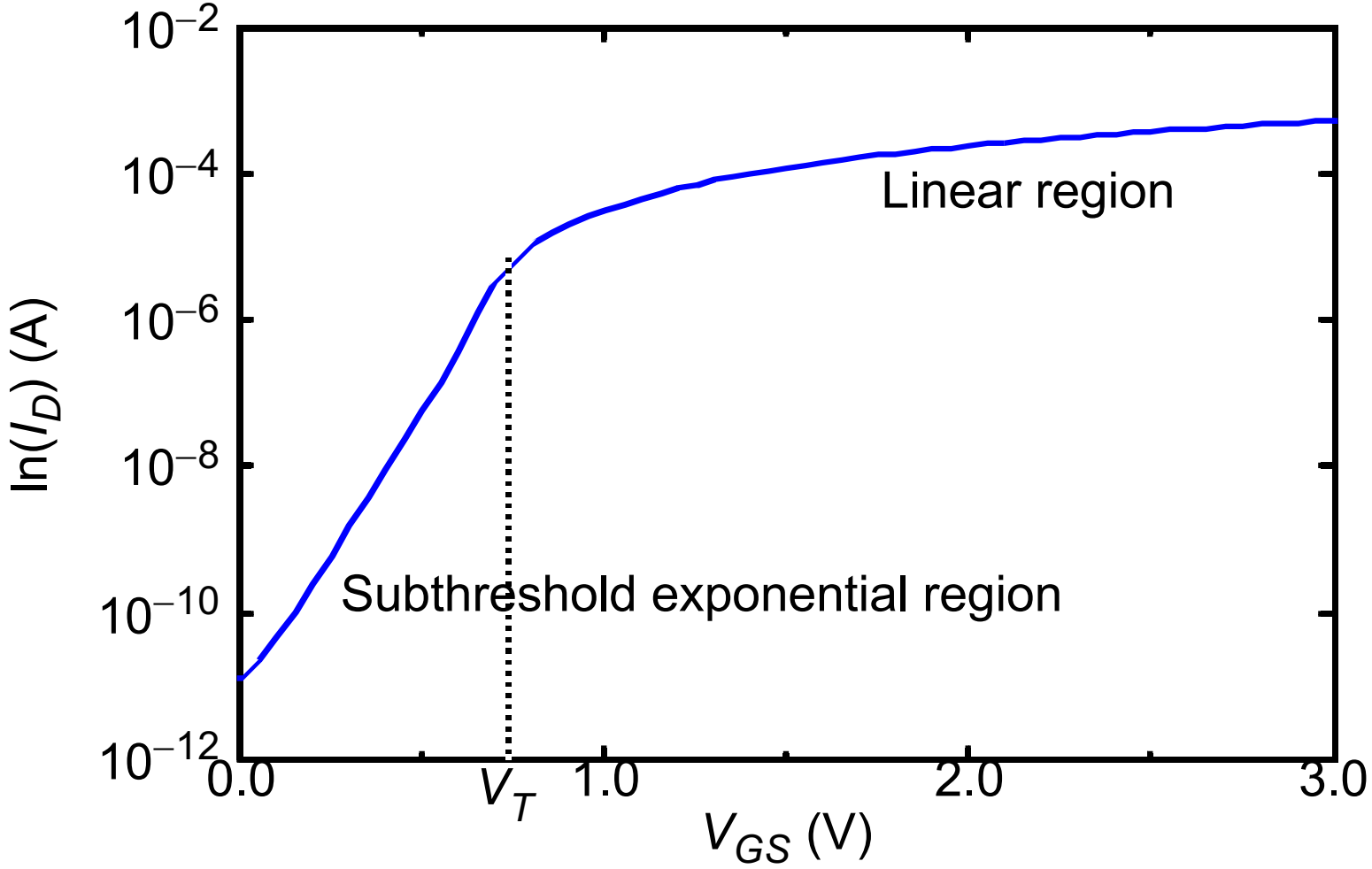
Nonideal characteristics

- *Velocity saturation*
- *Channel length modulation*
- *Body effect*
- ***Threshold Variations***
- *Parasitic Resistances*
- *Subthreshold Conduction*
- *Hot-carrier effects*
- *Latchup*
- *Process variations*

Nonideal characteristics

- Velocity saturation
- Channel length modulation
- Body effect
- Threshold Variations
- Parasitic Resistances
- ***Subthreshold Conduction***
- Hot-carrier effects
- Latchup
- Process variations

Sub-Threshold Conduction



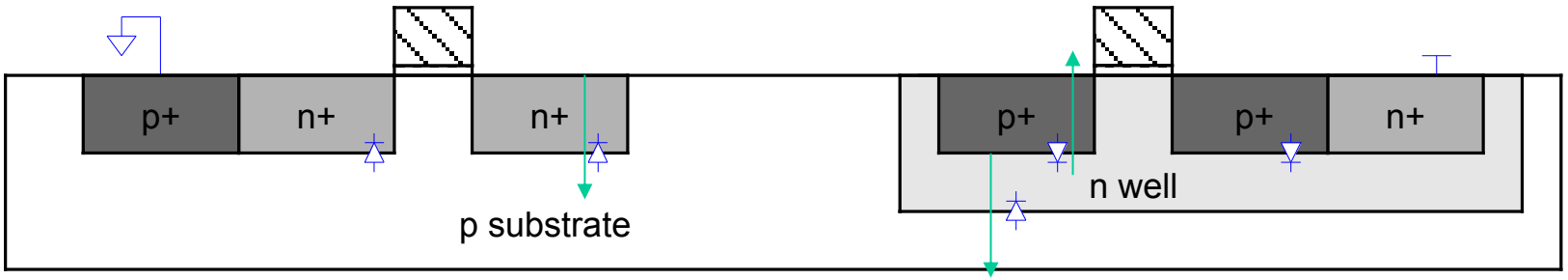
Nonideal characteristics

- *Velocity saturation*
- *Channel length modulation*
- *Body effect*
- *Threshold Variations*
- *Parasitic Resistances*
- *Subthreshold Conduction*
- ***Junction Leakage***
- *Latchup*
- *Process variations*

Junction leakage

- I_s depends on doping levels and on the area and perimeter of the diffusion region
- V_d is the diode voltage(V_{sb} and V_{db})
- Generally in the 0.1-0.01fA/um$_2$

$$I_d = I_s\left(e^{\frac{V_d}{V_T}} - 1\right)$$



Leakage Sources

- Subthreshold conduction
  - Transistors can’ t abruptly turn ON or OFF
- Junction leakage
  - Reverse-biased PN junction diode current
- Gate leakage
  - Tunneling through ultrathin gate dielectric

Subthreshold leakage is the biggest source in modern transistors