Digital Integrated Circuits

Lab 3
Logical Effort

Dr. Yanan Sun

Email: sunyanan@sjtu.edu.cn

Office: Rm 414, Building of Microelectronics

Outline

- Lab Contents
- Report Requirements

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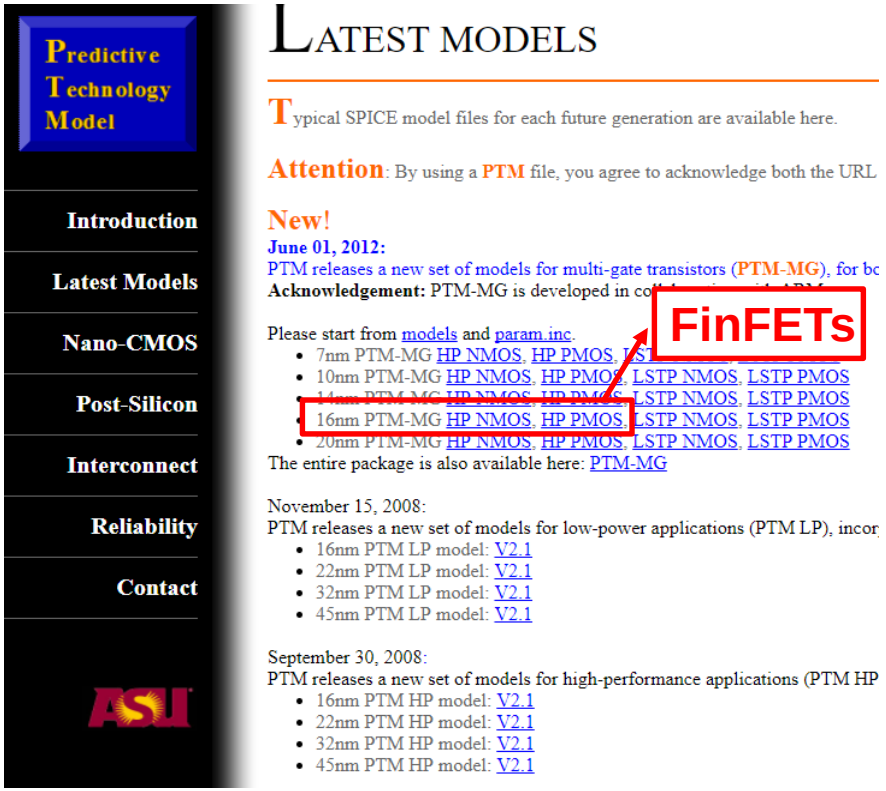
Device Models for Logical Effort Optimizaiton

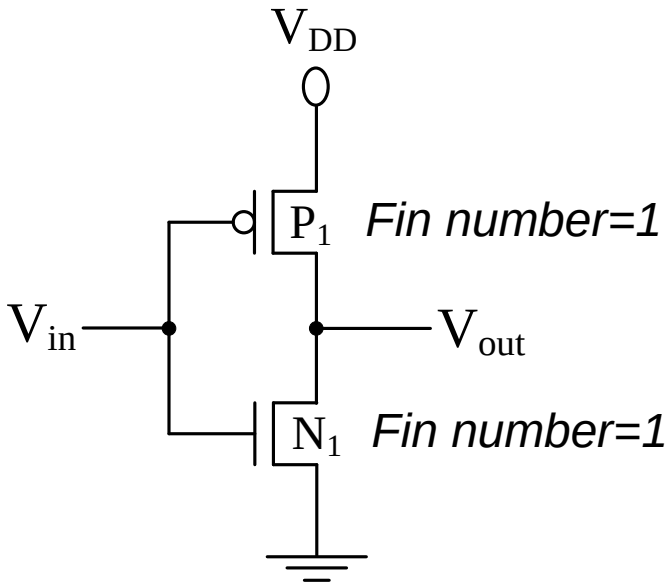
- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 10nm multi-gate (MG) FinFETs
  - PTM link: http://ptm.asu.edu/
  - Use the high-performance (HP) models
  - For both n-channel and p-channel devices



Simulation Settings

- L_g = 14 nm for FinFETs
- Supply voltage is 0.65V for FinFETs
- Simulation temperature
  - T = 25˚C

Minimum sized INV for FinFET



minimum-sized
un-skewed CMOS inverter

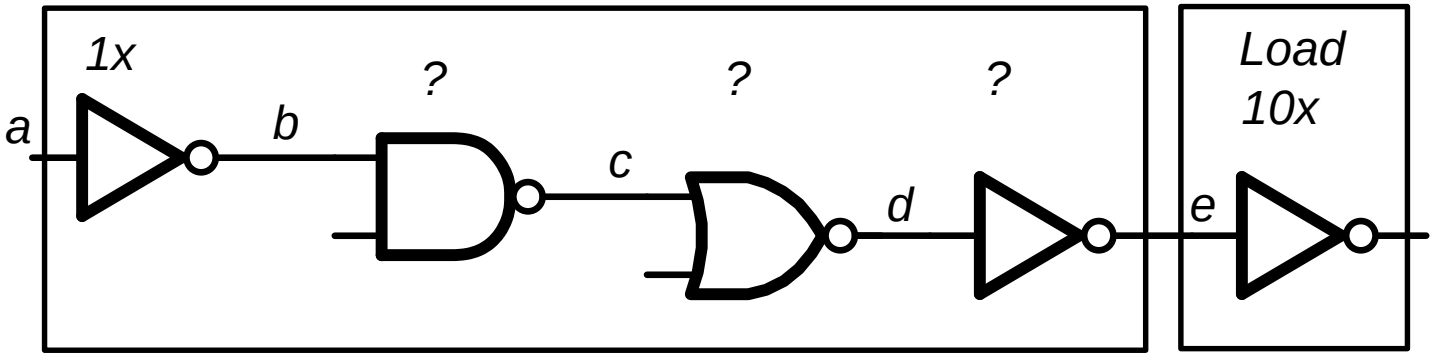
Minimum Sized Inv	PMOS	NMOS
Fin number	1	1
L	14n	14n
Design the fin number to ensure balanced driving current in pull-up and pull-down network		

Task1: Use Logical Effort to Size Gates

- Size each transistor in the circuit below properly to optimize the speed for FinFET, and construct the circuit with HSPICE

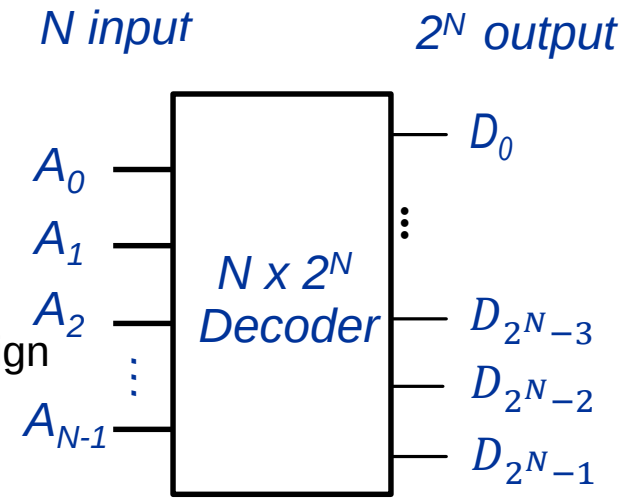
Vpulse	Value
V1	0V
V2	0.65v
Delay Time	1ns
Raise Time	50ps
Fall Time	50ps
Pulse Width	1ns
Period	2ns

Size the logic gates to minimize the propogation delay (a to e)



Task2: Use Logical Effort to Optimize 4x16 Decoder

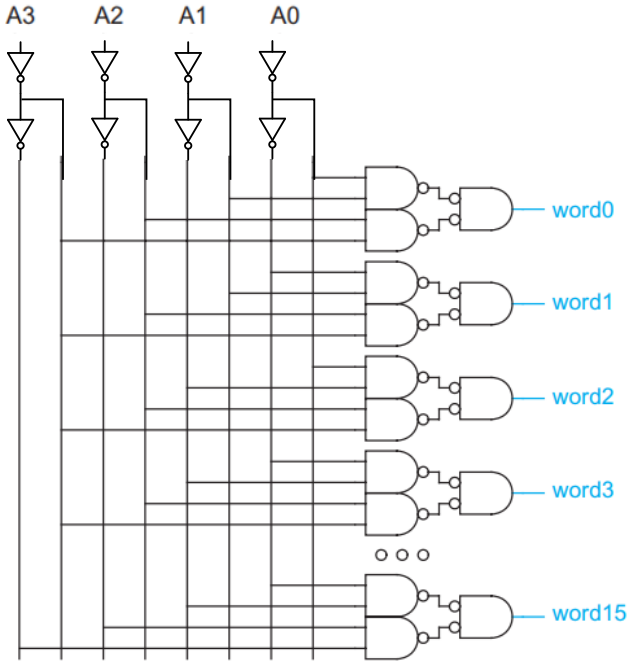
- Backgroud of decoder
  - Logic function: convert N-bit coded input to 2^N unique outputs
  - Can be used as address decoder in memory
    - Address line (input) has large fanout
    - Decoders typically have high electrical effort and branching effort
    - Decoder may have many stages, so the fastest design is the one that minimizes the logical effort



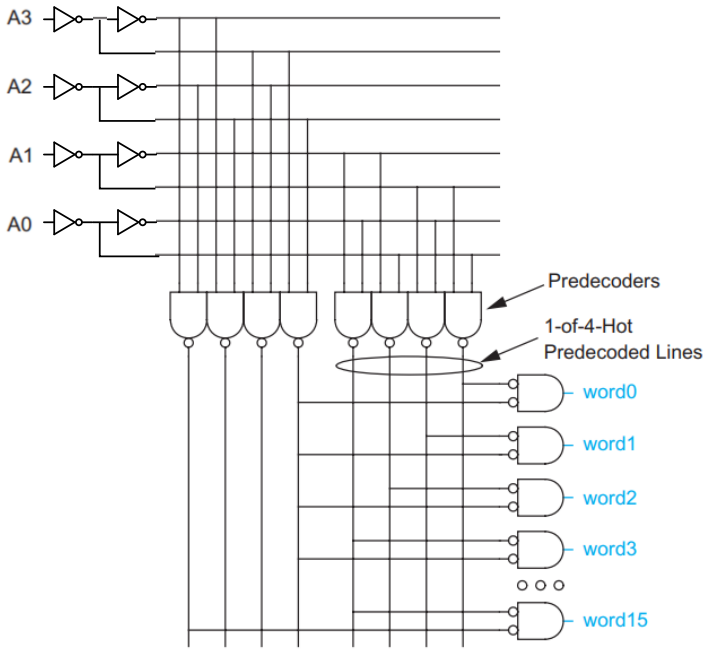
$$D_0 = \overline{A_{N-1}} \ldots \overline{A_3}\ \overline{A_2}\ \overline{A_1}\ \overline{A_0}$$
$$D_1 = \overline{A_{N-1}} \ldots \overline{A_3}\ \overline{A_2}\ \overline{A_1} A_0$$
$$\ldots$$
$$D_{2^N-1} = A_{N-1} \ldots A_3 A_2 A_1 A_0$$

Task2: Use Logical Effort to Optimize 4x16 Decoder

- An example of 4x16 decoder design:



Factoring the common NANDs out



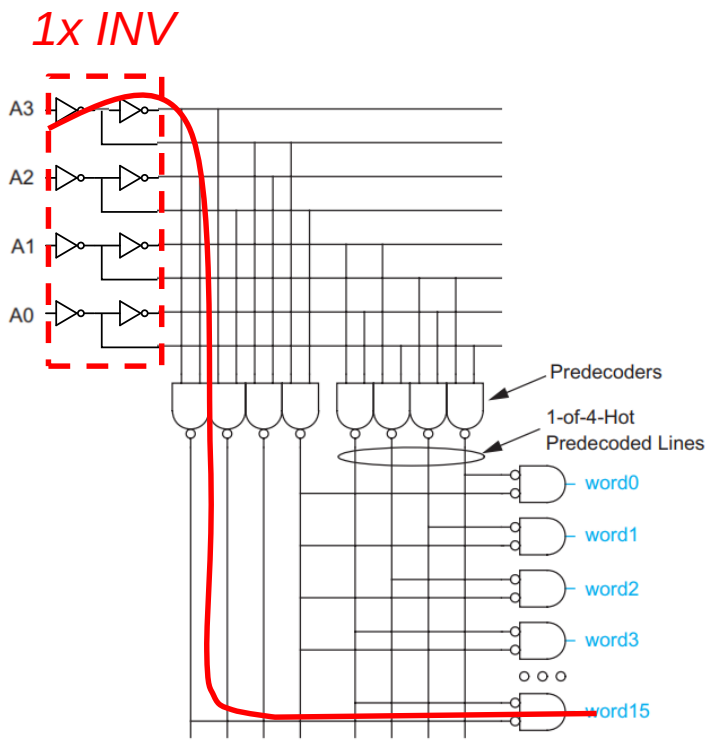
4-input AND function is built from a pair of 2-input NANDs followed by a 2-input NOR

But, many NAND gates share the same inputs and are redundant

Predecoding technique to reduce the area

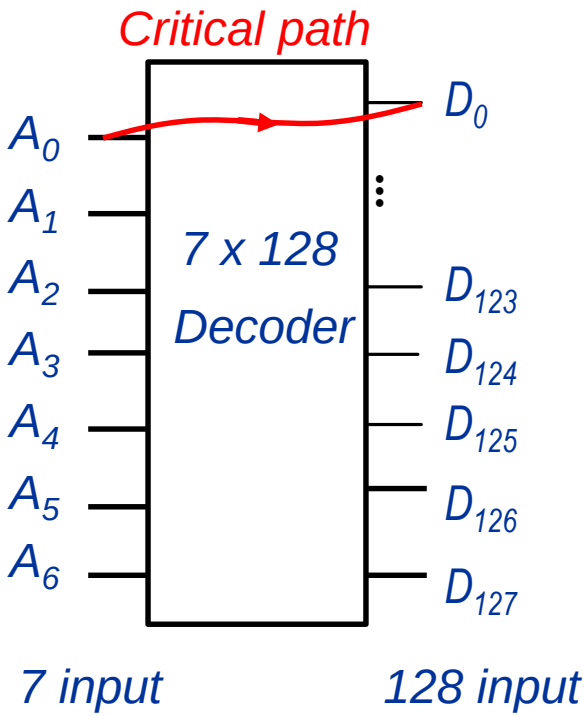
Task2: Use Logical Effort to Optimize 4x16 Decoder

- For a 4x16 decoder, optimize the critical path to minimize the propagration delay of decoder
  - Use the logical effort method
  - Assume that the input inverter/buffer is minimum sized
  - Assume that each output of decoder has a load of 256X minimum sized Finfet inverter
  - You can insert buffer at the output if necessary



Task3 (Optional): Use Logical Effort to Optimize 7x128 Decoder

- For a 7x128 decoder, first think about the scheme design. Then optimize the critical path to minimize the propagration delay of decoder
  - Use the logical effort method
  - Assume that the input inverter/buffer is minimum sized
  - Assume that each output of decoder has a load of 512X minimum sized Finfet inverter
  - You can insert buffer at the output if necessary



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Report Requirement

- Write your lab report like writing a technical document (readable, comprehensive analysis, no typo…)
- You may include
  - Lab procedures (e.g., screenshots of the critical steps)
  - Lab results (e.g., schematic view, symbol of inverter, screenshots of the simulation waveforms)
  - Observations and conclusions

Submission

- You need to submit your report and code
  - Name of report (in PDF format):
    lab3_report_[Name]_[Student No.].pdf
  - Name of code (compressing the files):
    lab3_code__[Name]_[Student No.].zip

- Please upload your report to Canvas course website

- Submission of Lab 3 report will be due on 19th December

Q & A

- If you have any technical problem, you can directly contact me

E-mail: yungsk@sjtu.edu.cn

Lab: Rm 208, Building of Microelectronics