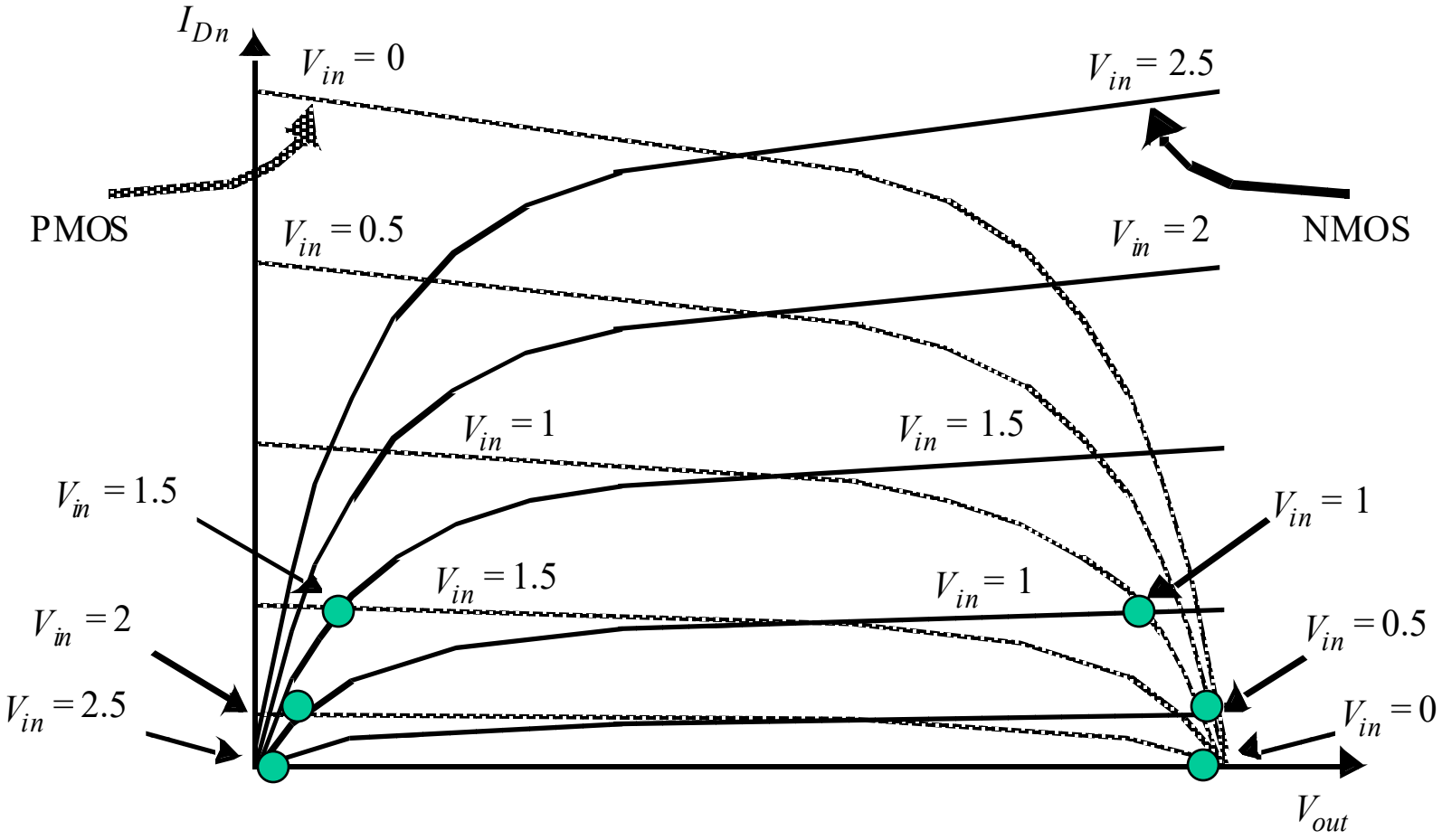
Chapter 3 Inverter Review

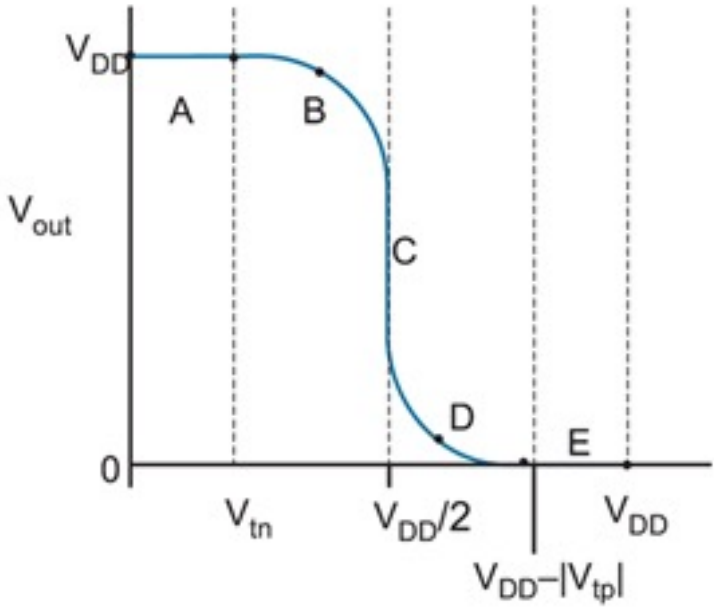
summary

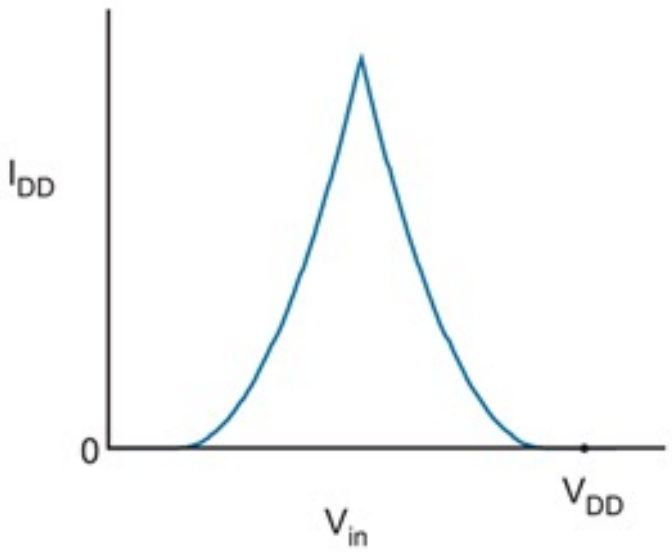
- CMOS static behavior
  - VTC, noise margin, threshold voltage
- CMOS dynamic behavior
  - Capacitance mosaic, delay
  - Ratio pMOS/nMOS:3.5,2.4,1.6
  - Optimizing inverter sizing
- Power
  - Power mosaic
  - Optimizing dynamic power
  - Short power consideration

CMOS Inverter Load Characteristics



CMOS Inverter VTC





Summary of CMOS inverter operation				
Region	Condition	P-device	N-device	output
A	$[0,V_{tn}]$	**linear**	cutoff	V_{DD}
B	$[V_{tn},V_{DD}/2]$	linear	saturated	$V_{DD}/2$
C	$=V_{DD}/2$	**saturated**	**saturated**	X drop
D	$[V_{DD}/2,V_{DD}-\|V_{TP}\|]$	saturated	linear	$<V_{DD}/2$
E	$[V_{DD}-\|V_{TP}\|, V_{DD}]$	cutoff	**linear**	0

CMOS properties

- High noise margins, the voltage swing is equal to the supply voltage
- Ratioless circuit structure
- Low output impedance
- High input resistance
- Low power

CMOS inverter static behavior

- ***Threshold Voltage***
- Noise Margin
- Gain
- DC robust

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right)$$

$$k_n = \beta_n = \mu_n C_{ox} \frac{W}{L}$$

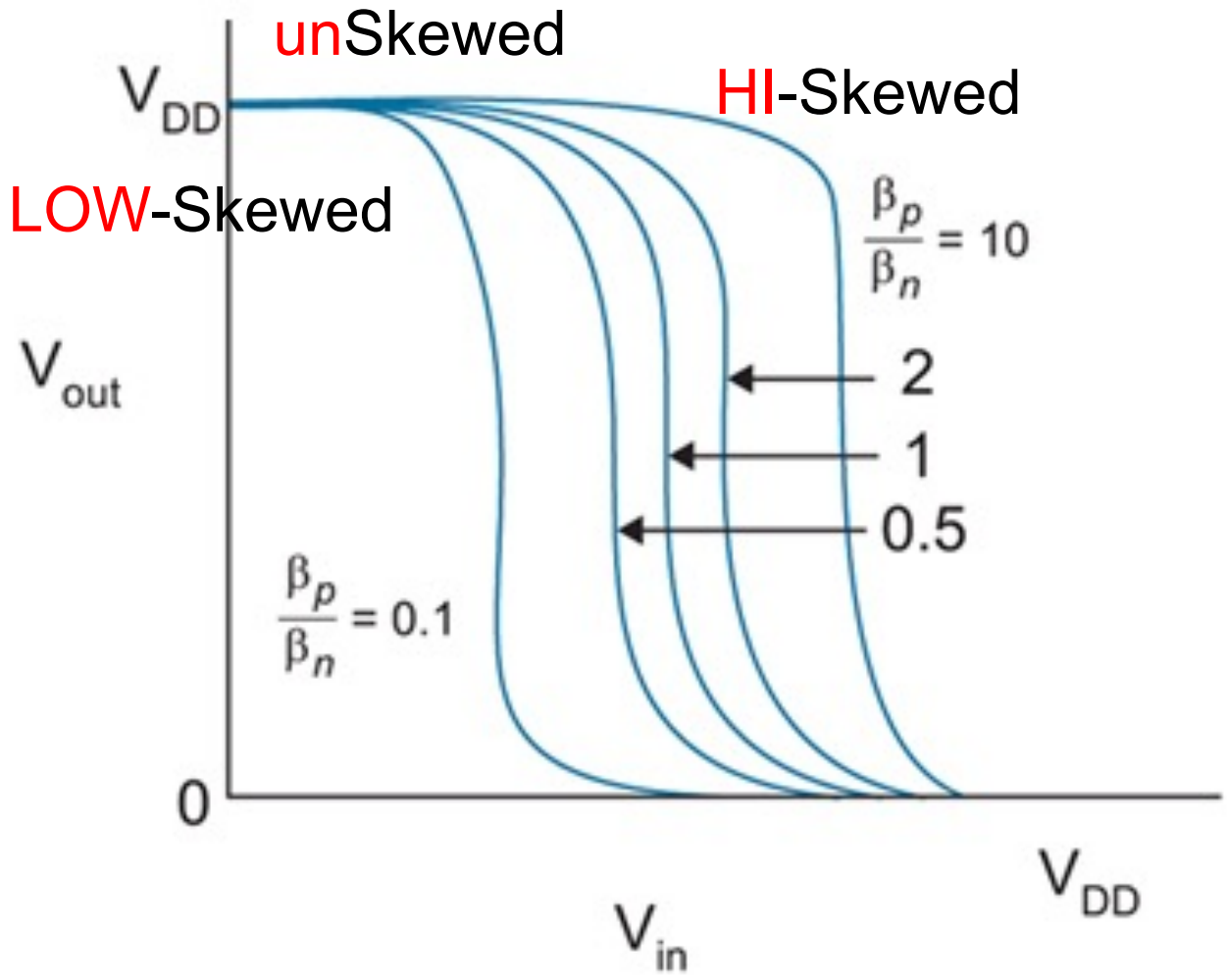
$$k_n\left((V_{gsn} - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_{gsp} - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) = 0$$

$$k_n\left((V_M - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2}\right) + k_p\left((V_M - V_D - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2}\right) =$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{dsat_n}}{2}\right) + \gamma\left(V_{DD} + V_{Tp} + \frac{V_{dsat_p}}{2}\right)}{1+\gamma} \approx \frac{\gamma V_{DD}}{1+\gamma}$$

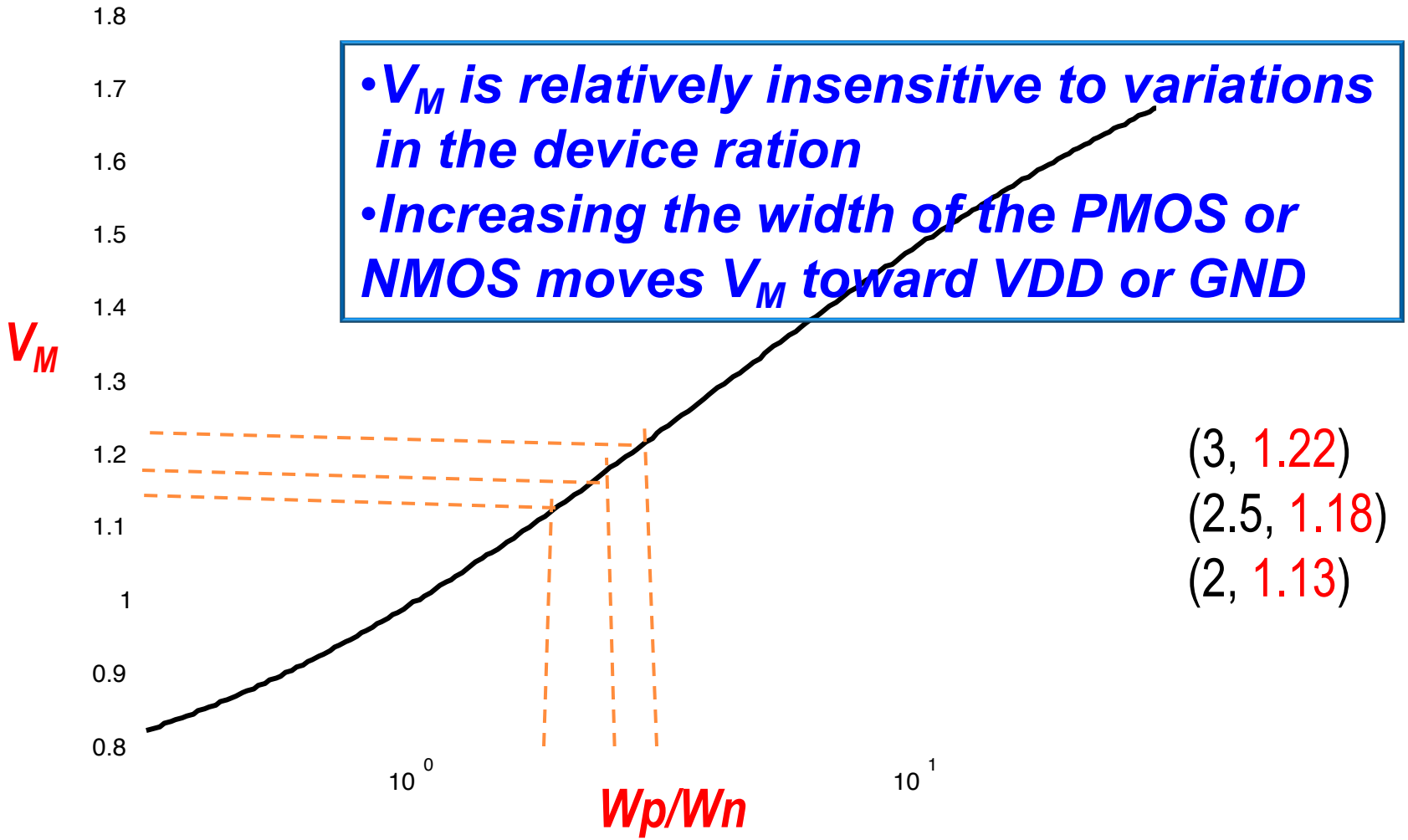
$$\gamma = \frac{k_p V_{dsat_p}}{k_n V_{dsat_n}} = \frac{W_p \nu_{dsat_p}}{W_n \nu_{dsat_n}}$$

$$V_{sat} \approx V_c = LE_c = L\frac{2\nu_{sat}}{\mu_{eff}}$$



$$V_M = \frac{\left(V_{Tn} + \frac{V_{dsat_n}}{2}\right) + \gamma\left(V_{DD} + V_{Tp} + \frac{V_{dsat_p}}{2}\right)}{1+\gamma} \approx \frac{\gamma V_{DD}}{1+\gamma}$$

Switching Threshold as a function of Transistor Ratio



$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_T)V_{dsat} - \frac{V_{dsat}^2}{2} \right) \qquad k_n = \beta_n = \mu_n C_{ox} \frac{W}{L}$$

$$k_n \left((V_{gsn} - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2} \right) + k_p \left((V_{gsp} - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2} \right) = 0$$

$$k_n \left((V_M - V_{Tn})V_{dsat_n} - \frac{V_{dsat_n}^2}{2} \right) + k_p \left((V_M - V_D - V_{Tp})V_{dsat_p} - \frac{V_{dsat_p}^2}{2} \right) =$$

$$\frac{W_p/L_p}{W_n/L_n} = = \approx \frac{k_n' V_{dsat_n} \left(V_M - V_{Tn} - \frac{V_{dsat_n}}{2} \right)}{k_p' V_{dsat_p} \left(V_{DD} - V_M + V_{Tp} + \frac{V_{dsat_p}}{2} \right)}$$

Switching threshold of CMOS inverter

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

Assuming $W_p/W_n=8$, calculating V_M=?

$$r = \frac{k_p' \, W_p/L_p \, V_{DSAT_p}}{k_n' \, W_n/L_n \, V_{DSAT_n}} = \frac{-30*(-1)}{115*0.63}*8 = 3.3$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSAT_n}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSAT_p}}{2})}{1+r}$$

$$= \frac{(0.43 + \frac{0.63}{2}) + 3.3(2.5 - 0.4 - \frac{0.4}{2})}{1+3.3} = \frac{0.75 + 3.3*1.9}{1+3.3} = 1.63V$$

Switching threshold of CMOS inverter

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

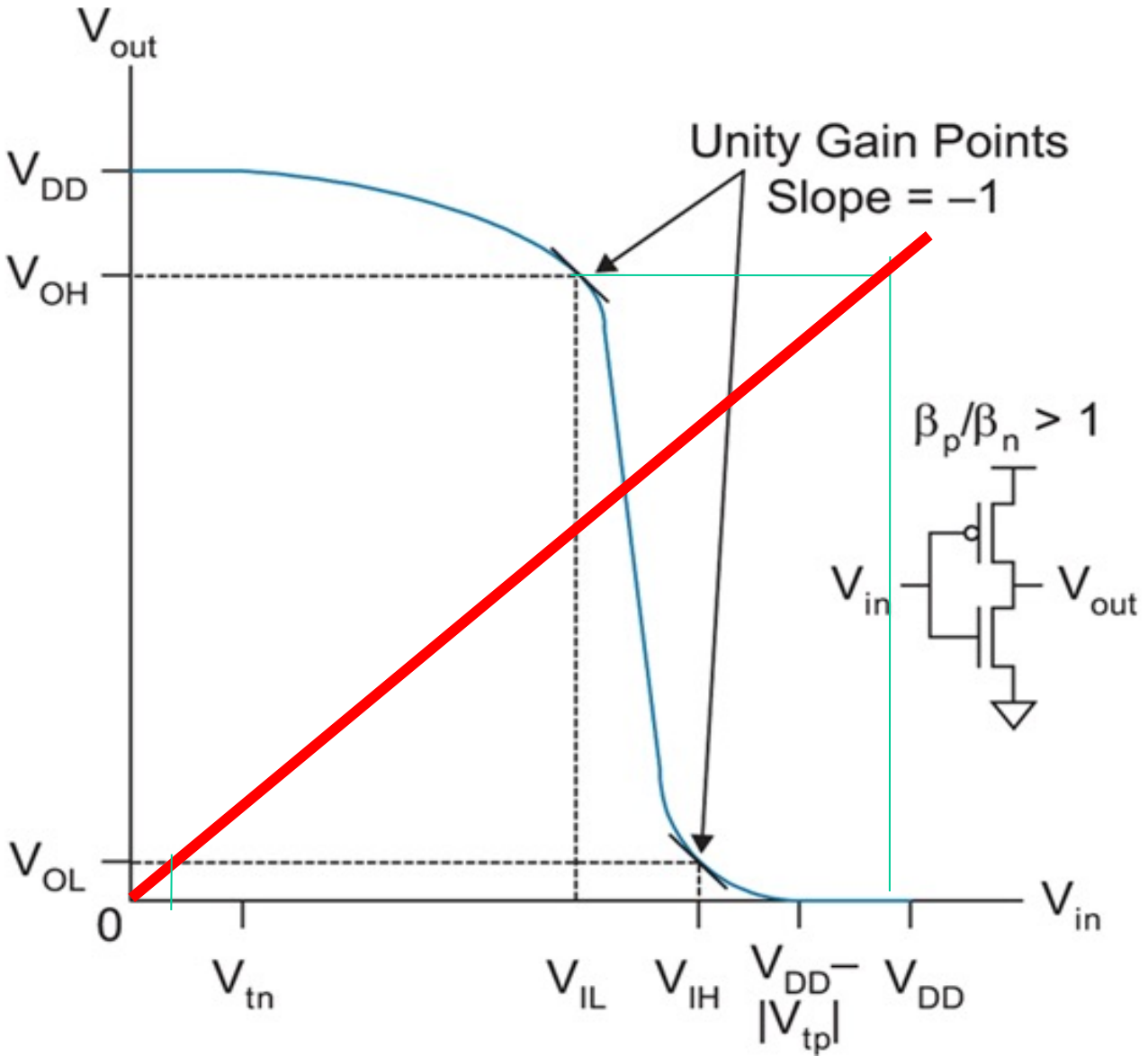
$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})}{-k_p' V_{DSAT_p}(V_{DD} - V_M + V_{Tp} + \frac{V_{DSAT_p}}{2})} = \frac{115\times10^{-6}\times0.63\times(1.25-0.43-\frac{0.63}{2})}{30\times10^{-6}\times1\times(1.25-0.4-\frac{1}{2})} = 3.5$$

This rate let $V_M=V_{dd}/2$!

CMOS inverter static behavior

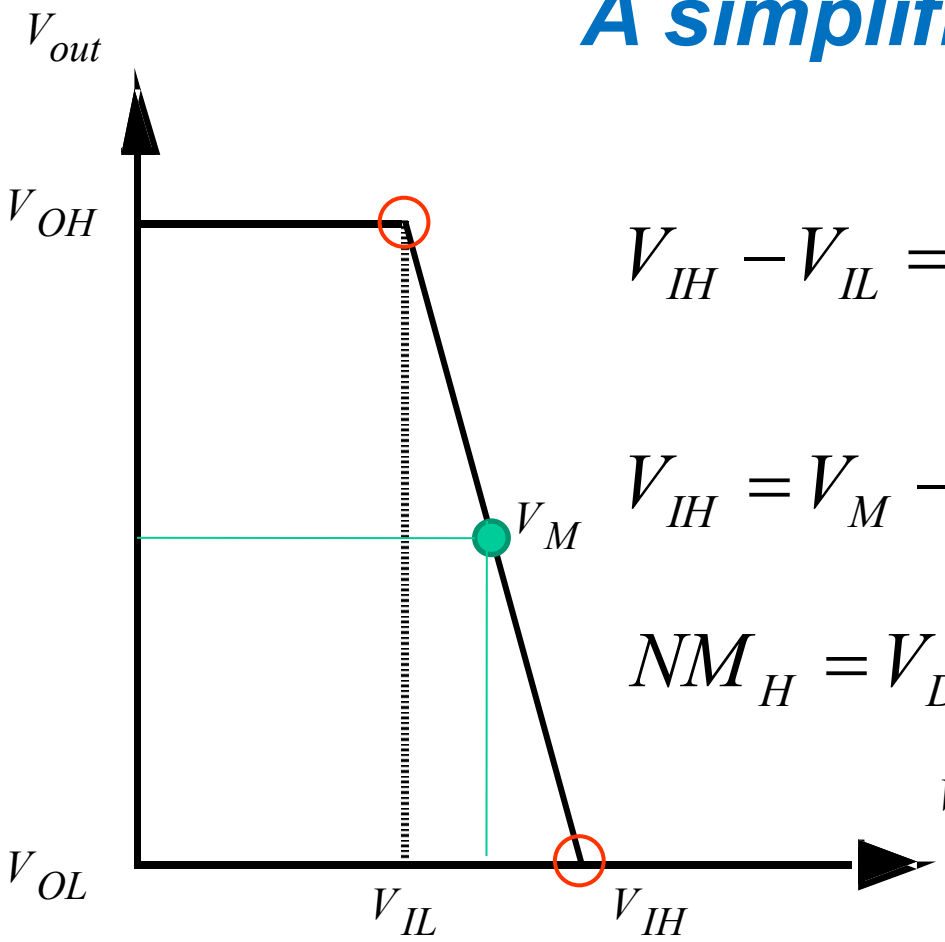
- Threshold Voltage
- ***Noise Margin***
- Gain
- DC robust

Determining V_{IH} and V_{IL}



Determining V_{IH} and V_{IL}

A simplified approach!



$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g}, V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH}, NM_L = V_{IL}$$

V_M increase, NM_H decrease, NM_L increase

Example

g=-30, V_{dd}=2.5V, V_M=1.0V Please estimate NM_H and NM_L

$V_{IH}=V_M-V_M/g=1.0*(1+1/30)=1.03V$

$V_{IL}=(V_{DD}-V_M)/g+V_M=-1.5/30+1.0=0.95V$

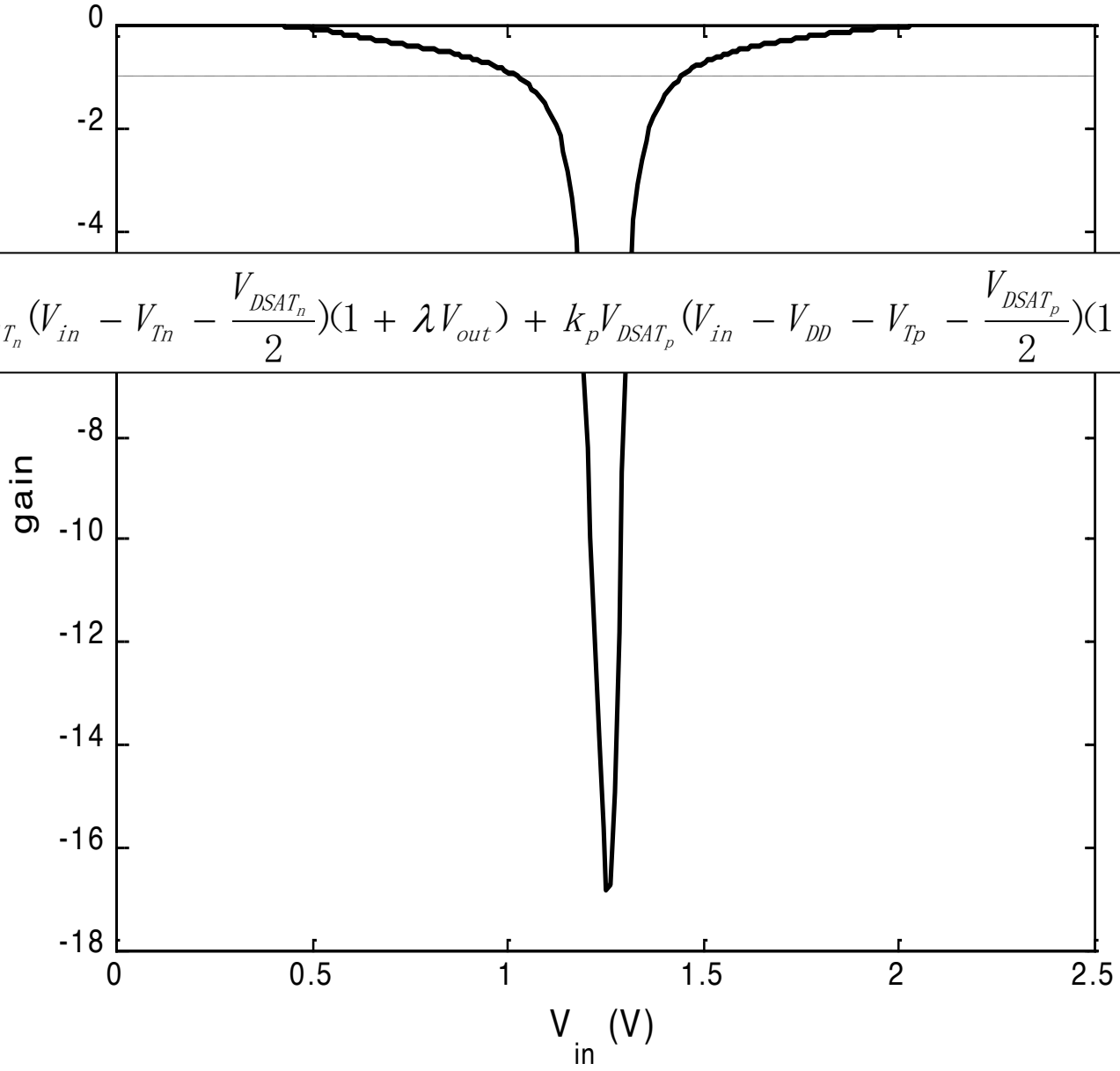
$NM_H=V_{OH}-V_{IH}=2.5-1.03=1.47V$

$NM_L=V_{IL}-V_{OL}=0.95V$

CMOS inverter static behavior

- Threshold Voltage
- Noise Margin
- ***Gain***
- DC robust

Inverter Gain



$$k_n V_{DSAT_n}(V_{in} - V_{Tn} - \frac{V_{DSAT_n}}{2})(1 + \lambda V_{out}) + k_p V_{DSAT_p}(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSAT_p}}{2})(1 + \lambda(V_{DD} - V_{out})) = 0$$

Inverter Gain

$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M}$$

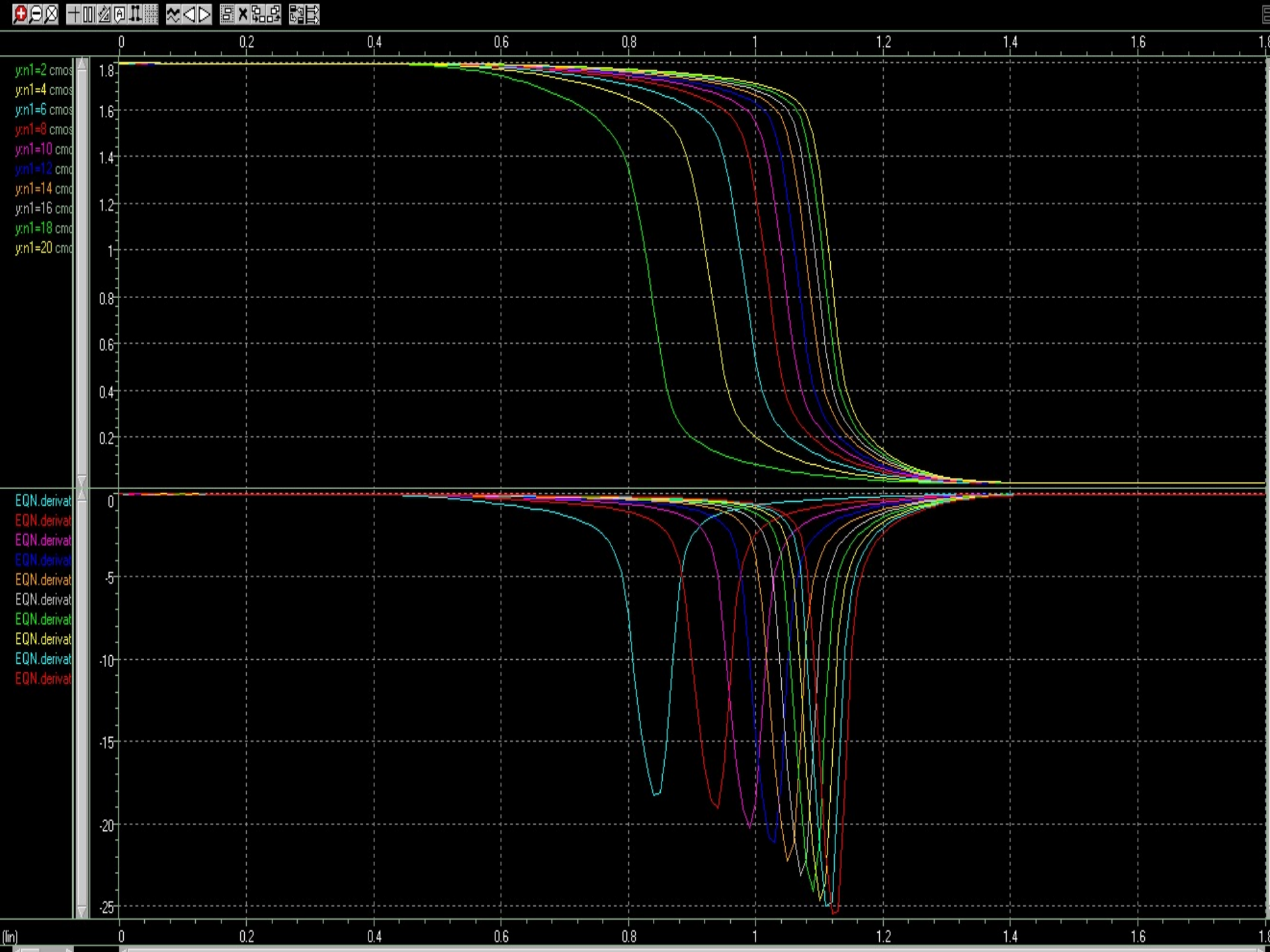
$$= -\left.\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{\lambda_n k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right) + \lambda_p k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - {V_{DSATp}}/{2}\right)}\right|_{V_{in}=V}$$

$$\approx -\frac{k_n V_{DSATn}(1+\lambda_n V_{out}) + k_p V_{DSATp}\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)}{k_n V_{DSATn}\left(V_{in} - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

$$= -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n - \lambda_p)}$$

Ratio increase, Gain increase

$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}}$$


y:n1=2 cmos
y:n1=4 cmos
y:n1=6 cmos
y:n1=8 cmos
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y:n1=14 cmo
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0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
0
-5
-10
-15
-20
-25
(lin)

homework1

*An inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of **64** and with the NMOS transistor minimum size (W=0.375um, L=0.25um,**W/L=1.5**) , Vdd=2.5V , Please give the gain of **V_M**, and **V_{IL},V_{IH},NM_L,NM_H, VTC** curve*

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

$$V_M = \frac{\left(V_{Tn} + {V_{DSATn}}/{2}\right) + \gamma\left(V_{DD} + V_{Tp} + {V_{DSATp}}/{2}\right)}{1+\gamma}$$

$$= \frac{(0.43 + 0.63/2) + 26.4 * (2.5 - 0.4 - 1/2)}{1 + 26.4}$$

$$= \frac{0.745 + 26.4 * 1.6}{1 + 26.4} = 1.57$$

$$\gamma = \frac{k_p' {W_p}/{L_p} V_{DSATp}}{k_n' {W_n}/{L_n} V_{DSATn}} = \frac{-30 * (-1)}{115 * 0.63} * 64 = 26.4$$

$$g = -\frac{1+\gamma}{\left(V_M - V_{Tn} - {V_{DSATn}}/{2}\right)(\lambda_n + \lambda_p)} = -\frac{1 + 26.4}{\left(1.57 - 0.43 - \frac{0.63}{2}\right)(0.06 + 0.1)}$$

$$= -\frac{27.4}{0.824 * 0.16} = -208$$

$V_{IH}=V_M-V_M/g=1.57*(1+1/208)=1.58V$ *$V_{IL}=(V_{DD}-V_M)/g+V_M=-0.93/208+1.57=1.57V$*

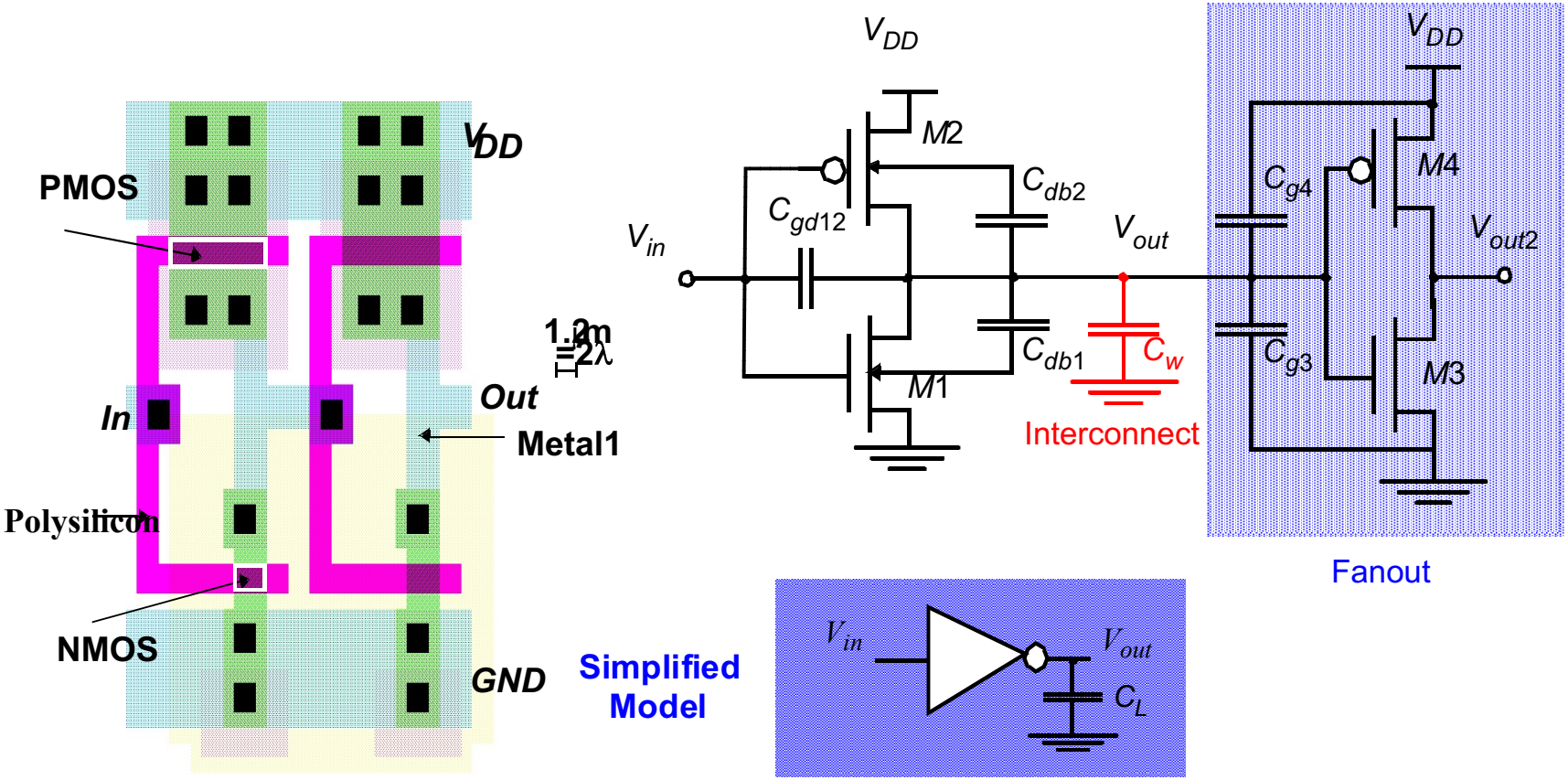
$NM_H=V_{OH}-V_{IH}=2.5-1.58=0.92V$

$NM_L=V_{IL}-V_{OL}=1.57V$

$C_{inverter}$ dynamic characteristic

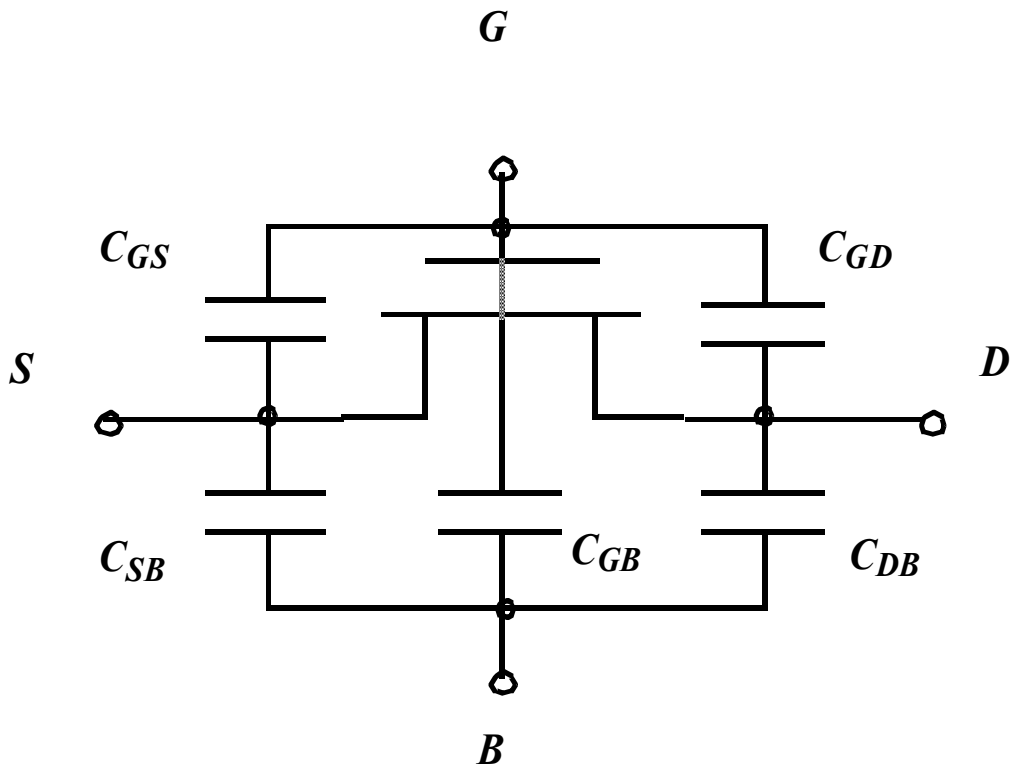
- ***Capacitances mosaic***
- Propagation delay
- Optimizing inverter sizing

Computing the Capacitances

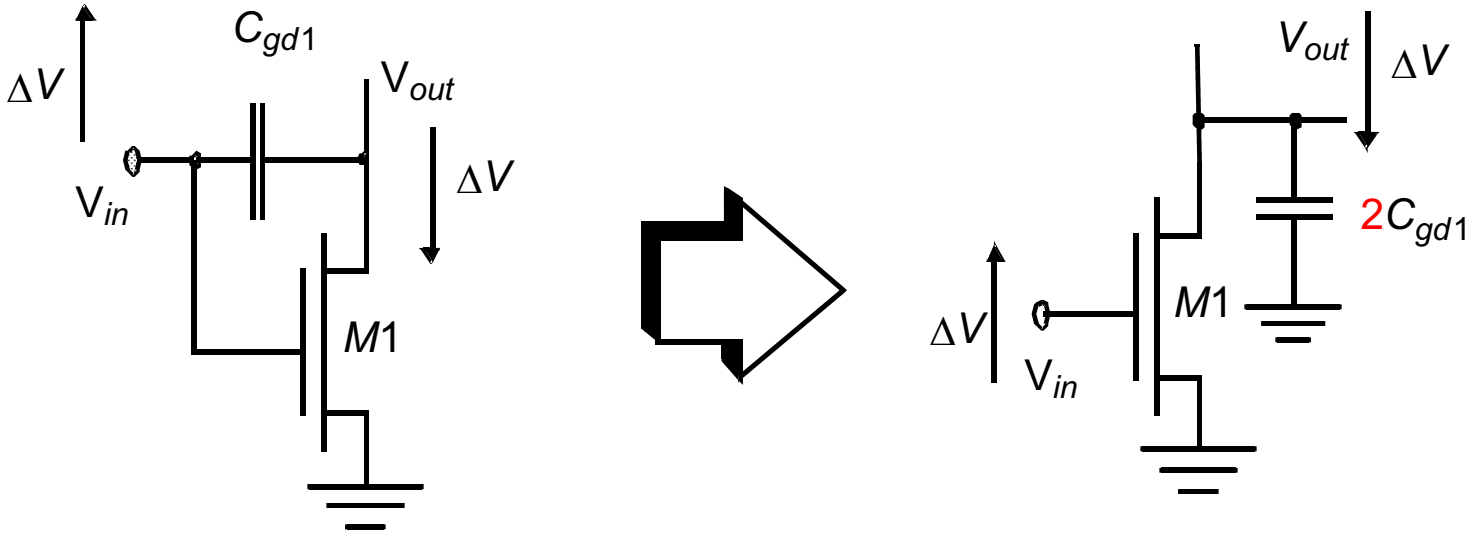


Capacitance model

$$C_{GS} = C_{GSO} + C_{GCS}$$
$$C_{GD} = C_{GDO} + C_{GCD}$$
$$C_{GB} = C_{GCB}$$
$$C_{SB} = C_{Sdiff}$$
$$C_{DB} = C_{Ddiff}$$

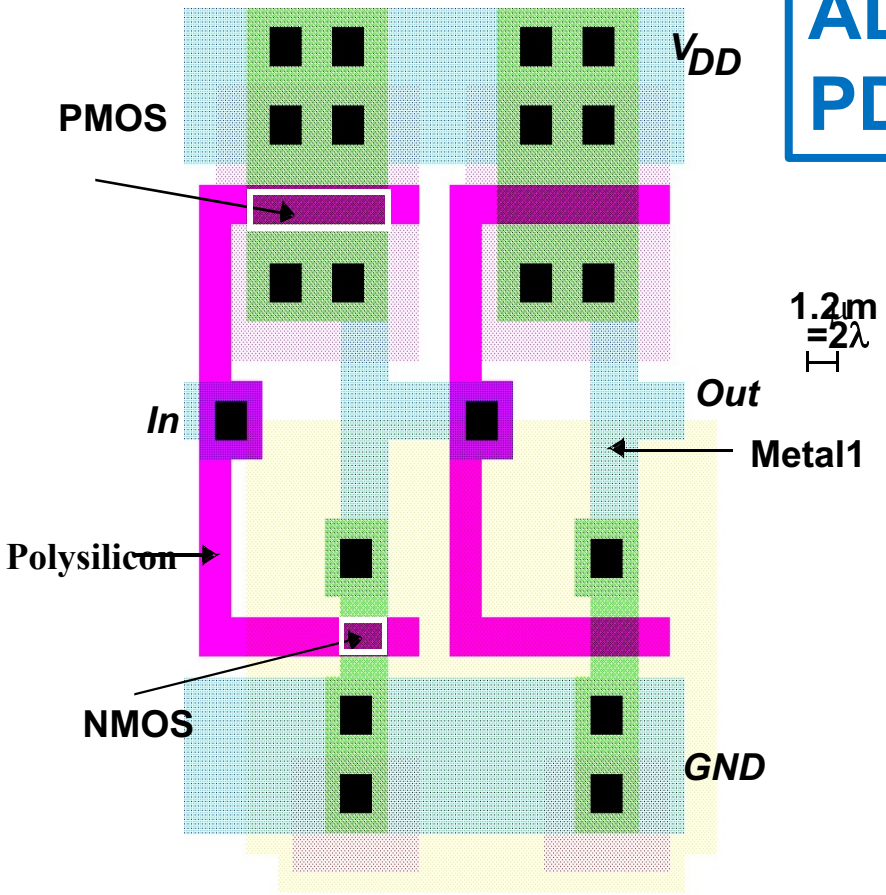


The Miller Effect



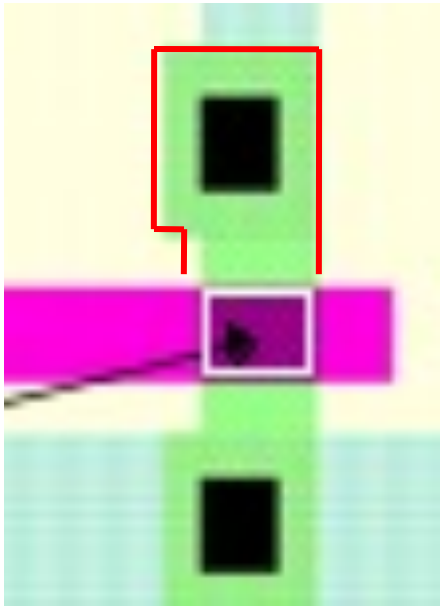
"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

Computing the Capacitances



$AD=4*4+3*1=16+3=19\lambda^2$

$PD=1+4+4+4+1+1=15\lambda$



Computing the Capacitances

capacitor	expression	Value(fF) (H->L)	Value(fF) (L->H)
C_{gd1}	$2C_{GDO_n}*W_n$	0.23	0.23
C_{gd2}	$2C_{GDO_p}*W_p$	0.61	0.61
C_{db1}	$K_{eqn}AD_nC_J+K_{eqwn}PD_nC_{JSW}$	0.66	0.90
C_{db2}	$K_{eqn}AD_nC_J+K_{eqwn}PD_nC_{JSW}$	1.5	1.15
C_{g3}	$(C_{GD0_n}+C_{GSO_n})W_n+C_{ox}W_nL_n$	0.76	0.76
C_{g4}	$(C_{GD0_p}+C_{GSO_p})W_p+C_{ox}W_pL_p$	2.28	2.28
C_w		0.12	0.12
C_L		6.1	6.0

$$C_j = \frac{dQ_j}{dV_D} = \frac{C_{j_0}}{\left(1 - V_D/\Phi_0\right)^m}$$

$$C_L=W_nC_n+W_pC_p+C_w$$

Cinverter dynamic characteristic

- Capacitances mosaic
- ***Propagation delay***
- Optimizing inverter sizing

Define NMOS-to-PMOS ratio

$$C_L = W_n C_n + W_p C_p + C_w$$

$$t_{pHL} = ln2 C_L R_{eqn} \approx \frac{C_L}{2\left(\frac{W}{L}\right)_n k'_n V_{dsatn}} \approx \frac{C_n}{2k'_n V_{dsatn}} + \frac{\beta C_p}{2k'_n V_{dsatn}}$$

$$t_{pLH} = ln2 C_L R_{eqp} \approx \frac{C_L}{2\left(\frac{W}{L}\right)_p k'_p V_{dsatp}} \approx \frac{C_p}{2k'_p V_{dsatp}} + \frac{C_n}{2\beta k'_p V_{dsatp}}$$

In order to create an inverter with a symmetrical propagate delays Also create symmetrical VTC

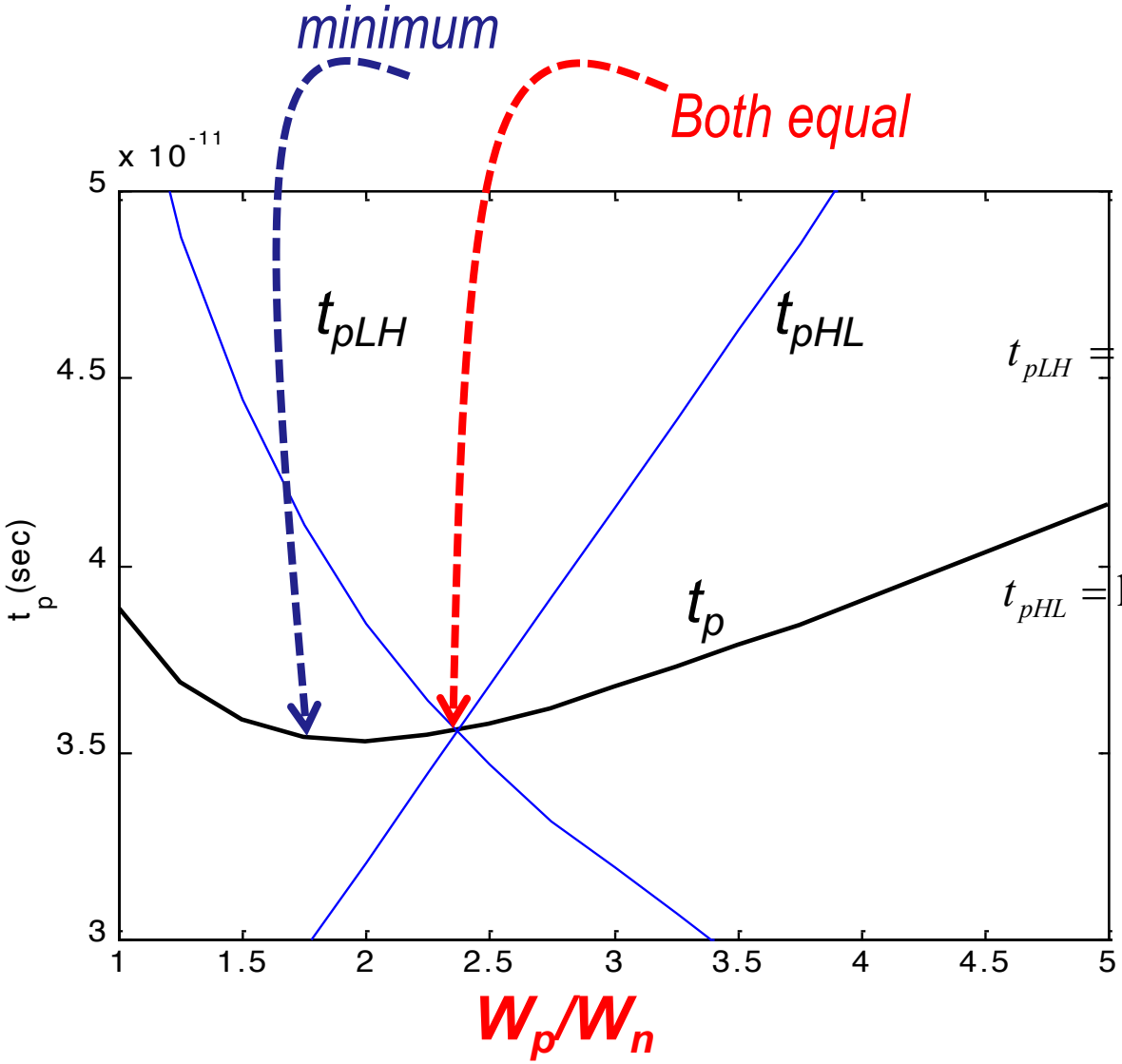
$$\gamma = R_{eq_p} / R_{eq_n} = \frac{(W/L)_n k'_n V_{DSAT_n}}{(W/L)_p k'_p V_{DSAT_p}} = 1$$

β=2.4 which Rn=Rp!

Parameters for manual model of generic 0.25um CMOS process(minimum length device)

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2))	λ(V^{-1})
NMOS	0.43	0.4	0.63	$115X10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30X10^{-6}$	-0.1

Which point is optimal delay?



$$t_{pLH} = \ln(2) C_L R_{eq_p} \approx \frac{C_L}{2(W/L)_p k'_p V_{DSAT_p}}$$

$$t_{pHL} = \ln(2) C_L R_{eq_n} \approx \frac{C_L}{2(W/L)_n k'_n V_{DSAT_n}}$$

Assume C_L=C

Design for Performance

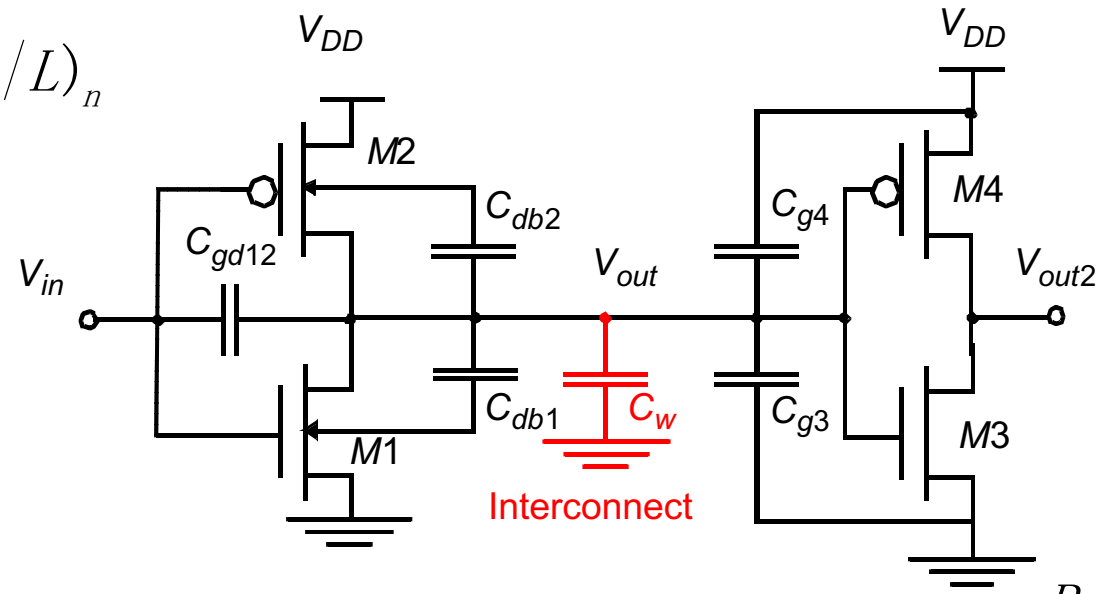
- Reduce C_L
  - internal diffusion capacitance of the gate itself，keep the drain diffusion as small as possible
  - interconnect capacitance
  - fanout
- Increase V_{DD}
  - can trade-off energy for performance
  - *increasing V_{DD} above a certain level yields only very minimal improvements*
- Increase W/L ratio of the transistor
  - the most powerful and effective performance optimization tool in the hands of the designer
  - watch out for self-loading! – when the intrinsic capacitance dominates the extrinsic load

Which point is optimal delay?

$$C_L = (C_{d_{n1}} + C_{d_{p1}}) + 2(C_{g_{n3}} + C_{g_{p4}}) + C_W = (1+\beta)(C_{d_{n1}} + 2C_{g_{n3}}) + C_W$$

$$= (1+\beta)C_s + C_W \qquad C_s = C_{d_{n1}} + 2C_{gn3}$$

$$\beta = (W/L)_p / (W/L)_n$$



$$t_p = \frac{t_{pLH} + t_{pHL}}{2} = \frac{\ln 2}{2}((1+\beta)C_s + C_W)(R_{eq_n} + \frac{R_{eq_p}}{\beta})$$

$$= 0.345((1+\beta)C_s + C_W)R_{eq_n}(1 + \frac{\gamma}{\beta})$$

Which point is optimal delay?

$$\frac{\partial t_p}{\partial \beta} = 0$$

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

$$\frac{\partial[0.345((1+\beta)C_S + C_W)R_{eq_n}(1+\frac{\gamma}{\beta})]}{\partial\beta} = 0$$

$$\beta = \sqrt{\gamma(1+\frac{C_W}{C_S})} \approx \sqrt{\gamma} = \sqrt{\frac{31}{13}}\Big|_{\substack{Vdd=2.5V \\ 0.25um}} = 1.5$$

This r is different from before! It is the resistor rate of the NMOS and PMOS

Summary of **Ratio**

Beta=1.5, we have minimum delay

$$\beta = \sqrt{\gamma} \approx \sqrt{\frac{k_n' V_{DSat_n}}{k_p' V_{DSat_p}}}$$

Beta=2.4, we have equal delay t_{phl}=t_{plh}

$$\beta = \gamma = \frac{k_n' V_{DSat_n}}{k_p' V_{DSat_p}}$$

Beta=3.5, we have V_M=V_{dd}/2

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSAT_n}(V_M - V_{Tn} - \frac{V_{DSAT_n}}{2})}{-k_p' V_{DSAT_p}(V_{DD} - V_M + V_{Tp} + \frac{V_{DSAT_p}}{2})} = \frac{115\times10^{-6}\times0.63\times(1.25-0.43-\frac{0.63}{2})}{30\times10^{-6}\times1\times(1.25-0.4-\frac{1}{2})} = 3.5$$

Cinverter dynamic characteristic

- Capacitances mosaic
- Propagation delay
- ***Optimizing inverter sizing***

Increasing inverter performance by sizing the NMOS and PMOS

$$t_p = 0.69R_{eq}(C_{int} + C_{ext}) = 0.69R_{eq}C_{int}(1 + C_{ext}/C_{int})$$

$$= 0.69\,(R_{ref}/S)\,(SC_{iref})\,(1 + C_{ext}/SC_{iref})$$

$$= t_{p0} + t_{p0}\frac{C_{ext}}{SC_{iref}}$$

$$= t_{p0}(1 + \frac{C_2}{C_1})$$

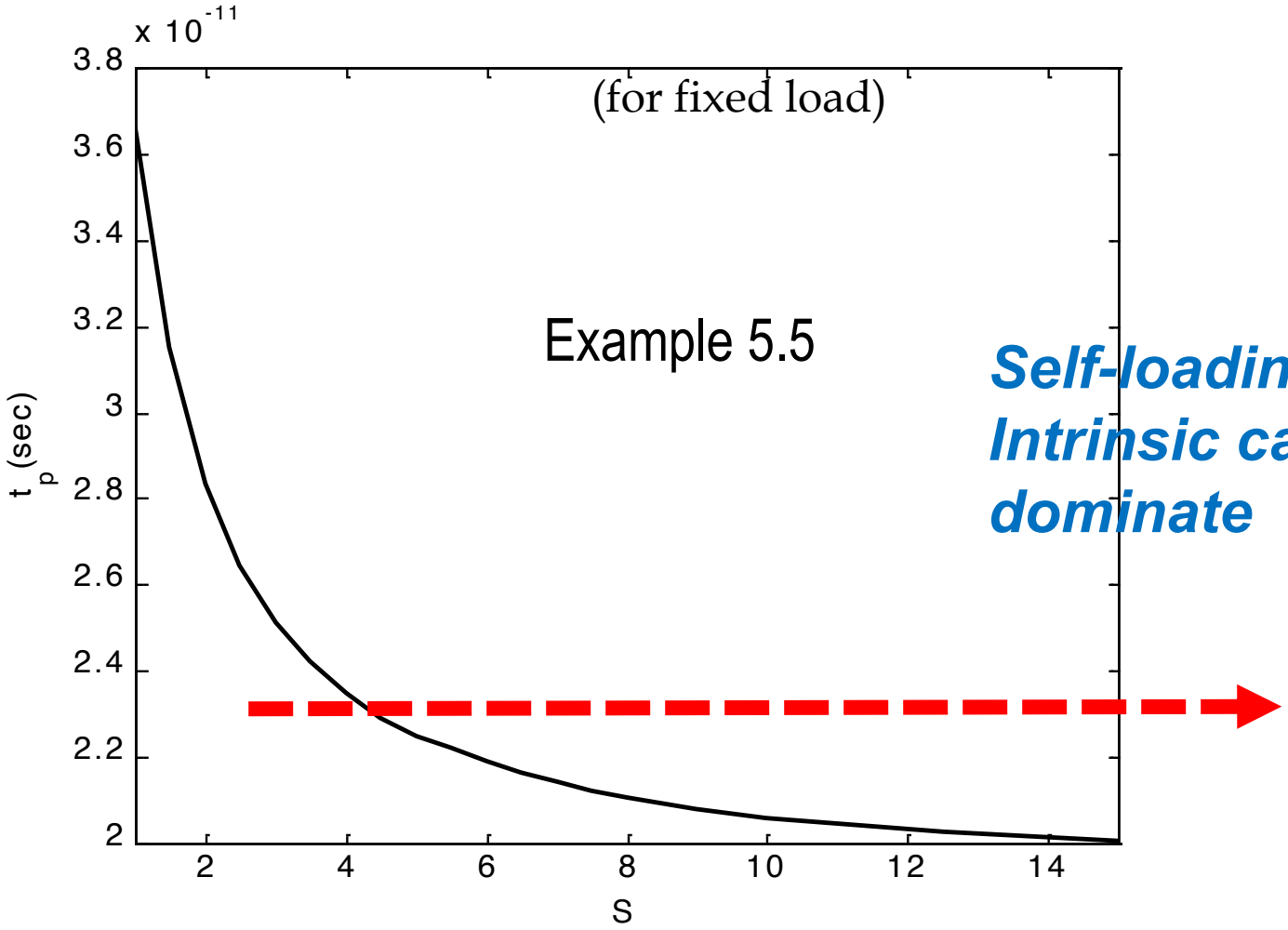
If load

S>>0 will eliminate the impact of any external load

If no load

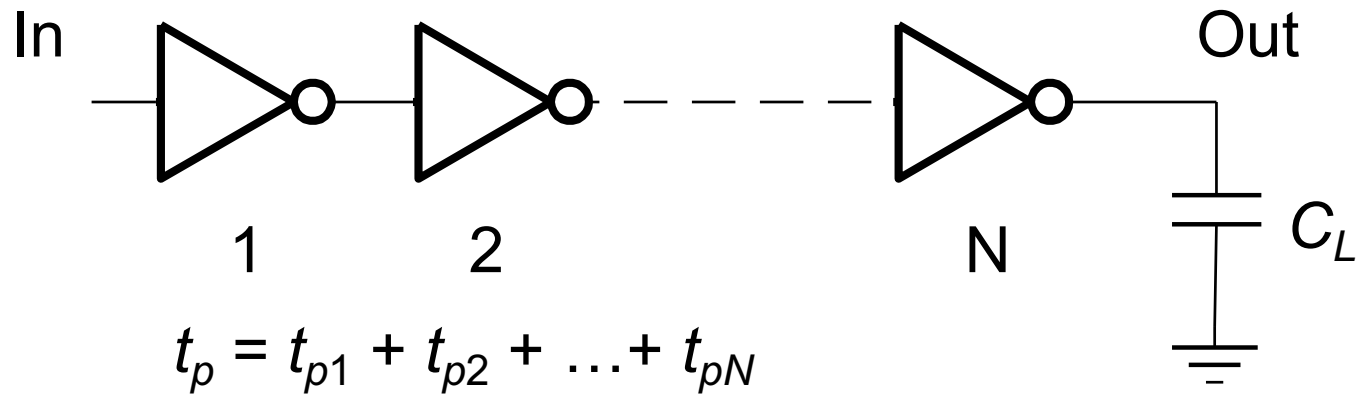
Intrinsic delay is independent of the sizing of the gate

Device Sizing



Self-loading effect: Intrinsic capacitances dominate

Apply to Inverter Chain



$$t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$$

$$t_{pj} \sim R_{unit} C_{unit} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{i=1}^{N} \left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}} \right), \quad C_{gin,N+1} = C_L$$

Optimal Tapering for Given N

- Delay equation has N - 1 unknowns, $C_{gin,2} - C_{gin,N}$
- Minimize the delay, find N - 1 partial derivatives

  Result: $C_{gin,j+1}/C_{gin,j} = C_{gin,j}/C_{gin,j-1}$
- Size of each stage is the geometric mean of two neighbors $C_{gin,j} = \sqrt{C_{gin,j-1}C_{gin,j+1}}$
- each stage has the same effective fanout (C_{out}/C_{in})
- ***each stage has the same delay***

Optimum size for fixed Number of Stages

When each stage is sized by *f* and has same eff. fanout *f*: $f^N = F = C_L / C_{gin,1}$

Effective fanout of each stage:

$$f = \sqrt[N]{F}$$

Minimum path delay

$$t_p = N t_{p0}\left(1 + \sqrt[N]{F} / \gamma\right)$$

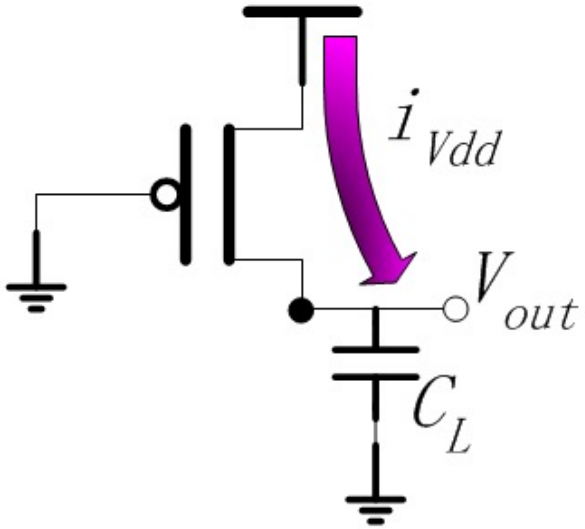
Where Does Power Go in CMOS?

- Dynamic Power Consumption
  - Charging and Discharging Capacitors
- Short Circuit Currents
  - Short Circuit Path between Supply Rails during Switching
- Leakage
  - Leaking diodes and transistors

Dynamic Power Consumption

- (dis)charge process
  - C_L is charged through pMOS on-resistance
  - C_L is discharged through nMOS on-resistance
- Power distribution
  - Charge processing:One part of Supply power is dissipated in the pMOS transistor,another part is dissipated in the charge C_L
  - Discharge processing:all dissipated in the nMOS transistor

Precise measure of dynamic power consumption



$$E_{V_{dd}} = \int_0^\infty i_{V_{dd}}(t) V_{dd}\, dt = V_{dd} \int_0^\infty C_L \frac{dv_{out}}{dt} dt$$

$$= C_L V_{dd} \int_0^{V_{dd}} dv_{out} = C_L V_{dd}^2$$

$$E_C = \int_0^\infty i_{V_{dd}}(t) v_{out}\, dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out}\, dt$$

$$= C_L \int_0^{V_{dd}} v_{out}\, dv_{out} = \frac{C_L V_{dd}^2}{2}$$

CMOS Energy & Power Equations

$$E = C_L V_{DD}^2 P_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage} 1/f_{clock}$$

$$f_{0\rightarrow1} = P_{0\rightarrow1} * f_{clock}$$

$$P = C_L V_{DD}^2 f_{0\rightarrow1} + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leakage}$$

Dynamic power ***Short-circuit power*** ***Leakage power***

Lowering Dynamic Power

Capacitance:
Function of fan-out, wire length, transistor sizes

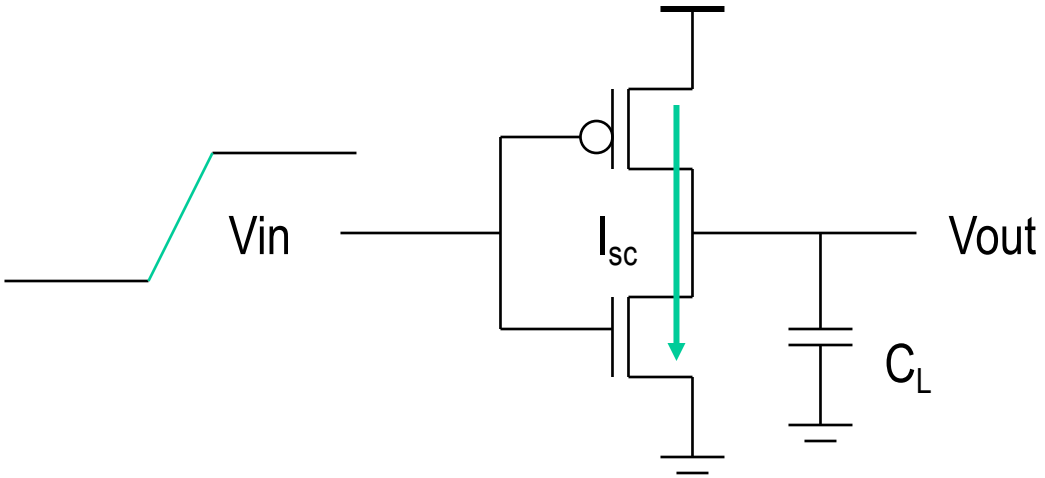
Supply Voltage:
Has been dropping with successive generations

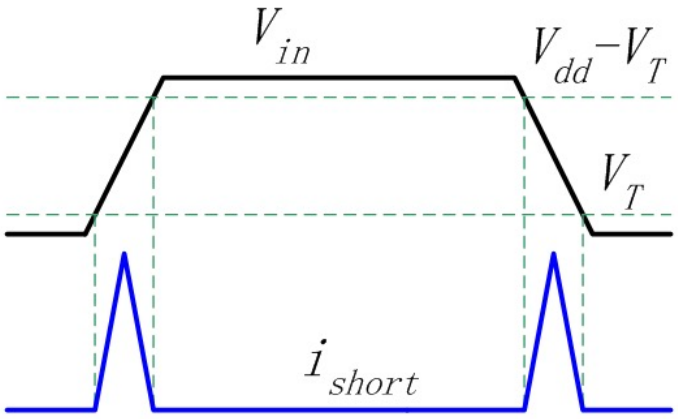
$$P_{dyn} = C_L V_{DD}^2 P_{0\rightarrow1} f$$

Activity factor:
How often, on average, do wires switch?

Clock frequency:
Increasing…

Short Circuit Power Consumption



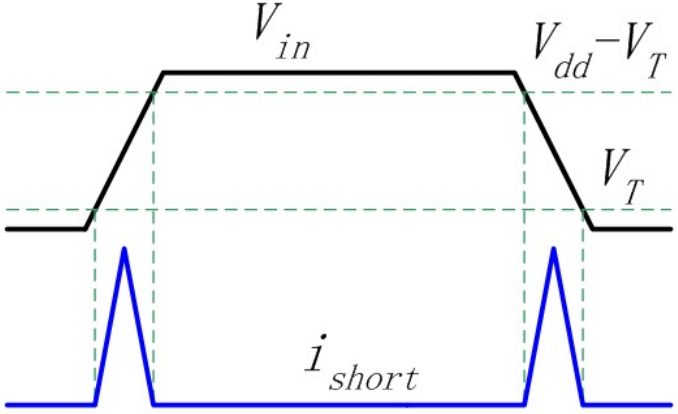


Finite slope of the input signal causes a direct current path between V_{DD} and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

Short Circuit power consumption

- Energy of ever switch activity

$$E_{dp} = V_{dd}\frac{I_{peak}}{2}t_{rise} + V_{dd}\frac{I_{peak}}{2}t_{f}$$



- Average power

$$P_{dp} = \frac{t_{rise}+t_{fall}}{2}V_{dd}I_{peak}f$$

- ***Short circuit occupy no more than 20% of dynamic power***

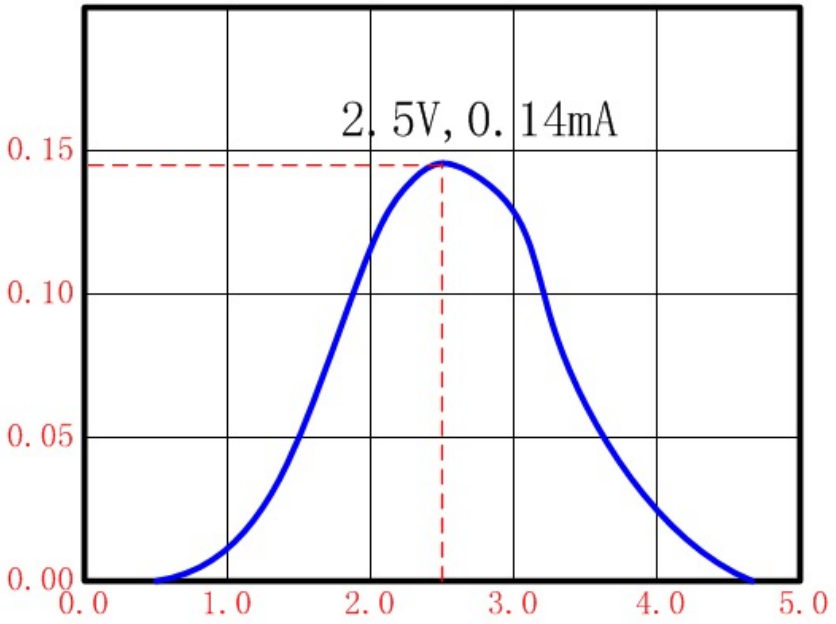
$$t_{sc} = \frac{V_{DD}-2V_T}{V_{DD}}t_s \approx \frac{V_{DD}-2V_T}{V_{DD}} \times \frac{t_{r(f)}}{0.8}$$

An example

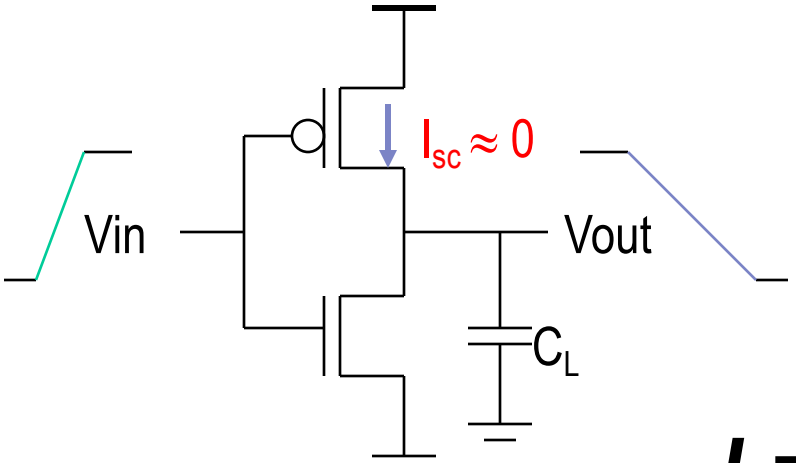
- Assume rise/fall time both are 300ps
- Short circuit power:

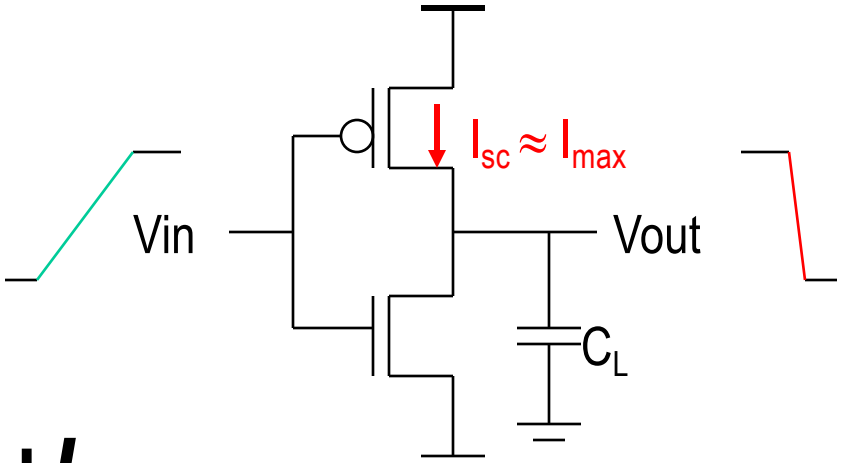
  300ps×5V × 0.14mA=0.21pJ
- Dynamic power

  30pF × 5V × 5V=0.75pJ



Impact of C_L on P_{sc}





$$I_n = I_{sc} + I_d$$

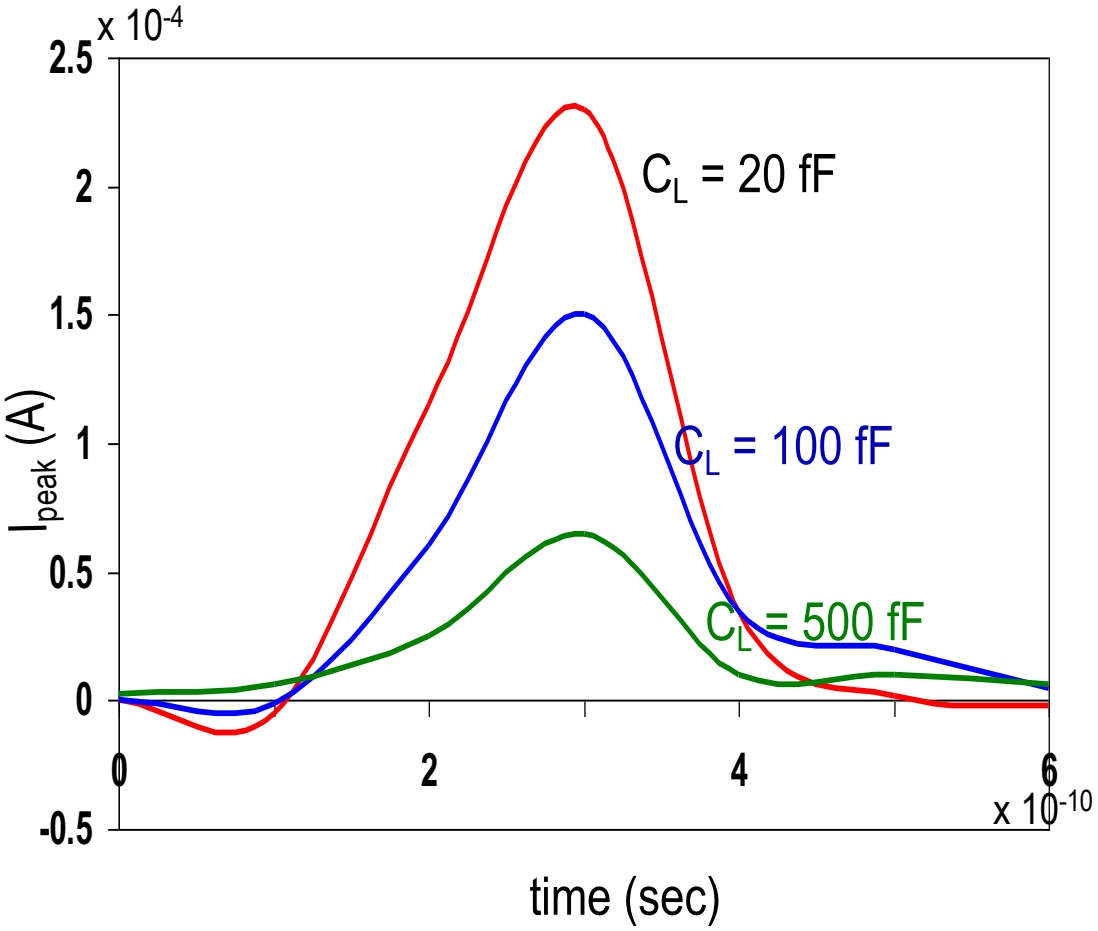
Large capacitive load

Output fall time significantly larger than input rise time.

Small capacitive load

Output fall time substantially smaller than the input rise time.

I_{peak} as a Function of C_L

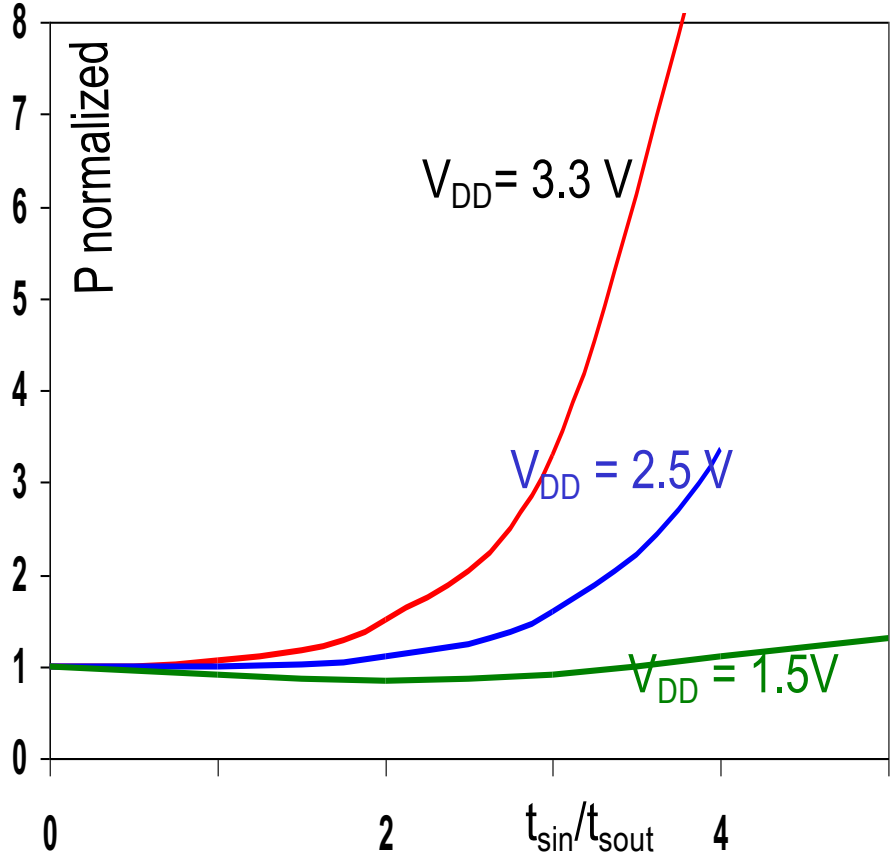


500 psec input slope

When load capacitance is small, I_{peak} is large.

Short circuit dissipation is minimized by matching the rise/fall times of the input and output signals - slope engineering.

P_{sc} as a Function of Rise/Fall Times



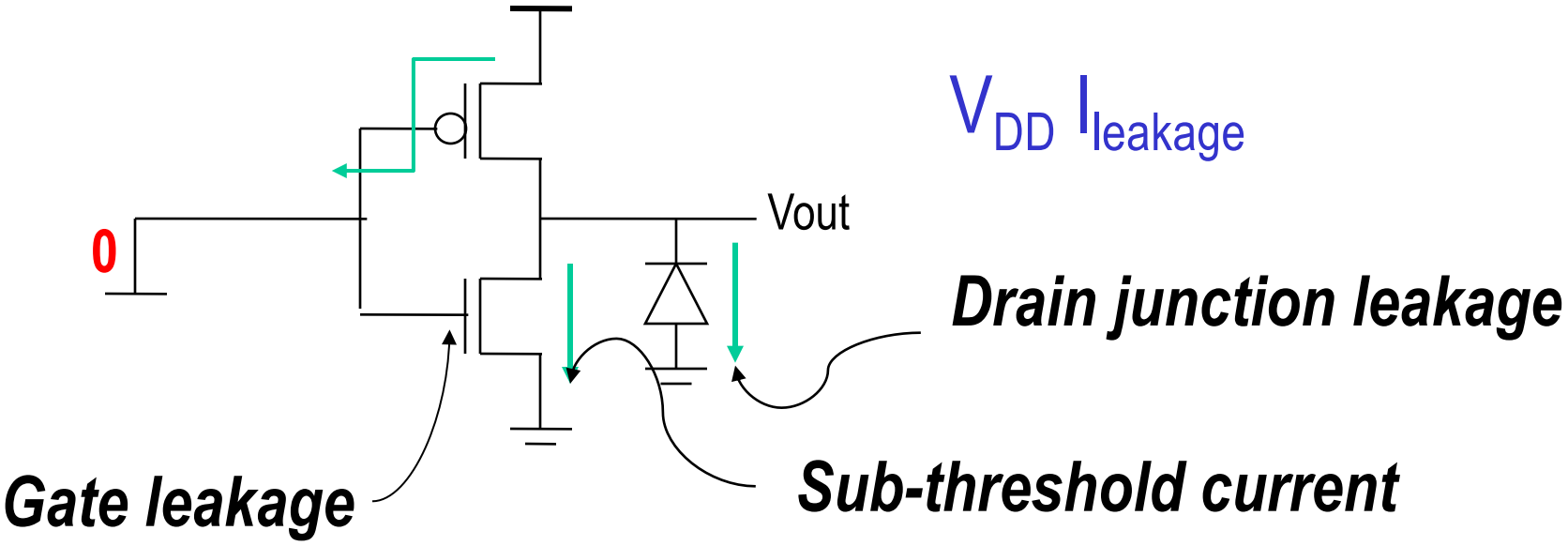
When load capacitance is small (t_{sin}/t_{sout} > 2 for V_{DD} > 2V) the power is dominated by P_{sc}

If $V_{DD} < V_{Tn} + |V_{Tp}|$ then P_{sc} is eliminated since both devices are never on at the same time.

W/L_p = 1.125 μm/0.25 μm
W/L_n = 0.375 μm/0.25 μm
C_L = 30 fF

normalized wrt zero input rise-time dissipation

Leakage (Static) Power Consumption



Sub-threshold current is the dominant factor.
All increase exponentially with temperature!

Technology Scaling Models

- ***Full scaling(constant electrical)***
  - Ideal model –dimensions and voltage scale together by the same factor S
- ***Fixed voltage scaling***
  - Most common model until recently- only dimensions scale, voltages remain constant
- ***General scaling***
  - Most realistic for today's situation-voltages and dimensions scale with different factors

Scaling Relationships for Long Channel Devices

Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
W, L, t_{ox}		1/S	1/S	1/S
V_{DD}, V_T		1/S	1/U	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_L	$C_{ox}WL$	1/S	1/S	1/S
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{av}	$k_{n,p} V^2$	1/S	S/U^2	S
t_p (intrinsic)	$C_L V / I_{av}$	1/S	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S
PDP	$C_L V^2$	$1/S^3$	$1/SU^2$	1/S

Difference between long and short channels

$$I_{Dsat} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$I_D\Big|_{V_{DS}=V_{DSAT}} = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

$$= v_{sat} C_{ox} W (V_{GT} - \frac{V_{DSAT}}{2})$$

Transistor Scaling (velocity-saturated devices)

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
√ *Area*/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	$1/S$	$1/U$	1
Current Density	$I_{sat}/Area$	S	S^2/U	S^2
Ron	V/I_{sat}	1	1	1
√ *Intrinsic Delay*	$R_{on}C_{gate}$	$1/S$	$1/S$	$1/S$
√ P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	$P/Area$	1	S^2/U^2	S^2