Digital Integrated Circuits

Lab 4

Adder Simulation

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Outline

- Lab Contents
- Report Requirements

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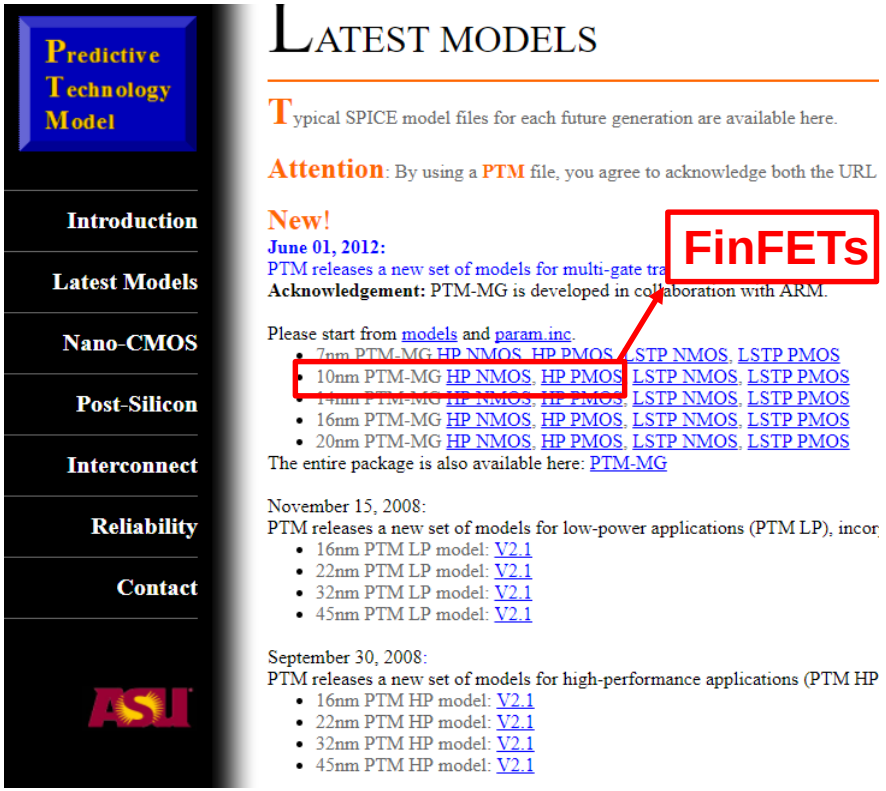
Device Models for Logical Effort Optimizaiton

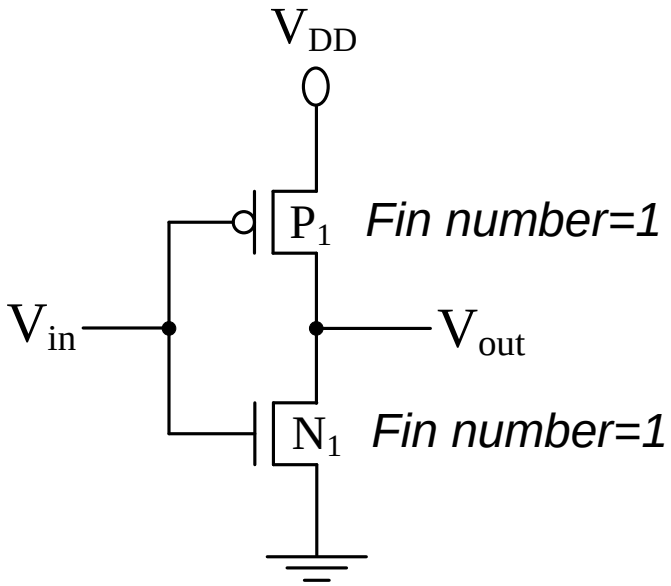
- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 10nm multi-gate (MG) FinFETs
  - PTM link: http://ptm.asu.edu/
  - Use the high-performance (HP) models
  - For both n-channel and p-channel devices



Simulation Settings

- L_g = 14 nm for FinFETs
- Supply voltage is 0.65V for FinFETs
- Simulation temperature
  - T = 25˚C

Minimum sized INV for FinFET

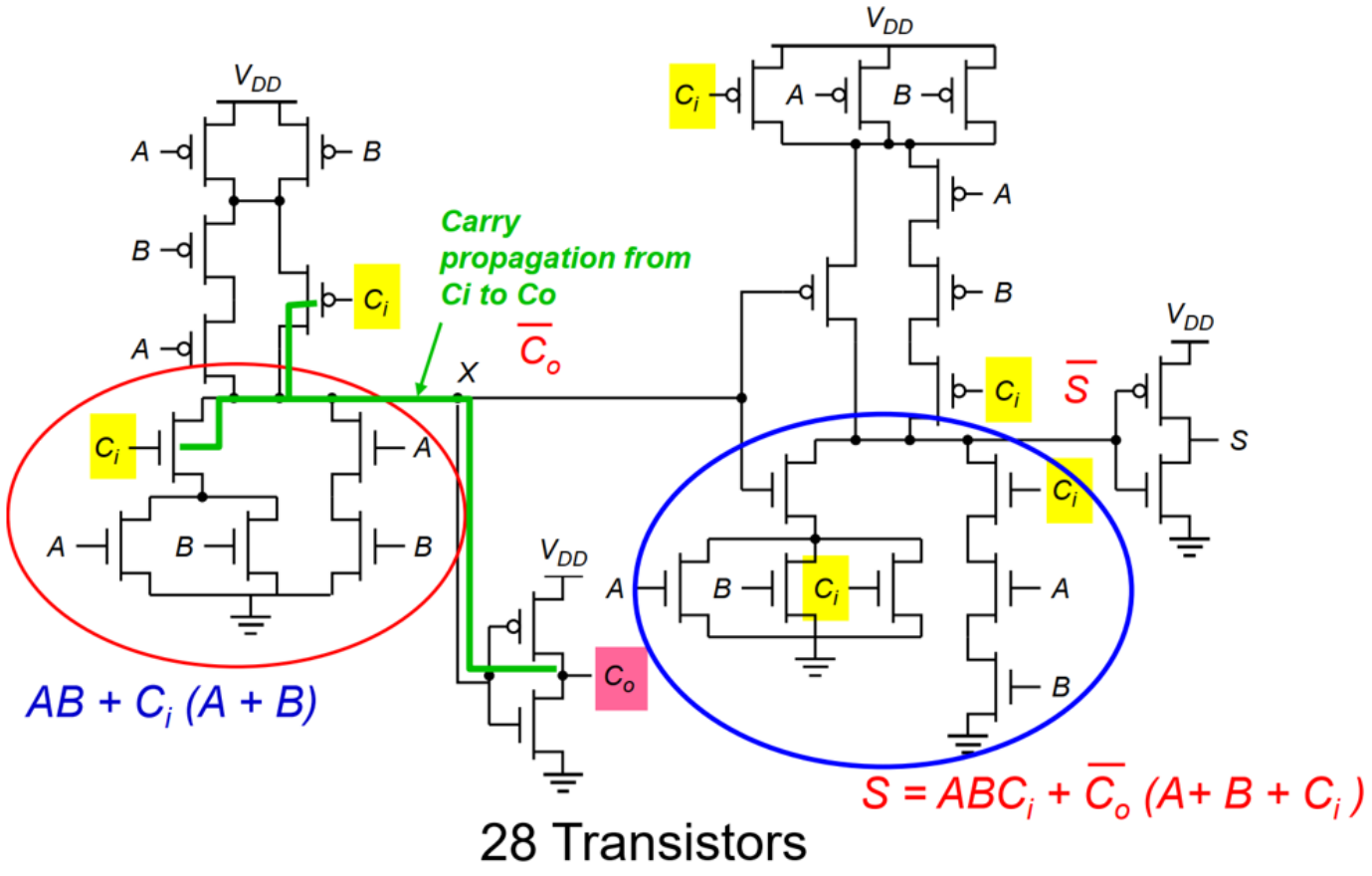


minimum-sized
un-skewed CMOS inverter

Minimum Sized Inv	PMOS	NMOS
Fin number	1	1
L	14n	14n
Design the fin number to ensure balanced driving current in pull-up and pull-down network		

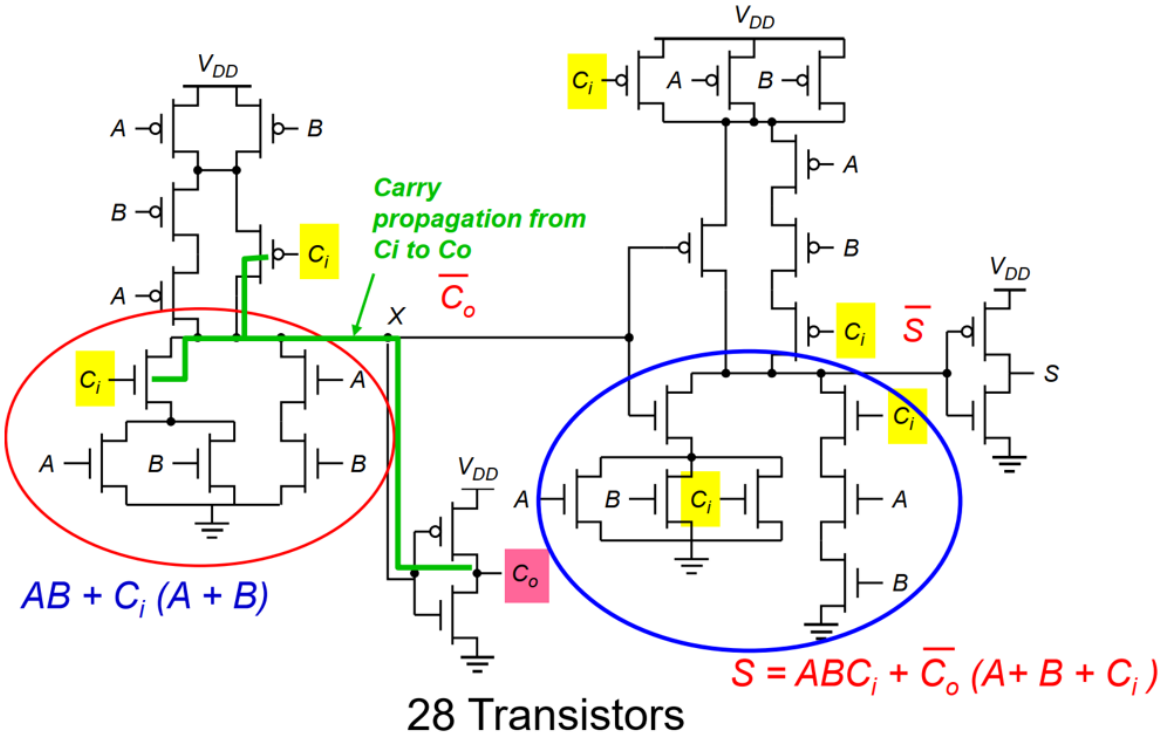
Conventional 28T Adder

- 28T加法器由两部分组成，分别产生进位信号和求和信号
- 进位信号的下拉网络满足逻辑表达式 $AB + C_i$（$A + B$）
- 求和信号下拉网络满足逻辑表达式 $ABC_i + \overline{C_o}$（$A + B + C_i$）



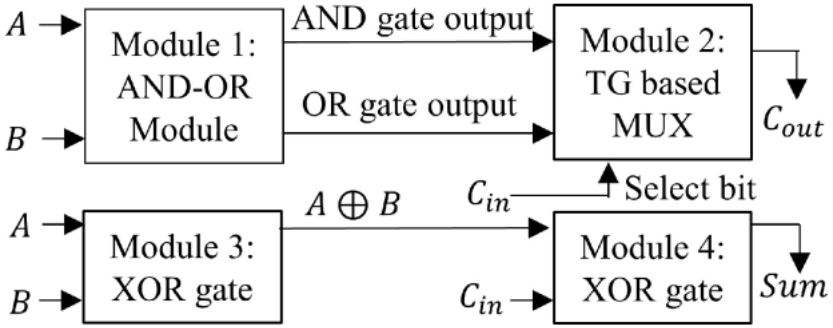
传统28T加法器弊端

- 面积：28T面积开销比较大
- 延迟：进位Cout需要经过两级逻辑门、延迟大
- 功耗：晶体管数量多，内部节点寄生效应较大，功耗大



Hybrid Full Adder-1

- 下图是近年来提出的一种混合型加法器：由互补逻辑，传输管和传输门构成（22T）

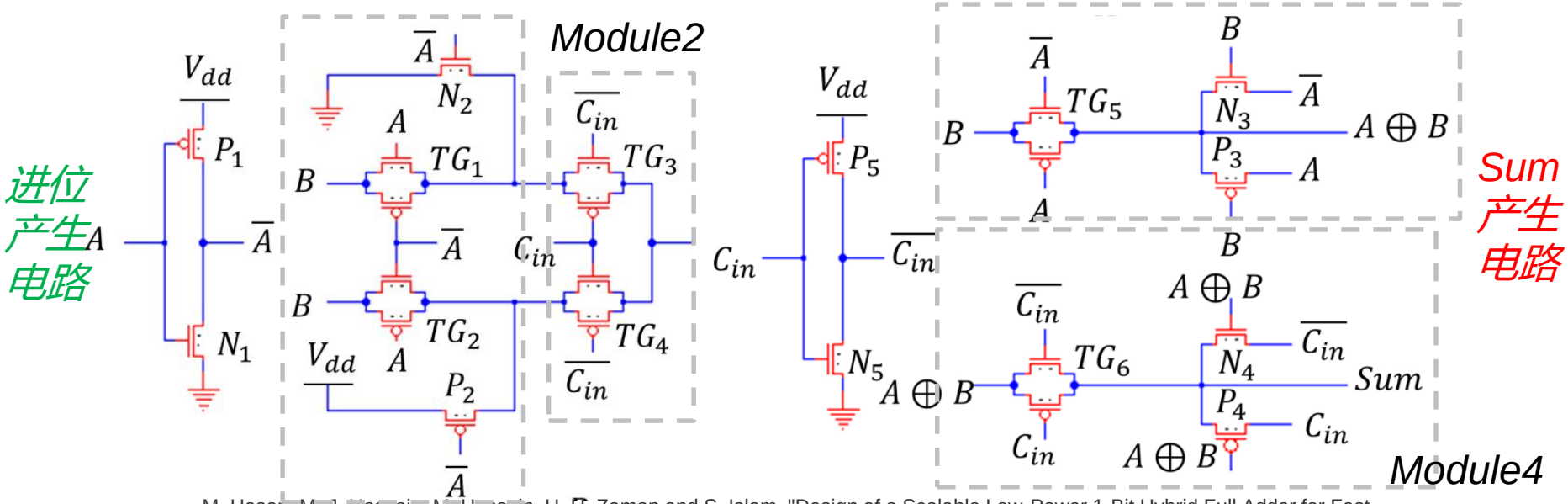


$$C_o = AB\bar{C}i + (A+B)Ci$$

$$S_o = A \oplus B \oplus Ci$$

完成AND/OR 通过 Cin选择AND /OR

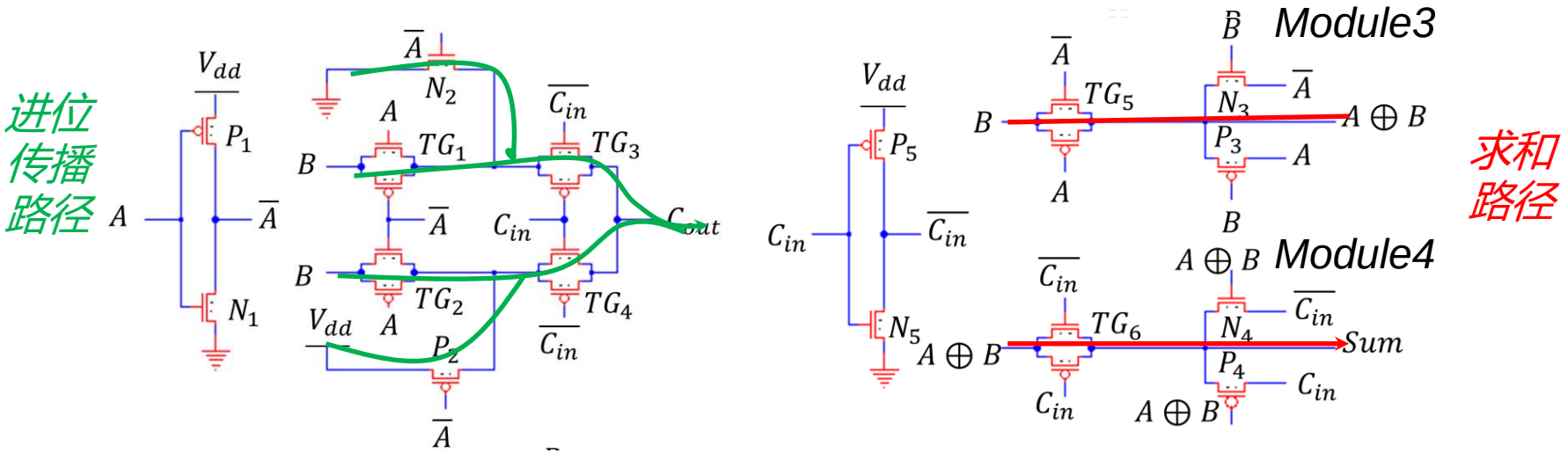
两级XOR 门求解 S



M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1464-1468, Aug. 2020, doi: 10.1109/TCSII.2019.2940558.

Hybrid Full Adder-1优势

- 仅需22T，比传统CMOS全加器（28T）面积更小
- 进位传播路径短 → TG+TP或者TG+TG，速度快
- 相比于传统CMOS全加器 → 管子数量少，总节点寄生电容更小，功耗更低
- 相比于传统的传输管逻辑全加器 → 级联性能更好，无需中间 buffer

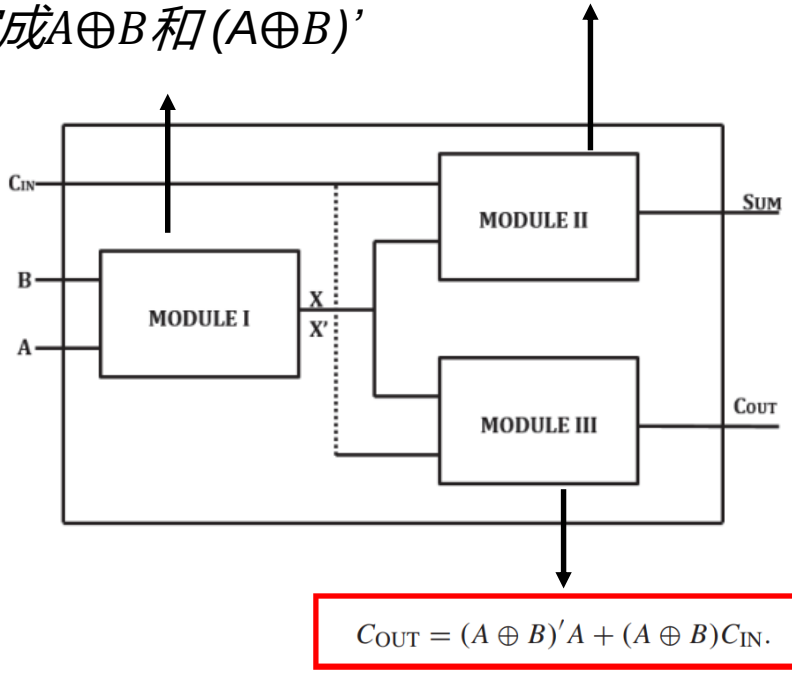


Hybrid Full Adder-2

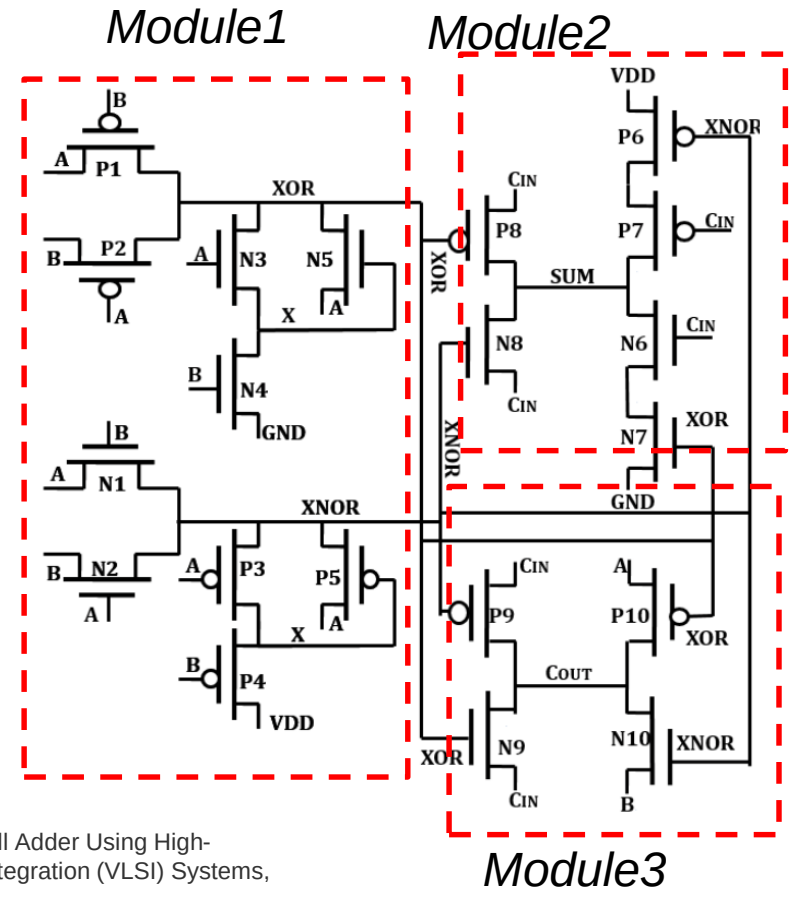
- 下图是第二种混合型全加器：由互补传输管逻辑，传输门逻辑，传输管逻辑和CMOS逻辑组成

$$SUM = (A \oplus B) \oplus C'_{IN} + (A \oplus B)' \oplus C_{IN}.$$

完成A⊕B和(A⊕B)'



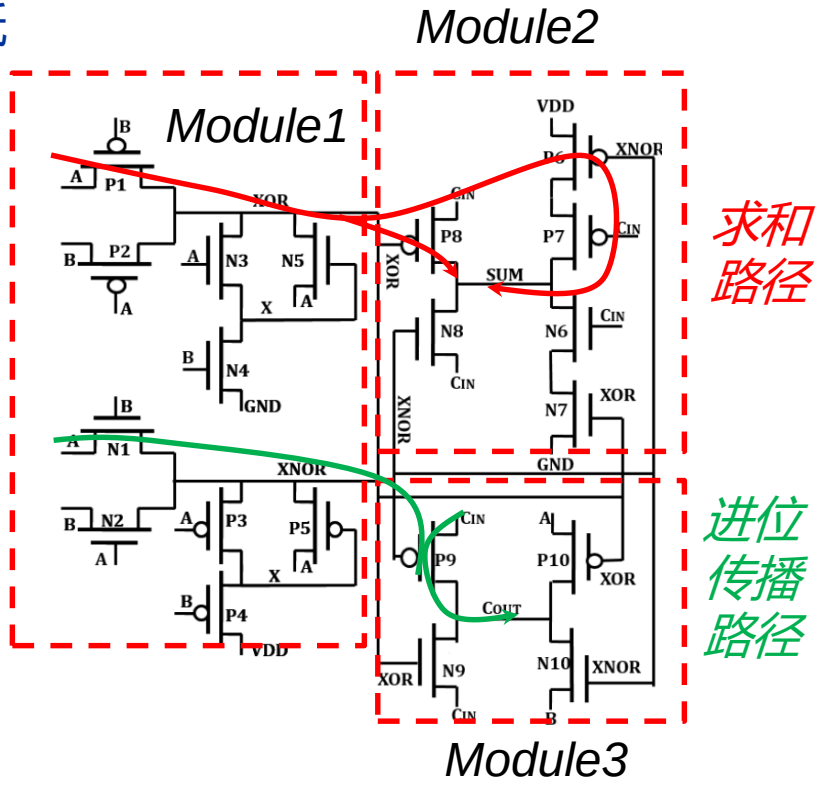
$$C_{OUT} = (A \oplus B)'A + (A \oplus B)C_{IN}.$$



J. Kandpal, A. Tomar, M. Agarwal and K. K. Sharma, "High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 6, pp. 1413-1422, June 2020, doi: 10.1109/TVLSI.2020.2983850.

Hybrid Full Adder-2优势

- 10T XOR-XNOR模块 +4T 进位生成模块 +6T求和生成模块
- 20T面积小
- 求和信号由CMOS逻辑产生，驱动能力强
- 进位传播关键路径短
- 晶体管少，内部节点寄生效应小，功耗低
- 无需反相器对信号取反，延迟和功耗低



Task1: Design a Full Adder

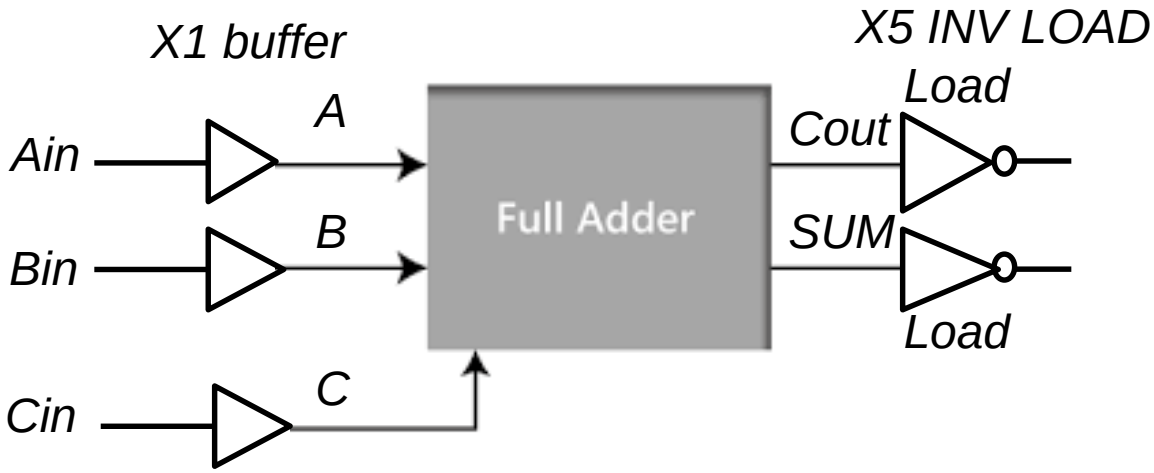
- Choose two to three of full adder structures mentioned in class (28T, majority based adder, transmission gate adder, complementary pass transistor adder and hybrid adder) to simulate
- Verify your adder functionality with the full adder truth table
- Report delay, power, and area measurement of your full adder

A	B	CIN	COUT	SUM
0	1	1	1	0
0	1	0	0	1
0	0	1	0	1
0	0	0	0	0
1	1	1	1	1
1	1	0	1	0
1	0	1	1	0
1	0	0	0	1

NOTE:

- *Area: estimate the area of full-adder roughly by accumulate the area of each single transistor, i.e. ∑ Fin_number*[Width_fin*Lg]*

任务一测量电路



注意：

1、延迟测量为 buffer输出信号到负载输入信号的传播时间

2、功耗测量只包括全加器，不包括负载和 buffer

3、全加器结构为任意选择的两到三种加法器（可以是其他参考文献中提到的结构）

任务一测量要求

- 延迟测量：给出输入到求和信号以及输入到进位信号的传播延迟测量信息，测量数据模式按照实验给出测量

Delay path	Data pattern	Delay path	Data pattern
① A to SUM	000->100	④ C to Cout	100->101
② B to SUM	000->010		010->011
③ C to SUM	000->001		

- 功耗测量使用如下语句测量即可

```
VA A GND PULSE (0 0.65 2N 50p 50p 4n 8n)
VB B GND PULSE (0 0.65 2N 50p 50p 2n 4n)
VC C GND PULSE (0 0.65 2N 50p 50p 1n 2n)

.measure  tran Power AVG "abs(I(VDD)*V(VDD))" FROM=1ns TO=9ns
```

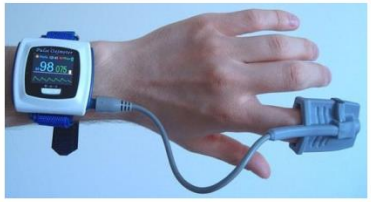
人工智能和深度学习应用









Cloud AI

Big data training

Big models

>1kW

Fast response

~100W

Critical performance

~10W

~100 billions of devices

- Low power
- Low latency
- Low cost

<1W

Edge AI

Source: ISSCC'20 14.3

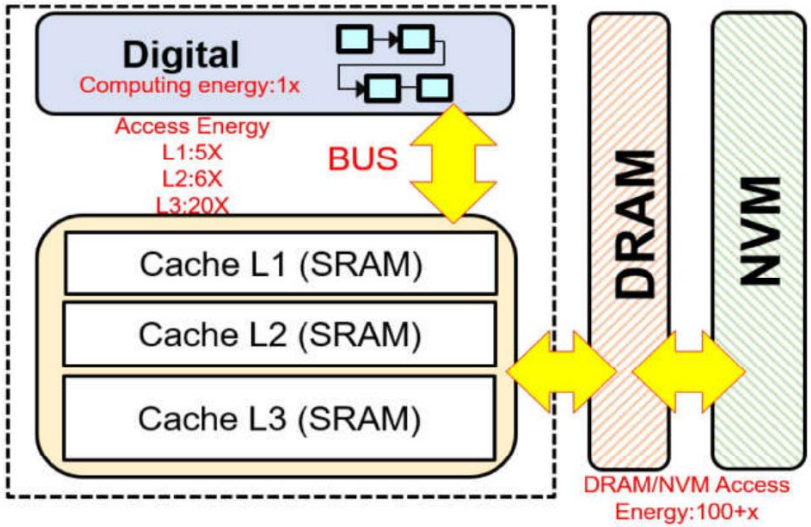
传统智能应用部署在边缘端，支持低能耗，低延迟以及低成本的智能计算是要点

Yue, Jinshan et al. "14.3 A 65nm Computing-in-Memory-Based CNN Processor with 2.9-to-35.8TOPS/W System Energy Efficiency Using Dynamic-Sparsity Performance-Scaling Architecture and Energy-Efficient Inter/Intra-Macro Data Reuse." *2020 IEEE International Solid- State Circuits Conference - (ISSCC)* (2020): 234-236.

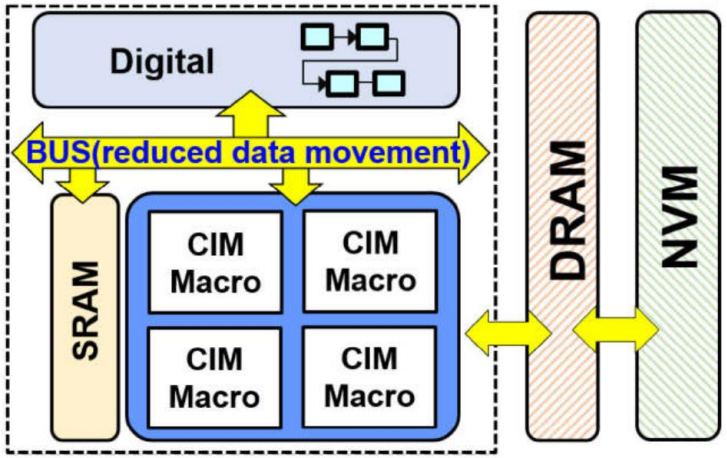
Background of In-Memory Computing

- Artificial intelligence (AI) and machine learning (ML) are widely used in many cognitive tasks
- Requirement for AI accelerator in edge applications : low power, low latency, low cost
- **In-Memory Computing (IMC)** is a new architecture for reducing the energy/latency by massively parallel energy-efficient MAC operation

Traditional CNN Accelerator



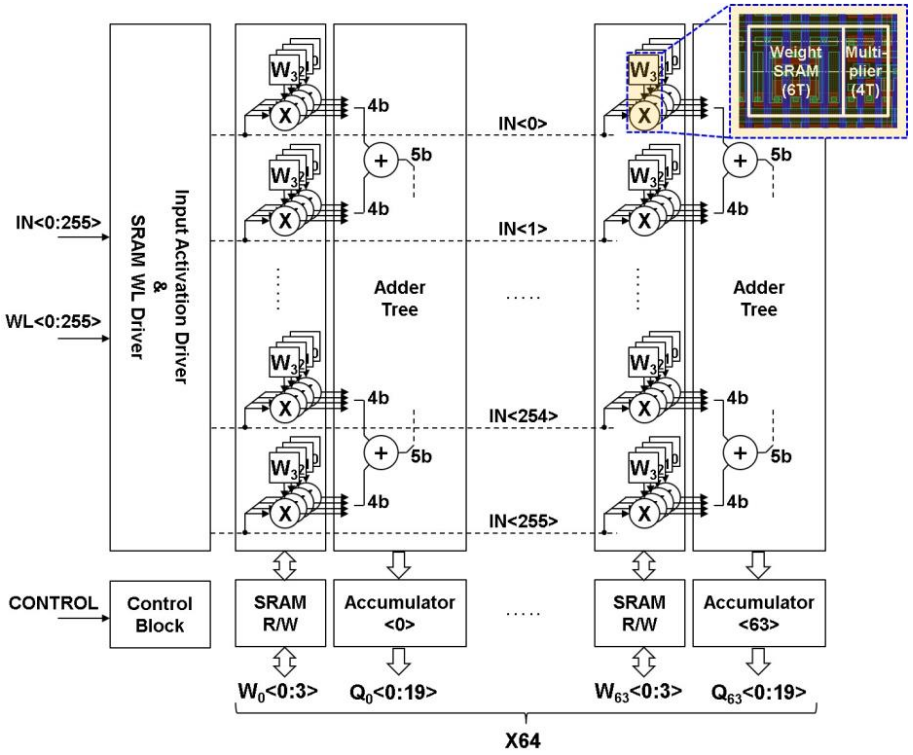
IMC-based CNN Accelerator



X. Si et al., "15.5 A 28nm 64Kb 6T SRAM Computing-in-Memory Macro with 8b MAC Operation for AI Edge Chips," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), 2020, pp. 246-248, doi: 10.1109/ISSCC19947.2020.9062995.

Background of IMC - Architecture

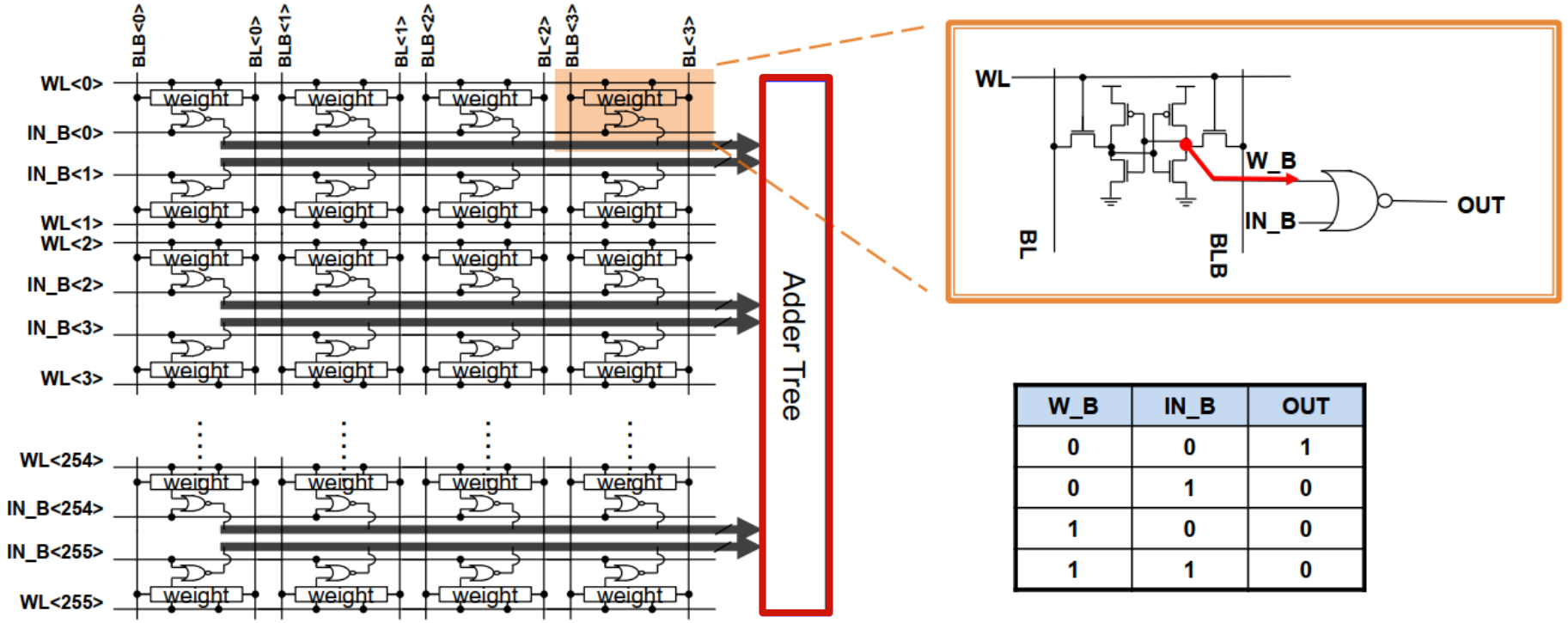
- Using memory array and computing logic gate to complete basic MAC operations
- Weights are stored in SRAM, inputs are fed into SRAM array
- Bit-wise multiplications are finished by single logic gate
- Adder-tree based accumulators accumulate bit-wise multiplication results



Y.-D. Chih, P.-H. Lee, H. Fujiwara et al., "16.4 An 89TOPS/W and 16.3TOPS/mm2 All-Digital SRAM-Based Full-Precision Compute-In Memory Macro in 22nm for Machine-Learning Edge Applications," IEEE International Solid- State Circuits Conference (ISSCC), pp. 252-254, Febrary 2021.

Background IMC – MAC operation

- Insert NOR gate and **adder tree** into SRAM array to realize multiplication and accumulation (MAC) operations
- Support 1b-input and 4b-weight MAC operation within one cycle.

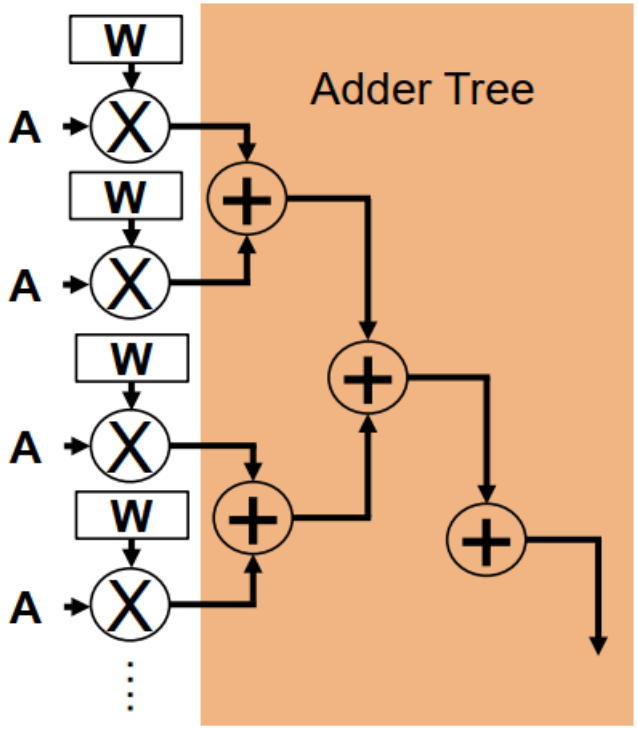


W_B	IN_B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Y.-D. Chih, P.-H. Lee, H. Fujiwara et al., "16.4 An 89TOPS/W and 16.3TOPS/mm2 All-Digital SRAM-Based Full-Precision Compute-In Memory Macro in 22nm for Machine-Learning Edge Applications," IEEE International Solid- State Circuits Conference (ISSCC), pp. 252-254, Febrary 2021.

Background of IMC – Adder Tree

- Hardware requirement for accumulation of 256 “4bit inputs x 4bits signed/unsigned weight” with 1-bit serial multiply



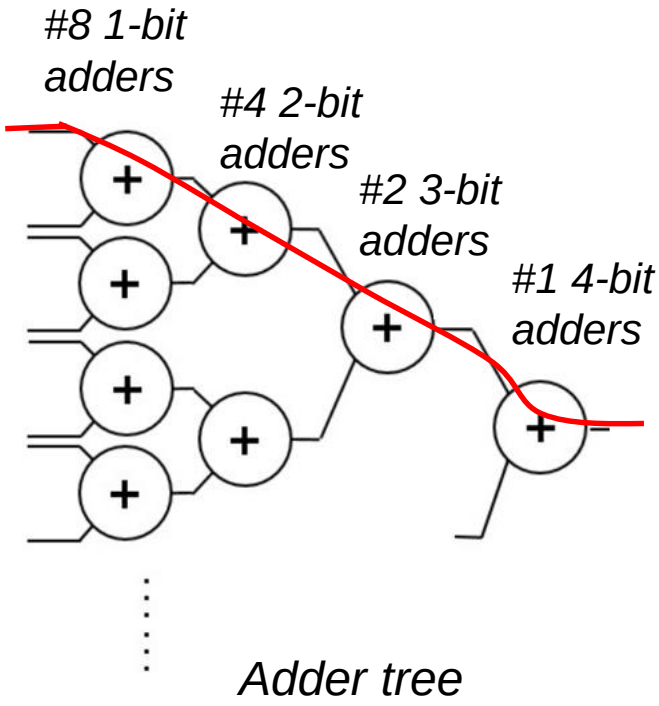
Adder Type	Number
5 bits adder	128
6 bits adder	64
7 bits adder	32
8 bits adder	16
9 bits adder	8
10 bits adder	4
11 bits adder	2
12 bits adder	1

Y.-D. Chih, P.-H. Lee, H. Fujiwara et al., "16.4 An 89TOPS/W and 16.3TOPS/mm2 All-Digital SRAM-Based Full-Precision Compute-In Memory Macro in 22nm for Machine-Learning Edge Applications," IEEE International Solid- State Circuits Conference (ISSCC), pp. 252-254, Febrary 2021.

Task2(optional): Design an Adder Tree

- Construct an adder tree to accumulate 16*1b unsigned input to 1*4b unsigned output
- You can choose different full adder structures
- Report latency of critical path （from data input to the 4 bits adder final carry out）

Adder Type	Number
1 bits adder	8
2 bits adder	4
3 bits adder	2
4 bits adder	1



任务二测量要求

- 延迟测量数据模式：

初始数据 16 bit 输入 (1111 1111 1111 1110) → 16 bit 输入 (1111 1111 1111 1111)

- 加法树输入(所有1 bit adder) 均加经过1X buffer，输出(4 bit adder) 均加上5X INV_load，延迟测量为buffer输出到最终进位输出

- 输入激励的特性按照左侧表格给定

Metrics	Value
V1	0V
V2	0.65v
Delay Time	1ns
Raise Time	50ps
Fall Time	50ps

Outline

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Report Requirement

- The report may include:
  - Lab procedures (e.g., screenshots of the critical steps)
  - Lab results (e.g., area, delay and power measurement, screenshots of simulation waveforms)
  - Observations and conclusions

Submission

- You need to submit your report
  - Name of report (in PDF format): lab4_report_[Name]_[Student No.].pdf

- Please upload your report to Canvas course website

- Submission of Lab 4 report will be due on 6th January