# Digital Integrated Circuits

# Lab 3

# Review

**Dr. Yanan Sun**

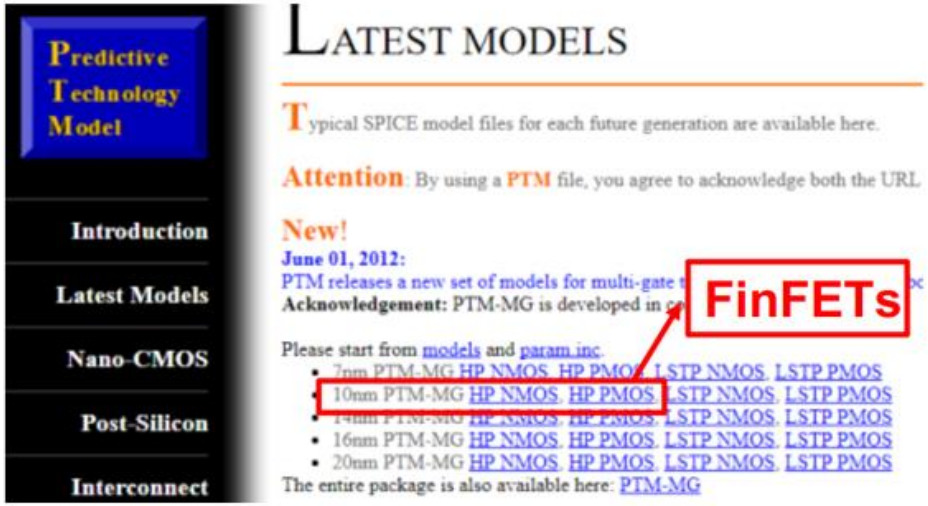
Email: sunyanan@sjtu.edu.cn

Office: Rm 414, Building of Microelectronics

# Device Models for Inverter Simulation

- Use the Predictive Technology Model (PTM) to evaluate 10nm multi-gate (MG) FinFETs

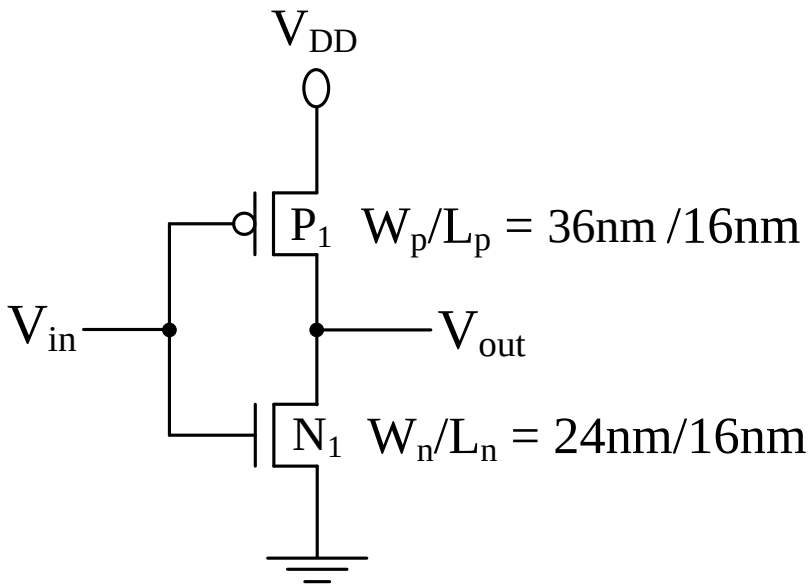
  - PTM link: http://ptm.asu.edu/
  - Use the high-performance (HP) models
  - For both n-channel and p-channel devices



# Simulation Settings

- $L_g$ = 14 nm for FinFETs
- Supply voltage is 0.65V for FinFETs
- Simulation temperature
  - T = 25˚C

# Minimum sized INV for FinFET




minimum-sized
un-skewed CMOS inverter

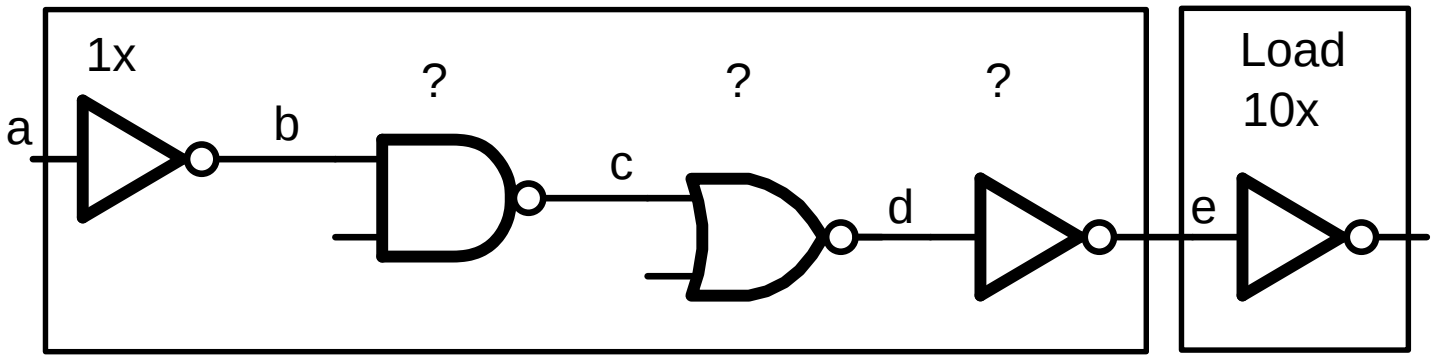
| Minimum Sized Inv | PMOS | NMOS |
|---|---|---|
| Fin number | 1 | 1 |
| L | 14n | 14n |
| Design the fin number to ensure balanced driving current in pull-up and pull-down network | | |

# Task1: Use Logical Effort to Size Gates

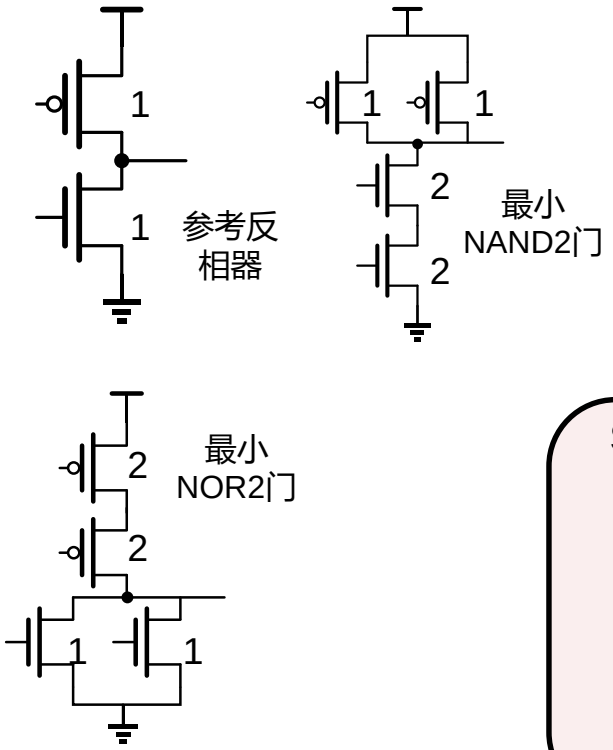
- Size each transistor in the circuit below properly to optimize the speed for FinFET, and construct the circuit with HSPICE

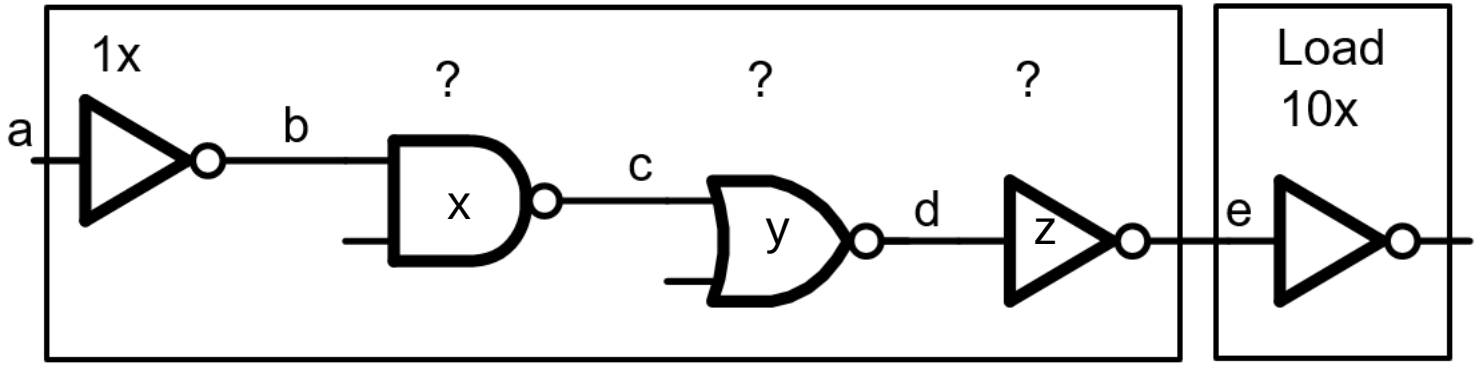
| Vpulse | Value |
|---|---|
| V1 | 0V |
| V2 | 0.65v |
| Delay Time | 1ns |
| Raise Time | 50ps |
| Fall Time | 50ps |
| Pulse Width | 1ns |
| Period | 2ns |

Size the logic gate to minimize the propogation delay (a to e)



# 理论计算FinFET逻辑链路最优延迟




| stage | 1 | 2 | 3 | 4 | | |
|---|---|---|---|---|---|---|
| g | $g_1=1$ | $g_2=3/2$ | $g_3=3/2$ | $g_4=1$ | ⟹ | G=1.5*1.5 |
| b | $b_1=1$ | $b_2=1$ | $b_3=1$ | $b_4=1$ | ⟹ | B=1 |
| f | $f_1=x/1$ | $f_2=y/x$ | $f_3=z/y$ | $f_4=10/z$ | ⟹ | F=10 |

$h_i = g_i f_i b_i$

$h_{opt} = H^{1/4} = (GBF)^{1/4}$

$= (10*1.5*1.5)^{1/4} = 2.18$

$f_1 = 2.18 ; f_2 = 1.45 ; f_3 = 1.45 ; f_4 = 2.18$

x=2.18 ⟹

y=3.16 ⟹

z=4.58 ⟹

| Gate | Size |
|---|---|
| NAND2 | 1.45X |
| NOR2 | 2.11X |
| INV | 4.58X |

$2.18*\frac{2}{3}$

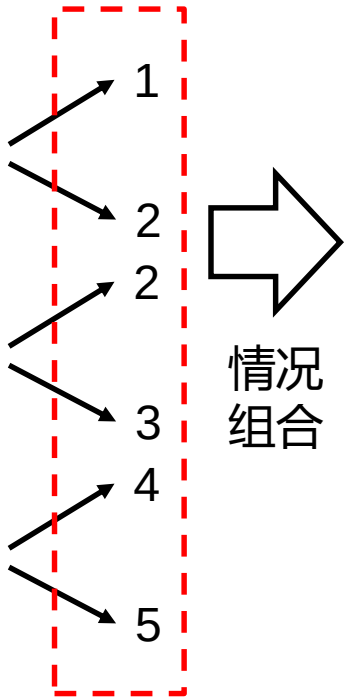
$4.58*\frac{2}{2}$

这里求出来的size为逻辑门相对于最小逻辑门的相对尺寸

# 考虑FinFet中Fin number取整

由于fin_number只能为整数，
所以逻辑门尺寸取整

| Gate | Size |
|---|---|
| NAND2 | 1.45X |
| NOR2 | 2.11X |
| INV | 4.58X |



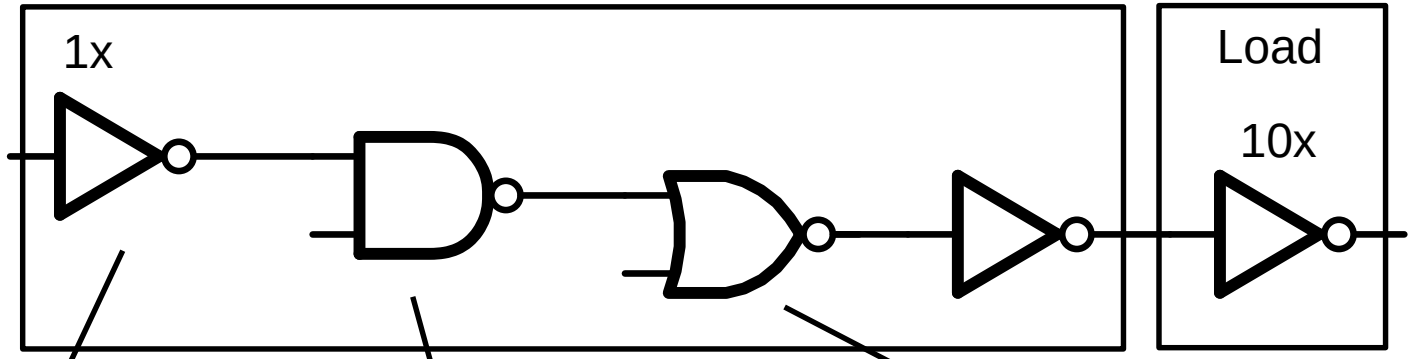

情况组合

| NAND2相对于最小与门尺寸 | NOR2相对于最小或门尺寸 | INV相对于最小反相器尺寸 |
|---|---|---|
| 1 | 2 | 4 |
| 1 | 2 | 5 |
| 1 | 3 | 4 |
| 1 | 3 | 5 |
| 2 | 2 | 4 |
| 2 | 2 | 5 |
| 2 | 3 | 4 |
| 2 | 3 | 5 |

| h1 | h2 | h3 | h4 | $\sum_{i=1}^{4} h_i$ |
|---|---|---|---|---|
| 1.5 | 3 | 2 | 2.5 | 9 |
| 1.5 | 3 | 2.5 | 2 | 9 |
| 1.5 | 4.5 | 1.33 | 2.5 | 9.8 |
| 1.5 | 4.5 | 1.67 | 2 | 9.67 |
| 3 | 1.5 | 2 | 2.5 | 9 |
| 3 | 1.5 | 2.5 | 2 | 9 |
| 3 | 2.25 | 1.33 | 2.5 | 9.18 |
| 3 | 2.25 | 1.67 | 2 | 8.92 |

***得到逻辑门尺寸后，进一步搭建和仿真电路***

# FinFET逻辑链路搭建与仿真




```
.subckt INV IN OUT SIZE=K

Xpfet out in vdd vdd PFET l=lg NFIN="1*SIZE"
Xnfet out in gnd gnd NFET l=lg NFIN="1*SIZE"

.ends
```

```
.subckt NAND A B OUT SIZE=K

Xpfet1 out B VDD VDD PFET l=lg NFIN="1*SIZE"
Xpfet2 out A VDD VDD PFET l=lg NFIN="1*SIZE"
Xnfet1 out B K1 gnd NFET l=lg NFIN="2*SIZE"
Xnfet2 K1 A  gnd gnd NFET l=lg NFIN="2*SIZE"

.ends
```

```
.subckt NOR A B OUT SIZE=K

Xpfet1 out B K1  VDD PFET l=lg NFIN="2*SIZE"
Xpfet2 K1  A VDD VDD PFET l=lg NFIN="2*SIZE"
Xnfet1 out B gnd gnd NFET l=lg NFIN="1*SIZE"
Xnfet2 out A gnd gnd NFET l=lg NFIN="1*SIZE"

.ends
```

```
XINV_S1 A B  INV SIZE="1"

XNAND_S2 B VDD C  NAND SIZE="F2"

XNOR_S3 C GND D   NOR SIZE="F3"

XINV_S4 D E INV SIZE="F4"

XINV_LOAD E OUT  INV SIZE=10
```

## 测量语句：

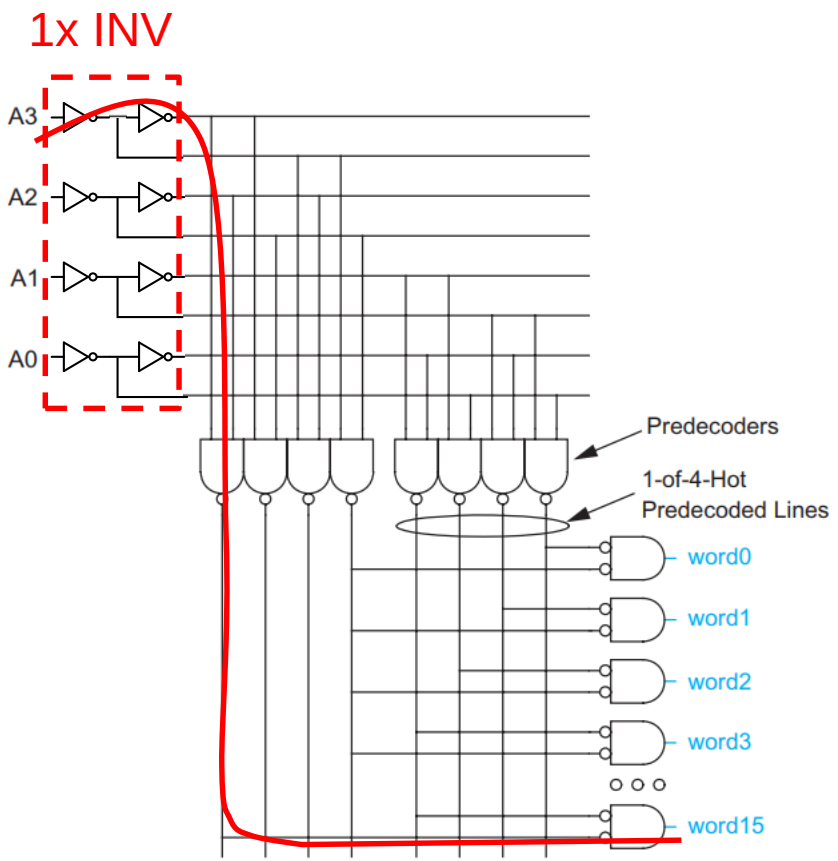
```
.measure TRAN TAH_HL trig v(A)="supply*0.5" RISE=1 targ V(E)= "supply*0.5" RISE=1
.measure TRAN TAH_LH trig v(A)="supply*0.5" fall=1 targ V(E)= "supply*0.5" FALL=1

.MEASURE TRAN TAH PARAM="(TAH_HL+TAH_LH)/2"
```

# 路径优化参考答案

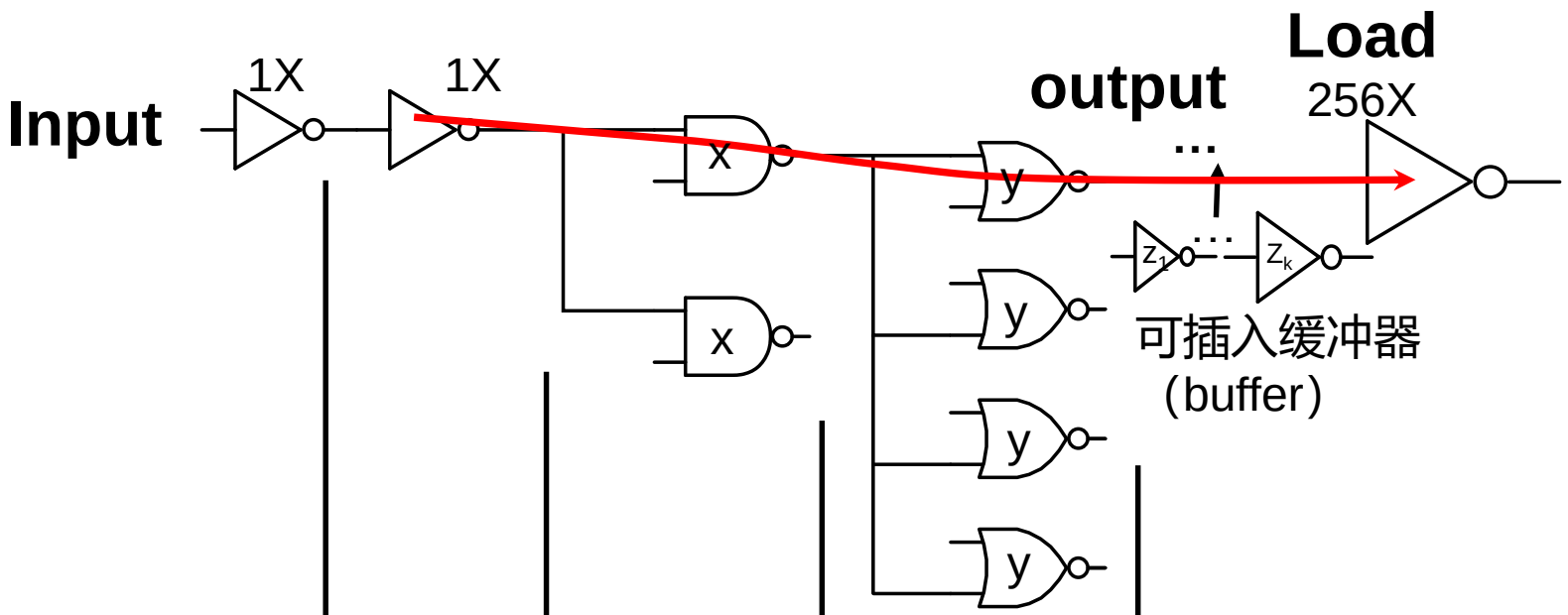
| 与非门尺寸 | 或非门尺寸 | 反相器尺寸 | 测量延迟（s） |
|---|---|---|---|
| 1 | 2 | 4 | 1.568e-11 |
| 1 | 2 | 5 | 1.576e-11 |
| 1 | 2 | 4 | 1.624e-11 |
| 1 | 3 | 5 | 1.622e-11 |
| 2 | 2 | 4 | 1.741e-11 |
| 2 | 2 | 5 | 1.748e-11 |
| 2 | 3 | 4 | 1.749e-11 |
| 2 | 3 | 5 | 1.746e-11 |

# Task2: Use Logical Effort to Optimize 4x16 Decoder

- For a 4x16 decoder, optimize the critical path to minimize the propagation delay of decoder
  - Use the logical effort method
  - Assume that the input inverter/buffer is minimum sized
  - Assume that each output of decoder has a load of 256X minimum sized Finfet inverter
  - You can insert buffer at the output if necessary



# 关键路径分析




H=GBF
G=1*3/2*3/2=9/4
B=2*4=8
F=256
H=4608

| stage | 1 | 2 | 3 | ... | N |
|---|---|---|---|---|---|
| g | 1 | 3/2 | 3/2 | ... | 1 |
| b | 2 | 4 | 1 | ... | 1 |
| f | x/1 | y/x | $z_1$/y | ... | $256/z_k$ |
| h | 2x | 6y/x | $3z_1/2y$ | | $256/z_k$ |

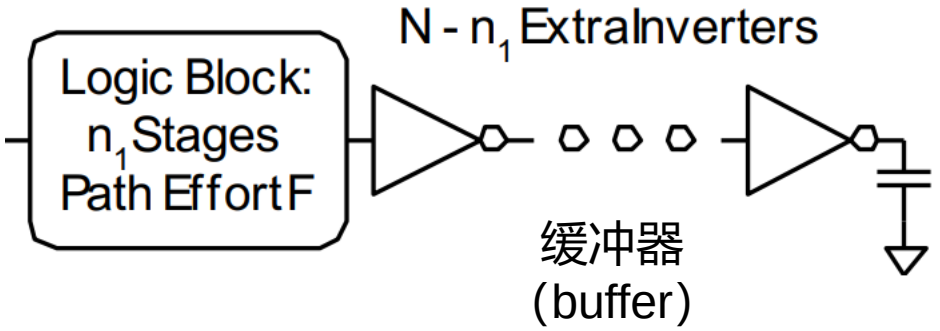
# 最优反相器级数推导

$$D = NH^{\frac{1}{N}} + \sum_{i=1}^{n_1} p_i + (N - n_1)p_{inv}$$

$$\frac{\partial D}{\partial N} = -H^{\frac{1}{N}} \ln H^{\frac{1}{N}} + H^{\frac{1}{N}} + p_{inv} = 0$$

$$h = H^{\frac{1}{N}}$$

$$h(1 - \ln h) + p_{inv} = 0$$



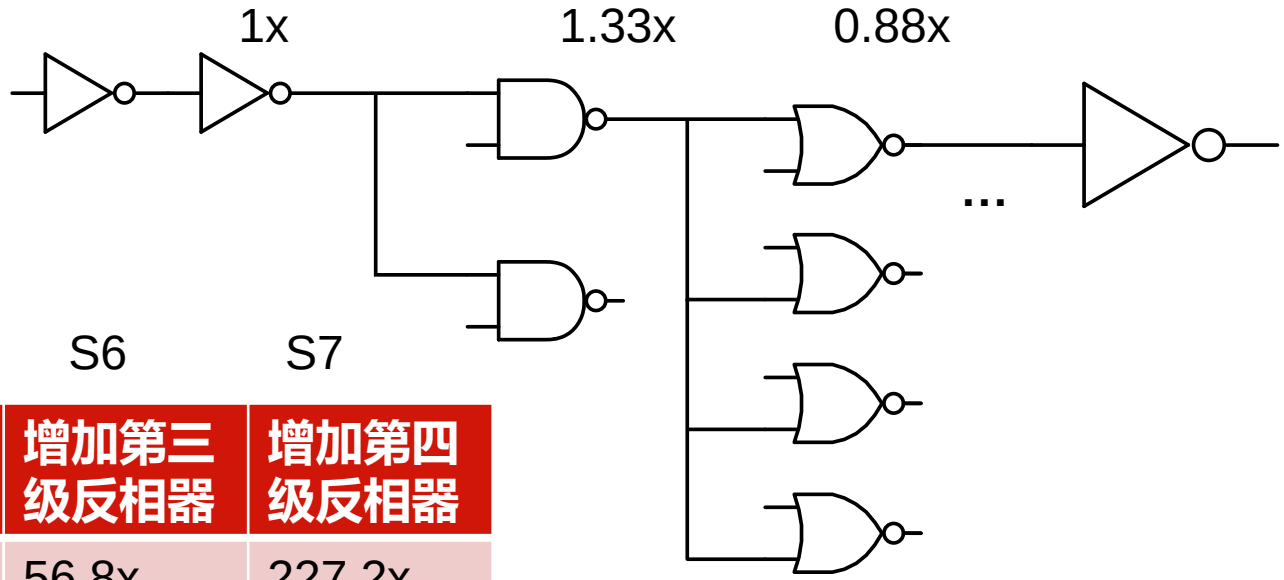

一般的， pinv = 1,可以解得 h= 3.59 ，取h=4，所以 N=$log_4 H$

**实验中 H=4608，N= $log_4 4608 = 6.08$，N可以取6或者7(不包含一级反相器，N从第二级反相器开始计算)。由于$n_1$=3，缓冲器中反相器最优级数为偶数，N可以取7，缓冲器中反相器级数取4。**

# 逻辑链路优化

- 当计算得到最优级数和h后，继续计算每一级逻辑门相对于对应最小逻辑门的尺寸
- 当h=4时，NAND门尺寸为1.33x,NOR门尺寸为0.88x
- 紧接着NOR门之后的缓冲器，第一级反相器尺寸应该为3.55x, 之后的反相器尺寸以4x放大

**注：逻辑链路搭建可以只搭出关键路径，分支路径可以只给出分支的第一个逻辑门，不需要完全搭出**



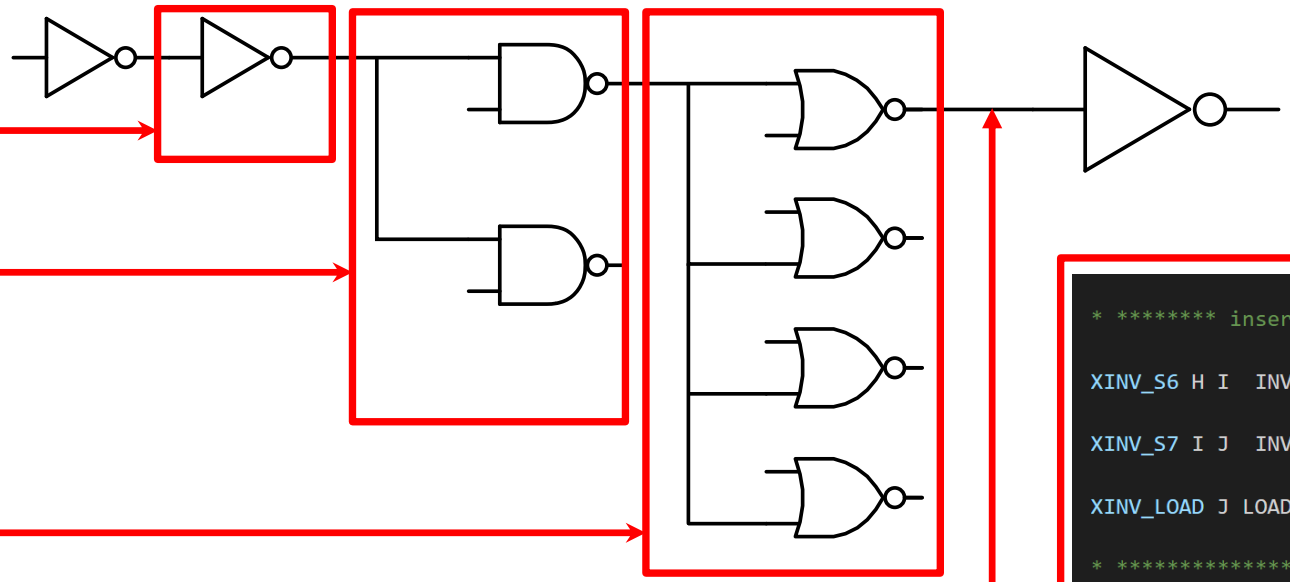

| S1 | S2 | S3 | S4 | S5 | S6 | S7 |
|---|---|---|---|---|---|---|
| 第一级反相器 | 第二级NAND | 第三级NOR | 增加第一级反相器 | 增加第二级反相器 | 增加第三级反相器 | 增加第四级反相器 |
| 1x | 1.33x | 0.88x | 3.55x | 14.2x | 56.8x | 227.2x |

考虑fin_number及逻辑门尺寸取整：

1x 2x 固定为1x 3x 4x 14x 15x 56x 57x 227x 228x

# 逻辑链路搭建与测量 N=7(缓冲器含4级反相器)

```
XINV_S0 A B  INV SIZE="1"

XINV_S1 B C  INV SIZE="1"

XNAND_S2 C VDD E  NAND SIZE="S2"

******** branch *********
XNAND_S2_DMY1 C VDD E0  NAND SIZE="S2"
.........................


XNOR_S3 E GND F   NOR SIZE="1"

******** branch *********
XNOR_S3_DMY1 E GND F0   NOR SIZE="1"

XNOR_S3_DMY2 E GND F1   NOR SIZE="1"

XNOR_S3_DMY3 E GND F2   NOR SIZE="1"
**************************

******** insert buffer1 ******
XINV_S4 F G  INV SIZE="S4"

XINV_S5 G H  INV SIZE="S5"
```



```
* ******** insert buffer2 ******
XINV_S6 H I  INV SIZE="S6"

XINV_S7 I J  INV SIZE="S7"

XINV_LOAD J LOADOUT  INV SIZE=256

* ********************************
```

# 测量结果：插入缓冲器含4级反相器

| S2 | S4 | S5 | S6 | S7 | 延迟（s） |
|---|---|---|---|---|---|
| 1 | 3 | 14 | 56 | 227 | 3.1220E-11 |
| 1 | 3 | 14 | 56 | 228 | 3.1230E-11 |
| 1 | 3 | 14 | 57 | 227 | 3.1230E-11 |
| 1 | 3 | 14 | 57 | 228 | 3.1240E-11 |
| 1 | 3 | 15 | 56 | 227 | 3.1250E-11 |
| 1 | 3 | 15 | 56 | 228 | 3.1260E-11 |
| 1 | 3 | 15 | 57 | 227 | 3.1260E-11 |
| 1 | 3 | 15 | 57 | 228 | 3.1270E-11 |
| 1 | 4 | 14 | 56 | 227 | 3.1010E-11 |
| 1 | 4 | 14 | 56 | 228 | 3.1020E-11 |
| 1 | 4 | 14 | 57 | 227 | 3.1020E-11 |
| 1 | 4 | 14 | 57 | 228 | 3.1030E-11 |
| 1 | 4 | 15 | 56 | 227 | 3.0990E-11 |
| 1 | 4 | 15 | 56 | 228 | 3.1000E-11 |
| 1 | 4 | 15 | 57 | 227 | 3.1000E-11 |
| 1 | 4 | 15 | 57 | 228 | 3.1010E-11 |

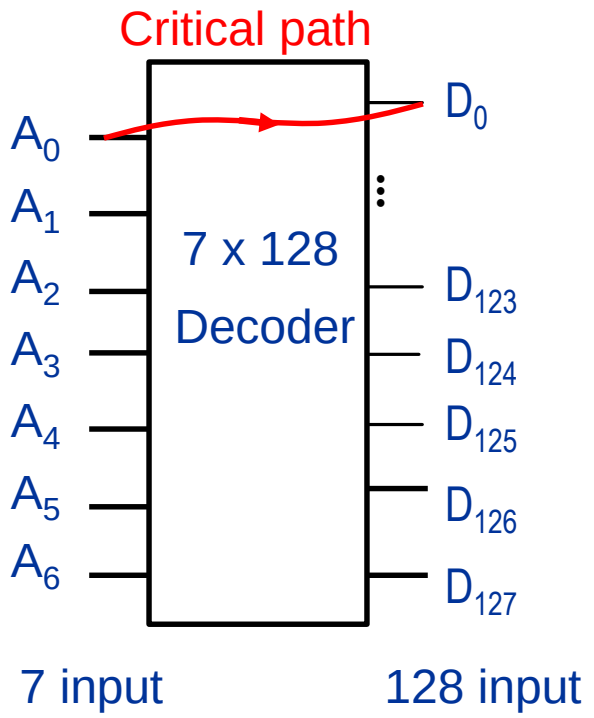
# 测量结果：插入缓冲器含4级反相器

| S2 | S4 | S5 | S6 | S7 | 延迟（s） |
|---|---|---|---|---|---|
| 2 | 3 | 14 | 56 | 227 | 3.1770E-11 |
| 2 | 3 | 14 | 56 | 228 | 3.1780E-11 |
| 2 | 3 | 14 | 57 | 227 | 3.1780E-11 |
| 2 | 3 | 14 | 57 | 228 | 3.1790E-11 |
| 2 | 3 | 15 | 56 | 227 | 3.1800E-11 |
| 2 | 3 | 15 | 56 | 228 | 3.1810E-11 |
| 2 | 3 | 15 | 57 | 227 | 3.1810E-11 |
| 2 | 3 | 15 | 57 | 228 | 3.1820E-11 |
| 2 | 4 | 14 | 56 | 227 | 3.1540E-11 |
| 2 | 4 | 14 | 56 | 228 | 3.1550E-11 |
| 2 | 4 | 14 | 57 | 227 | 3.1550E-11 |
| 2 | 4 | 14 | 57 | 228 | 3.1560E-11 |
| 2 | 4 | 15 | 56 | 227 | 3.1510E-11 |
| 2 | 4 | 15 | 56 | 228 | 3.1520E-11 |
| 2 | 4 | 15 | 57 | 227 | 3.1520E-11 |
| 2 | 4 | 15 | 57 | 228 | 3.1530E-11 |

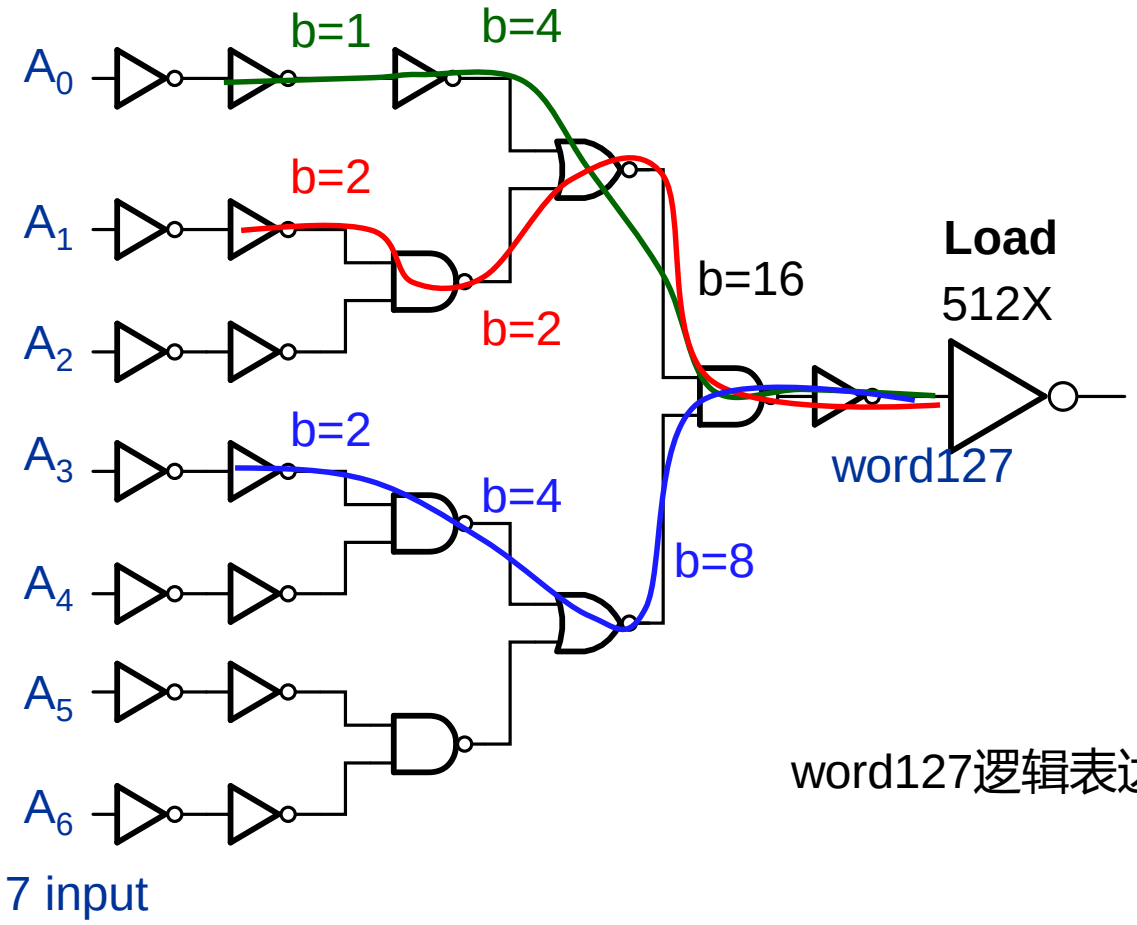
# *Task3 (Optional): Use Logical Effort to Optimize 7x128 Decoder*

- For a 7x128 decoder, first think about the scheme design. Then optimize the critical path to minimize the propagation delay of decoder

  - Use the logical effort method
  - Assume that the input inverter/buffer is minimum sized
  - Assume that each output of decoder has a load of 512X minimum sized Finfet inverter
  - You can insert buffer at the output if necessary



# 关键路径分析




- 可以看到一共有三条不同支路，对于这三条支路，其H1=512*64*1.5*1.5=73728，H2=H3=512*64*1.5*1.5*1.5=110592, 对应的最优化级数为

  N1= $log_4(73728) = 8.08$

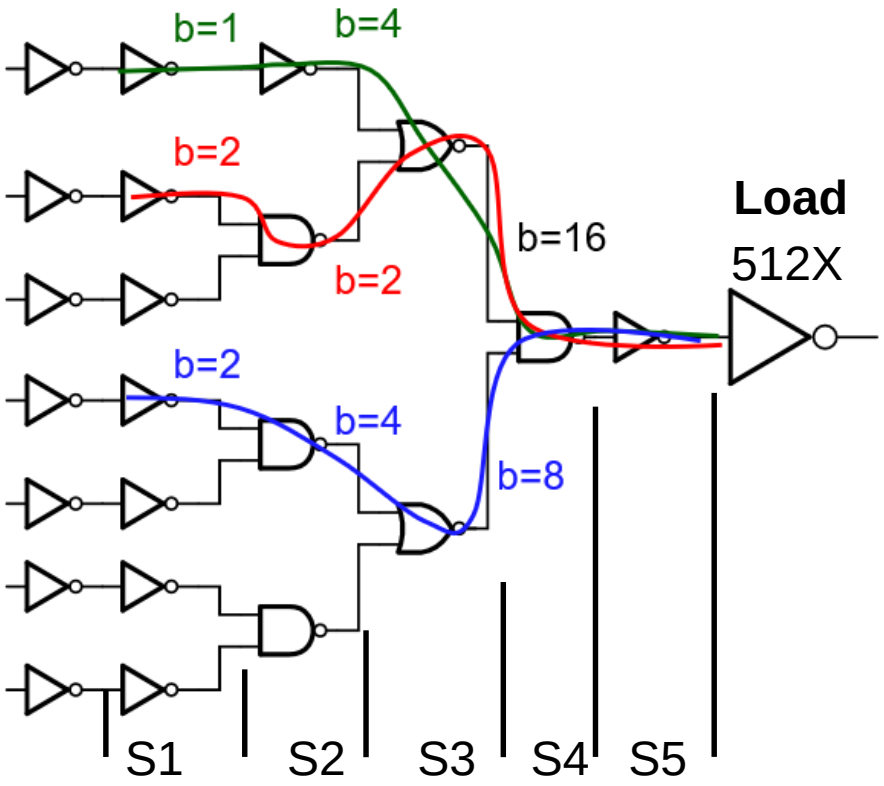
  N2=N3= $log_4(110592) = 8.37$

- **第一条支路延迟低于第二和第三条，因此第二和第三条为关键路径**

- **本次实验分析第二和第三条关键路径，且不考虑第一级反相器后分支**

word127逻辑表达式：$A_0A_1A_2A_3\ A_4A_5\ A_6$

# 考虑第二条支路




固定为1

| S1 | S2 | S3 | S4 | S5 |
|---|---|---|---|---|
| 1x | 1.33x | 1.78x | 0.30x | 1.19x |

| S6 | S7 | S8 | S9 |
|---|---|---|---|
| 4.76x | 19.04x | 76.16x | 304.64x |

插入buffer（含4级反相器）

# 测量结果：插入buffer含2级反相器

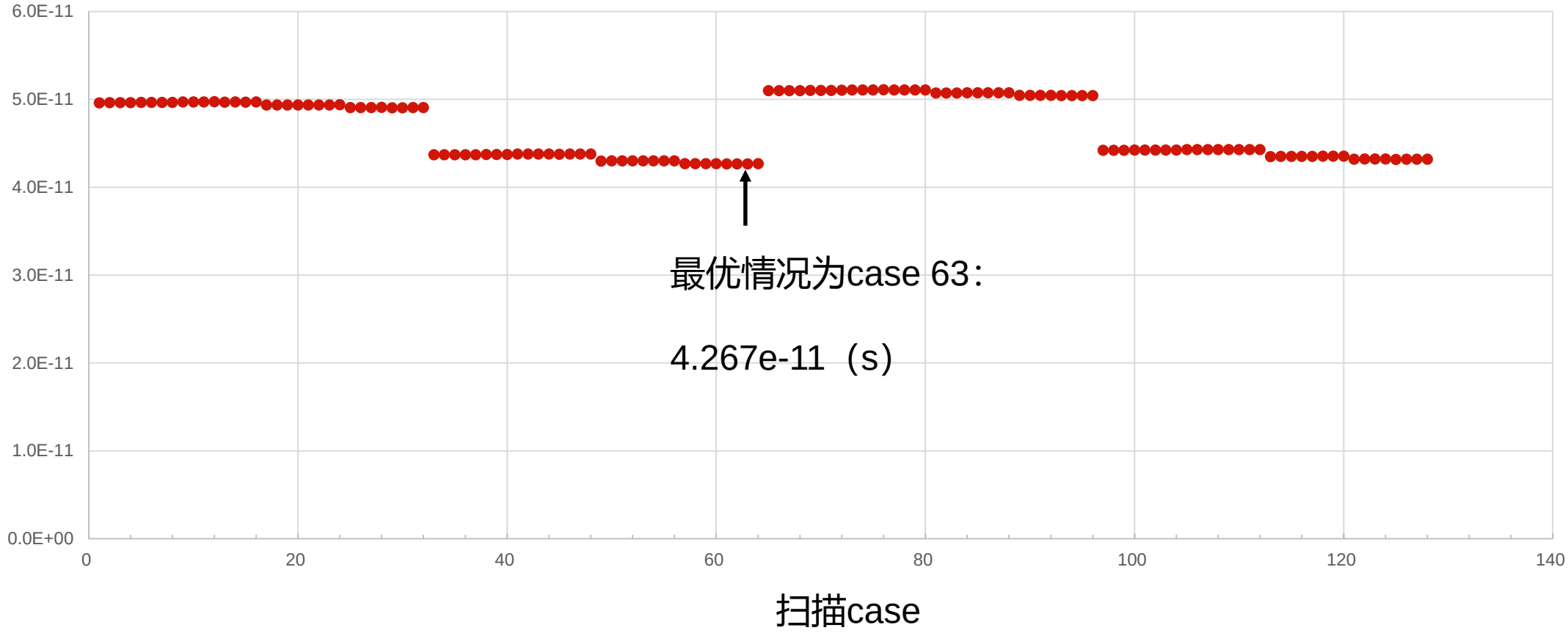
| S2 | S3 | S5 | S6 | S7 | 延迟（s） |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 4 | 19 | 5.9710E-11 |
| 1 | 1 | 1 | 4 | 20 | 5.8910E-11 |
| 1 | 1 | 1 | 5 | 19 | 5.9770E-11 |
| 1 | 1 | 1 | 5 | 20 | 5.8930E-11 |
| 1 | 1 | 2 | 4 | 19 | 5.9450E-11 |
| 1 | 1 | 2 | 4 | 20 | 5.8650E-11 |
| 1 | 1 | 2 | 5 | 19 | 5.9140E-11 |
| 1 | 1 | 2 | 5 | 20 | 5.8290E-11 |
| 1 | 2 | 1 | 4 | 19 | 5.3770E-11 |
| 1 | 2 | 1 | 4 | 20 | 5.2970E-11 |
| 1 | 2 | 1 | 5 | 19 | 5.3830E-11 |
| 1 | 2 | 1 | 5 | 20 | 5.2990E-11 |
| 1 | 2 | 2 | 4 | 19 | 5.3080E-11 |
| 1 | 2 | 2 | 4 | 20 | 5.2280E-11 |
| 1 | 2 | 2 | 5 | 19 | 5.2750E-11 |
| 1 | 2 | 2 | 5 | 20 | 5.1910E-11 |

# 测量结果：插入buffer含2级反相器

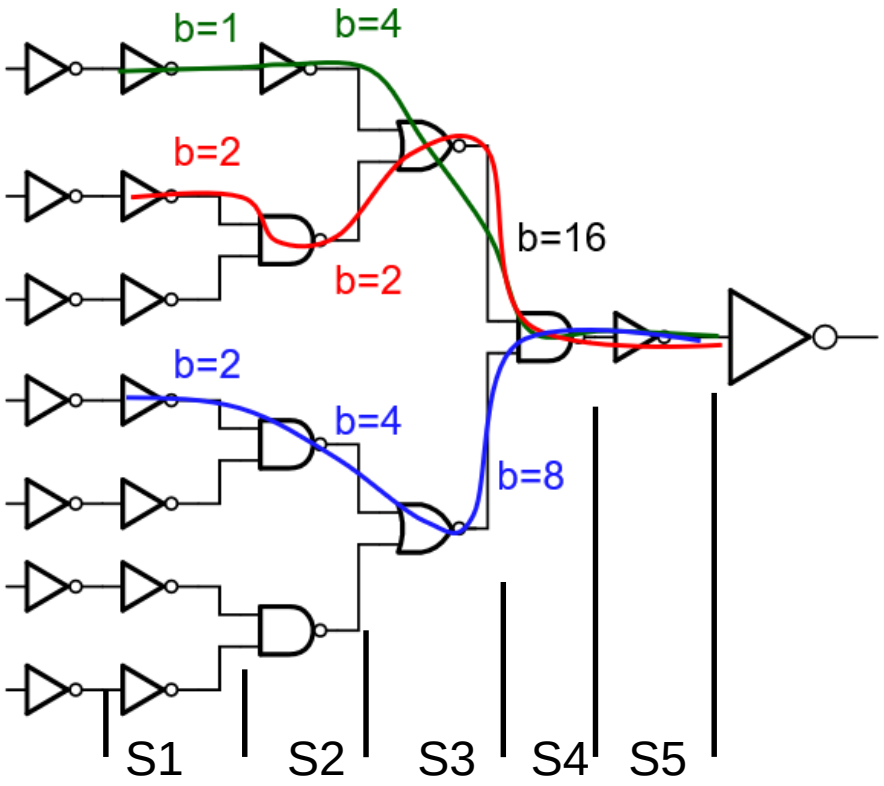
| S2 | S3 | S5 | S6 | S7 | 延迟（s） |
|---|---|---|---|---|---|
| 2 | 1 | 1 | 4 | 19 | 6.1080E-11 |
| 2 | 1 | 1 | 4 | 20 | 6.0280E-11 |
| 2 | 1 | 1 | 5 | 19 | 6.1140E-11 |
| 2 | 1 | 1 | 5 | 20 | 6.0310E-11 |
| 2 | 1 | 2 | 4 | 19 | 6.0830E-11 |
| 2 | 1 | 2 | 4 | 20 | 6.0020E-11 |
| 2 | 1 | 2 | 5 | 19 | 6.0510E-11 |
| 2 | 1 | 2 | 5 | 20 | 5.9670E-11 |
| 2 | 2 | 1 | 4 | 19 | 5.4280E-11 |
| 2 | 2 | 1 | 4 | 20 | 5.3490E-11 |
| 2 | 2 | 1 | 5 | 19 | 5.4340E-11 |
| 2 | 2 | 1 | 5 | 20 | 5.3510E-11 |
| 2 | 2 | 2 | 4 | 19 | 5.3600E-11 |
| 2 | 2 | 2 | 4 | 20 | 5.2790E-11 |
| 2 | 2 | 2 | 5 | 19 | 5.3270E-11 |
| 2 | 2 | 2 | 5 | 20 | 5.2420E-11 |

# 测量结果：插入buffer含4级反相器

| | S2 | S3 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|
| 扫描尺寸结果 | 1X | 2X | 2X | 5X | 20X | 77X | 304X |



# 考虑第三条支路




固定为1　固定为1

| S1 | S2 | S3 | S4 | S5 |
|---|---|---|---|---|
| 1x | 1.33x | 0.88x | 0.30x | 1.19x |

| S6 | S7 | S8 | S9 |
|---|---|---|---|
| 4.76x | 19.04x | 76.16x | 304.64x |

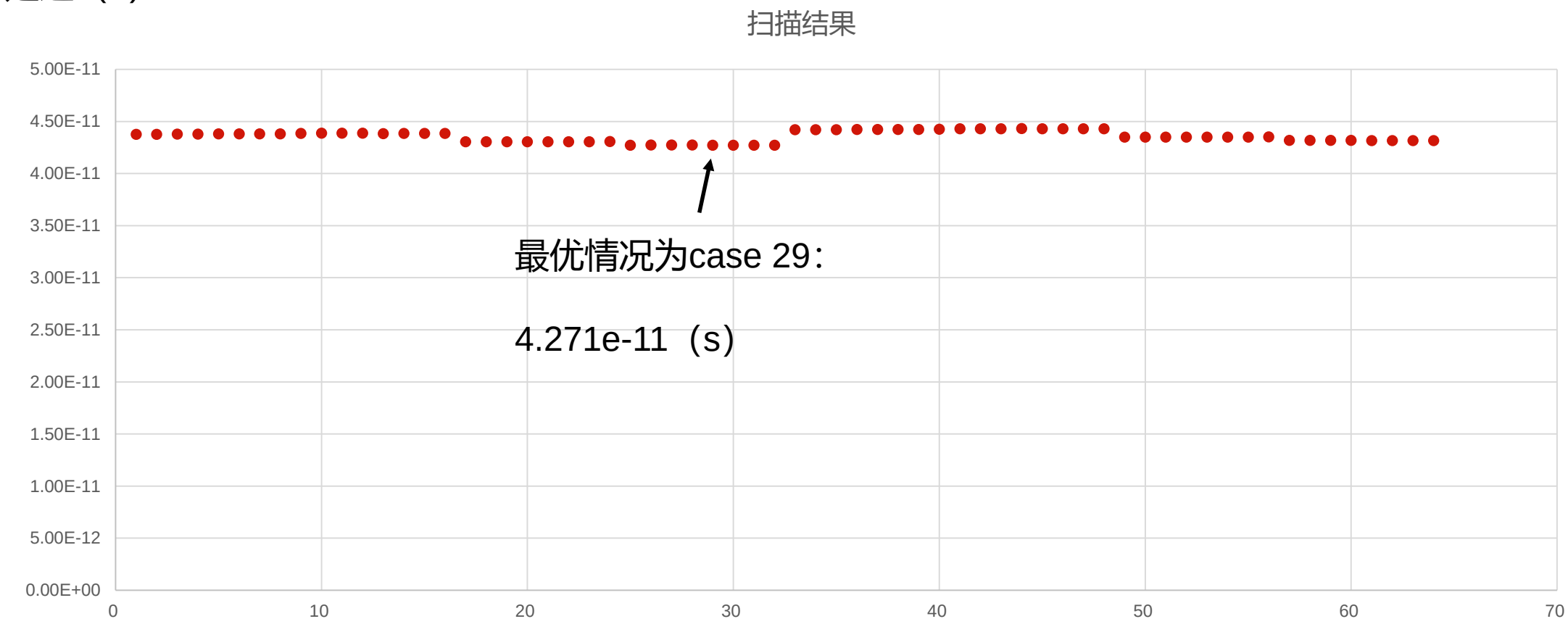
插入buffer（含4级反相器）

# 测量结果：插入buffer含2级反相器

| S2 | S5 | S6 | S7 | 延迟（s） |
|---|---|---|---|---|
| 1 | 1 | 4 | 19 | 5.3850E-11 |
| 1 | 1 | 4 | 20 | 5.3050E-11 |
| 1 | 1 | 5 | 19 | 5.3910E-11 |
| 1 | 1 | 5 | 20 | 5.3070E-11 |
| 1 | 2 | 4 | 19 | 5.3140E-11 |
| 1 | 2 | 4 | 20 | 5.2330E-11 |
| 1 | 2 | 5 | 19 | 5.2800E-11 |
| 1 | 2 | 5 | 20 | 5.1960E-11 |
| 2 | 1 | 4 | 19 | 5.4290E-11 |
| 2 | 1 | 4 | 20 | 5.3490E-11 |
| 2 | 1 | 5 | 19 | 5.4350E-11 |
| 2 | 1 | 5 | 20 | 5.3520E-11 |
| 2 | 2 | 4 | 19 | 5.3580E-11 |
| 2 | 2 | 4 | 20 | 5.2780E-11 |
| 2 | 2 | 5 | 19 | 5.3250E-11 |
| 2 | 2 | 5 | 20 | 5.2410E-11 |

# 测量结果：插入buffer含4级反相器

| S2 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|
| 1x | 2x | 5x | 20x | 76x | 304x |




**注意支路二和支路三应该拥有相同的延迟，但是由于finfet 的fin数量只能取整，在优化时候尺寸偏离了理想值，所以两条支路延迟存在差异，但是实际测出来两条支路的延迟差距不大，本次实验选择一条优化即可**

# 作业批改情况汇总

1、Task 1注意标准逻辑门尺寸size, 堆叠管子尺寸需要相应增大

2、Task 2/3 部分同学没有考虑最优级数优化

3、Task 2/3 部分同学通过优化级数后重新取h值也是可以的；因为h选取不一样，测量结果会有不同，但是误差应该不会太大

4、部分同学只有理论推导，完全没有仿真结果

5、部分同学仿真精度和仿真步长设置和参考答案不同，所以结果会有几皮秒差距，属于可接受范围

6、实验报告里面不需要大量粘贴代码，介绍核心代码如子电路即可