Digital Integrated Circuits

Lab 2

Inverter Simulation

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Outline

- Lab Contents
- Report Requirements

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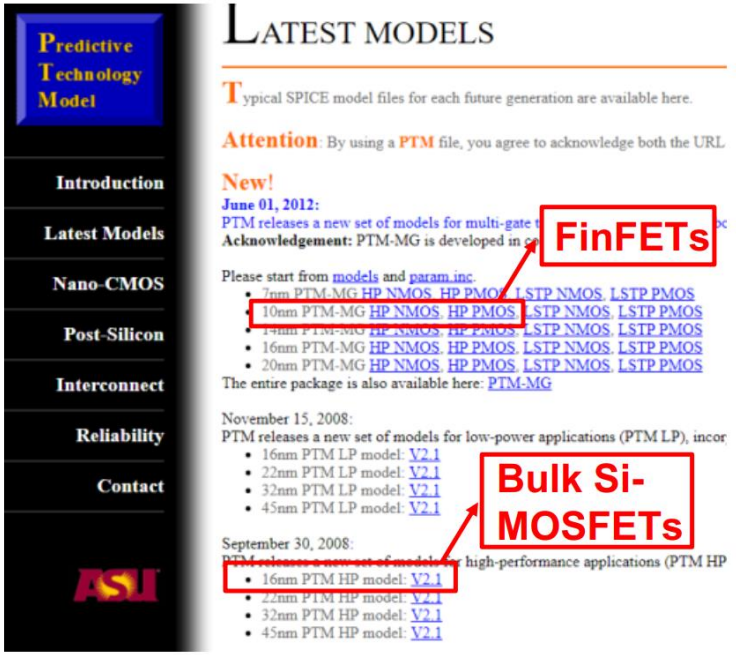
Device Models for Inverter Simulation

- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 16nm bulk Si-MOSFETs and 10nm multi-gate (MG) FinFETs
  - PTM link: http://ptm.asu.edu/
  - Use the high-performance (HP) models
  - For both n-channel and p-channel devices

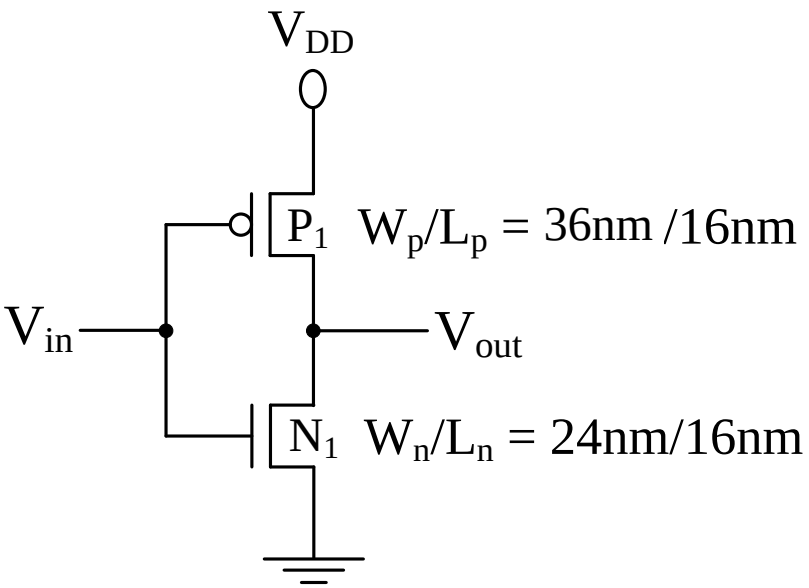


Simulation Settings

- L_g = 14 nm for FinFETs while L_g = 16nm for bulk Si-MOSFETs
- Supply voltage is 0.65V for FinFETs and 0.7V bulk Si-MOSFETs
- Simulation temperature
  - T = 25˚C

Task 1: Gate capacitance measurement of inverters

- Measure the gate capacitance (C_g) of CMOS inverters for both bulk and FinFET
  - 1X, 32X of minimum sized inverter



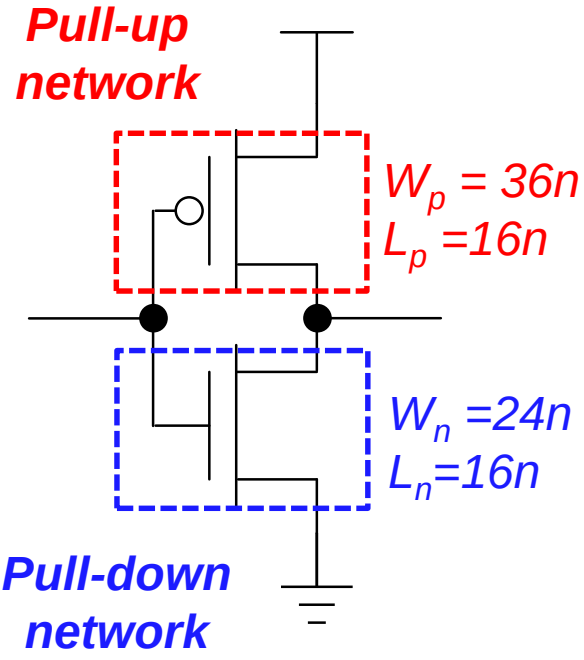
minimum-sized
un-skewed CMOS inverter

Minimum Sized Inv	PMOS	NMOS
W	36n	24n
L	16n	16n
You are free to change these widths, but in the minimum tuning step of 4nm		

Minimum Sized Inv	PMOS	NMOS
Fin number	1	1
L	14n	14n
Design the fin number to ensure balanced driving current in pull-up and pull-down network		

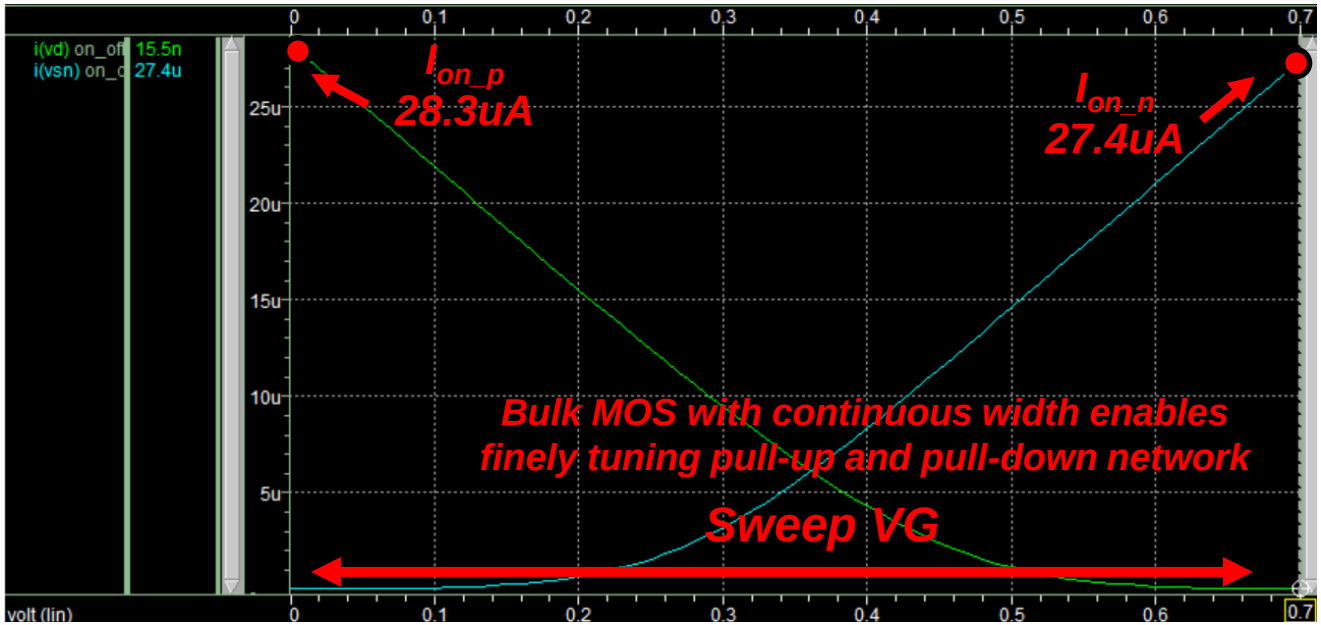
Minimum Inverter Sizing with approximately symmetrical driving strength for bulk silicon

- For bulk-inverter: the PMOS and the NMOS width ratio is ~1.5



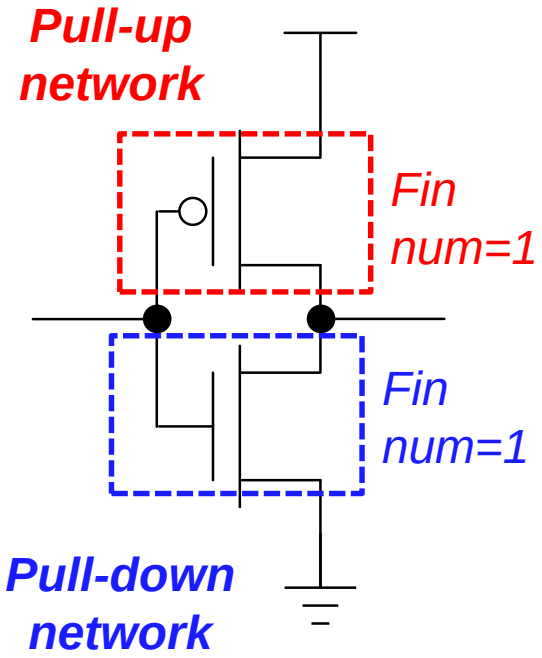
Minimum-sized bulk inverter

Bulk PMOS and NMOS with approximately symmetrical on-state currents: Wp/Wn = 36n/24n =1.5



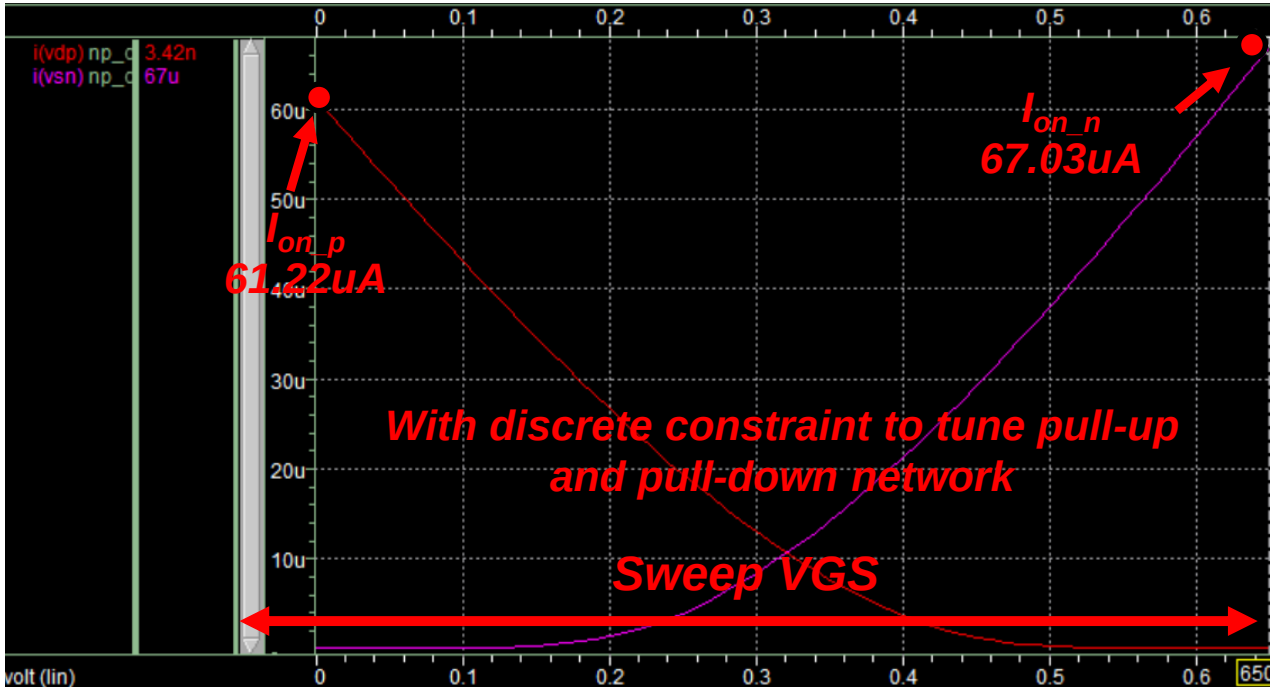
Minimum Inverter Sizing with approximately symmetrical driving strength for FinFET

- For bulk-inverter: the PMOS and the NMOS fin number ratio is ~1.0



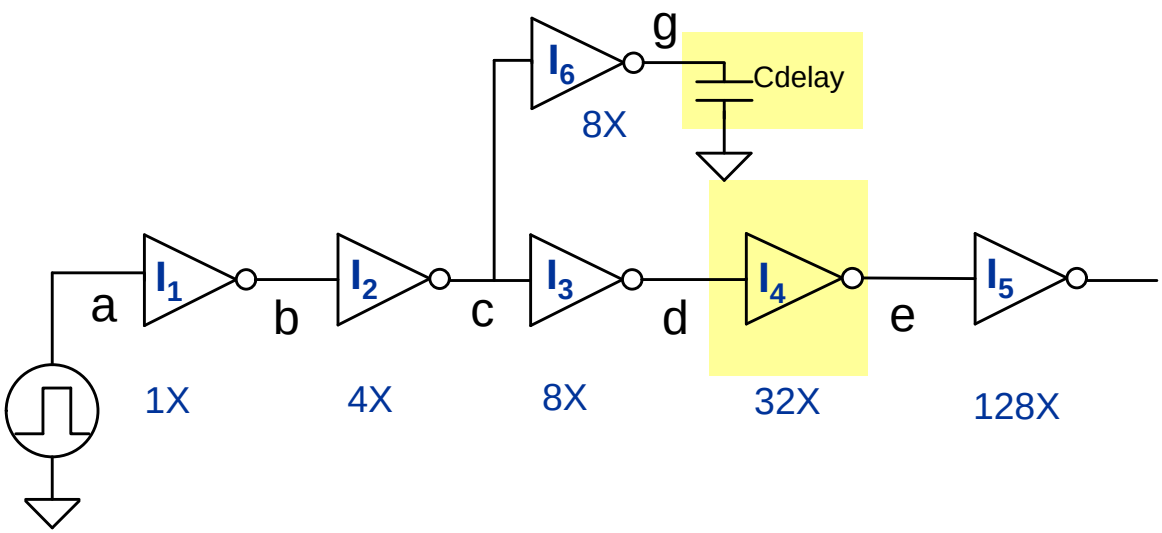
Minimum-sized finfet inverter

FinFET PMOS and NMOS with approximately symmetrical on-state currents: Fin numbers are both equal to 1



Steps of Measuring Gate Capacitance of Inverter:

- Adjust the capacitance value of C_{delay} until the average propagation delay from *c* to *g* equals the delay from *c* to *d*
- Then C_{delay} is equal to the effective gate capacitance of inverter I_4



Vpulse	
V1	0V
V2	0.7V/0.65v
Delay Time	1ns
Raise Time	50ps
Fall Time	50ps
Pulse Width	1ns
Period	2ns

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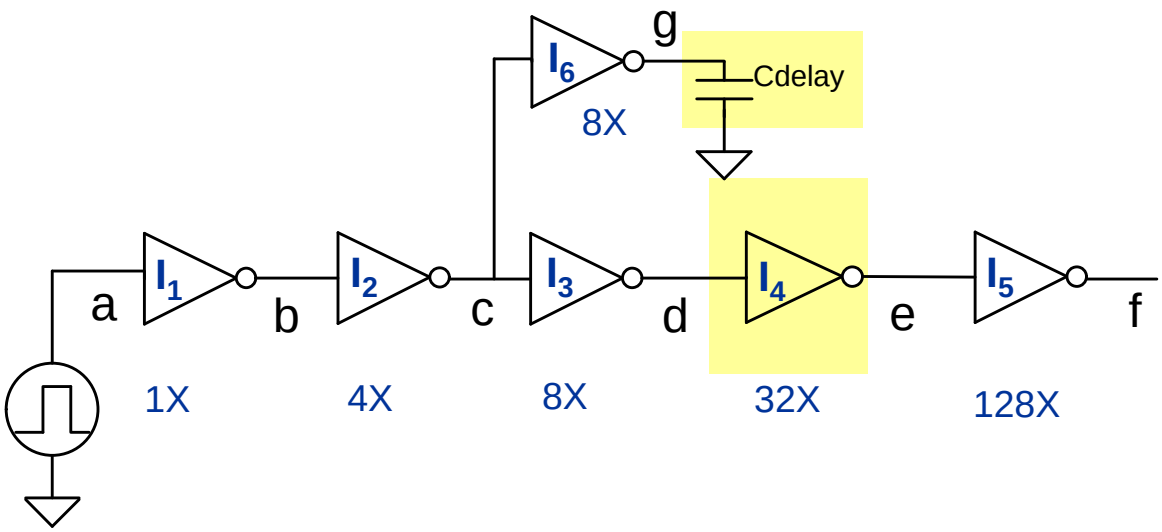
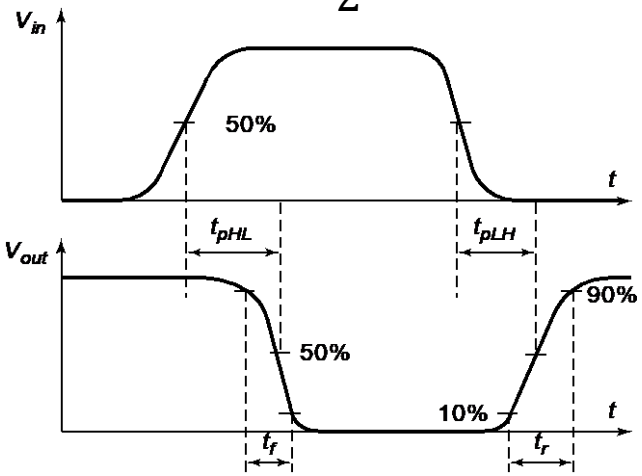


$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$



Hint: You can use the .MEASURE command to measure the propagation delay

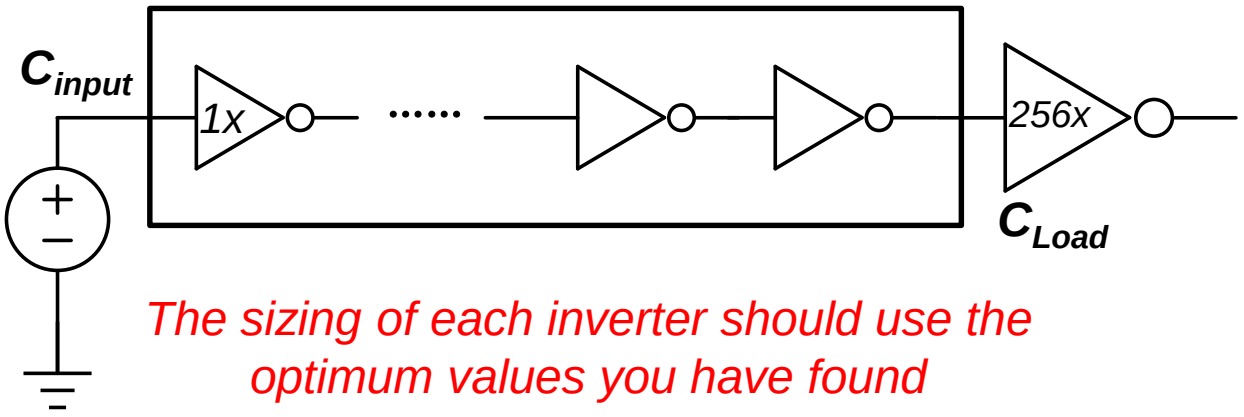
For example (measure the propagation delay from c to g for L->H transition):

.MEASURE TRAN t_{pLH}
+ TRIG V(c)='0.5*SUPPLY' FALL=2
+ TARG V(g)='0.5*SUPPLY' RISE=2

Task 2: Delay Optimization of Inverter Chain

- For a given input capacitance (minimum sized inverter) and C_{load} (256x of minimum sized inverter), design the inverter chain to minimize the delay for both bulk silicon and FinFET

Optimize the Stage Number and size each stage

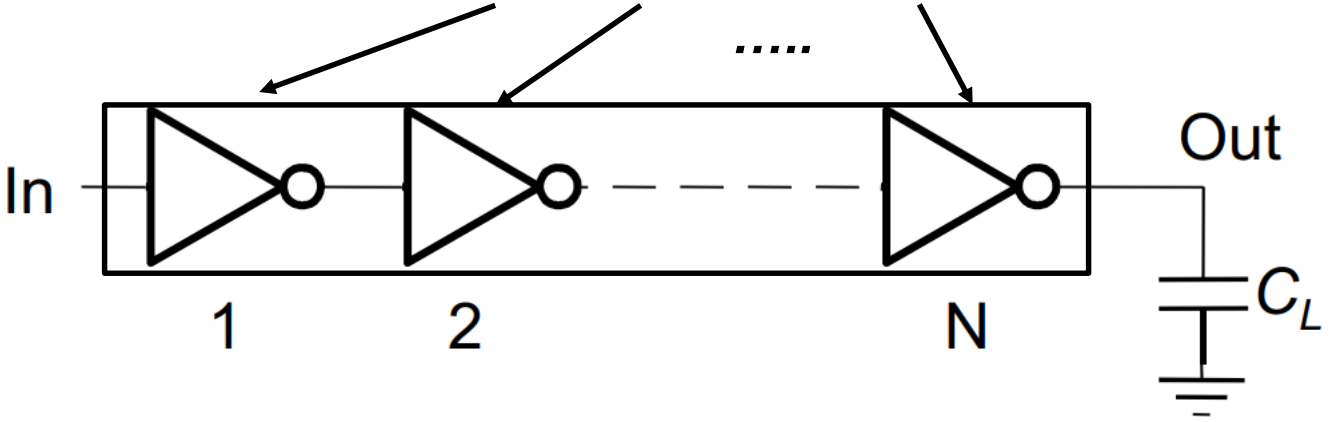


The sizing of each inverter should use the optimum values you have found

Delay Optimization of Inverter Chain

- Total propagation delay of inverter chain

$$t_p = t_{p1} + t_{p2} + \cdots + t_{pN}$$



When the chain has minimum delay, t_p has the form:

$$t_p = Nt_{p0}\left(1+\frac{f}{\gamma}\right) \quad f^N = F = \frac{C_L}{C_{g,1}}$$

f_{opt} = 3.6 for γ = 1

$$f = \exp\left(1+\gamma/f\right)$$

In fact, t_p can be transformed to a function only related to f :

$$t_p = Nt_{p0}\left(1+\frac{f}{\gamma}\right) = \frac{t_{p0}\ln F}{\gamma}\left(\frac{f}{\ln f}+\frac{\gamma}{\ln f}\right)$$

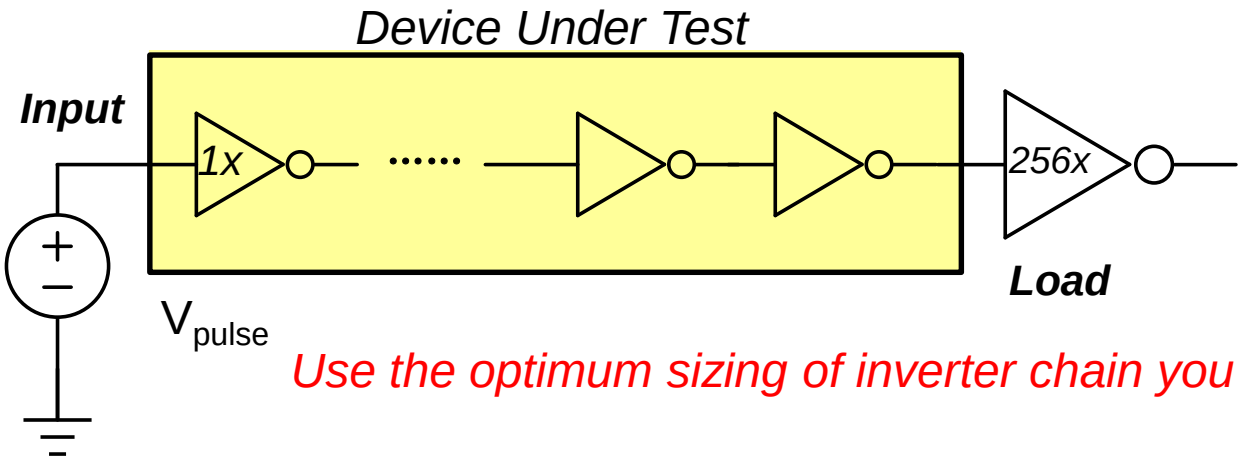
To minimize t_p $\Longrightarrow$ $\frac{\partial t_p}{\partial f} = \frac{t_{p0} lnF}{\gamma} \cdot \frac{lnf - 1 - \frac{\gamma}{f}}{ln^2 f} = 0$

Steps for Sizing the Inverter Chain

- Add a DC supply and a pulse generator for the input signal. Set the following parameters for the pulse generator: V1 = 0, V2 = Vdd. Choose appropriate Delay time, Rise time = Fall time, Pulse width, and Period so that you can easily observe and measure the delay from the simulated waveforms.
- Insert appropriate number of inverters and determine the sizes of each inverter between the minimum-sized inverter and the capacitor load so that the delay from the input signal to the output at the capacitor is minimized (This is the key part of this whole lab).
- For bulk silicon, the minimum tuning step of width of each transistor is 4nm. For FinFET, the fin number of each transistor needs to be integer.

Task 3: Power of Inverter Chain

- Measure the power of inverter chain
  - Only include the power consumption of inverter chain
  - Apply a pulse voltage on the input node and measure the power averaging for multiple cycles



Use the optimum sizing of inverter chain you have found

Hint:

- You can use two different power supply sources for the DUT inverter and other parts (for example, use V_{DD1} for the DUT inverter while using V_{DD2} for the other parts, if you have)
- You can use the .MEASURE command to measure the power consumption
  For example (measure the power of the circuit from V_{DD}):
  .MEASURE TRAN avgpower AVG P(VDD1) FROM=1ns TO=80ns

Task 4 (optional): Optimum Vdd for Minimizing EDP

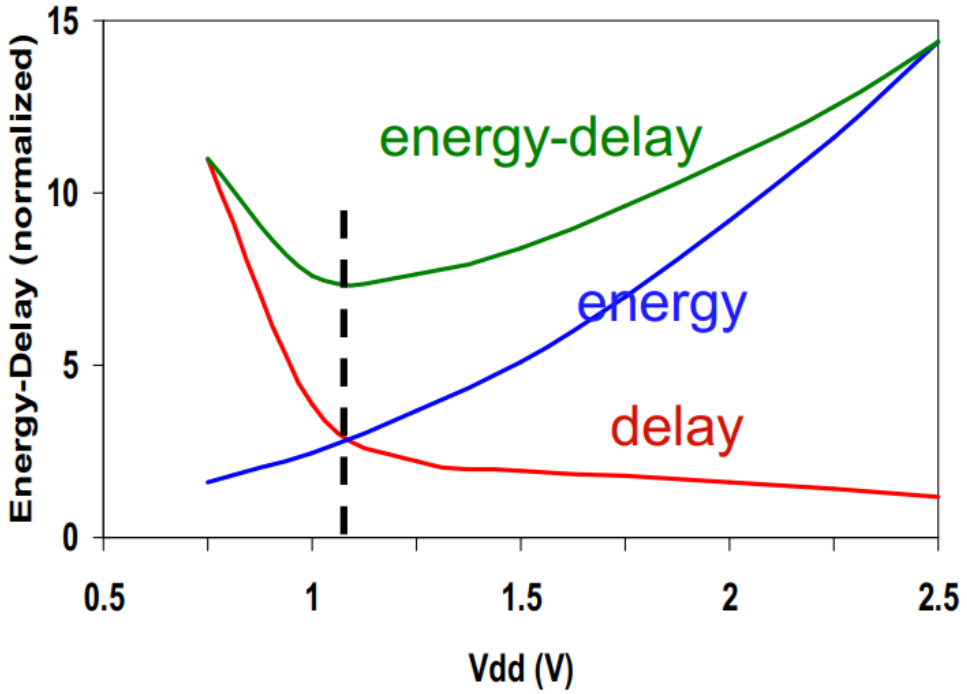
- Find the optimal point of V_{DD} to minimize the energy and delay Product

Power-Delay Product (PDP):

$$PDP = P_{av} t_p$$

Energy-Delay Product (EDP):

$$EDP = PDP * t_p = P_{av} t_p^2 = \frac{C_L V_{DD}^2}{2} t_p$$



Hint:

- *You can sweep the VDD beyond the standard supply voltage*
- *Ultral-low VDD may result in unfunctional circuit, so you need to check the functionality of circuit*

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Report Requirement

- Write your lab report like writing a technical document (readable, comprehensive analysis, no typo…)
- You may include
  - Introduction/background
  - Lab procedures
  - Lab results
  - Technical analysis of the simulation results
  - Observations and conclusions

Submission

- You need to submit your report and code
  - Name of report (in PDF format):
    lab2_report_[Name]_[Student No.].pdf
  - Name of code (compressing the files):
    lab2_code__[Name]_[Student No.].zip

- Please upload your report to Canvas course website

- Submission of lab2 report and code will be due on 21th November 2021

Q & A

- If you have any technical problem, you can directly contact me or TA

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