DIC
ID: 519021911248
Name: ZhuoHao Li

Lab 2

2021-11-17

1 Introduction

Inverter is the basic unit when designing the complicated CMOS logic. So it's important to do inverter simulation due to better acknowledgement about more complex and obscure DIC coming later.

2 Lab Procedures

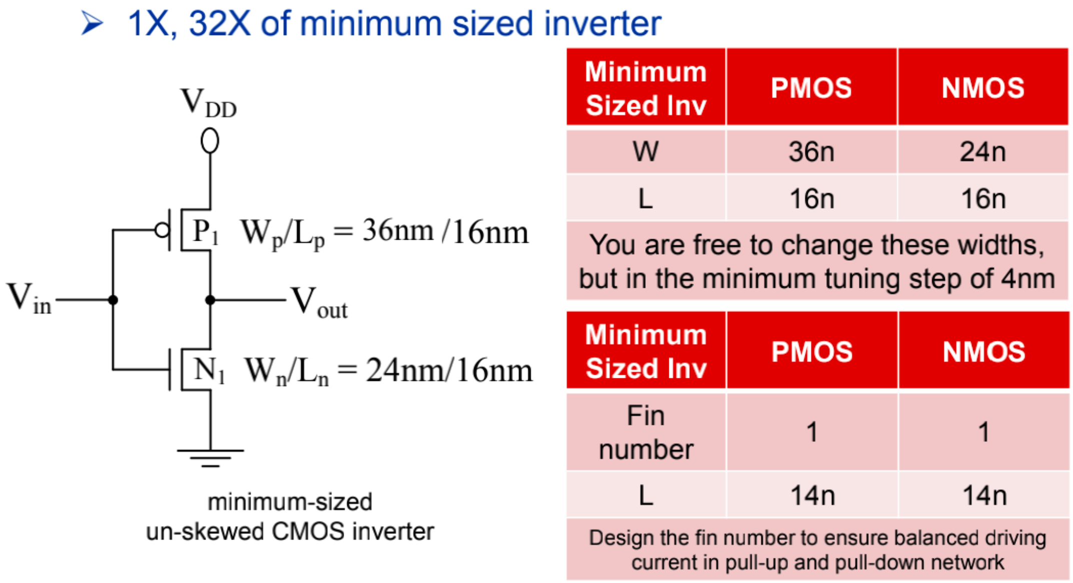
This lab is also based on using the Predictive Technology Model (PTM) to evaluate the DC characteristics of 16nm bulk Si-MOSFETs and 10nm multi-gate (MG) FinFETs. And the simulation settings are shown as belows:

1. Lg = 14 nm for FinFETs while Lg = 16nm for bulk Si-MOSFETs
2. Supply voltage is 0.65V for FinFETs and 0.7V for bulk Si-MOSFETs
3. Simulation temperature T = 25 ° C

I connect the output load to the ground instead of floating in task1 and task2. I don't think there's nothing bad after I confirm with the TA that the output pin should be floating when I was doing task3. The result or more specifically, the conclusion in this lab won't change at more. If TA want data simulated in float connection, just contact me.

2.1 Measurement of C_g

The basic structure of t an inverter is shown as belows (reference: slides page6)



➢ 1X, 32X of minimum sized inverter

minimum-sized
un-skewed CMOS inverter

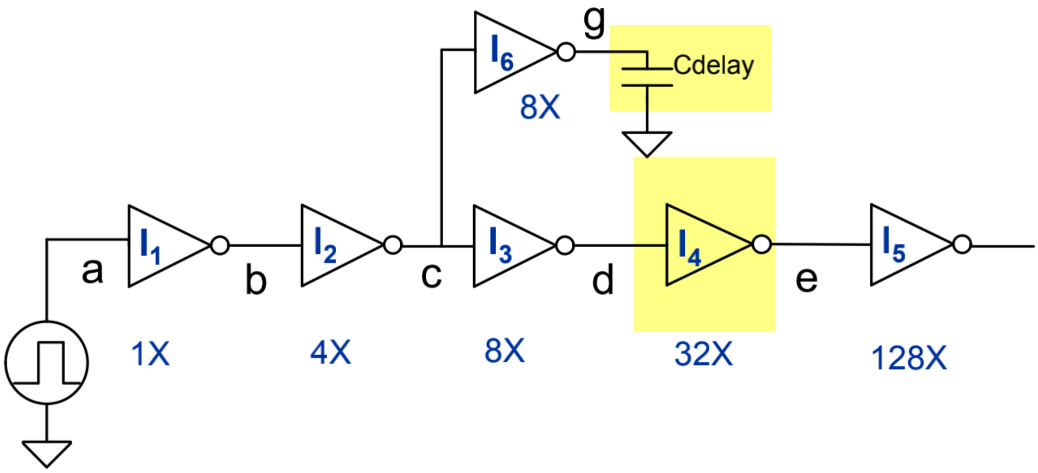
Minimum Sized Inv	PMOS	NMOS
W	36n	24n
L	16n	16n
You are free to change these widths, but in the minimum tuning step of 4nm		

Minimum Sized Inv	PMOS	NMOS
Fin number	1	1
L	14n	14n
Design the fin number to ensure balanced driving current in pull-up and pull-down network		

As we can see, the $\lambda = 8nm$due to the process. So the voltage vdd = 0.7V for bulk silicon and 0.65V for FinFet. And we can assume that the unit inverter has a symmetrical propagation delay which means

$t_{pLH} = t_{pHL}$. We can derive the standard inverter size under the specific process shown as the right figure. The basic $\frac{(W/l)_p}{(W/l)_n} = 1.5$ (notice: not equals to 2 as we learned in class). Overriding the same process of analysis, we can ensure the $\frac{(fin.n)_p}{(fin.n)_n} = 1.0$ to perform a minimum FinFet inverter.

We can estimate the C_g as the following figure:



The proof of the method is simple, take the 32 × inverter shown in the figure as an example. Due to the pre-driving network is the same. So if the $t_{c\to g} = t_{c\to d}$, we can estimate the $C_g = C_{delay}$. Totally the same as the FinFet!

So the code is as belows:

```
.TITLE bulk_c_32
.lib ”./LAB1_LIB/BULK/models” ptm16hp_bulk

.option post
.global vdd gnd
.temp 25

.param supply = 0.7V
.param length = 16nm
.param n_width = 24nm
.param p_width = 36nm
.param Cdelay = 1.8fF


.subckt inv in out l=16nm w1=24nm w2=36nm
xnmos out in gnd gnd nfet l=length w=w1
xpmos out in vdd vdd pfet l=length w=w2
```

```
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv w1='4*24n' w2='4*36n'
x3 vout2 vout3 inv w1='8*24n' w2='8*36n'
x4 vout3 vout4 inv w1='32*24n' w2='32*36n'
x5 vout4 vout5 inv w1='128*24n' w2='128*36n'
x6 vout2 g inv w1='8*24n' w2='8*36n'
C g gnd Cdelay

vs vin1 gnd pulse(0,0.7,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply

.TRAN 1ns 9ns sweep Cdelay 1.78fF 1.8fF 0.005fF

.measure tran tpLH1
+trig V(vout2)='0.5*supply' fall=2
+targ V(g)='0.5*supply' rise=2
.measure tran tpHL1
+trig V(vout2)='0.5*supply' rise=2
+targ V(g)='0.5*supply' fall=2
.measure tran tpLH2
+trig V(vout2)='0.5*supply' fall=2
+targ V(vout3)='0.5*supply' rise=2
.measure tran tpHL2
+trig V(vout2)='0.5*supply' rise=2
+targ V(vout3)='0.5*supply' fall=2
.measure tp1 param='(tpLH1+tpHL1)/2'
.measure tp2 param='(tpLH2+tpHL2)/2'


.end
```

t1 bulk c32.sp

By using the same idea, we can derive the **FinFet** simulation code shown as belows:

```
.TITLE finfet_c_1
.lib "./LAB1_LIB/FINFET/models" ptm16hp

.option post
.global vdd gnd
.temp 25

.param supply = 0.65V
.param length = 14nm
* .param n_width = 24nm
* .param p_width = 36nm
.param Cdelay = 1.8fF


.subckt inv in out l=length n1=1 n2=1
xnmos out in gnd gnd nfet l=length NFIN=n1
xpmos out in vdd vdd pfet l=length NFIN=n2
```

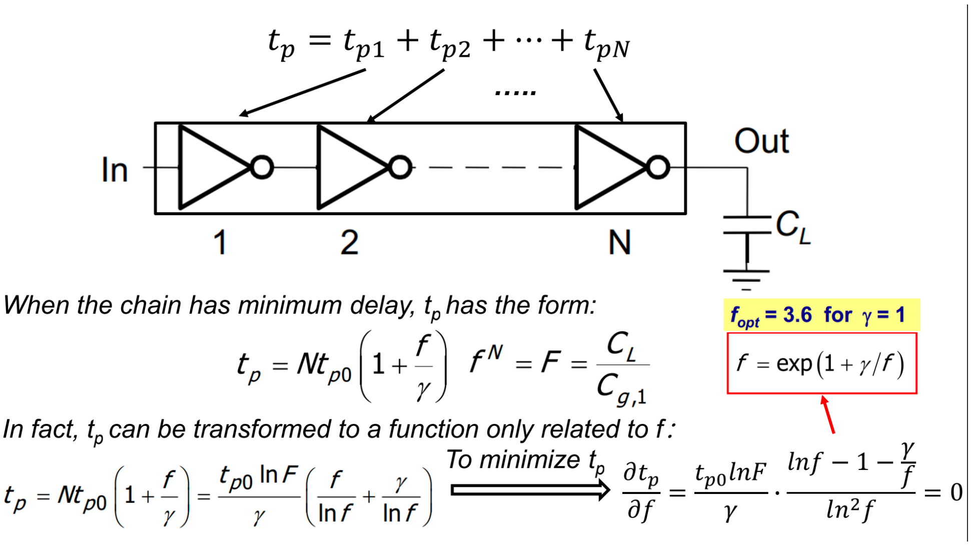
```
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv n1='4*1' n2='4*1'
x3 vout2 vout3 inv n1='8*1' n2='8*1'
x4 vout3 vout4 inv
x5 vout4 vout5 inv n1='128*1' n2='128*1'
x6 vout2 g inv n1='8*1' n2='8*1'
C g gnd Cdelay

vs vin1 gnd pulse(0,0.7,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply

.TRAN 1ns 9ns sweep Cdelay 1.5fF 2fF 0.05fF

.measure tran tpLH1
+trig V(vout2)='0.5*supply' fall=2
+targ V(g)='0.5*supply' rise=2
.measure tran tpHL1
+trig V(vout2)='0.5*supply' rise=2
+targ V(g)='0.5*supply' fall=2
.measure tran tpLH2
+trig V(vout2)='0.5*supply' fall=2
+targ V(vout3)='0.5*supply' rise=2
.measure tran tpHL2
+trig V(vout2)='0.5*supply' rise=2
+targ V(vout3)='0.5*supply' fall=2
.measure tp1 param='(tpLH1+tpHL1)/2'
.measure tp2 param='(tpLH2+tpHL2)/2'


.end
```

t1 finfet c1.sp

2.2 Delay Optimization of Inverter Chain

For a given input capacitance (minimum sized inverter) and Cload (256x of minimum sized inverter), design the inverter chain to minimize the delay for both bulk silicon and FinFET

We usually simulate the idea like this figure shown as belows:



$$t_p = t_{p1} + t_{p2} + \cdots + t_{pN}$$

When the chain has minimum delay, t_p has the form:

$$t_p = Nt_{p0}\left(1+\frac{f}{\gamma}\right) \quad f^N = F = \frac{C_L}{C_{g,1}}$$

f_{opt} **= 3.6 for** γ **= 1**

$$\boxed{f = \exp(1+\gamma/f)}$$

In fact, t_p can be transformed to a function only related to f:

$$t_p = Nt_{p0}\left(1+\frac{f}{\gamma}\right) = \frac{t_{p0}\ln F}{\gamma}\left(\frac{f}{\ln f}+\frac{\gamma}{\ln f}\right) \xrightarrow{\text{To minimize } t_p} \frac{\partial t_p}{\partial f} = \frac{t_{p0}lnF}{\gamma}\cdot\frac{lnf-1-\frac{\gamma}{f}}{ln^2 f} = 0$$

Theoretically, we can derive the formula of the **optimal** fan-out for each inverter in a single inverter chain is 3.6 due to the formulation shown above. Usually we choose 4 or 3 due to the circumstances. The formuala to caculate the levels of a chain is $N = \frac{lnF}{lnf}$. There is a detail we must pay enough attention to is the bulk's parameter, width, can be a float. In contrast, FinFet's parameter, FIN number, should definitely be an **integer**. **So I choose 2,3,4,5 for f value and 2-level,3-level,5-level for N to figure out each delay for bulk and choose 3,4 for f value, 5-level,6-level for N for FINFET.**

The complete process is:

1. Add a DC supply and a pulse generator for the input signal. Set the following parameters for the pulse generator and I override the PULSE used in task1 that I can easily observe and measure the delay from the simulated MT0 file.

2. Insert appropriate number of inverters and determine the sizes of each inverter between the minimum-sized inverter and the capacitor load so that the delay from the input signal to the output at the capacitor is minimized

3. (Be careful!) For bulk silicon, the minimum tuning step of width of each transistor is 4nm. For FinFET, the fin number of each transistor needs to be integer.

I just take the optimal chain design for bulk and FINFET as an example, the code is shown as below:

```

x1 vin1 vout1 inv
x2 vout1 vout2 inv w1=’4*24n’ w2=’4*36n’
x3 vout2 vout3 inv w1=’16*24n’ w2=’16*36n’
x4 vout3 vout4 inv w1=’64*24n’ w2=’64*36n’
xload vout4 gnd inv w1=’256*24n’ w2=’256*36n’

vs vin1 gnd pulse(0,0.7,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply

.TRAN 1ns 9ns
```

```

.measure tran tpLH
+trig V(vin1)='0.5*supply' fall=2
+targ V(vout4)='0.5*supply' rise=2
.measure tran tpHL
+trig V(vin1)='0.5*supply' rise=2
+targ V(vout4)='0.5*supply' fall=2

.measure tp param='(tpLH+tpHL)/2'
```

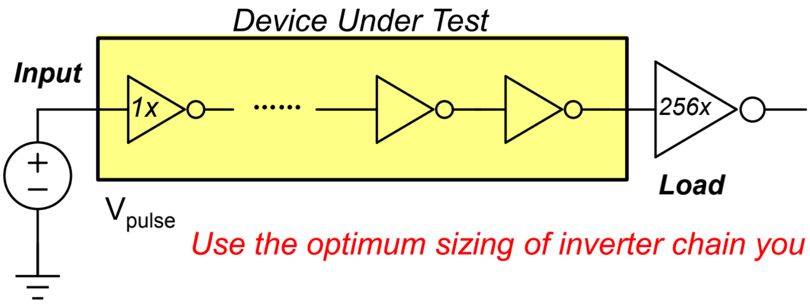
t2 bulk .sp (core code)

```

.subckt inv in out l=length n1=1 n2=1
xnmos out in gnd gnd nfet l=length NFIN=n1
xpmos out in vdd vdd pfet l=length NFIN=n2
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv n1=4 n2=4
x3 vout2 vout3 inv n1=16 n2=16
x4 vout3 vout4 inv n1=64 n2=64
xload vout4 gnd inv n1=256 n2=256

vs vin1 gnd pulse(0,0.65,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply

.TRAN 1ns 9ns

.measure tran tpLH
+trig V(vin1)='0.5*supply' fall=2
+targ V(vout4)='0.5*supply' rise=2
.measure tran tpHL
+trig V(vin1)='0.5*supply' rise=2
+targ V(vout4)='0.5*supply' fall=2

.measure tp param='(tpLH+tpHL)/2'
```

t2 finfet .sp (core code)

2.3 Power of Inverter Chain

Measure the power of inverter chain Only include the power consumption of inverter chain.Apply a pulse voltage on the input node and measure the power averaging for multiple cycles.



Use the optimum sizing of inverter chain you have found

Hint:

1. We can use two different power supply sources for the DUT inverter and other parts (for example, use VDD1 for the DUT inverter while using VDD2 for the other parts)

2. We can use the *.MEASURE* command to measure the power consumption. For example to measure the power of the circuit from VDD:

```
    .MEASURE TRAN avgpower AVG P(VDD1) FROM=1ns TO=80ns
```

   This shows how we can get the average power for the inverter chain is that seperating the Vdd to different parts and use *.measure* to check a single voltage supply.

In this task, I just let the output of the load inverter to be float. The core code is shown as below:

```

.param supply = 0.7V
.param supplyload = 0.7v
.param length = 16nm
.param n_width = 24nm
.param p_width = 36nm

.subckt inv in out l=length w1=24nm w2=36nm
xnmos out in gnd gnd nfet l=length w=w1
xpmos out in vdd vdd pfet l=length w=w2
.ends

.subckt invload in out l=length w1=24nm w2=36nm
xnmos out in gnd gnd nfet l=length w=w1
xpmos out in vdd2 vdd2 pfet l=length w=w2
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv w1='4*24n' w2='4*36n'
x3 vout2 vout3 inv w1='16*24n' w2='16*36n'
x4 vout3 vout4 inv w1='64*24n' w2='64*36n'
xload vout4 vout5 invload w1='256*24n' w2='256*36n'

vs vin1 gnd pulse(0,0.7,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply
vdd2 vdd2 gnd supplyload
```

```

.TRAN 1ns 9ns

.MEASURE TRAN avgpower AVG P(VDD) FROM=1ns TO=9ns

.end
```

t3 bulk power .sp (core code)

The **FINFET** simulation is quite similar, it is shown as belows:

```
.option post
.global vdd gnd vdd2
.temp 25

.param supply = 0.65V
.param supplyload = 0.65v
.param length = 14nm

.subckt inv in out l=length n1=1 n2=1
xnmos out in gnd gnd nfet l=length NFIN=n1
xpmos out in vdd vdd pfet l=length NFIN=n2
.ends

.subckt invload in out l=length n1=1 n2=1
xnmos out in gnd gnd nfet l=length NFIN=n1
xpmos out in vdd2 vdd2 pfet l=length NFIN=n2
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv n1=4 n2=4
x3 vout2 vout3 inv n1=16 n2=16
x4 vout3 vout4 inv n1=64 n2=64
xload vout4 vout5 invload n1=256 n2=256

vs vin1 gnd pulse(0,0.65,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply
vdd2 vdd2 gnd supplyload

.TRAN 1ns 9ns

.MEASURE TRAN avgpower AVG P(VDD) FROM=1ns TO=9ns

.end
```

t3 finfet power .sp

2.4 Optimal Vdd for Minimizing EDP

Find the optimal point of VDD to minimize the energy and delay Product.

EDP (Energy-Delay-Product) is defined as:

$$EDP = P_{average} t_{propagation}^2$$

It’s quite simple since finished task2 and task3. We just need to combine the task2 and task3 code.

The core code is shown as below:

```
.TITLE bulk_chain
.lib ”./LAB1_LIB/BULK/models” ptm16hp_bulk

.option post
.global vdd gnd vdd2
.temp 25

.param supply = 0.7V

.param length = 16nm
.param n_width = 24nm
.param p_width = 36nm



.subckt invload in out l=length w1=24nm w2=36nm
xnmos out in gnd gnd nfet l=length w=w1
xpmos out in vdd2 vdd2 pfet l=length w=w2
.ends


.subckt inv in out l=length w1=24nm w2=36nm
xnmos out in gnd gnd nfet l=length w=w1
xpmos out in vdd vdd pfet l=length w=w2
.ends

x1 vin1 vout1 inv
x2 vout1 vout2 inv w1=’4*24n’ w2=’4*36n’
x3 vout2 vout3 inv w1=’16*24n’ w2=’16*36n’
x4 vout3 vout4 inv w1=’64*24n’ w2=’64*36n’
xload vout4 gnd invload w1=’256*24n’ w2=’256*36n’

vs vin1 gnd pulse(0,0.7,1ns,50ps,50ps,1ns,2ns)
vdd vdd gnd supply
vdd2 vdd2 gnd supply



.TRAN 1ns 9ns sweep supply 0.7 1.3 0.05

.measure tran tpLH1
+trig V(vin1)=’0.5*supply’ fall=2
+targ V(vout1)=’0.5*supply’ rise=2
.measure tran tpHL1
+trig V(vin1)=’0.5*supply’ rise=2
+targ V(vout1)=’0.5*supply’ fall=2
.measure tp1 param=’(tpLH1+tpHL1)/2’


.measure tran tpLH2
```

```
+trig V(vout1)='0.5*supply' fall=2
+targ V(vout2)='0.5*supply' rise=2
.measure tran tpHL2
+trig V(vout1)='0.5*supply' rise=2
+targ V(vout2)='0.5*supply' fall=2
.measure tp2 param='(tpLH2+tpHL2)/2'


.measure tran tpLH3
+trig V(vout2)='0.5*supply' fall=2
+targ V(vout3)='0.5*supply' rise=2
.measure tran tpHL3
+trig V(vout2)='0.5*supply' rise=2
+targ V(vout3)='0.5*supply' fall=2
.measure tp3 param='(tpLH3+tpHL3)/2'


.measure tran tpLH4
+trig V(vout3)='0.5*supply' fall=2
+targ V(vout4)='0.5*supply' rise=2
.measure tran tpHL4
+trig V(vout3)='0.5*supply' rise=2
+targ V(vout4)='0.5*supply' fall=2
.measure tp4 param='(tpLH4+tpHL4)/2'

.measure tp param='tpLH1+tpLH2+tpLH3+tpLH4'

.MEASURE TRAN avgpower AVG P(VDD) FROM=1ns TO=9ns

.measure EDP param='avgpower*tp*tp'

.end
```

ALL you need is just combine the task3 and task 4 code into one

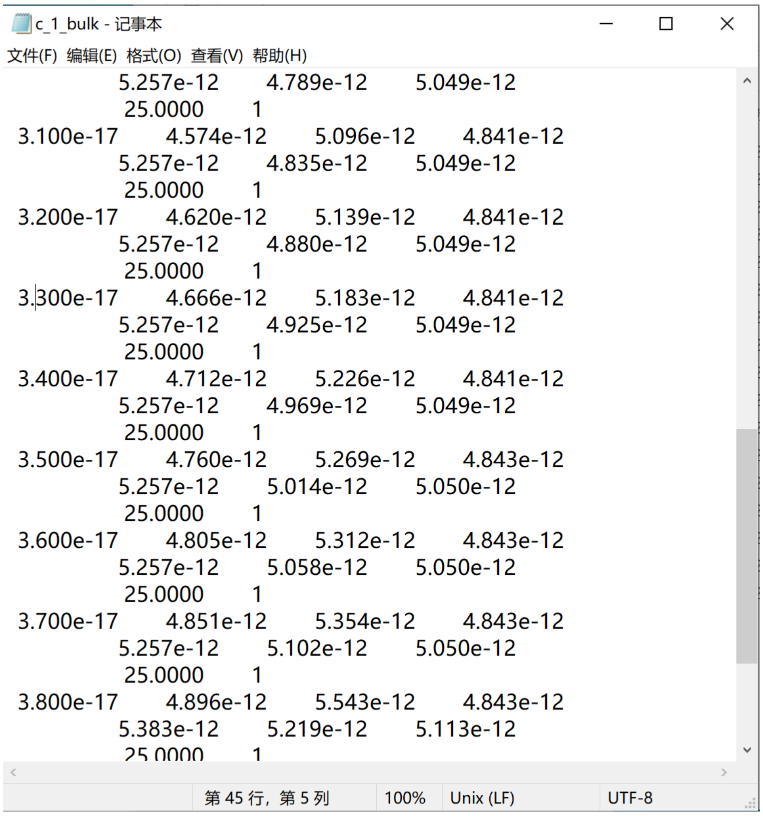
Due to the page limit, the FINFET optimal vdd will not displayed here, you can check them by unzipping what I upload.

3 Lab Results

3.1 Measurement of C_g

3.1.1 Minimized bulk CMOS inverter

The screenshot after t1_bulk_c1.sp

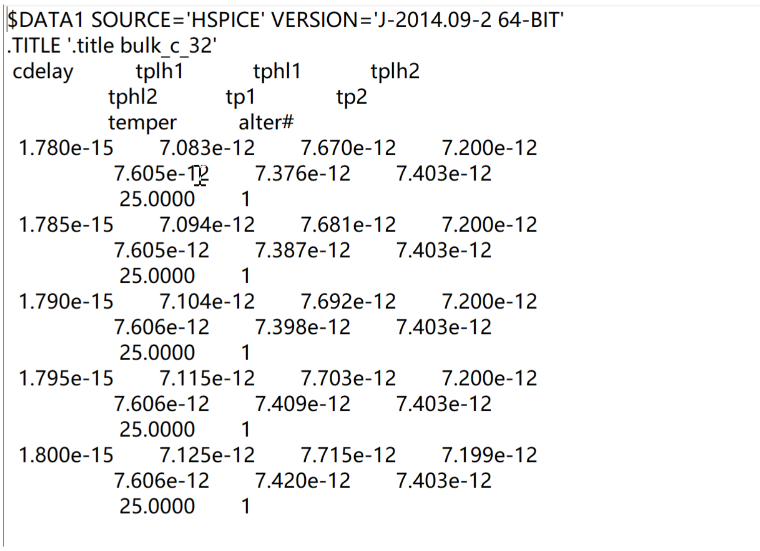


```
          5.257e-12      4.789e-12      5.049e-12
           25.0000        1
 3.100e-17      4.574e-12      5.096e-12      4.841e-12
          5.257e-12      4.835e-12      5.049e-12
           25.0000        1
 3.200e-17      4.620e-12      5.139e-12      4.841e-12
          5.257e-12      4.880e-12      5.049e-12
           25.0000        1
 3.300e-17      4.666e-12      5.183e-12      4.841e-12
          5.257e-12      4.925e-12      5.049e-12
           25.0000        1
 3.400e-17      4.712e-12      5.226e-12      4.841e-12
          5.257e-12      4.969e-12      5.049e-12
           25.0000        1
 3.500e-17      4.760e-12      5.269e-12      4.843e-12
          5.257e-12      5.014e-12      5.050e-12
           25.0000        1
 3.600e-17      4.805e-12      5.312e-12      4.843e-12
          5.257e-12      5.058e-12      5.050e-12
           25.0000        1
 3.700e-17      4.851e-12      5.354e-12      4.843e-12
          5.257e-12      5.102e-12      5.050e-12
           25.0000        1
 3.800e-17      4.896e-12      5.543e-12      4.843e-12
          5.383e-12      5.219e-12      5.113e-12
           25.0000        1
```

The C_g is about 3.6×10^{-17} F

3.1.2 32 Minimized bulk CMOS inverter

The screenshot after t1_bulk_c32.sp

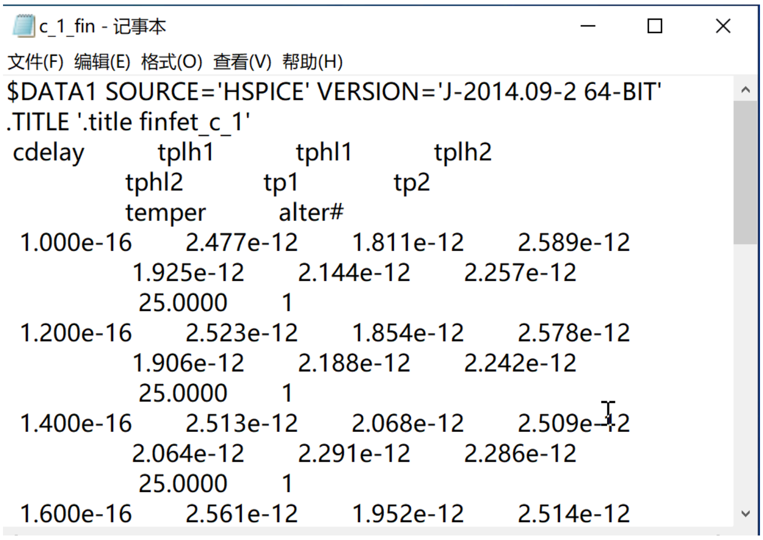


```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_c_32'
 cdelay          tplh1          tphl1          tplh2
          tphl2          tp1            tp2
          temper         alter#
 1.780e-15      7.083e-12      7.670e-12      7.200e-12
          7.605e-12      7.376e-12      7.403e-12
           25.0000        1
 1.785e-15      7.094e-12      7.681e-12      7.200e-12
          7.605e-12      7.387e-12      7.403e-12
           25.0000        1
 1.790e-15      7.104e-12      7.692e-12      7.200e-12
          7.606e-12      7.398e-12      7.403e-12
           25.0000        1
 1.795e-15      7.115e-12      7.703e-12      7.200e-12
          7.606e-12      7.409e-12      7.403e-12
           25.0000        1
 1.800e-15      7.125e-12      7.715e-12      7.199e-12
          7.606e-12      7.420e-12      7.403e-12
           25.0000        1
```

The C_g is about 1.79×10^{-15} F

3.1.3 Minimized FinFet CMOS inverter

The screenshot after t1_finfet_c1.sp

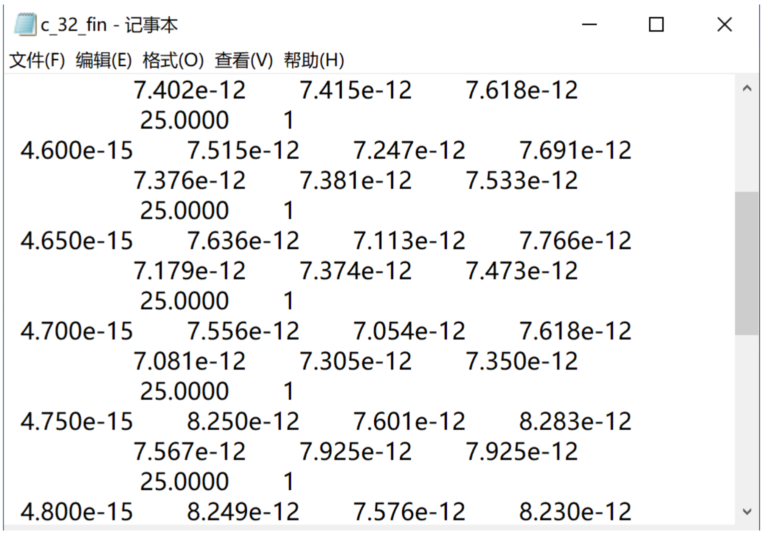


```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title finfet_c_1'
 cdelay          tplh1           tphl1           tplh2
                 tphl2           tp1             tp2
                 temper          alter#
  1.000e-16       2.477e-12       1.811e-12       2.589e-12
                  1.925e-12       2.144e-12       2.257e-12
                   25.0000        1
  1.200e-16       2.523e-12       1.854e-12       2.578e-12
                  1.906e-12       2.188e-12       2.242e-12
                   25.0000        1
  1.400e-16       2.513e-12       2.068e-12       2.509e-12
                  2.064e-12       2.291e-12       2.286e-12
                   25.0000        1
  1.600e-16       2.561e-12       1.952e-12       2.514e-12
```

The C_g is about 1.4×10^{-16} F

3.1.4 32 Minimized bulk CMOS inverter

The screenshot after t1_finfet_c32.sp



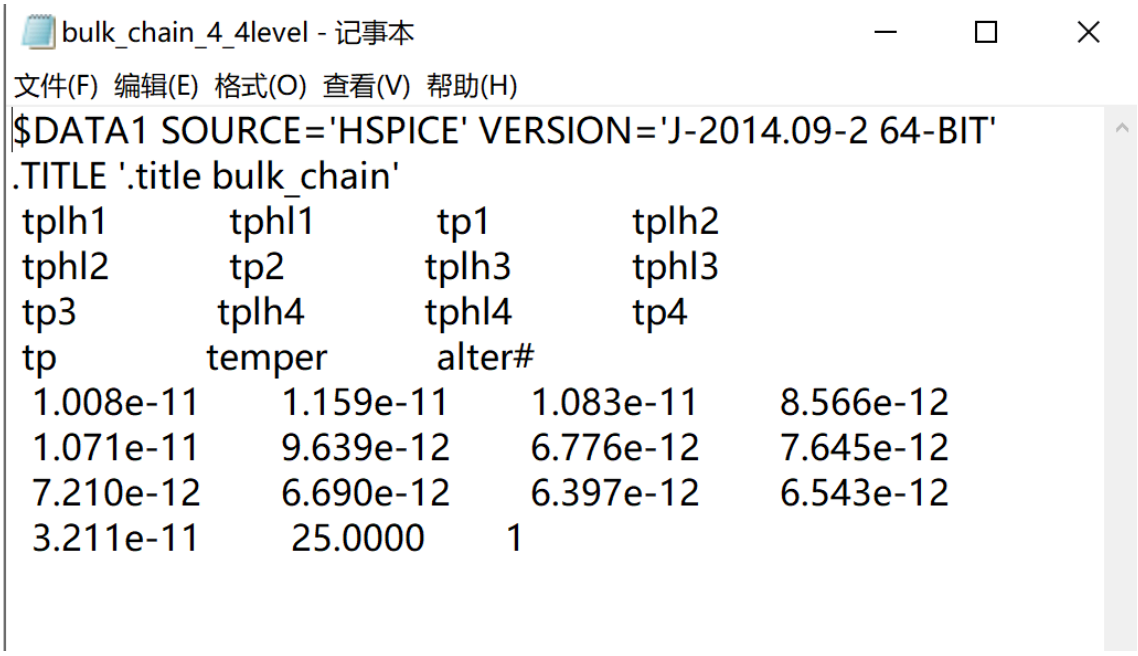
```
                  7.402e-12       7.415e-12       7.618e-12
                   25.0000        1
  4.600e-15       7.515e-12       7.247e-12       7.691e-12
                  7.376e-12       7.381e-12       7.533e-12
                   25.0000        1
  4.650e-15       7.636e-12       7.113e-12       7.766e-12
                  7.179e-12       7.374e-12       7.473e-12
                   25.0000        1
  4.700e-15       7.556e-12       7.054e-12       7.618e-12
                  7.081e-12       7.305e-12       7.350e-12
                   25.0000        1
  4.750e-15       8.250e-12       7.601e-12       8.283e-12
                  7.567e-12       7.925e-12       7.925e-12
                   25.0000        1
  4.800e-15       8.249e-12       7.576e-12       8.230e-12
```

The C_g is about 4.75×10^{-15} F

3.2 Delay Optimization of Inverter Chain

3.2.1 bulk silicon

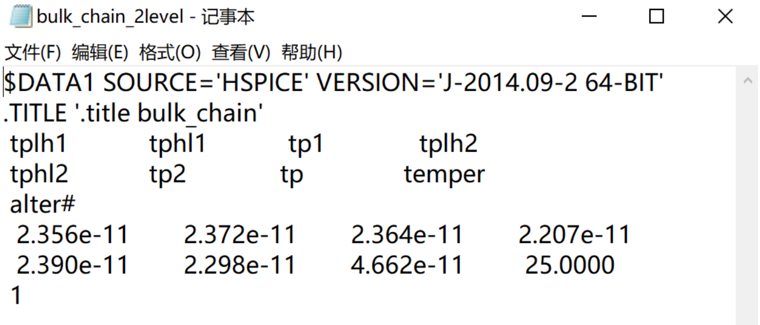
The optimal one is $f = 4, N = 4$, shown as belows:


bulk_chain_4_4level - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

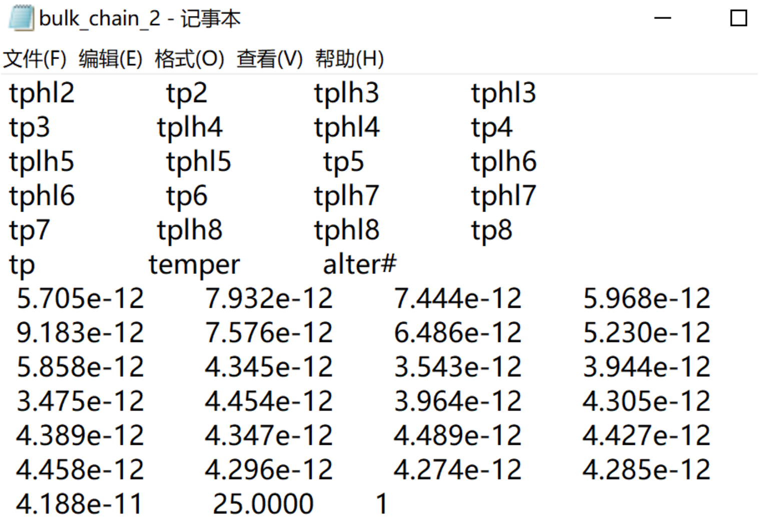
```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh1          tphl1          tp1            tplh2
 tphl2          tp2            tplh3          tphl3
 tp3            tplh4          tphl4          tp4
 tp             temper         alter#
  1.008e-11      1.159e-11      1.083e-11      8.566e-12
  1.071e-11      9.639e-12      6.776e-12      7.645e-12
  7.210e-12      6.690e-12      6.397e-12      6.543e-12
  3.211e-11       25.0000        1
```

The optimal size of the chain is 4-level with f=4

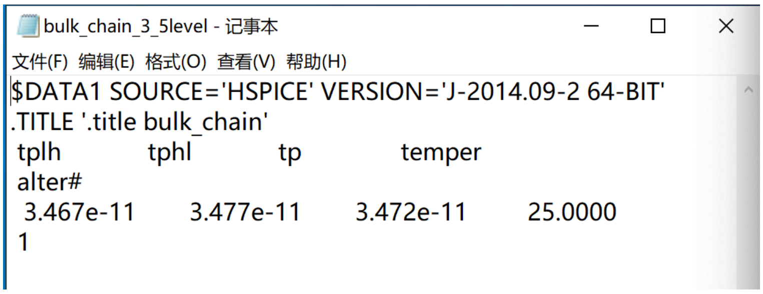
The other results are also shown as below:


bulk_chain_2level - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

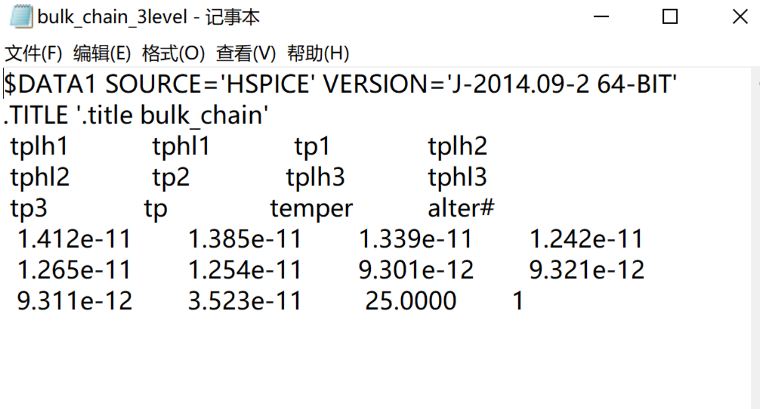
```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh1          tphl1          tp1            tplh2
 tphl2          tp2            tp             temper
 alter#
  2.356e-11      2.372e-11      2.364e-11      2.207e-11
  2.390e-11      2.298e-11      4.662e-11       25.0000
 1
```



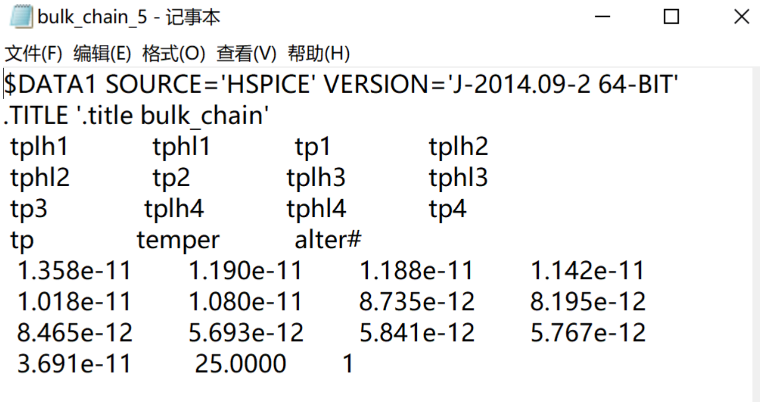
```
 tphl2          tp2            tplh3          tphl3
 tp3            tplh4          tphl4          tp4
 tplh5          tphl5          tp5            tplh6
 tphl6          tp6            tplh7          tphl7
 tp7            tplh8          tphl8          tp8
 tp             temper         alter#
  5.705e-12      7.932e-12      7.444e-12      5.968e-12
  9.183e-12      7.576e-12      6.486e-12      5.230e-12
  5.858e-12      4.345e-12      3.543e-12      3.944e-12
  3.475e-12      4.454e-12      3.964e-12      4.305e-12
  4.389e-12      4.347e-12      4.489e-12      4.427e-12
  4.458e-12      4.296e-12      4.274e-12      4.285e-12
  4.188e-11       25.0000        1
```


bulk_chain_3_5level - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh          tphl          tp            temper
 alter#
  3.467e-11     3.477e-11     3.472e-11     25.0000
 1
```


bulk_chain_3level - 记事本
文件(F) 编辑(E) 格式(O) 查看(V) 帮助(H)

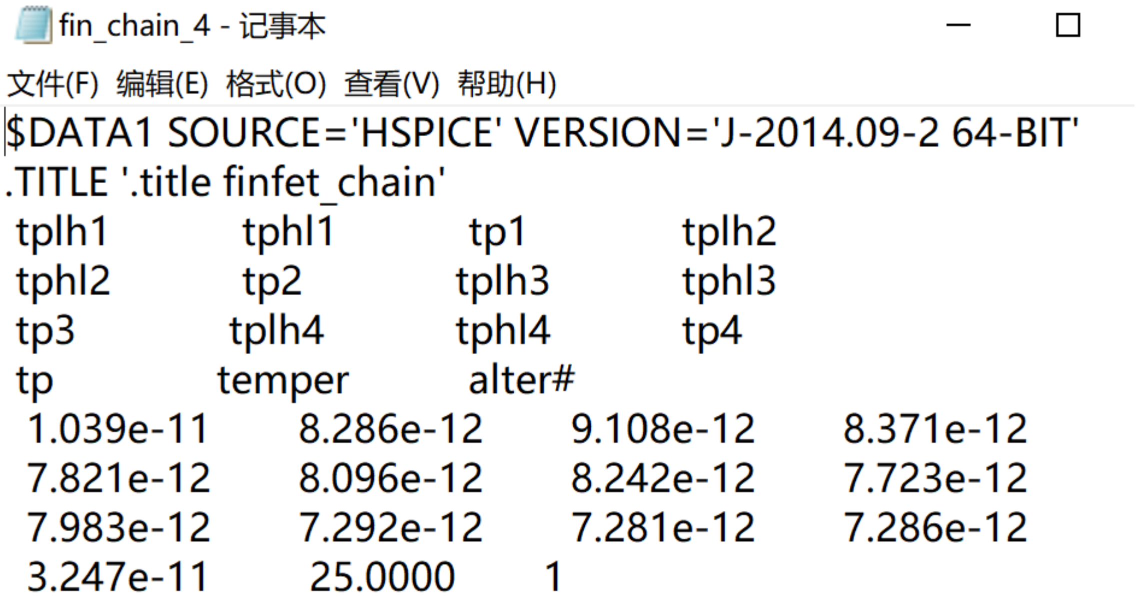
```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh1         tphl1         tp1           tplh2
 tphl2         tp2           tplh3         tphl3
 tp3           tp            temper        alter#
  1.412e-11     1.385e-11     1.339e-11     1.242e-11
  1.265e-11     1.254e-11     9.301e-12     9.321e-12
  9.311e-12     3.523e-11     25.0000       1
```



```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh1         tphl1         tp1           tplh2
 tphl2         tp2           tplh3         tphl3
 tp3           tplh4         tphl4         tp4
 tp            temper        alter#
  1.358e-11     1.190e-11     1.188e-11     1.142e-11
  1.018e-11     1.080e-11     8.735e-12     8.195e-12
  8.465e-12     5.693e-12     5.841e-12     5.767e-12
  3.691e-11     25.0000       1
```

3.2.2 FinFet

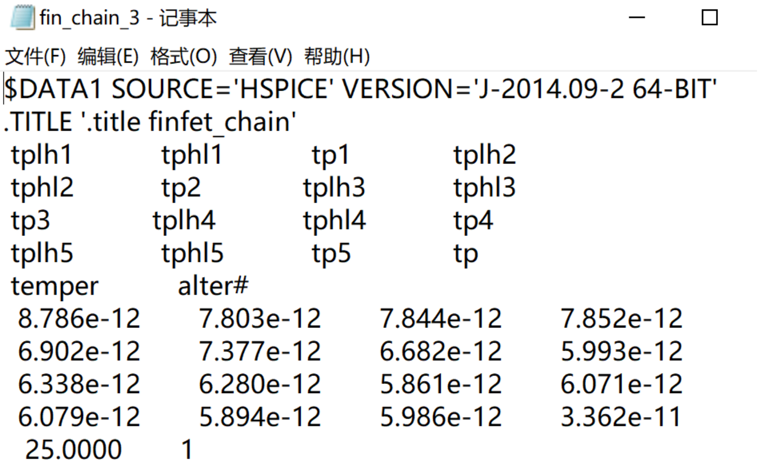
The optimal one is $f = 4, N = 4$, **shown as belows:**



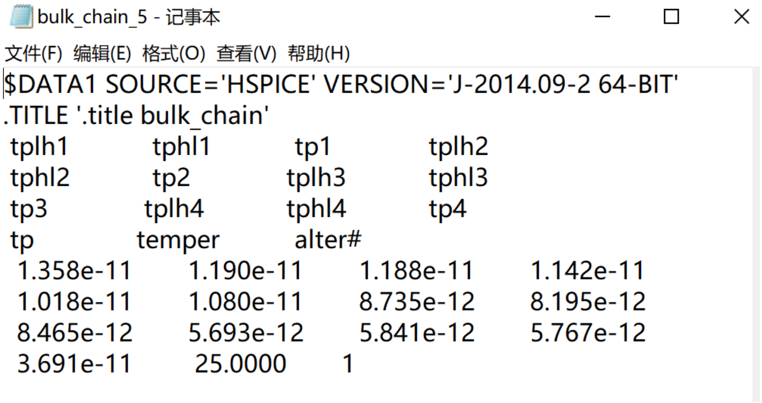
```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title finfet_chain'
 tplh1          tphl1          tp1            tplh2
 tphl2          tp2            tplh3          tphl3
 tp3            tplh4          tphl4          tp4
 tp             temper         alter#
  1.039e-11      8.286e-12      9.108e-12      8.371e-12
  7.821e-12      8.096e-12      8.242e-12      7.723e-12
  7.983e-12      7.292e-12      7.281e-12      7.286e-12
  3.247e-11       25.0000        1
```

The optimal size of the chain is 4-level with f=4, but we also found that 5-level FINFET delay is quite approached to the 4-level FINFET. I think both is alright, we choose 4-level for convenience later(You can check the code in the .zip)

The other results are also shown as below:



```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title finfet_chain'
 tplh1          tphl1          tp1            tplh2
 tphl2          tp2            tplh3          tphl3
 tp3            tplh4          tphl4          tp4
 tplh5          tphl5          tp5            tp
 temper         alter#
  8.786e-12      7.803e-12      7.844e-12      7.852e-12
  6.902e-12      7.377e-12      6.682e-12      5.993e-12
  6.338e-12      6.280e-12      5.861e-12      6.071e-12
  6.079e-12      5.894e-12      5.986e-12      3.362e-11
   25.0000        1
```

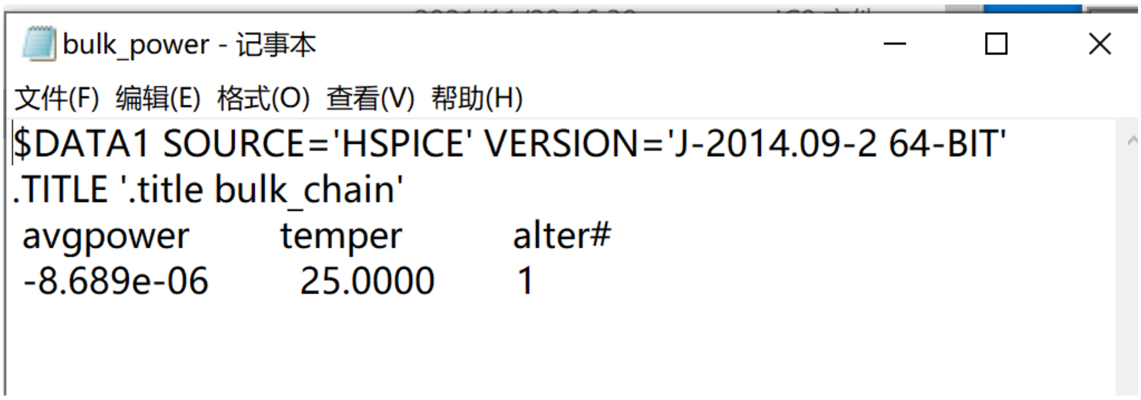


```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 tplh1          tphl1          tp1            tplh2
 tphl2          tp2            tplh3          tphl3
 tp3            tplh4          tphl4          tp4
 tp             temper         alter#
  1.358e-11      1.190e-11      1.188e-11      1.142e-11
  1.018e-11      1.080e-11      8.735e-12      8.195e-12
  8.465e-12      5.693e-12      5.841e-12      5.767e-12
  3.691e-11       25.0000       1
```

3.3 Power of Inverter Chain

3.3.1 bulk silicon

The result is shown as below:

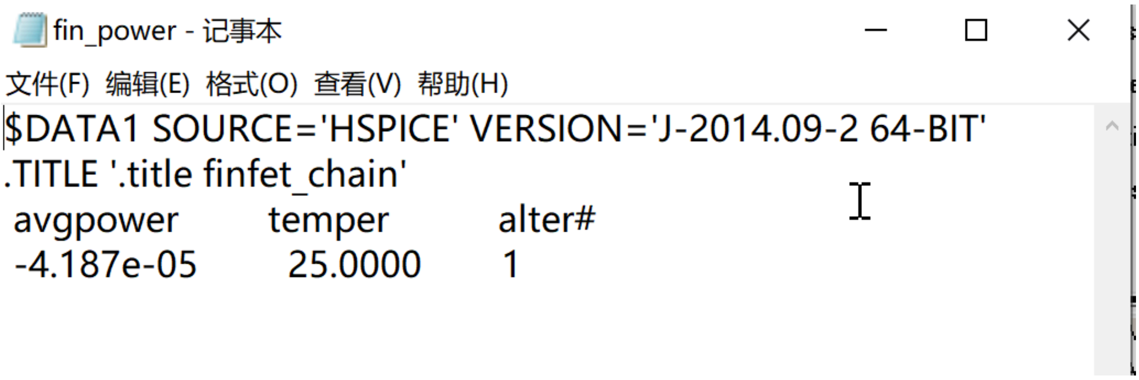


```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title bulk_chain'
 avgpower       temper         alter#
 -8.689e-06      25.0000       1
```

In this circumstance, the power of the chain is about 8.689 $\times 10^{-6} W$

3.3.2 FinFet

The result is shown as below:



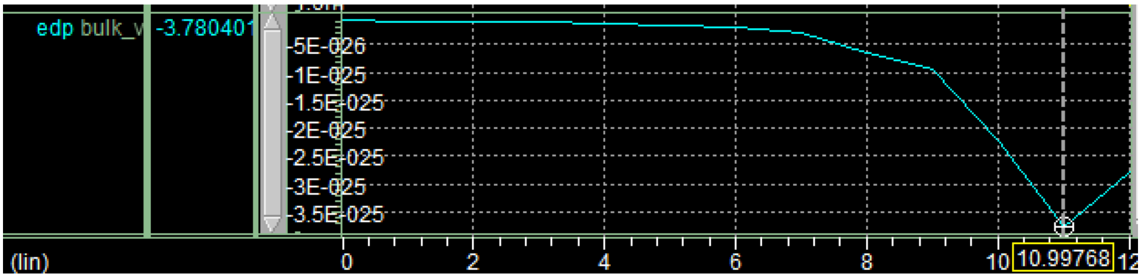
```
$DATA1 SOURCE='HSPICE' VERSION='J-2014.09-2 64-BIT'
.TITLE '.title finfet_chain'
 avgpower       temper         alter#
 -4.187e-05      25.0000       1
```

In this circumstance, the power of the chain is about 4.1876 $\times 10^{-6} W$

3.4 Optimal Vdd for Minimizing EDP

3.4.1 bulk silicon

The waveform is shown as below:



The optimal Vdd is about 1.1V

3.4.2 FinFet

The optimal Vdd is about 0.9V

4 Technical Analysis of the Simulation Results

1. Why there is a difference between $C_g(1)$ and $C_g(32)$: I'm not sure about this, I suppose it might be some parasitic capacitance in the inverter chain. There's some capacitance which is not related to the size and due to the expansion of our sweeping it will cause some little error.

2. details about propagation delay measure: The propagation delay measurement is required to measure each stage tp and sum them to get the result. At the very beginning I just measure the propagation delay from the input pin to the out load. But this is not correct due to the formula written in the slides. The propagation delay from the very beginning to the end may be come acorss a whole period which will leads to a negative tplh or tphl.

3. The 5-level and 4-level FINFET's propagation delay is quite closed to each other. In the resource code, I assign each level of the 5-level chain as 1,3,9,28,84,256. Due to the limitation that FIN-number is required to be an integer, we cannot assign them just as accurate value as the f=2.5 approxiamtely, we only can assign them as probable value. This might cause some problem due to the unequal value between each level. But I think the difference between 4-level and 5-level is quite tiny that can be ignored.

4. Power: The power is separated into 2 parts and measured by command mentioned before. This shows why we cannot design a pretty long chain. It will highly apparently increase the total power consumption and also cause a unwelcomed delay.

5 Observations and conclusions

1. More levels, more delay and power consumption.
2. Design a inverter chain is a power-efficiency trade off work. EDP is an acceptable parameter to figure out which point is the optimal one.
3. The C_g is a measurement of equal idea.