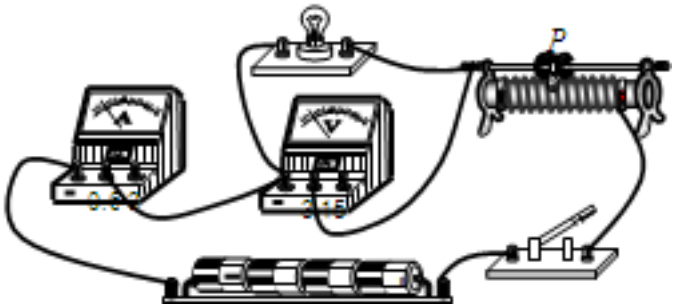
1.Introduction

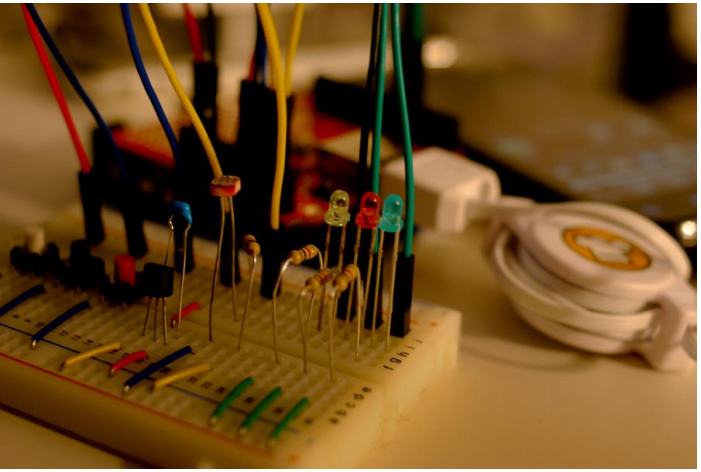
If the automobile had followed the same development cycle as the computer, a Rolls-Royce would today cost $100, get one million miles to the gallon and explode once a year

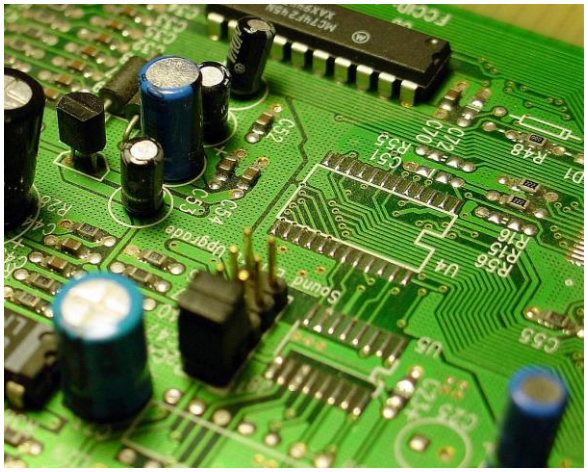
outline

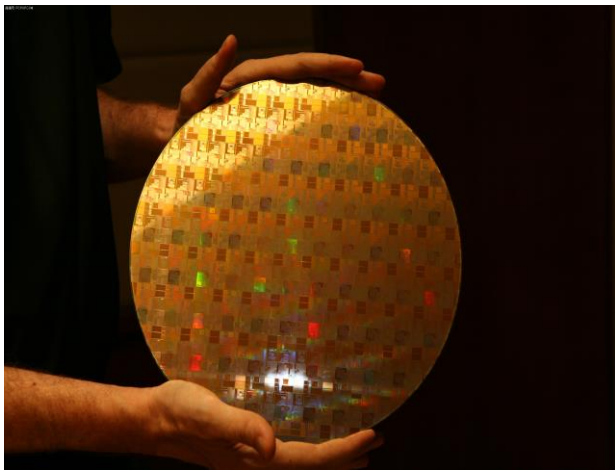
1. *Course Introduction*
2. *a brief history of IC*
3. *DIC characteristics/Design partitioning*
4. *Semiconductor processing*
5. *Layout and Testing*

How it be created?









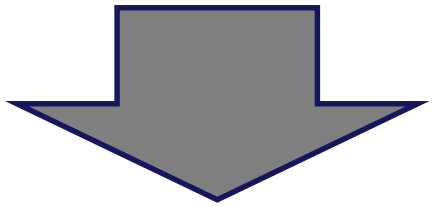
Semiconductor processing

- *Fabrication/*assembling
- Layout fundamental/testing

CMOS Fabrication

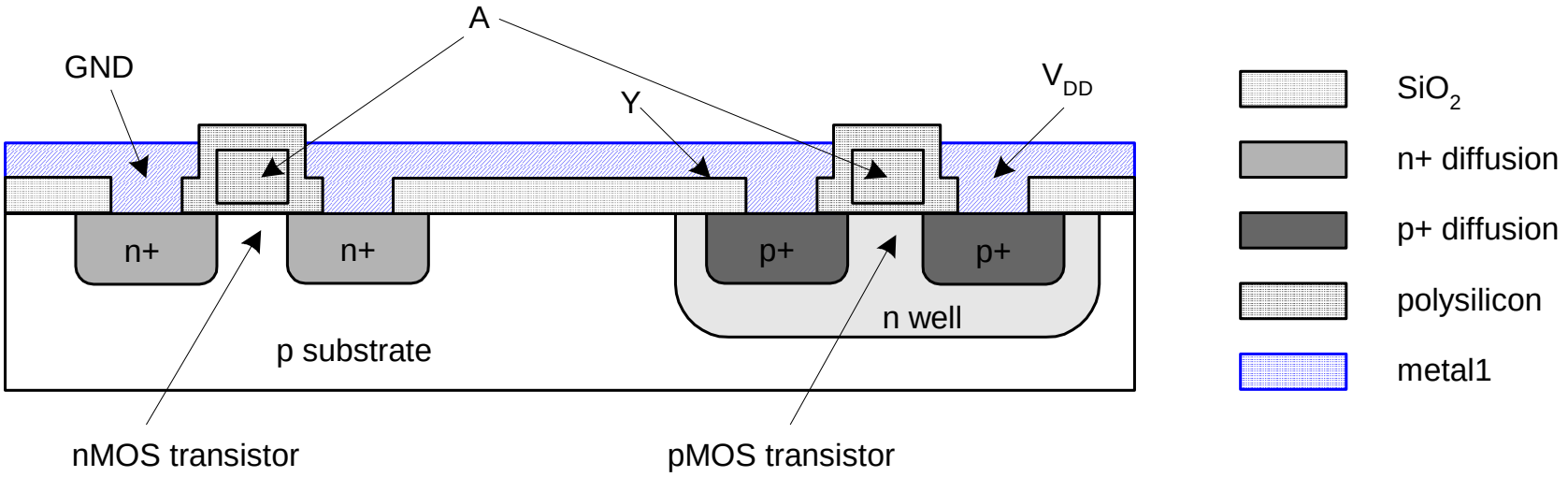
- CMOS transistors are fabricated on silicon wafer
- photolithography process similar to printing press
- On each step, different materials are deposited or etched

Easiest to understand by viewing both top and cross-section of wafer in a simplified process



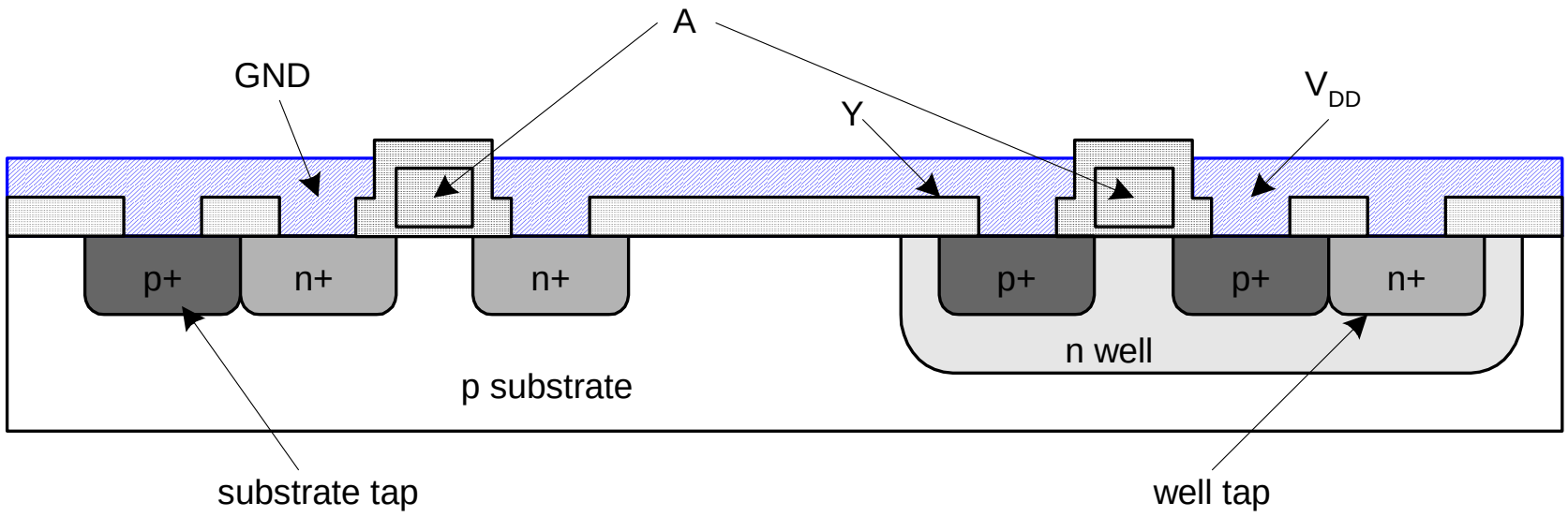
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



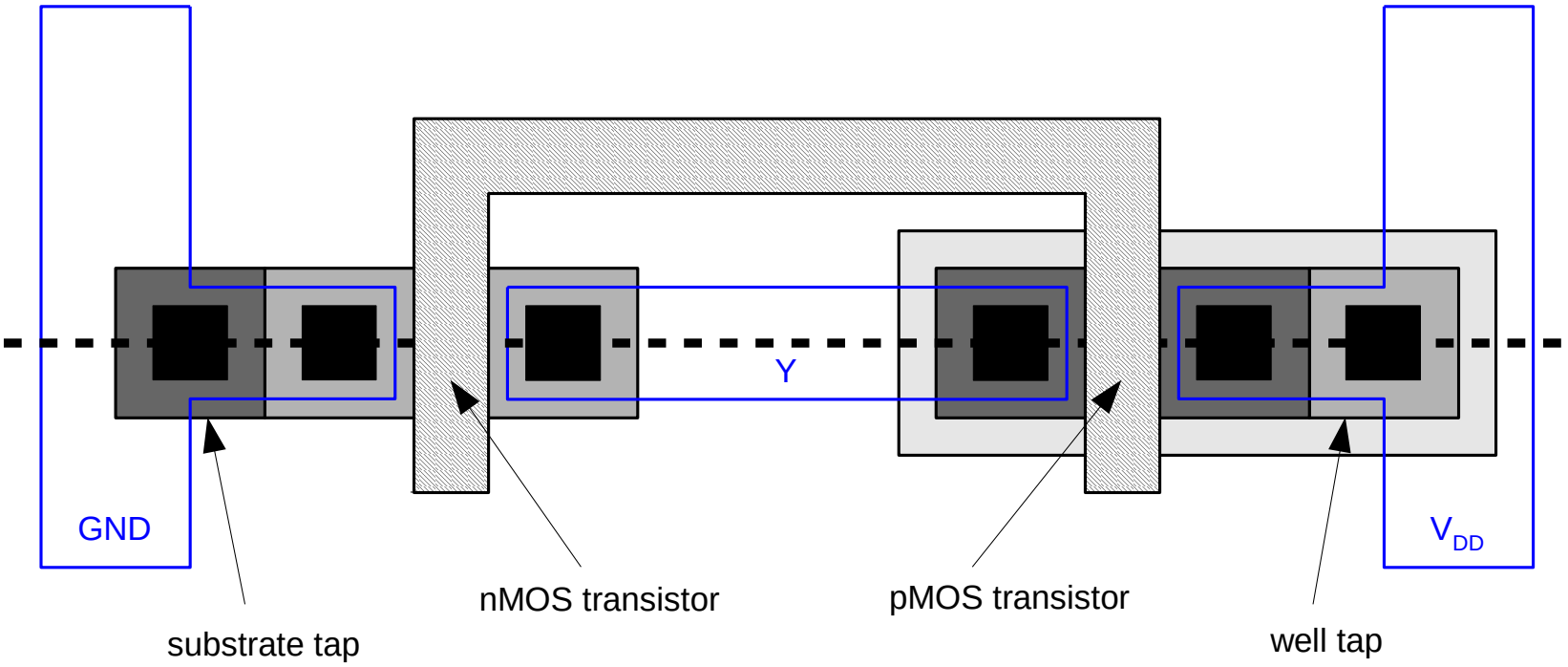
Well and Substrate Taps

- Substrate must be tied to GND and n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



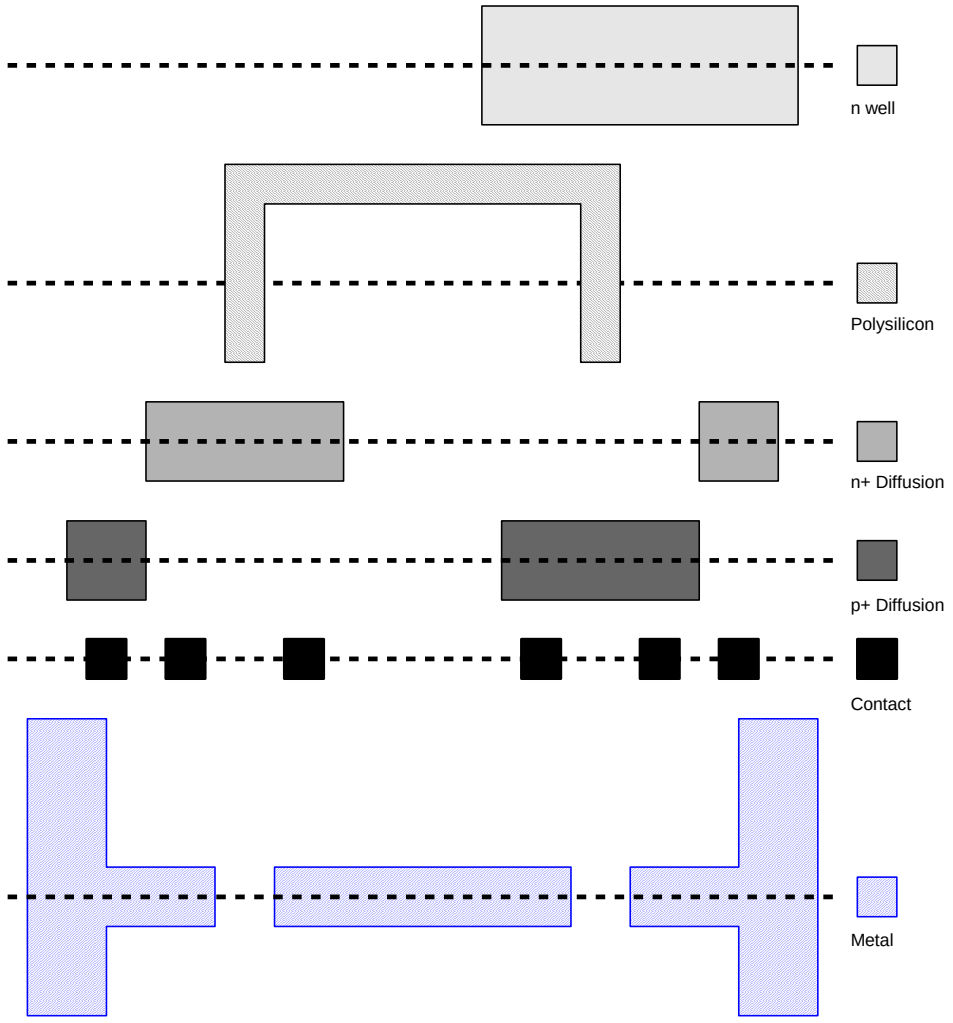
Inverter Mask Set

- Transistors and wires are defined by masks
- Cross-section taken along dashed line



Detailed Mask Views(Six masks)

- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal

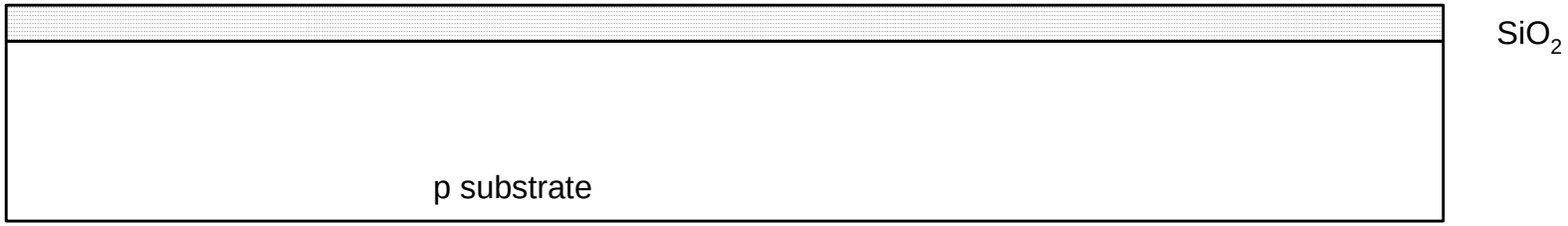


Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

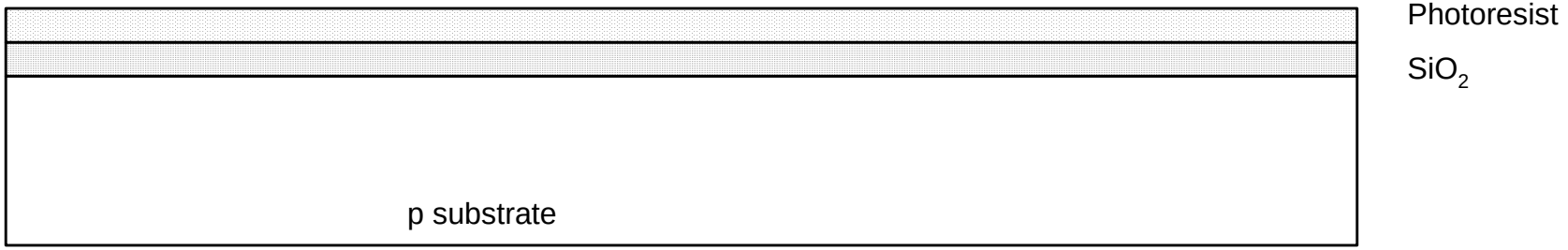
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 ºC with Si and O_2 in oxidation furnace



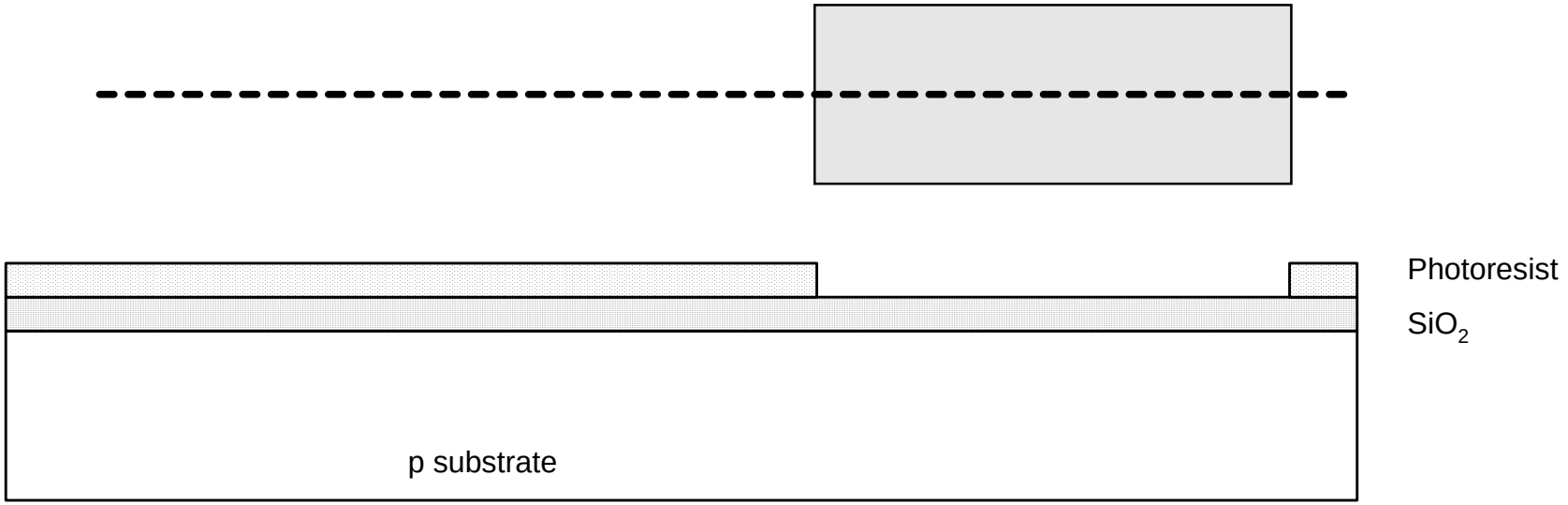
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



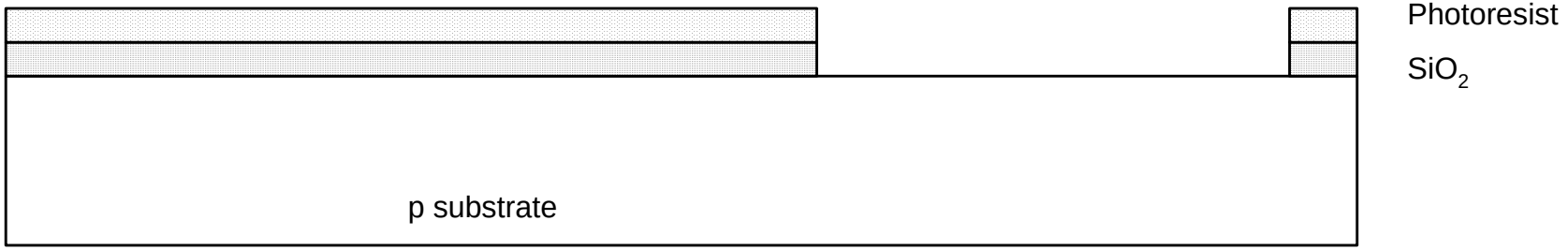
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



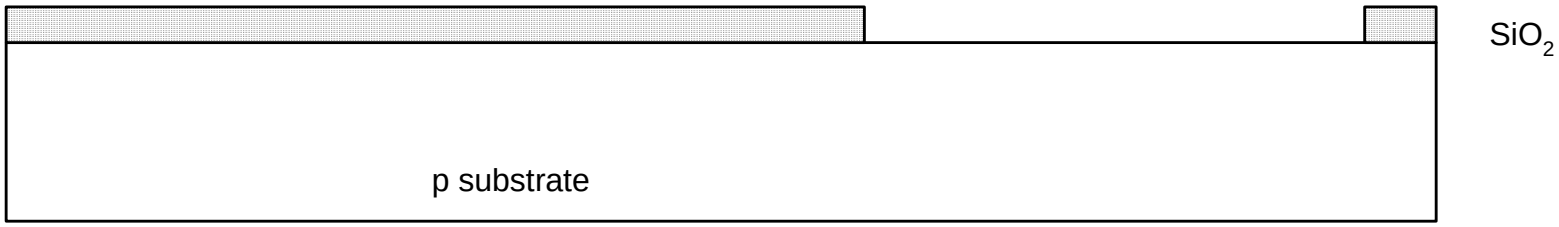
Etch

- Etch oxide with hydrofluoric acid (HF)
- Only attacks oxide where resist has been exposed



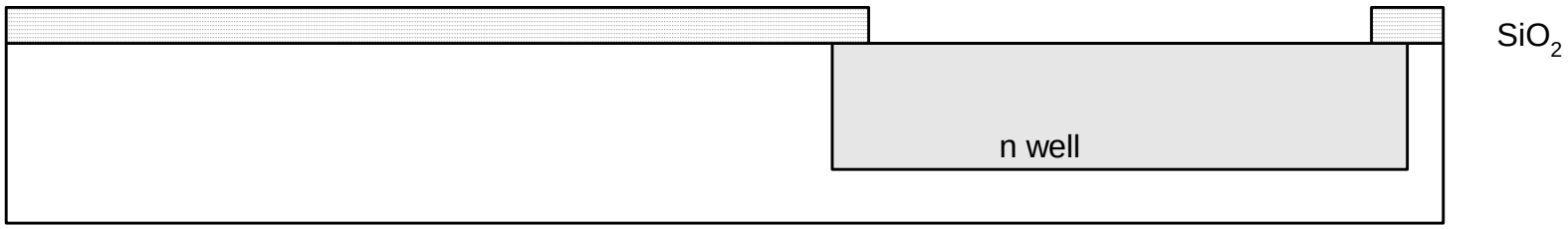
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



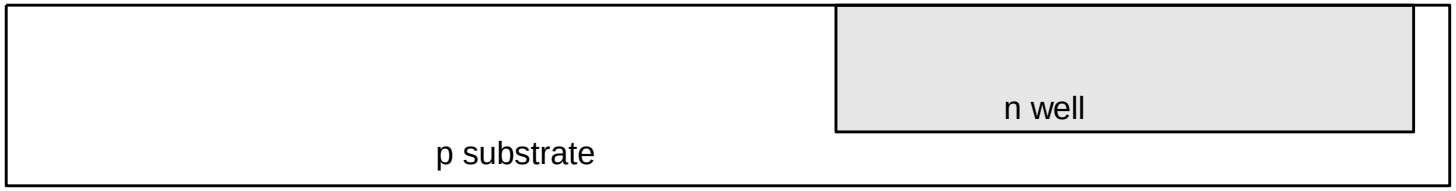
n-well

- n-well is formed with diffusion or ion implantation
- ***Diffusion***
  - Place wafer in furnace with **arsenic** gas
  - Heat until As atoms diffuse into exposed Si
- ***Ion Implanatation***
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



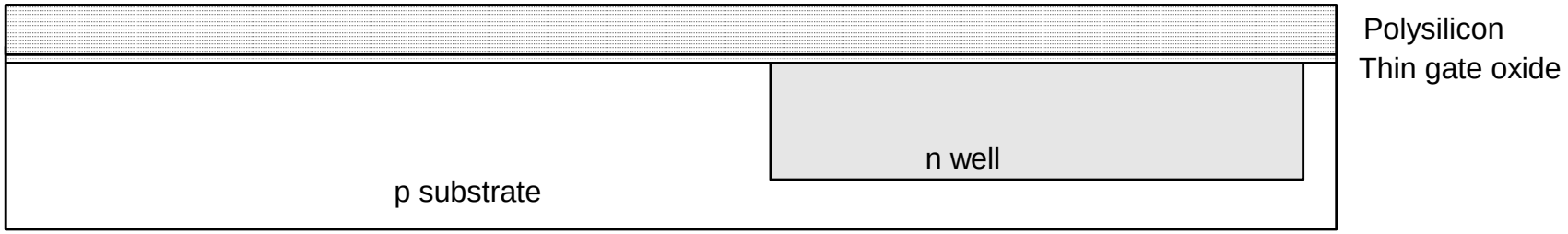
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



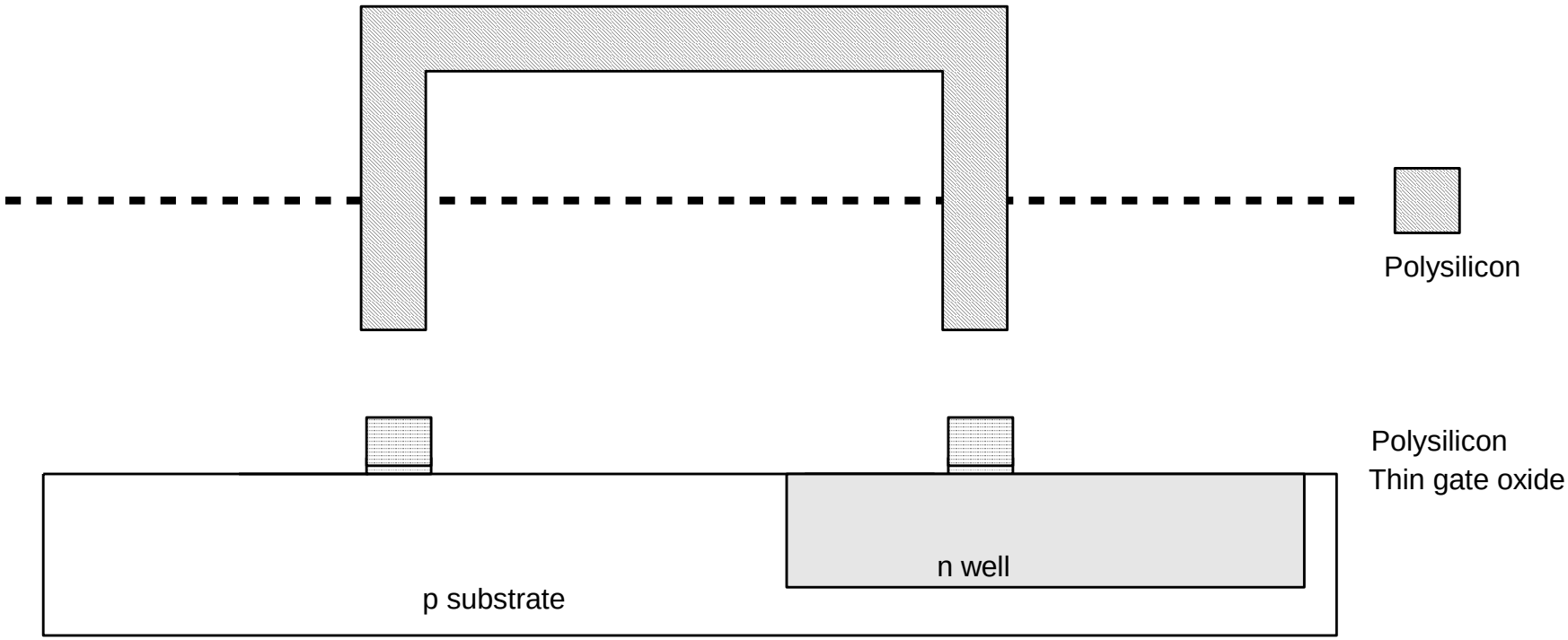
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



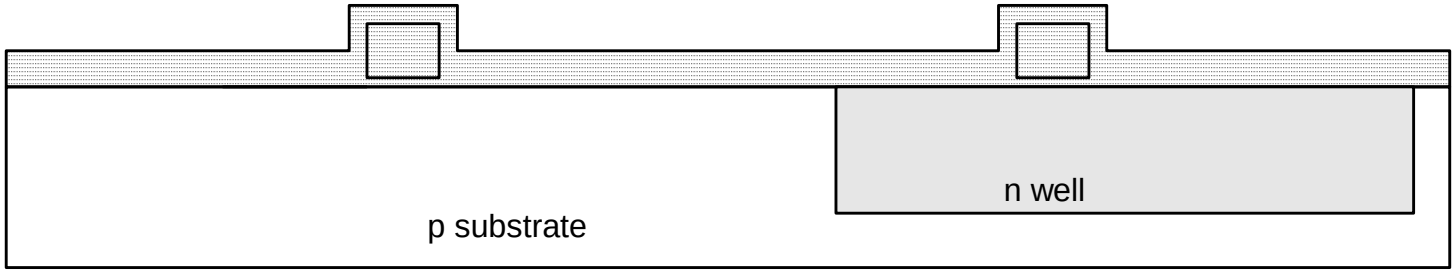
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



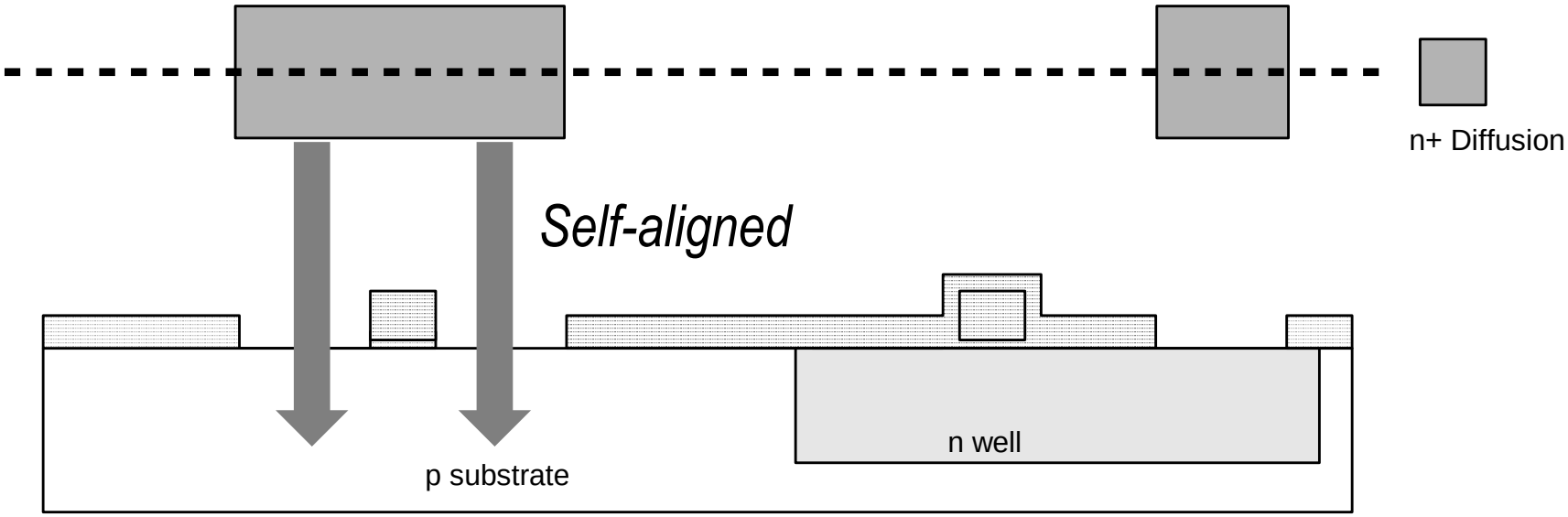
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms **nMOS source**, **drain**, and **n-well contact**



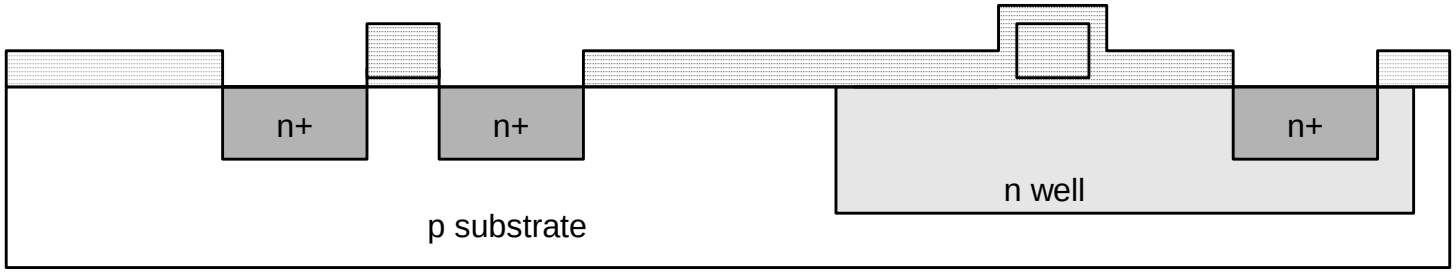
N-diffusion

- Pattern oxide and form n+ regions
- Self-aligned process where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



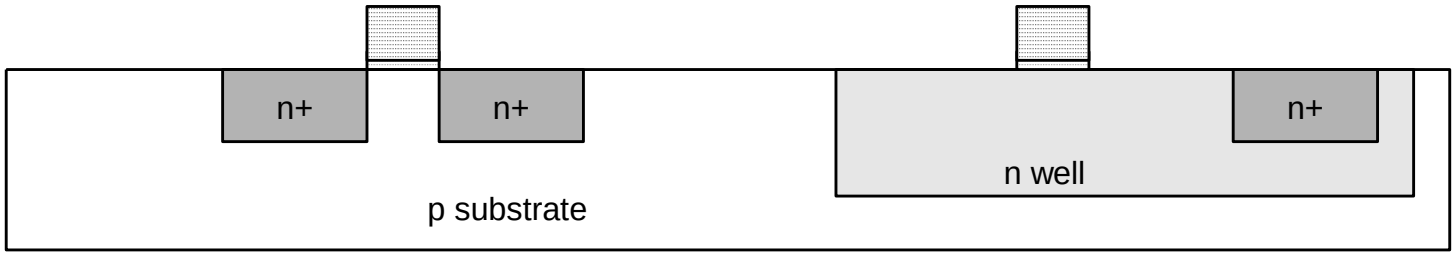
N-diffusion cont.

- Historically **dopants** were diffused
- Usually **ion implantation** today
- But regions are still called diffusion



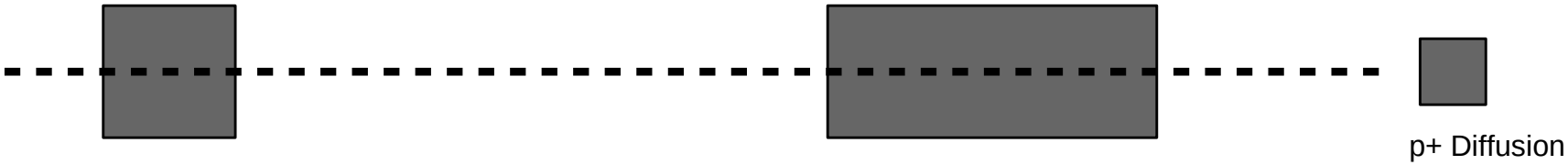
N-diffusion cont.

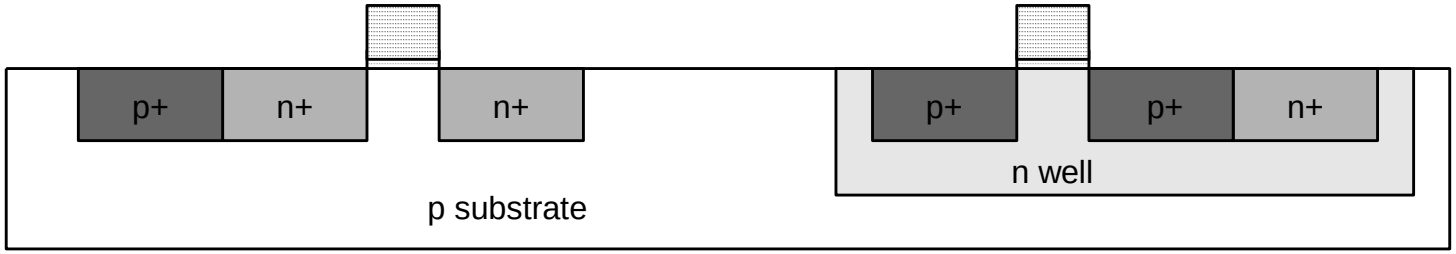
- Strip off oxide to complete patterning step



P-Diffusion

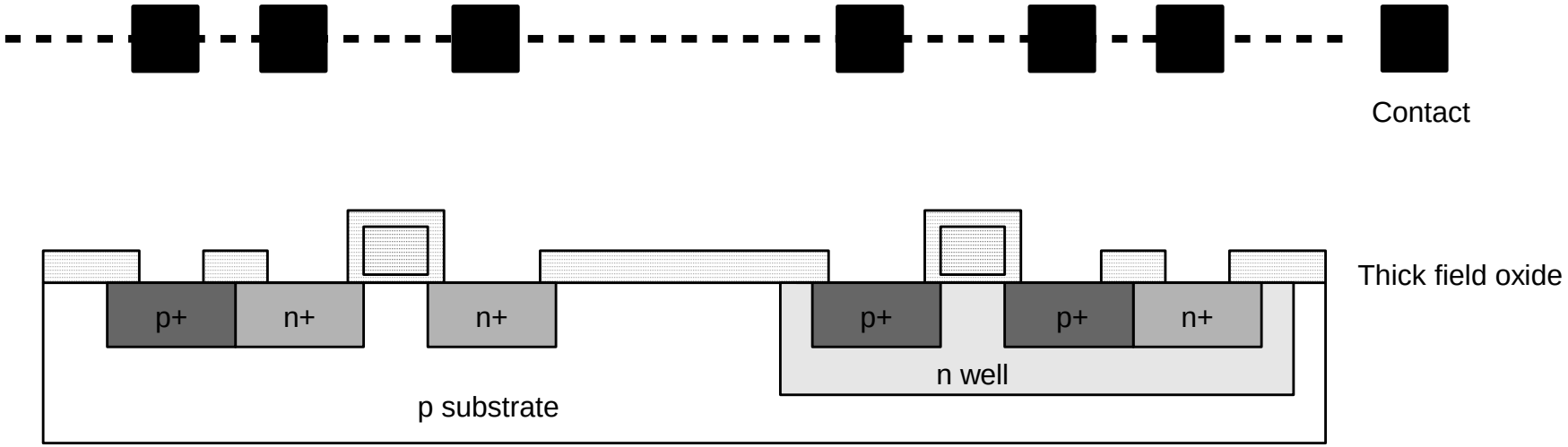
- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact





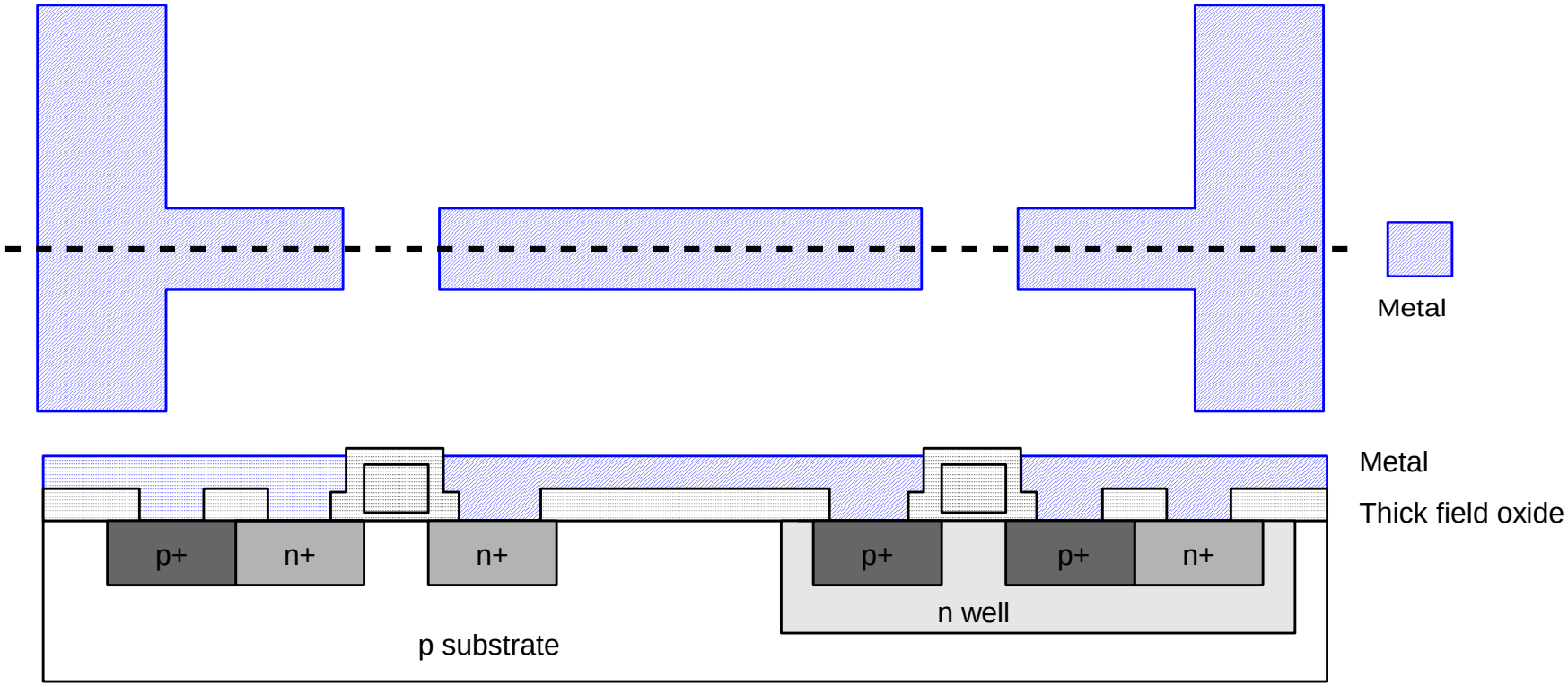
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



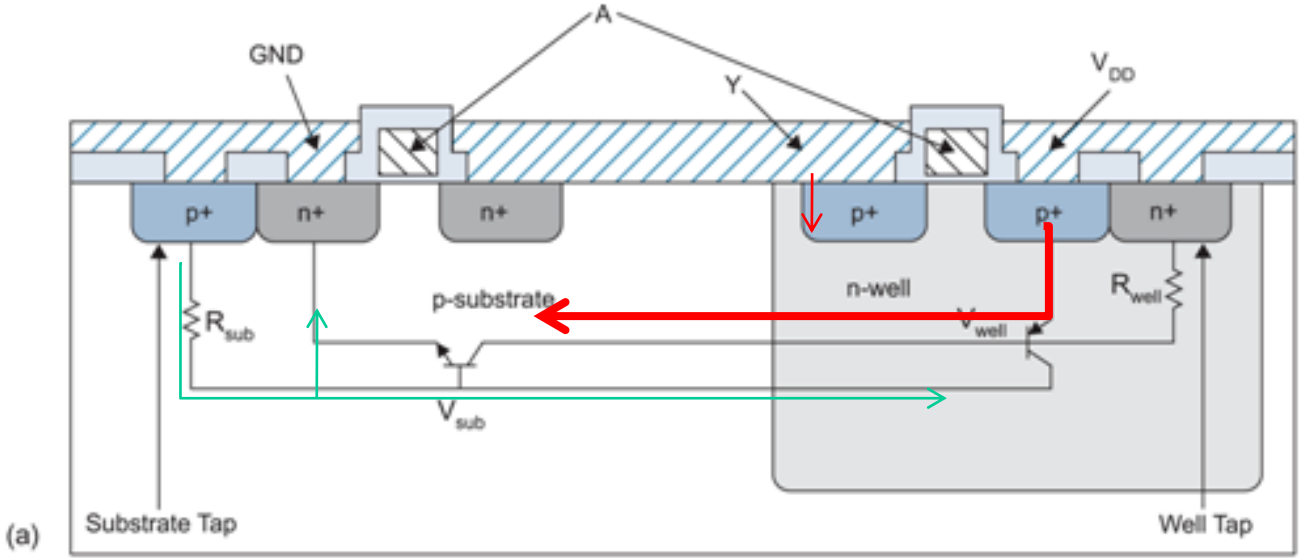
Metalization

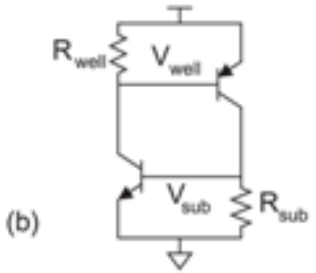
- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

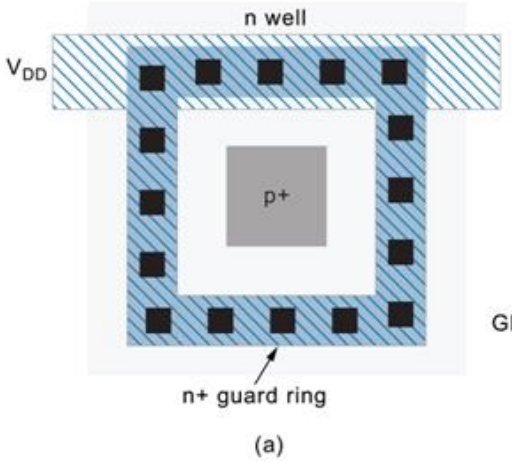


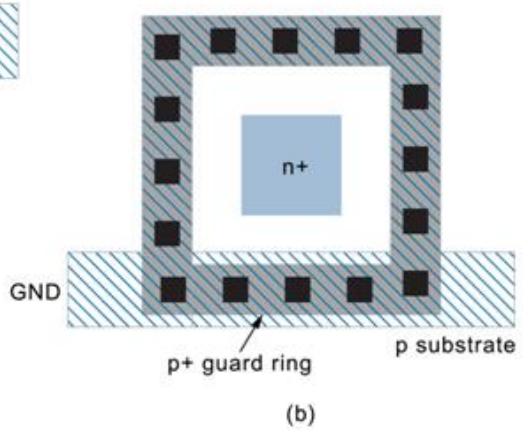
Latchup

External voltages can ring below GND or above VDD





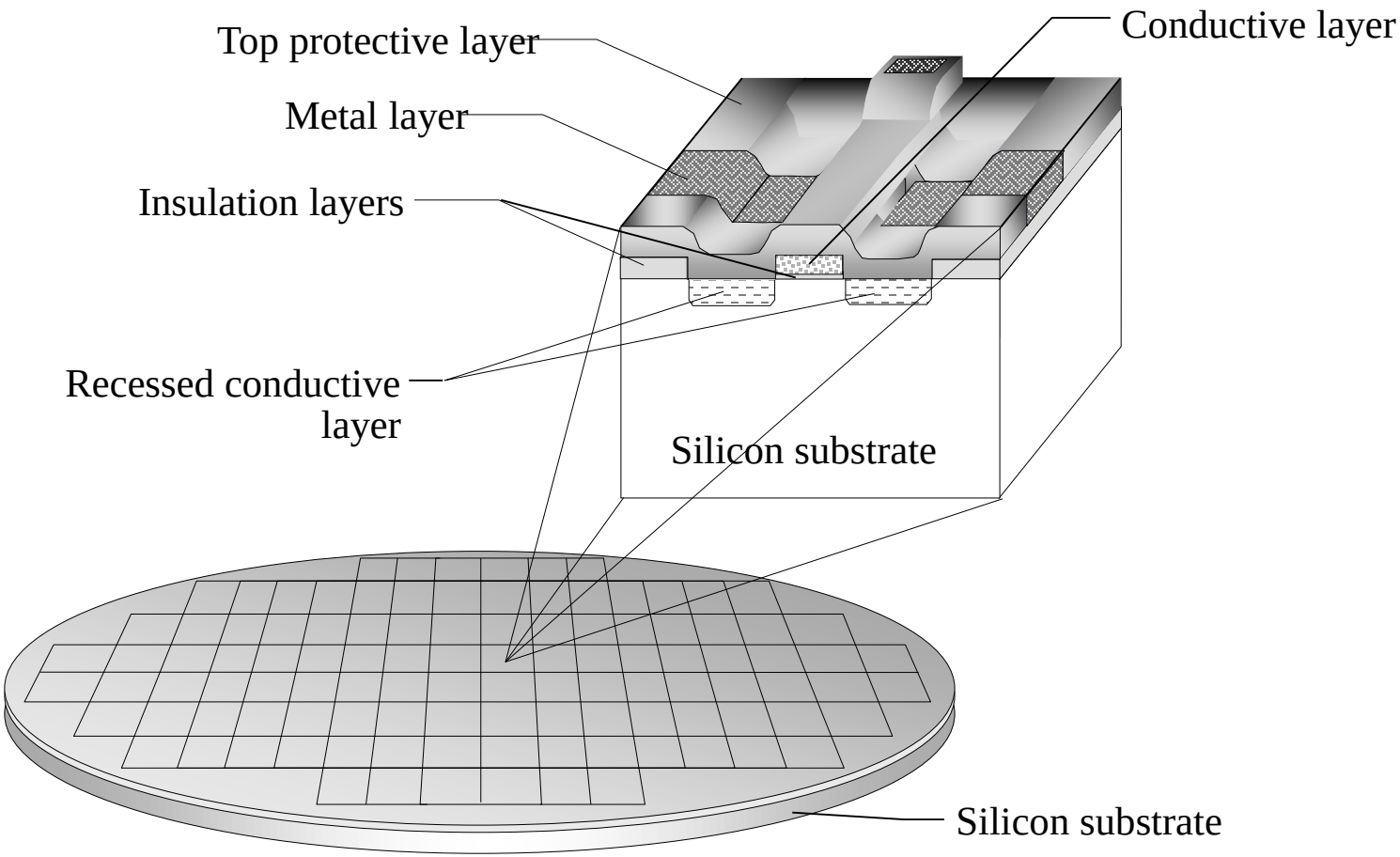




Something more…

- photolithography from Greek
- photo(light),lithos(stone),a graphe(picture) means “carving pictures in stone using light”

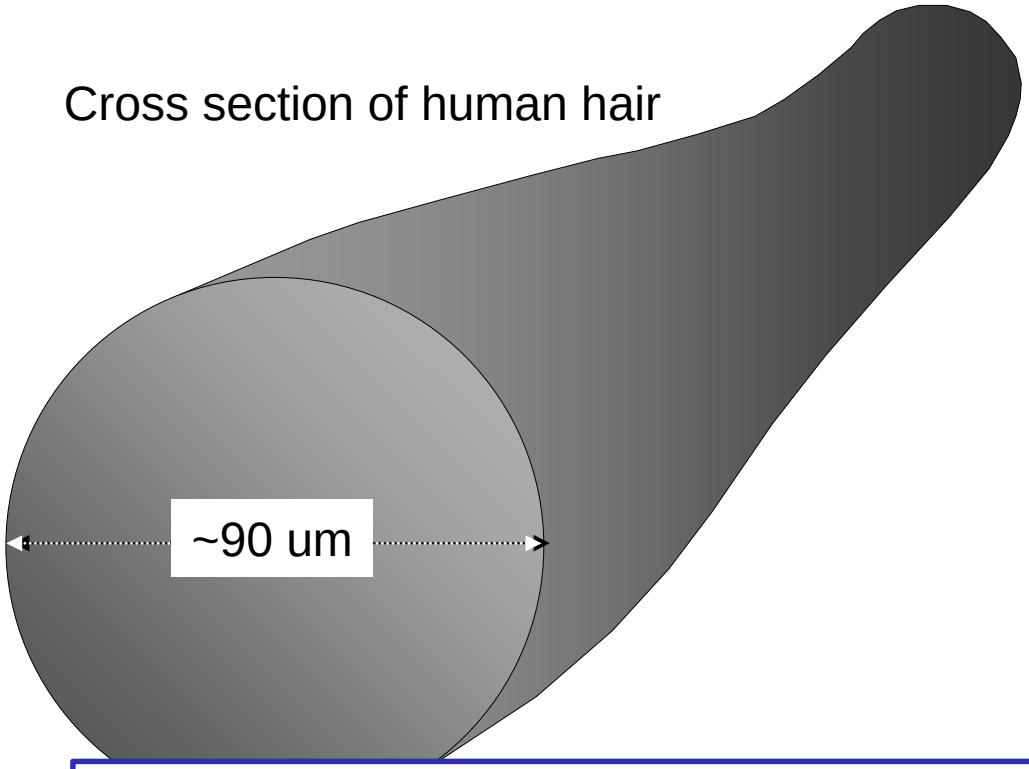
Devices and Layers from a Silicon Chip



Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

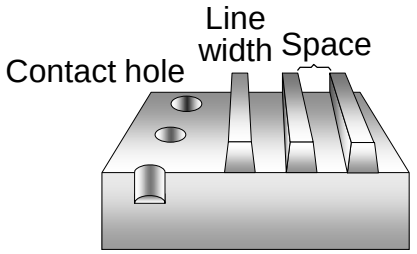
Relative Size of Human Hair to Feature Size

Cross section of human hair



Minimum IC feature size = 10nm

$$\frac{\textbf{90 um}}{\textbf{10 nm}} = \textbf{9,000}$$



The relative size of the human hair is approximately **9,000** times the size of the smallest feature size on an integrated circuit.

What is it meaning?

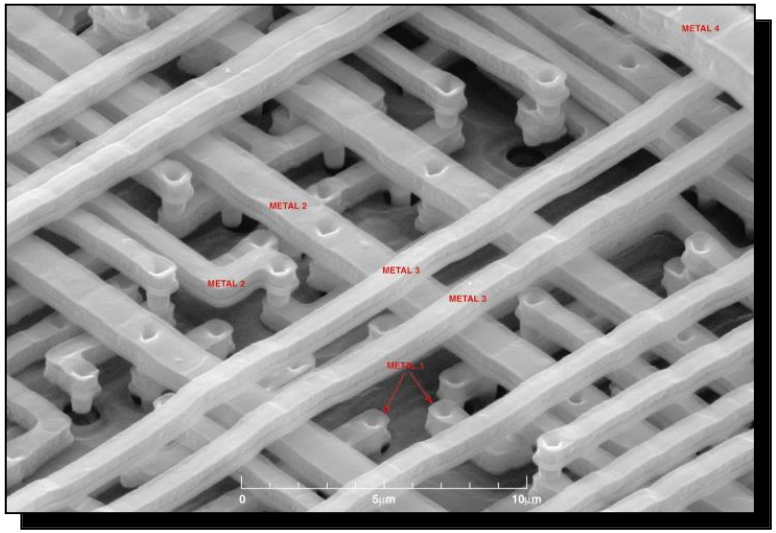
5000 acres=3*10^{7} m^{2} → ***1*10^{-3} m^{2}***

上海交通大学闵行校区二期建设规划总平面图

Same constrain as hair and CD

Stages of IC Fabrication

- Wafer preparation
- Wafer fabrication
- Wafer test/sort
- Assembly/packaging
- Final test

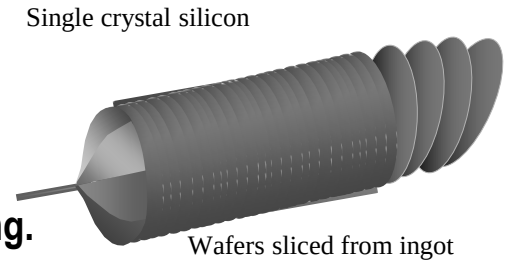


For a great tour through the IC manufacturing process and its different steps, check http://www.fullman.com/

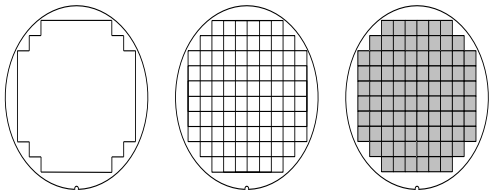
Slides reference
Semiconductor manufacturing technology
Michael Quirk, Julian Serda

Stages of IC Fabrication

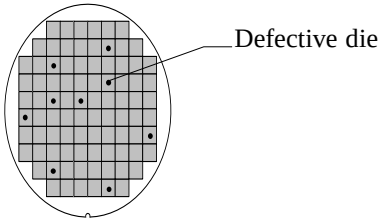
1. **Wafer Preparation includes crystal growing, rounding, slicing and polishing.**



2.

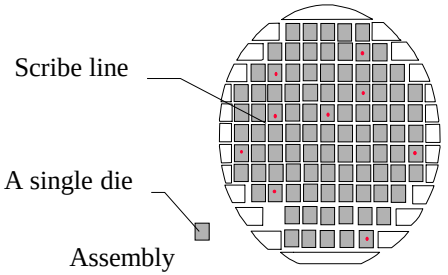


3. **Test/Sort includes probing, testing and sorting of each die on the wafer.**

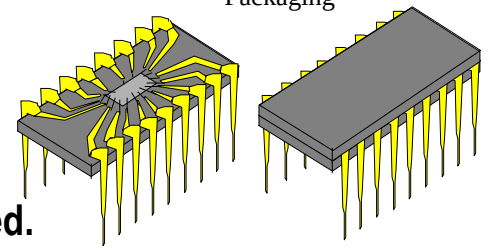


4. **Assembly and Packaging:**

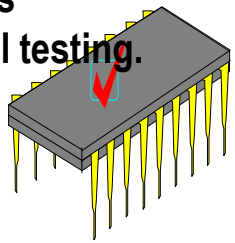
The wafer is cut along scribe lines to separate each die.



Metal connections are made and the chip is encapsulated.

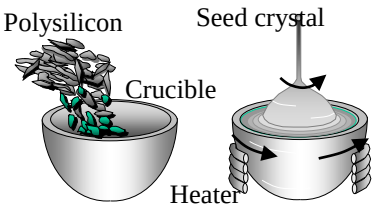


5. **Final Test ensures IC passes electrical and environmental testing.**

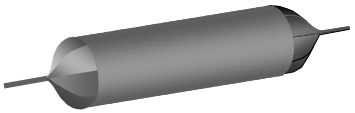


Preparation of Silicon Wafers

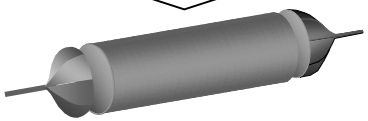
1. **Crystal Growth**



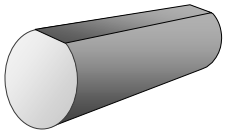
2. **Single Crystal Ingot**



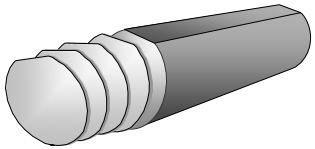
3. **Crystal Trimming and Diameter Grind**



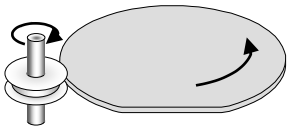
4. **Flat Grinding**



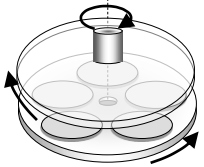
5. **Wafer Slicing**



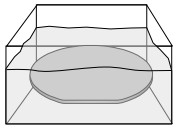
6. **Edge Rounding**



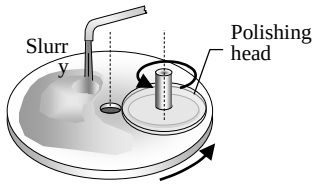
7. **Lapping**



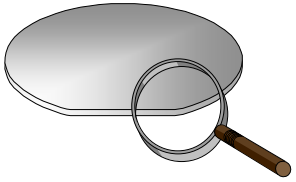
8. **Wafer Etching**



9. **Polishing**

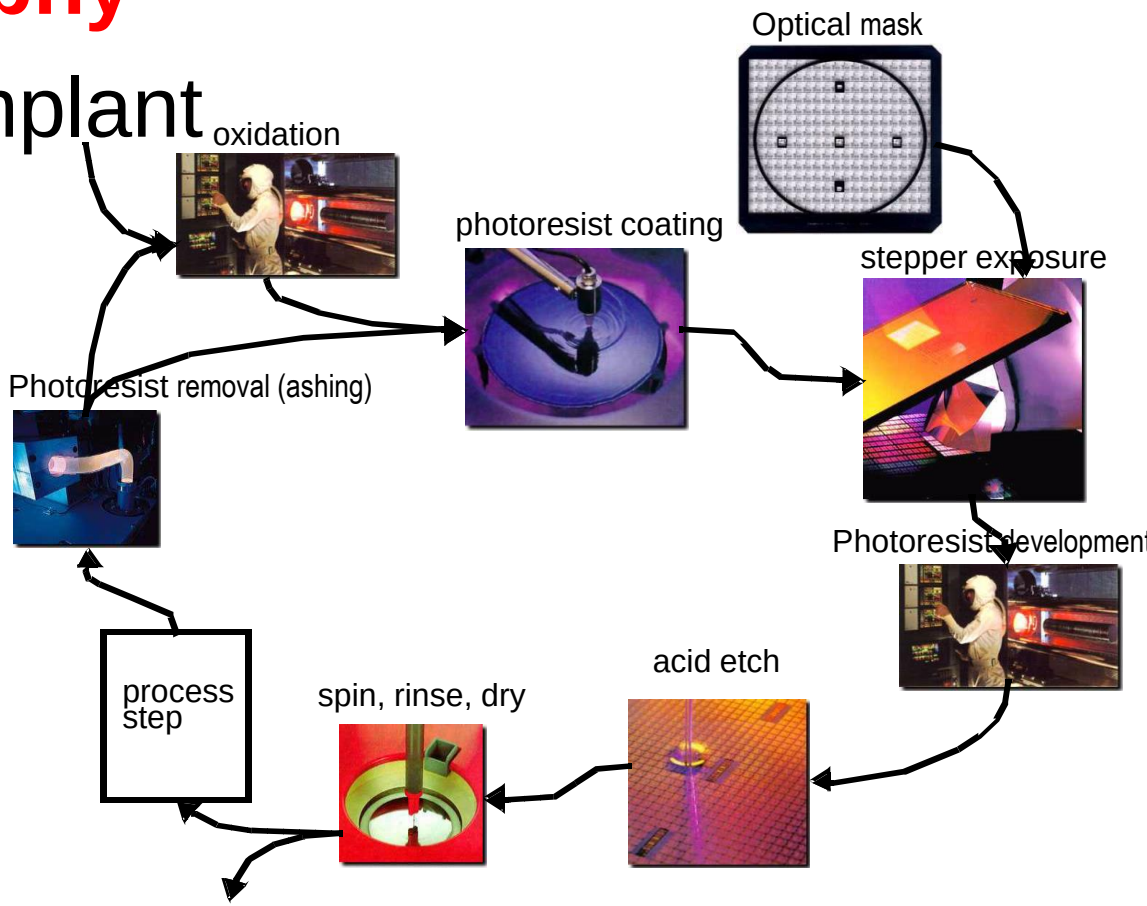


10. **Wafer Inspection**



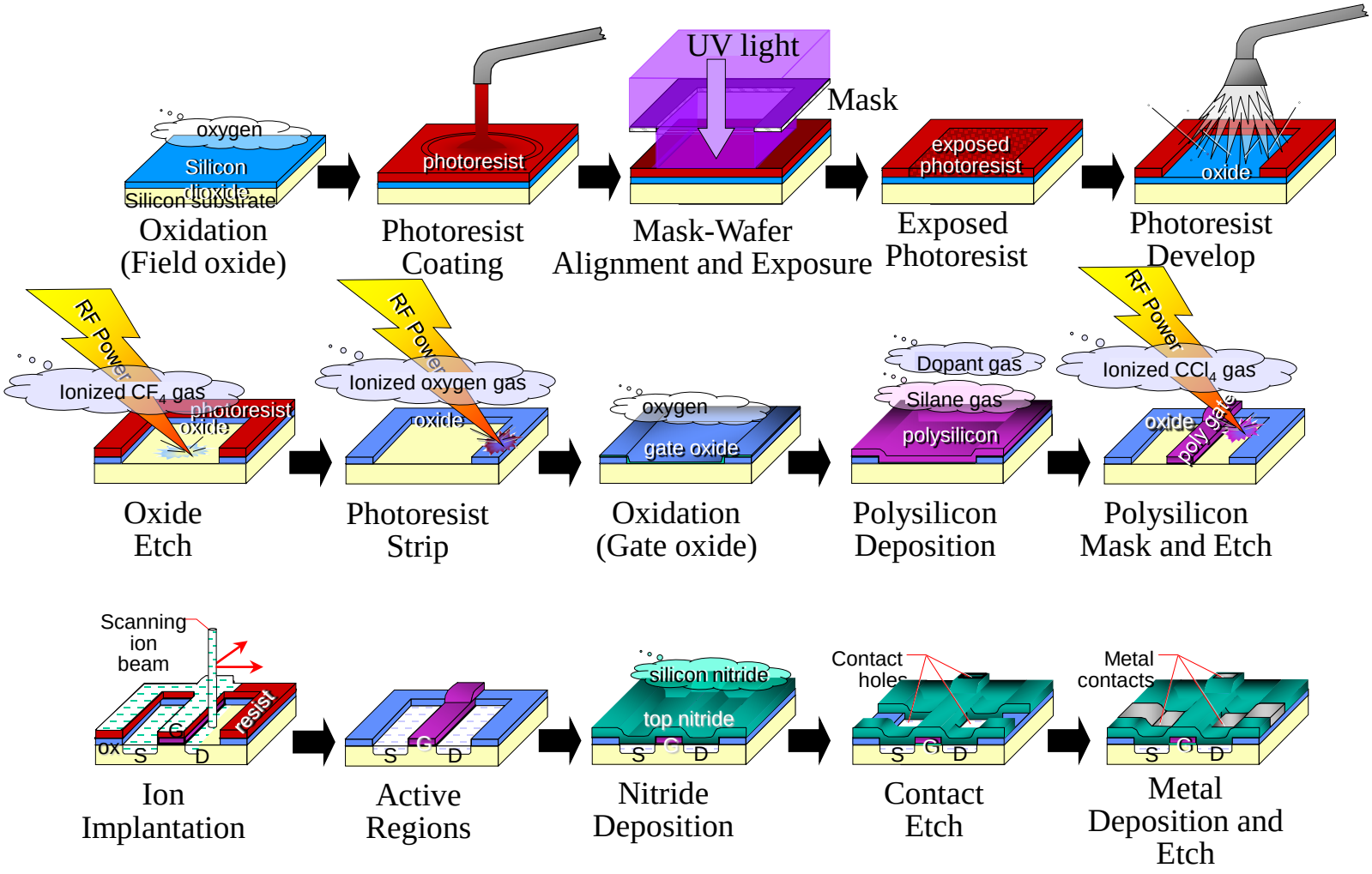
CMOS Process Flow

- **Photolithography**
- Diffusion/Ion Implant
- Polish
- Etch
- Thin Films

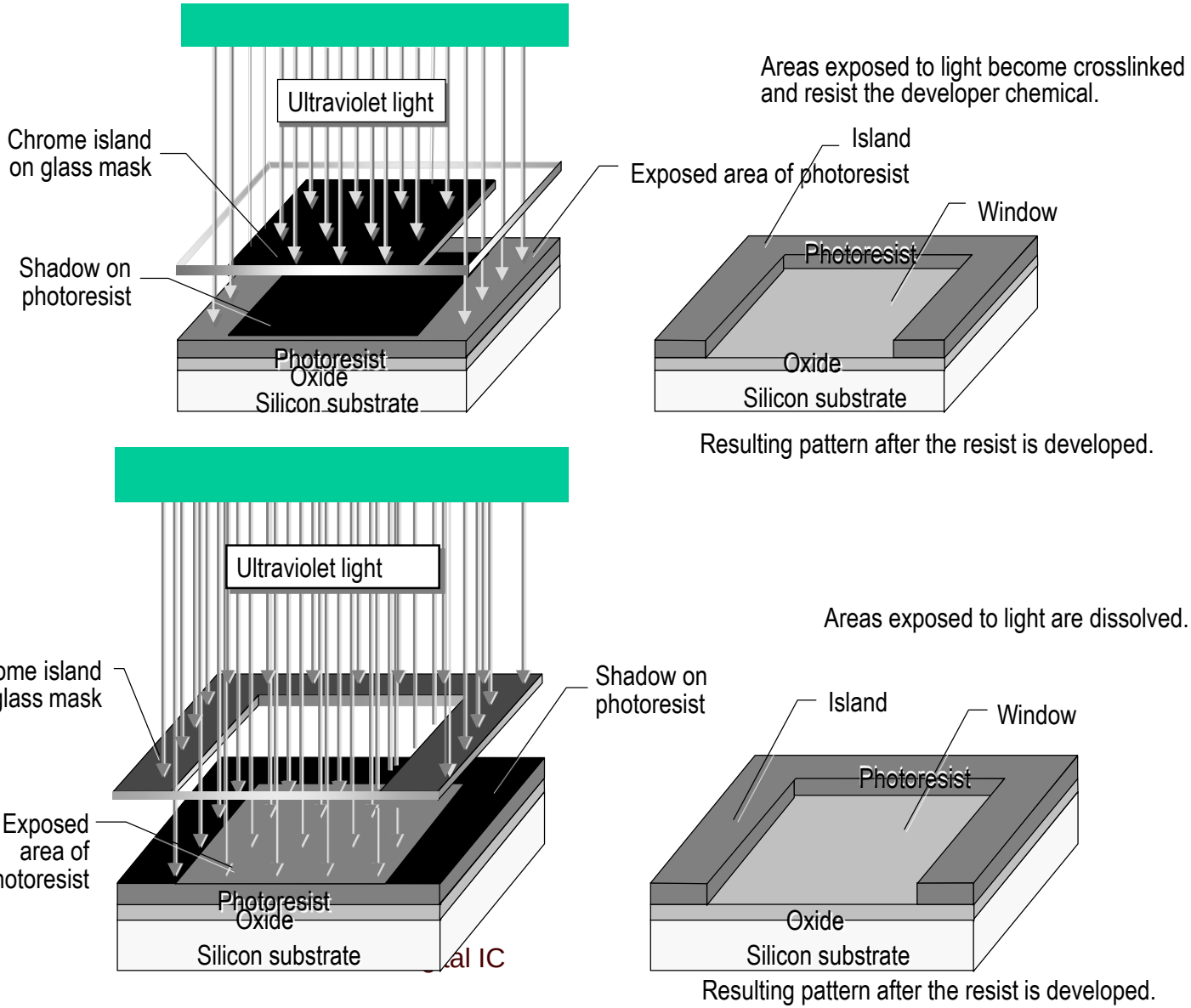


a typical Photo-Lithographic Process cycle

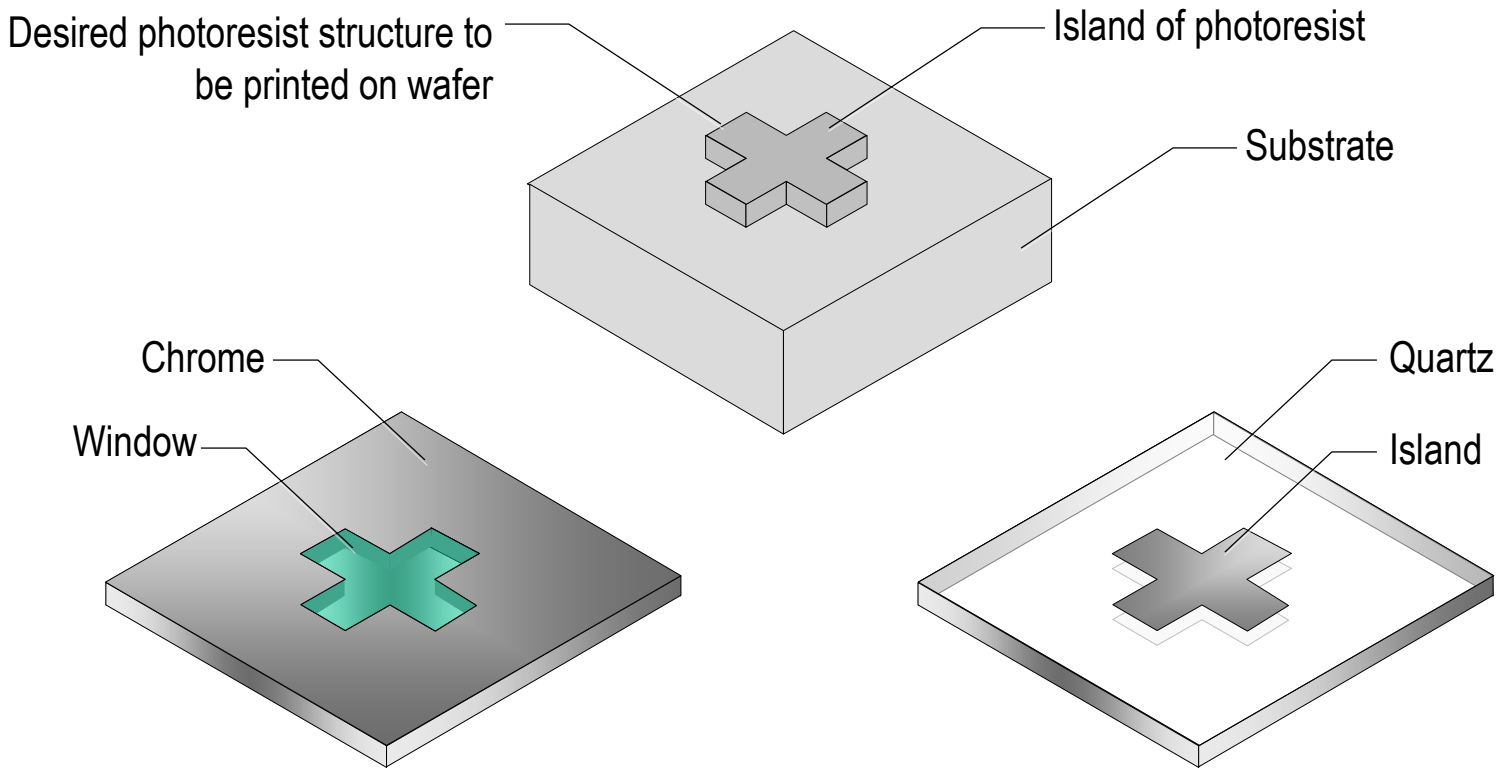
Major Fabrication Steps in MOS Process Flow



Negative/Positive Lithography



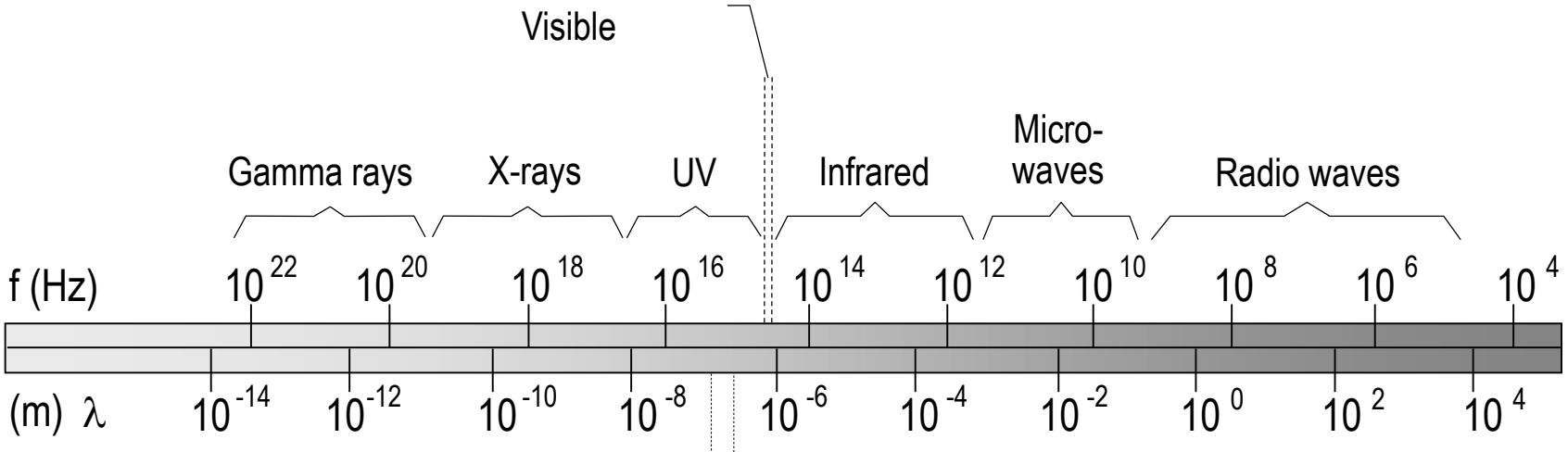
Relationship Between Mask and Resist

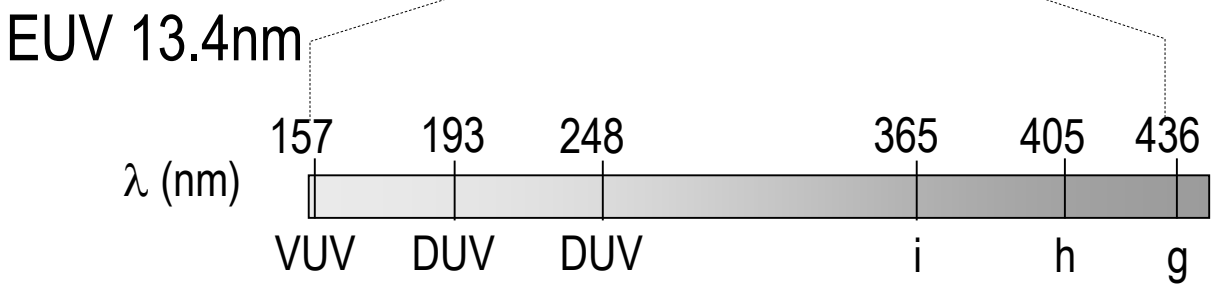


Mask pattern required when using ***negative*** photoresist (opposite of intended structure)

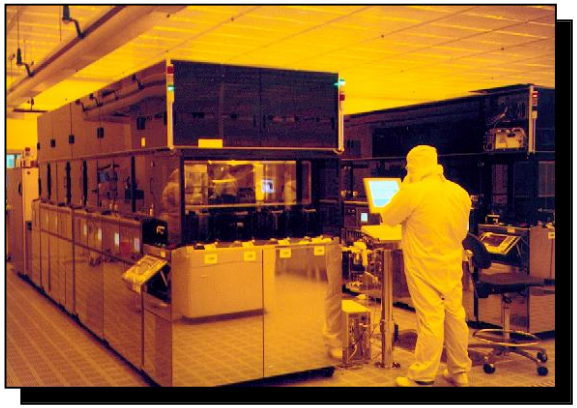
Mask pattern required when using ***positive*** photoresist (same as intended structure)

Important Wavelengths for Photolithography Exposure





Common UV wavelengths used in optical lithography.

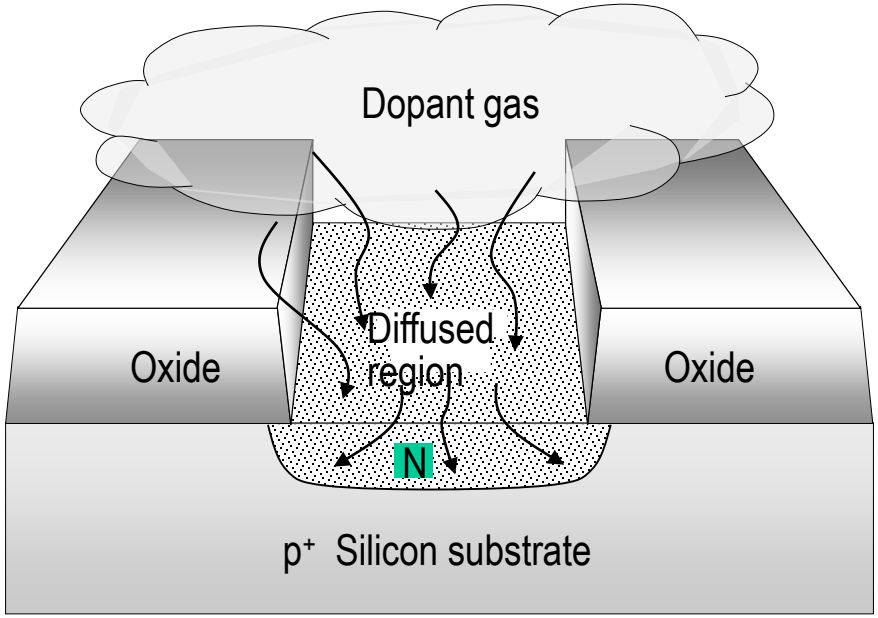


CMOS Process Flow

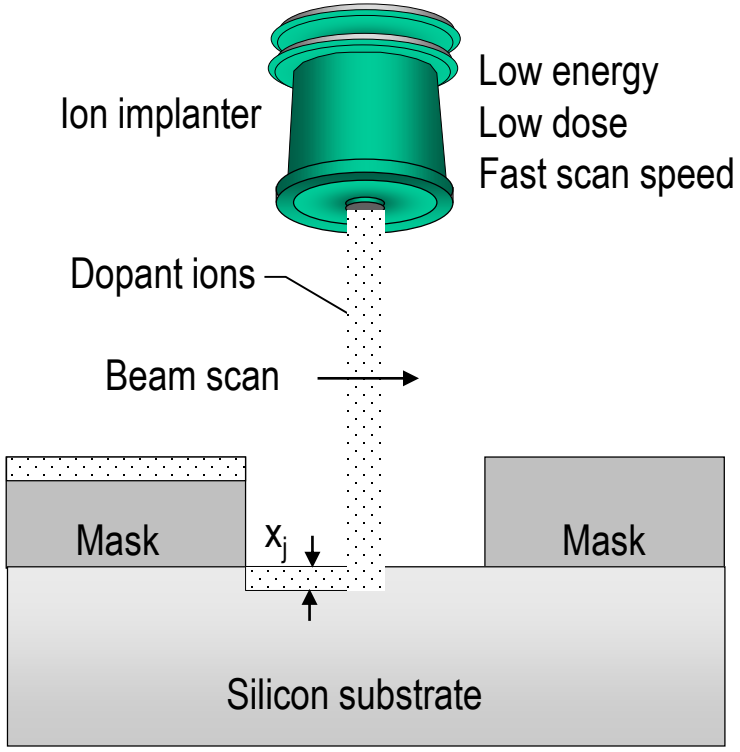
- Photolithography
- ***Diffusion/Ion Implant***
- Polish
- Etch
- Thin Films

Doped Region in a Silicon Wafer

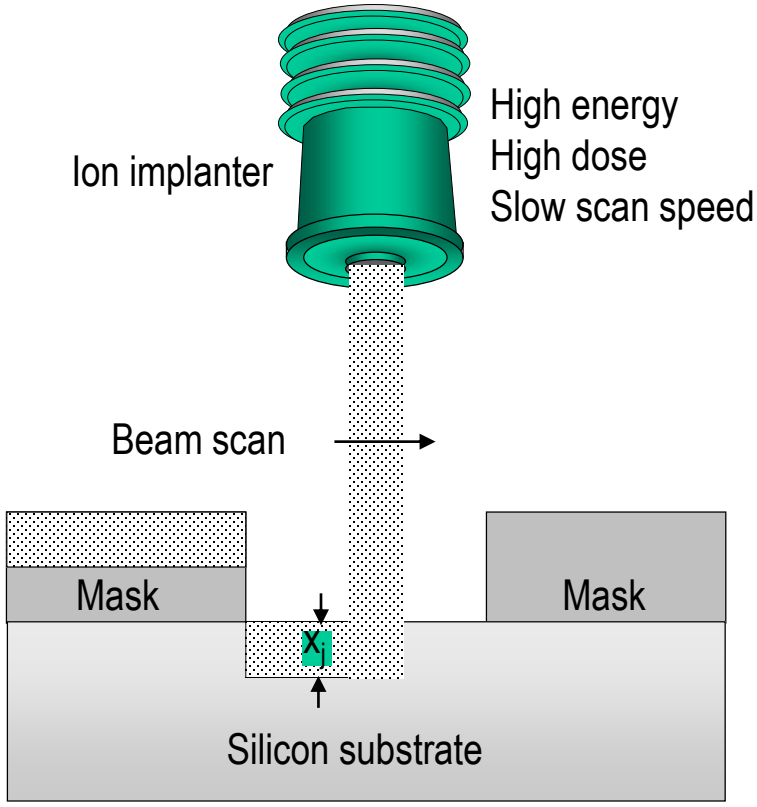
- Diffusion Principles
  - Three Steps
    - Predeposition
    - Drive-in
    - Activation
  - Dopant Movement
  - Solid Solubility
  - Lateral Diffusion
- Diffusion Process
  - Wafer Cleaning
  - Dopant Sources



Controlling Dopant Concentration and Depth



a) Low dopant concentration (n^-, p^-) and shallow junction (x_j)

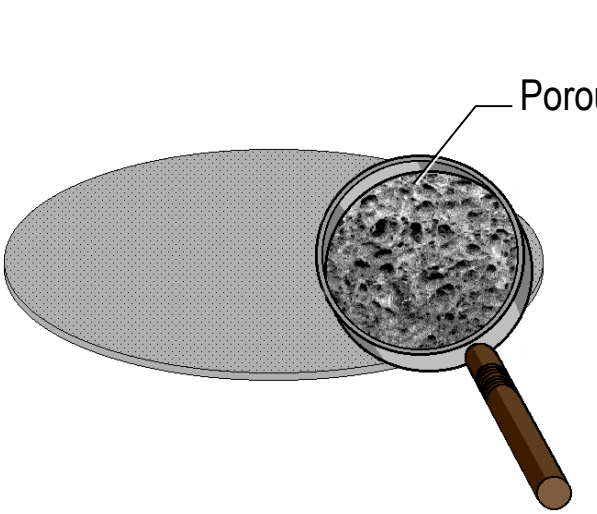


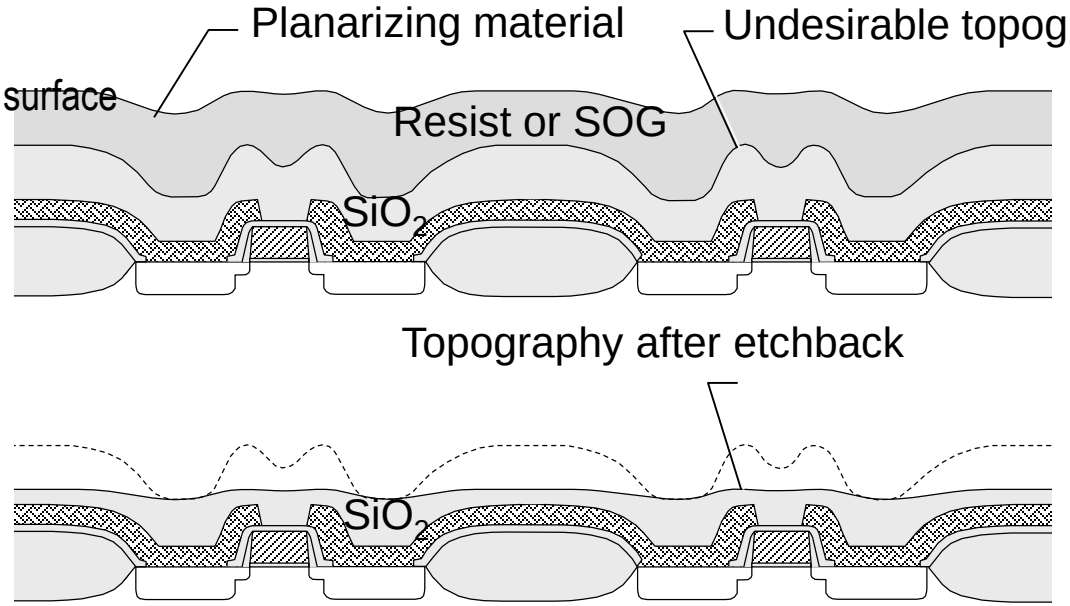
b) High dopant concentration (n^+, p^+) and deep junction (x_j)

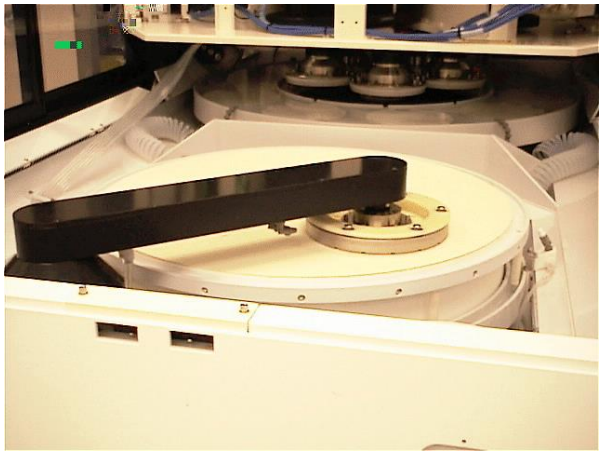
CMOS Process Flow

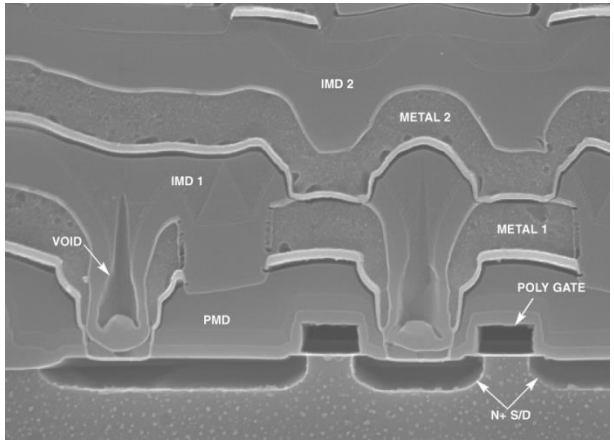
- Photolithography
- Diffusion/Ion Implant
- **Polish/Etch**
- Thin Films

CMP Polishing Pad/Etchback Planarization

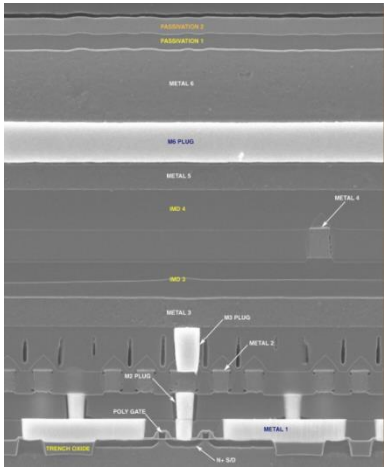






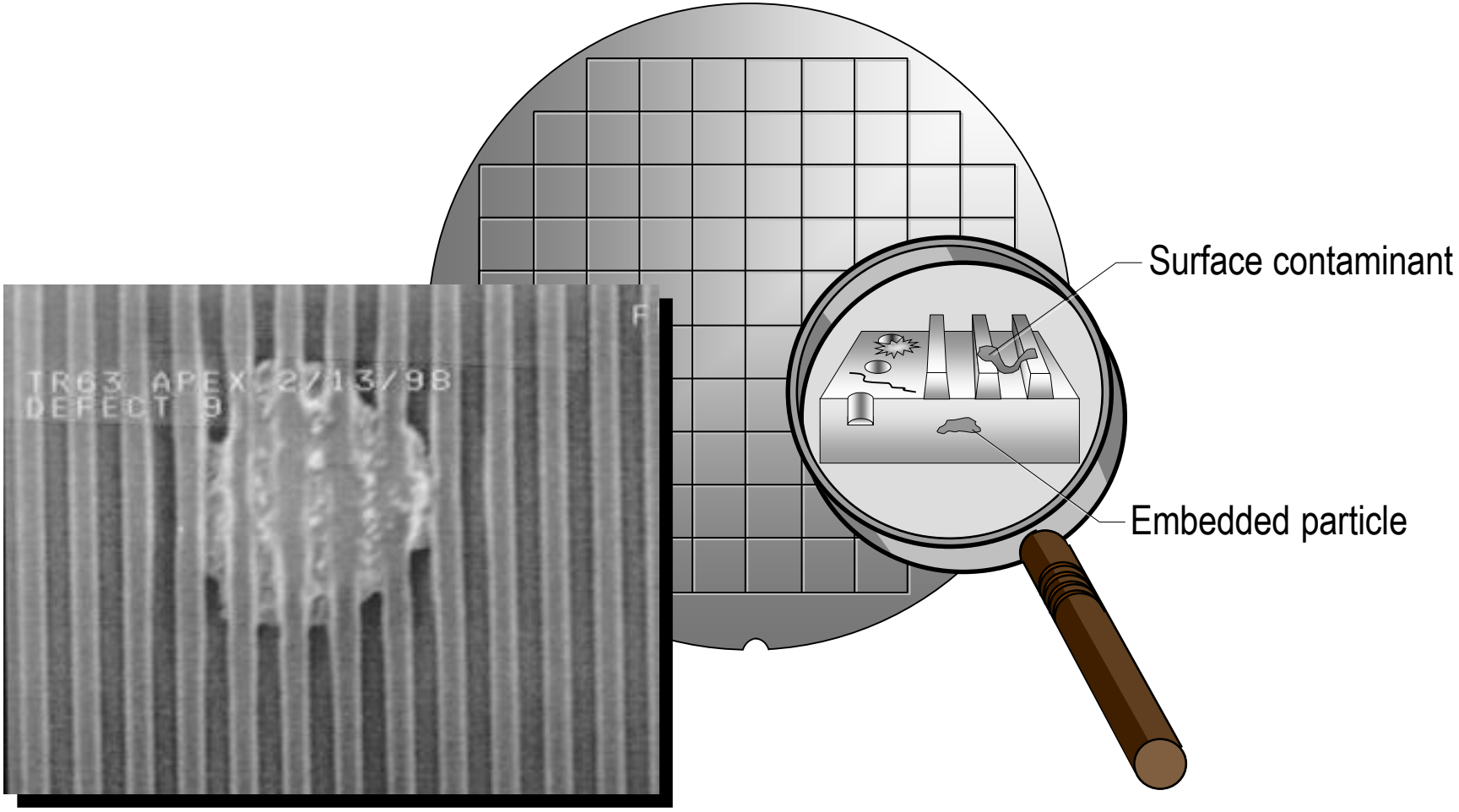


Non-planarized IC product



Planarized IC product

Contamination Control in Wafer Fabs



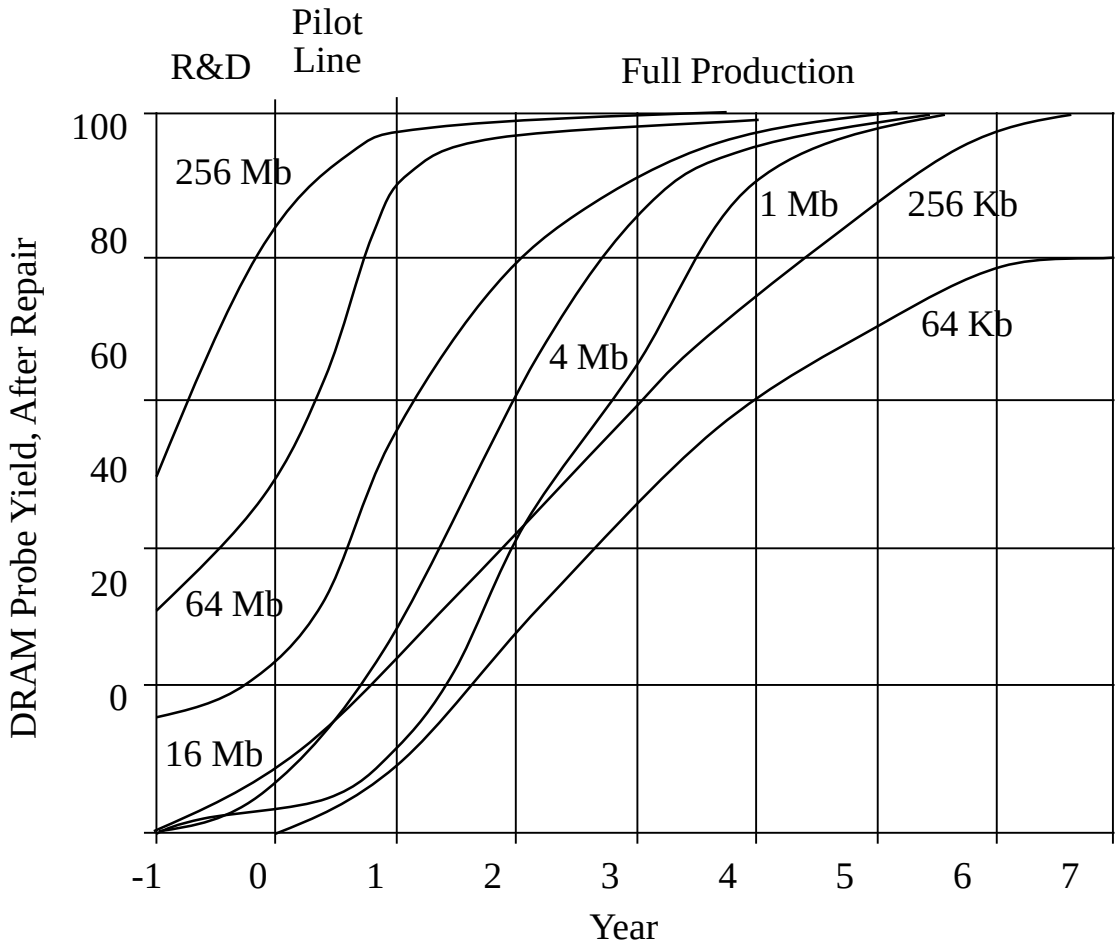
Definition of Airborne Particulate Cleanliness Classes Per Federal Standard 209E

	Particles/ft^3				
Class	**0.1 μm**	**0.2 μm**	**0.3 μm**	**0.5 μm**	**5 μm**
1	3.50 x 10	7.70	3.00	1.00	
10	3.50×10^2	7.50 x 10	3.00 x 10	1.00×10^1	
100		7.50×10^2	3.00×10^2	1.00×10^2	
1,000				1.00×10^3	7.00
10,000				1.00×10^4	7.00 x 10
100,000				1.00×10^5	7.00×10^2

CMOS is not the unique solution!

- Vacuum tube
- Bipolar
- nMOS
- **CMOS**
- GeSi
- Graphene
- … …

Reduced Time to Product Maturity for DRAM Production



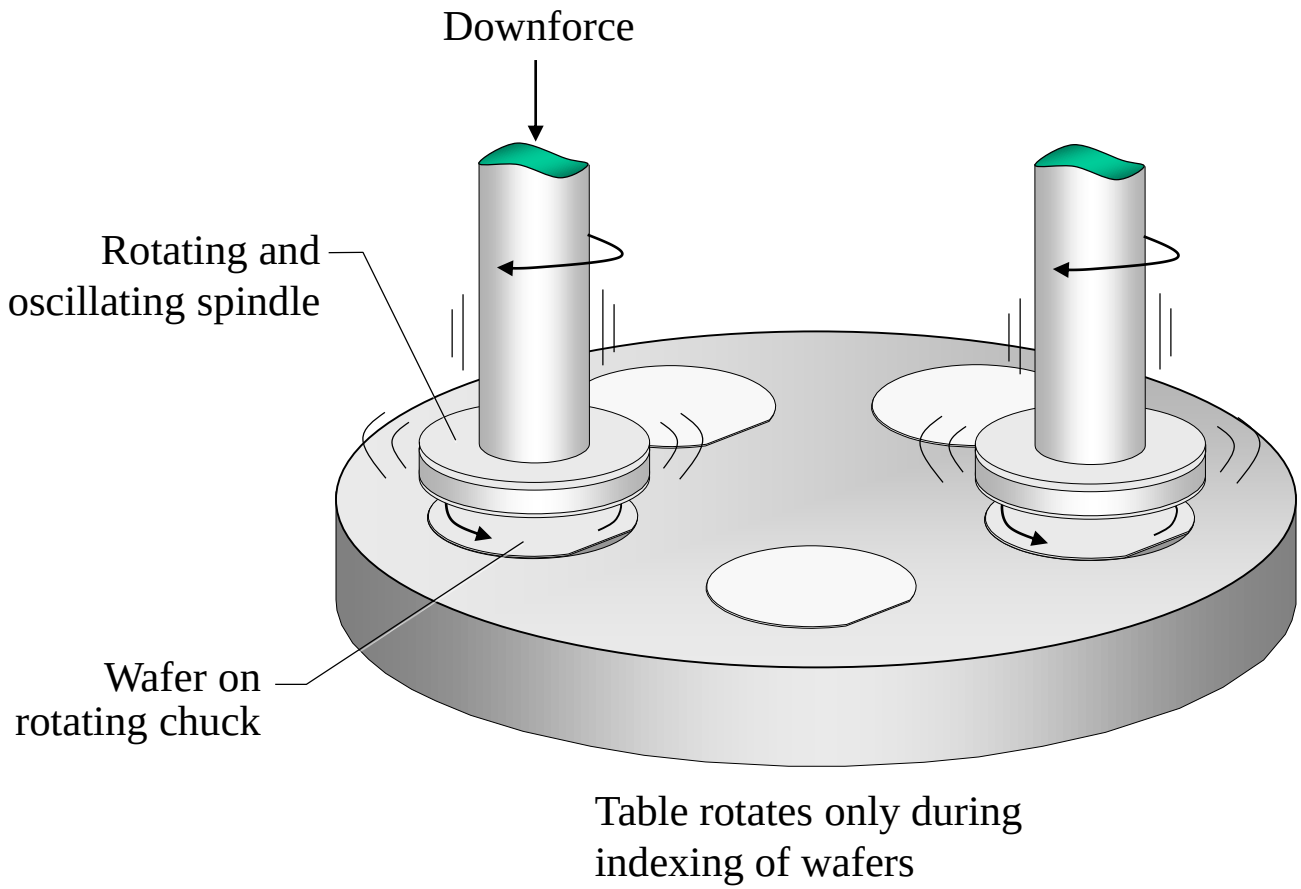
Semiconductor processing

- Semiconductor fabrication
- Layout fundamental
- Semiconductor testing
- ***Semiconductor assembling***

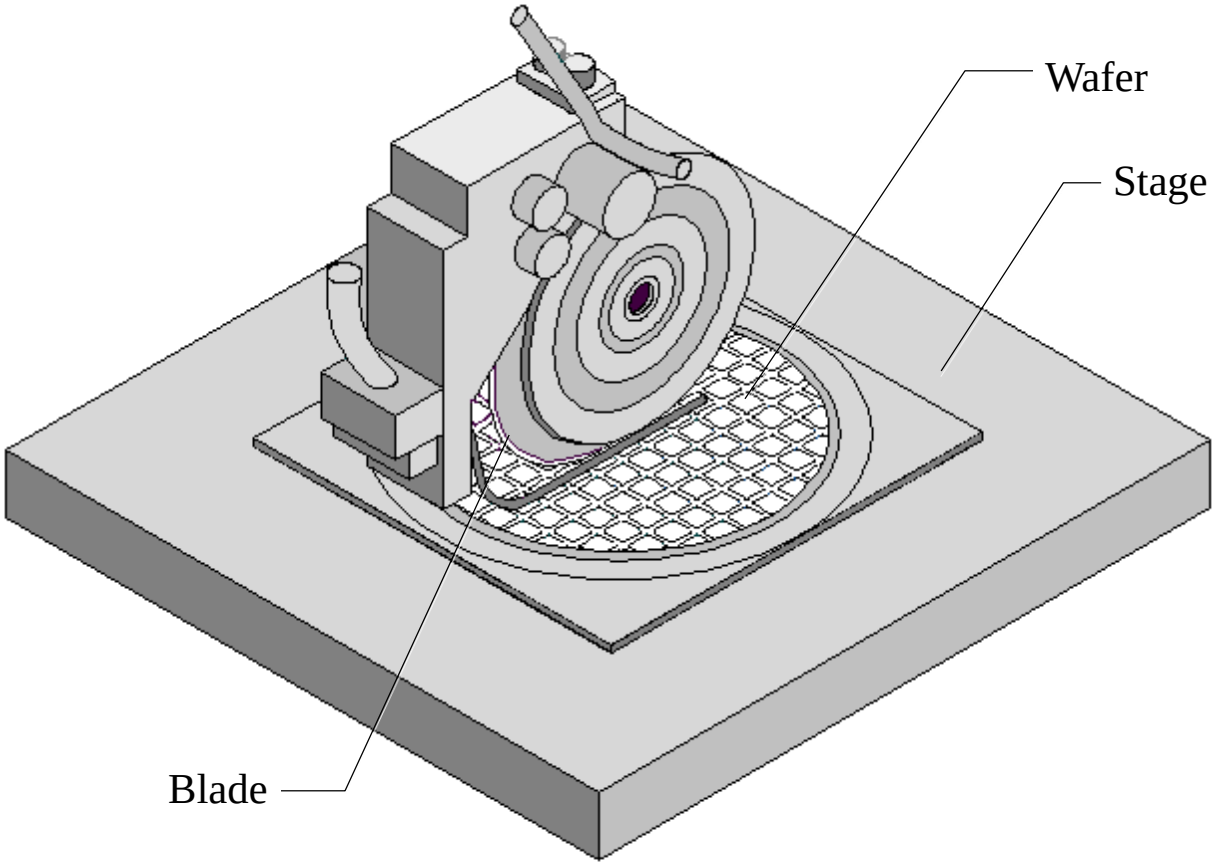
Traditional Assembly

- Wafer preparation (backgrind)
- Die separation
- Die attach
- Wire bonding

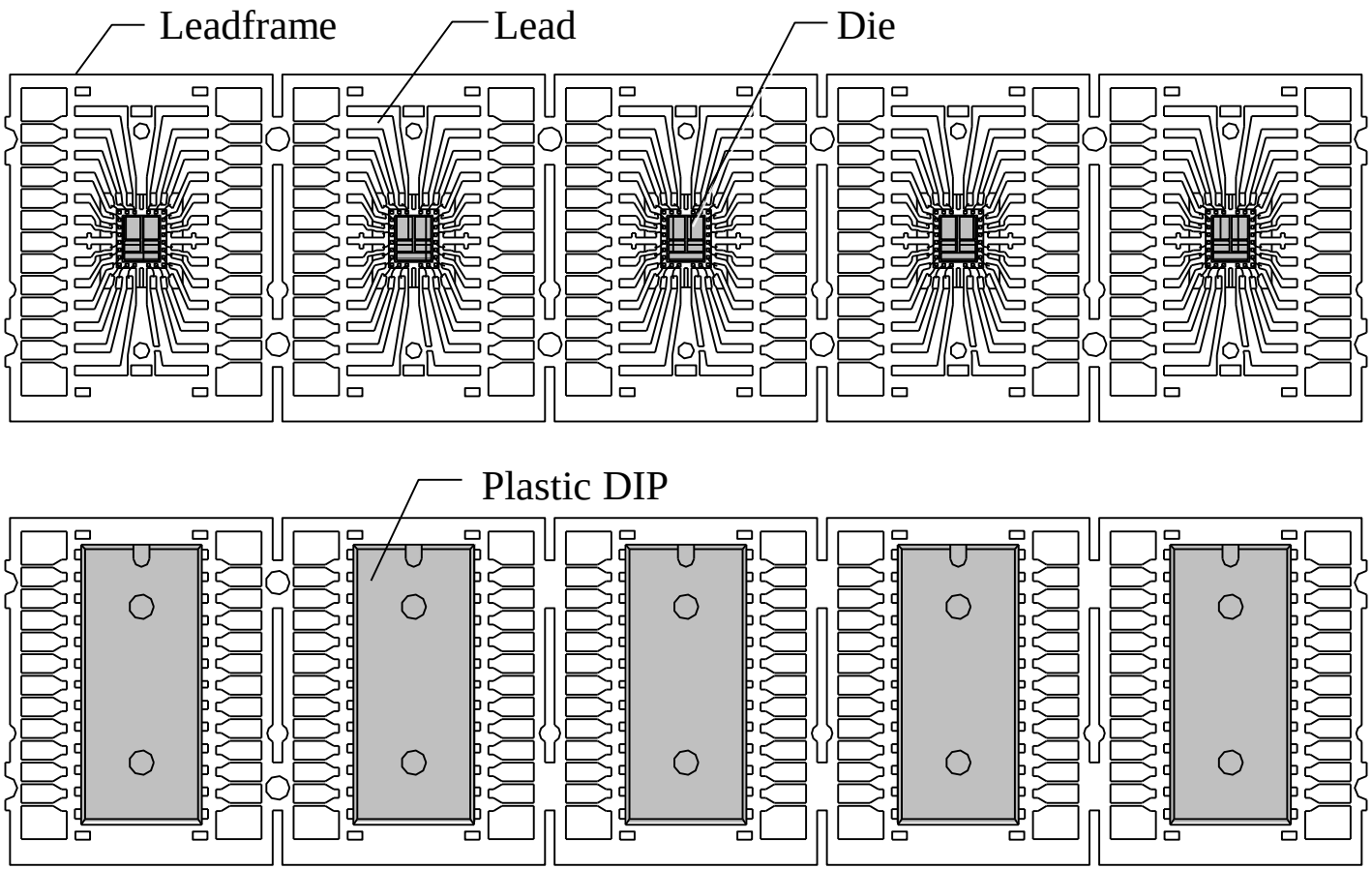
Schematic of the Backgrind Process



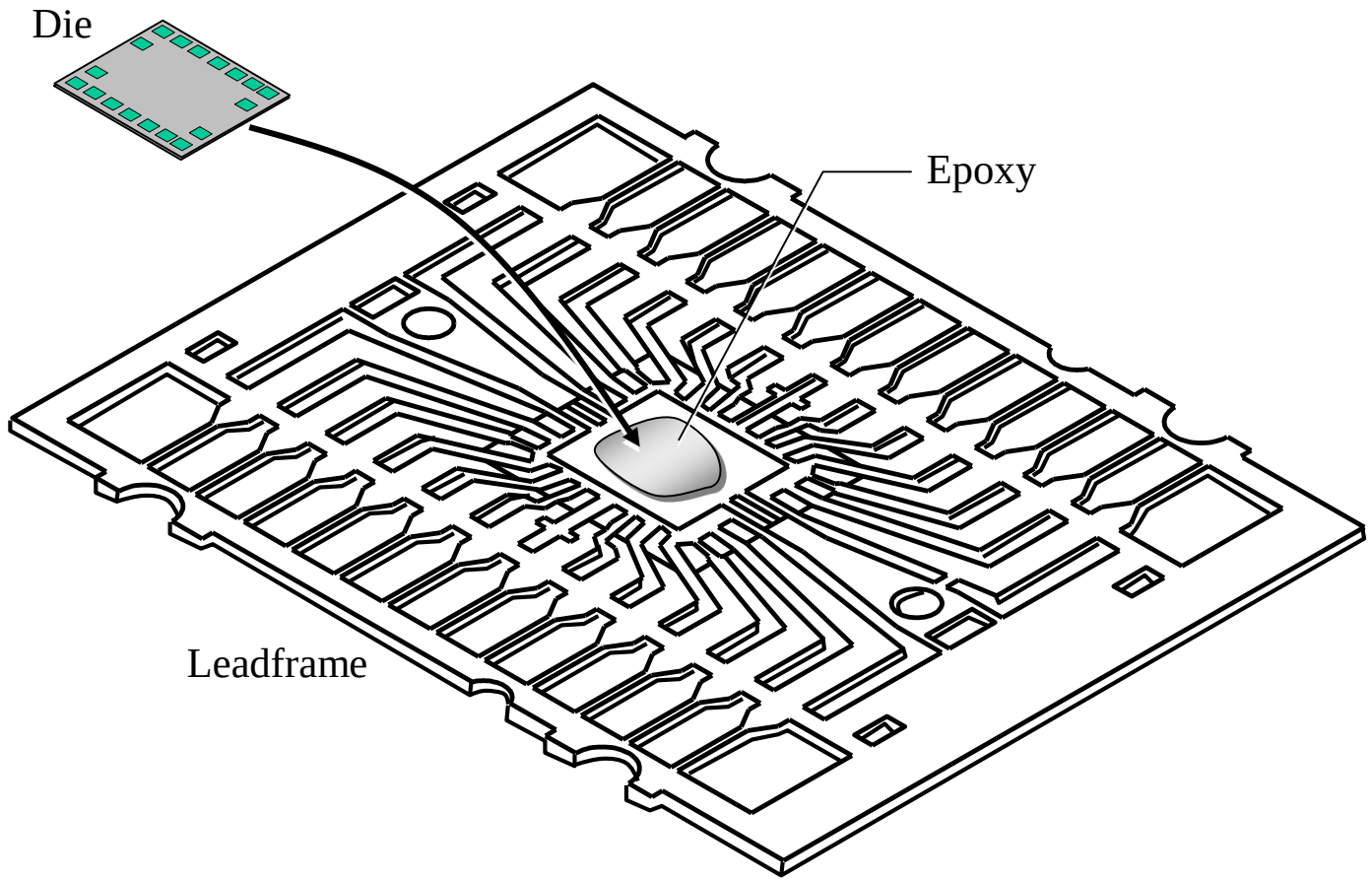
Wafer Saw and Sliced Wafer



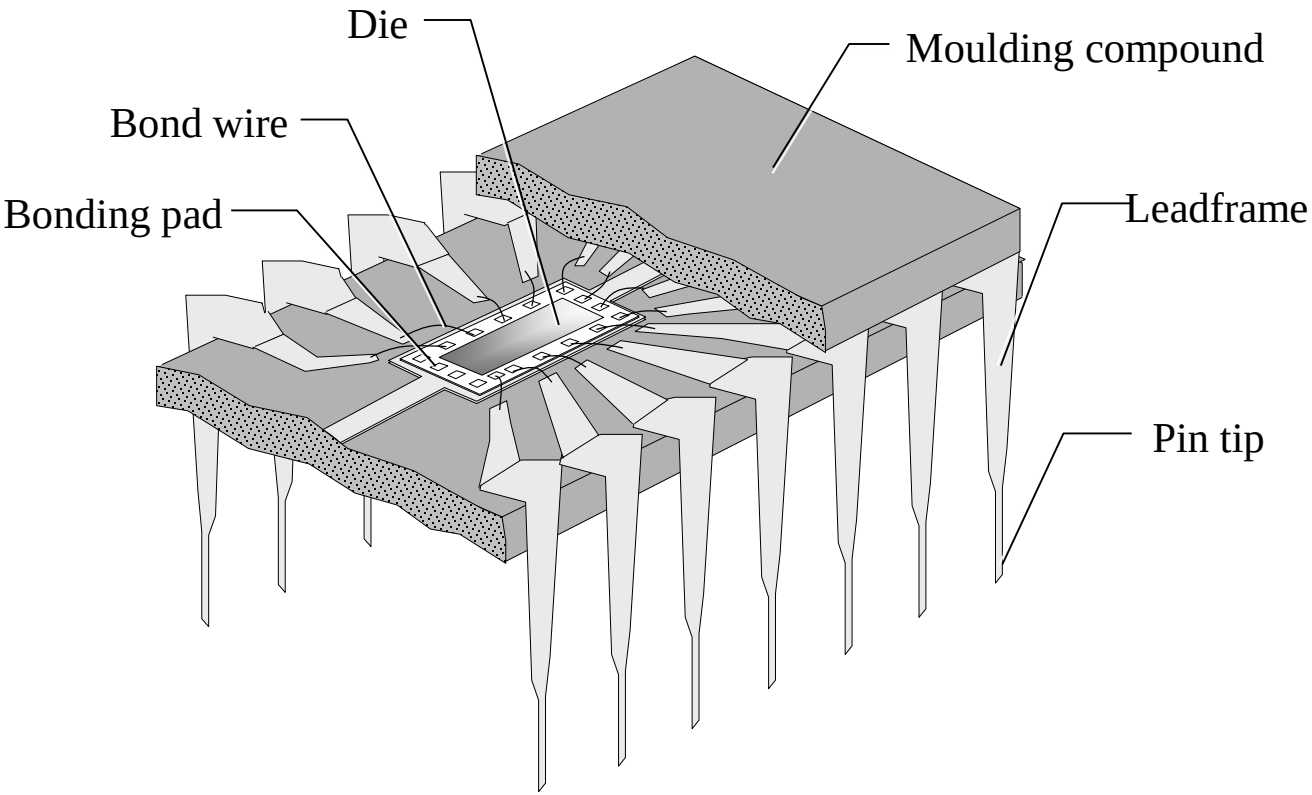
Typical Leadframe for Die Attach



Epoxy Die Attach



Wires Bonded from Chip Bonding Pads to Leadframe



Wirebonding Chip to Leadframe

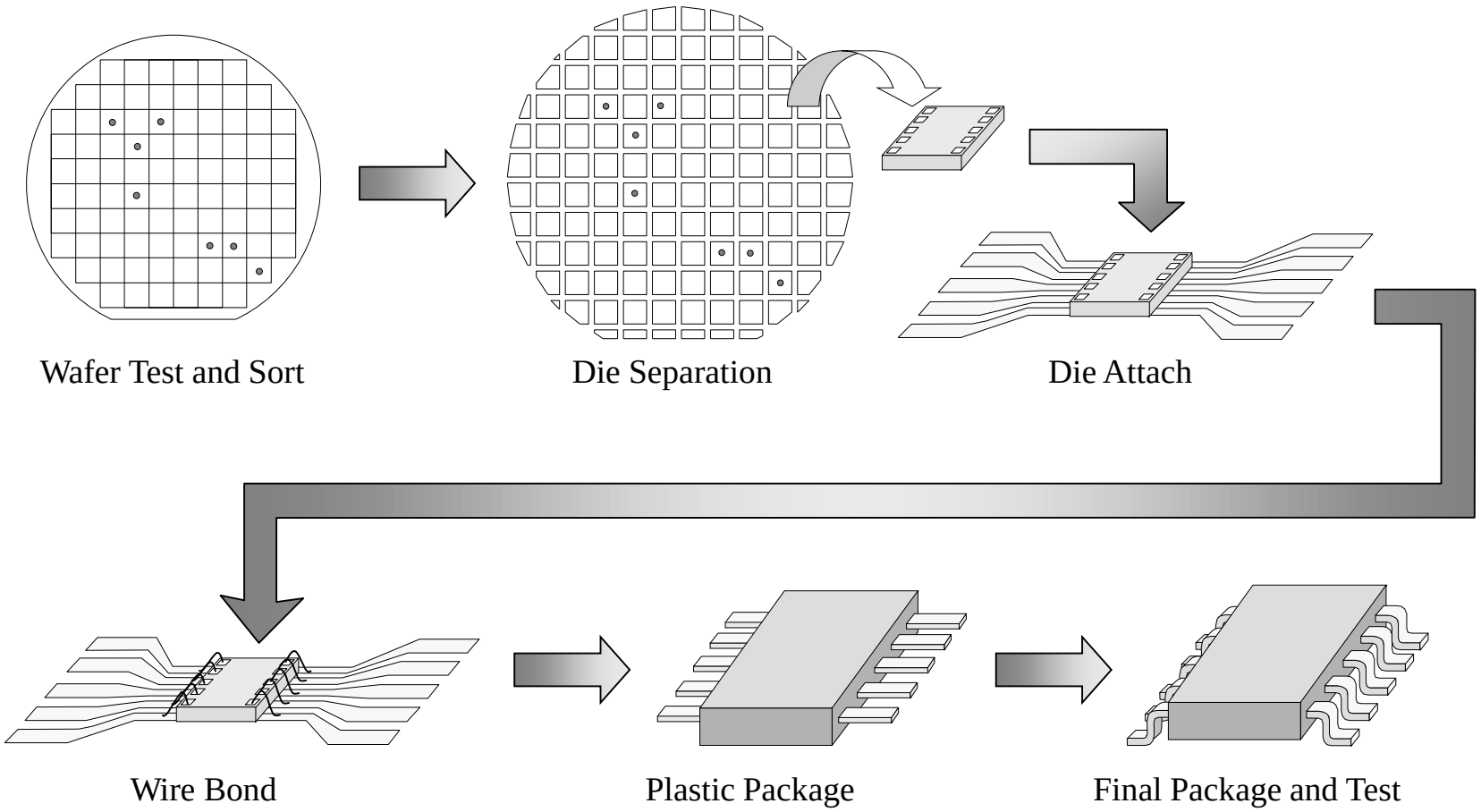
Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

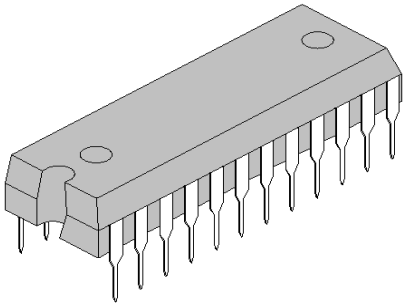
Important Functions of IC Packaging

- Protection from the environment and handling damage.
- Interconnections for signals into and out of the chip.
- Physical support of the chip.
- Heat dissipation.

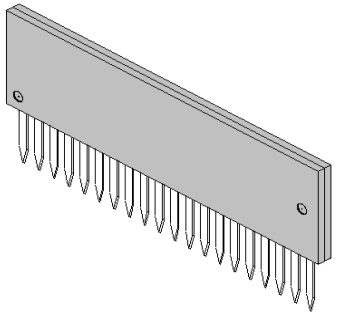
Traditional Assembly and Packaging



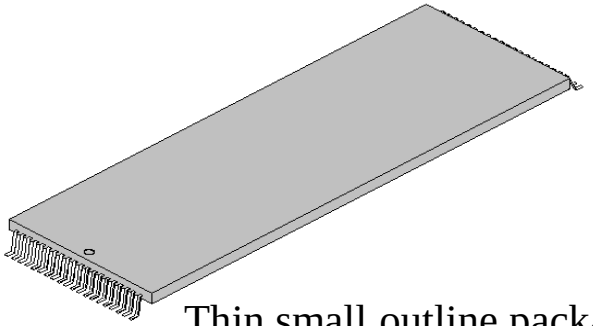
Typical IC Packages



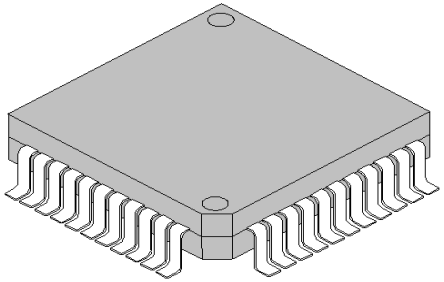
Dual in-line package
(DIP)



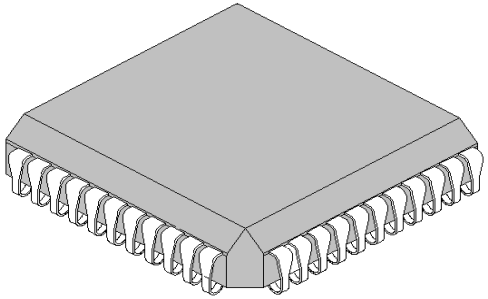
Single in-line package
(SIP)



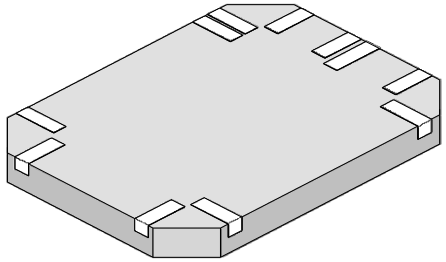
Thin small outline package
(TSOP)



Quad flat pack
(QFP)



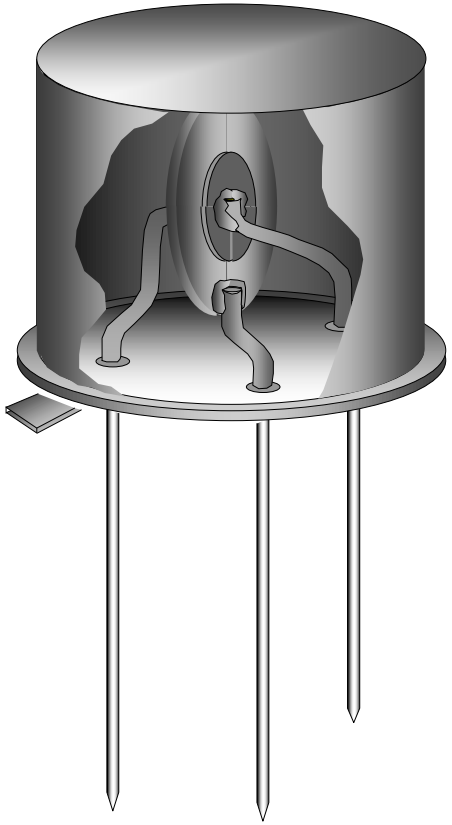
Plastic leaded chip carrier
(PLCC)



Leadless chip carrier
(LCC)

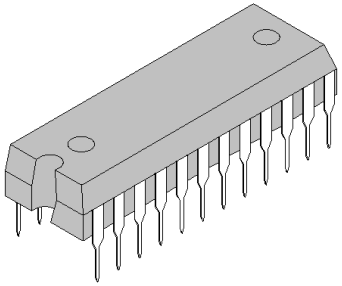
Traditional Packaging

- Plastic Packaging
- Ceramic Packaging
- TO-Style Metal Package(old)

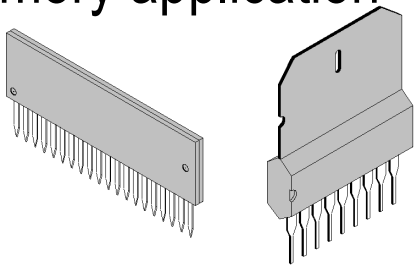


General package mode

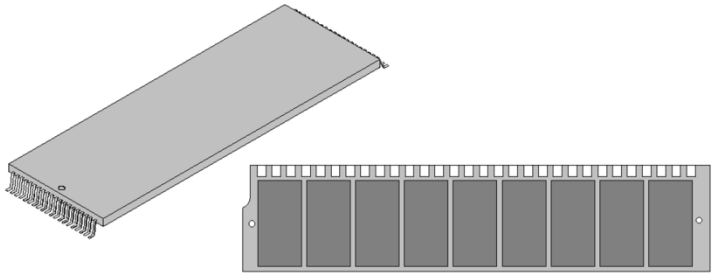
Plastic Dual In-Line Package (DIP) for Pin-In-Hole (PIH)1970s-1980s



Single In-Line Package (SIP), decreasing capacity and cost Memory application

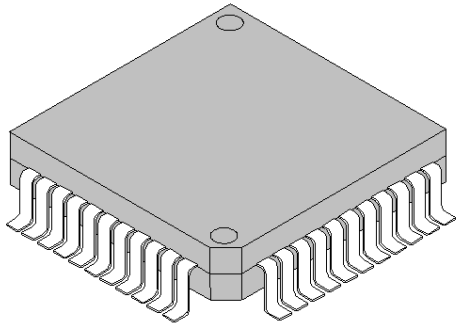


Thin Small Outline Package (TSOP) Memory and smartcard Single In-Line Memory Module (SIMM)

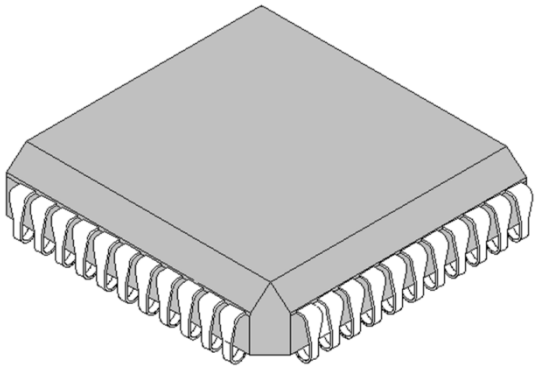


General package mode

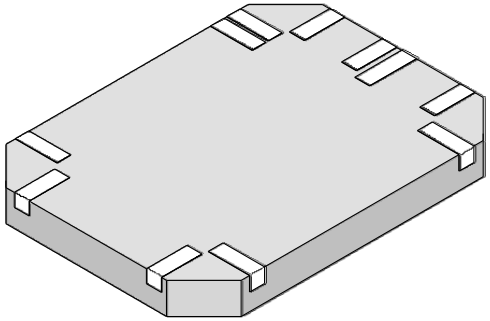
Quad Flatpack (QFP) with Gull Wing Surface Mount Leads



Plastic Leaded Chip Carrier (PLCC) with J-Leads for Surface Mount

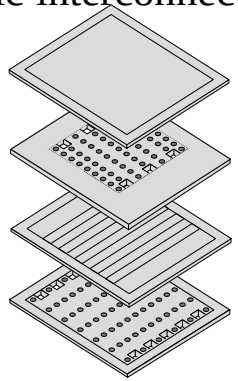


Leadless Chip Carrier (LCC)

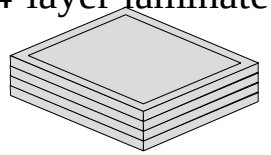


Laminated Refractory Ceramic Process Sequence

Ceramic interconnect layers

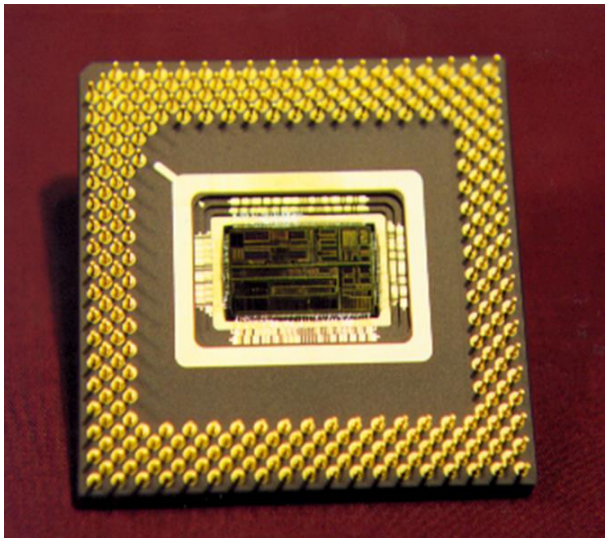


4-layer laminate



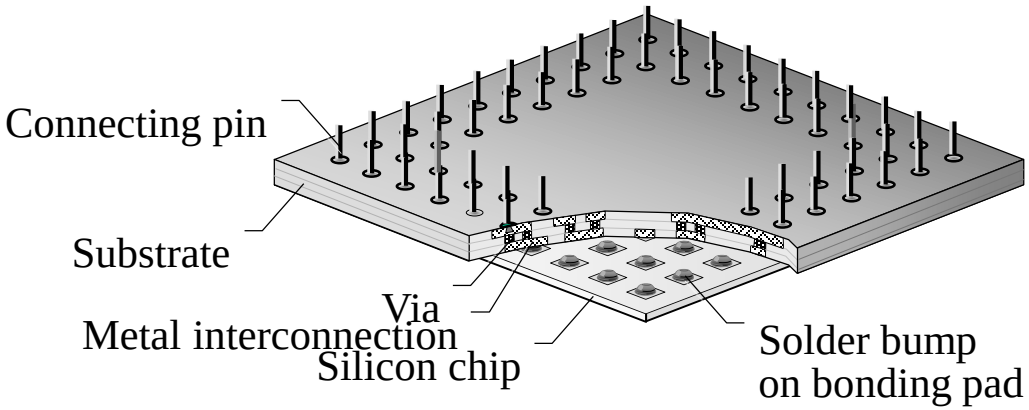
Advanced Packaging

- Flip chip
- Ball grid array (BGA)
- Chip on board (COB)
- Tape automated bonding (TAB)
- Multichip modules (MCM)
- Chip scale packaging (CSP)
- Wafer-level packaging

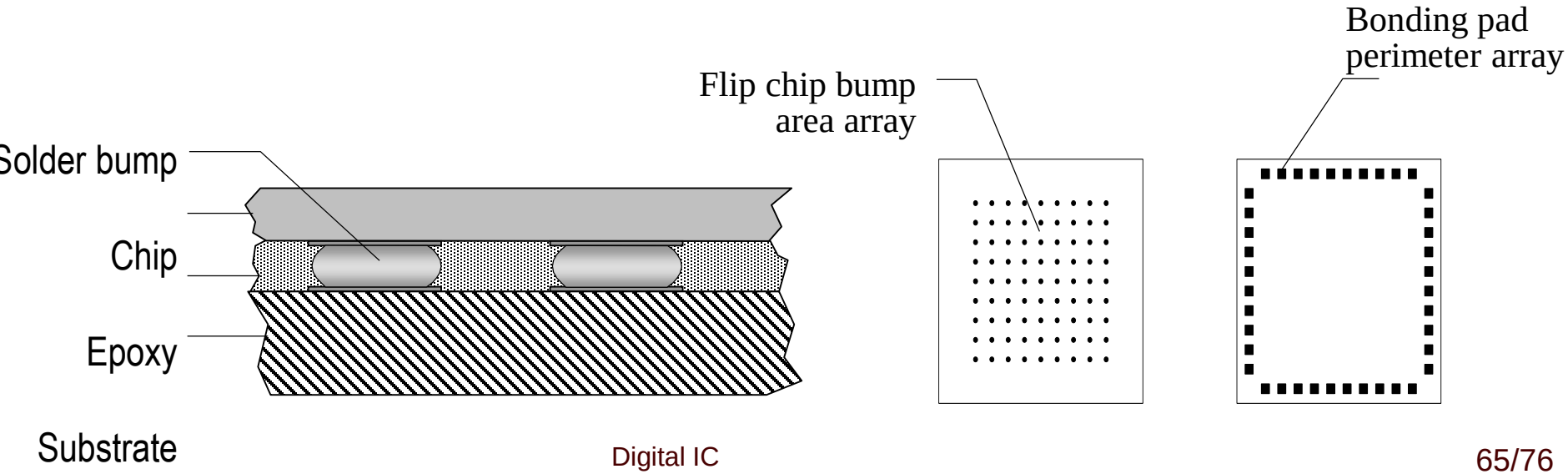


Advanced Packaging

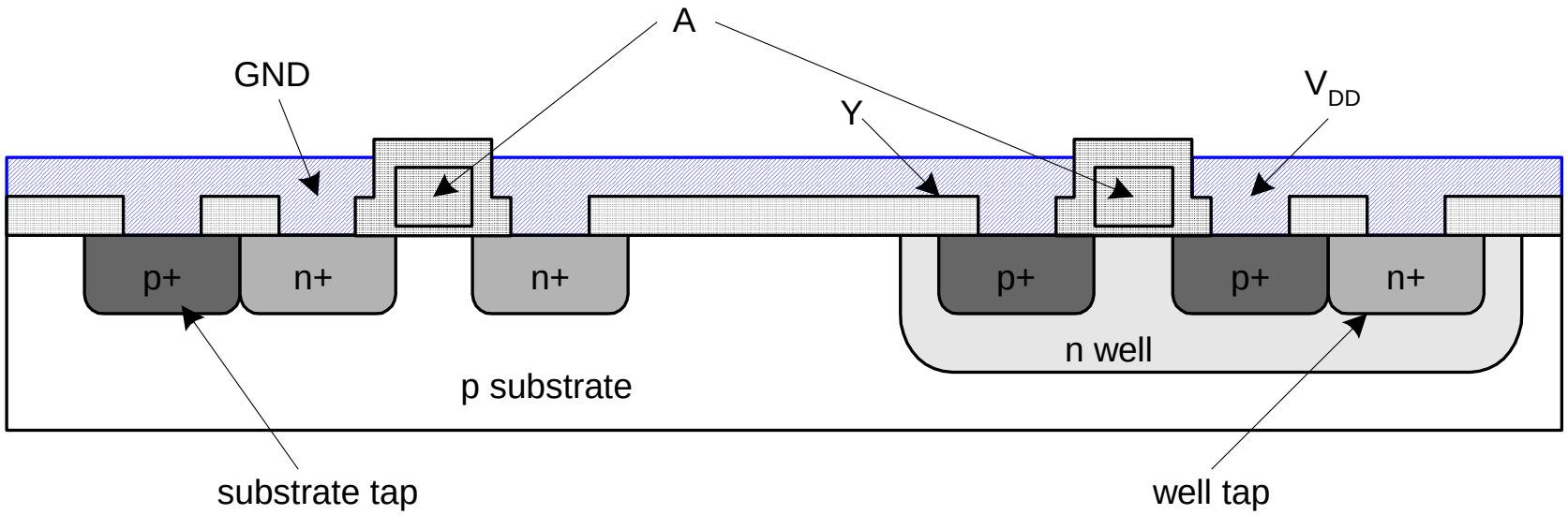
Flip Chip Package



Flip Chip Area Array Solder Bumps Versus Wirebond



quiz



N+，P+ means：

Substrate tap are used for substrate connect.