

# Digital Integrated Circuits

## **Lab 3**

### **Logical Effort**

**Dr. Yanan Sun**

Email: [sunyanan@sjtu.edu.cn](mailto:sunyanan@sjtu.edu.cn)

Office: Rm 414, Building of Microelectronics

# ***Outline***

- ❑ Lab Contents
- ❑ Report Requirements

# ***Outline***

- Lab Contents
- Report Requirements

# Device Models for Logical Effort Optimizaiton

□ Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of 10nm multi-gate (MG) FinFETs

- PTM link:  
<http://ptm.asu.edu/>
- Use the high-performance (HP) models
- For both n-channel and p-channel devices

**Predictive Technology Model**

**LATEST MODELS**

Typical SPICE model files for each future generation are available here.

**Attention:** By using a **PTM** file, you agree to acknowledge both the URL

**New!**  
**June 01, 2012:**  
PTM releases a new set of models for multi-gate transistors (**PTM-MG**), for bc  
Acknowledgement: PTM-MG is developed in collaboration with ASU and IBM.

Please start from [models](#) and [param.inc](#).

- 7nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 10nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 14nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 16nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 20nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)

The entire package is also available here: [PTM-MG](#)

November 15, 2008:  
PTM releases a new set of models for low-power applications (PTM LP), incor

- 16nm PTM LP model: [V2.1](#)
- 22nm PTM LP model: [V2.1](#)
- 32nm PTM LP model: [V2.1](#)
- 45nm PTM LP model: [V2.1](#)

September 30, 2008:  
PTM releases a new set of models for high-performance applications (PTM HP)

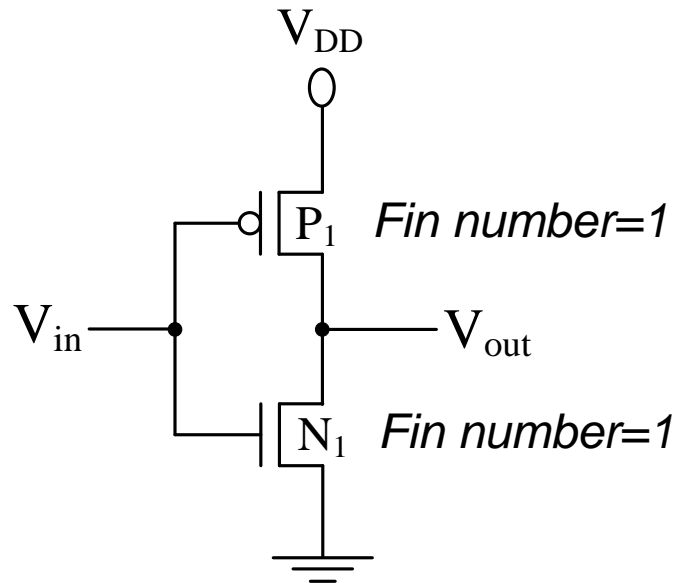
- 16nm PTM HP model: [V2.1](#)
- 22nm PTM HP model: [V2.1](#)
- 32nm PTM HP model: [V2.1](#)
- 45nm PTM HP model: [V2.1](#)

**ASU**

# ***Simulation Settings***

- ❑  $L_g = 14 \text{ nm}$  for FinFETs
- ❑ Supply voltage is  $0.65\text{V}$  for FinFETs
- ❑ Simulation temperature
  - $T = 25^\circ\text{C}$

## Minimum sized INV for FinFET



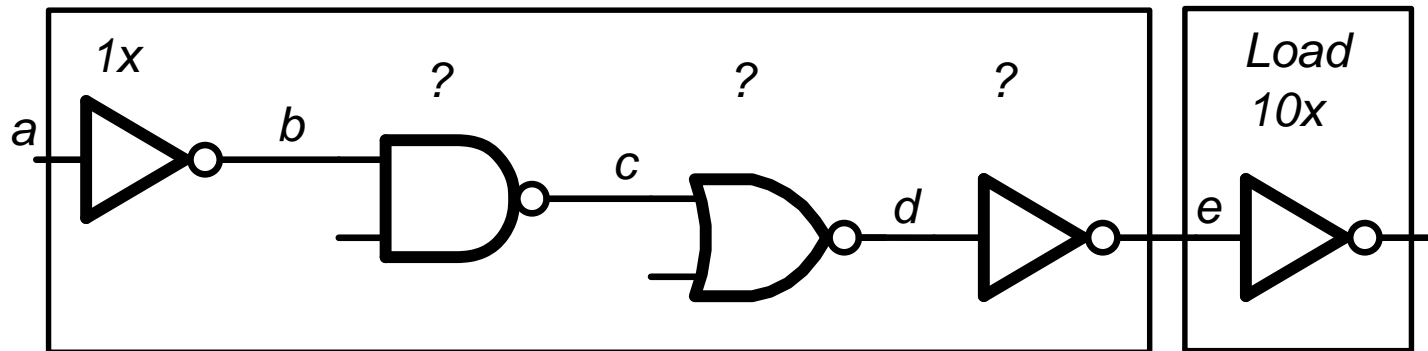
minimum-sized  
un-skewed CMOS inverter

| Minimum Sized Inv   | PMOS | NMOS |
|---|------|------|
| Fin number  | 1    | 1    |
| L   | 14n  | 14n  |
| Design the fin number to ensure balanced driving current in pull-up and pull-down network |      |      |

# Task1: Use Logical Effort to Size Gates

- Size each transistor in the circuit below properly to optimize the speed for FinFET, and construct the circuit with HSPICE

*Size the logic gates to minimize the propagation delay (a to e)*

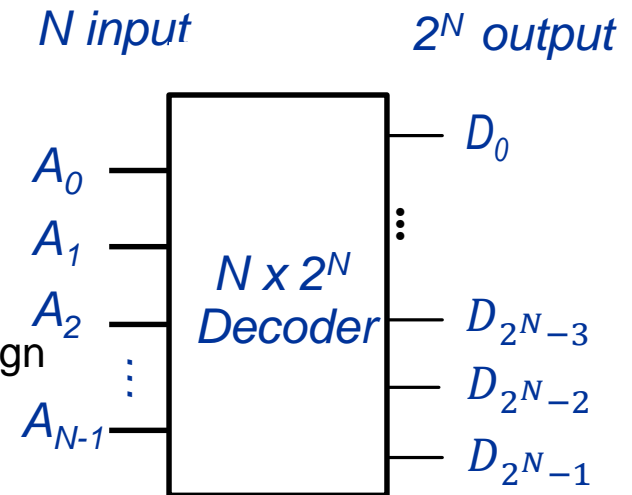


| Vpulse      | Value |
|-------------|-------|
| V1          | 0V    |
| V2          | 0.65v |
| Delay Time  | 1ns   |
| Raise Time  | 50ps  |
| Fall Time   | 50ps  |
| Pulse Width | 1ns   |
| Period      | 2ns   |

## Task2: Use Logical Effort to Optimize 4x16 Decoder

### □ Backgroud of decoder

- Logic function: convert N-bit coded input to  $2^N$  unique outputs
- Can be used as address decoder in memory
  - Address line (input) has large fanout
  - Decoders typically have high electrical effort and branching effort
  - Decoder may have many stages, so the fastest design is the one that minimizes the logical effort

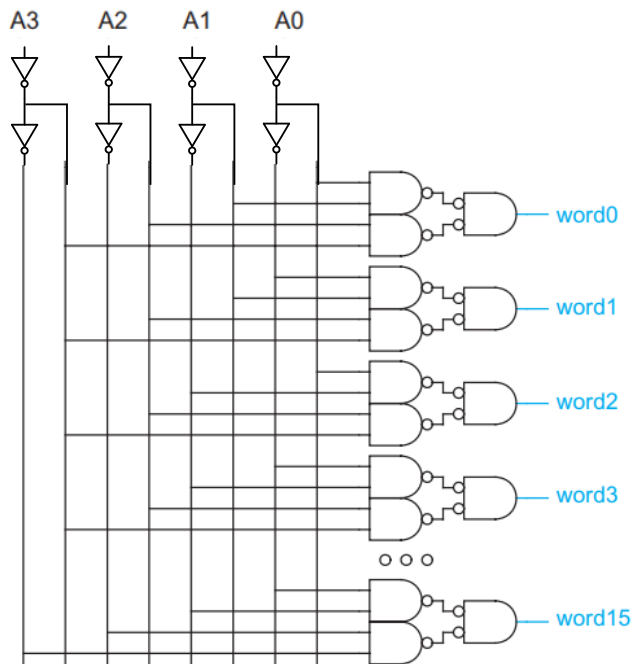


$$\begin{aligned} D_0 &= \overline{A_{N-1}} \dots \overline{A_3} \overline{A_2} \overline{A_1} \overline{A_0} \\ D_1 &= \overline{A_{N-1}} \dots \overline{A_3} \overline{A_2} \overline{A_1} A_0 \\ &\dots \\ D_{2^N-1} &= A_{N-1} \dots A_3 A_2 A_1 A_0 \end{aligned}$$

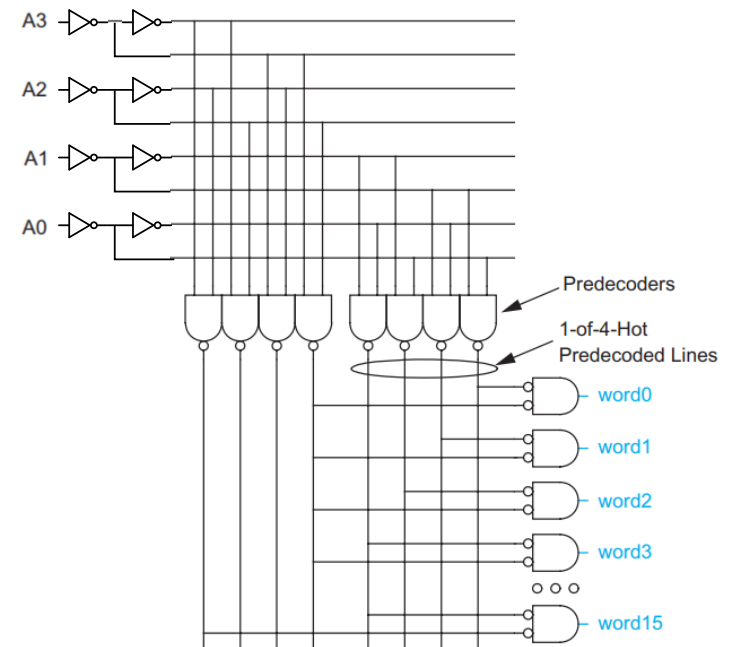
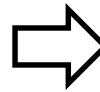


## Task2: Use Logical Effort to Optimize 4x16 Decoder

- An example of 4x16 decoder design:



Factoring the  
common  
NANDs out



4-input AND function is built from a pair of 2-input NANDs followed by a 2-input NOR

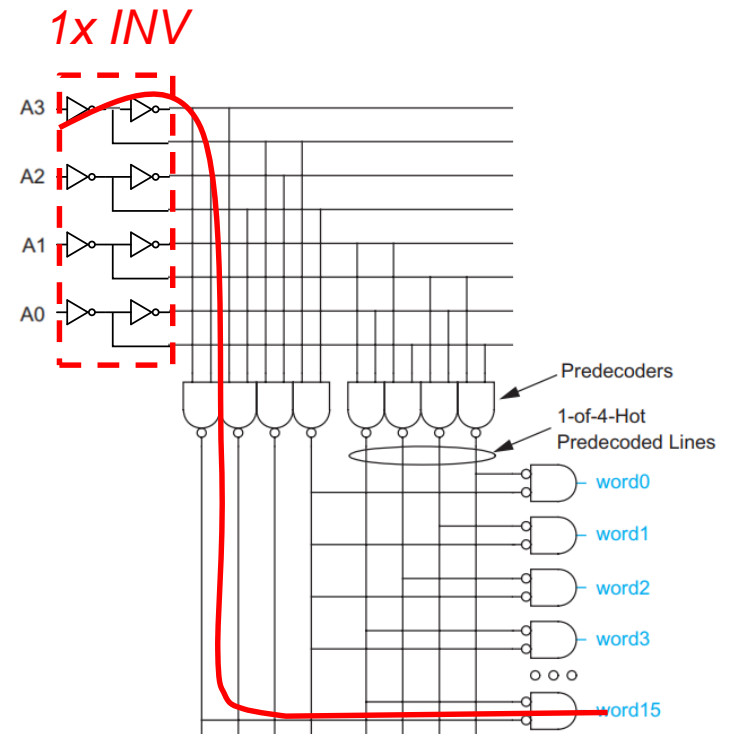
But, many NAND gates share the same inputs and are redundant

Predecoding technique to reduce the area

## Task2: Use Logical Effort to Optimize 4x16 Decoder

- ❑ For a 4x16 decoder, optimize the critical path to minimize the propagation delay of decoder

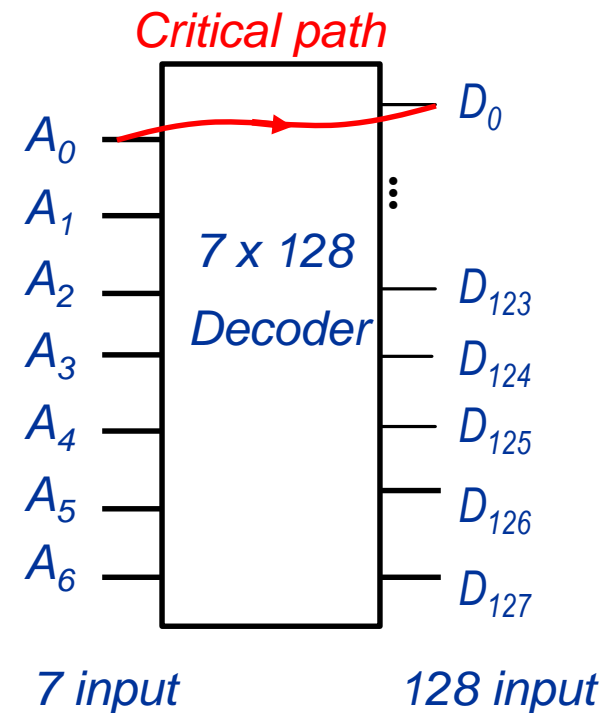
- Use the logical effort method
- Assume that the input inverter/buffer is minimum sized
- Assume that each output of decoder has a load of 256X minimum sized Finfet inverter
- You can insert buffer at the output if necessary



## Task3 (Optional): Use Logical Effort to Optimize 7x128 Decoder

- ❑ For a 7x128 decoder, first think about the scheme design. Then optimize the critical path to minimize the propagation delay of decoder

- Use the logical effort method
- Assume that the input inverter/buffer is minimum sized
- Assume that each output of decoder has a load of 512X minimum sized Finfet inverter
- You can insert buffer at the output if necessary



# ***Outline***

- Lab Contents
- Report Requirements

# ***Report Requirement***

- ❑ Write your lab report like writing a technical document (readable, comprehensive analysis, no typo...)
- ❑ You may include
  - Lab procedures (e.g., screenshots of the critical steps)
  - Lab results (e.g., schematic view, symbol of inverter, screenshots of the simulation waveforms)
  - Observations and conclusions

# Submission

- ❑ You need to submit your report and code
  - Name of report (in PDF format):  
lab3\_report\_[Name]\_[Student No.].pdf
  - Name of code (compressing the files):  
lab3\_code\_\_[Name]\_[Student No.].zip
  
- ❑ Please upload your report to Canvas course website
  
- ❑ Submission of Lab 3 report will be due on 19<sup>th</sup> December

# Q & A

- If you have any technical problem, you can directly contact me

*E-mail: [yungsk@sjtu.edu.cn](mailto:yungsk@sjtu.edu.cn)*

*Lab: Rm 208, Building of Microelectronics*