数字集成电路课程设计

课程简介

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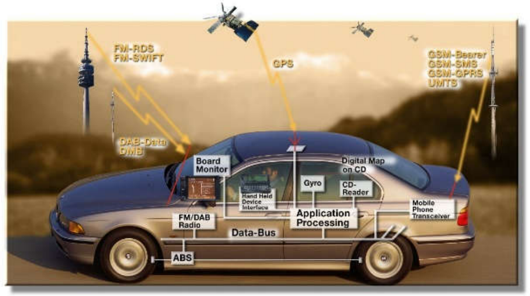
IC - National Strategy

- Processors
  - CPU, DSP, Controllers
- Memory chips
  - RAM, DRAM, Flash
- Analog
  - RF, AD/DA, audio/video processing
- Programmable
  - PLA, FPGA、GPU
- Embedded systems
  - Used in cars, factories
  - Network cards
- System-on-chip (SoC)
  - Mobile computing
  - Beyond 5G
  - Wearable computing
  - AI



IC Industry Segmentation in China

IC design: the biggest product value and fastest growth rate

IC Design in China

IC Design Companies in China

2010-2019年芯片设计企业数量增长情况

主要城市：北京、上海、深圳
重要城市:无锡、杭州、西安、成都、南京、苏州、合肥

IC 2025 Prediction in China

王阳元：2035年5037亿美元（10%增长率），占比56%

Top Semiconductor Companies

$ 470B + 2018 WW semiconductor revenue, Top 15 accounts for 80% of all, no Chinese player

Largest IC Product Categories, 2018F

Rank	Market	$B
1	DRAM	$101,620
2	NAND Flash	$62,604
3	Std PC, Server MPU	$50,782
4	Computer and Periph- Spcl Purp Logic	$27,619
5	Wireless Comm Spcl Purp Logic	$25,998
Rank	**Shipments**	**Units, M**
1	Power Management Analog	71,192
2	Wireless Comm-App Specific Analog	23,376
3	General Purpose Logic	21,675
4	Industrial-App Specific Analog	18,924
5	Automotive-App Specific Analog	15,969

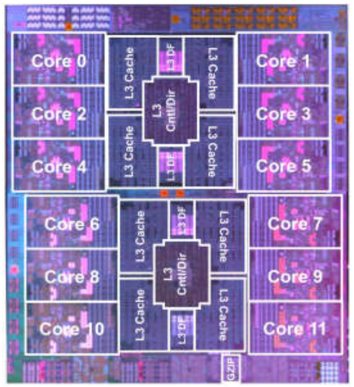
Source: IC Insights

2018F Top 15 Semiconductor Sales Leaders ($M, Including Foundries)

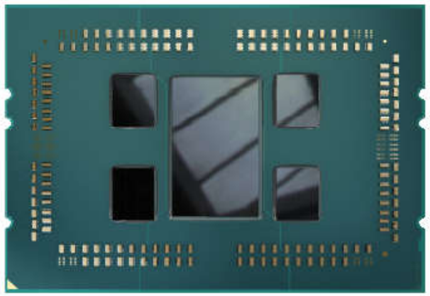
2018F Rank	2017 Rank	Company	Headquarters	2017 Total Semi Sales ($M)	2018 Total Semi Sales ($M)	2018F/2017 % Change
1	1	Samsung	South Korea	65,882	83,258	26%
2	2	Intel	U.S.	61,720	70,154	14%
3	4	SK Hynix	South Korea	26,722	37,731	41%
4	3	TSMC (1)	Taiwan	32,163	34,209	6%
5	5	Micron	U.S.	23,920	31,806	33%
6	6	Broadcom Ltd. (2)	U.S.	17,795	18,455	4%
7	7	Qualcomm (2)	U.S.	17,029	16,481	-3%
8	9	Toshiba/Toshiba Memory	Japan	13,333	15,407	16%
9	8	TI	U.S.	13,910	14,962	8%
10	10	Nvidia (2)	U.S.	9,402	12,896	37%
11	12	ST	Europe	8,313	9,639	16%
12	15	WD/SanDisk	U.S.	7,840	9,480	21%
13	11	NXP	Europe	9,256	9,394	1%
14	13	Infineon	Europe	8,126	9,246	14%
15	14	Sony	Japan	7,891	8,042	2%
-	-	**Top-15 Total**		**323,302**	**381,160**	**18%**

(1) Foundry (2) Fabless Source: Company reports, IC Insights' Strategic Reviews database

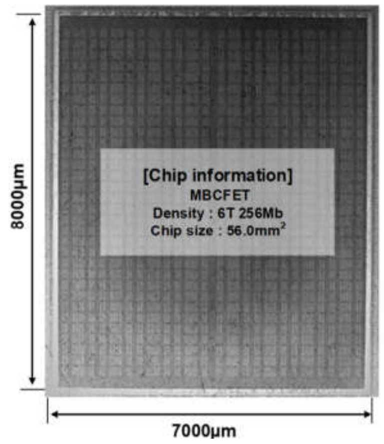
ISSCC- IC Design Olympic Games



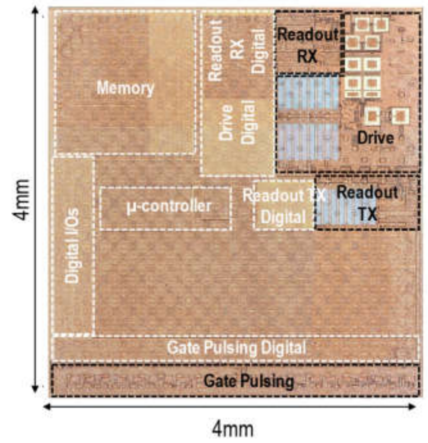
12 core, 5GHz
IBM, 14nm SOI



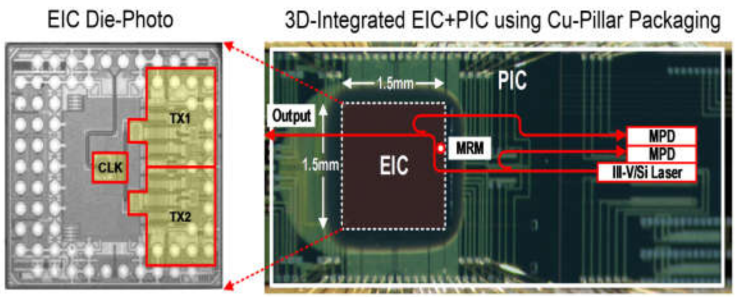
Zen 2, CPU
AMD, 7nm



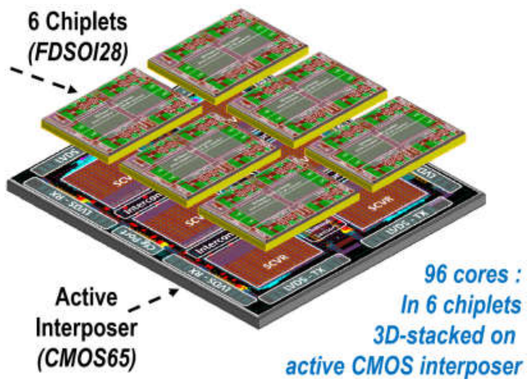
GAA SRAM
Samsung, 3nm



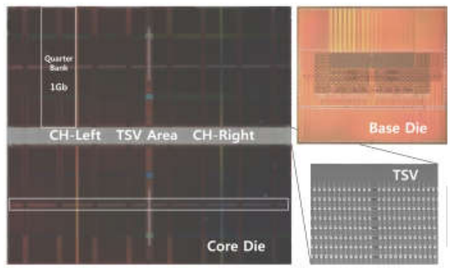
Qubit Chip
Intel, 22nm FinFET



112G PAM4 EPIC
Intel, 28nm



96 3D Core
List, ST



128G HBM DRAM
SK hynix

Current Situation

- ISSCC paper
  - Intel: 10 papers per year on average
  - MIT: 3~4 papers per year
  - Mainland: less than 1 paper per year on average
  - Mainland: no mainstream large scale IC with advanced process

- JSSC paper
  - Intel: 15 papers one year (peak)
  - MIT: 12 papers one year (peak)
  - Mainland: 13 papers in 2019
  - Mainland: Less than 1 paper per year on average

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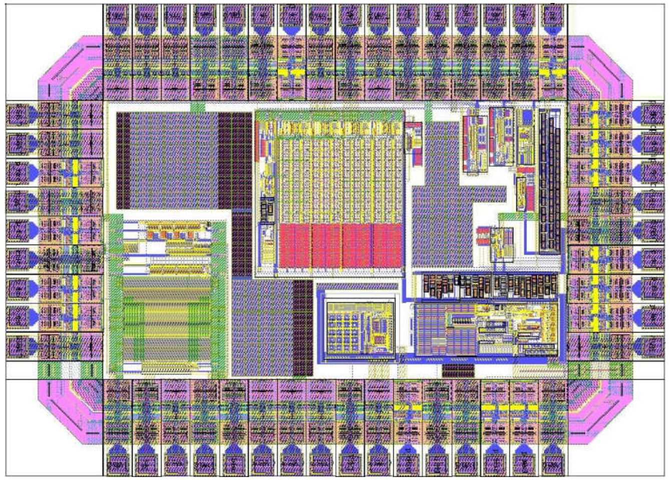
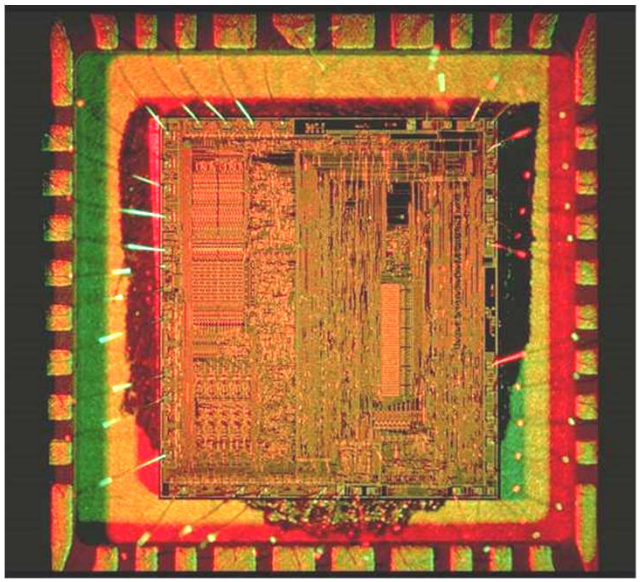
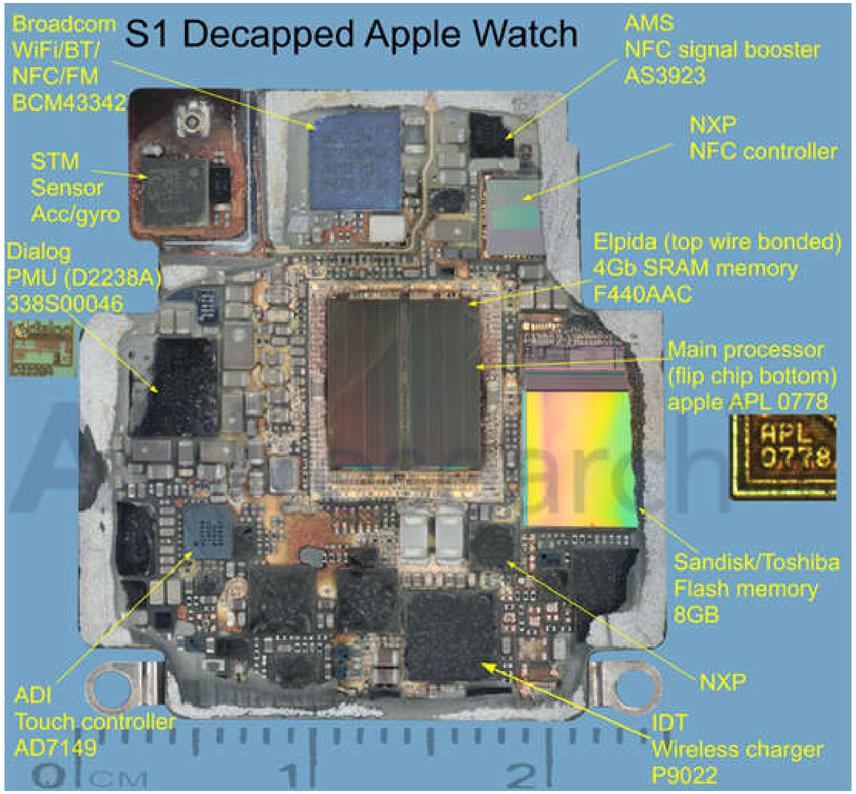
What are Inside a Chip?

- A chip may include:
  - Hundreds of millions of transistors
  - ~MB embedded SRAM
  - DSP, IP cores
  - PLL, ADC, DAC…
  - Several networks
  - … …
- Design Metrics:
  - Speed
  - Power
  - Area
  - Manufacturing yield
  - DFT
  - Reliability





Examples of Current iwatch



What the Course is

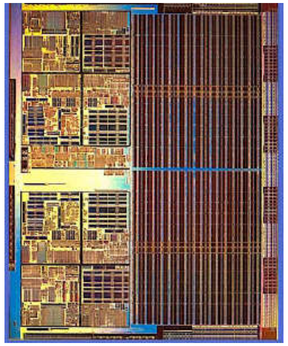
Design a digital IC chip with your team members

Specifications

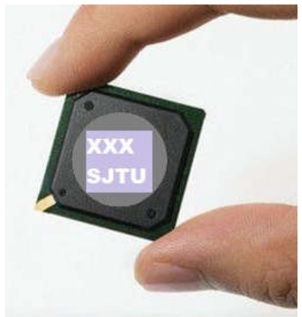
- 9 bit ≤ resolution ≤ 10 bit
- 18 MHz ≤ conversion rate ≤ 30 MHz
- 18 MHz ≤ clock frequency ≤ 30 MHz
- Integral nonlinearity ≥ 1 LSB
- . . . .

Our Course

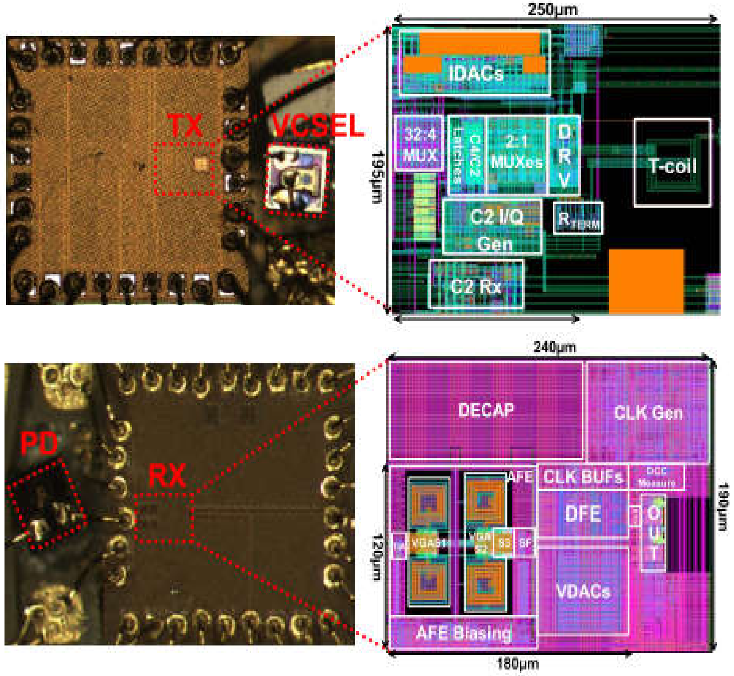
IC Chip Layout



A Real Chip



Brief of the Course



Target of the course:

- Learn how to design a real chip

Skills from the course:

- Design methodology and flow
- EDA tools
- Architecture design
- Design trade-off
- Verilog coding
- Analysis and optimization
- Sign-off
- Package and Measurement

Specifications of the Design

Task: （Optional）

- Energy-efficient SHA 256/SM3 processor ***
- Multi/Many-core Network-on-Chip ****
- High performance ME processor for H.266 ****

Details:

完成电路的结构设计、Verilog HDL代码设计、逻辑仿真、性能分析、逻辑综合、时序分析与验证和物理设计，芯片流片与测试（可选），进行结果分析比较。

Teaching Specialty

Teaching style:

- Discussion-driven teaching
- Teamwork for a project
- Be a architecture designer

Your contributions:

- Propose your own VLSI architecture
- Describe your own Verilog code
- Tradeoff of the design as you wish

Our requirements:

- Meet our specifications
- Do your best
- Do different work from other teams

Grading Policy

- 电路结构设计，20%
  - 有效性、合理性、新颖性
- RTL代码设计与验证，20%
  - 规范性、有效性、完整性
- 逻辑综合与物理设计，30%
  - 完整性、合理性、可信度
- 设计报告+ppt+答辩，20%
  - 逻辑性、可读性、规范性
- 团队精神+出勤情况，10%

Information of Instructors and TA

- 何卫锋，副研究员

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  -mail: hewf@sjtu.edu.cn

- 办公室

  -闵行校区微电子大楼410房间

- 实验室

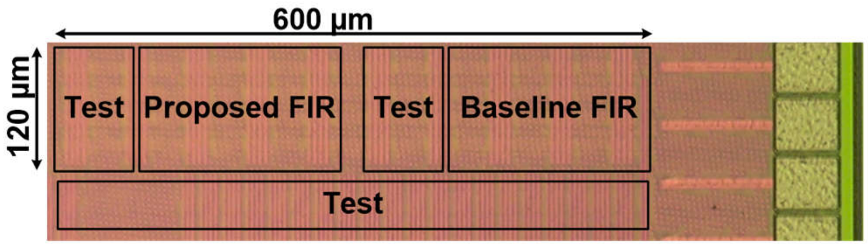
  -闵行校区微电子大楼202房间

- 助教

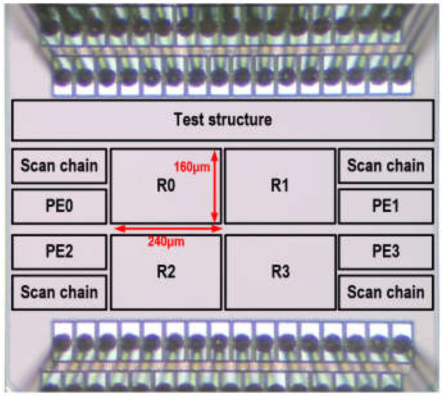
  -裴秉玺（13380396674）、林初雄（18317010875）

  -李婕妤（18916022612）、邵琳（15618062793）

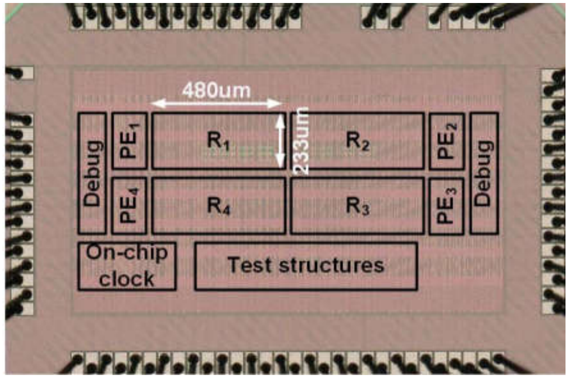
Chip Design of My students



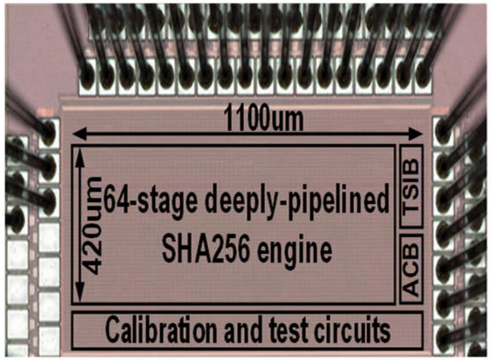
65nm FIR， W. Jin, JSSC’17



45nm NoC，C. Lin, CICC’22



65nm NoC，C. Lin, ISSCC’20，JSSC’21



28nm SHA256， J. Li,CICC’22

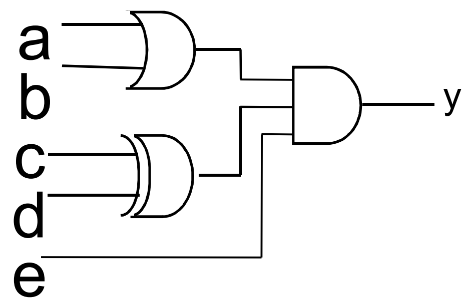
Our Basic Design Flow

Run Industrial EDA tools

Verilog HDL — **Digital IC Description** — $y=(a+b)\&(c\oplus d)\&e$

VCS, Verdi — **Logic Simulation**

Design Compiler — **Logic Synthesis**



Formality — **Logic Circuit**

ICC/Encounter — **Physical Synthesis**

Prime Time — **Layout of design**