**VLSI**
ID: 519021911248
Name: ZhuoHao Li

# Homework 2

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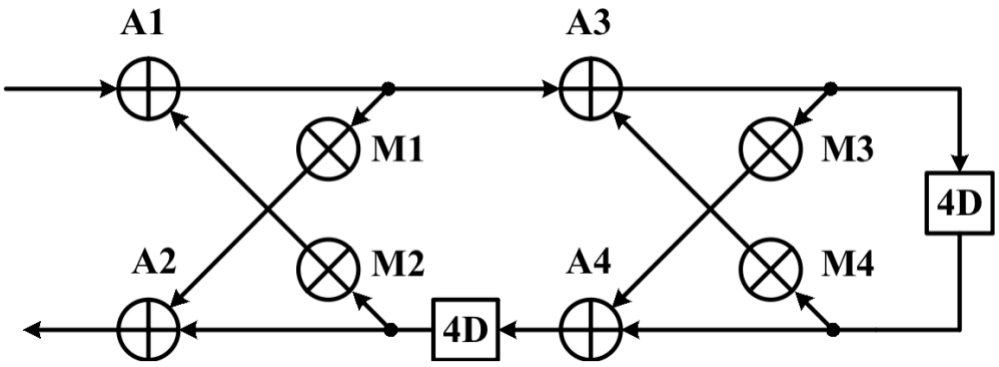
**EX.1**

**Fold the DFG. Assume that each multiplier is pipelined by 2-stages and each adder is pipelined by 1 stage. The multiplication operation requires 2 u.t. and the addition operation requires 1 u.t. and assume the following folding sets for the iteration period N = 2.**

$S_{M1}$ = { M2 , M1 } , $S_{M2}$ = { M3 , M4 } , $S_{A1}$ = { A1 , A2 } , $S_{A2}$ = { A4 , A3 }

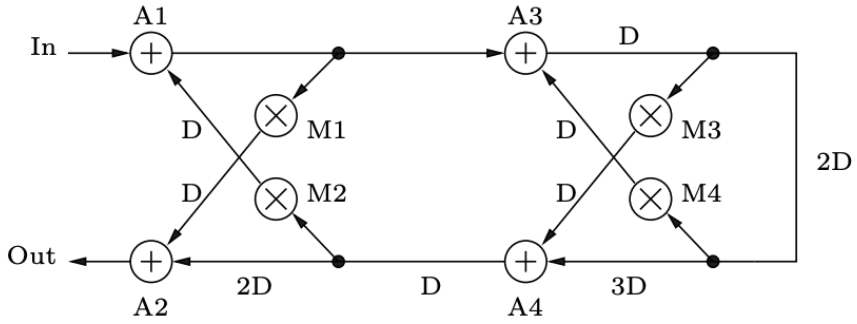
a) Perform retiming for folding so that the folding sets result in nonnegative edge delays in the folded architecture.
b) Fold the retimed DFG.
c) Minimize the number of registers and redesign the folded architecture.




**Solution to EX.1**

**(a)**

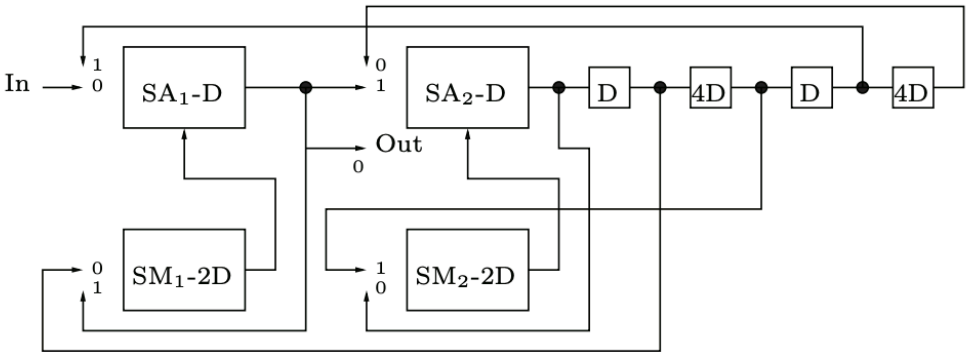
Notes: we cannot simply fold the diagram due to some negative delays generated after folding. For example, $D_F(A3 \to M4) = 2(0) - 1 + 1 - 1 = -1 < 0$, which leads to unimplemented and non-casual system. Retiming can prevent that happen:




**(b)**

There're 11 edges in the retimed diagram:
$D_F(A1 \to M1) = 2(0) - 1 + 1 - 0 = 0$
$D_F(A1 \to A3) = 2(0) - 1 + 1 - 0 = 0$
$D_F(A3 \to M3) = 2(1) - 1 + 0 - 1 = 0$
$D_F(A3 \to M4) = 2(3) - 1 + 1 - 1 = 5$

$D_F(A3 \to A4) = 2(6) - 1 + 0 - 1 = 10$
$D_F(A4 \to A2) = 2(3) - 1 + 1 - 0 = 6$
$D_F(A4 \to M2) = 2(1) - 1 + 0 - 0 = 1$
$D_F(M1 \to A2) = 2(1) - 2 + 1 - 1 = 0$
$D_F(M2 \to A1) = 2(1) - 2 + 0 - 0 = 0$
$D_F(M3 \to A4) = 2(1) - 2 + 0 - 0 = 0$
$D_F(M4 \to A3) = 2(1) - 2 + 1 - 1 = 0$
Folded diagram is as below:




$SA_1, SA_2$ has 1 pipeline delay inside, $SM_1, SM_2$ has 2 pipeline delays inside

**(c)**

Lifetime analysis shows that there are actually only 8 registers (compared to 10) needed.

Table 1: life analysis

| Variable | life |
|---|---|
| A1 | 1 →1 |
| A2 | NULL |
| A3 | 2 →12 |
| A4 | 1 →7 |
| M1 | 3 →3 |
| M2 | 2 →2 |
| M3 | 2 →2 |
| M4 | 3 →3 |

The redesigned architecture is:

Table 2: Register Scheduling

| . | In | A1 | A2 | A3 | A4 | M1 | M2 | M3 | M4 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | |
| 1 | A4 | | | | | | | | |
| 2(0) | A3 | A4 | | | | | | | |
| 3(1) | | A3 | A4 | | | | | | |
| 4(0) | | | A3 | A4 | | | | | |
| 5(1) | | | | A3 | A4 | | | | |
| 6(0) | | | | | A3 | A4 | | | |
| 7(1) | | | | | | A3 | A4 | | |
| 8(0) | | | | | | | A3 | | |
| 9(1) | | | | | | | | A3 | |
| 10(0) | | | | | | | | | A3 |
| 11(1) | | | | | | | | | A3 |
| 12(0) | | | | | | | | | A3 |