VLSI
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Homework 2

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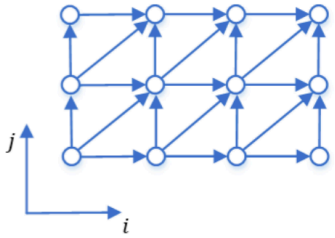
EX.1

7.1 对于右图所示的依赖图

- **下面各组调度和投影中哪组是可行的?**
  - ***a)*** $s^T = [1\ 0]$, $d^T = [1\ 0]$
  - ***b)*** $s^T = [1\ 2]$, $d^T = [2\ -1]$
  - ***c)*** $s^T = [1\ 1]$, $d^T = [1\ 0]$
  - ***d)*** $s^T = [1\ -2]$, $d^T = [1\ 0]$
- **推导每个可行组的投影脉动阵列**



Solution to EX.1

(a)

In the DG, each node has input[0:1] and input[1:0], with output[1:1]. It's similar to the example wo mentioned in class. For a systolic design, $s^T d^T \neq 0$. And teh delay mapping should be larger than 0, due to Delay mapping: [1,-2][0,1]=-2, [1,-2][1,0]=1, [1,-2][1,1]=-1 in the case (d), it's invalid. So for **a), c)**, they're okay. And HUE = 1 for all.

(b)

assume that p^T=[0, 1]

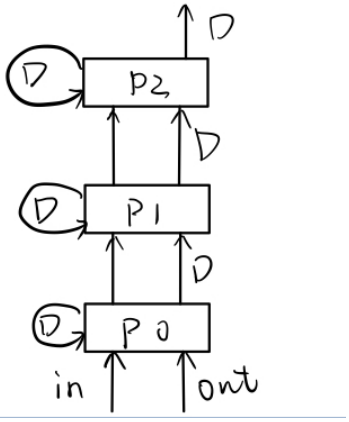
a)

I=[i, j], $p^T I$=j, so for each line, they have the same processor mapping.

s^T=[1, 0], $s^T I$ = i, so for each column, they have the same edge delay.

Edge mapping: [0,1][0,1]=1, [0,1][1,0]=0, [0,1][1,1]=1.

Delay mapping: [1,0][0,1]=0, [1,0][1,0]=1, [1,0][1,1]=1.



c)

I=[i, j], $p^T I$=j, so for each line, they have the same processor mapping.

s^T=[1, 1], $s^T I$ = i+j, so for each column, they have the same edge delay.

Edge mapping: [0,1][0,1]=1, [0,1][1,0]=0, [0,1][1,1]=1.

Delay mapping: [1,1][0,1]=1, [1,1][1,0]=1, [1,1][1,1]=2.