Folding

Version	@March 7, 2022
Property	

Concepts

> trade-off: DECREASE area (1/N) - INCREASE latency (N)

Folding is the reverse operation of Unfolding

eg. Originally, there's 1 inout and output in a cycle period, after folding, there's 1 inout and output in at least N cycle periods. N means folding factor

Math Description

Folding Equation

Details

$U \to V$, delay is $w(e)$. Folding algorithm will be scheduled at $Nl+u$ and $Nl+v$
$NL+v$ for l th iteration

- U output happens at $Nl+u+P_u$
- due to delay on the wire, V uses the output at the time of $N[l+w(e)]+v$

Folding Equation/Latency

$$D_F(U \to V) = Nw(e) - P_u + v - u$$

Folding Set

Folding set is an oder set which execute the same operation, the order is the execute time order mentioned before (u, v)

Order

Elements in folding set need to be WELL ordered, ensuring $D_F(U \to V) \geq 0$ for each. It's called REASONABLE FOLDING

Folding Example

For a specific folding set:

1. calculate D_F for each path

$D_F(U \to V) = Nw(e) - P_u + v - u$

$D_F(1 \to 2) = 4(1) - 1 + 1 - 3 = 1$
$D_F(1 \to 5) = 4(1) - 1 + 0 - 3 = 0$
$D_F(1 \to 6) = 4(1) - 1 + 2 - 3 = 2$
$D_F(1 \to 7) = 4(1) - 1 + 3 - 3 = 3$
$D_F(1 \to 8) = 4(2) - 1 + 1 - 3 = 5$
$D_F(3 \to 1) = 4(0) - 1 + 3 - 2 = 0$
$D_F(4 \to 2) = 4(0) - 1 + 1 - 0 = 0$
$D_F(5 \to 3) = 4(0) - 2 + 2 - 0 = 0$
$D_F(6 \to 4) = 4(1) - 2 + 0 - 2 = 0$
$D_F(7 \to 3) = 4(1) - 2 + 2 - 3 = 1$
$D_F(8 \to 4) = 4(1) - 2 + 0 - 1 = 1$

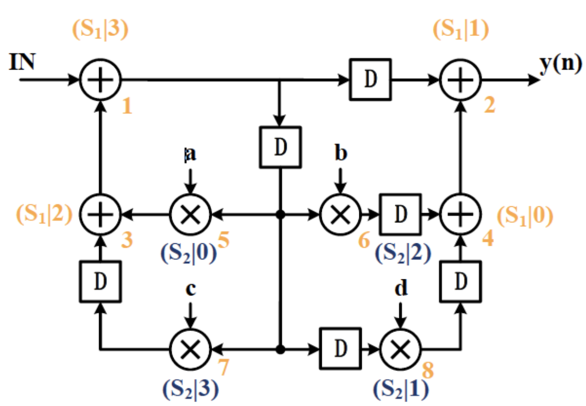
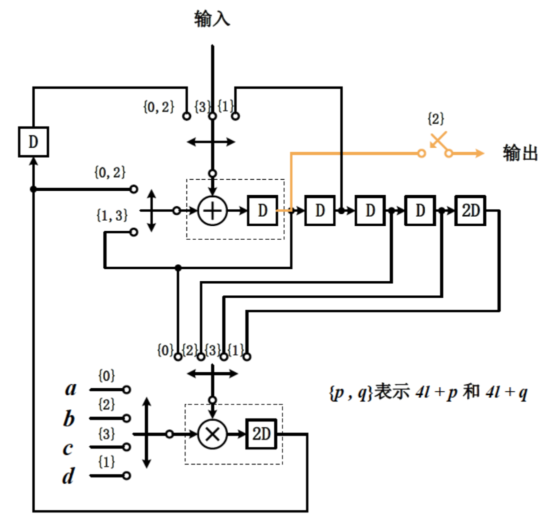


Fig. Lecture6_p28

1. construct each node with basic element by new D_F

   Principles:

   - Use feedback to represent 0 delays
   - Specify every input
   - Coefficient



Register Minimization

Life Analysis

Folding will insert extra registers in the system, life analysis determine the least registers.

How to calculate the largest register number?

- Linear Life Diagram
  - Only consider the first iteration

Step to Minimize

- Calculate the Least Register
- Forward
- Backward

Register Minimization in Folded Arch

- if $V < 0$ → non-rational folding → retiming
  - increase $w(e)$

Step

- retiming
- folding equation, get $D_F(u \to v)$
- life diagram
  - $T_{input} = u + P_U$
  - $T_{output} = T_{input} + max\{D_F(U \to V)\}$
- calculate the least registers
- forward, backward distribute
  - Switch needed, which can manage datapath valid due the life diagram before.