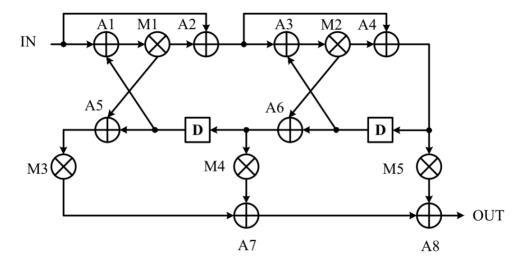
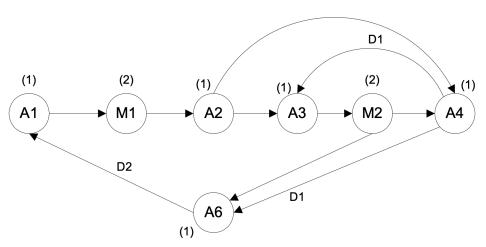
1 Question

Compute the iteration bound of this DFG using the LPM algorithm assuming that addition and multiplication require 1 and 2 u.t., respectively.



2 Answer

First, create the DFG of the original circuits. Only the elements with feedback or in a loop can be shown in DFG.



DFG OF FEEBACK LOOP IN THE UPPER PART WITH 2 DELAY ELEMENTS

So, the $L^{(1)}$ can be compute as below:

$$L^{(1)} = \left[\begin{array}{cc} 4 & 4 \\ 8 & 8 \end{array} \right]$$

\mathbf{VLSI}

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${\bf Homework}\ {\bf 1}$

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So, we can have $L^{(2)}, L^{(\infty)}$,

$$L^{(2)} = \left[\begin{array}{cc} 12 & 12 \\ 16 & 16 \end{array} \right]$$

$$L^{(\infty)} = MAX\{\frac{4}{1}, \frac{8}{1}, \frac{12}{2}, \frac{16}{2}\} = 8$$

So the boundary iteration is 8.