# **Systolic Array**

<b>E</b> Version	@March 14, 2022
<b>■</b> Property	

Concept

DG

Vector

Design Flow

Regular DG

Projection, Process Vector, Scheduling Vector

Edge Mapping

The End

# **Concept**

#### DG

- DG: describe basic datapath and relations between different elements in algorithm
  - **Nodes**: computing in a system
  - **Edges**: priority constraints
  - No delay elements

#### **Vector**

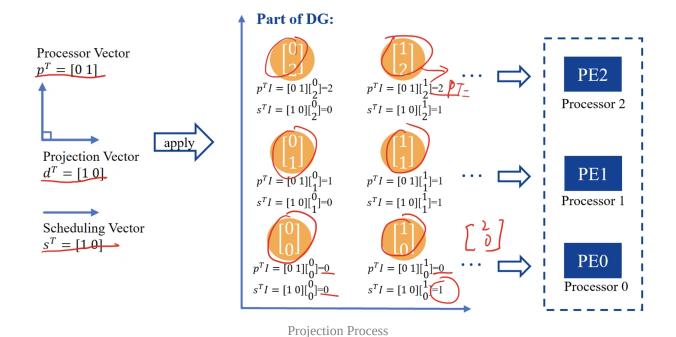
- $I^T$ 
  - represent **location** of a computing element
- $ullet d^T$  ,  $p^Td=0$  is necessary
  - projection vector
- $p^T$ 
  - $\circ \;\;$  process vector (or space vector),  $p^T I$  represents I will be executed by the processor
- $s^T$

scheduling vector

# **Design Flow**

#### Regular DG

### **Projection, Process Vector, Scheduling Vector**



Different Vectors mean different application

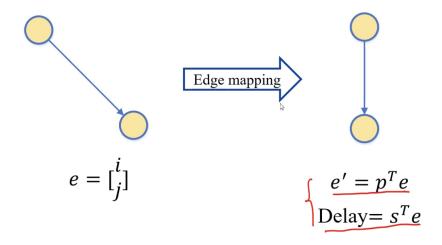
 $p^Te$  represents **Process Data Flow Direction**,  $s^Te$  represents **Timing Data Flow Direction** 

- B1
  - Broadcast Input, Weights Stay, Move Results
- B2
  - Broadcast Input, Move Weights, Result Stay
- F

Systolic Array 2

• Fan-In Results, Move Inputs, Weights Stay

## **Edge Mapping**



 $e' = p^T e$  $Delay = s^T e$ 

- method
  - syllabus: input, weight, output
  - o formula:
    - e' means data flow direction in Arch
    - ullet Delay means delay in Arch

### The End