SPI Communication used by the Accelerometer

1) Timing Diagram for 4-Wire SPI Communication

We used 4-fire configuration for SPI communication, the timing diagram is shown below.

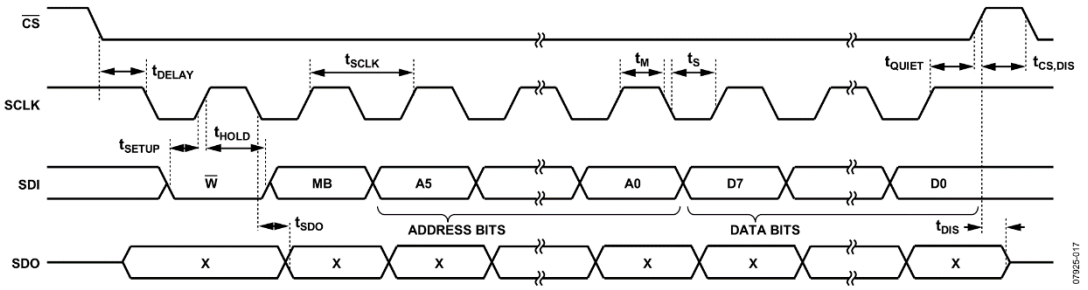

Figure 5. SPI 4-Wire Write

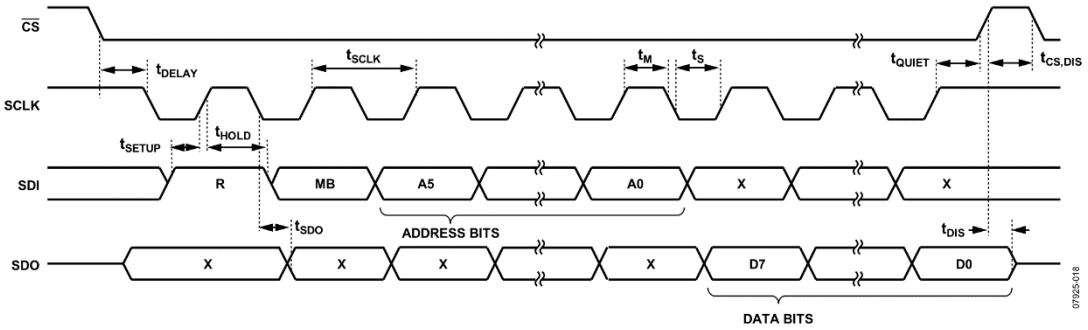

Figure 6. SPI 4-Wire Read

Figure 1 Timing Diagram for 4-Wire SPI Communication, from ADXL345 Data Sheet

1. **CS**: To start the transmission, we need to set CS line to be low, which is the serial port enable line controlled by the SPI master; to end the transmission, CS line should be set to high.
2. **SCLK**: The serial port clock SCLK is supplied by the SPI master. During no-transmission period when CS is high, SCLK would also keep high, thus, we set *the clock polarity* to be 1.
3. **SDI / SDO**: SDI and SDO function as the serial data input and output, respectively. Data are supposed to be sampled at the rising edge of SCLK, thus, we set *the clock phase* to be 1.
   a) For the first 8 bits (the first byte):
      - The first bit is Read/Write control bit: 0 for Write and 1 for Read.
      - The second bit is multi-byte bit, which controls to read/write a single byte or multiple bytes in a single transmission: 0 for single byte and 1 for multiple bytes.
      - The last six bits are for the register address.

   b) After the first byte is set, each subsequent eight clock pulses (a set of clock pulses) will cause the device to point to the next register for a read or write, until the clock pulses stop and CS is set to high.

   c) If we want to perform read/write on non-sequential registers, a complete new cycle are required: from setting CS to low, addressing the new register, to setting CS to high.

2) Circuit Connection

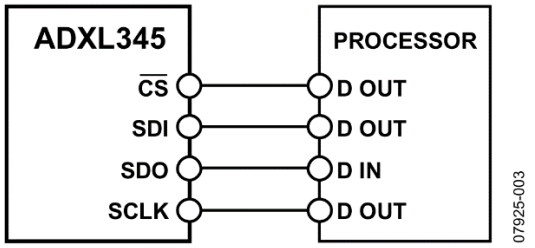

Figure 2 4-Wire SPI Connection Diagram, from ADXL345 Data Sheet

From the 4-wire SPI connection diagram in the data sheet, we connected the circuit as below:

Table 1 Circuit Connection Map

ADXL345	ESP8266
VIN	3V
GND	GND
CS	Pin (16)
SDO	MI
SDA	MO
SCL	SCK

3) Initialization Sequence

We initialized five registers of ADXL345 in our initialization function:

1. **BW_RATE**: This is data rate and power mode control register (0x2C), the value is set to be 00001010, as we selected normal operation mode and set the output data rate as 100Hz.
2. **POWER_CTL**: This is power-saving features control register (0x2D), the value is set to be 00101000. We set the link bit to the value of 1 in the register. Thus, both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. The AUTO_SLEEP bit is set to be 0 to disable auto sleep. Besides, the measure bit is set to be 1 to place the part into measurement mode.
3. **INT_ENABLE**: This is interrupt enable control register(0x2E), the value is set to be 11111111 to enable their respective functions to generate interrupts.
4. **DATA_FORMAT**: This is data format control register(0x31), the value is set to be 00001000.
   - The SELF_TEST bit is set to be 0 to disable the self-test force;
   - The SPI bit is set to be 0 to set the device to 4-wire SPI mode;
   - The INT_INVERT bit is set to be 0 to set the interrupts to active high;
   - The FULL_RES bit is set to be 1 to set the device to full resolution mode;
   - The Justify bit is set to be 0 to set the device to select right justified mode with sign extension;
   - The Range bits are set to be 00 to set g range to ± 2g.
5. **FIFO_CTL**: This is FIFO control register(0x38), the value is set to be 10000000.
   The FIFO_MODE bits are set to be 01 for the Stream mode.
   As the low power mode is not used, the sample bit and trigger bit are set to be 0 to finish initialization.