Zhuwei Qin

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EDUCATION

Oregon State University, Corvallis, OR
Master of Engineering(MENG), GPA: 3.67/4.0 Sep. 2015 to present
Electrical & Computer Engineering
Related courses: Energy-efficient VLSI Design, VLSI System Design(FPGA), Computer Architecture, Interconnection Networks, GPU Architecture, CMOS Integrated Circuits

Tianjin University of Science & Technology(TUST), Tianjin, China
Bachelor of Engineering, GPA:87/100 Aug. 2010 to Jul. 2014

SKILLS

Programming language: System Verilog, C, JAVA, C++, SQL

Software/Platforms: Quartus II, FPGA, Modelsim, Linux, Arduino, Myeclipse, Matlab

SELECTED PROJECTS

Warp Scheduling for GPGPU Workloads Sep.2016 to present

- Investigating stall factors of selected warp such as synchronization primitives, no available instructions in the instruction buffer or instruction cache misses, control hazard, data hazard, data cache misses, and structural hazard
- Determining the scheduling latency that is caused by the scheduling policy.
- Profiling the behavior of GPGPU workloads by using GPGPU-sim.

FPGA-Based Voltmeter Apr. 2016 to Jun. 2016

- Designed transmit and receive UART interface to communicate to and from PC
- Select the desired ADC analog input channel by sending a single number from PC
- Sent voltage reading back to the PC via UART twice a second (2Hz)

Thin Client GameStream System Apr. 2016 to Jun. 2016

- Steaming game from a remote computer to the thin client based on Raspberry Pi 3.
- Built the Linux environment to support the NVidia game stream

Design of Multiplier and its VLSI Implementation Jan. 2016 to Mar. 2016

- Designed NAND, NOR, XOR gates schematic and creating the logic gates Layout.
- Running DRC, ERC, and NCC check and verified whether the gates functions properly in LTspice.
- Designed a full-adder and a 4x4 bit multiplier in schematic and layout.
- The max clock rate under Monte Carlo transistor model is 1.54Ghz

Survey on bypass of effective power-gating Jan. 2016 to Mar. 2016

- Survey on conventional power-gating techniques
- Proposed a new scheme, which can break the intrinsic dependence between node and router

Book Inventory Management (Java EE web application) Jun. 2016 to Aug. 2016

- Developed a Web application to allow user to add delete and view books.
- Implemented **MVC(struts)** framework, using Java Servlets, JSP, and JavaBeans technologies.
- Implemented data storage by **MySQL** database.
- Implemented a DAO manager using JDBC and connection pools

Publications

2014 Arduino Easy Start（with Y.Hai, Z.Dai）

HONORS AND AWARDS

2015 INTO OSU Continued Success Scholarship
2014 Thesis design award as outstanding graduate in TUSU
2012 Honorable Mention, “TI Cup” Tianjin Electronic Design Competition for College Students
2012 Outstanding Individual, TUST