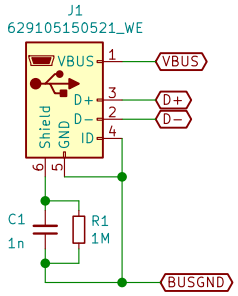
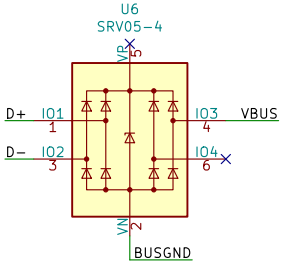
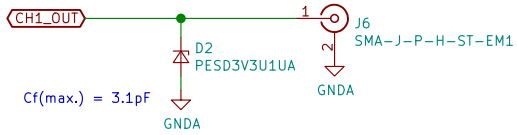
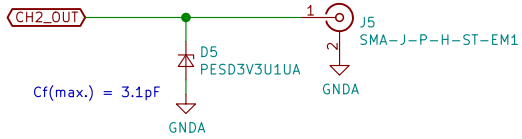
USB connector & ESD protection





Channels output connector (SMA)





Mounting holes

Power

Power.sch

DAC

DAC.sch

FPGA

FPGA.sch

MCU

MCU.sch

TOP

Sheet: /
File: arbitrary_func_gen.sch

Title: Arbitrary function generator

Size: A4	Date: 11.07.2019	Rev: 1.0
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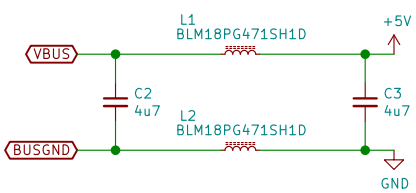
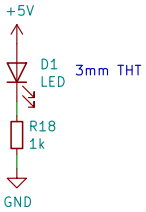
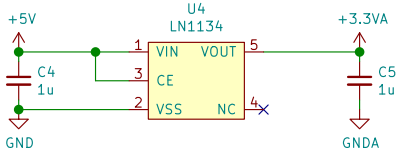
USB input filter

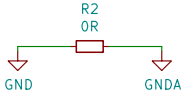


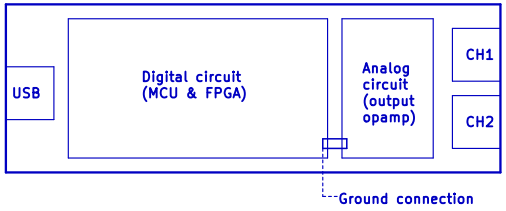


Analog Supply



Analog & digital ground connection

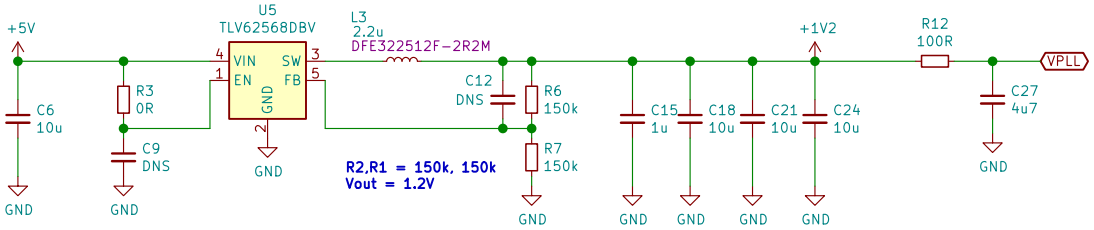


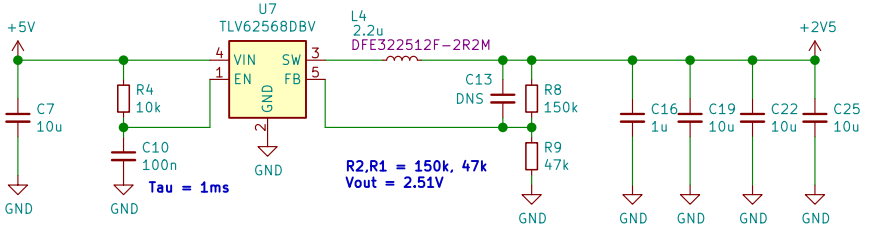


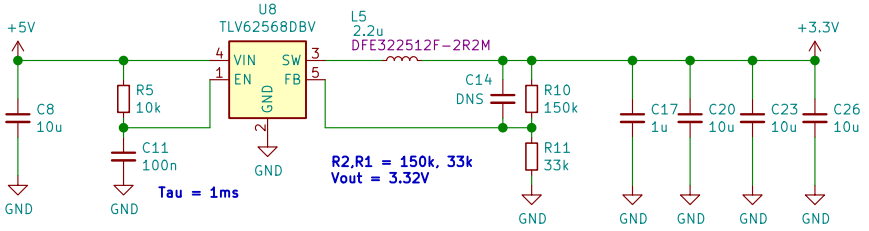
MCU & FPGA Supply

Ramp-up (soft start):
1.2V -> 1.3 V/ms (FPGA: 10 V/ms MAX.)
2.5V -> 2.6 V/ms
3.3V -> 3.5 V/ms

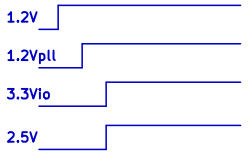
Vfb = 0.6V







Power-up sequence for FPGA



Power supply

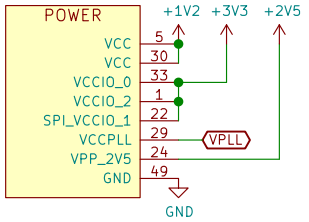
Sheet: /Power/
File: Power.sch

Title: Arbitrary function generator

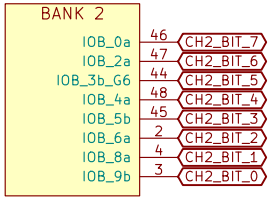
Size: A4 | Date: **11.07.2019** | **Rev: 1.0**
KiCad E.D.A. kicad (5.1.2)-2 | Id: 2/5

FPGA

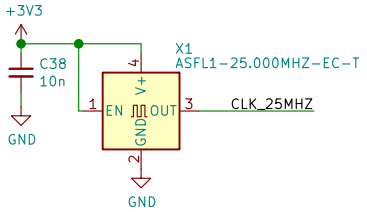
U1D
IEC5LP1K-QFN48



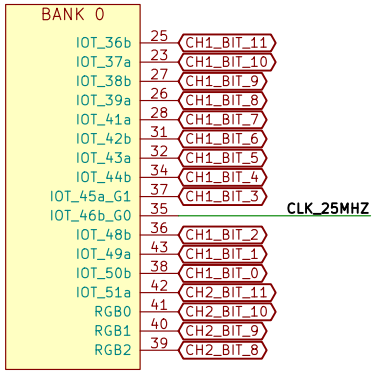
U1C
IEC5LP1K-QFN48



25 MHz clock

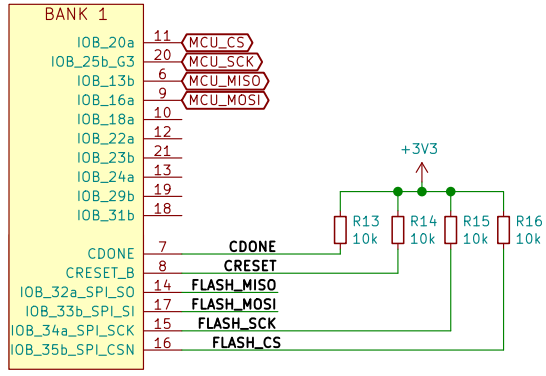


U1A
IEC5LP1K-QFN48

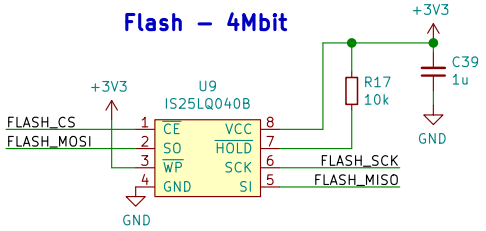


*bold labels are fixed

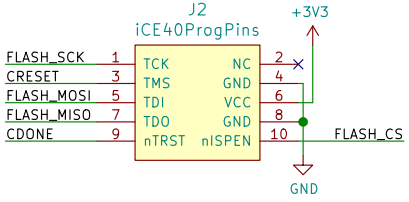
U1B
IEC5LP1K-QFN48



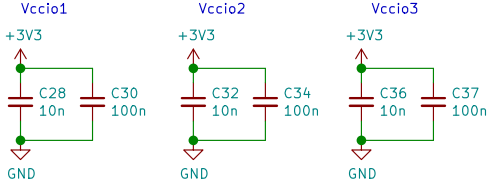
Flash – 4Mbit

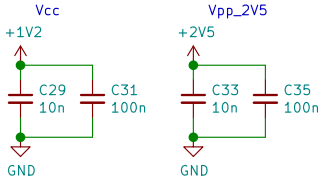


Programming header



Bypass capacitors





FPGA

Sheet: /FPGA/
File: FPGA.sch

Title: Arbitrary function generator

Size: A4	Date: 11.07.2019	Rev: 1.0
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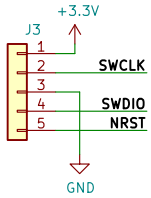
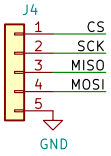
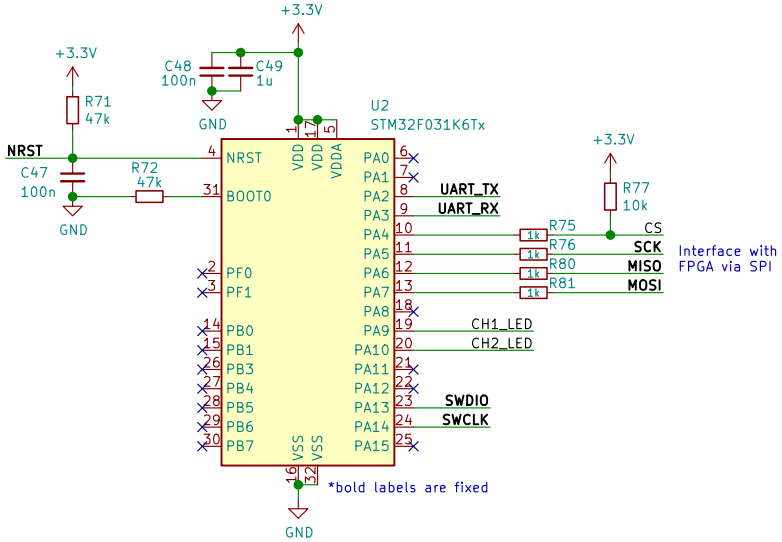
Programming header

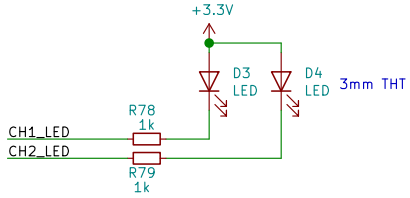


Debug header



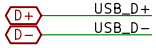


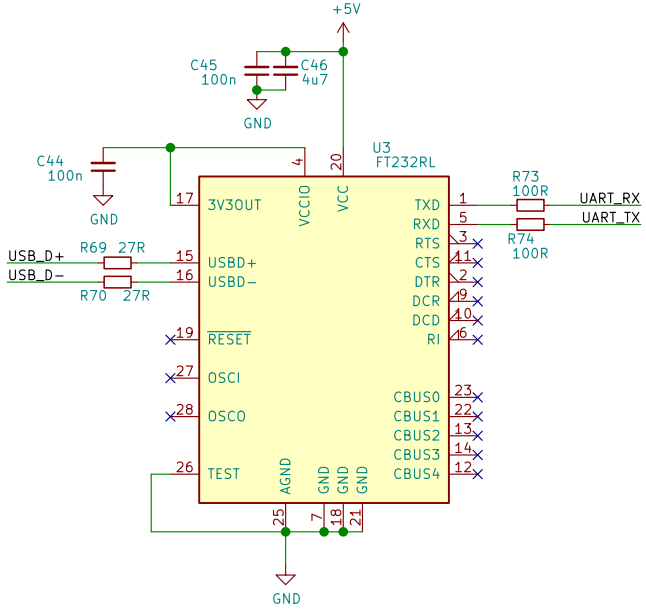
Channel Status LEDs



Interface with FPGA

Interface with PC





MCU & PC interface

Sheet: /MCU/ File: MCU.sch		
Title: Arbitrary function generator		
Size: A4	Date: **11.07.2019**	**Rev: 1.0**
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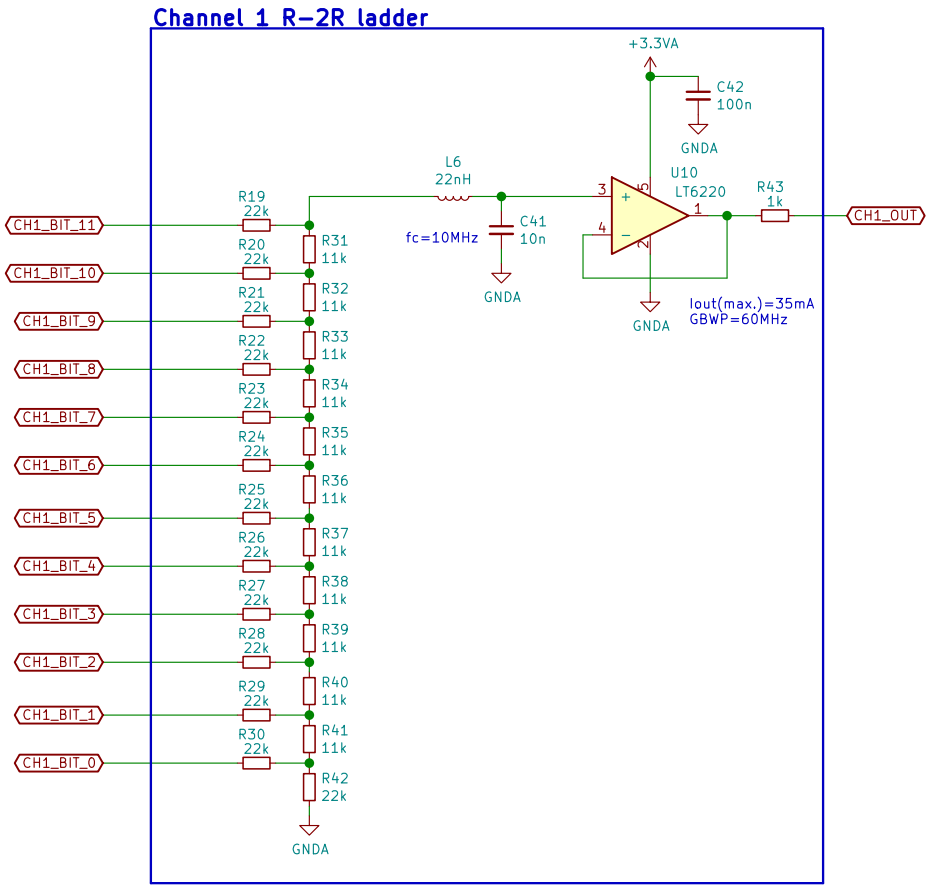
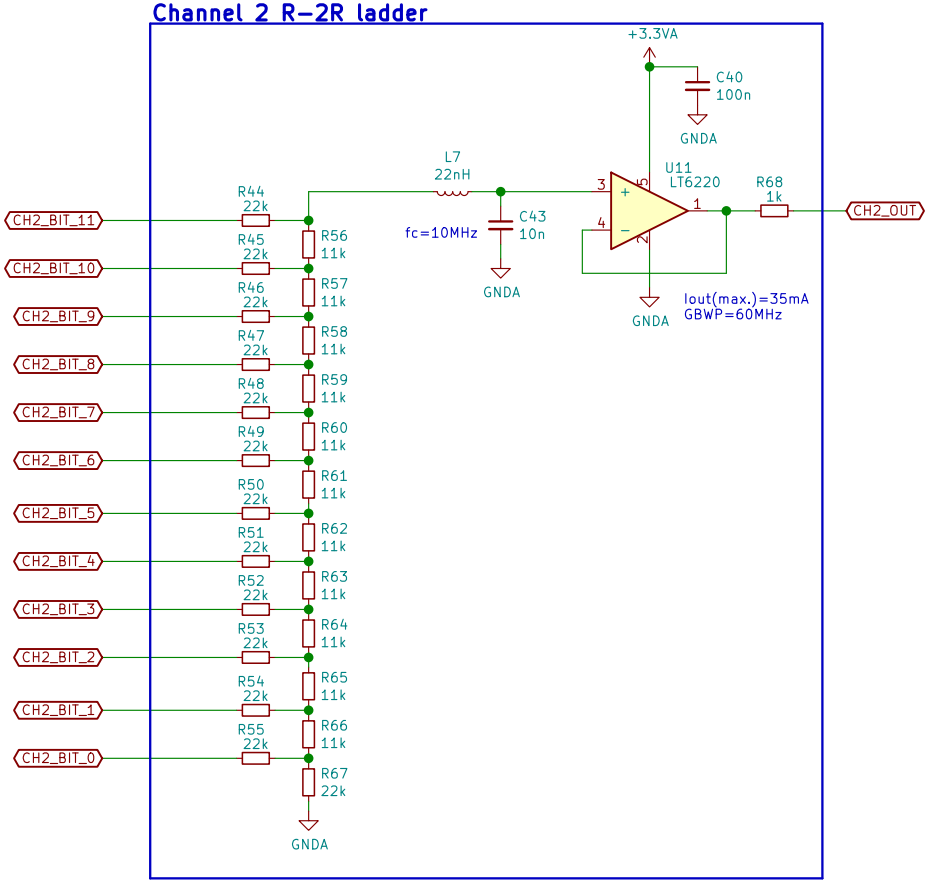
12-bit DAC





DAC

Sheet: /DAC/
File: DAC.sch

Title: Arbitrary function generator

Size: A4	Date: **11.07.2019**	**Rev: 1.0**
KiCad E.D.A. kicad (5.1.2)-2		Id: 5/5