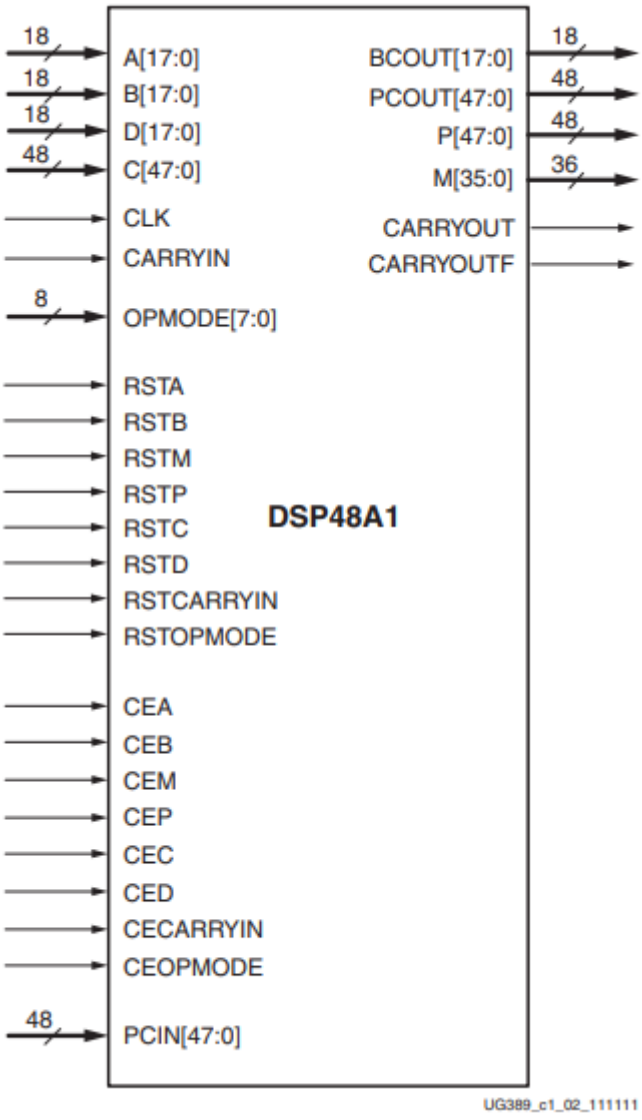
Spartan6 - DSP48A1

Made by: Ziad Alaa Anis Mohamed Kamal Kassem



Project Specs:

The Spartan-6 family offers a high ratio of DSP48A1 slices to logic, making it ideal for math intensive applications. Design DSP48A1 slice of the spartan6 FPGAs.

Parameter	Function
A0REG, A1REG, B0REG, and B1REG	The A0REG, A1REG, B0REG, and B1REG attributes can take values of 0 or 1. These values define the number of pipeline registers in the A and B input paths. A0REG defaults to 0 (no register). A1REG defaults to 1 (register). B0REG defaults to 0 (no register) B1REG defaults to 1 (register). A0 and B0 are the first stages of the pipelines. A1 and B1 are the second stages of the pipelines
CREG, DREG, MREG, PREG, CARRYINREG, CARRYOUTREG, and OPMODEREG	These attributes can take a value of 0 or 1. The number defines the number of pipeline stages. Default: 1 (registered)
CARRYINSEL	The CARRYINSEL attribute is used in the carry cascade input, either the CARRYIN input will be considered or the value of opmode[5]. This attribute can be set to the string CARRYIN or OPMODE5. Default: OPMODE5. Tie the output of the mux to 0 if none of these string values exist.
B_INPUT	The B_INPUT attribute defines whether the input to the B port is routed from the B input (attribute = DIRECT) or the cascaded input (BCIN) from the previous DSP48A1 slice (attribute = CASCADE). Default: DIRECT. Tie the output of the mux to 0 if none of these string values exist.
RSTTYPE	The RSTTYPE attribute selects whether all resets for the DSP48A1 slice should have a synchronous or asynchronous reset capability. This attribute can be set to ASYNC or SYNC. Default: SYNC.

Signal Name	Function
A	18-bit data input to multiplier, and optionally to post adder/subtracter depending on the value of OPMODE[1:0].
B	18-bit data input to pre-adder/subtracter, to multiplier depending on OPMODE[4], or to post-adder/subtracter depending on OPMODE[1:0].
C	48-bit data input to post-adder/subtracter.
D	18-bit data input to pre-adder/subtracter. D[11:0] are concatenated with A and B and optionally sent to post-adder/subtracter depending on the value of OPMODE[1:0].
CARRYIN	carry input to the post-adder/subtracter
M	36-bit buffered multiplier data output, routable to the FPGA logic. It is either the output of the M register (MREG = 1) or the direct output of the multiplier (MREG = 0).
P	Primary data output from the post-adder/subtracter. It is either the output of the P register (PREG = 1) or the direct output of the post adder/subtracter (PREG = 0).
CARRYOUT	Cascade carry out signal from post-adder/subtracter. It can be registered in (CARRYOUTREG = 1) or unregistered (CARRYOUTREG = 0). This output is to be connected only to CARRYIN of adjacent DSP48A1 if multiple DSP blocks are used.
CARRYUOUTF	Carry out signal from post-adder/subtracter for use in the FPGA logic. It is a copy of the CARRYOUT signal that can be routed to the user logic.

Signal Name	Function
CLK	DSP clock
OPMODE	Control input to select the arithmetic operations of the DSP48A1 slice.

Signal Name	Function
CEA	Clock enable for the A port registers: (A0REG & A1REG).
CEB	Clock enable for the B port registers: (B0REG & B1REG).
CEC	Clock enable for the C port registers (CREG).
CECARRYIN	Clock enable for the carry-in register (CYI) and the carry-out register (CYO).
CED	Clock enable for the D port register (DREG).
CEM	Clock enable for the multiplier register (MREG).
CEOPMODE	Clock enable for the opmode register (OPMODEREG).
CEP	Clock enable for the P output port registers (PREG = 1).

Notes:

-Note: opmode input has a register and mux pair in the design entry the same way as the input A, D, or C.

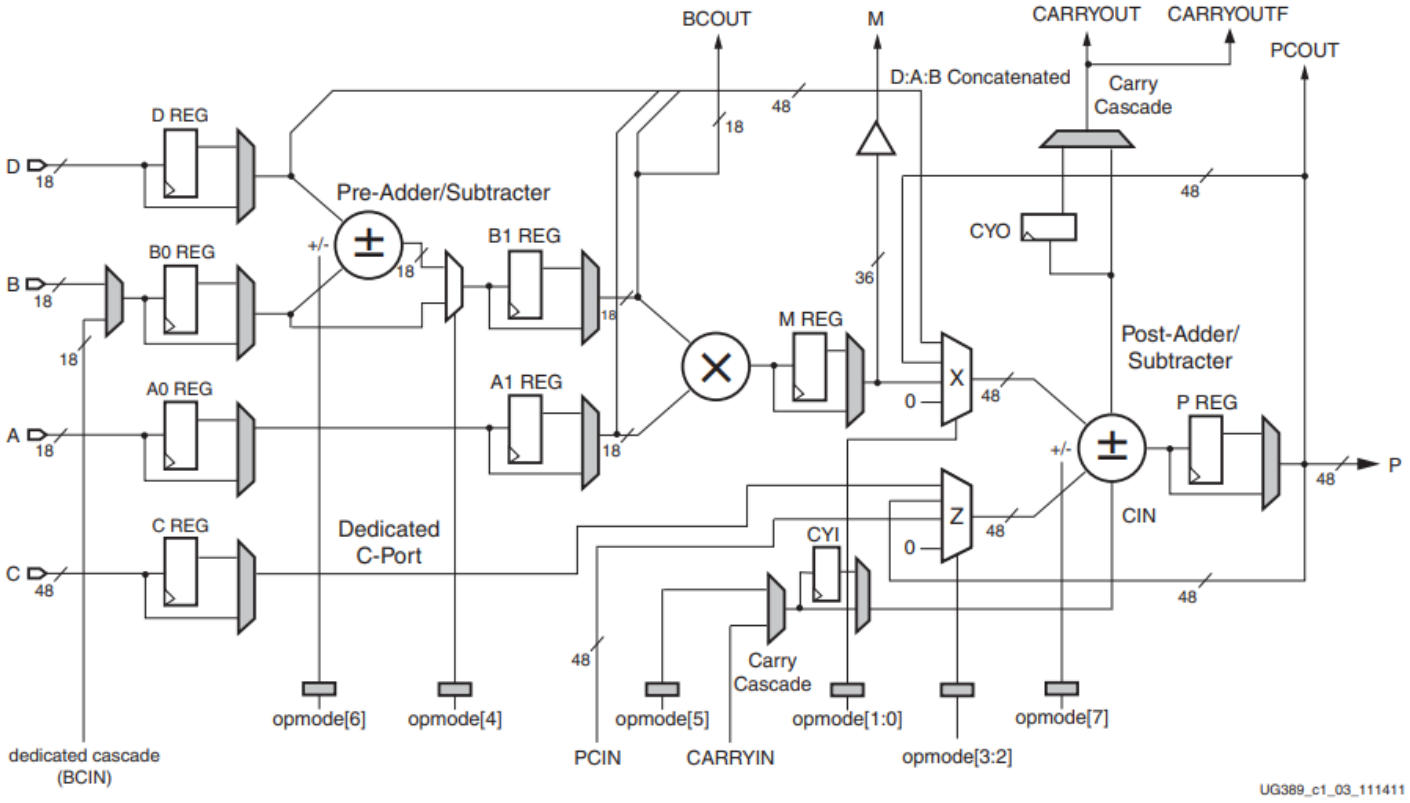
-Reset Input Ports: All the resets are active high reset. They are either sync or async depending on the parameter RSTTYPE.

Signal Name	Function
RSTA	Reset for the A registers: (A0REG & A1REG).
RSTB	Reset for the B registers: (B0REG & B1REG).
RSTC	Reset for the C registers (CREG).
RSTCARRYIN	Reset for the carry-in register (CYI) and the carry-out register (CYO).
RSTD	Reset for the D register (DREG).
RSTM	Reset for the multiplier register (MREG).
RSTOPMODE	Reset for the opmode register (OPMODEREG).
RSTP	Reset for the opmode register (OPMODEREG).

Signal Name	Function
BCIN	Cascade input for Port B.
BCOUT	Cascade output for Port B.
PCIN	Cascade input for Port P.
PCOUT	Cascade output for Port P.

OPMODE Pin Descriptions:

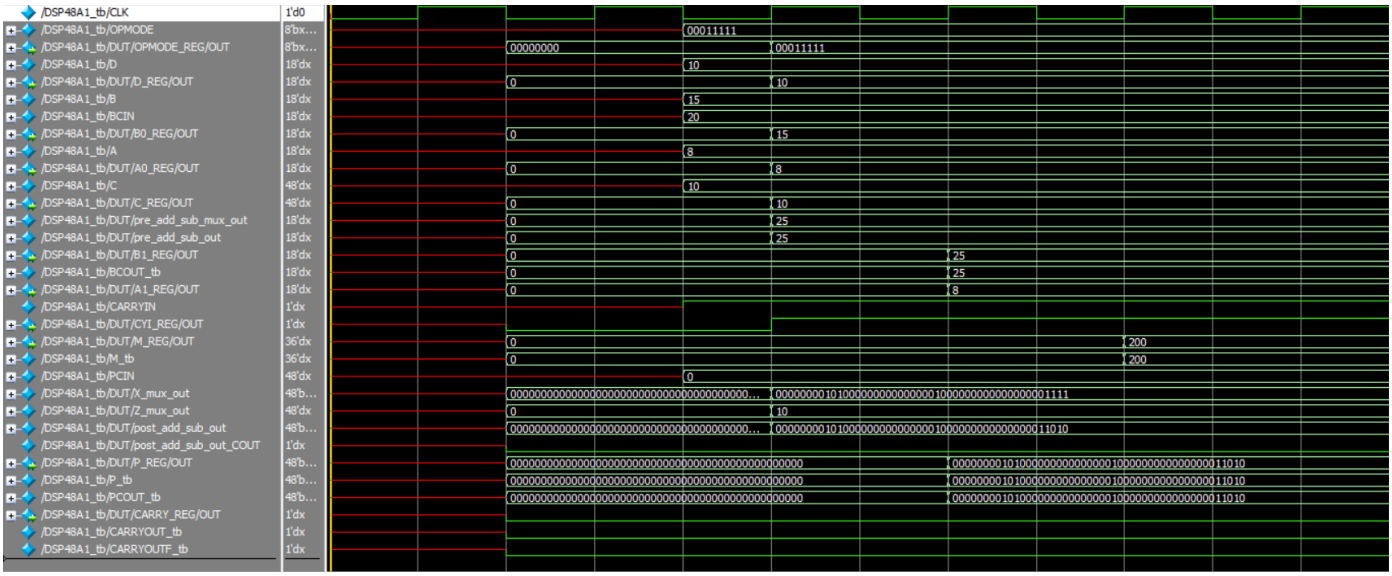
Port Name	Function
OPMODE[1:0]	Specifies the source of the X input to the post-adder/subtracter
OPMODE[3:2]	Specifies the source of the Z input to the post-adder/subtracter
OPMODE[4]	Specifies the use of the pre-adder/subtracter
OPMODE[5]	Forces a value on the carry input of the carry-in register (CYI) or direct to the CIN to the post-adder. Only applicable when CARRYINSEL = OPMODE5
OPMODE[6]	Specifies whether the pre-adder/subtracter is an adder or subtracter
OPMODE[7]	Specifies whether the post-adder/subtracter is an adder or subtracter



Test Bench 1:

Measuring the activity of:

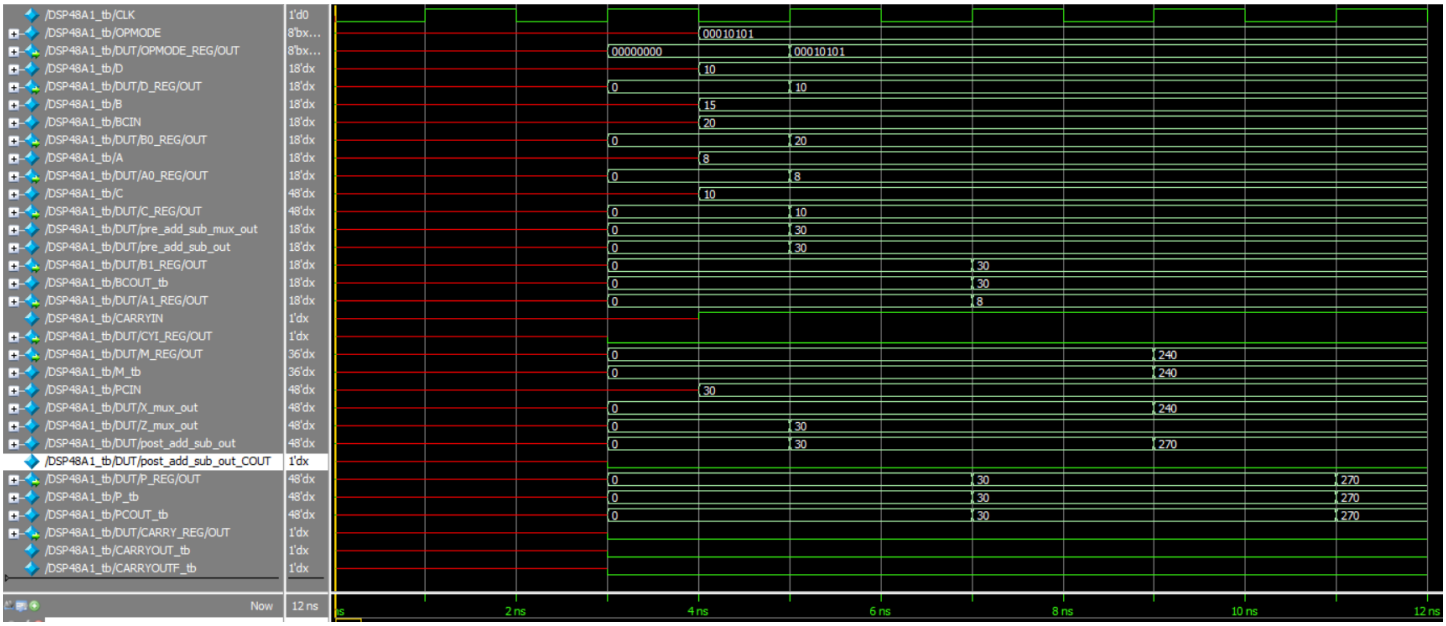
- All the Registers Activated
- The Asynchronous Reset
- B input → B
- Concatenation of D:A:B
- Carry in selection →Carry in



Test Bench 2:

Measuring the activity of:

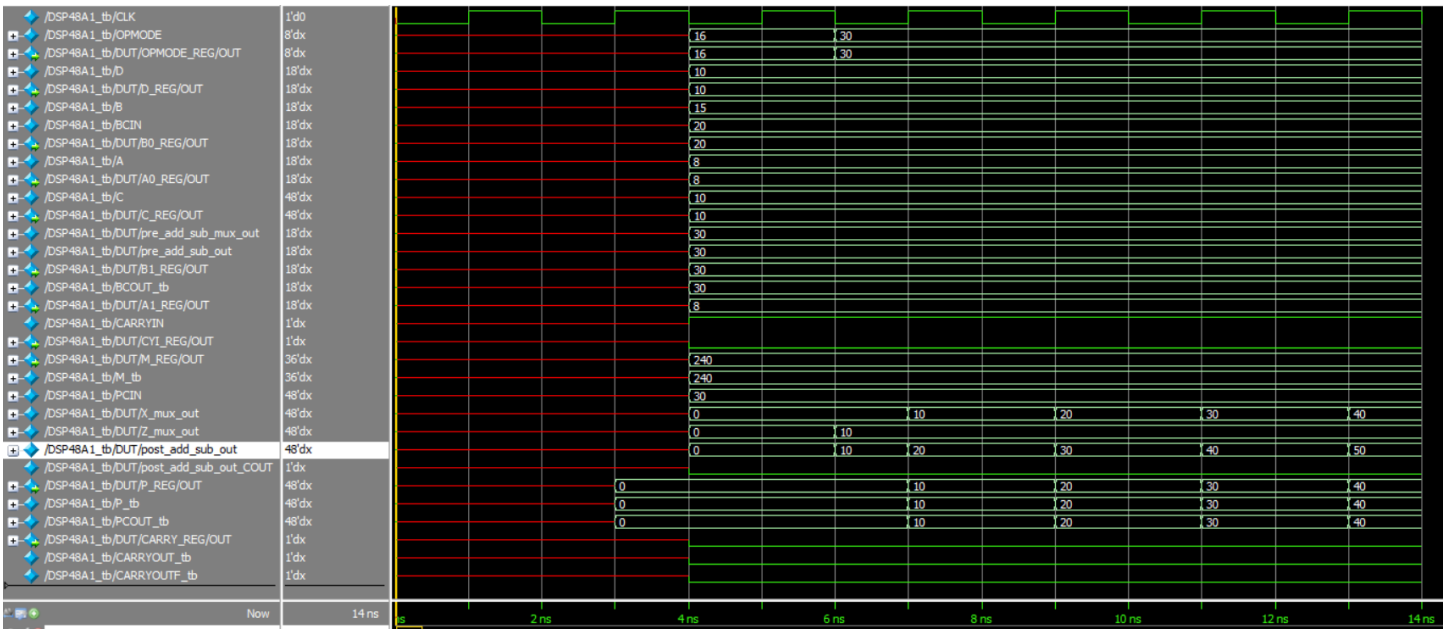
- All the Registers Activated
- The Synchronous Reset
- B input → BCIN
- Multiplication and M_REG functionality
- Z mux → PCIN
- Carry in selection →OPMODE[5]



Test Bench 3:

Measuring the activity of:

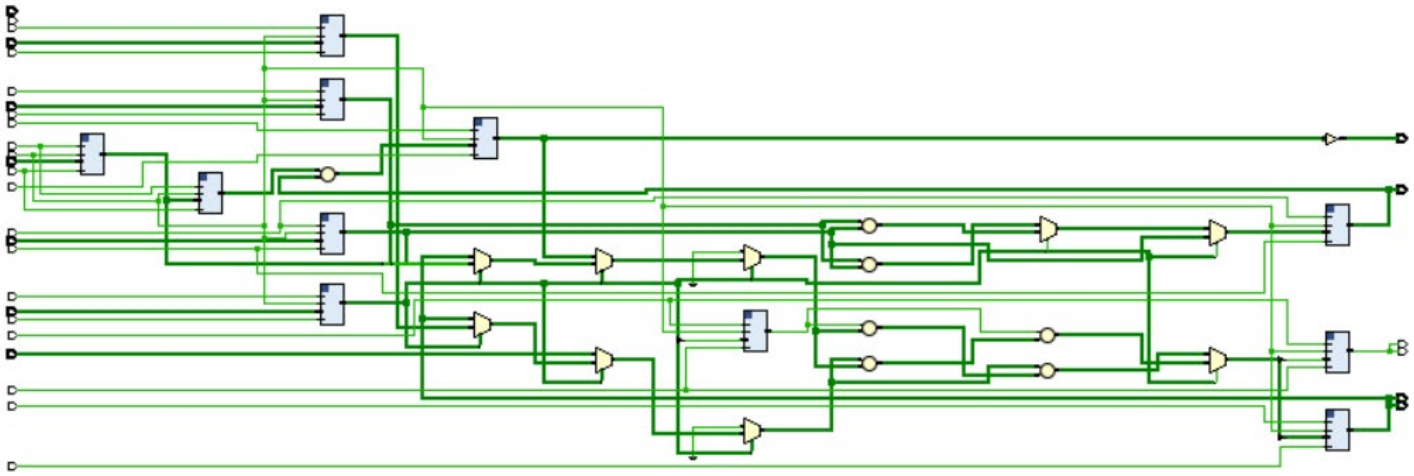
- All the Registers Deactivated Except PREG for testing the X MUX
- B input → BCIN
- X mux → P
- Z mux → C
- Carry in selection →OPMODE[5]



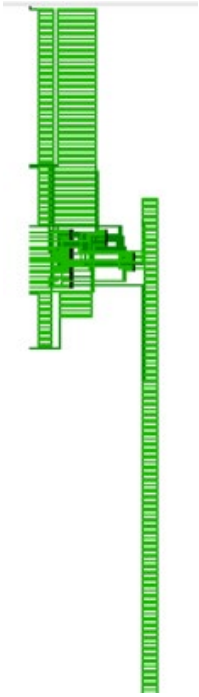
Automation Script for Questa-sim: Using Run.do file

Vivado For Synthesizing :

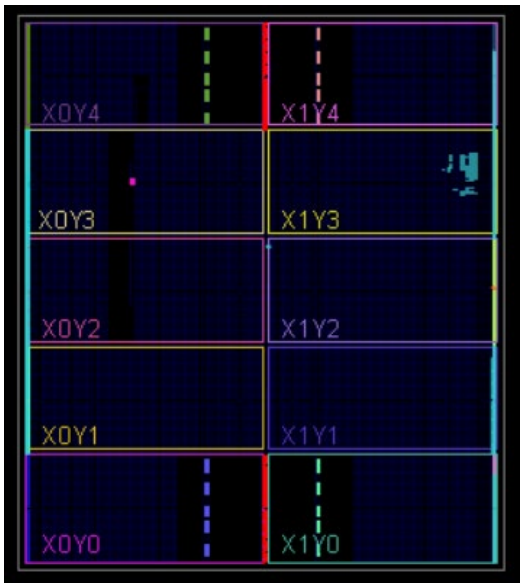
Elaboration:



Synthesis:



Implementation:



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.761 ns	Worst Hold Slack (WHS):	0.263 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	88	Total Number of Endpoints:	88	Total Number of Endpoints:	145

All user specified timing constraints are met.

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | **Utilization**

Hierarchy

Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	237	143	94	237	51	1	327	1

Tcl Console | **Messages** | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Warning (68) | Info (246) | Status (475) | Show All

[Synth 8-2490] overwriting previous definition of module DSP48A1 [Desgin.v:1]
[Synth 8-3331] design param_mux__parameterized0 has unconnected port CEN (21 more like this)
Synthesis (43 warnings)
[Synth 8-2490] overwriting previous definition of module DSP48A1 [Desgin.v:1]
[Synth 8-3331] design param_mux__parameterized0 has unconnected port CEN (40 more like this)
[Constraints 18-5210] No constraint will be written out.
Implementation (1 warning)
Route Design (1 warning)
DRC (1 warning)
Pin Planning (1 warning)
[DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SPIx4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), and Y27 (IO_L6P_T0_FCS_B_14)

Questa-lint:

Methodology:

-FPGA

-use goal: Implementation

condition_const	Condition expression is a constant. Module DSP48A1,…	DSP48A1	Rtl Design Style	open	unassig…	
condition_const	Condition expression is a constant. Module DSP48A1,…	DSP48A1	Rtl Design Style	open	unassig…	
assign_with_multi_arith_…	Assignment statement has more than one arithmetic o…	DSP48A1	Rtl Design Style	open	unassig…	2.10.6.6, 2.10.6.7
conditional_operator_nes…	Conditional operator has a nested conditional operato…	DSP48A1	Rtl Design Style	open	unassig…	2.1.5.1
feedthrough_path	Module has a feedthrough path from an input port to a…	param_mux	Connectivity	open	unassig…	2.5.1.6
gen_label_missing	Generate block label missing in the module. GenBlock…	param_mux	Rtl Design Style	open	unassig…	
multiplication_operator	Expression has a multiplication operator. Module DSP…	DSP48A1	Rtl Design Style	open	unassig…	2.10.6.5
parameter_name_duplicate	Same parameter name is used in more than one mod…	DSP48A1	Nomenclature…	open	unassig…	1.1.4.3, 3.2.2.2
reserved_keyword	Name of the design element matches a reserved key…	param_mux	Nomenclature…	open	unassig…	1.1.1.3
reserved_keyword	Name of the design element matches a reserved key…	param_mux	Nomenclature…	open	unassig…	1.1.1.3
reserved_keyword	Name of the design element matches a reserved key…	param_mux	Nomenclature…	open	unassig…	1.1.1.3
unloaded_input_port	Module input drives no logic. Port CARRYIN, Module …	DSP48A1	Connectivity	open	unassig…	
unloaded_input_port	Module input drives no logic. Port BCIN, Module DSP…	DSP48A1	Connectivity	open	unassig…	
unloaded_input_port	Module input drives no logic. Port CEN, Module para…	param_mux	Connectivity	open	unassig…	
unloaded_input_port	Module input drives no logic. Port CLK, Module param…	param_mux	Connectivity	open	unassig…	
unloaded_input_port	Module input drives no logic. Port RST, Module param…	param_mux	Connectivity	open	unassig…	
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
line_char_large	Line has more characters than the specified limit. Curr…	none	Rtl Design Style	open	unassig…	3.1.4.5
multi_ports_in_single_line	Multiple ports are declared in one line. Module DSP48…	DSP48A1	Rtl Design Style	open	unassig…	3.5.6.3
multi_ports_in_single_line	Multiple ports are declared in one line. Module param…	param_mux	Rtl Design Style	open	unassig…	3.5.6.3

```
# ==========================================================================
# Status Commands
# Version 2021.1 4558100 win64 28-Jan-2021
# Timestamp     : 2025-02-25 16:45:45
# Description   : Provides list of commands associated with the status(s) that are exported from GUI.
# Design        : DSP48A1
# Database      : D:/Kareem_Wassem/DESIGN/Projects/Project_1/lint.db
# ==========================================================================


lint report item  -arg module=param_mux  -arg port1=IN  -arg port2=OUT  -arg file=Paramtrized_mux.v  -check {feedthrough_path} -status {uninspected}
lint report item  -arg expression=Z_mux_out+X_mux_out+{'h000000000000,carry_mux_out}  -arg count=2  -arg module=DSP48A1  -arg file=Desgin.v  -check {assign_with_multi_arith_operations} -rtl_id {1bda49de_00200} -status {uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {arith_expr_with_conditional_operator} -message {All are acceptable} -owner {Ziad Kassem} -reviewer {Eng. Magdy} -rtl_id {1bda49de_00200} -status {waived}
lint report item  -arg count=113  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg count=123  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg count=133  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {multiplication_operator} -rtl_id {cdac293_00200} -status {uninspected}
lint report item  -arg count=146  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {multi_ports_in_single_line} -status {uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {arith_expr_with_conditional_operator} -message {All are acceptable} -owner {Ziad Kassem} -reviewer {Eng. Magdy} -rtl_id {839a1935_00200} -status {waived}
lint report item  -arg count=127  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg count=122  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg module=param_mux  -arg port=RST  -arg file=Paramtrized_mux.v  -check {unloaded_input_port} -status {uninspected}
lint report item  -arg {reason=VHDL keyword}  -arg module=param_mux  -arg name=IN  -arg file=Paramtrized_mux.v  -check {reserved_keyword} -status {uninspected}
lint report item  -arg count=118  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
```

```
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {condition_const} -rtl_id {8636a513_00200} -status
{uninspected}
lint report item  -arg module=DSP48A1  -arg port=CARRYIN  -arg file=Desgin.v  -check {unloaded_input_port} -status
{uninspected}
lint report item  -arg module=param_mux  -arg port=CEN  -arg file=Paramtrized_mux.v  -check {unloaded_input_port} -status
{uninspected}
lint report item  -arg parameter=RSTTYPE  -arg count=2  -arg module1=DSP48A1  -arg module2=param_mux  -arg file1=Desgin.v
 -arg file2=Paramtrized_mux.v  -check {parameter_name_duplicate} -status {uninspected}
lint report item  -arg {reason=VHDL keyword}  -arg module=param_mux  -arg name=OUT  -arg file=Paramtrized_mux.v  -check
{reserved_keyword} -status {uninspected}
lint report item  -arg count=155  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg count=145  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}
lint report item  -arg genblock=if  -arg module=param_mux  -arg file=Paramtrized_mux.v  -check {gen_label_missing} -status
{uninspected}
lint report item  -arg {reason=Case variant of verilog keyword}  -arg module=param_mux  -arg name=REG  -arg
file=Paramtrized_mux.v  -check {reserved_keyword} -status {uninspected}
lint report item  -arg module=param_mux  -arg port=CLK  -arg file=Paramtrized_mux.v  -check {unloaded_input_port} -status
{uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {conditional_operator_nested} -status {uninspected}
lint report item  -arg module=DSP48A1  -arg file=Desgin.v  -check {condition_const} -rtl_id {fa5870fb_00200} -status
{uninspected}
lint report item  -arg module=param_mux  -arg file=Paramtrized_mux.v  -check {multi_ports_in_single_line} -status
{uninspected}
lint report item  -arg module=DSP48A1  -arg port=BCIN  -arg file=Desgin.v  -check {unloaded_input_port} -status
{uninspected}
lint report item  -arg count=114  -arg limit=110  -arg file=Desgin.v  -check {line_char_large} -status {uninspected}

# Completed writing status commands
# ================================================================================
```