EDA PROJECT 3

CSE-215

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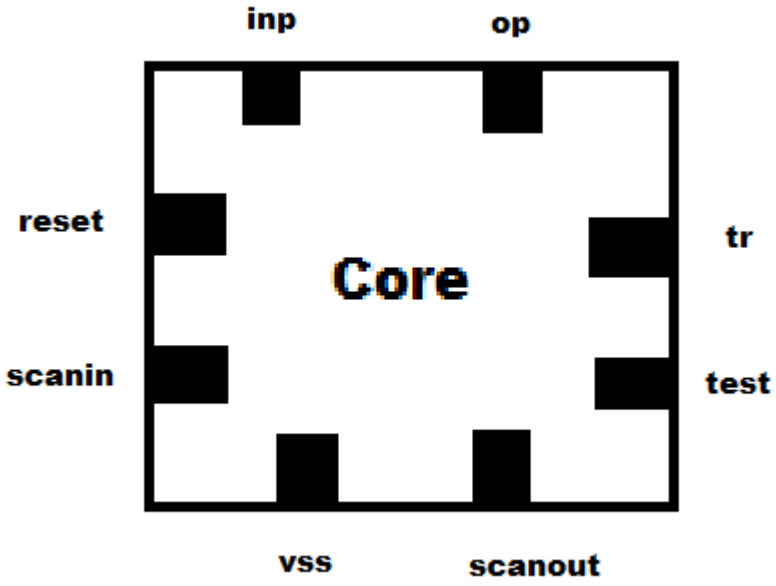
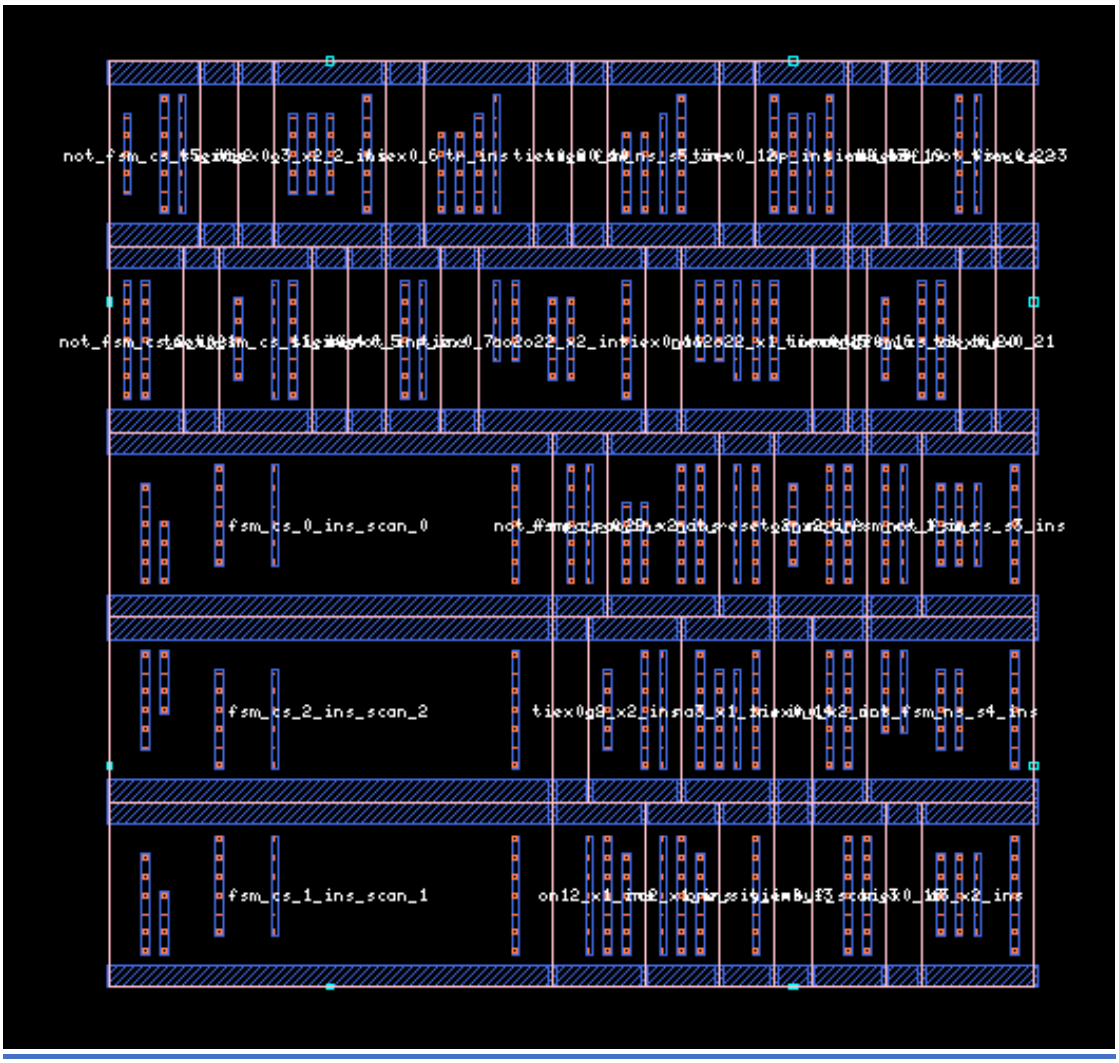
Introduction:

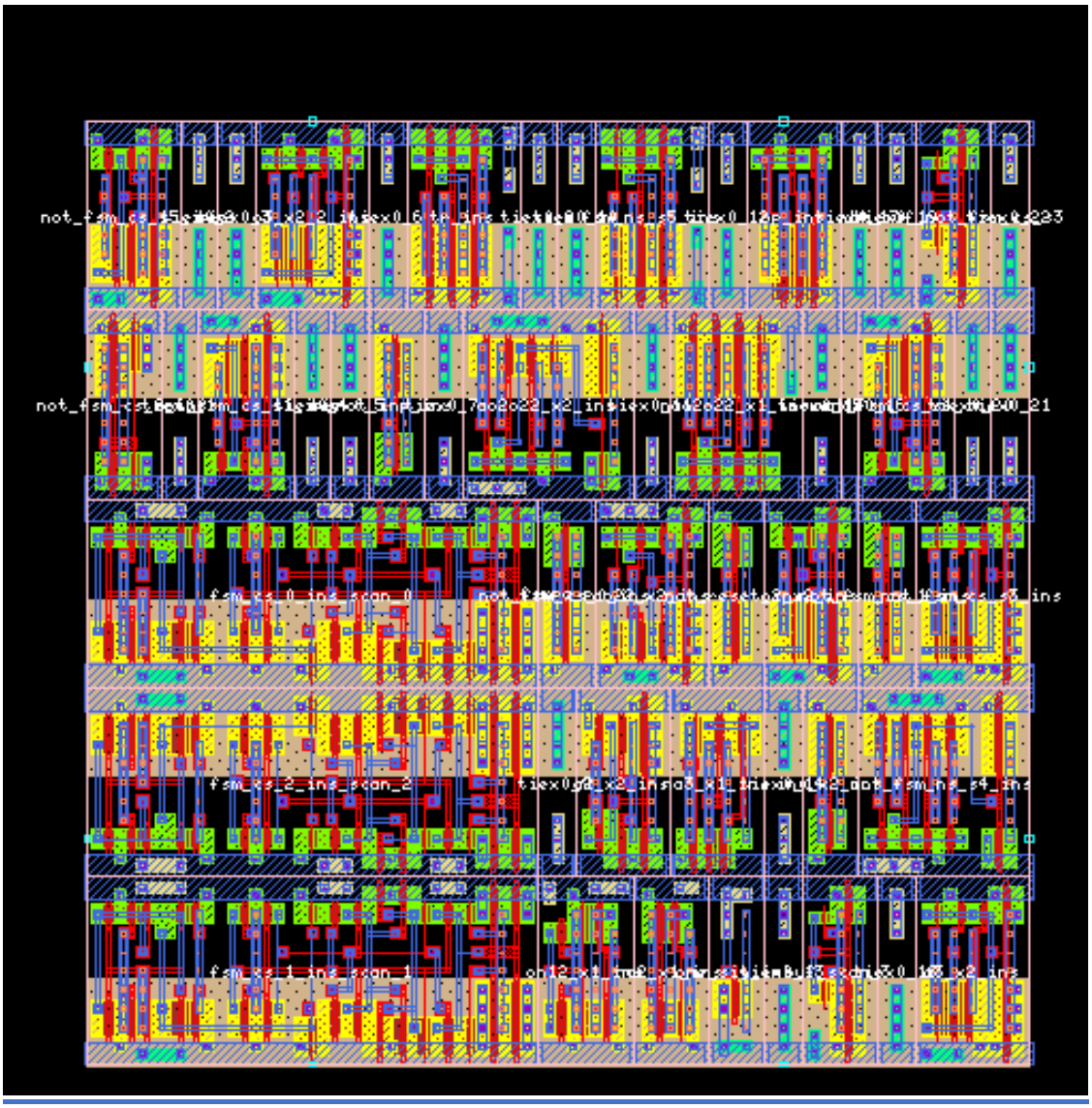
In this phase of our project we'll finish our chip design. Completing on Part 1&2 of the project where we obtained our Finite State Machine, and chose which encoding we're going to complete our project with, which was encoding "a". In this part we'll start Placement and Routing of our chip

Floor Planning:

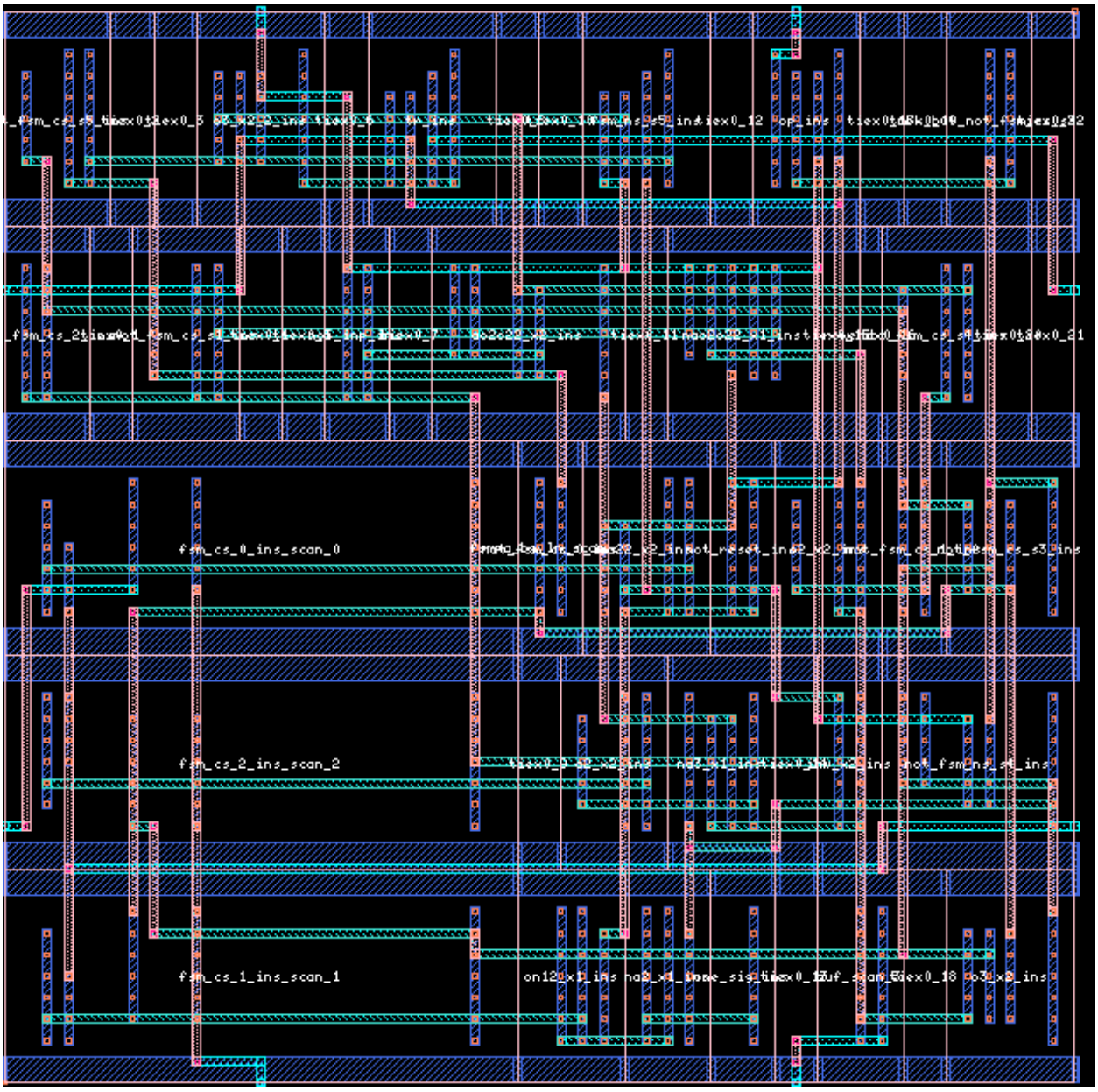


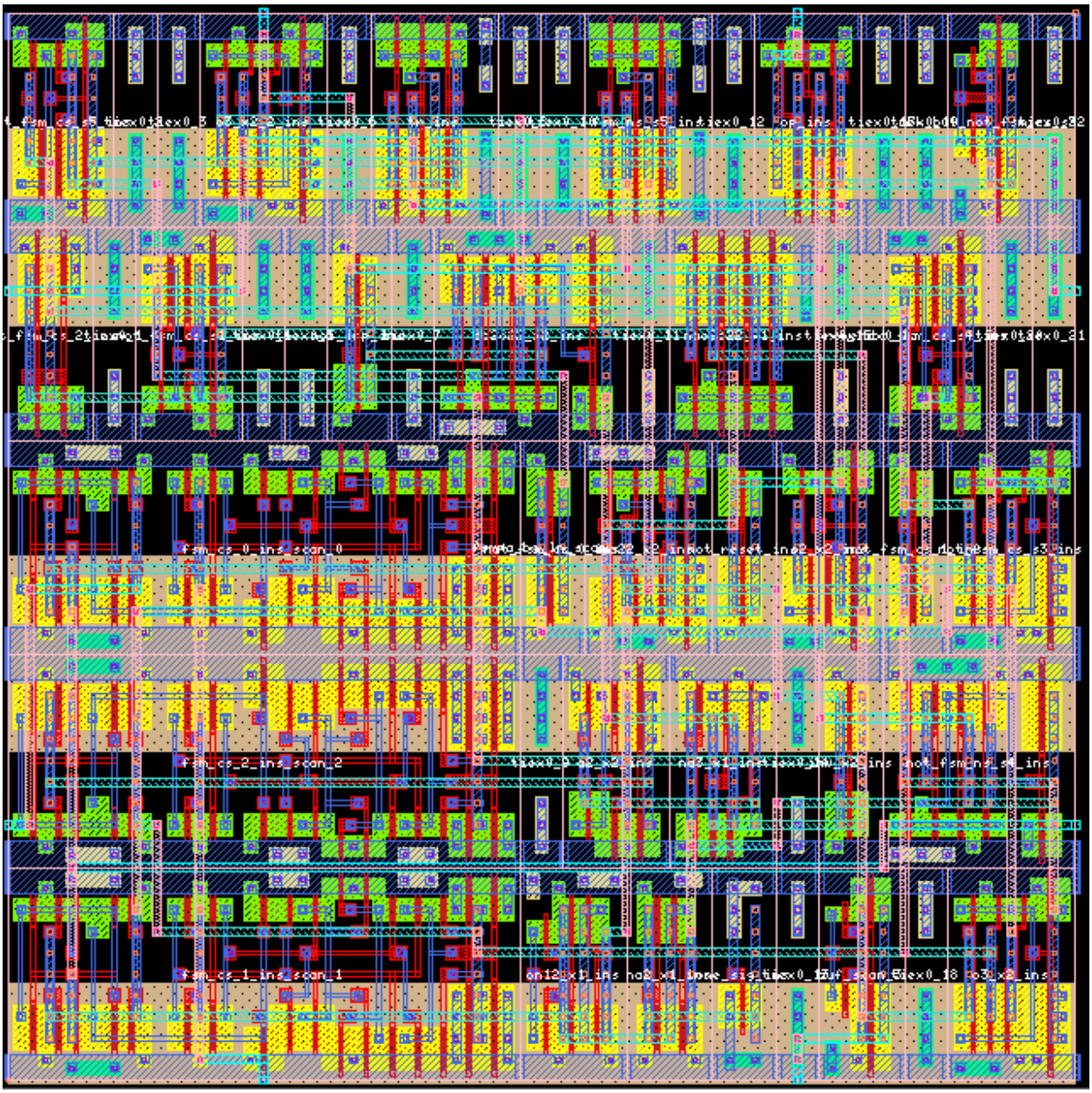
OCP graal result:





NERO graal result:





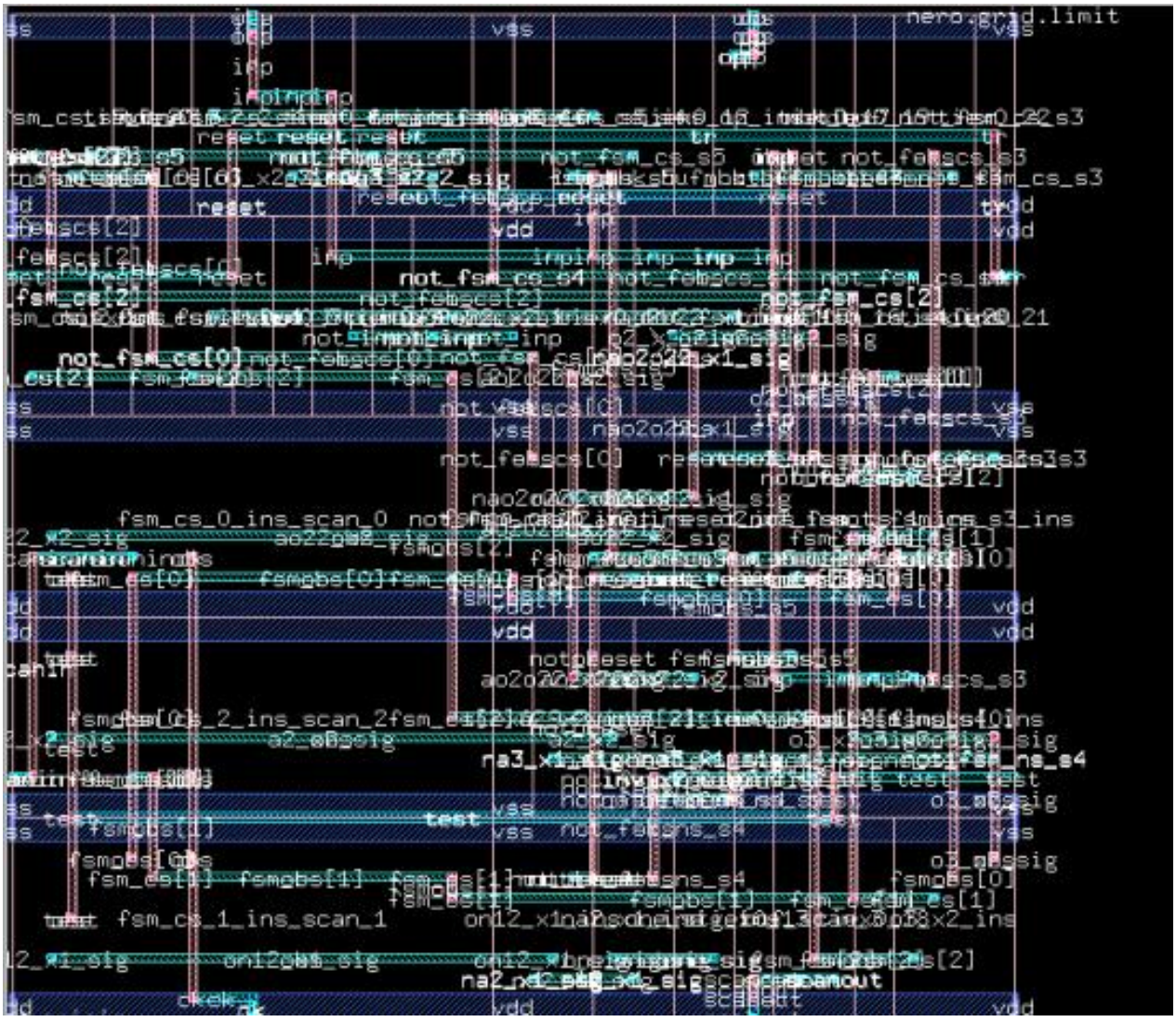
lvx result:

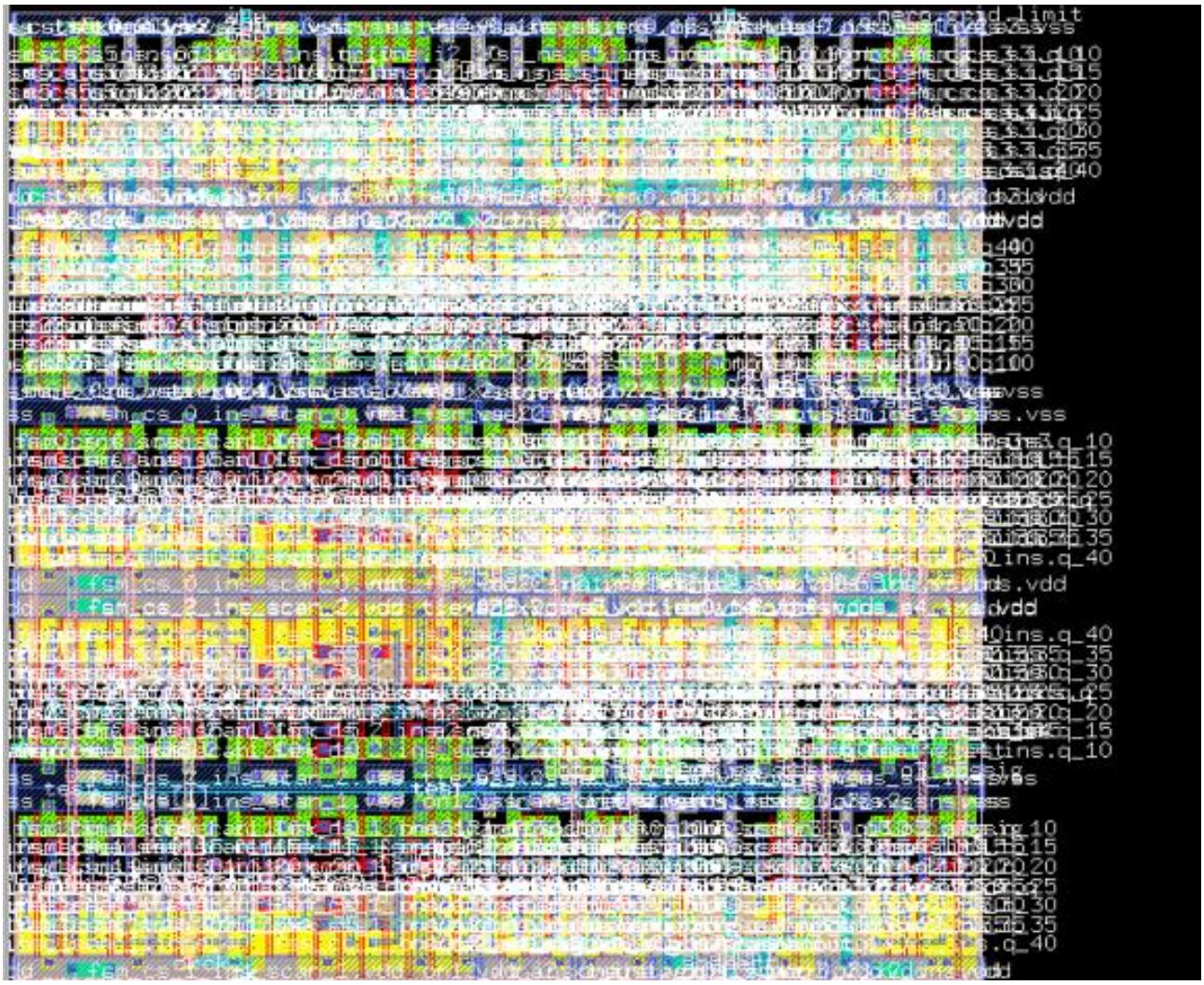
```
***** Compare Terminals .............
***** O.K.      (0 sec)

***** Compare Instances ..........
***** O.K.      (0 sec)

***** Compare Connections .............
***** O.K.      (0 sec)
```

dreal result:





Appendix:

Makefile:

```
#-------fsm----------------------------------------#

all: fsmpa.vbe \
     fsmpj.vbe \
     fsmpm.vbe \
     fsmpo.vbe \
     fsmpr.vbe
            @echo "<-- Generated"
#-------syf_boom-----------------------------------------#
syf_boom: fsmpa_bm.vbe \
           fsmpj_bm.vbe \
           fsmpm_bm.vbe \
         fsmpo_bm.vbe \
           fsmpr_bm.vbe
            @echo "<-- Generated"
#-------syf_boog-----------------------------------------#
syf_boog: fsmpa_bg.vst \
           fsmpj_bg.vst \
           fsmpm_bg.vst \
         fsmpo_bg.vst \
```

```
            fsmpr_bg.vst
               @echo "<-- Generated"
#-------syf_loon-----------------------------------------#
syf_loon: fsmpa_bg_ln.vst \
            fsmpj_bg_ln.vst \
            fsmpm_bg_ln.vst \
          fsmpo_bg_ln.vst \
            fsmpr_bg_ln.vst
               @echo "<-- Generated"
#-------proof--------------------------------------------#
proof: fsmpa_bg_ln_net.vbe
               @echo "<-- Generated"
#-------ac_scapin_registers------------------------------------------#
DFT: fsmpa_bg_ln_scan.vst
               @echo "<-- Generated"

#-------Finite State Machine Synthesis-----------------#

vhd_to_fsm:
          rename .vhd .fsm *.vhd

fsmpa.vbe: fsmp.fsm
          @echo "    Encoding Synthesis -> fsma.vbe"
          syf -CEV -a fsmp
```

```
fsmpj.vbe: fsmp.fsm
	@echo "    Encoding Synthesis  -> fsmj.vbe"
	syf -CEV -j fsmp

fsmpm.vbe: fsmp.fsm
	@echo "    Encoding Synthesis  -> fsmm.vbe"
	syf -CEV -m fsmp

fsmpo.vbe: fsmp.fsm
	@echo "    Encoding Synthesis  -> fsmo.vbe"
	syf -CEV -o fsmp

fsmpr.vbe: fsmp.fsm
	@echo "    Encoding Synthesis  -> fsmr.vbe"
	syf -CEV -r fsmp

runall: fsmpa.vbe fsmpj.vbe fsmpm.vbe fsmpo.vbe fsmpr.vbe

#-------Boom-----------------------------------------#
%_bm.vbe : %.vbe
	@echo "    Boolean Optimization -> $@"
	boom -V -d 50 $* $*_bm > $*_boom.out
#-------Boog-----------------------------------------#
%_bg.vst: %.vbe paramfile.lax
	@echo "    Logical Synthesis -> $@"
```

```
	boog -x 1 -l paramfile $* $*_bg > $*_boog.out
#-------loon-----------------------------------------#
%_ln.vst: %.vst paramfile.lax
	@echo "    Netlist Optimization -> $@"
	loon -x 1 -l paramfile $* $*_ln > $*_loon.out
#-------proof----------------------------------------#
%_bg_ln_net.vbe: %_bg_ln.vst %.vbe
	@echo "    FormalCecking -> $@"
	flatbeh $*_bg_ln $*_bg_ln_net> $*_flatbeh.out
	proof -d $* $*_bg_ln_net > $*_proof.out
#-------DFT------------------------------------------#
%_scan.vst: %.vst scan.path
	@echo "    scan-path insertion -> $@"
	scapin -VRB $* scan $*_scan > scapin.out
#-------OCP------------------------------------------#
%_p.ap:pinorder.ioc %_bg_ln_scan.vst
	@echo " ---> placement $*_p.ap"
	MBK_IN_LO=vst; export MBK_IN_LO; \
	MBK_OUT_PH=ap; export MBK_OUT_PH; \
	ocp -v -ring -ioc pinorder $*_bg_ln_scan $*_p > $*_p.out
#-------placementgraal-------------------------------#
placement_graal:
	RDS_TECHO_NAME=./techno/techno-symb.rds; \
	export RDS_TECHO_NAME; \
	graal -l fsmpa_p
```

```
	@echo "<-- Placement_graal"
#-------NERO----------------------------------------#
%_bg_ln_scan.ap: %_p.ap %_bg_ln_scan.vst
	@echo "    Routing -> $@"
	MBK_IN_LO=vst; export MBK_IN_LO; \
	MBK_IN_PH=ap; export MBK_IN_PH; \
	MBK_OUT_PH=ap; export MBK_OUT_PH; \
	nero -V -p $*_p $*_bg_ln_scan $*_bg_ln_scan  > $*_bg_ln_scan_nero.out
	@echo "    generated -> $@"
routing_graal:
	RDS_TECHO_NAME=./techno/techno-symb.rds; \
	export RDS_TECHO_NAME; \
	graal -l fsmpa_bg_ln_scan
	@echo "<-- routing_graal"
#-------cougar & lvx----------------------------------------#
%.al: %.ap
	MBK_IN_PH=ap; export MBK_IN_PH; \
	MBK_OUT_LO=al; export MBK_OUT_LO; \
	RDS_TECHO_NAME=./techno/techno-035.rds; \
	export RDS_TECHO_NAME; \
	cougar -v $* > $*_co.out
	lvx vst al $* $* -f > $*_lvx.out
#----------druc----------------------------------------#
druc_core: fsmpa_bg_ln_scan.ap
	MBK_IN_PH=ap; export MBK_IN_PH; \
```

```
	RDS_OUT=cif; export RDS_OUT; \
	RDS_TECHO_NAME=./techno/techno-symb.rds; \
	export RDS_TECHO_NAME; \
	druc fsmpa_bg_ln_scan > fsmpa_bg_ln_scan_druc.out
#------------s2r-------------------------------#
fsmpa_chip.cif: fsmpa_bg_ln_scan.ap
	@echo "    s2r -> $@"
	MBK_IN_PH=ap; export MBK_IN_PH; \
	RDS_OUT=cif; export RDS_OUT; \
	RDS_TECHO_NAME=./techno/techno-035.rds; \
	export RDS_TECHO_NAME; \
	s2r -v -r fsmpa_bg_ln_scan fsmpa_chip > fsmpa_chip_s2r.out

chip_dreal:
	RDS_IN=cif; export RDS_IN; \
	RDS_TECHNO_NAME=./techno/techno_035.rds; \
	export RDS_TECHNO_NAME; \
	dreal -l fsmpa_chip
	@echo "<-- chip_dreal done"
#-------Clean Up-----------------------------------#

clean :
	rm -f  *.vbe *.enc *~
	@echo "Erase all the files generated by the makefile"
```

Pinorder.ioc

LEFT(#IOs from bottom to top

(IOPIN scanin.0);

(IOPIN reset.0);)

TOP(#IOs from left to right

(IOPIN inp.0);

(IOPIN op.0);)

RIGHT(#IOs from bottom to top

(IOPIN test.0);

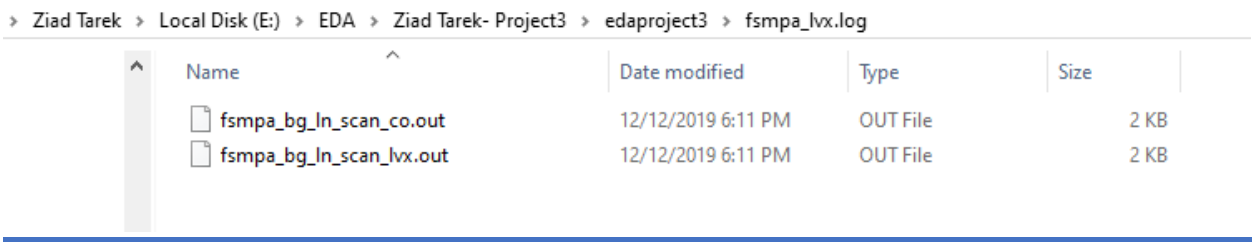
(IOPIN tr.0);)

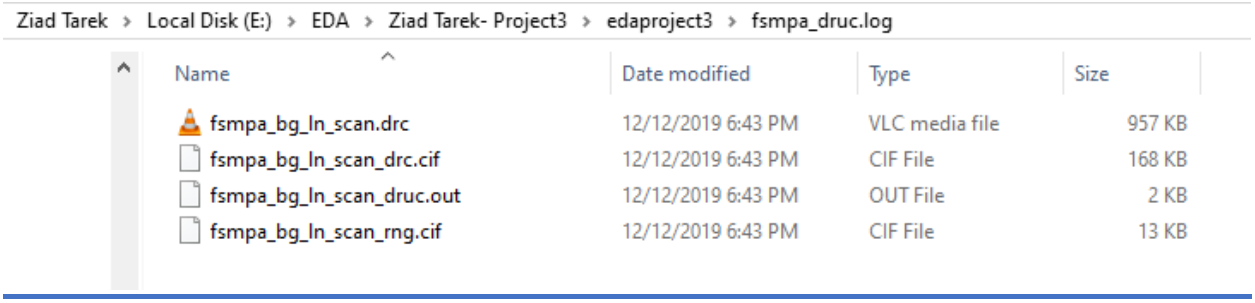
BOTTOM(#IOs from left to right

(IOPIN ck.0);

(IOPIN scanout.0);)

Log files:




Ziad Tarek › Local Disk (E:) › EDA › Ziad Tarek- Project3 › edaproject3 › fsmpa_druc.log
Name
Date modified
Type
Size
fsmpa_bg_ln_scan.drc
12/12/2019 6:43 PM
VLC media file
957 KB
fsmpa_bg_ln_scan_drc.cif
12/12/2019 6:43 PM
CIF File
168 KB
fsmpa_bg_ln_scan_druc.out
12/12/2019 6:43 PM
OUT File
2 KB
fsmpa_bg_ln_scan_rng.cif
12/12/2019 6:43 PM
CIF File
13 KB