

Implementation of SOC Pipelined RISC-V Processor (RV32I) with an APB Master interface From RTL to GDS

Ziad Ahmed

9//5//2024

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RTL To GDS
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[GitHub REPO](#)



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System Description & Overview

Description

This project involves designing and implementing a Pipelined RISC-V Processor (RV32I) integrated with an Advanced Peripheral Bus (APB) interface. The processor will feature a pipelined architecture, enhancing instruction throughput and overall performance.

Key components of the project include:

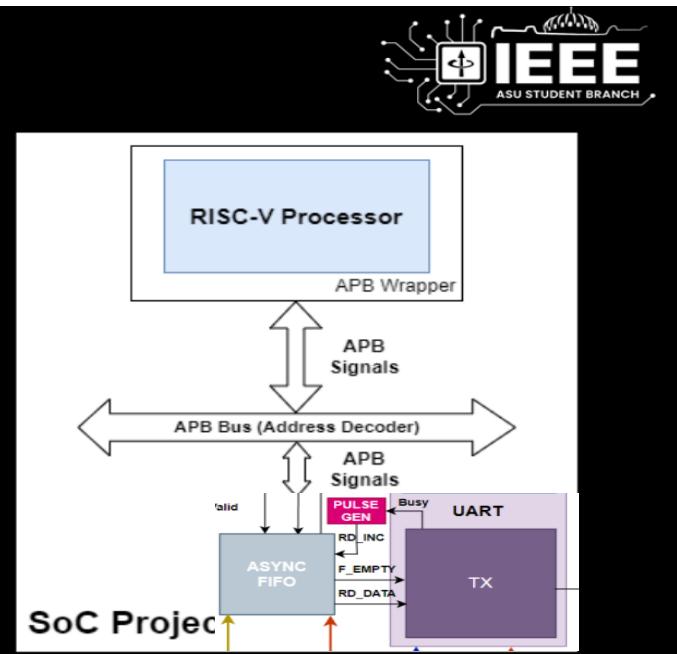
- **Pipelined RISC-V Processor (RV32I):** A 32-bit RISC-V processor with a pipelined architecture to execute multiple instructions simultaneously, improving efficiency and performance.
- **APB Master Interface:** The processor will incorporate an APB Master interface, enabling it to communicate with peripherals via the APB protocol, a widely used bus standard in embedded systems.
- **APB Address Decoder:** A custom APB address decoder will be implemented to generate the appropriate PSEL (Peripheral Select) signals for each connected peripheral based on the address, ensuring correct data routing.
- **Asynchronous FIFO:** to avoid Data loss caused by CDC
- **UART with APB Slave Interface:** The project also includes the design of a Universal Asynchronous Receiver-Transmitter (UART) with an APB Slave interface and register layering, facilitating serial communication between the processor and external devices.

This comprehensive project demonstrates proficiency in processor design, bus interfacing, and peripheral integration, crucial for modern embedded systems.

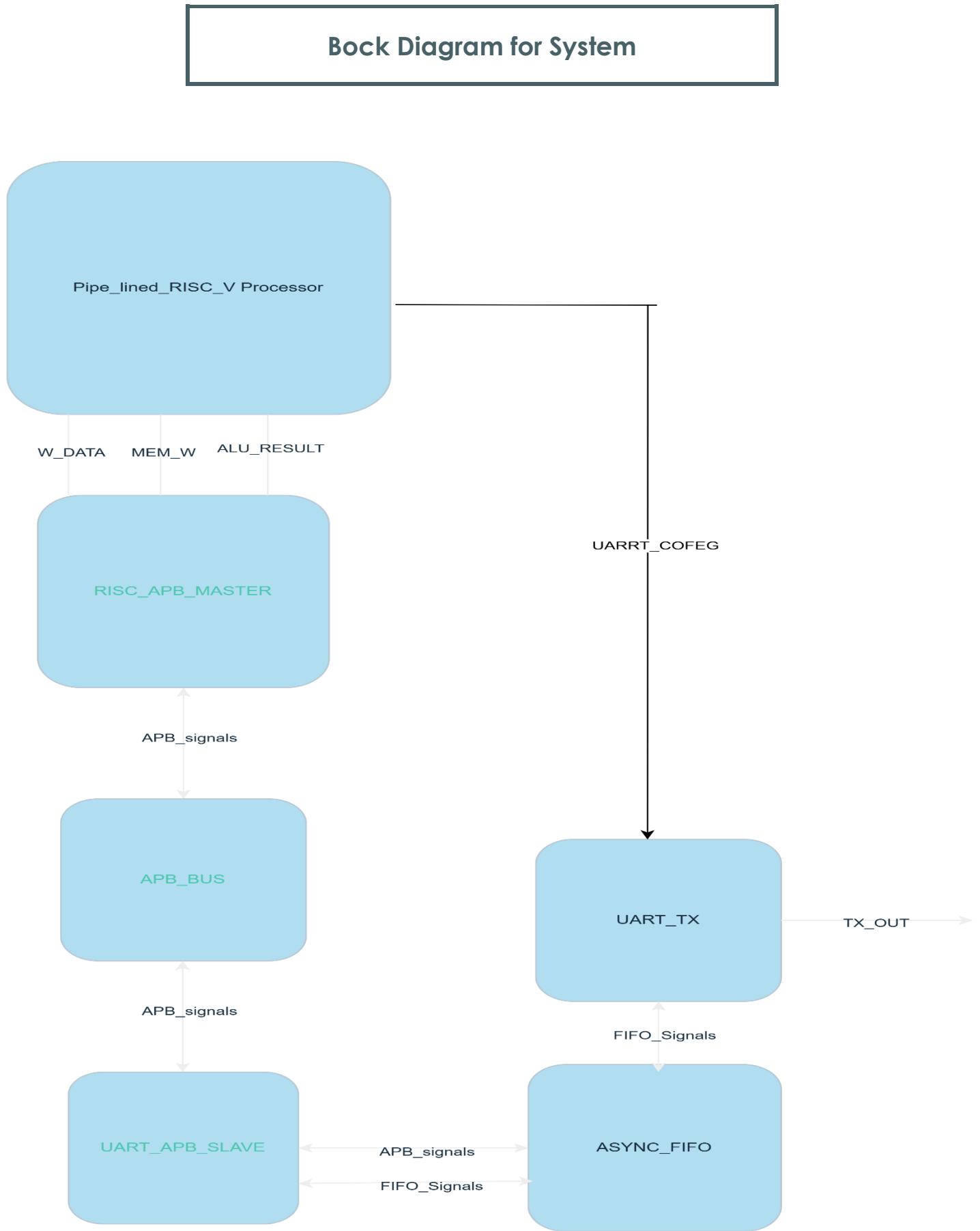
Final Project

Your Final Project in this workshop will consist of:

- A Pipelined RISC-V Processor (RV32I), with an APB Master interface.
- An APB Address Decoder (Generates the correct PSEL signal to each peripheral based on address).
- A UART with an APB Slave interface and Register Layering.

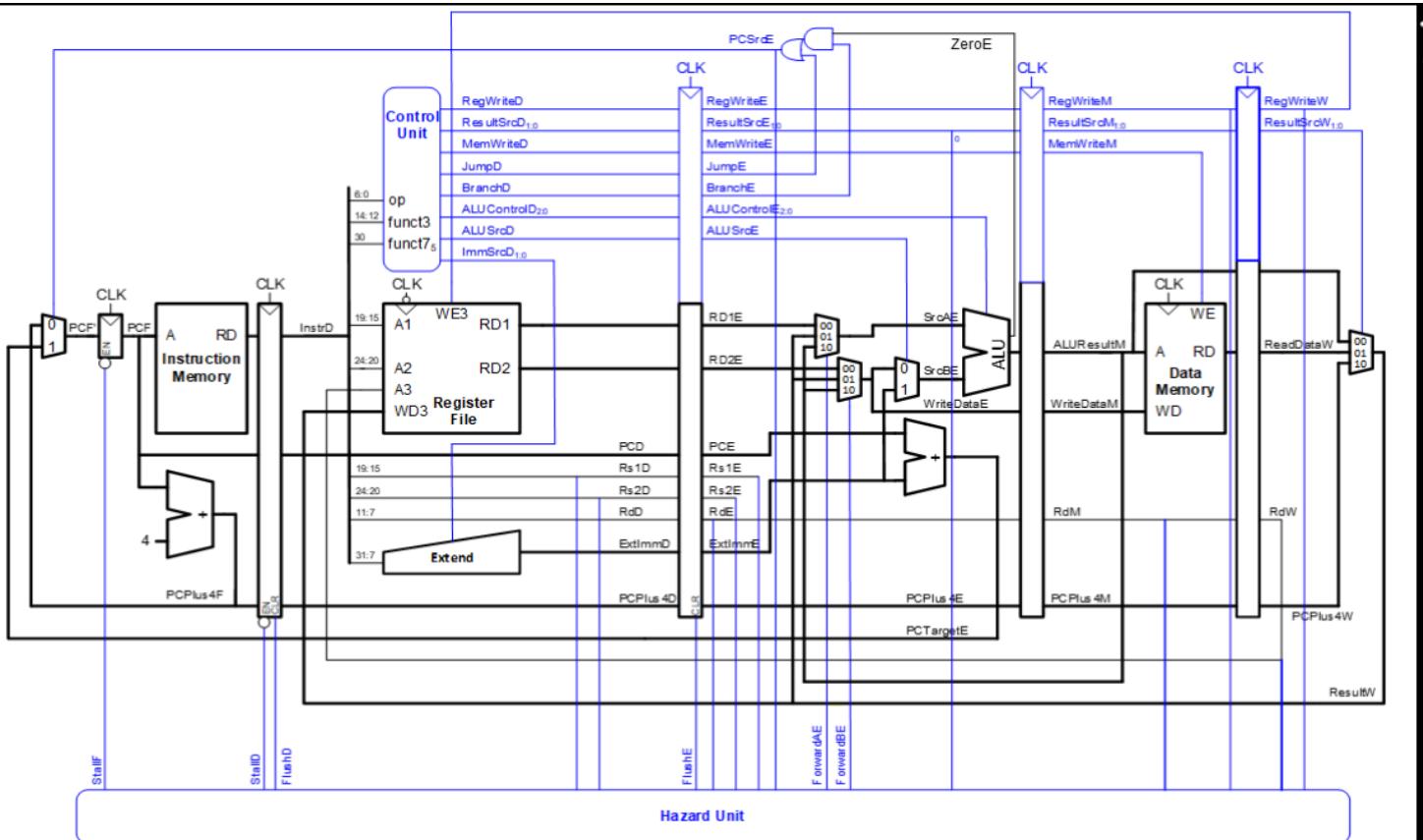


Block diagrams

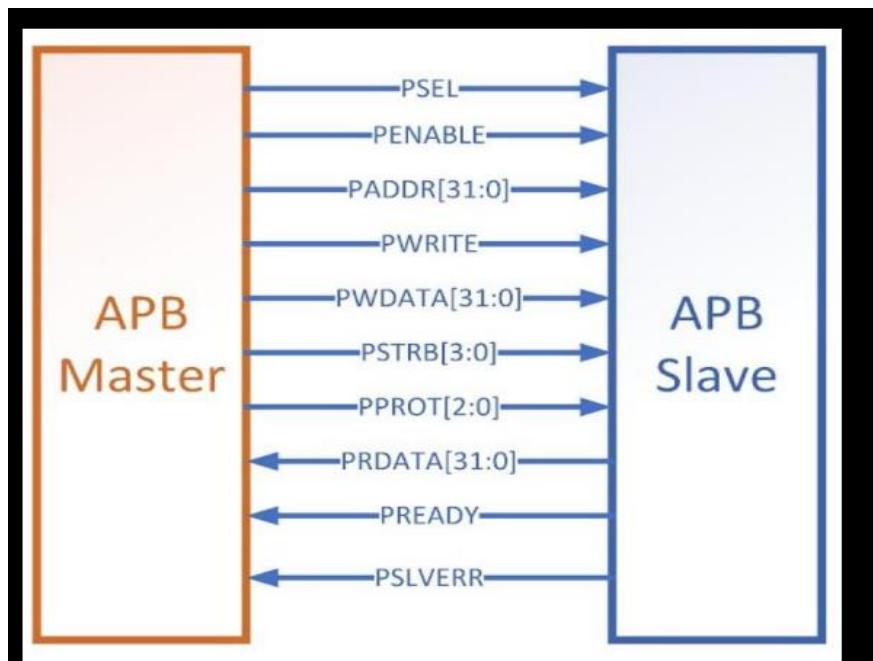


Detailed Block Diagram for each Block

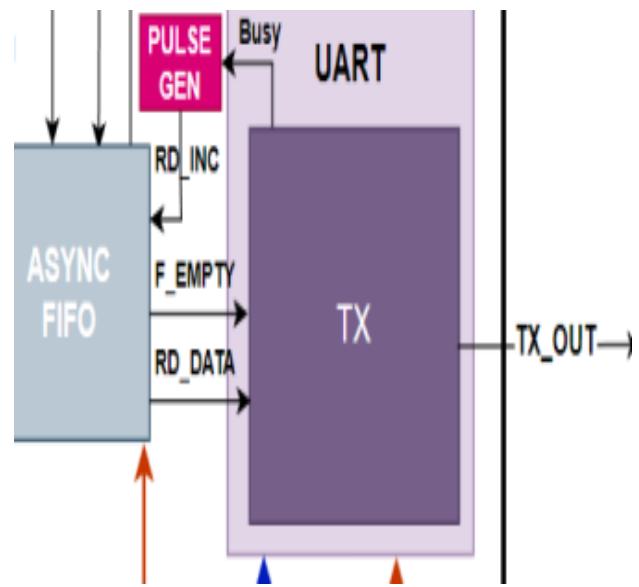
RISC V Block Diagram



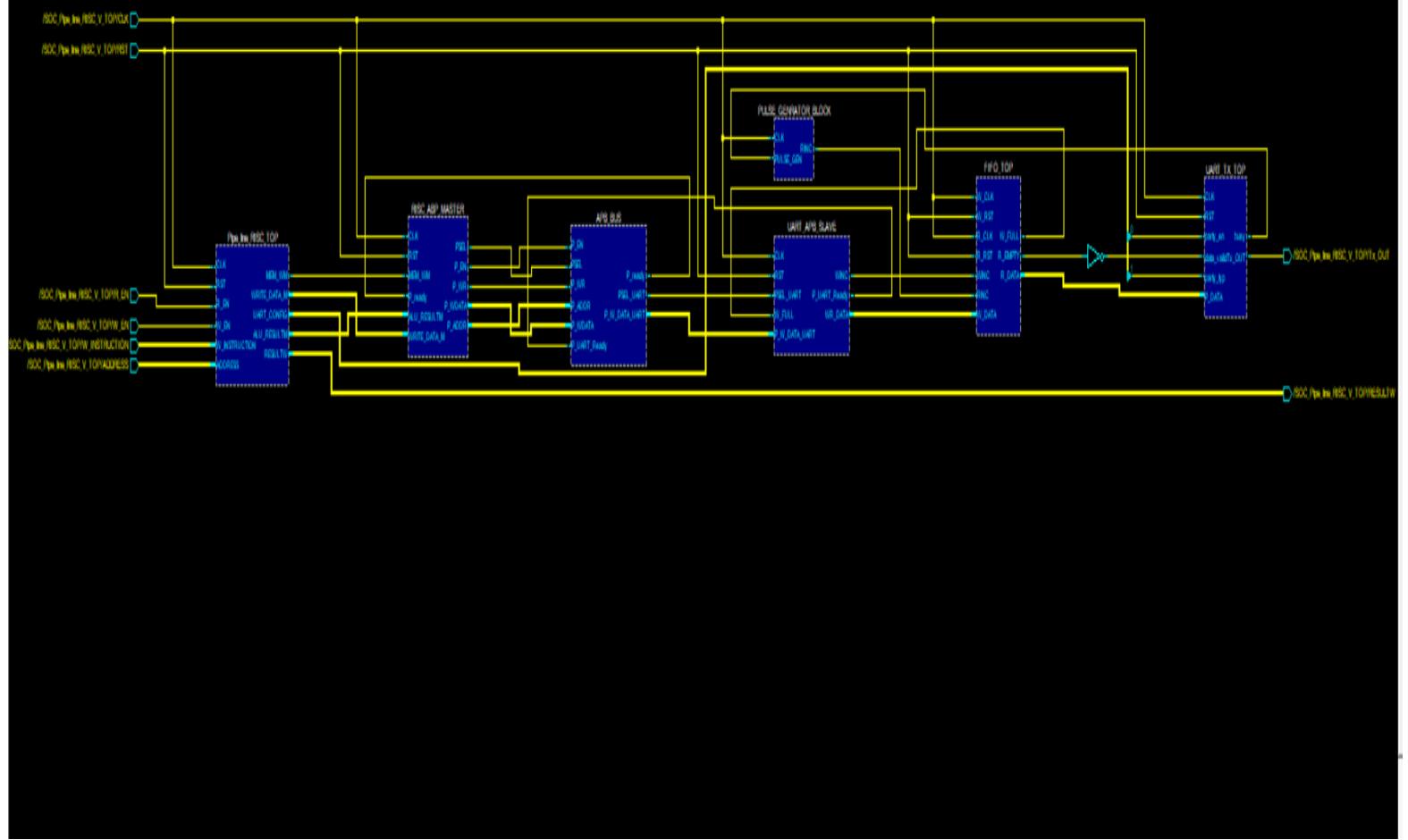
APB Block Diagram



UART & FIFO Block Diagrams



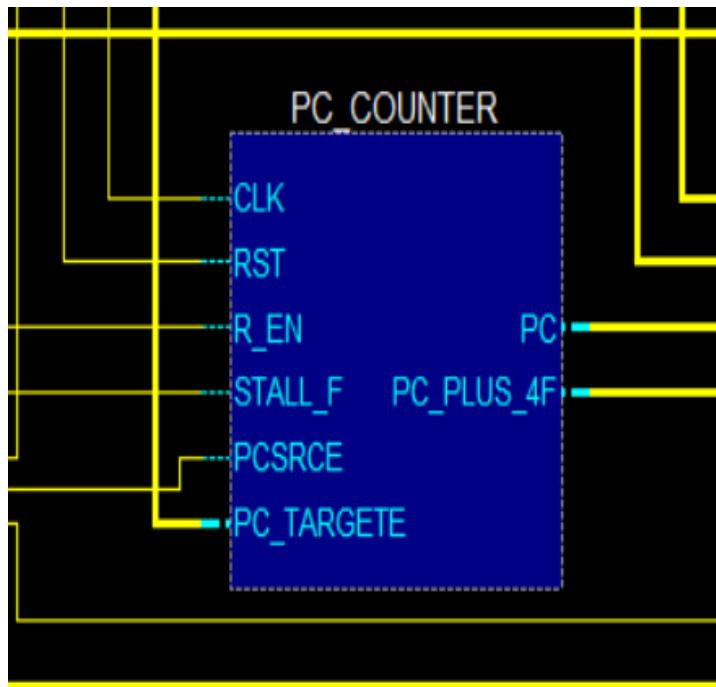
Schematic For SYSTEM after RTL phase



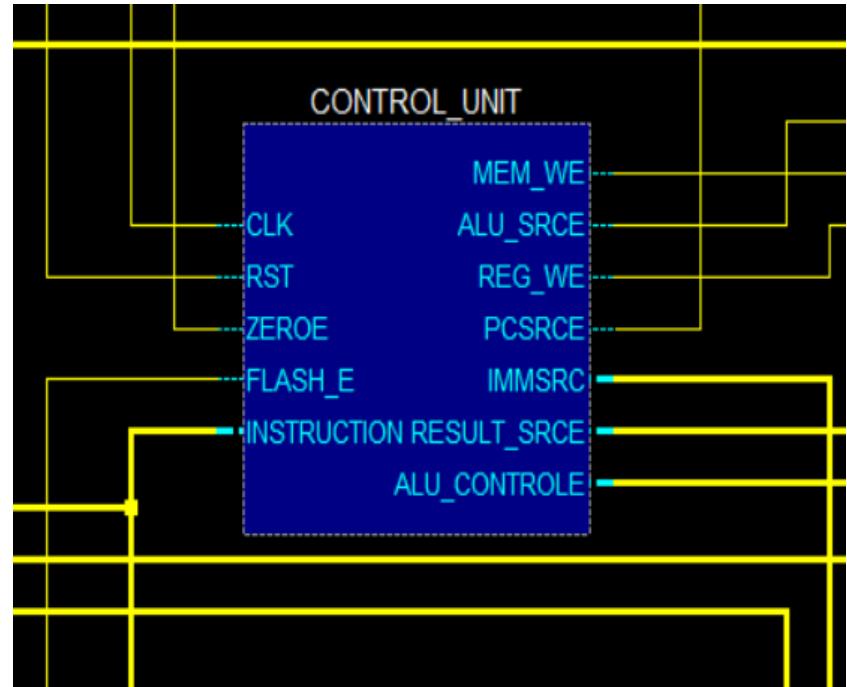
Main Blocks for The System after RTL

RISC_V Blocks

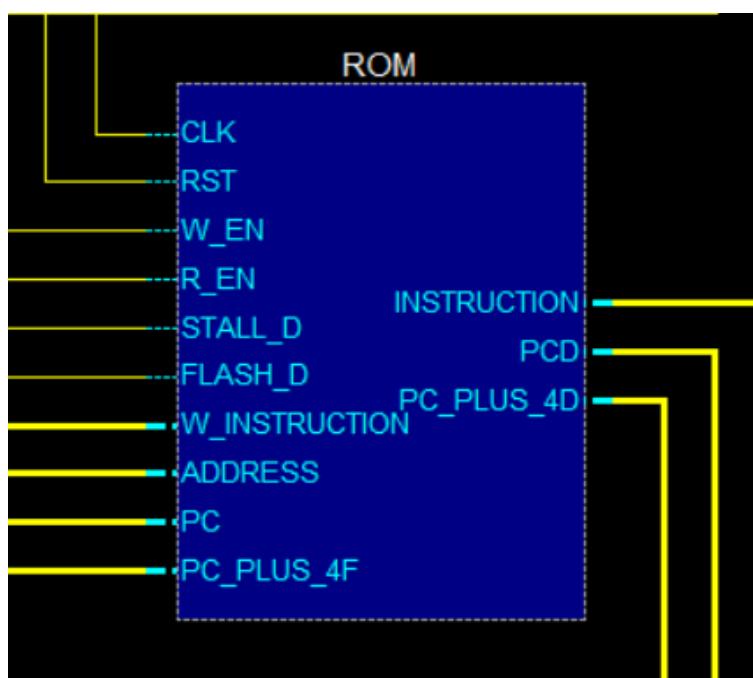
PC_Counter



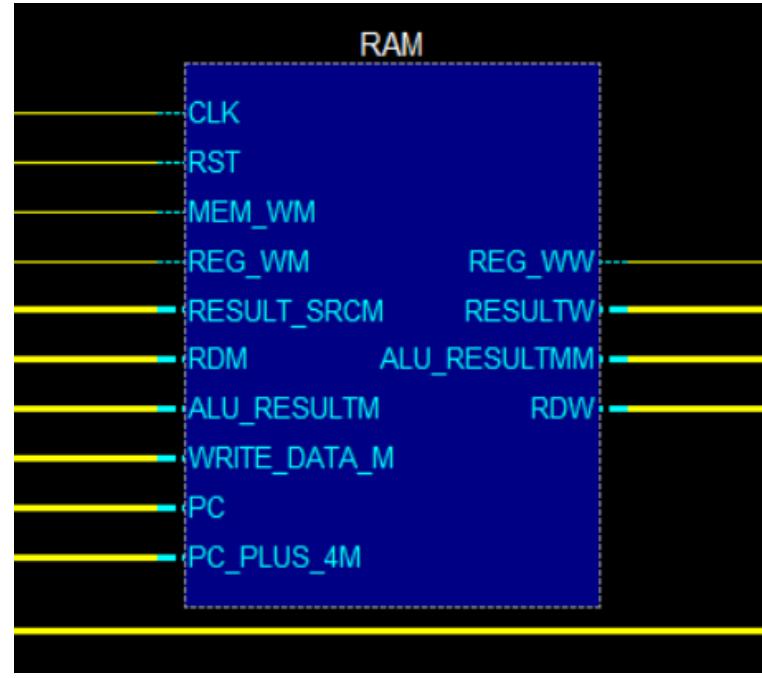
Control Unit



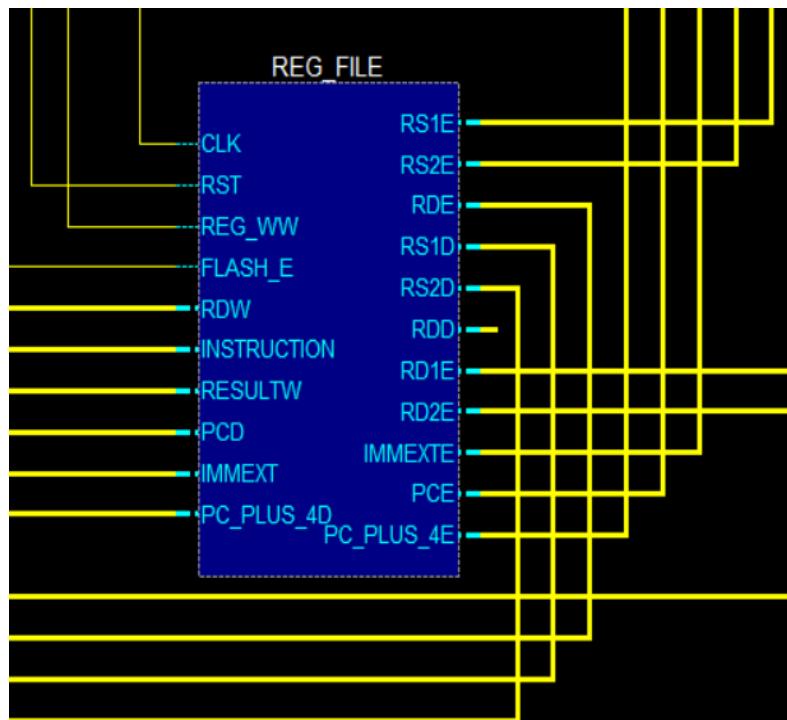
Instruction memory (ROM)



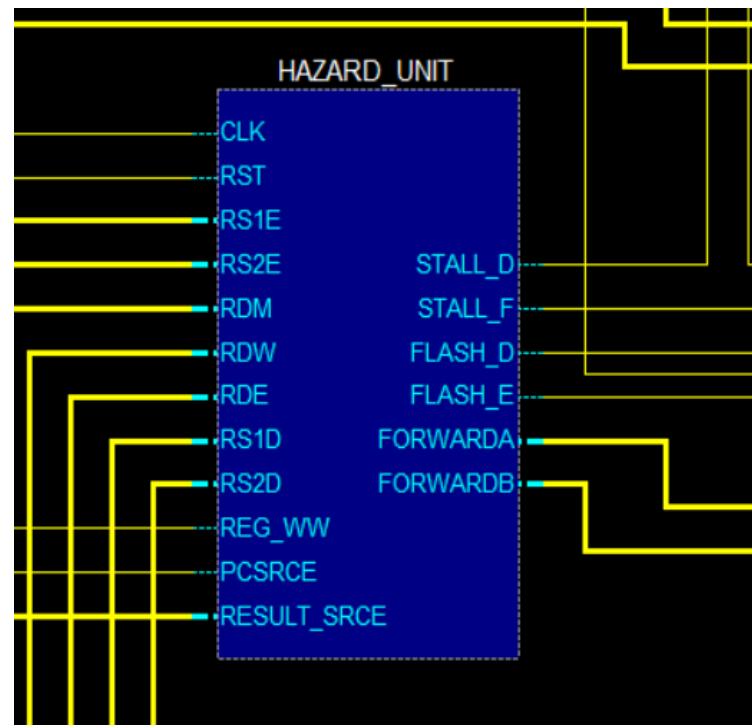
Data memory (RAM)



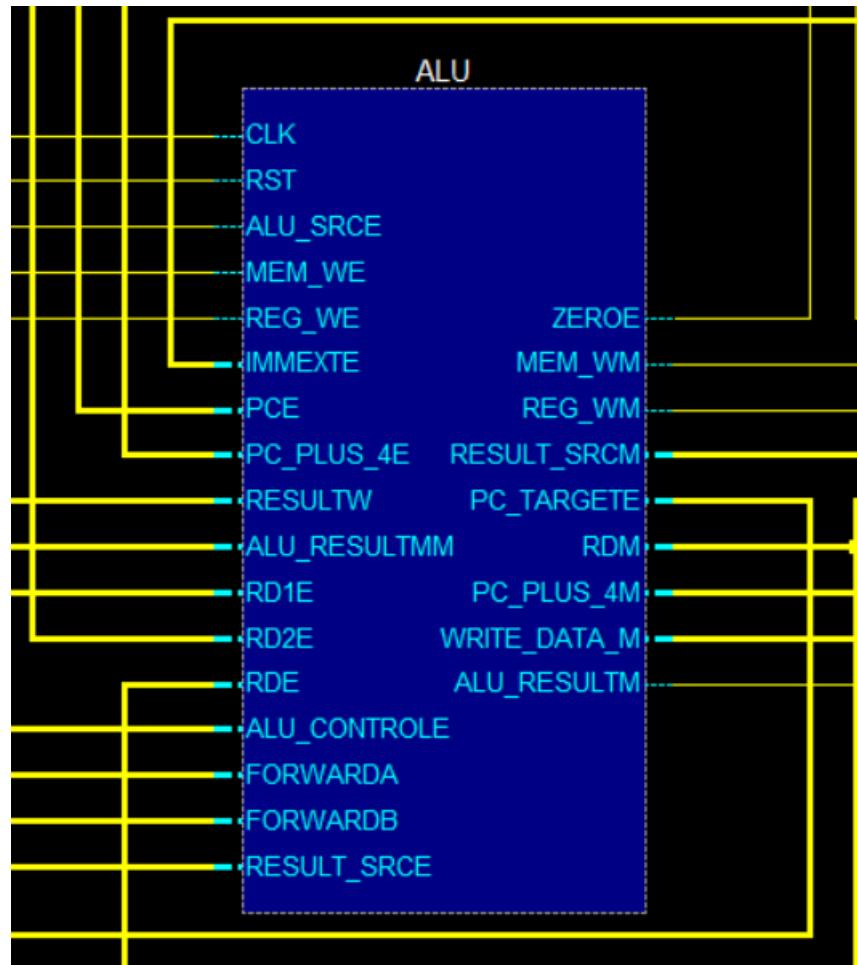
Reg_File



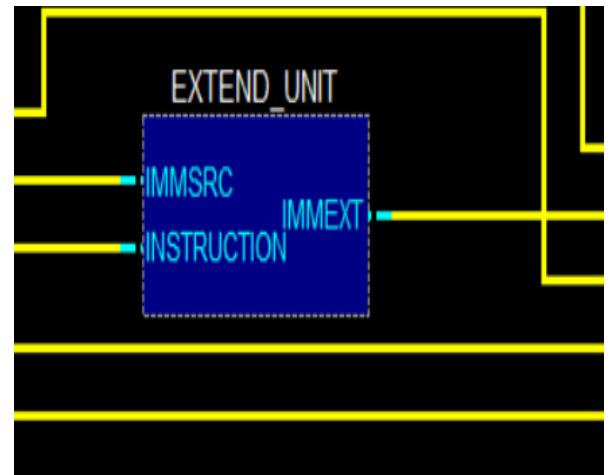
Hazard Unit



ALU

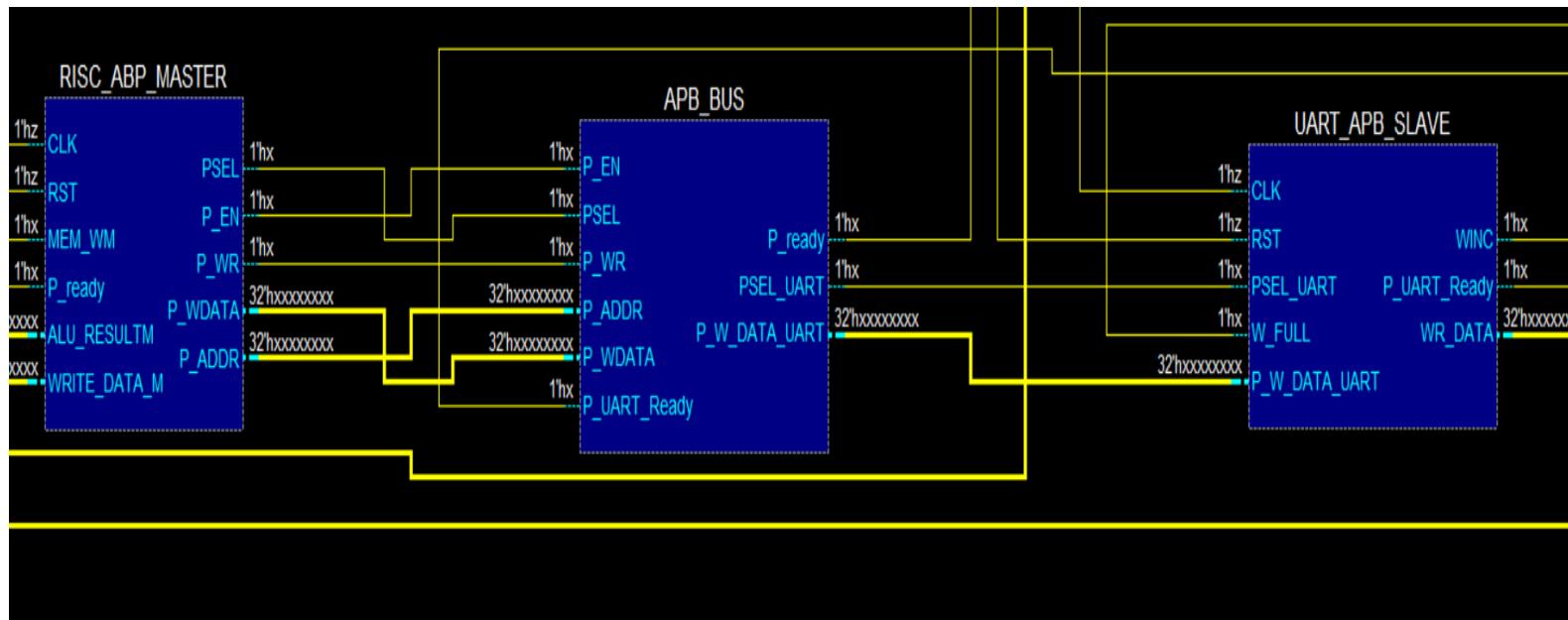


Extend Unit

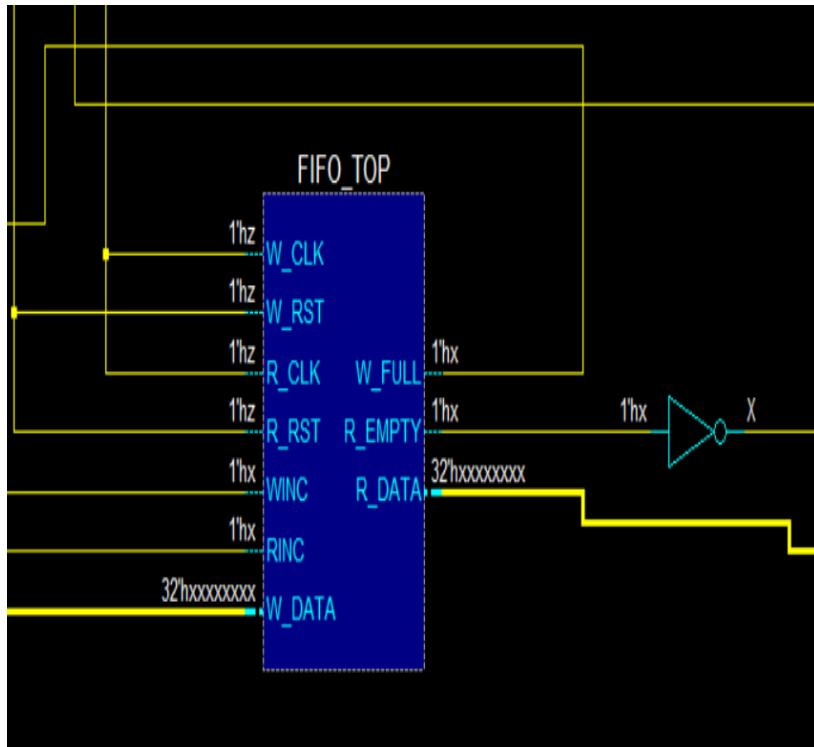


SOC Blocks

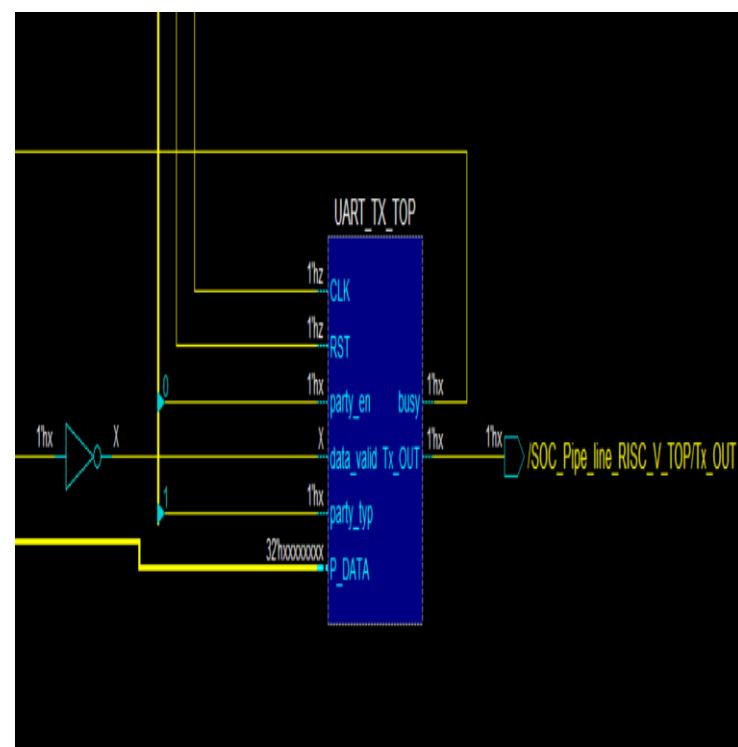
APB Blocks Master && Slave && BUS



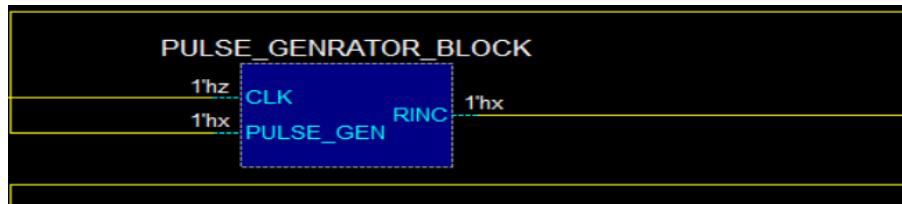
FIFO



UART_TX



Bulse Generator



Functional Verification for System

Wave forms Testing PipeLined_RISC_V Functionality

Sample assembly program

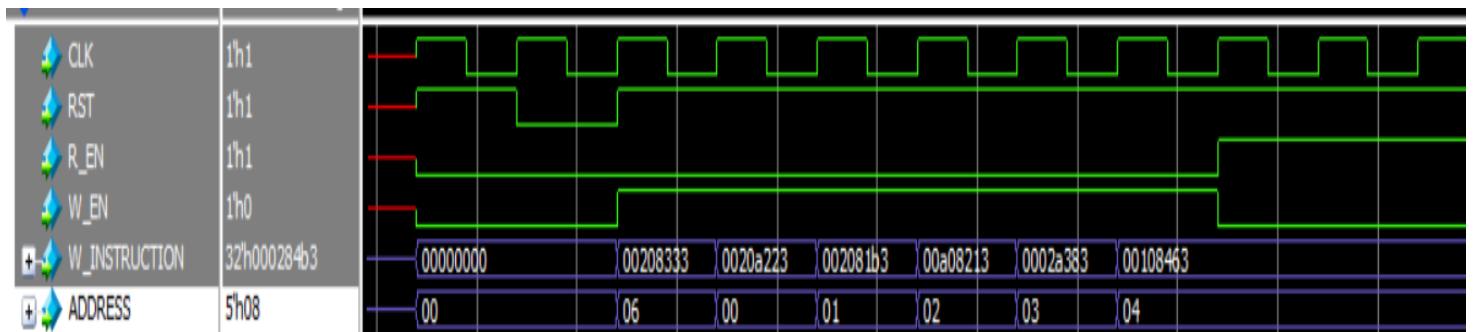
```
##### Sample assembly program #####
      ### S Format Instruction sw
0x0000_0000      sw x2, 4(x1)      ##### Machine Code == 32'b0000000000001000001010001000100011
      ### R Format Instruction ADD
0x0000_0004      add x3, x1, x2      ##### Machine Code == 32'b000000000000100000100000110110011
      ### I Format Instruction ADDI
0x0000_0008      addi x4, x1, 10      ##### Machine Code == 32'b00000000101000001000001000010011
      ### I Format Instruction lw
0x0000_000c      lw x7, 4(x1)      ##### Machine Code == 32'b0000000000000000101010001110000011
      ### B Format Instruction BEQ
0x0000_0010      beq x1, x1, label      ##### Machine Code == 32'b00000000000010000100000001100011
0x0000_0014      NOP
0x0000_0018      label      add x6, x1, x2      ##### Machine Code == 32'b000000000000100001000010001100011

##### DATA Hazard Case Loading in Reg5 and use it in the next R instruction as rs1
0x0000_0020      lw x5, 4(x1)      ##### Machine Code == 32'b0000000000000000101010001010000011
0x0000_0024      add x9, x5, x0      ##### Machine Code == 32'b0000000000000000101000010010110011
```

Transcript Snip Showing Passed Test Cases

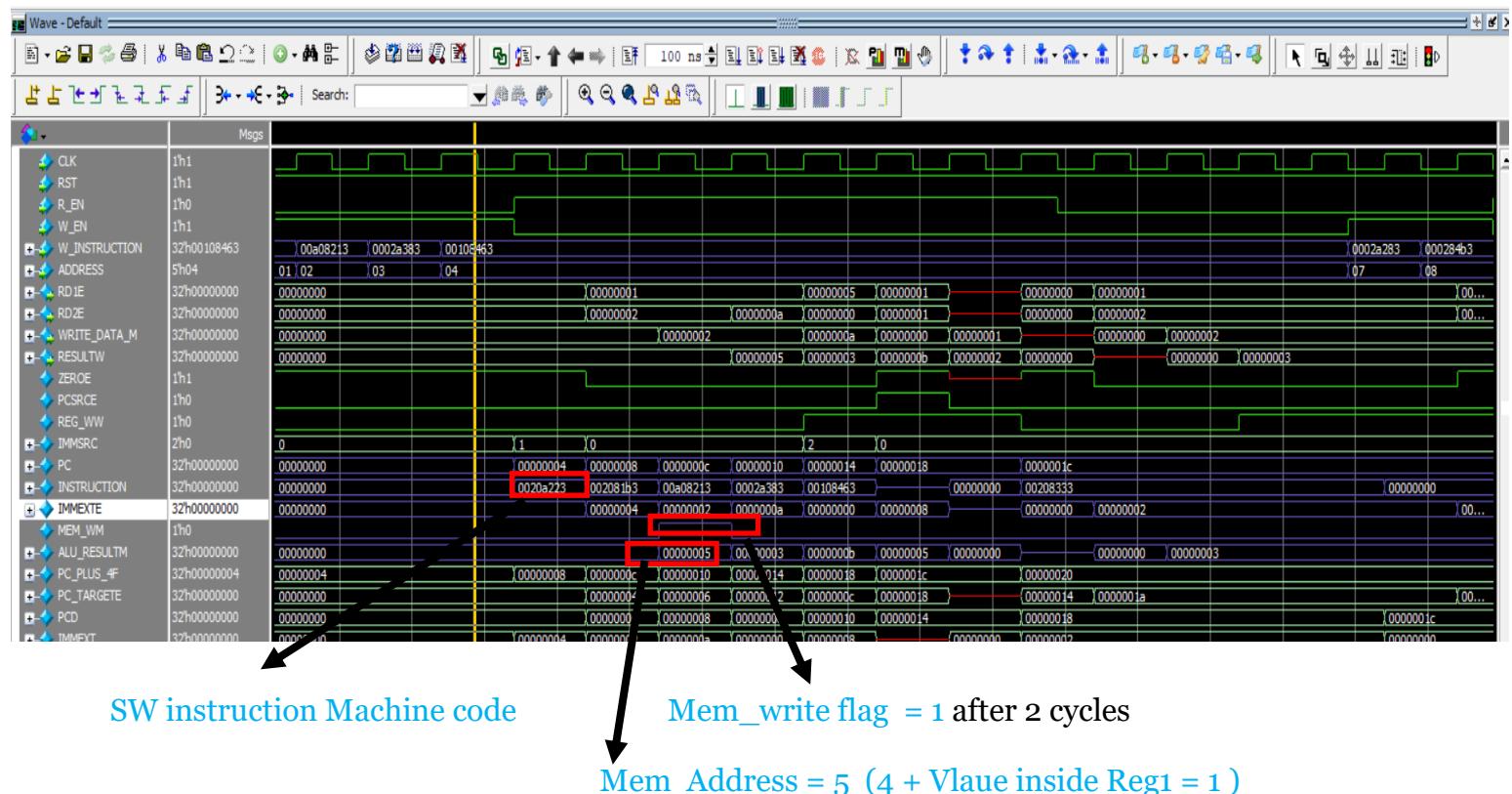
```
VSIM 117> run -all
# TESTING sw Instruction (sw x2, 4(x1)) Storing value inside REG2 = 2 into Location 5 in the Memory
# Test Case Passed and the Value stored in REG 2 =      2 at Time      130
# TESTING R Instruction Add operation (add x3, x1, x2) REG3 == 1 + 2
# Test Case Passed and the Value stored in REG 3 =      3 at Time      140
# TESTING I Instruction Addi operation (addi x4, x1, 10) REG4 == 1 + 10
# Test Case Passed and the Value stored in REG 4 =      11 at Time      150
# TESTING lw Instruction Load operation (lw x7, 4(x1)) loading From Location 5 in The Memory = 2 Into REG7
# Test Case Passed and the Value stored in REG 7 =      2 at Time      160
# TESTING BEQ Instruction (beq x1, x1, label) Branching into label which stored at PC Adress 0x00000018
# Test Case Passed and the Value For PC = 0x 00000018 at Time      170
# Test Branching at label which stored at PC Adress 0x00000018 (add x6, x1, x2) REG6 == 1 + 2
# Test Case Passed and the Value stored in REG 6 =      3 at Time      200
# TESTING lw Instruction Load operation (lw x5, 4(x1)) loading From Location 5 in The Memory = 2 Into REG5 THEN use it in next R Instruction To make Sure That DATA Hazard Won't Happen
# Test Case Passed and the Value stored in REG 5 =      2 at Time      270
# TESTING R Instruction Add operation (add x9, x5, x0) REG9 == 0 + 2
# Test Case Passed and the Value stored in REG 9 =      2 No Hazard DATA at Time      290
# ** Note: $stop : E:/Digital Projects/SOC_Pipe_line_RISC_V/SINGLE_RISC_V_TB.v(124)
#   Time: 320 ns Iteration: 0 Instance: /SINGLE_RISC_V_TB
# Break in Module SINGLE_RISC_V_TB at E:/Digital Projects/SOC_Pipe_line_RISC_V/SINGLE_RISC_V_TB.v line 124
```

Writing 5 Instructions in 5 consecutive clock cycles Pipelining

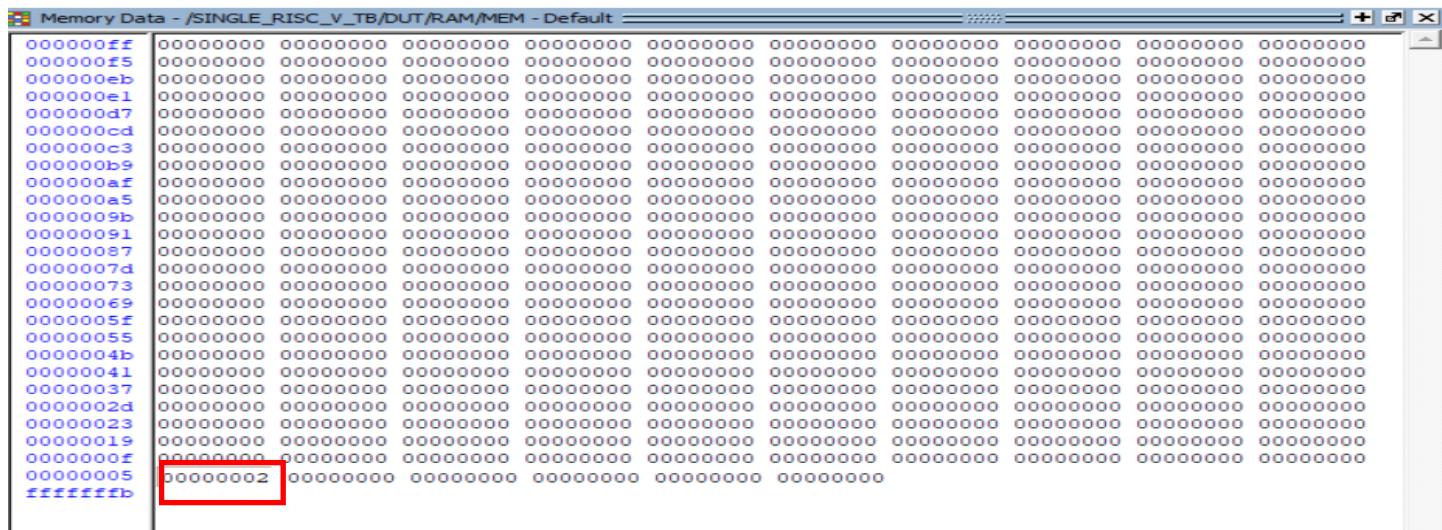


WAVE_FORM FOR SW instruction

SW x2, 4(x1)

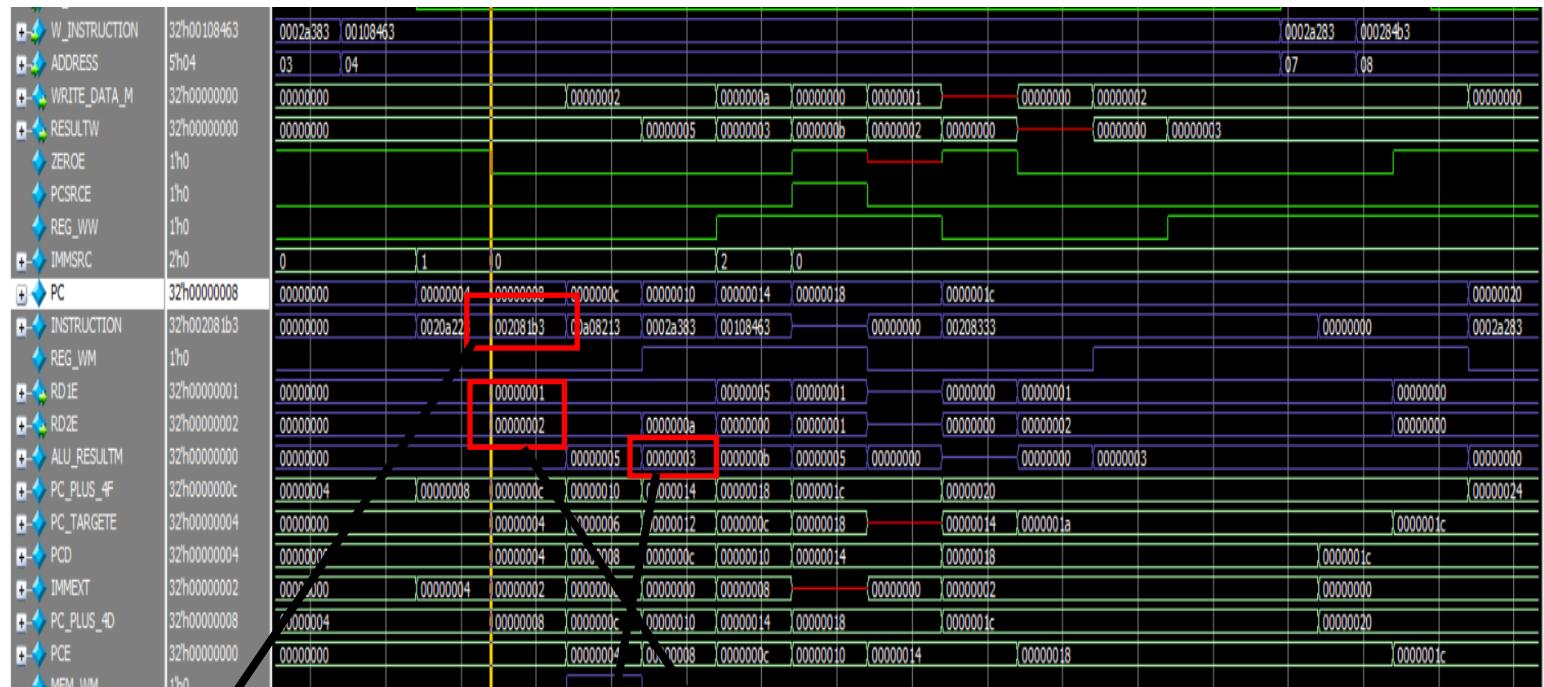


Value Stored In **location 5** In the RAM (Should = Value inside REG2 which is 2)



WAVE FORM FOR ADD instruction

add x3, x1, x2



ADD instruction Machine code

RD1E = 1 RD2E = 2 Values inside REG1®2

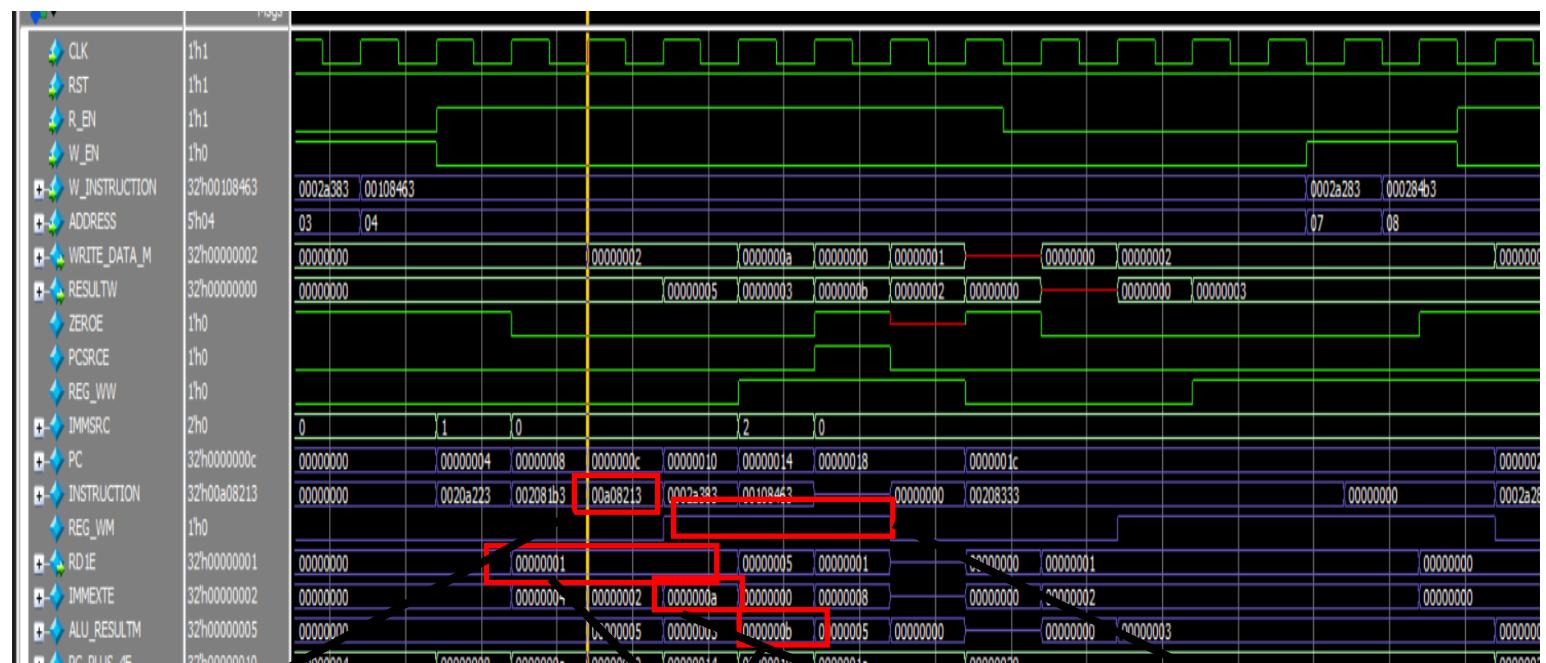
ALU Result = 3 after 2cycles from execute Add Instruction
Which will be stored In REG3

Value Stored In REG3 In the REG_FILE (Should = Value inside REG1 + REG2 = 1 + 2)

Memory Data - /SINGLE_RISC_V_TB/DUT/REG_FILE/REGESTERS - Default															
0000001f	0000001f	0000001e	0000001d	0000001c	0000001b	0000001a	00000019								
00000018	00000018	00000017	00000016	00000015	00000014	00000013	00000012								
00000011	00000011	00000010	0000000f	0000000e	0000000d	0000000c	0000000b								
0000000a	0000000a	00000009	00000008	00000002	00000006	00000005	0000000b								
00000003	00000003	00000002	00000001	00000000											
fffffffffc															

WAVE_FORM FOR ADDI instruction

addi x4, x1, 10



ADD instruction Machine code

RD1E = 1

RD2E = 2 Values inside REG1®2

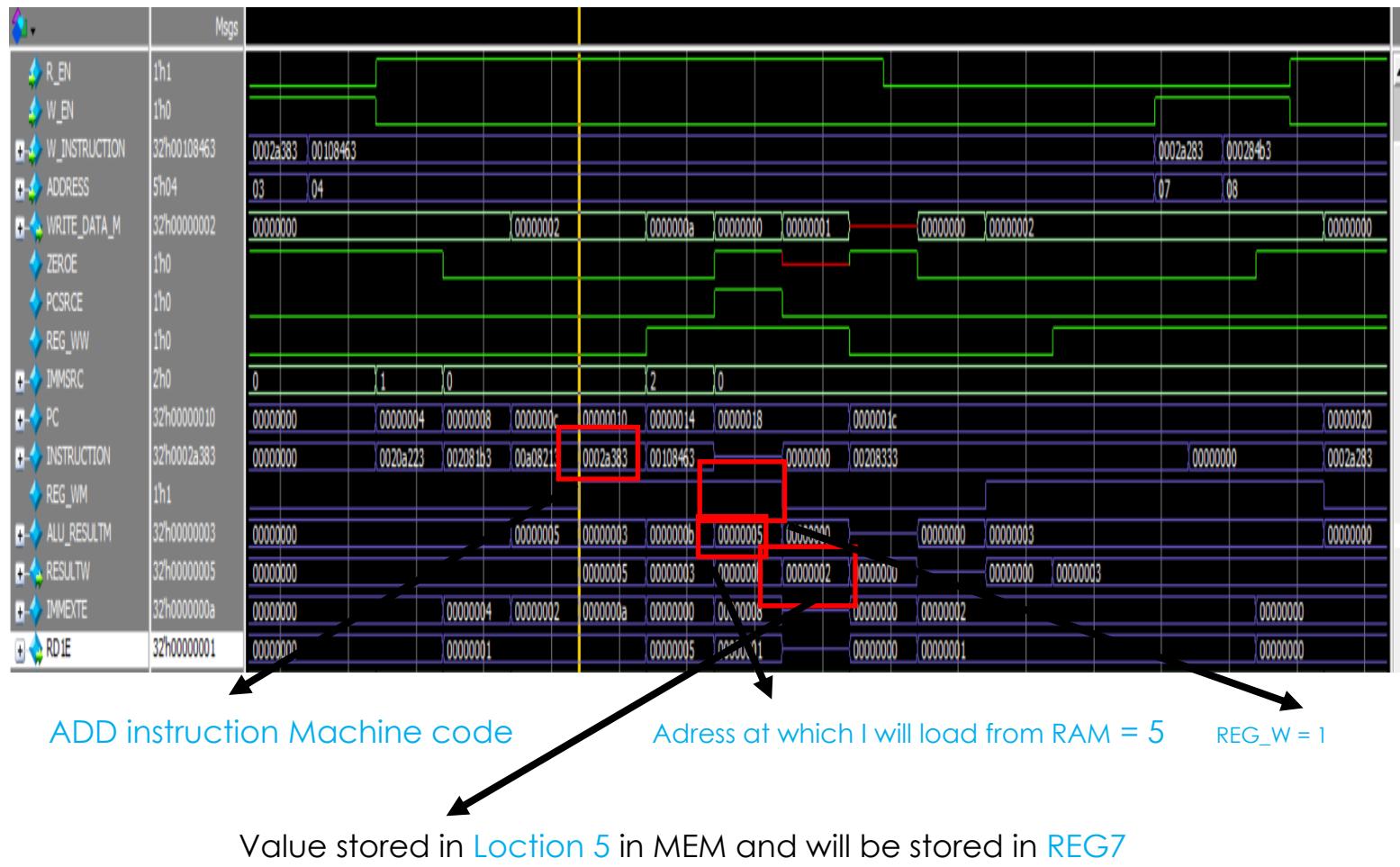
ALU Result = 11 after 2cycles from execute AddI Instruction
Which will be stored In REG4

Value Stored In REG4 In the REG_FILE (Should = Value inside REG1 + 10 = 1 + 10)

Memory Data - /SINGLE_RISC_V_TB/DUT/REG_FILE/REGESTERS - Default									
0000000f	0000000f	0000001e	0000001d	0000001c	0000001b	0000001a	00000019		
00000018	00000018	00000017	00000016	00000015	00000014	00000013	00000012		
00000011	00000011	00000010	0000000f	0000000e	0000000d	0000000c	0000000b		
0000000a	0000000a	00000009	00000008	00000002	00000006	00000005	0000000b		
00000003	00000003	00000002	00000001	00000000					
fffffffc									

WAVE_FORM FOR LW instruction

lw x7, 4(x1)

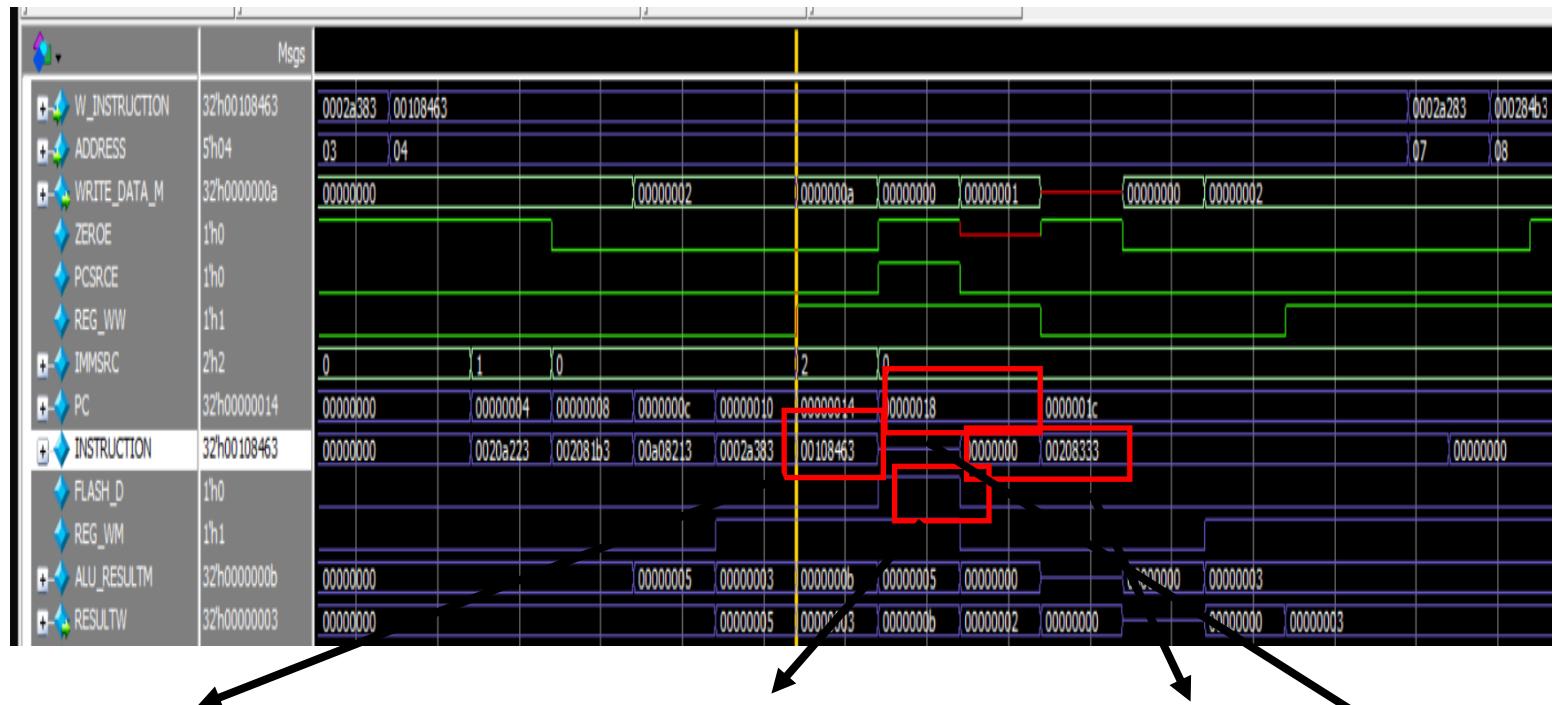


Value Stored In REG7 In REG_File(Should = Loction 1 In the RAM = 2)

Memory Data - /SINGLE_RISC_V_TB/DUT/REG_FILE/REGESTERS - Default	
0000001f	0000001f 0000001e 0000001d 0000001c 0000001b 0000001a 00000019
00000018	00000018 00000017 00000016 00000015 00000014 00000013 00000012
00000011	00000011 00000010 0000000f 0000000e 0000000d 0000000c 0000000b
0000000a	0000000a 00000009 00000008 00000002 00000006 00000005 0000000b
00000003	00000003 00000002 00000001 00000000
fffffc	

WAVE_FORM FOR BEQ instruction

beq x1, x1, label



BEQ instruction Machine code Flash D = 1 Making Instruction = 0 to prevent any DATA HAZARD (preventing Execution the next instruction till we new New PC Adress = 0X0000_0018)

Then it will do instruction stored in this PC Adress => which is (add x6, x1, x2)

The Value stored in REG6 = $1 + 2 = 3$

Memory Data - /SINGLE_RISC_V_TB/DUT/REG_FILE/REGESTERS - Default															
0000001f	0000001f	0000001e	0000001d	0000001c	0000001b	0000001a	00000019	00000018	00000017	00000016					
00000015	00000015	00000014	00000013	00000012	00000011	00000010	0000000f	0000000e	0000000d	0000000c					
0000000b	0000000b	0000000a	00000009	00000008	00000002	00000003	00000005	0000000b	00000003	00000002					
00000001	00000001	00000000													
fffffff7															

DATA Hazard Case

lw x5, 4(x1)
add x9, x5, x0

loading From Location 5 in The RAM = 2 Into REG 5 THEN use it in next R Instruction As rs1 To make Sure That DATA Hazard Won't Happen



- STALL_F = 1 FLASH_E = 1 STALL_D = 1**
- 1: Stall the Fetch Stage: Do not allow a new instruction to be fetched.
 - 2- Stall the Decode Stage: Do not allow a new instruction to be decoded.
 - 3- Flush the Execute Stage: Clear the data currently coming from the Decode stage, as the current instruction executing has not started yet
- And That's happened Because at Execute stage Rs1 matches Memory stage Rd Forward from Memory stage
- And Then **FORWARDA = 1** to forward DATA From Result signal to into ALU first operand preventing DATA HAZARD

From Reg File The Value stored in REG5 = 2 && REG9 = REG5 + REG0 = 2 + 0 = 0

Wave forms Testing APB & FIFO & UART_TX Functionality

Sample assembly program

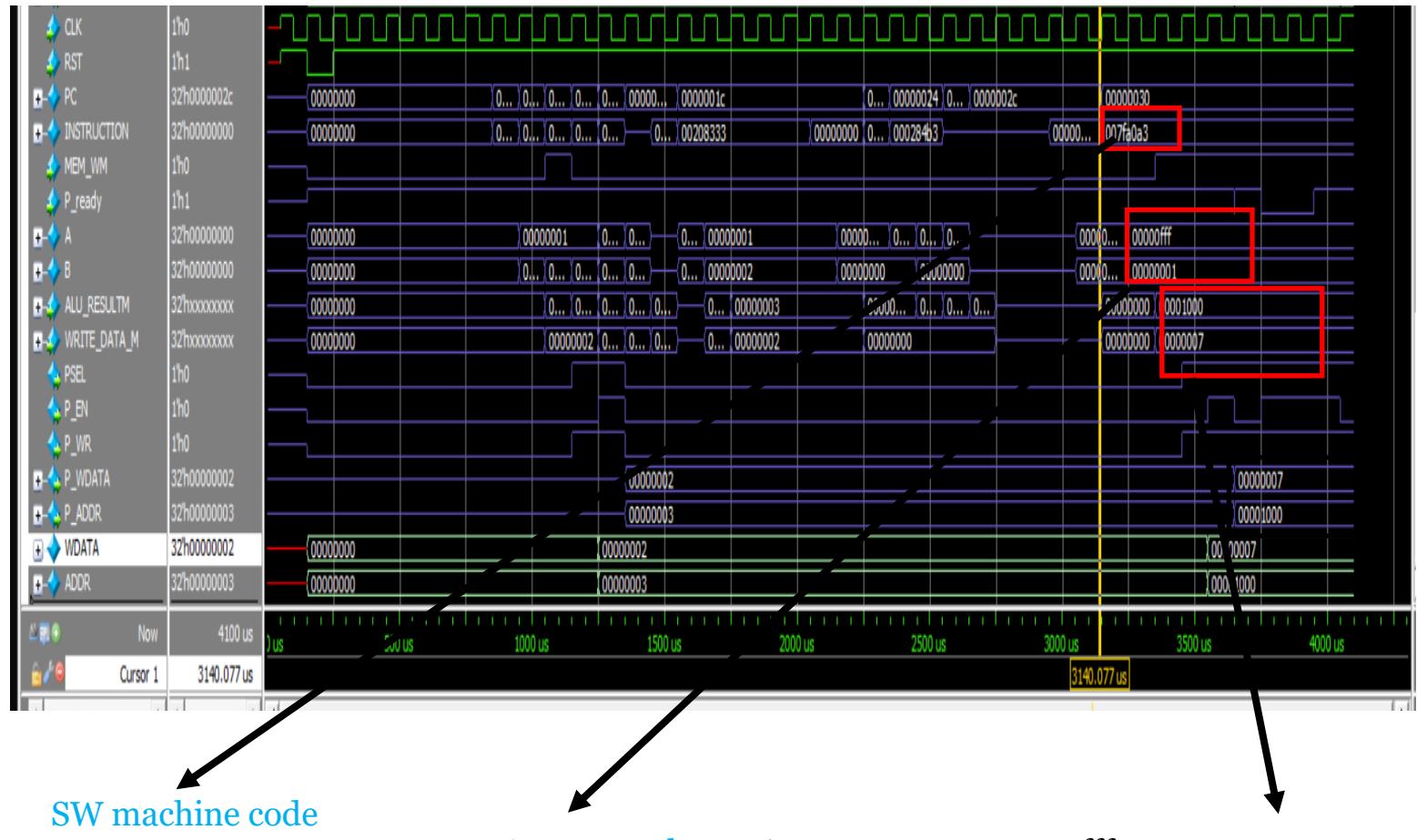
```
*****TESTING _SOC*****
##### Sample assembly program #####
### making value inside REG31 = start Address of UART_MEM
0x0000_0028      add x31,x0,0x0fff          ##### Machine Code == 32'0000111111000000011110010011
### sw Value inside REG7 = 7 into UART_MEM
0x0000_002c      sw x7, 1(x31)           ##### Machine Code == 32'00000000111111101000010100011
```

Transcript Snip Showing Passed Test Cases

```
*****TESTING _SOC*****
# TESTING sw Instruction (sw x7, 1(x31)) Storing value inside REG7 = 7 into UART_MEM (At Address = 0x0000ffff == x31 + 1) to send it
# Test Case Failed and the Value stored in UART_MEM = 0 at Time 3800
# TESTING FIFO Write Operation
# Test Case Passed and the Value stored FIFO_MEM = 7 at Time 4300
# TESTING UART_TX Operation
# TEST CASE PASSED and UART_TX sent DATA = 0x 00000007 at time 7550
# ** Note: $stop : E:/Digital Projects/SOC_Pipe_line_RISC_V/SOC_Pipe_line_RISC_V_TB.v(160)
# Time: 7850 us Iteration: 0 Instance: /SOC_Pipe_line_RISC_V_TB
```

WAVEFORM FOR SW instruction

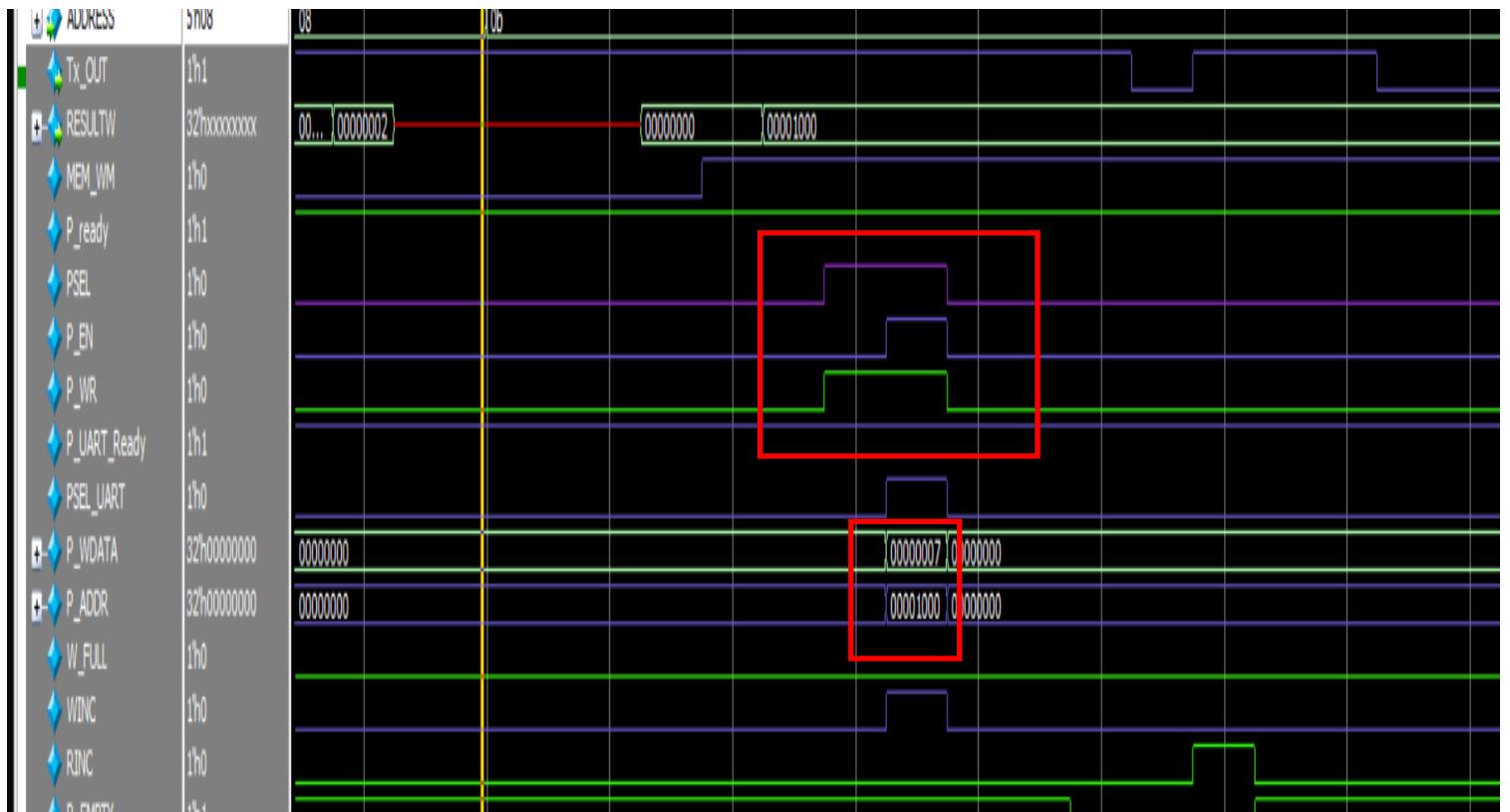
sw x7, 1(x31)



The **Address = ALU_ResultM** (UART_start_Address MEM)

Value will be stored in **UART = W_DATA_M** (UART_TX will send this Value)

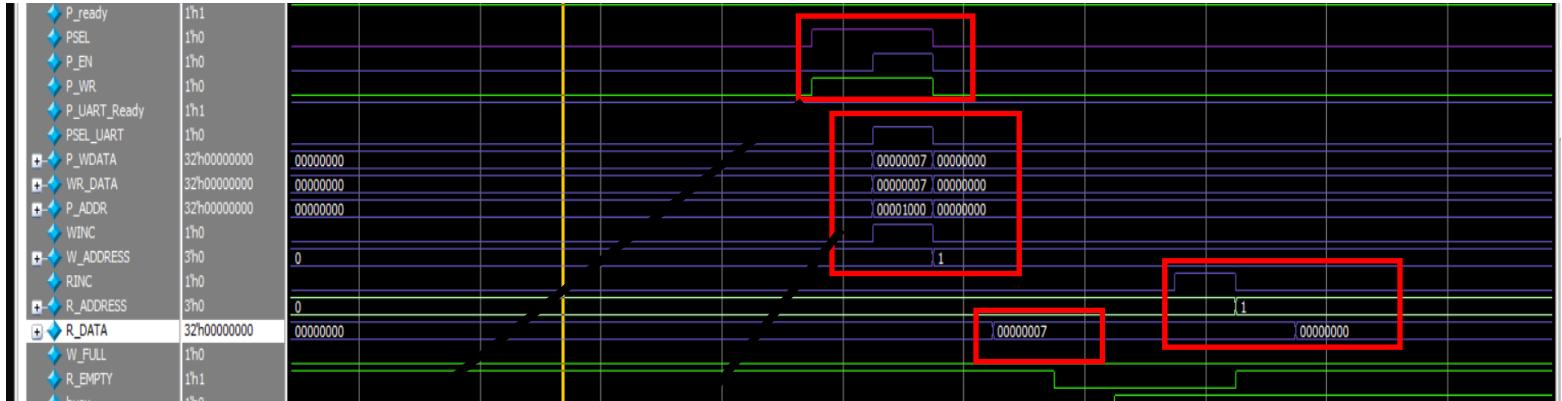
WAVEFORM FOR APB Signals



P_WR = 1 because we store in the UART MEM
 PSEL_UART = 1 once Address was in the range of UART Addresses
 Then P_EN = 1 after one cycle from this

After this P_WDATA = 7 (value was inside W_DATA_M)
 P_ADDR = 0X00001000 (Value inside ALU_RESULT_M)

WAVEFORM FOR FIFO Signals



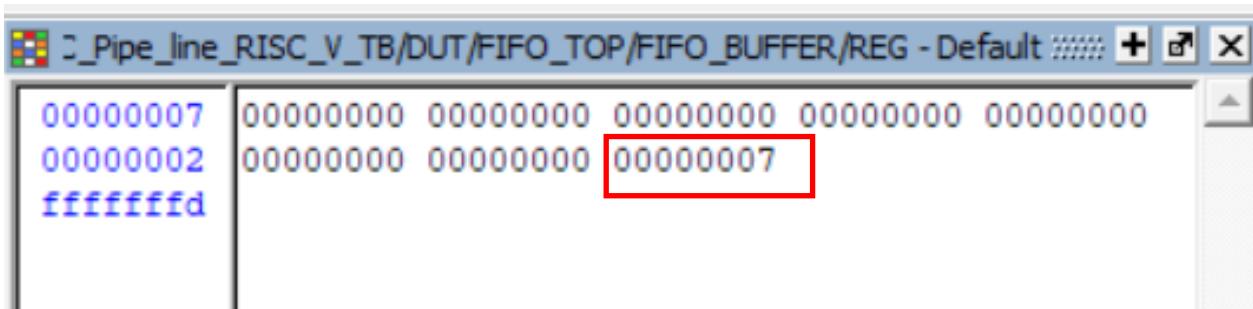
Once **PSEL && P_EN = 1 && P_Address** in the **UART_Addresses Range (0x1000)**

Then **PSEL_UART = 1 && FIFO Will Receive DATA WR_DATA = 0x7**

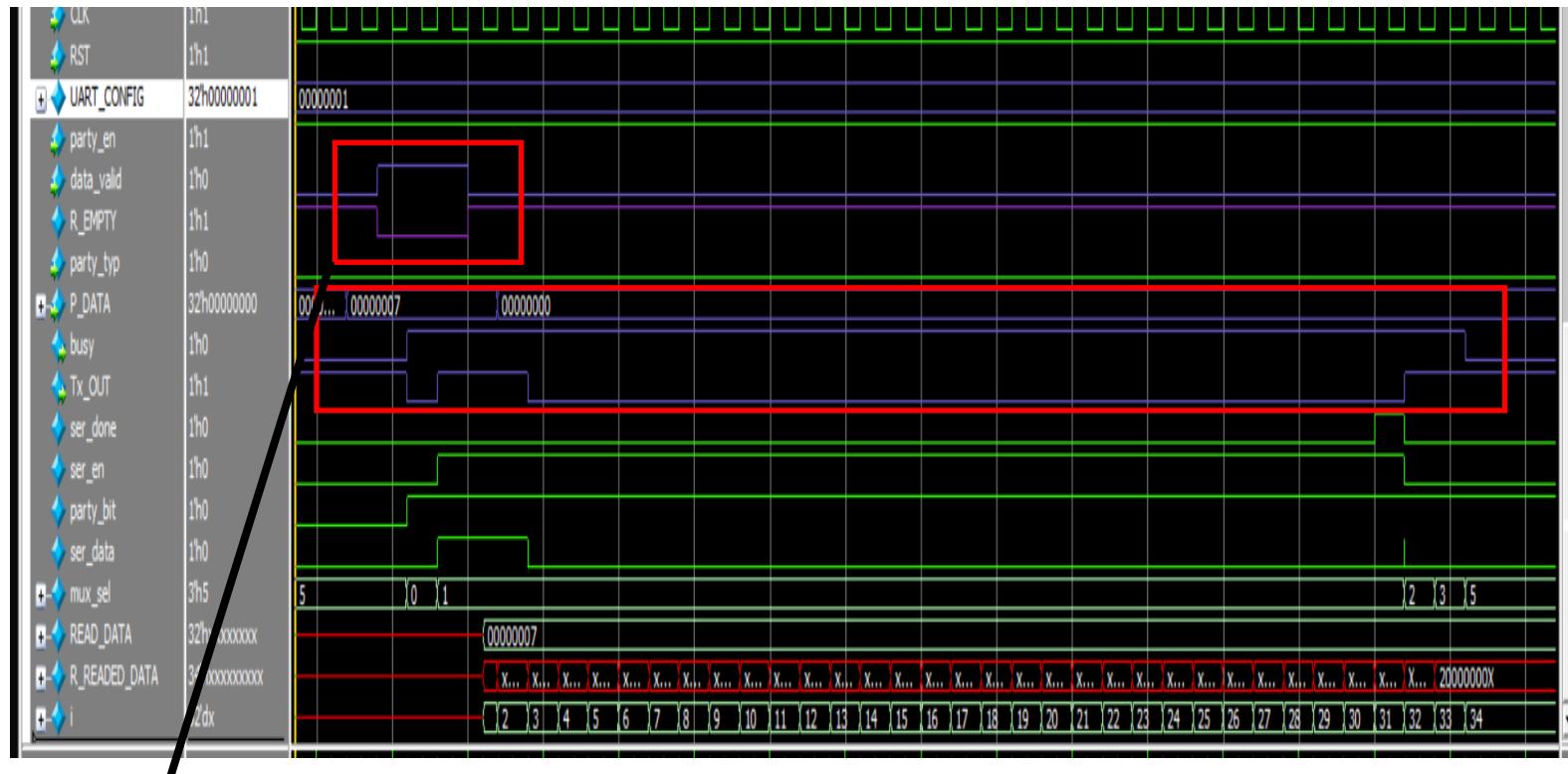
And **FIFO W_EN = 1 && after 2 cycles R_EMPTY = 0 so FIFO R_EN = 1**

And **R_DATA = 0x7 && UART will send it**

Value stored in FIFO correctly in **address = 0**



WAVEFORM FOR UART_TX



Once **R_EMPTY = 0** then **Data_Valid = 1**
 Knowing UART to Send this DATA (**P_DATA = 0x7**)

Then **UART_busy = 1** to update **R_EN** of **FIFO** to indicate to the next DATA to be Sent
 And **UART TX_OUT** Will start Sending DATA Frame Serially
 (Start bit // DATA // parity // end)

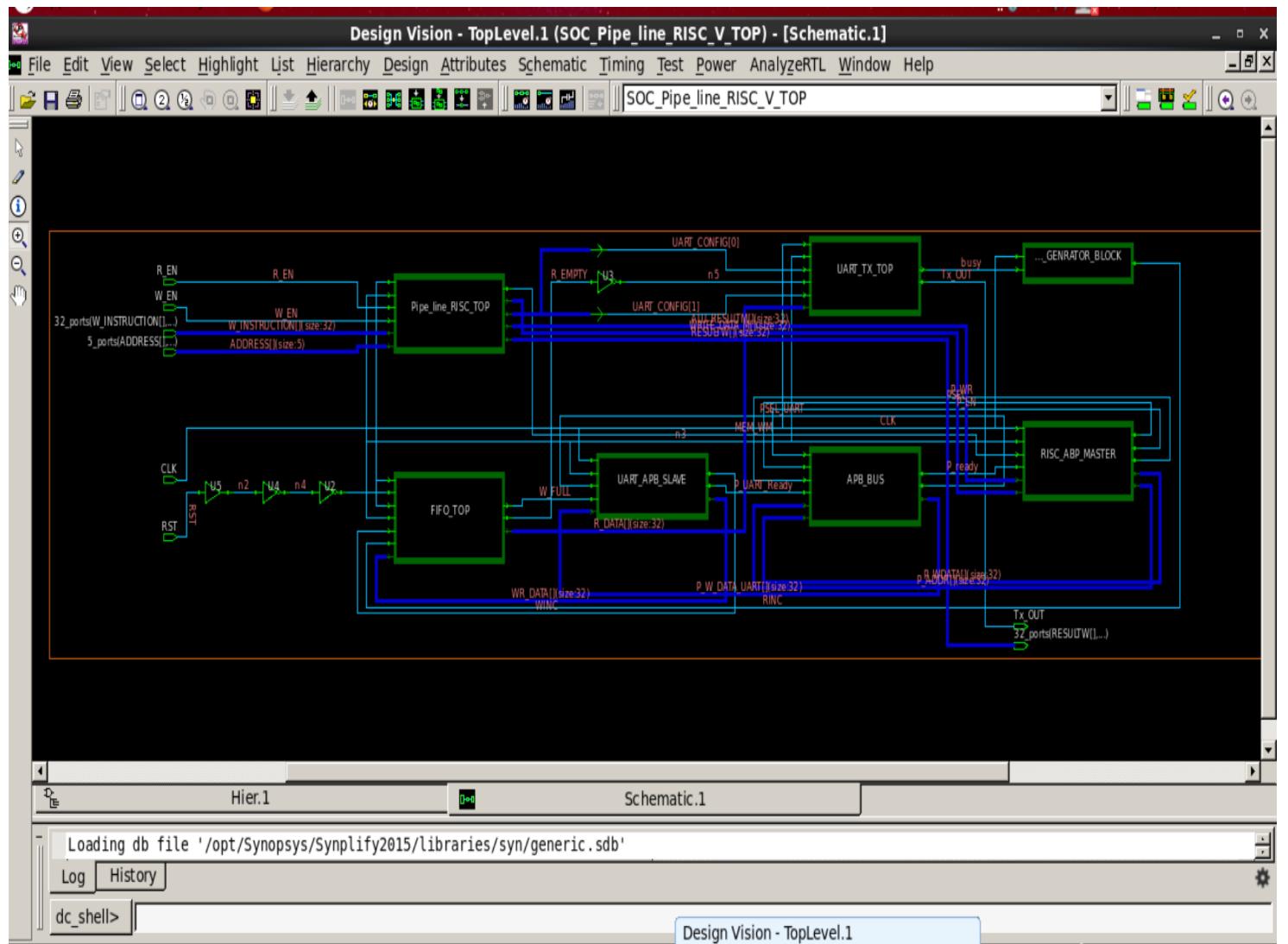
UART_CONFEG is reserved Register responsible for indicating **Parity_en && Parity_typ**

After sending the Frame **Busy = 0** to know FIFO the UART is Available, and you can Pass DATA to him

SYSTEM ASIC FLOW

synthesis Stage

Schematic after synthesis



synthesis Constraints

Synthesis Stage: -

- i. Add the following constraints in **cons.tcl** file.

- ## ○Create your master clock

- CLK (3.686 MHz)

- Create a clock uncertainty with 0.2 ns for setup

- Create a clock uncertainty with 0.1 ns for hold

- Input delays on all input ports except (CLK & RST) with 20% clock period

- output delays on all output ports with 20% clock period

- Add Buffer driving cell for all input ports

- Add load of 0.1 pf on all output ports

- Set operation condition using slow and fast libraries

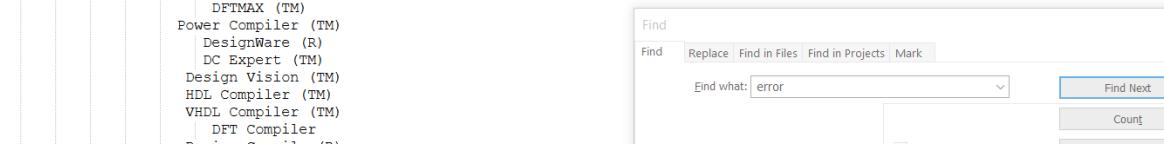
- ## ii. Run synthesis and check the followings

- o No Errors, loops and latches in syn.log file

- Check Setup timing analysis report for Violating paths

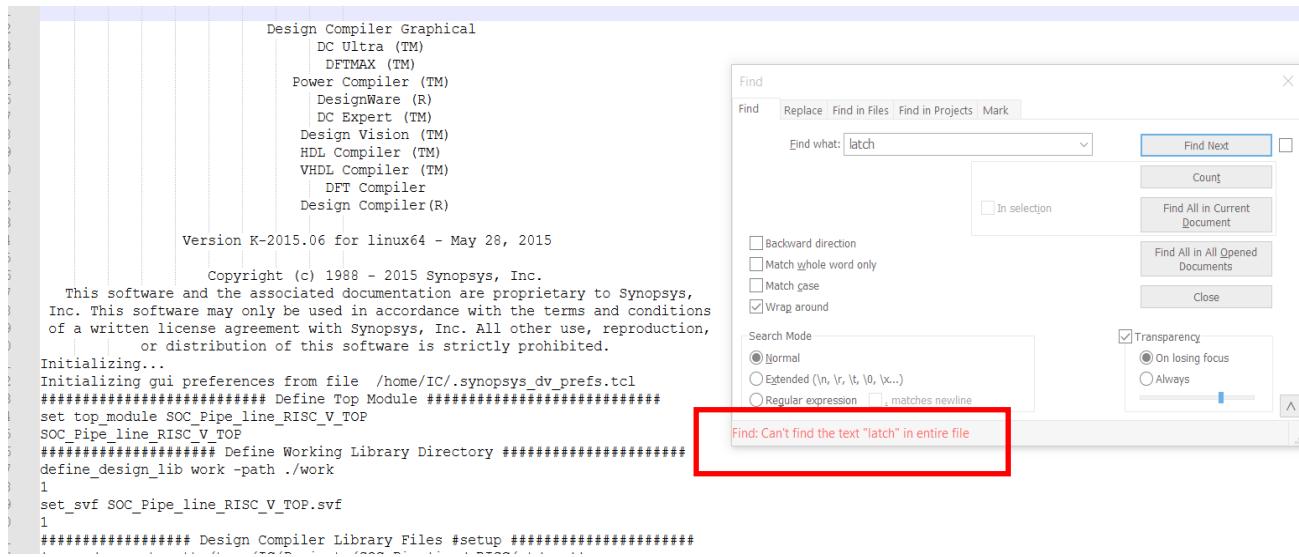
- o Check Hold timing analysis report for Violating paths

No Errors in syn.log file



```
1 Design Compiler Graphical
2 DC Ultra (TM)
3 DFTMAX (TM)
4 Power Compiler (TM)
5 DesignWare (R)
6 DC Expert (TM)
7 Design Vision (TM)
8 HDL Compiler (TM)
9 VHDL Compiler (TM)
10 DFT Compiler
11 Design Compiler(R)
12
13
14 Version K-2015.06 for linux64 - May 28, 2015
15
16 Copyright (c) 1988 - 2015 Synopsys, Inc.
17 This software and the associated documentation are proprietary to Synopsys,
18 Inc. This software may only be used in accordance with the terms and conditions
19 of a written license agreement with Synopsys, Inc. All other use, reproduction,
20 or distribution of this software is strictly prohibited.
21 Initializing...
22 Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl
23 ##### Define Top Module #####
24 set top_module SOC_Pipe_line_RISC_V_TOP
25 SOC_Pipe_line_RISC_V_TOP
26 ##### Define Working Library Directory #####
27 define_design_lib work -path .\work
28
```

No Latches in syn.log file



```
Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Design Compiler(R)

Version K-2015.06 for linux64 - May 28, 2015

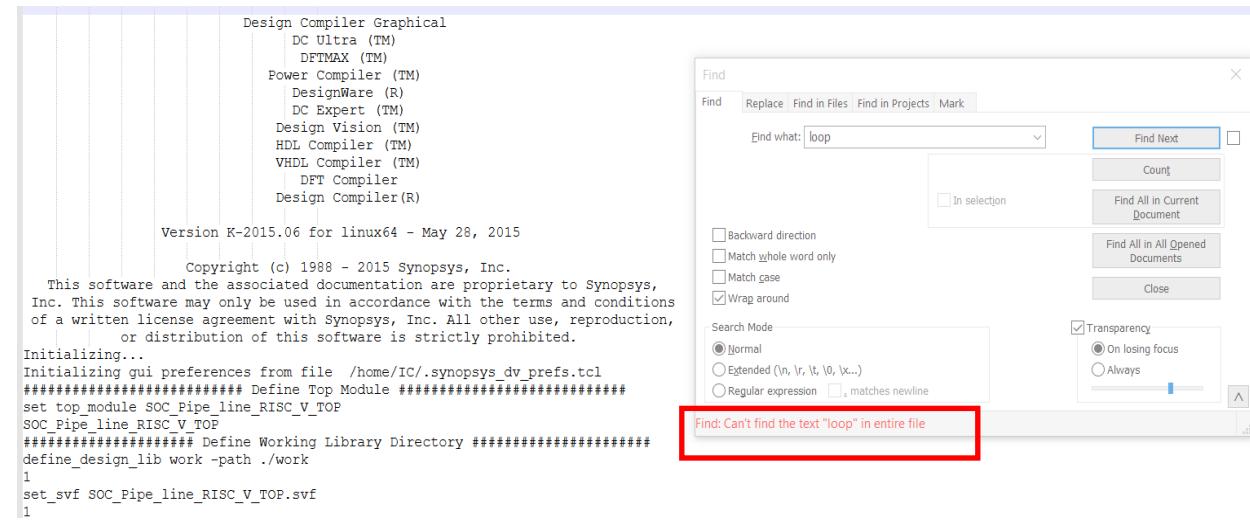
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Initializing...
Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl
#####
# Define Top Module #####
set top_module SOC_Pipe_line_RISC_V_TOP
SOC_Pipe_line_RISC_V_TOP
##### Define Working Library Directory #####
define_design_lib work -path ./work
1
set_svf SOC_Pipe_line_RISC_V_TOP.svf
1
##### Design Compiler Library Files #setup #####

```

No Loops in syn.log file



```
Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Design Compiler(R)

Version K-2015.06 for linux64 - May 28, 2015

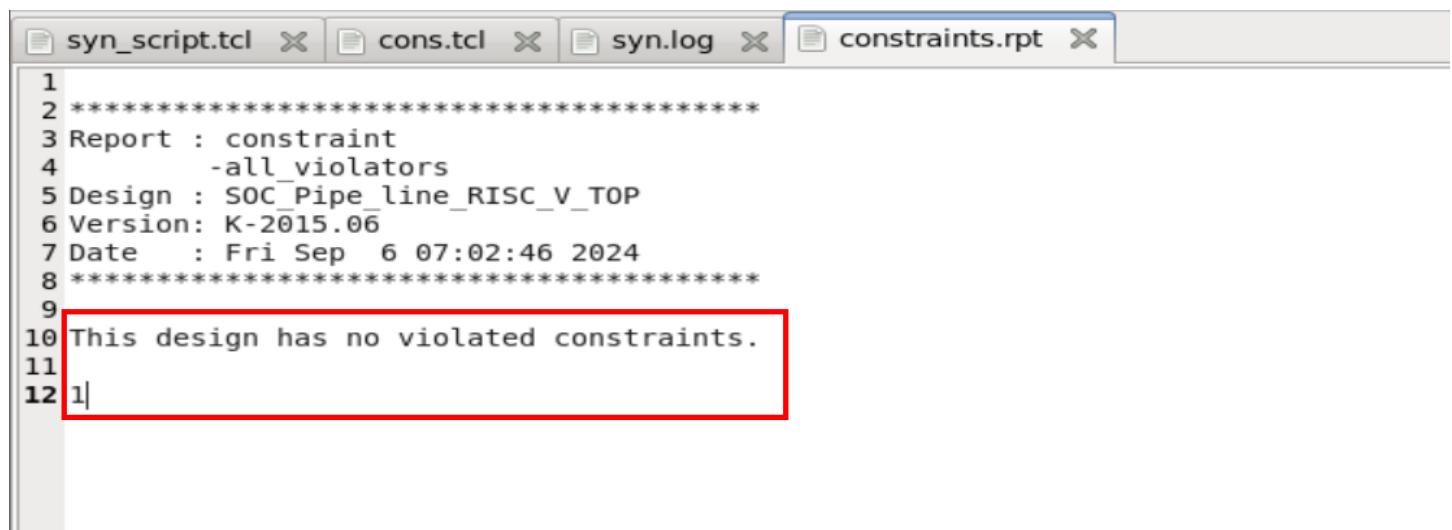
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Initializing...
Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl
#####
# Define Top Module #####
set top_module SOC_Pipe_line_RISC_V_TOP
SOC_Pipe_line_RISC_V_TOP
##### Define Working Library Directory #####
define_design_lib work -path ./work
1
set_svf SOC_Pipe_line_RISC_V_TOP.svf
1

```

Check violated constraints file



```
1 ****
2 **** Report : constraint
3 **** -all_violators
4 **** Design : SOC_Pipe_line_RISC_V_TOP
5 **** Version: K-2015.06
6 **** Date : Fri Sep 6 07:02:46 2024
7 **** ****
8 ****
9
10 This design has no violated constraints.
11
12 1|
```

Check violated Paths in Setup file

The screenshot shows a software interface with three tabs at the top: syn.log, hold.rpt, and setup.rpt. The setup.rpt tab is active. On the left, there is a code editor window displaying a timing report for a SOC_Pipe_line_RISC_V_TOP design. The report includes details like operating conditions, wire load model mode, and path information. On the right, a 'Find' dialog box is open with the search term 'violate' entered. A red box highlights the message 'Find: Can't find the text "violate" in entire file' which appears in the bottom right corner of the dialog.

```
1 ****
2 Report : timing
3     -path full
4     -delay max
5     -max_paths 100
6 Design : SOC_Pipe_line_RISC_V_TOP
7 Version: K-2015.06
8 Date : Fri Sep 6 07:02:46 2024
9 ****
10 # A fanout number of 1000 was used for high fanout net computations.
11
12 Operating Conditions: scmetro_tsmc_c1013g_rvt_ss_1p08v_125c Library: scmetro_tsmc_c1013g_rvt_ss_1p08v_125c
13 Wire Load Model Mode: top
14
15 Startpoint: W_EN (input port clocked by MASTER_CLK)
16 Endpoint: Pipe_line_RISC_TOP/ROM/REG_reg[29][31]
17     (rising edge-triggered flip-flop clocked by MASTER_CLK)
18 Path Group: INREG
19 Path Type: max
20
21 Point           Incr      Path
22 -----
23
24 clock MASTER_CLK (rise edge)          0.00    0.00
25 clock network delay (ideal)         0.00    0.00
26 input external delay                54.26   54.26 r
27 W_EN (in)                          0.02    54.28 r
28
29 Pipe_line_RISC_TOP/W_EN (Pipe_line_RISC_TOP_ADDRESS_BITS4) 0.00    54.28 r
30
31 Pipe_line_RISC_TOP/ROM/W_EN (ROM_ADDRESS_BITS4)            0.00    54.28 r
32 Pipe_line_RISC_TOP/ROM/U290/Y (NOR3BX2M)                  0.31    54.59 r
33 Pipe_line_RISC_TOP/ROM/U9/Y (NAND2X1M)                   0.29    54.88 f
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```

Check Area report

Hierarchical cell	Global cell area			Local cell area		
	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black-boxes	Design
SOC_Pipe_line_RISC_V_TOP	517139.6490	100.0	15.2971	0.0000	0.0000	SOC_Pipe_line_RISC_V_TOP
APB_BUS	296.5284	0.1	296.5284	0.0000	0.0000	APB_BUS
FIFO_TOP	13286.1198	2.6	7.0602	0.0000	0.0000	FIFO_TOP_DATA_WIDTH_TOP32_FIFO_DEPTH_TOP8_ADDRESS_BITS_TOP3
FIFO_TOP/DF_SYNC	414.1984	0.1	0.0000	414.1984	0.0000	DF_SYNC_ADDRESS_BITS3
FIFO_TOP/FIFO_BUFFER	12335.3462	2.4	4879.7750	7455.5711	0.0000	FIFO_BUFFER_DATA_WIDTH32_FIFO_DEPTH8_ADDRESS_BITS3
FIFO_TOP/FIFO_RD	264.7575	0.1	160.0312	104.7263	0.0000	FIFO_RD_ADDRESS_BITS3
FIFO_TOP/FIFO_WR	264.7575	0.1	161.2079	103.5496	0.0000	FIFO_WR_ADDRESS_BITS3
PULSE_GENRATOR_BLOCK	48.2447	0.0	5.8835	42.3612	0.0000	PULSE_GENRATOR_BLOCK
Pipe_line_RISC_TOP	498053.5749	96.3	14.1204	0.0000	0.0000	Pipe_line_RISC_TOP_ADDRESS_BITS4
Pipe_line_RISC_TOP/ALU	12248.2703	2.4	2622.8643	2718.1770	0.0000	ALU
Pipe_line_RISC_TOP/ALU/add_88	960.1872	0.2	960.1872	0.0000	0.0000	ALU_DW01_add_0
Pipe_line_RISC_TOP/ALU/eq_87	458.9130	0.1	458.9130	0.0000	0.0000	ALU_DW01_cmp6_0
Pipe_line_RISC_TOP/ALU/r67	956.6571	0.2	956.6571	0.0000	0.0000	ALU_DW01_add_I
Pipe_line_RISC_TOP/ALU/sll_81	1987.4463	0.4	1987.4463	0.0000	0.0000	ALU_DW01_ash_0
Pipe_line_RISC_TOP/ALU/srl_82	1472.0517	0.3	1472.0517	0.0000	0.0000	ALU_DW01_rash_0
Pipe_line_RISC_TOP/ALU/sub_78	1071.9737	0.2	1071.9737	0.0000	0.0000	ALU_DW01_sub_0
Pipe_line_RISC_TOP/CONTROL_UNIT	463.6198	0.1	204.7458	258.8740	0.0000	CONTROL_UNIT
Pipe_line_RISC_TOP/EXTEND_UNIT	158.8545	0.0	158.8545	0.0000	0.0000	EXTEND_UNIT
Pipe_line_RISC_TOP/HAZARD_UNIT	441.2625	0.1	441.2625	0.0000	0.0000	HAZARD_UNIT
Pipe_line_RISC_TOP/PC_COUNTER	1827.4151	0.4	490.6839	828.3960	0.0000	PC_COUNTER
Pipe_line_RISC_TOP/PC_COUNTER/r54	508.3344	0.1	508.3344	0.0000	0.0000	PC_COUNTER_DW01_add_0
Pipe_line_RISC_TOP/RAM	376944.0803	72.9	162182.2126	214761.8677	0.0000	RAM
Pipe_line_RISC_TOP/REG_FILE	61773.2205	11.9	30508.3018	31264.9187	0.0000	REG_FILE
Pipe_line_RISC_TOP/ROM	44182.7315	8.5	19554.4012	24628.3303	0.0000	ROM_ADDRESS_BITS4
RISC_ABP_MASTER	2944.1034	0.6	1193.1738	1750.9296	0.0000	RISC_ABP_MASTER
UART_APB_SLAVE	198.8623	0.0	198.8623	0.0000	0.0000	UART_APB_SLAVE
UART_TX_TOP	2296.9184	0.4	0.0000	0.0000	0.0000	UART_TX_TOP_DATA_WIDTH32
UART_TX_TOP/FSM	156.5011	0.0	78.8389	77.6622	0.0000	FSM_TX
UART_TX_TOP/MUX	17.6505	0.0	17.6505	0.0000	0.0000	MUX
UART_TX_TOP/parity	385.9576	0.1	360.0702	25.8874	0.0000	parity_calc_DATA_WIDTH32
UART_TX_TOP/serial	1736.8092	0.3	776.6220	960.1872	0.0000	serializer_DATA_WIDTH32
Total	231744.0116	285395.6373	0.0000			

1

Check Power report

Hierarchy	Switch Power	Int Power	Leak Power	Total Power	%
SOC_Pipe_line_RISC_V_TOP	2.22e-02	0.639	2.87e+08	0.948	100.0
UART_TX_TOP (UART_TX_TOP_DATA_WIDTH32)					
MUX (MUX)	3.22e-05	2.22e-03	1.44e+06	3.69e-03	0.4
parity (parity_calc_DATA_WIDTH32)	1.00e-08	5.38e-05	3.89e+05	4.43e-04	0.0
FSM (FSM_TX)	1.76e-07	1.62e-04	8.42e+04	2.47e-04	0.0
serial (serializer_DATA_WIDTH32)	3.18e-05	2.01e-03	9.52e+05	2.99e-03	0.3
PULSE_GENRATOR_BLOCK (PULSE_GENRATOR_BLOCK)					
r67 (ALU_DW01_add_1)	1.70e-08	1.18e-04	3.15e+04	1.50e-04	0.0
sub_78 (ALU_DW01_sub_0)	3.22e-07	2.96e-08	1.27e+04	1.30e-05	0.0
sll_81 (ALU_DW01_ash_0)	2.23e-07	2.96e-08	1.27e+04	1.30e-05	0.0
srl_82 (ALU_DW01_rash_0)	1.05e-07	2.21e-04	1.95e+05	4.16e-04	0.0
eq_87 (ALU_DW01_cmp6_0)	8.71e-08	2.15e-08	1.90e+05	4.06e-04	0.0
add_88 (ALU_DW01_add_0)	1.22e-05	1.81e-04	8.72e+05	1.07e-03	0.1
EXTEND_UNIT (EXTEND_UNIT)					
CONTROL_UNIT (CONTROL_UNIT)	1.05e-05	1.47e-05	1.00e+05	1.25e-04	0.0
ROM (ROM_ADDRESS_BITS4)					
r54 (PC_COUNTER_DW01_add_0)	8.19e-06	5.47e-04	2.22e+05	7.77e-04	0.1
PC_COUNTER (PC_COUNTER)					
r54 (PC_COUNTER_DW01_add_0)	9.11e-05	1.87e-03	1.08e+06	3.04e-03	0.3
	6.12e-06	1.49e-05	4.21e+05	4.42e-04	0.0

1

Formality Post Synthesis Stage

Testing Verification after Formality

The screenshot shows the Synopsys Formality (R) Console interface. At the top right, a red box highlights the status bar which displays "Verification Succeeded". Below the status bar, the console window shows a table of failing points. The table has columns for Type, Reference, Size, Implementation, and Loops. There are 11 rows of data, each corresponding to a DFF component. At the bottom left, it says "# of Passing Points: 11218". On the right side, there are buttons for "Analyze", "Analyze Selected Points", and "Get Loop Data". The bottom of the window shows a log area with tabs for Log, Errors, Warnings, History, and Last Command. The log area contains the command "formality (verify)>". The bottom status bar shows the shell state as "verify".

Check Falling Points Report

The screenshot shows a gedit window displaying the "failing_points.rpt" file. The window title is "failing_points.rpt (~/Projects/SOC_Pipelined_RISC/fm) - gedit". The file content is a script with several lines of text. A red box highlights the line "0 No failing compare points.".

```
1 ****
2 Report      : failing_points
3
4 Reference   : r:/WORK/SOC_Pipe_line_RISC_V_TOP
5 Implementation : i:/WORK/SOC_Pipe_line_RISC_V_TOP
6 Version     : L-2016.03-SP1
7 Date        : Fri Sep 6 09:30:16 2024
8 ****
9
0 No failing compare points.
1
2 1
```

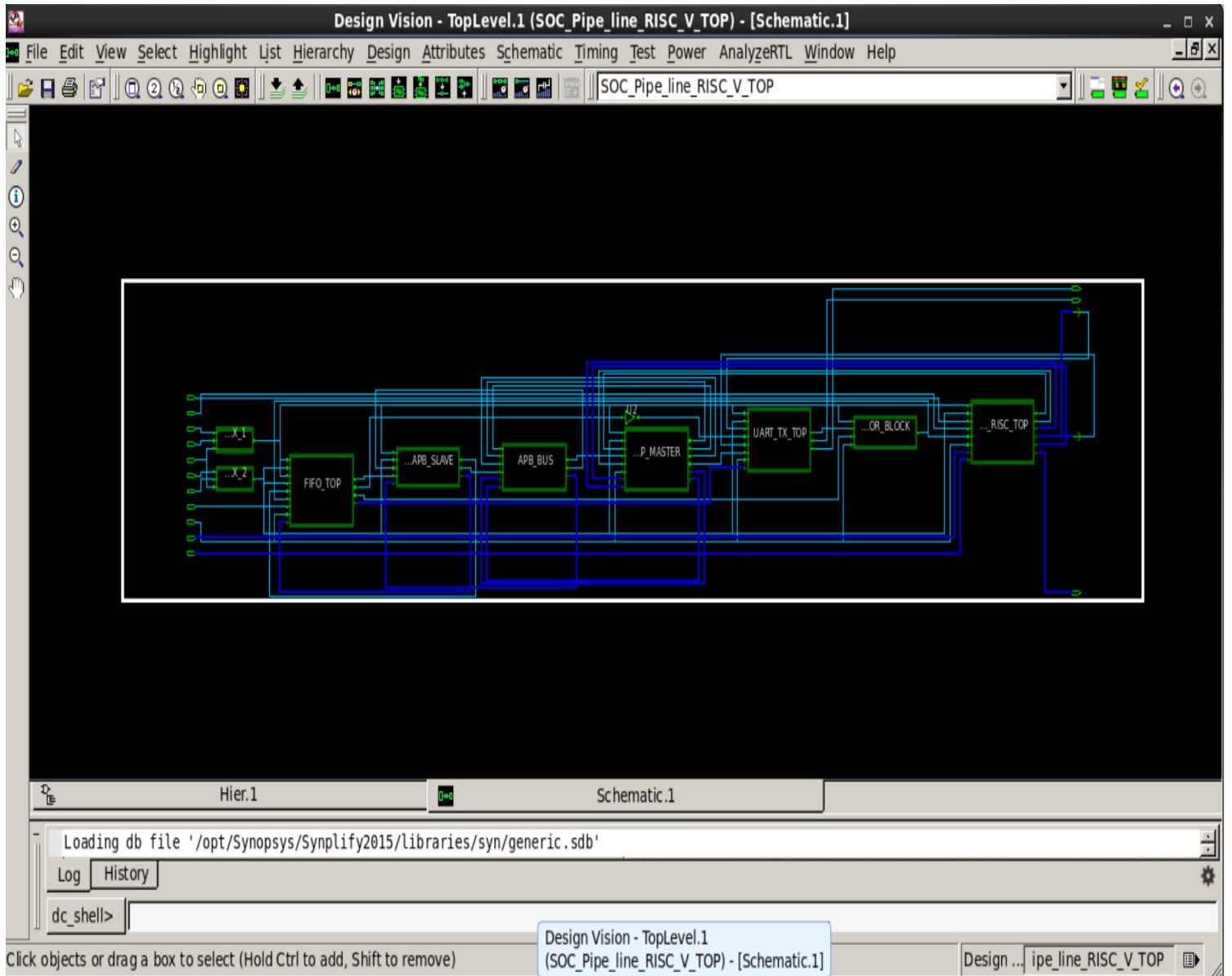
Check Aborted Compare Points Report

The screenshot shows a gedit window displaying the "aborted_points.rpt" file. The window title is "aborted_points.rpt (~/Projects/SOC_Pipelined_RISC/fm) - gedit". The file content is a script with several lines of text. A red box highlights the line "0 No aborted compare points.".

```
1 ****
2 Report      : aborted_points
3
4 Reference   : r:/WORK/SOC_Pipe_line_RISC_V_TOP
5 Implementation : i:/WORK/SOC_Pipe_line_RISC_V_TOP
6 Version     : L-2016.03-SP1
7 Date        : Fri Sep 6 09:30:16 2024
8 ****
9
0 No aborted compare points.
1
2 1
```

DFT Stage

Schematic after DFT



DFT Constraints

DFT Stage: -

- i. Define a new file with name **SYS_TOP_dft.v** inside **SYS_TOP** folder
- ii. Do the rtl preparation in **SYS_TOP_dft.v** including:-

Adding scan ports

- **SCAN_IN**
- **SCAN_EN**
- **SCAN_CLK**
- **SCAN_RST**
- **TEST_MODE**
- **SCAN_OUT**

2. adding Muxes on clocks and resets ports
- iii. Add the following constraints inside **cons.tcl**
 1. Add scan clock constraint using `create_clock`
 2. Add `SCAN_CLK` group in clock grouping command
 3. Input delays on all scan input ports with 20% clock period
 4. Output delays on all scan output ports with 20% clock period
5. Add `set_case_analysis 1 [get_port test_mode]` command to run timing analysis using scan clock
- iv. Add all the dft sections:-
 1. Architecture Scan Chains
 2. Define DFT Signals
 3. Create Test Protocol
 4. Pre-DFT Design Rule Checking
 5. Preview DFT
 6. Insert DFT
 7. Design Rule Checking post dft insertion

v. Run dft and check the followings

- o No Errors, loops and latches in **dft.log** file
- o Check Setup timing analysis report for Violating paths
- o Check Hold timing analysis report for Violating paths
- o Check dft coverage > 99 %

No Errors in dft.log file

```
syn.log hold.rpt setup.rpt area.rpt power.rpt dft.log
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```

Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Design Compiler(R)

Version K-2015.06 for linux64 - May 28, 2015

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Initializing...

Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl

Define Top Module

set top_module SOC_Pipe_line_RISC_V_TOP

SOC_Pipe_line_RISC_V_TOP

Define Working Library Directory

define_design_lib work -path ./work

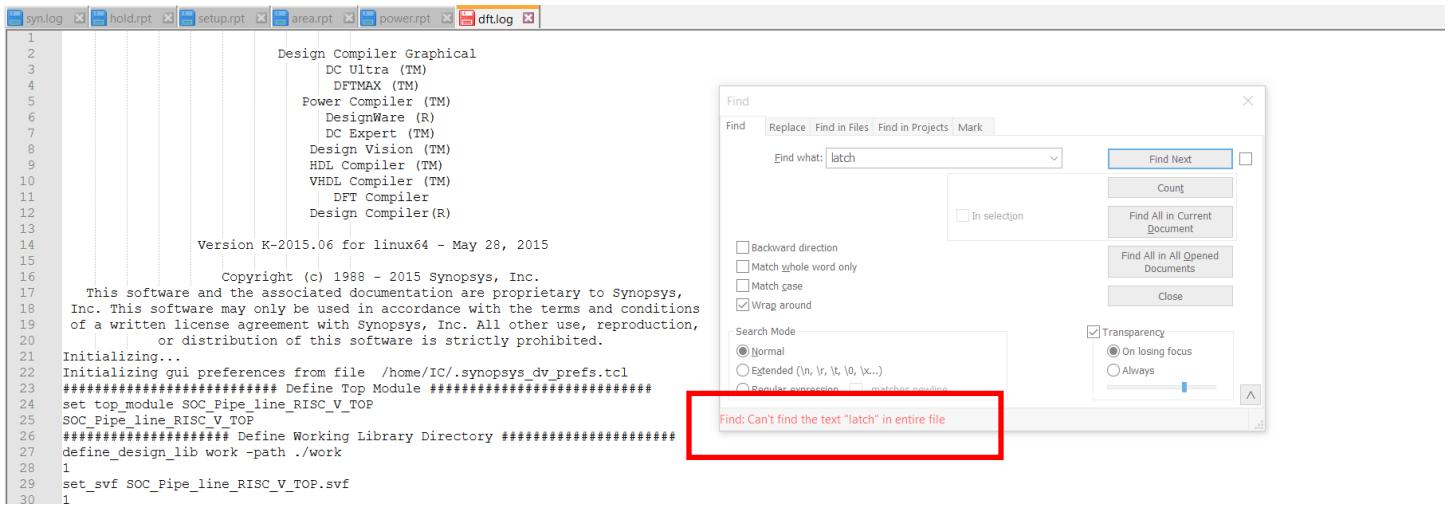
1

set_svf SOC_Pipe_line_RISC_V_TOP.svf

1

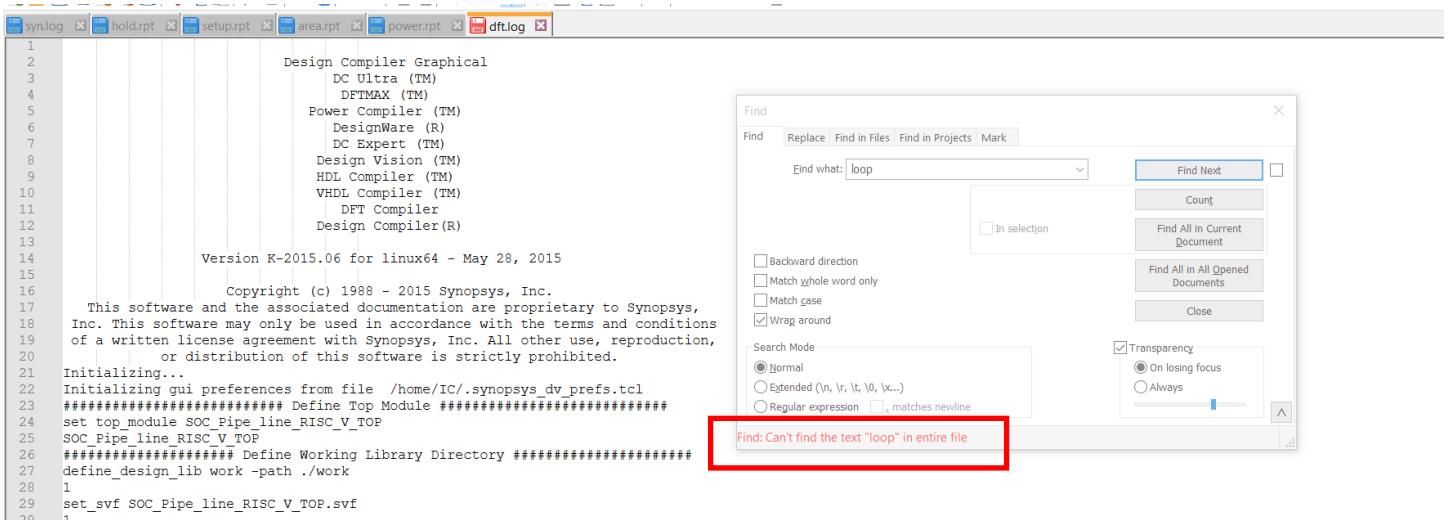
Design Compiler Library Files
lappend search_path /home/IC/Projects/SOC_Pipelined_RISC/std_cells
./opt/Synopsys/Synplify2015/libraries/syn /opt/Synopsys/Synplify2015/minpower/syn /opt/Synopsys/Synplify2015/dw/syn_ver /opt/Synopsys/Synplify2015/dw/sim_ver /
lappend search_path /home/IC/Projects/SOC_Pipelined_RISC/rtl

No Latches in dft.log file



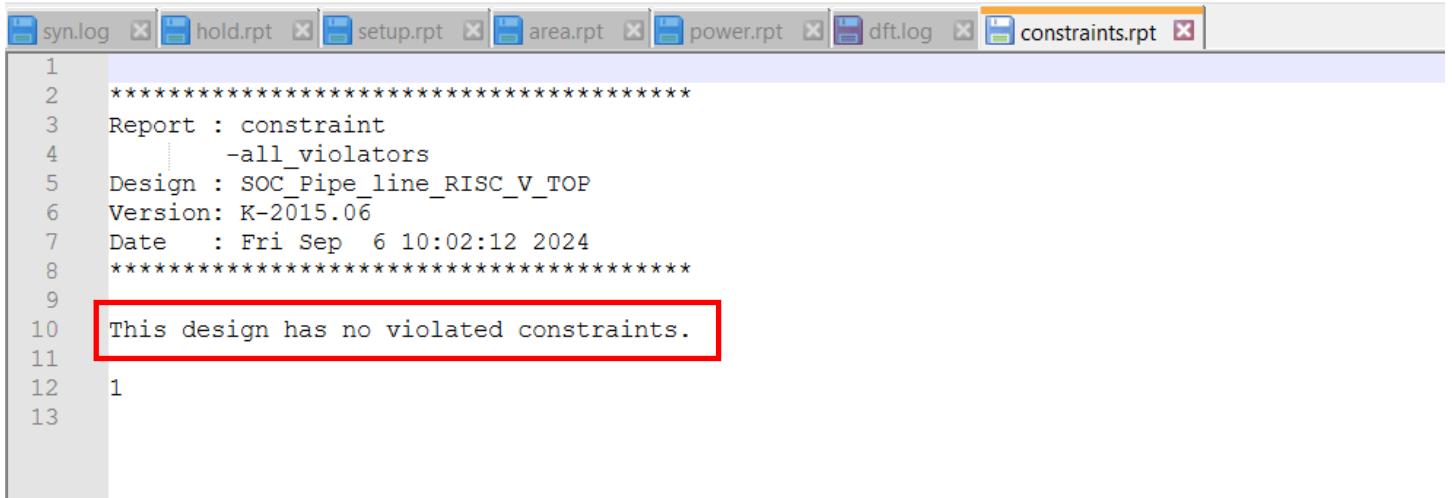
```
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13
14 Version K-2015.06 for linux64 - May 28, 2015
15 Copyright (c) 1988 - 2015 Synopsys, Inc.
16 This software and the associated documentation are proprietary to Synopsys,
17 Inc. This software may only be used in accordance with the terms and conditions
18 of a written license agreement with Synopsys, Inc. All other use, reproduction,
19 or distribution of this software is strictly prohibited.
20 Initializing...
21 Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl
22 ##### Define Top Module #####
23 set_top_module SOC_Pipe_line_RISC_V_TOP
24 SOC_Pipe_line_RISC_V_TOP
25 ##### Define Working Library Directory #####
26 define_design_lib work -path ./work
27 define_design_lib work -path ./work
28 1
29 set_svf SOC_Pipe_line_RISC_V_TOP.svf
30 1
```

No Loops in dft.log file



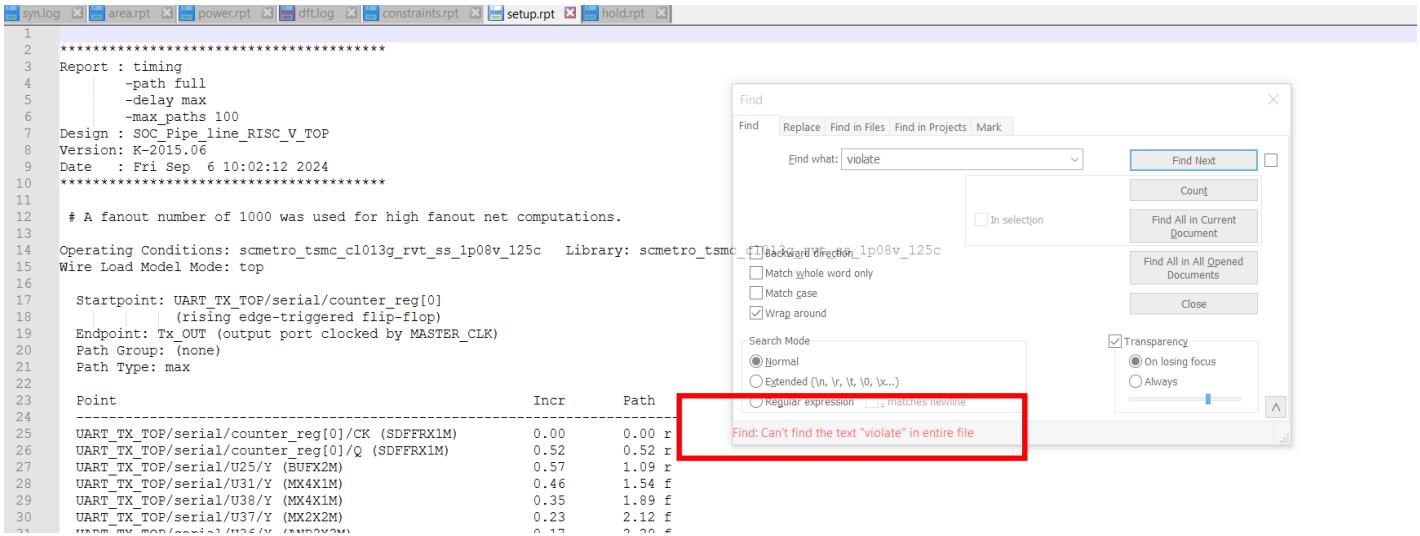
```
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13
14 Version K-2015.06 for linux64 - May 28, 2015
15 Copyright (c) 1988 - 2015 Synopsys, Inc.
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17 Inc. This software may only be used in accordance with the terms and conditions
18 of a written license agreement with Synopsys, Inc. All other use, reproduction,
19 or distribution of this software is strictly prohibited.
20 Initializing...
21 Initializing gui preferences from file /home/IC/.synopsys_dv_prefs.tcl
22 ##### Define Top Module #####
23 set_top_module SOC_Pipe_line_RISC_V_TOP
24 SOC_Pipe_line_RISC_V_TOP
25 ##### Define Working Library Directory #####
26 define_design_lib work -path ./work
27 define_design_lib work -path ./work
28 1
29 set_svf SOC_Pipe_line_RISC_V_TOP.svf
30 1
```

Check violated constraints file



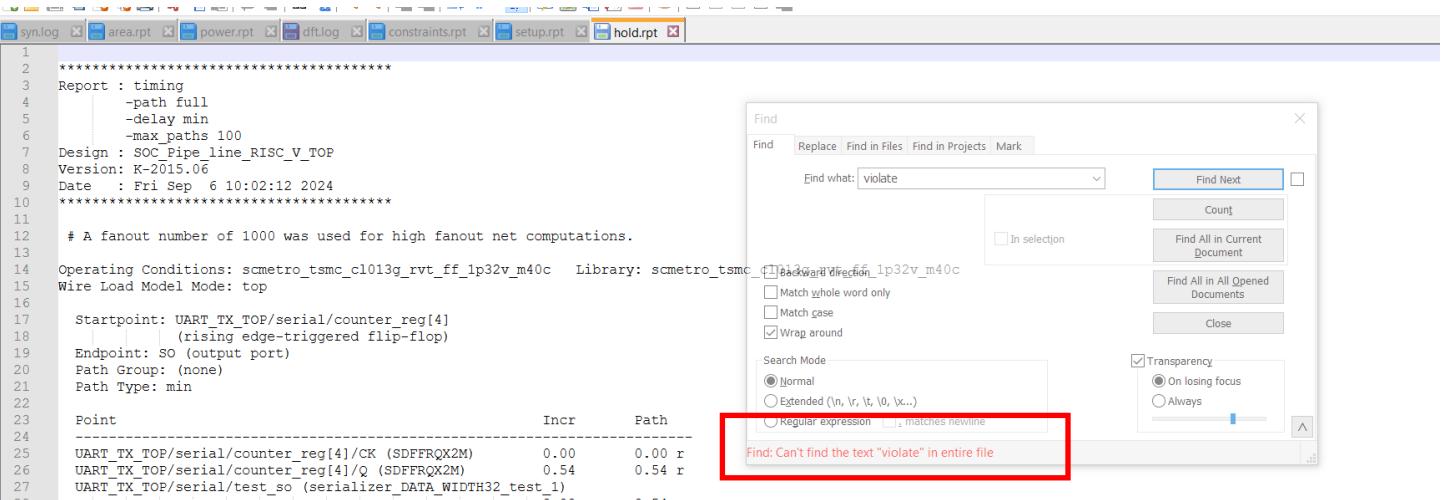
```
1 ****
2 Report : constraint
3     -all_violators
4 Design : SOC_Pipe_line_RISC_V_TOP
5 Version: K-2015.06
6 Date   : Fri Sep 6 10:02:12 2024
7 ****
8
9
10 This design has no violated constraints.
11
12 1
13
```

Check violated Paths in Setup file



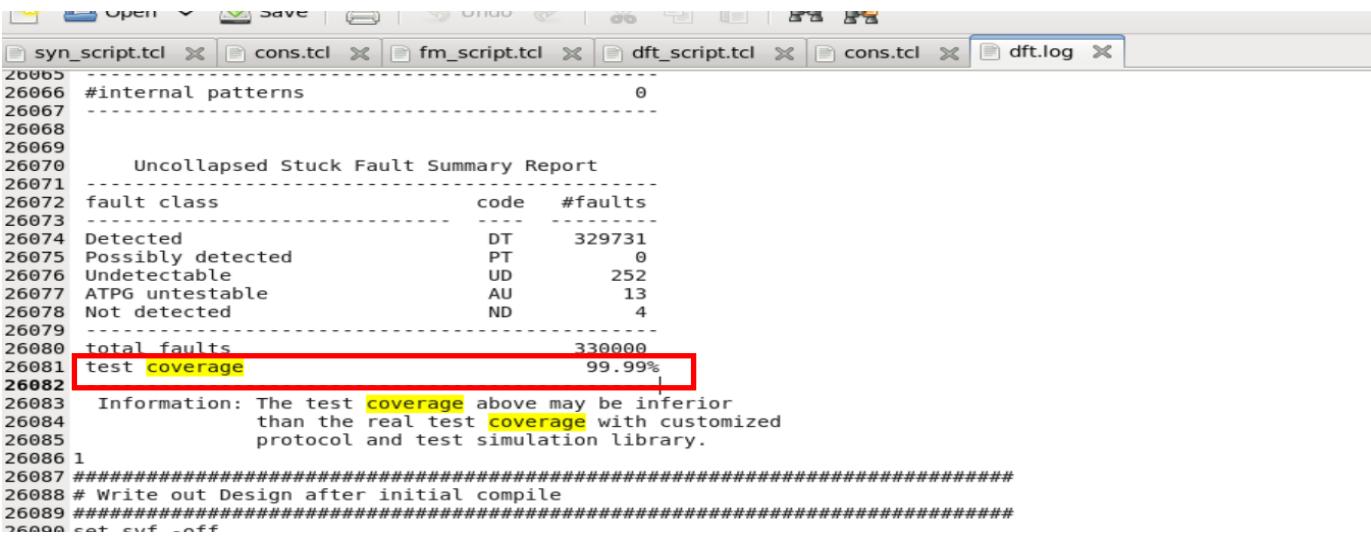
```
1 ****
2 Report : timing
3     -path full
4     -delay max
5     -max_paths 100
6 Design : SOC_Pipe_line_RISC_V_TOP
7 Version: K-2015.06
8 Date  : Fri Sep 6 10:02:12 2024
9 ****
10 # A fanout number of 1000 was used for high fanout net computations.
11
12 Operating Conditions: scmetro_tsmc_c1013g_rvt_ss_ip08v_125c Library: scmetro_tsmc
13 Wire Load Model Mode: top
14
15 Startpoint: UART_TX_TOP/serial/counter_reg[0]
16     (rising edge-triggered flip-flop)
17 Endpoint: Tx_OUT (output port clocked by MASTER_CLK)
18 Path Group: (none)
19 Path Type: max
20
21 Point           Incr      Path
22
23 UART_TX_TOP/serial/counter_reg[0]/CK (SDFFRX1M)    0.00  0.00 r
24 UART_TX_TOP/serial/counter_reg[0]/Q (SDFFRX1M)    0.52  0.52 r
25 UART_TX_TOP/serial/U25/Y (BUFX2M)                  0.57  1.09 r
26 UART_TX_TOP/serial/U31/Y (MX4X1M)                 0.46  1.54 f
27 UART_TX_TOP/serial/U38/Y (MX4X1M)                 0.35  1.89 f
28 UART_TX_TOP/serial/U37/Y (MX2X2M)                 0.23  2.12 f
29
30 ****
```

Check violated Paths in hold file



```
1 ****
2 Report : timing
3     -path full
4     -delay min
5     -max_paths 100
6 Design : SOC_Pipe_line_RISC_V_TOP
7 Version: K-2015.06
8 Date  : Fri Sep 6 10:02:12 2024
9 ****
10 # A fanout number of 1000 was used for high fanout net computations.
11
12 Operating Conditions: scmetro_tsmc_c1013g_rvt_ff_ip32v_m40c Library: scmetro_tsmc
13 Wire Load Model Mode: top
14
15 Startpoint: UART_TX_TOP/serial/counter_reg[4]
16     (rising edge-triggered flip-flop)
17 Endpoint: SO (output port)
18 Path Group: (none)
19 Path Type: min
20
21 Point           Incr      Path
22
23 UART_TX_TOP/serial/counter_reg[4]/CK (SDFFRQX2M)    0.00  0.00 r
24 UART_TX_TOP/serial/counter_reg[4]/Q (SDFFRQX2M)    0.54  0.54 r
25 UART_TX_TOP/serial/test_SO (serializer_DATA_WIDTH32_test_1)  ~ ~ ~
```

Check Coverage percentage

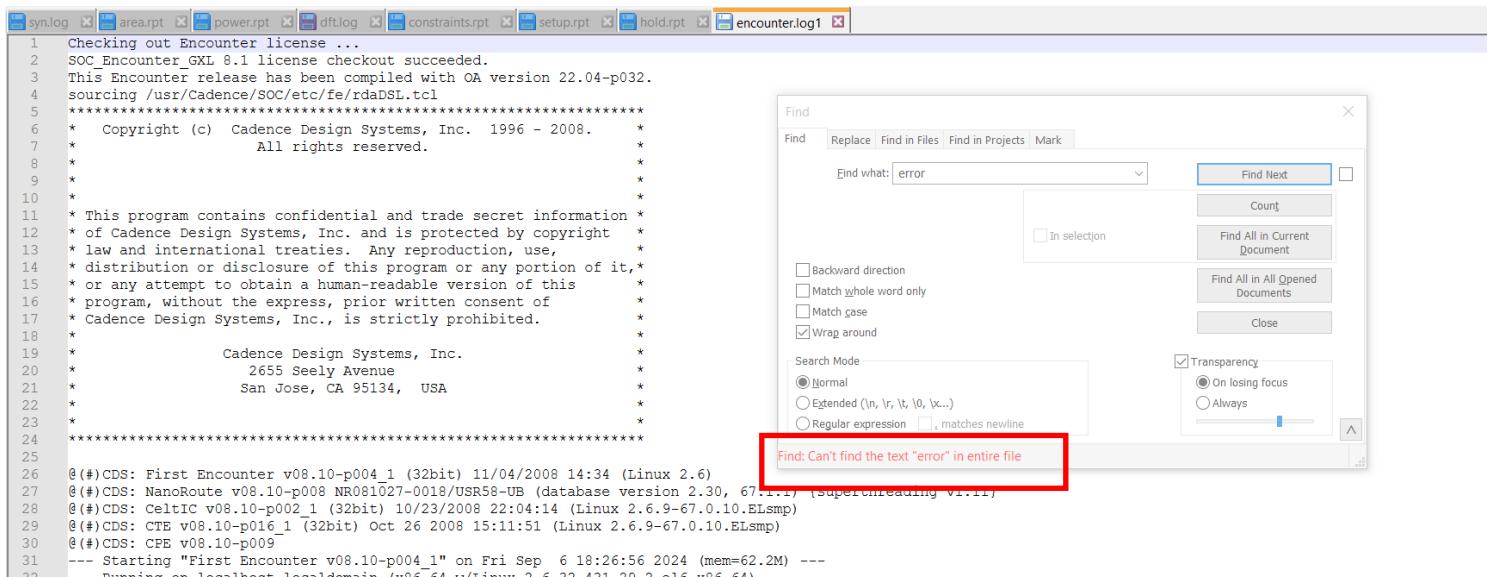


```
26065
26066 #internal patterns          0
26067 -----
26068
26069
26070     Uncollapsed Stuck Fault Summary Report
26071 -----
26072     fault class            code  #faults
26073 -----
26074     Detected              DT    329731
26075     Possibly detected     PT    0
26076     Undetectable         UD    252
26077     ATPG untestable       AU    13
26078     Not detected         ND    4
26079 -----
26080     total faults          330000
26081     test coverage          99.99%
26082
26083     Information: The test coverage above may be inferior
26084             than the real test coverage with customized
26085             protocol and test simulation library.
26086 1
26087 #####
26088 # Write out Design after initial compile
26089 #####
26090 set svf -off
```

SYSTEM PnR

Floor Plan

Check errors in after Source Design import.TCL_file after Reading all files (DFT & .lef & std_cells files) in SOC Encounter TOOL

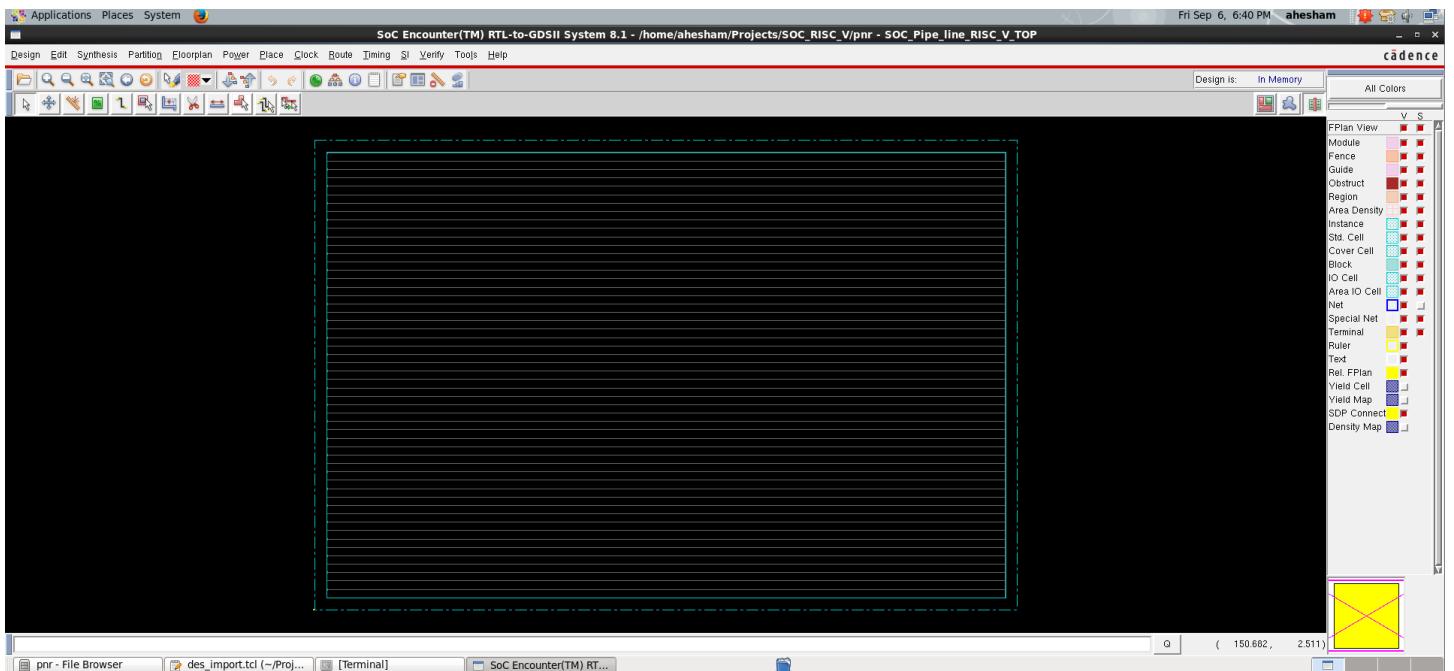


```
syn.log area.rpt power.rpt dft.log constraints.rpt setup.rpt hold.rpt encounter.log

1 Checking out Encounter license ...
2 SOC_Extractor_GXL 8.1 license checkout succeeded.
3 This Encounter release has been compiled with OA version 22.04-p032.
4 sourcing /usr/Cadence/SOC/etc/fe/rdaDSL.tcl
*****
6 * Copyright (c) Cadence Design Systems, Inc. 1996 - 2008. *
7 * All rights reserved.
8 *
9 *
10 *
11 * This program contains confidential and trade secret information *
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17 * Cadence Design Systems, Inc., is strictly prohibited.
18 *
19 * Cadence Design Systems, Inc.
20 * 2655 Seely Avenue
21 * San Jose, CA 95134, USA
22 *
23 *
24 *****
25
26 @(#)CDS: First Encounter v08.10-p004_1 (32bit) 11/04/2008 14:34 (Linux 2.6)
27 @(#)CDS: NanoRoute v08.10-p008 NR081027-0018/USR58-UB (database version 2.30, 67.1.1) (superthreading v1.11)
28 @(#)CDS: CeltIC v08.10-p002_1 (32bit) 10/23/2008 22:04:14 (Linux 2.6.9-67.0.10.ELsmp)
29 @(#)CDS: CTE v08.10-p016_1 (32bit) Oct 26 2008 15:11:51 (Linux 2.6.9-67.0.10.ELsmp)
30 @(#)CDS: CPE v08.10-p009
31 --- Starting "First Encounter v08.10-p004_1" on Fri Sep 6 18:26:56 2024 (mem=62.2M) ---
```

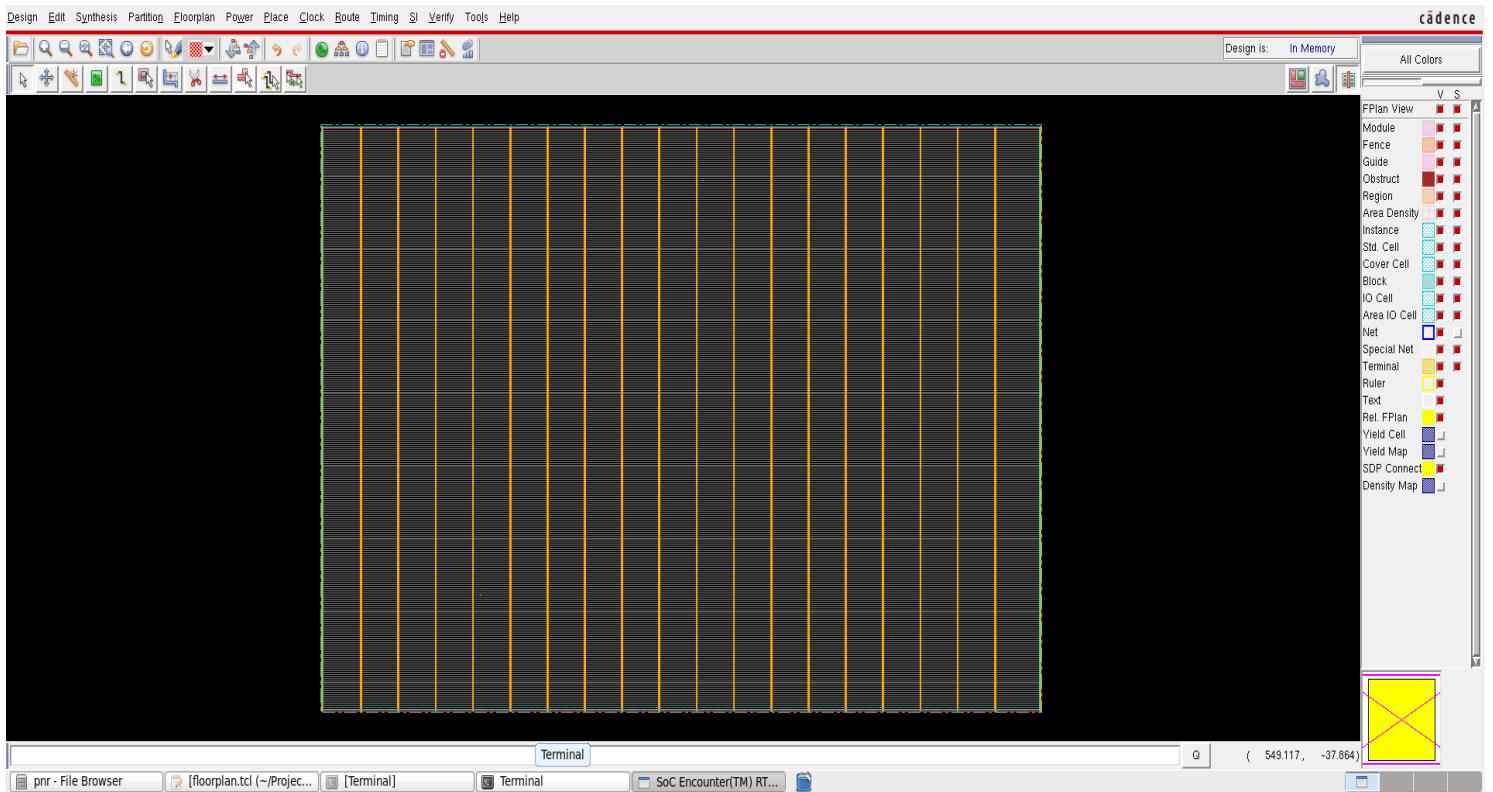
Find: Can't find the text "error" in entire file

Chip after source Floor_plan.tcl file

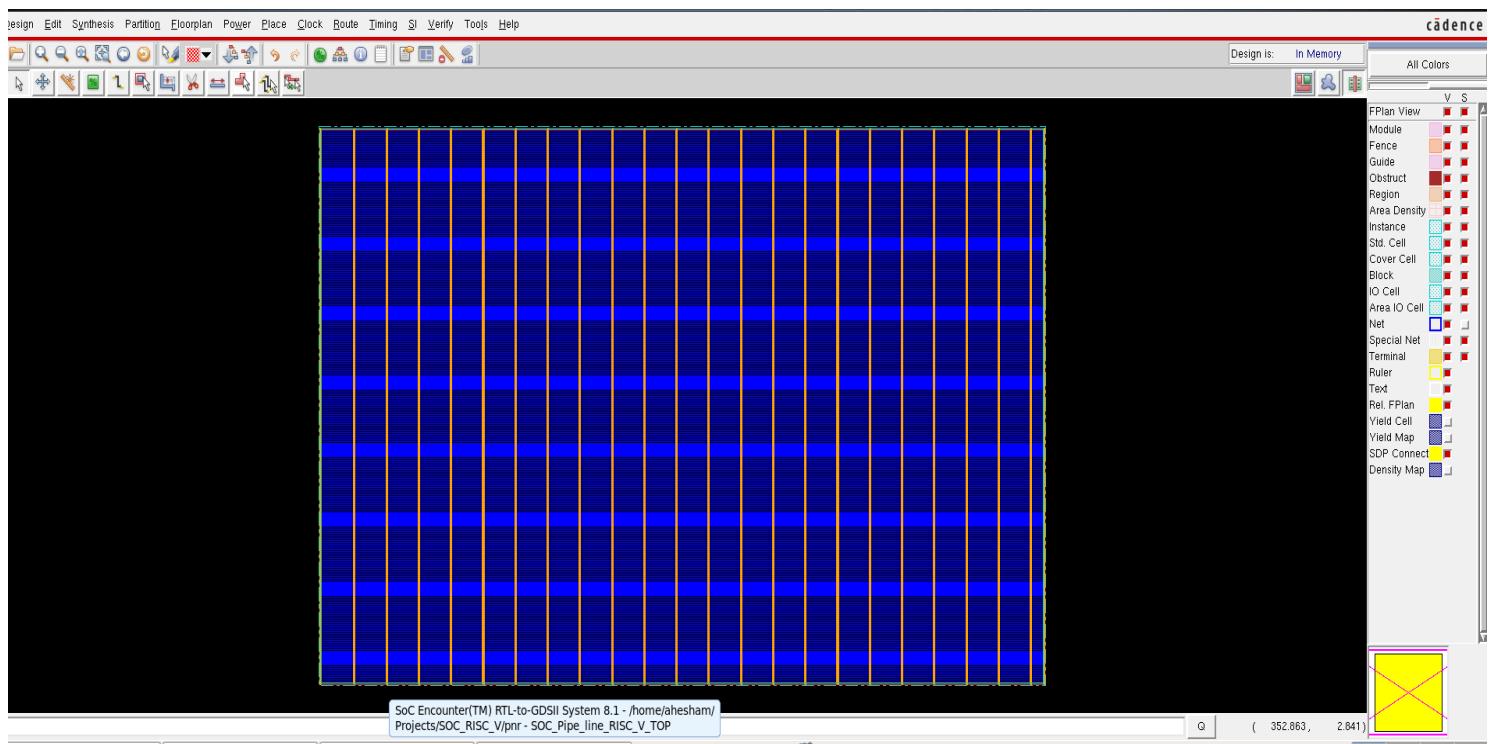


Power Plan

Chip after Adding Rings & Stripes



Chip after special routing



Checking Geometry & Connectivity

```
*** Starting Verify Geometry (MEM: 321.5) ***
```

```
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 8000
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
```

```
VG: elapsed time: 1.00
```

```
Begin Summary ...
```

```
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
```

```
End Summary
```

```
Verification Complete : 0 Viols. 0 Wrngs.
```

```
*****End: VERIFY GEOMETRY*****
```

```
*** verify geometry (CPU: 0:00:00.1 MEM: 1.0M)
```

```
***** Start: VERIFY CONNECTIVITY *****
```

```
Start Time: Fri Sep 6 19:23:41 2024
```

```
Design Name: SOC_Pipe_line_RISC_V_TOP
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (240.4700, 160.4700)
Error Limit = 1000; Warning Limit = 50
Check all nets
Net CLK: Found a geometry with bounding box (0.00,190.00) (0.20,190.20) outside
design boundary.
Violations for such geometries will be reported.
**** 19:23:41 **** Processed 5000 nets (Total 33603)
**** 19:23:41 **** Processed 10000 nets (Total 33603)
**** 19:23:41 **** Processed 15000 nets (Total 33603)
**** 19:23:41 **** Processed 20000 nets (Total 33603)
**** 19:23:41 **** Processed 25000 nets (Total 33603)
**** 19:23:41 **** Processed 30000 nets (Total 33603)
```

```
Begin Summary
```

```
Found no problems or warnings.
```

```
End Summary
```

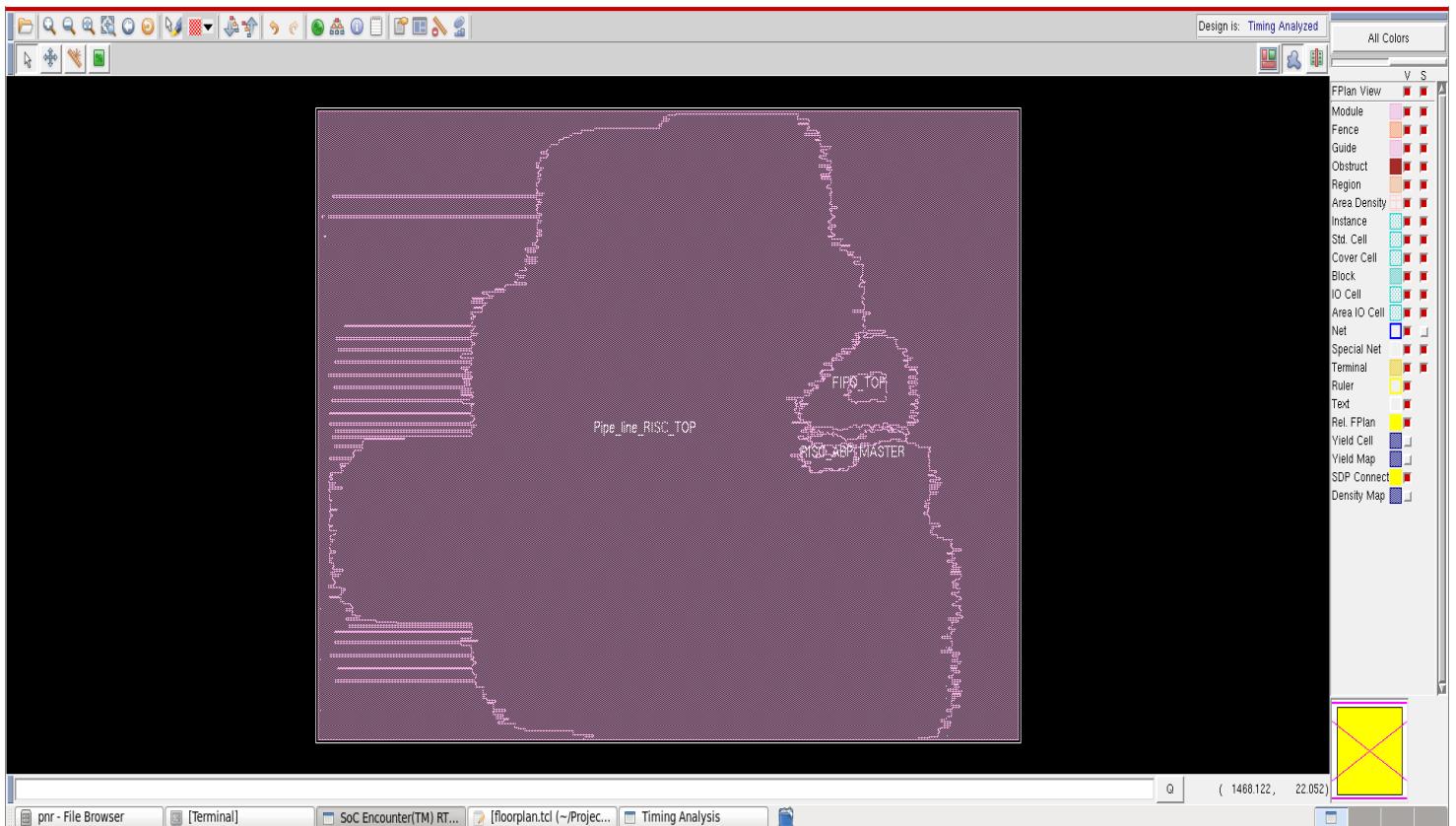
```
End Time: Fri Sep 6 19:23:41 2024
```

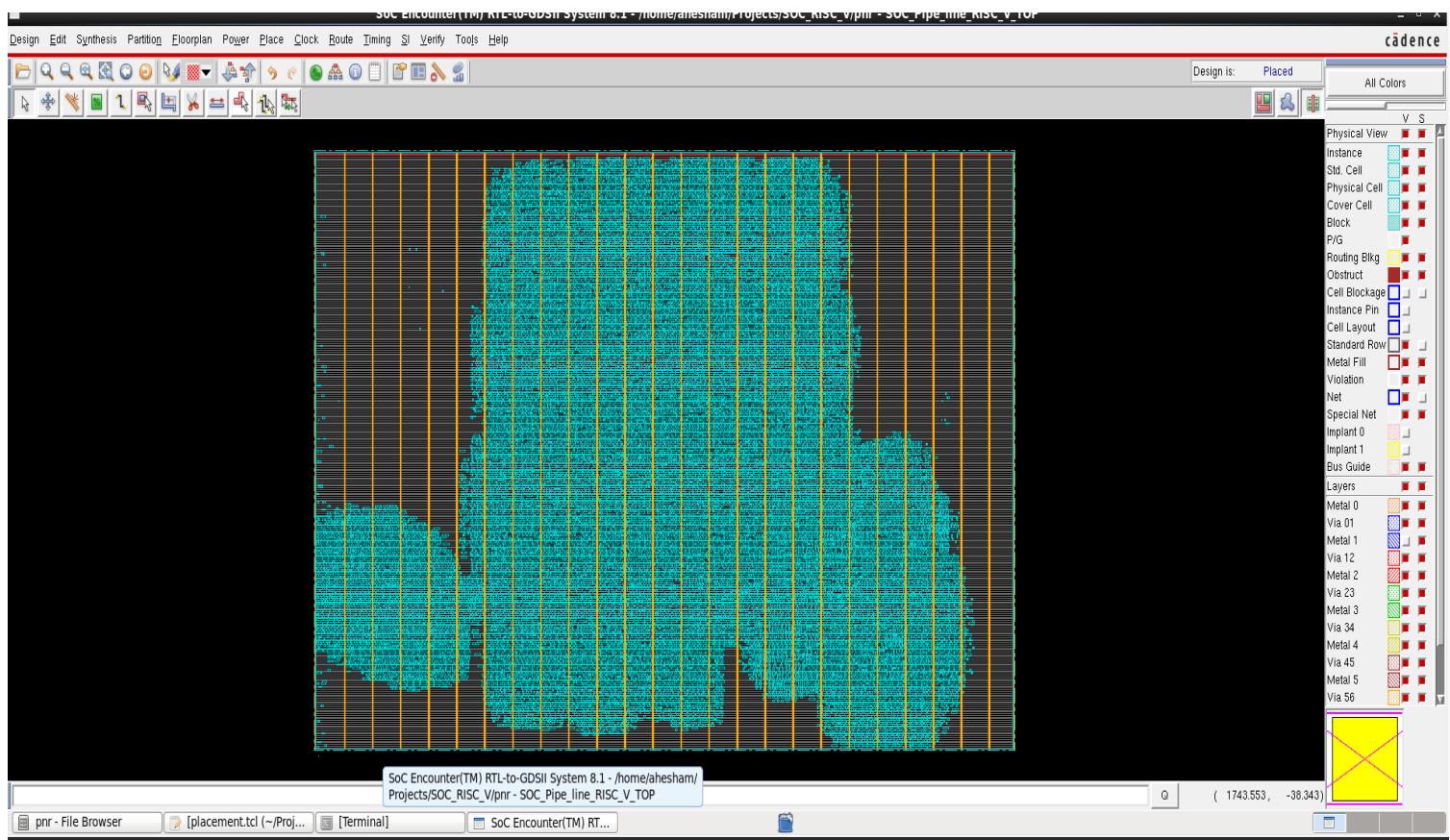
```
***** End: VERIFY CONNECTIVITY *****
```

```
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0.00.00.1 MEM: 0.00M)
```

Placement

Chip after Source Placement.tcl file





Check Timing analysis

Setup

```
timeDesign Summary

+-----+-----+-----+-----+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+-----+
| WNS (ns): | 115.371 | 984.686 | 115.371 | 161.721 | N/A | N/A |
| TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths: | 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths: | 43649 | 22369 | 22431 | 33 | N/A | N/A |
+-----+-----+-----+-----+-----+
|          Real          | Total |
|      |Nr nets(terms)| Worst Vio |Nr nets(terms)|
|      +-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 1 (1) |
| max_tran | 0 (0) | 0.000 | 1 (1) |
| max_fanout | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+
Density: 39.469%
Routing Overflow: 0.00% H and 0.05% V
```

Hold

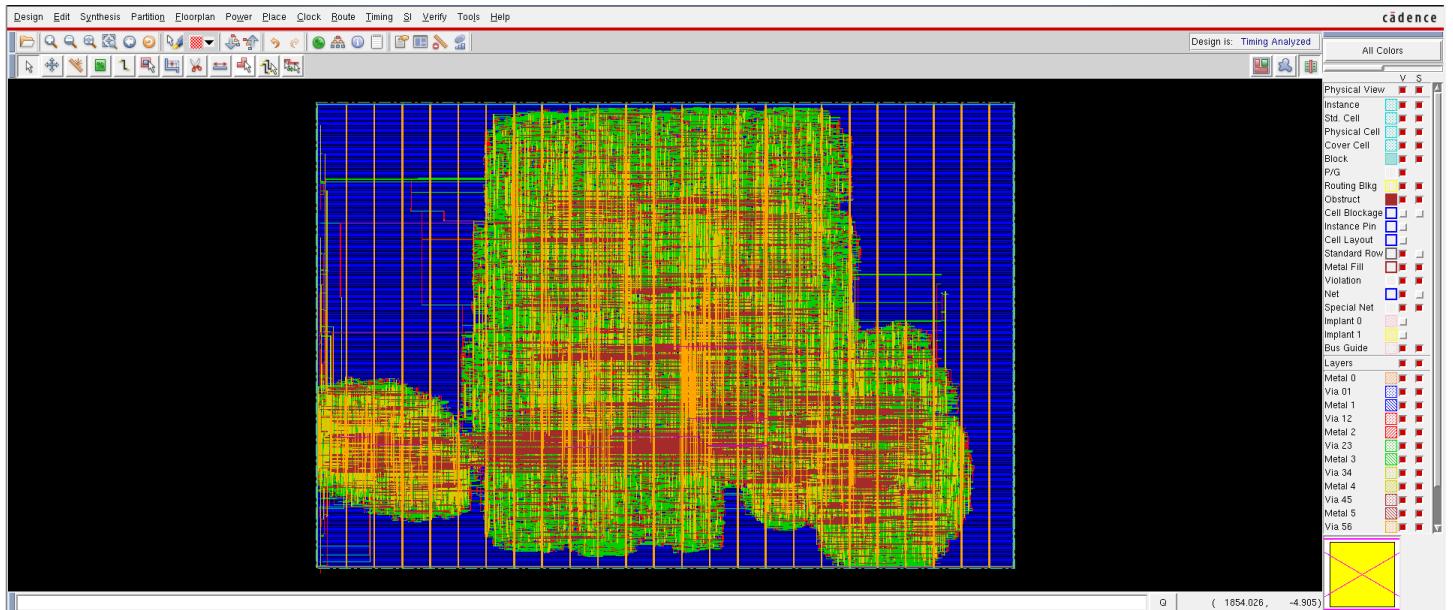
```
timeDesign Summary

+-----+-----+-----+-----+-----+
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+-----+
| WNS (ns): | 0.042 | 0.042 | 0.043 | 54.404 | N/A | N/A |
| TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths: | 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths: | 43650 | 22370 | 22431 | 33 | N/A | N/A |
+-----+-----+-----+-----+
Density: 41.478%
Routing Overflow: 0.00% H and 0.07% V
Reported timing to dir timingReports
Total CPU time: 25.14 sec
Total Real time: 26.0 sec
Total Memory Usage: 540.566406 Mbytes
encounter 4>
```

SoC Encounter(TM) RTL-to-GDSII System 8.1 - /home/ahesham/Projects/SOC_RISC_V/pnr - SOC_Pipe_line_RISC_V_TOP

CTS

Chip after Source cts.tcl file



Check Timing analysis

Setup

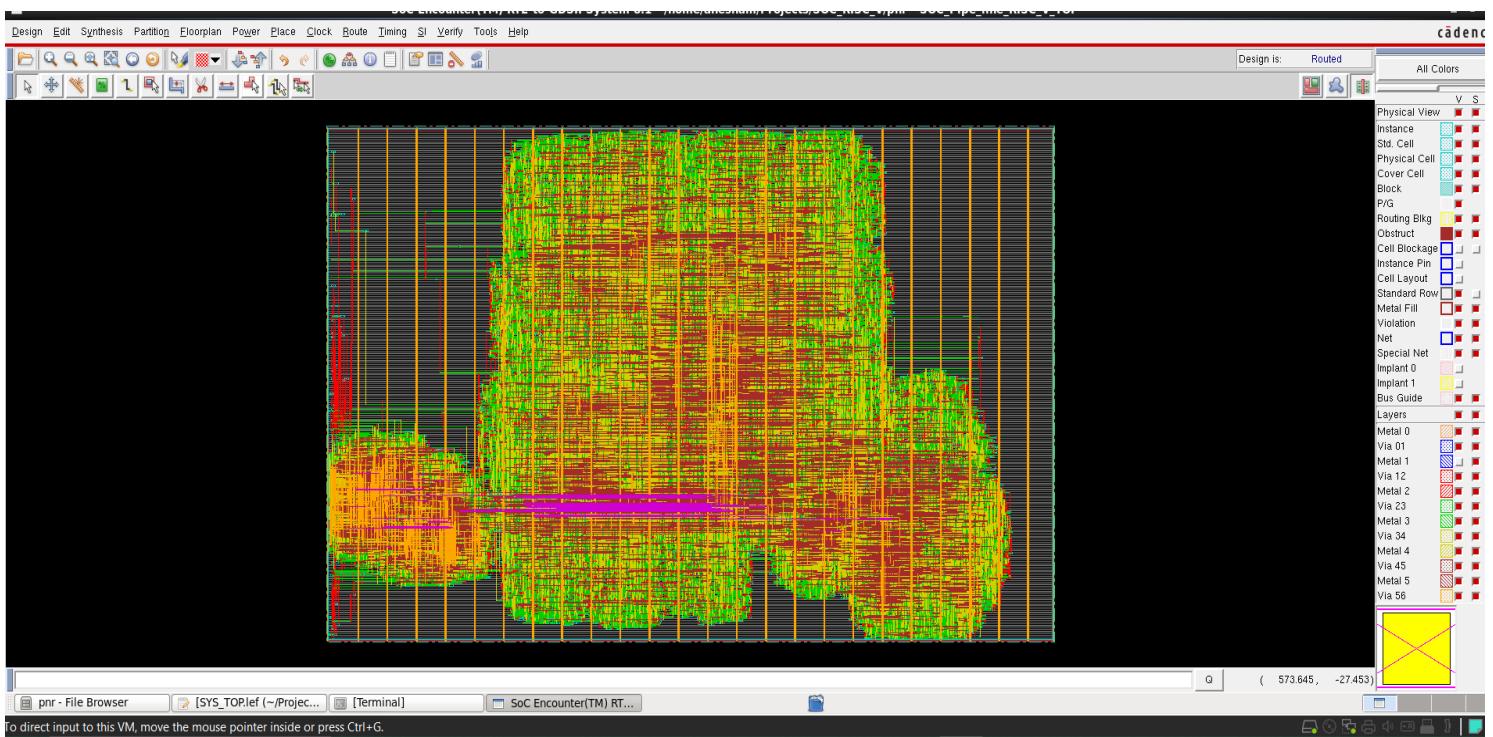
```
timeDesign Summary
+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+
| WNS (ns):| 116.872 | 984.669 | 116.872 | 160.303 | N/A | N/A |
| TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths:| 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths:| 43649 | 22369 | 22431 | 33 | N/A | N/A |
+-----+
+-----+
| DRVs | Real | Total |
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
+-----+
Density: 39.767%
Routing Overflow: 0.00% H and 0.07% V
Reported timing to dir timingReports
Total CPU time: 24.71 sec
Total Real time: 25.0 sec
Total Memory Usage: 545.71875 Mbytes
encounter 8> |
```

Hold

```
timeDesign Summary
+-----+
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+
| WNS (ns):| 0.042 | 0.078 | 0.042 | 36.006 | N/A | N/A |
| TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths:| 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths:| 43649 | 22369 | 22431 | 33 | N/A | N/A |
+-----+
+-----+
Density: 39.773%
Routing Overflow: 0.00% H and 0.07% V
Reported timing to dir timingReports
Total CPU time: 25.32 sec
Total Real time: 26.0 sec
Total Memory Usage: 582.59375 Mbytes
encounter 8> |
```

Routing

Chip after Source routing.tcl file



Check Timing analysis

Setup

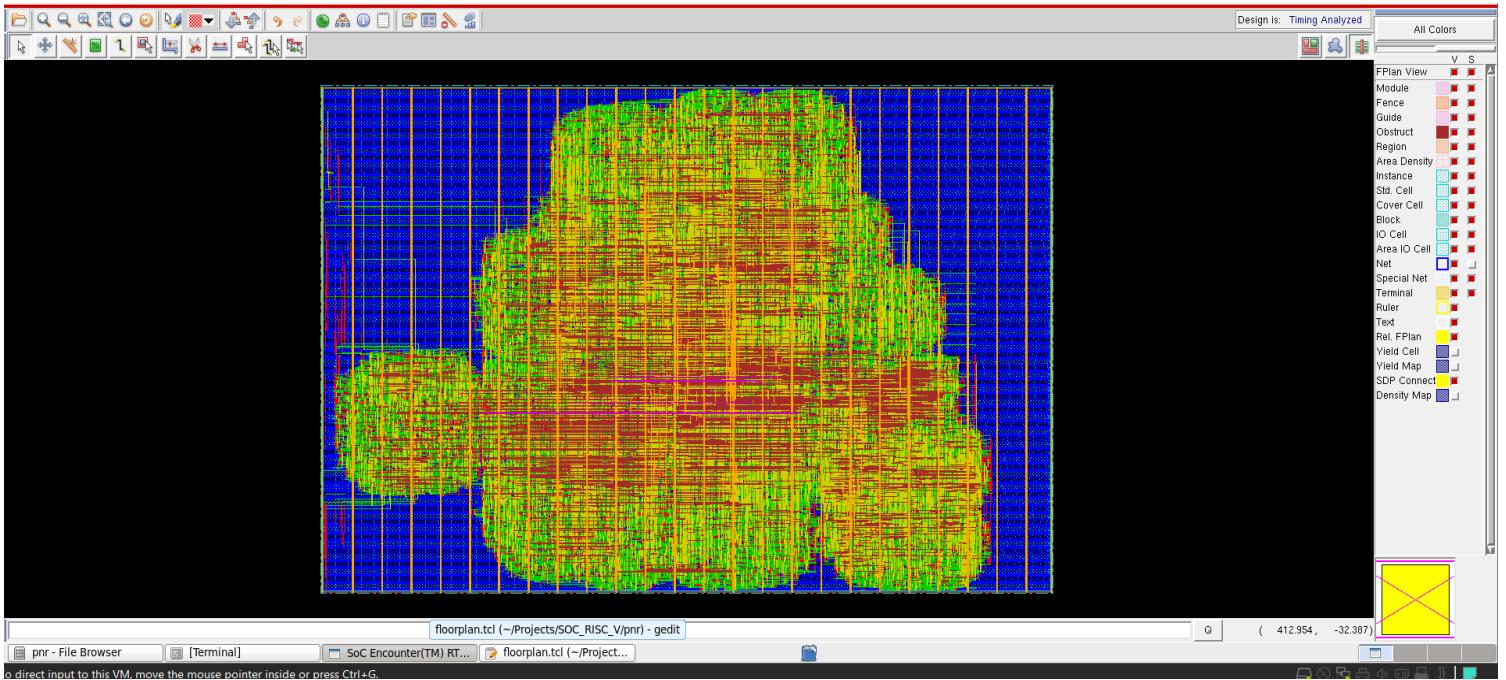
Hold

```
timeDesign Summary
+-----+-----+-----+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+
| WNS (ns):| 117.089 | 984.995 | 117.089 | 160.523 | N/A | N/A |
| TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths:| 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths:| 43649 | 22369 | 22431 | 33 | N/A | N/A |
+-----+
| DRVs | Real | Total |
|      | Nr nets(terms)| Worst Vio | Nr nets(terms)|
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
+-----+
Density: 39.773%
```

```
timeDesign Summary
+-----+-----+-----+-----+
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+
| WNS (ns):| 0.036 | 0.082 | 0.036 | 35.914 | N/A | N/A |
| TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | N/A | N/A |
| Violating Paths:| 0 | 0 | 0 | 0 | N/A | N/A |
| All Paths:| 43649 | 22369 | 22431 | 33 | N/A | N/A |
+-----+
Density: 39.773%
Reported timing to dir timingReports
Total CPU time: 23.69 sec
Total Real time: 24.0 sec
Total Memory Usage: 593.582031 Mbytes
```

Chip Finishing

Chip after Source chip_finishing.tcl file



EXPORT FILEs (GDS file /....)

