FINAL_SYSTEM_REPORT

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8//14//2024

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Wave_Forms_For_ Low Power Configurable Multi Clock Digital System

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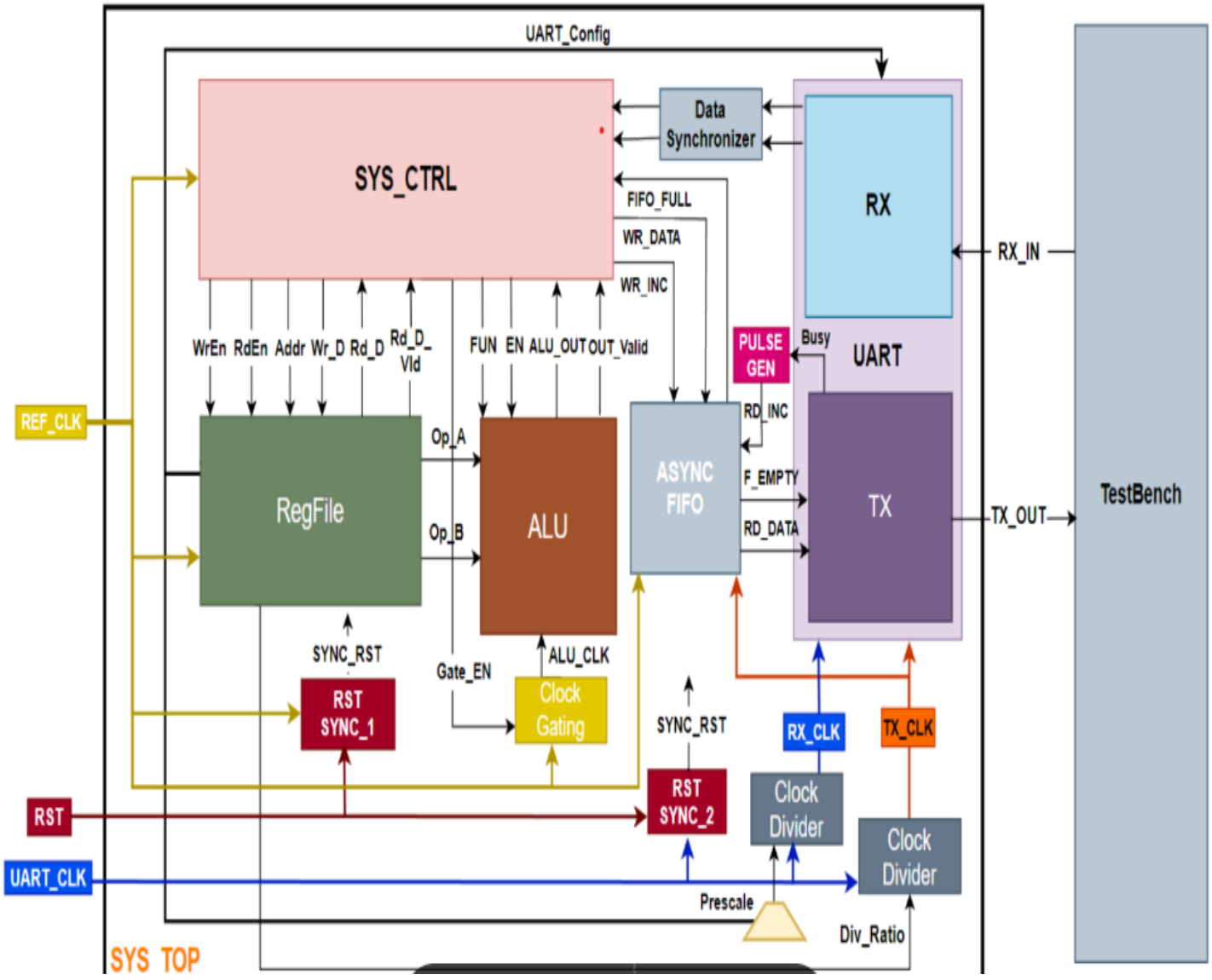
ENG: ALI-ELTEMSAH

Final System

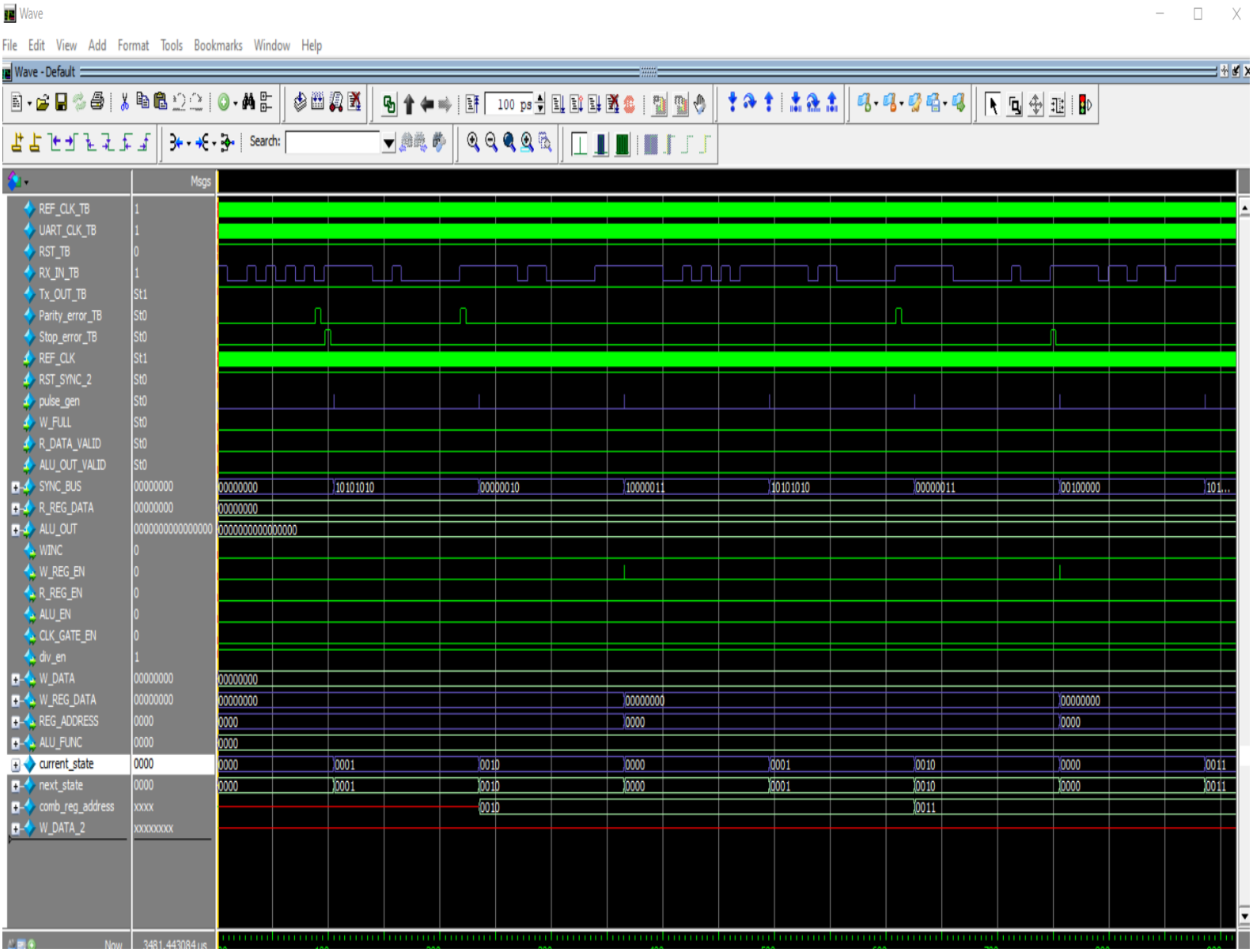


FSM_WAVE_FORM FOR UART_RX

@RESCIVNIG FIRISIT 3 FRAMES FOR WRITE OPERTION IN REG [2] (UART_CONFEG_REG) 0XAA TEHN 0X02 TEHN 0XA3 TO MAKE PAR_TYPE ODD AND PRESCALE 32

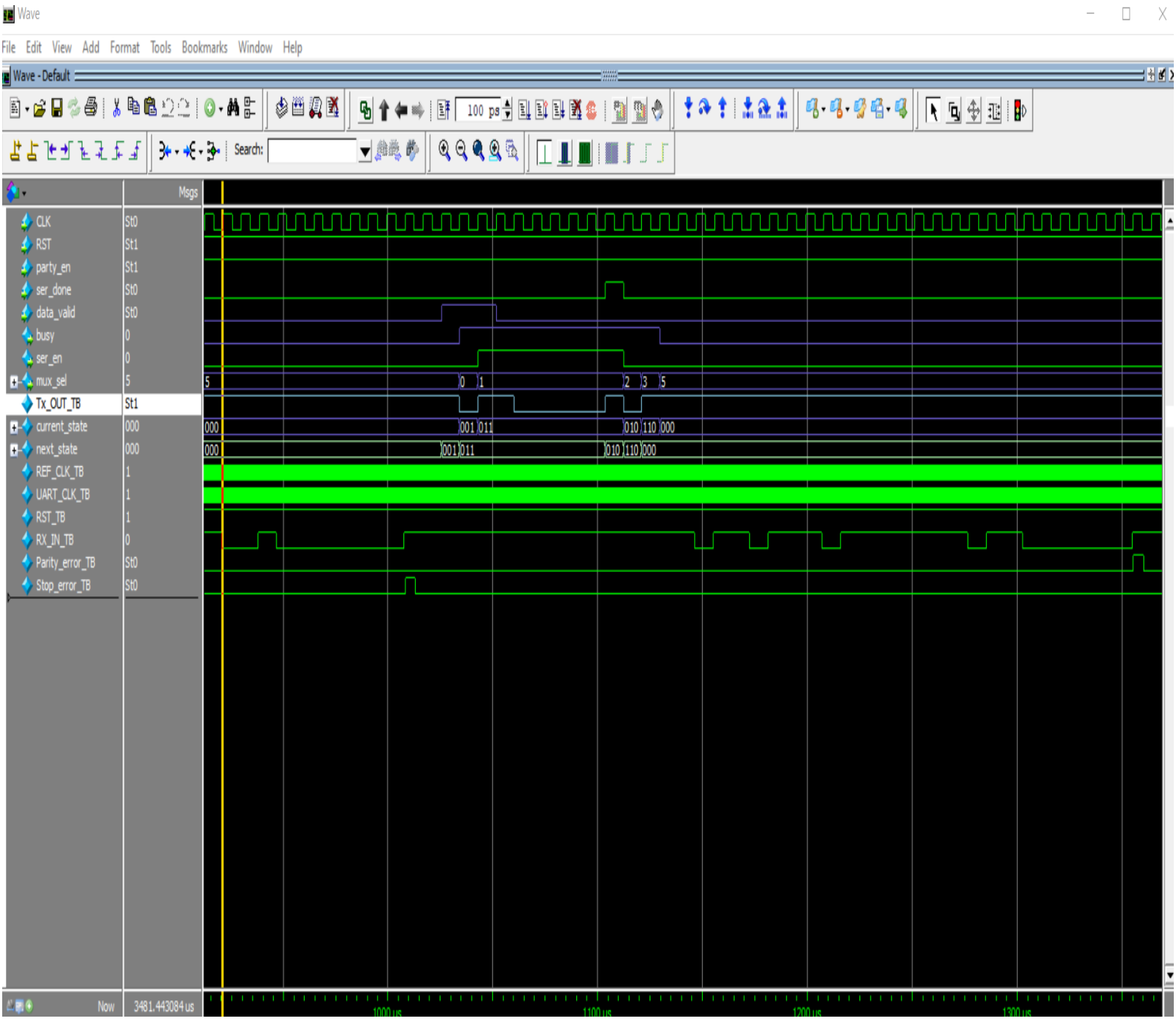
FSM_WAVE_FORM FOR SYS_CONTROL

@RESCIVNIG FIRISIT 3 FRAMES FOR WRITE OPERTION IN REG [2] // REG [3] SHOWING Transition between 3 states for W_OP idle ‘000 WRITE_DATA ‘001 PASS_DATA ‘010

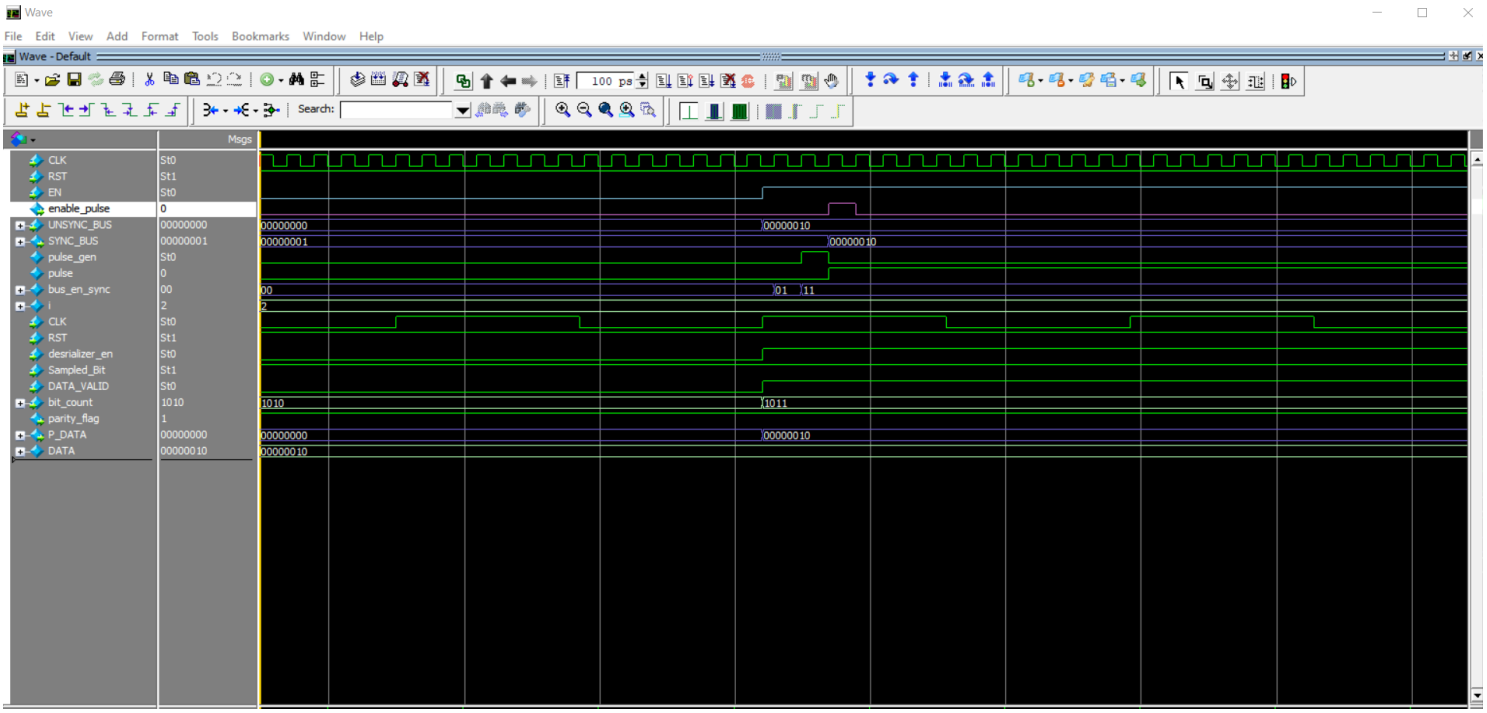


FSM_WAVE_FORM FOR UART_TX

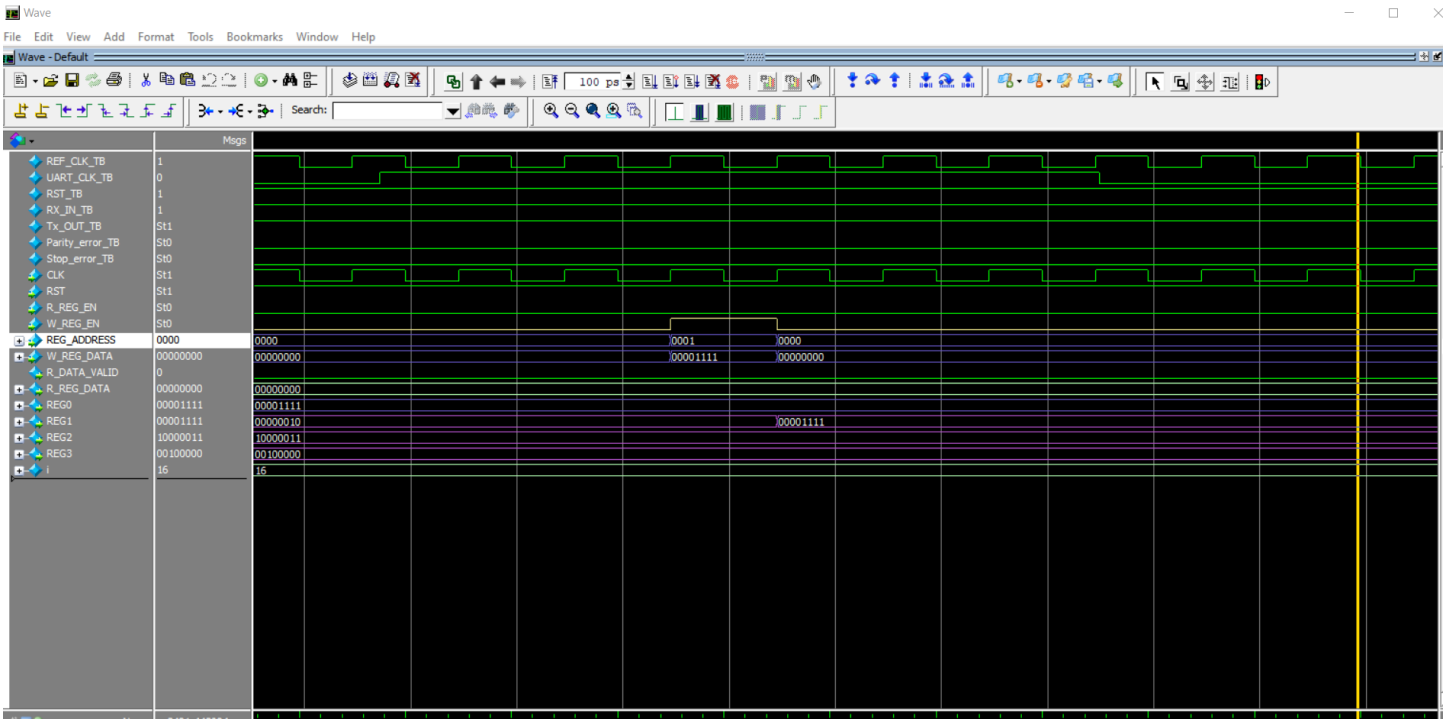
@SENDIND FRAME FOR READ OPERTION VALUE INSIDE REG [2] WHICH IS '0XA3



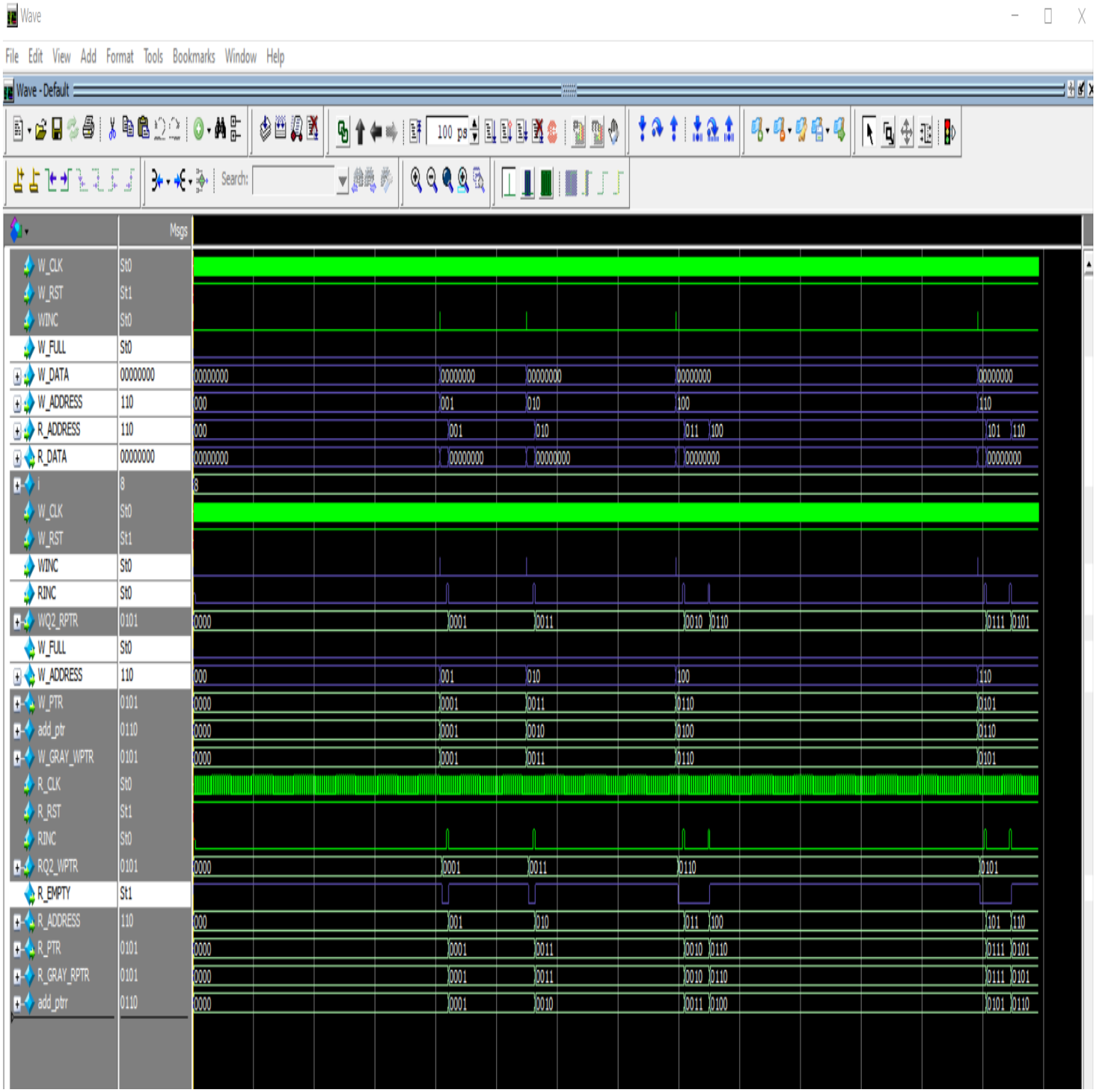
PULSE_GEN_WAVE_FORM FORM DATA_SYNC



REG_MEM_WAVE_FORM FOR REG 0/1/2/3

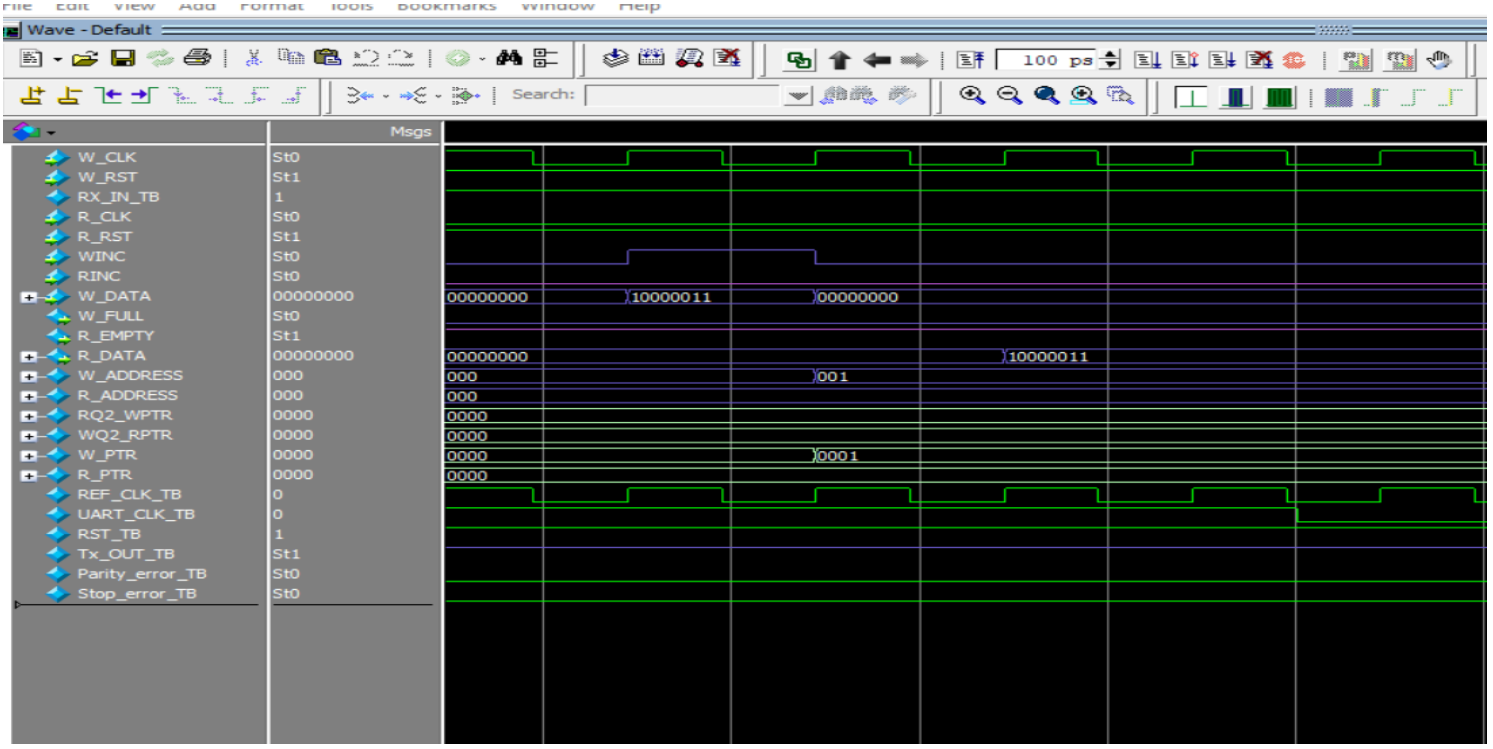


MEM_WAVE_FORM FOR FIFO

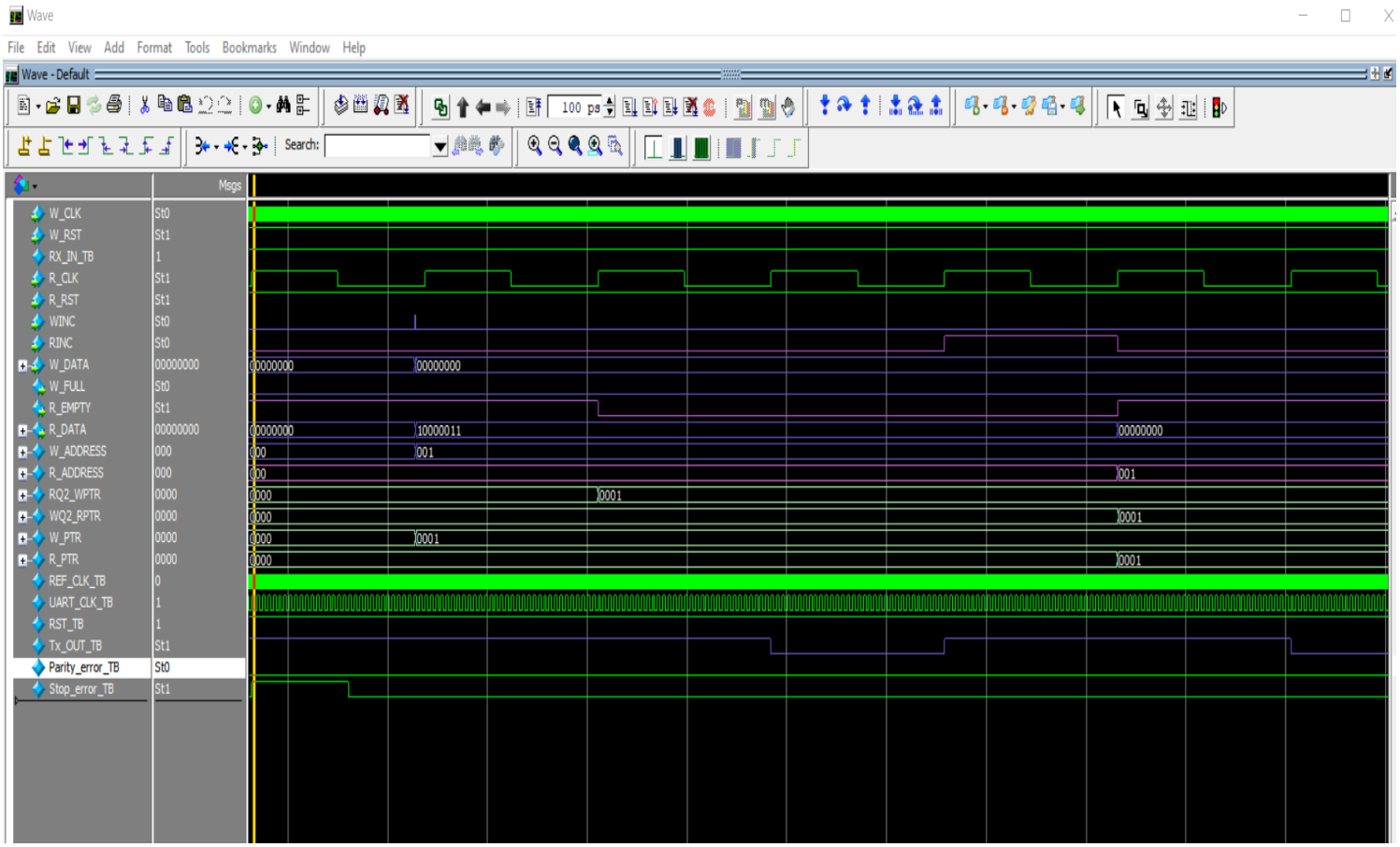


WAVE_FORM FOR WINC//W_DATA//RINC

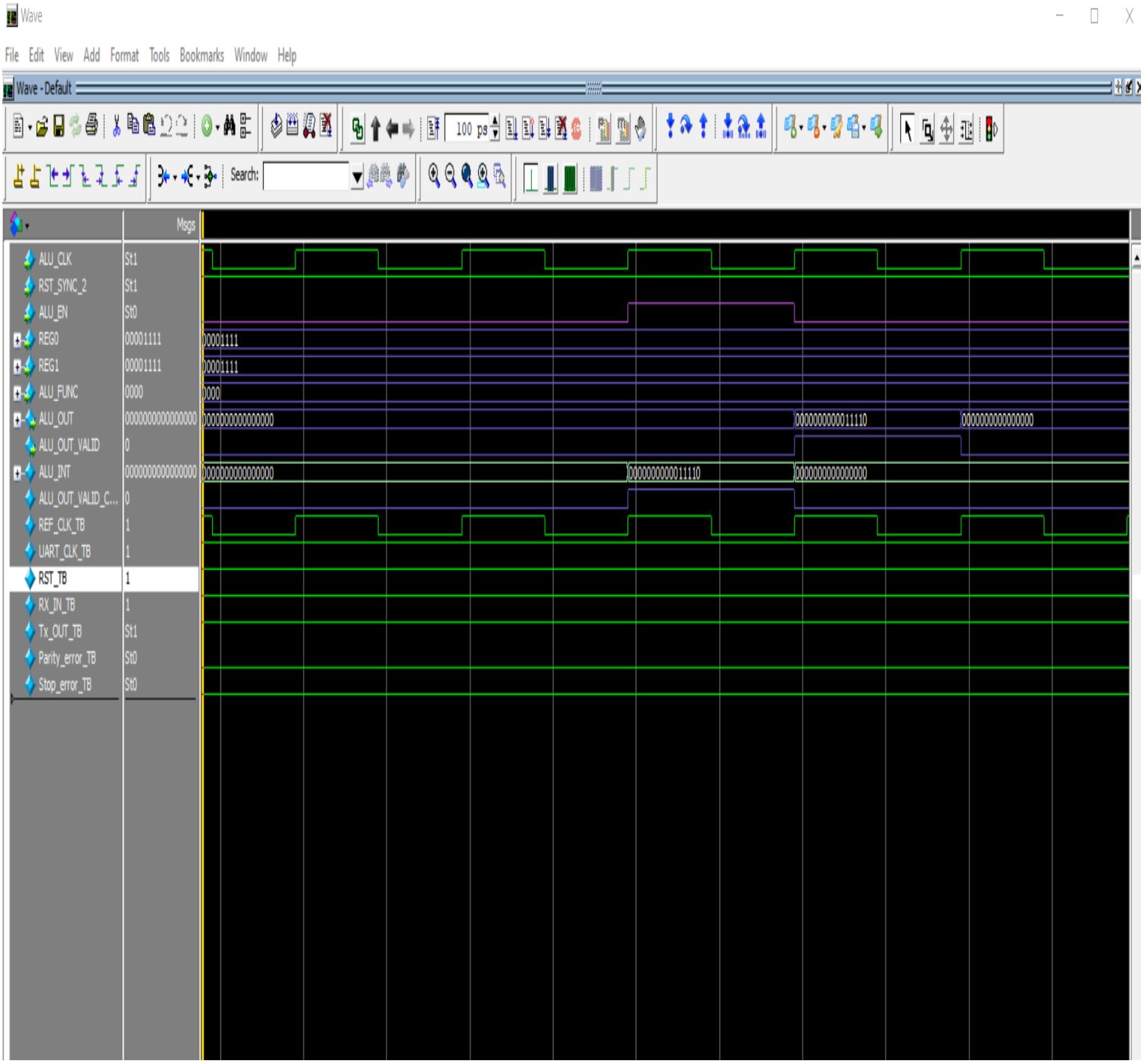
WINC && WRITE



RINC && READ



WAVE_FORM FOR ALU



Transcript snip

```
# vlog -f source_file.txt
ModelSim> do run.txt
# ** Warning: (vlib-34) Library already exists at "work".
#
# Model Technology ModelSim ALTERA vlog 10.1b Compiler 2012.04 Apr 27 2012
# -- Compiling module ALU_RTL
# -- Compiling module Bit_counter
# -- Compiling module CLK_DIV
# -- Compiling module CLOCK_GATING
# -- Compiling module Data_Sampling
# -- Compiling module DATA_SYNC
# -- Compiling module Deserializer
# -- Compiling module DF_SYNC
# -- Compiling module FIFO_BUFFER
# -- Compiling module FIFO_RD
# -- Compiling module FIFO_TOP
# -- Compiling module FIFO_WR
# -- Compiling module FSM
# -- Compiling module FSM_TX
# -- Compiling module MUX
# -- Compiling module parity_calc
# -- Compiling module Parity_Check
# -- Compiling module PRESCALE_BLOCK
# -- Compiling module PULSE_GENRATOR_BLOCK
# -- Compiling module Reg_file
# -- Compiling module RESET_SYNC
# -- Compiling module serializer
# -- Compiling module SYSTEM_CONTROL
# -- Compiling module Start_Check
# -- Compiling module Stop_Check
# -- Compiling module SYSTEM_TOP
# -- Compiling module SYSTEM_TOP_TB
# -- Compiling module SYS_UART_TOP
# -- Compiling module UART_RX_TOP
# -- Compiling module UART_TX_TOP
#
# Top level modules:
#         SYSTEM_TOP_TB
```

```
# vsim -voptargs=+accs work.SYSTEM_TOP_TB
# Loading work.SYSTEM_TOP_TB
# Loading work.SYSTEM_TOP
# Loading work.RESET_SYNC
# Loading work.PRESCALE_BLOCK
# Loading work.CLK_DIV
# Loading work.CLOCK_GATING
# Loading work.PULSE_GENRATOR_BLOCK
# Loading work.DATA_SYNC
# Loading work.SYS_UART_TOP
# Loading work.UART_RX_TOP
# Loading work.FSM
# Loading work.Bit_counter
# Loading work.Data_Sampling
# Loading work.Start_Check
# Loading work.Stop_Check
# Loading work.Deserializer
# Loading work.Parity_Check
# Loading work.UART_TX_TOP
# Loading work.serializer
# Loading work.FSM_TX
# Loading work.parity_calc
# Loading work.MUX
# Loading work.SYSTEM_CONTROL
# Loading work.Reg_file
# Loading work.ALU_RTL
# Loading work.FIFO_TOP
# Loading work.FIFO_BUFFER
# Loading work.FIFO_WR
# Loading work.FIFO_RD
# Loading work.DF_SYNC
# TEST CASE 1 WRITE OPERATION IN REG2  = 00100011 and REG3 = 00100000
# TEST CASE 2 READ OPERATION DATA inside REG2  && REG3 RESCPICTIVLY
# TEST CASE PASSED and readed data from REG_FILE = 10000011 at time              1137695
# TEST CASE PASSED and readed data from REG_FILE = 00100000 at time              1493597
# TEST CASE 3 ALU OPERATION (A + B)  A = 00000001  && B = 00000010
# Testing the Least 8 bits from ALU_OUT &&  EXPECTED_RESULT = 00000011
# Testing the Most 8 bits from ALU_OUT &&  EXPECTED_RESULT = 00000000
# TEST CASE PASSED and readed data LEST_8_BITS from REG_FILE = 00000011 at time              2214083
# TEST CASE PASSED and readed data MOST_8_BITS from REG_FILE = 00000000 at time              2214083
# TEST CASE 4 WRITE OPERATION IN REG0  = 00001111 and REG1 = 00001111
# TEST CASE 5 ALU OPERATION_WITHOUT_OPERANDS USIND DATA INSIDE REG0 && REG1 <<<  (A + B)  A = 00001111  && B = 00001111
# Testing the Least 8 bits from ALU_OUT &&  EXPECTED_RESULT = 00011110
# Testing the Most 8 bits from ALU_OUT &&  EXPECTED_RESULT  = 00000000
# TEST CASE PASSED and readed data LEST_8_BITS from REG_FILE = 00011110 at time              3455401
# TEST CASE PASSED and readed data MOST_8_BITS from REG_FILE = 00000000 at time              3455401
# Break in Module SYSTEM_TOP_TB at SYSTEM_TOP_TB.v line 83
```