UART_RX

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JULY//13//2024

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Digital IC Design

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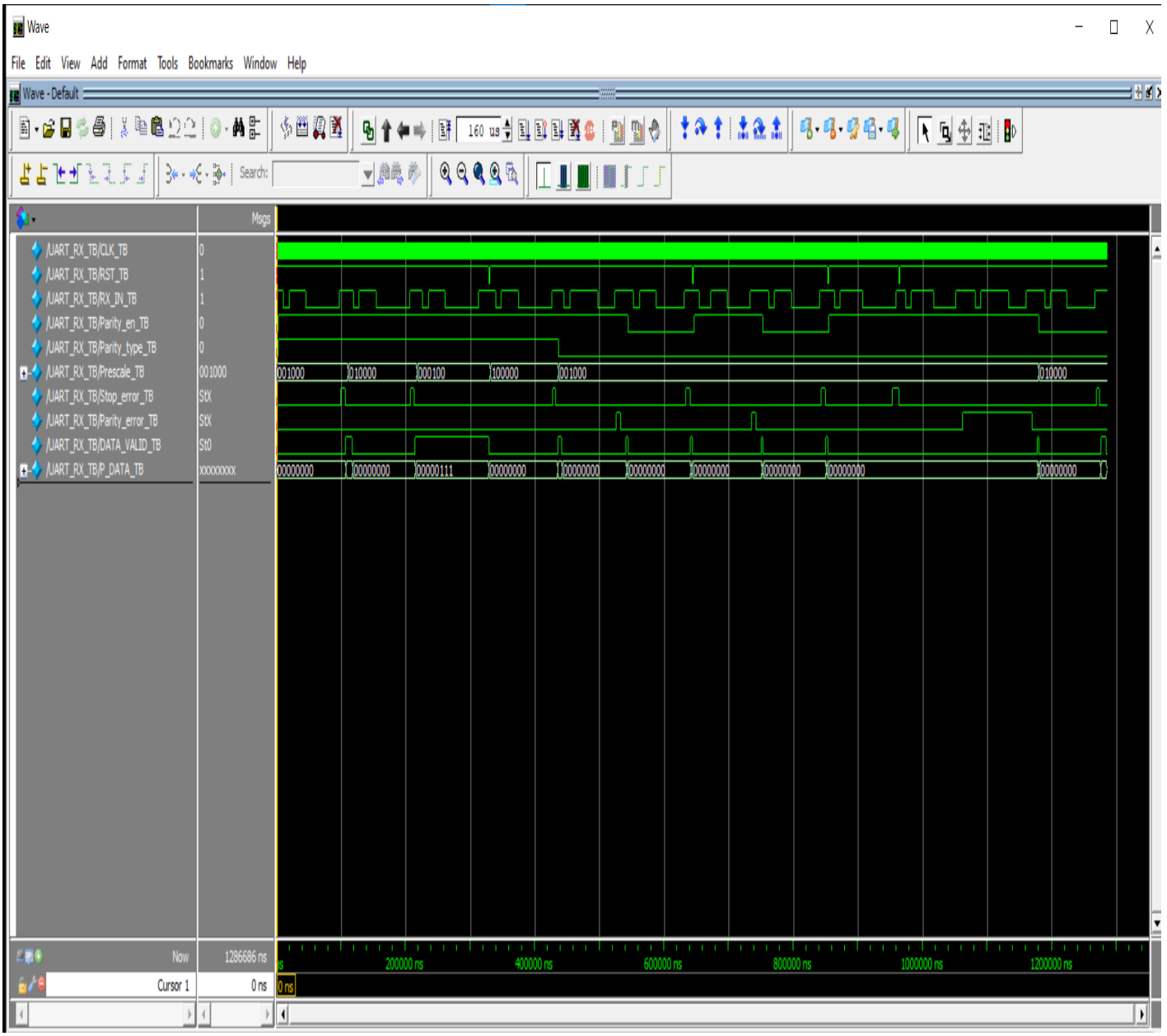
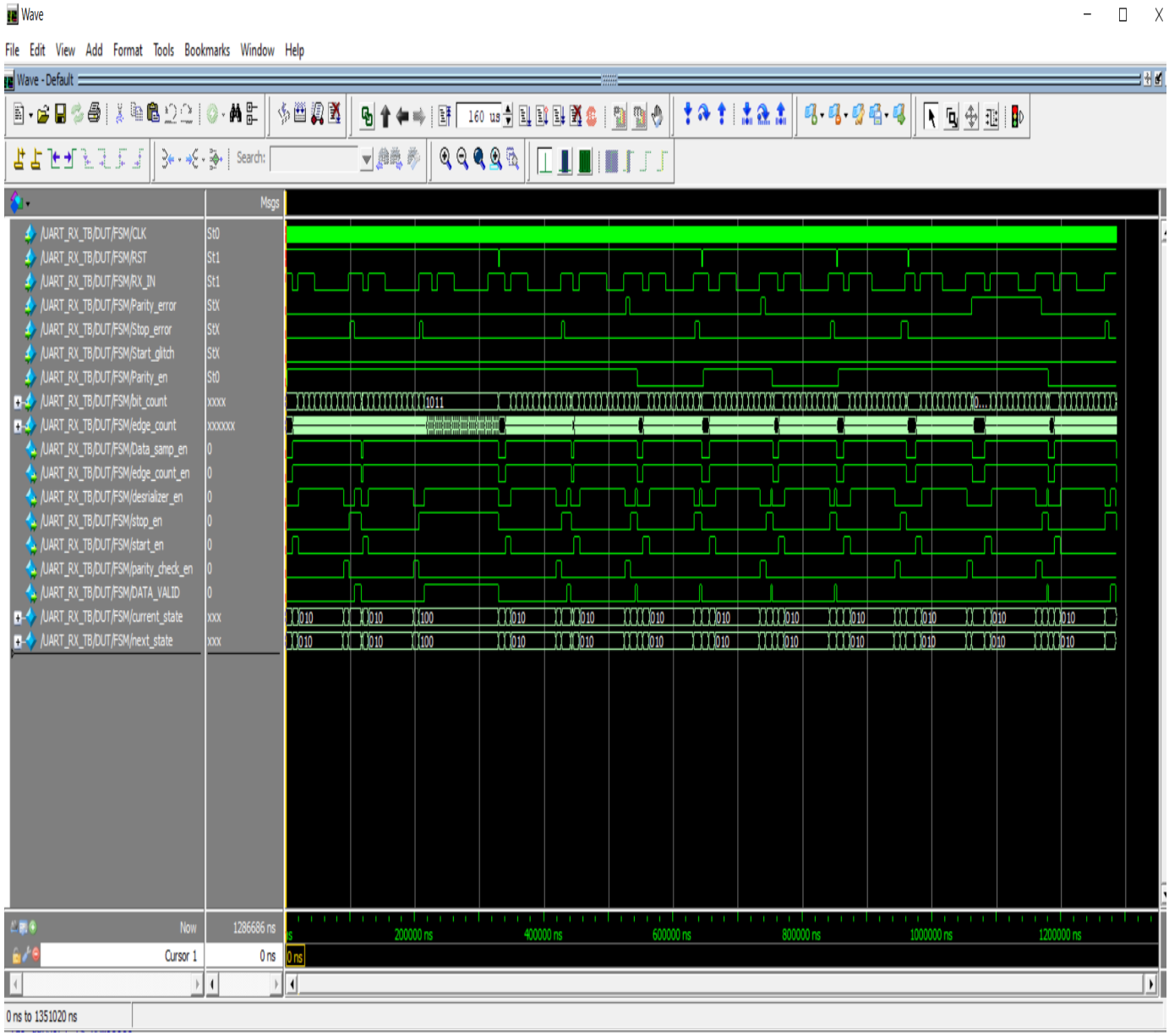
ENG: ALI EL TEMSAH

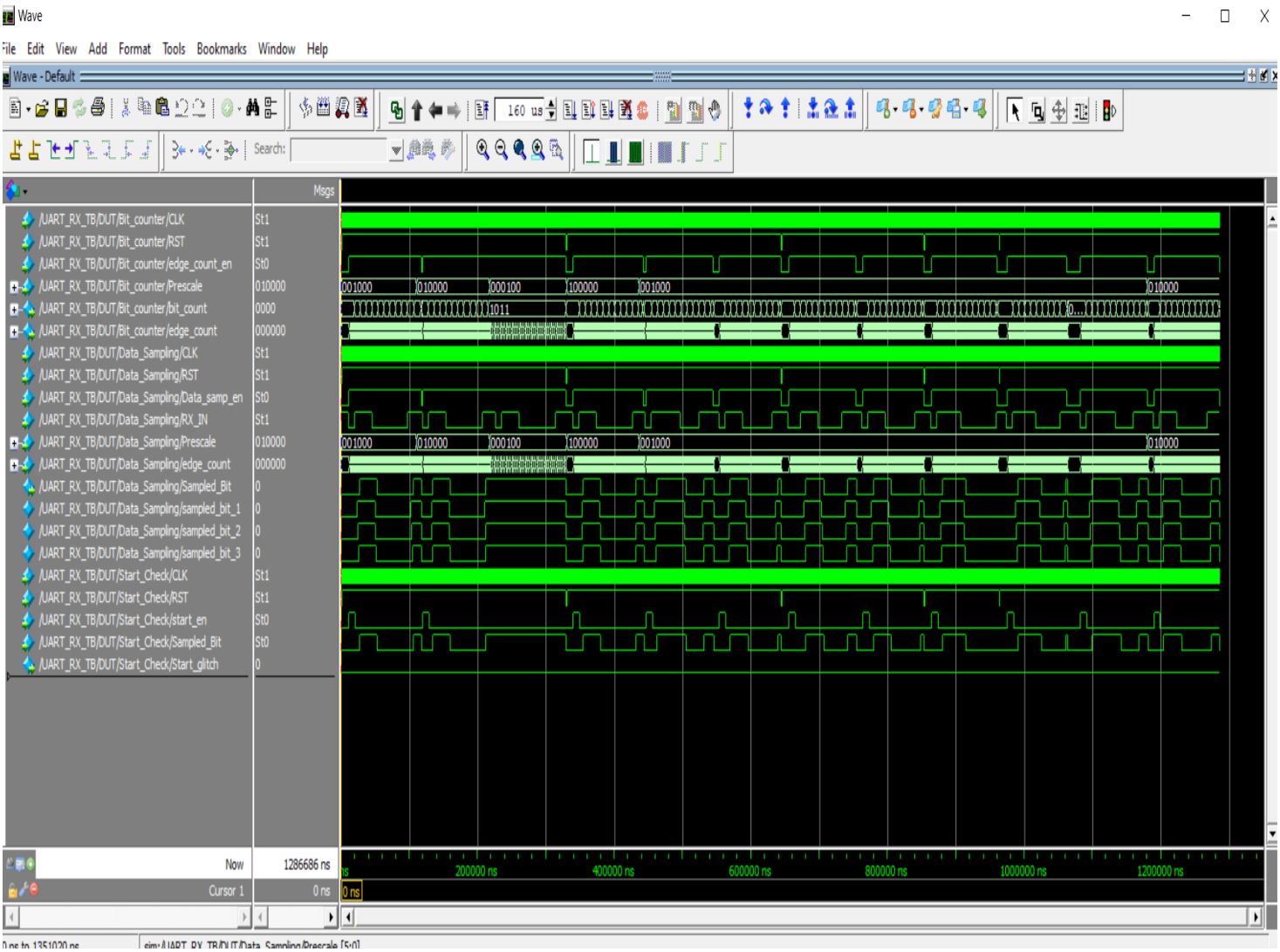
Wave form of UART_RX OUTPUTS



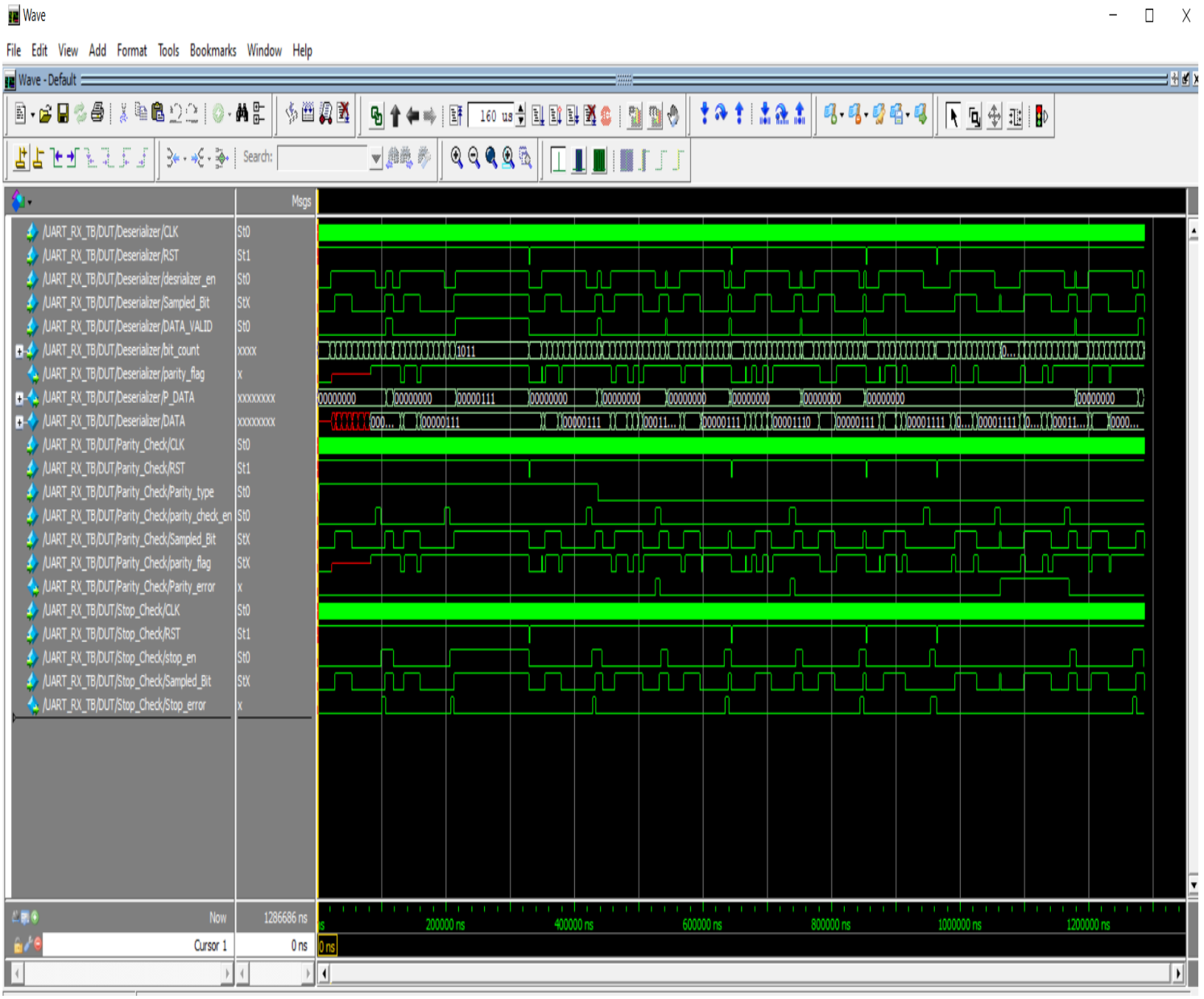
Wave form of FSM



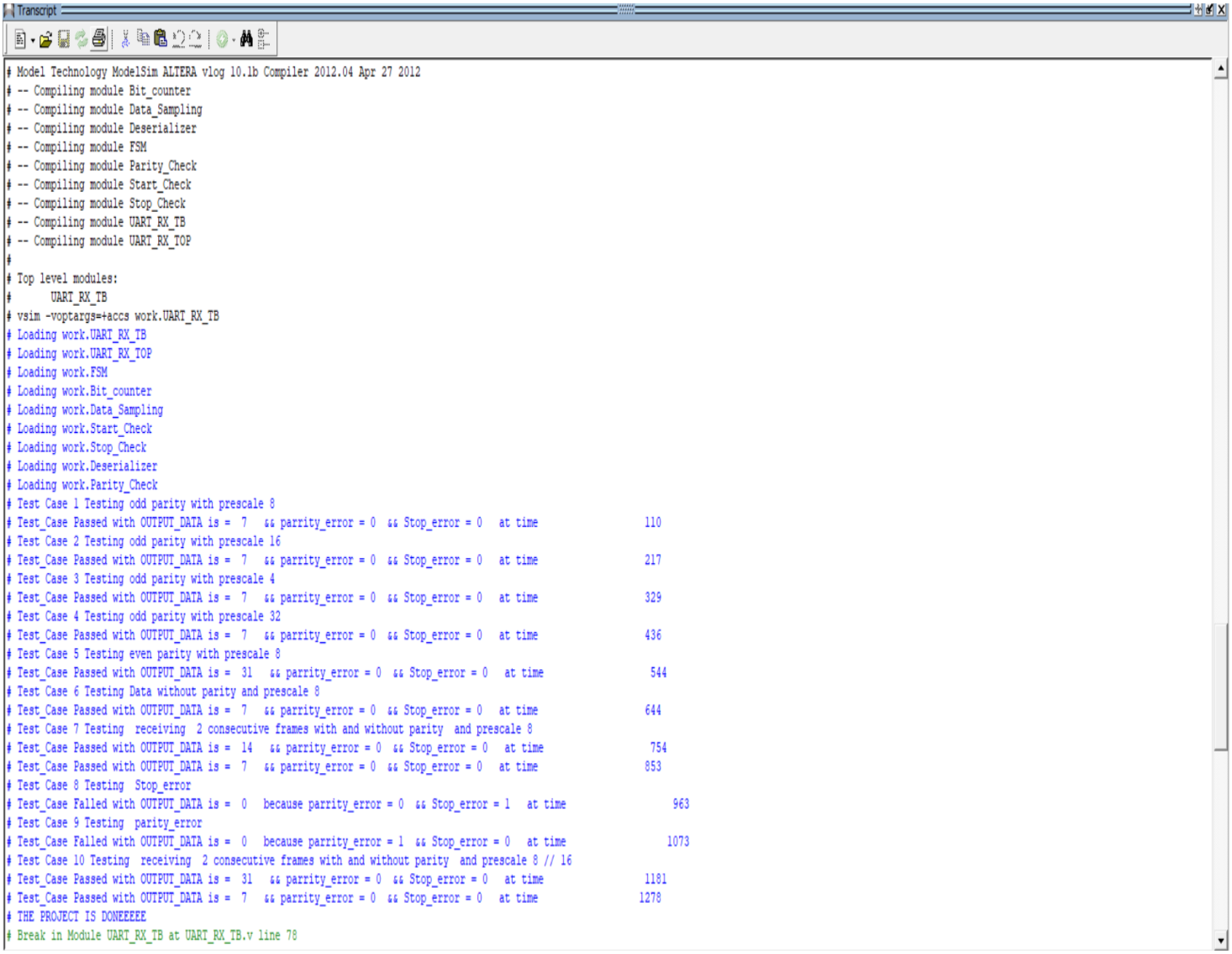
Wave form of Bit counter & Data Sampling & Start Check



Wave form of Deserializer & Parity Check & Stop Check



log window snip shot



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Transcript
# Model Technology ModelSim ALTERA vlog 10.1b Compiler 2012.04 Apr 27 2012
# -- Compiling module Bit_counter
# -- Compiling module Data_Sampling
# -- Compiling module Deserializer
# -- Compiling module FSM
# -- Compiling module Parity_Check
# -- Compiling module Start_Check
# -- Compiling module Stop_Check
# -- Compiling module UART_RX_TB
# -- Compiling module UART_RX_TOP
#
# Top level modules:
#       UART_RX_TB
# vsim -voptargs=+accs work.UART_RX_TB
# Loading work.UART_RX_TB
# Loading work.UART_RX_TOP
# Loading work.FSM
# Loading work.Bit_counter
# Loading work.Data_Sampling
# Loading work.Start_Check
# Loading work.Stop_Check
# Loading work.Deserializer
# Loading work.Parity_Check
# Test Case 1 Testing odd parity with prescale 8
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                110
# Test Case 2 Testing odd parity with prescale 16
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                217
# Test Case 3 Testing odd parity with prescale 4
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                329
# Test Case 4 Testing odd parity with prescale 32
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                436
# Test Case 5 Testing even parity with prescale 8
# Test_Case Passed with OUTPUT_DATA is =  31   && parrity_error = 0  && Stop_error = 0   at time               544
# Test Case 6 Testing Data without parity and prescale 8
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                644
# Test Case 7 Testing  receiving  2 consecutive frames with and without parity  and prescale 8
# Test_Case Passed with OUTPUT_DATA is =  14   && parrity_error = 0  && Stop_error = 0   at time               754
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                853
# Test Case 8 Testing  Stop_error
# Test_Case Falled with OUTPUT_DATA is =  0   because parrity_error = 0  && Stop_error = 1   at time                963
# Test Case 9 Testing  parity_error
# Test_Case Falled with OUTPUT_DATA is =  0   because parrity_error = 1  && Stop_error = 0   at time               1073
# Test Case 10 Testing  receiving  2 consecutive frames with and without parity  and prescale 8 // 16
# Test_Case Passed with OUTPUT_DATA is =  31   && parrity_error = 0  && Stop_error = 0   at time               1181
# Test_Case Passed with OUTPUT_DATA is =  7   && parrity_error = 0  && Stop_error = 0   at time                1278
# THE PROJECT IS DONEEEEE
# Break in Module UART_RX_TB at UART_RX_TB.v line 78
```