System Lab

You have to go through the digital backend flow including: -

- Synthesis
- Formality post-synthesis
- DFT
- Formality post-dft
- PnR
- Formality post-pnr
- GLS

Steps: -

1. Create Projects folder inside IC directory
2. Copy System folder from your computer into the virtual machine inside Projects folder
   - Synthesis Stage: -
     i. Add the following constraints in cons.tcl file.
     - Create your master clocks
       - REF_CLK (50 MHz)
       - UART_CLK (3.686 MHz)
     - Create your generated clocks
       - ALU_CLK (master_clk = REF_CLK , div_ratio = 1)
       - RX_CLK (master_clk = UART_CLK , div_ratio = 1)
       - TX_CLK (master_clk = UART_CLK , div_ratio = 32)
     - Create a clock uncertainty with 0.2 ns for setup (all master & generated clocks)
     - Create a clock uncertainty with 0.1 ns for hold (all master & generated clocks)
     - Clock Grouping
     - Input delays on all input ports except (CLK & RST) with 20% clock period
     - output delays on all output ports with 20% clock period
     - Add Buffer driving cell for all input ports
     - Add load of 0.1 pf on all output ports
     - Set operation condition using slow and fast libraries

     ii. Run synthesis and check the followings
     - No Errors, loops and latches in syn.log file
     - Check Setup timing analysis report for Violating paths
     - Check Hold timing analysis report for Violating paths
   - Formality post-synthesis Stage: -
     i. Run Formality and check it is succeeded with no failing points

- DFT Stage: -
  - i. Define a new file with name SYS_TOP_dft.v inside SYS_TOP folder
  - ii. Do the rtl preparation in SYS_TOP_dft.v including:-
    - Adding scan ports
      - SCAN_IN
      - SCAN_EN
      - SCAN_CLK
      - SCAN_RST
      - TEST_MODE
      - SCAN_OUT
    - 2. adding Muxs on clocks and resets ports
  - iii. Add the following constraints inside cons.tcl
    - 1. Add scan clock constraint using create_clock
    - 2. Add SCAN_CLK group in clock grouping command
    - 3. Input delays on all scan input ports with 20% clock period
    - 4. output delays on all scan output ports with 20% clock period
    - 5. Add set_case_analysis 1 [get_port test_mode] command to run timing analysis using scan clock
  - iv. Add all the dft sections: -
    - 1. Archirecture Scan Chains
    - 2. Define DFT Signals
    - 3. Create Test Protocol
    - 4. Pre-DFT Design Rule Checking
    - 5. Preview DFT
    - 6. Insert DFT
    - 7. Design Rule Checking post dft insertion
  - v. Run dft and check the followings
    - ○ No Errors, loops and latches in dft.log file
    - ○ Check Setup timing analysis report for Violating paths
    - ○ Check Hold timing analysis report for Violating paths
    - ○ Check dft coverage > 99 %
- Formality post-dft Stage: -
  - i. Run Formality and check it is succeeded with no failing points
- PnR Stage: -
  - i. Go through the PnR flow Using: -
    - 1. SYS_TOP.lef
    - 2. MMMC.tcl
- Formality post-pnr Stage: -
  - i. Run Formality and check it is succeeded with no failing points
- GLS: -
  - i. Run GLS using Modelsim with the following files: -

1.SYS_TOP.v (pnr netlist)
2.SYS_TOP.sdf (post-pnr sdf)
3.Verilog Library