ASYNCRONCE FIFO

8//8//2024

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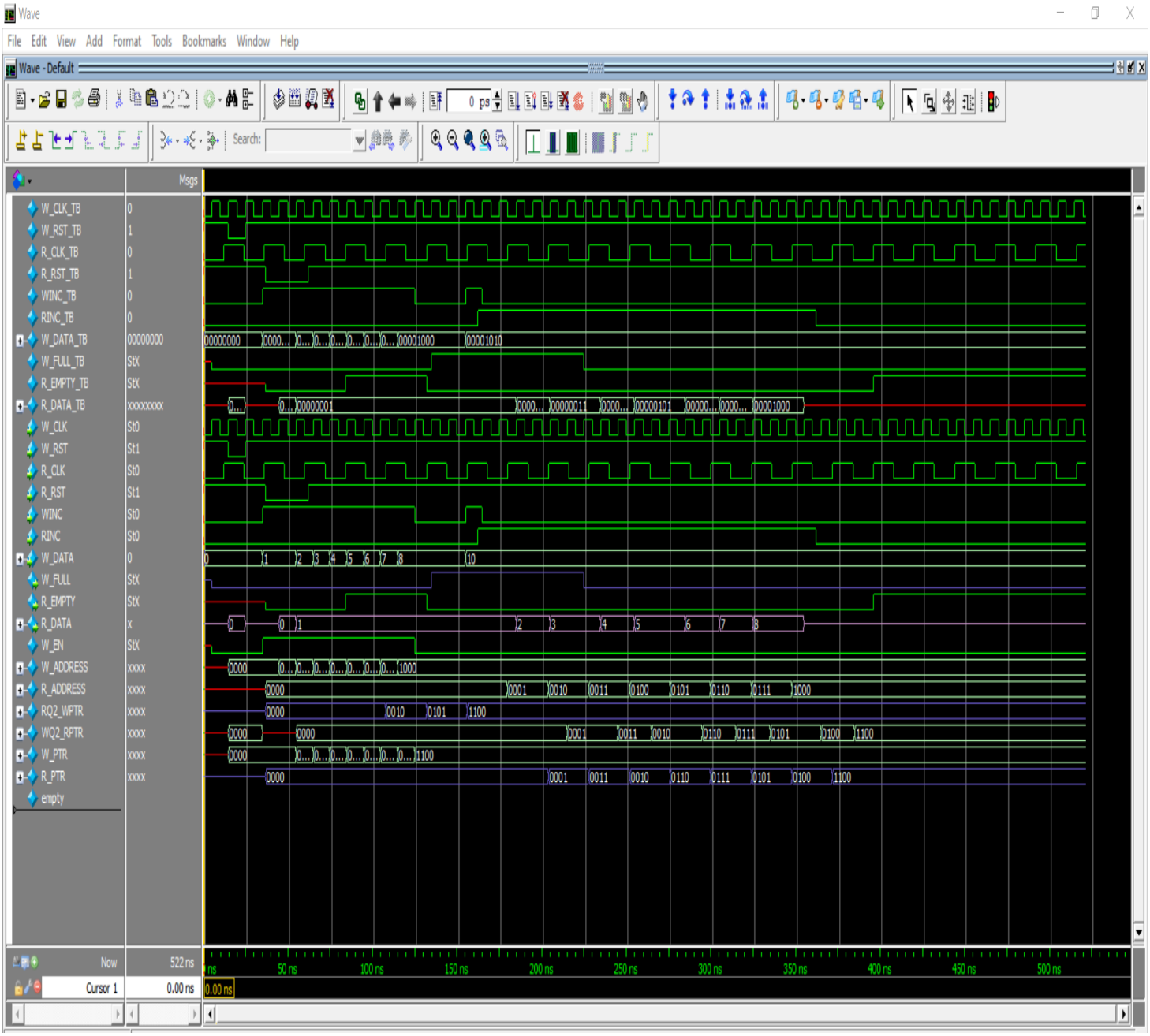
Wave form TEST READ & WRITE OPERATION AND EMPTY & FULL FLAGES



Log window snip shot

```
project open {E:/Digital Projects/ASYNC_FIFO/ASYNC_FIFO}
# Loading project ASYNC_FIFO
ModelSim> do run.txt
# ** Warning: (vlib-34) Library already exists at "work".
#
# Model Technology ModelSim ALTERA vlog 10.1b Compiler 2012.04 Apr 27 2012
# -- Compiling module DF_SYNC
# -- Compiling module FIFO_BUFFER
# -- Compiling module FIFO_RD
# -- Compiling module FIFO_TOP
# -- Compiling module FIFO_TOP_TB
# -- Compiling module FIFO_WR
#
# Top level modules:
#       FIFO_TOP_TB
# vsim -voptargs=+accs work.FIFO_TOP_TB
# Loading work.FIFO_TOP_TB
# Loading work.FIFO_TOP
# Loading work.FIFO_BUFFER
# Loading work.FIFO_WR
# Loading work.FIFO_RD
# Loading work.DF_SYNC
# TEST CASE 1 TESTING W_FULL FLAG  before sending any DATA
# Test_Case  is Succeeded with W_FULL = 0    at Time                  35
# TEST CASE 2 TESTING R_EMPTY FLAG before sending any DATA
# Test_Case  is Succeeded with R_EMPTY = 1    at Time                 87
# TEST CASE 4 TESTING W_FULL FLAG after sending 8 DATA Byetes and not reciving any one of them
# TEST CASE 3 TESTING R_EMPTY FLAG after sending  DATA
# Test_Case  is Succeeded with R_EMPTY = 0    at Time                 137
# Test_Case  is Succeeded with W_FULL = 1    at Time                 145
# TEST CASE 5 TESTING R_DATA at index zero in FIFO
# Test_Case  is Succeeded with  R_DATA =   1    at Time                162
# TEST CASE 6 TESTING R_EMPTY FLAG after reading all  DATA
# Test_Case  is Succeeded with R_EMPTY = 1    at Time                 397
# Break in Module FIFO_TOP_TB at FIFO_TOP_TB.v line 94
# Simulation Breakpoint: Break in Module FIFO_TOP_TB at FIFO_TOP_TB.v line 94
# MACRO ./run.txt PAUSED at line 7

VSIM(paused)>
```