Clock_Divider

Ziad Ahmed

JULY//13//2024

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Digital IC Design

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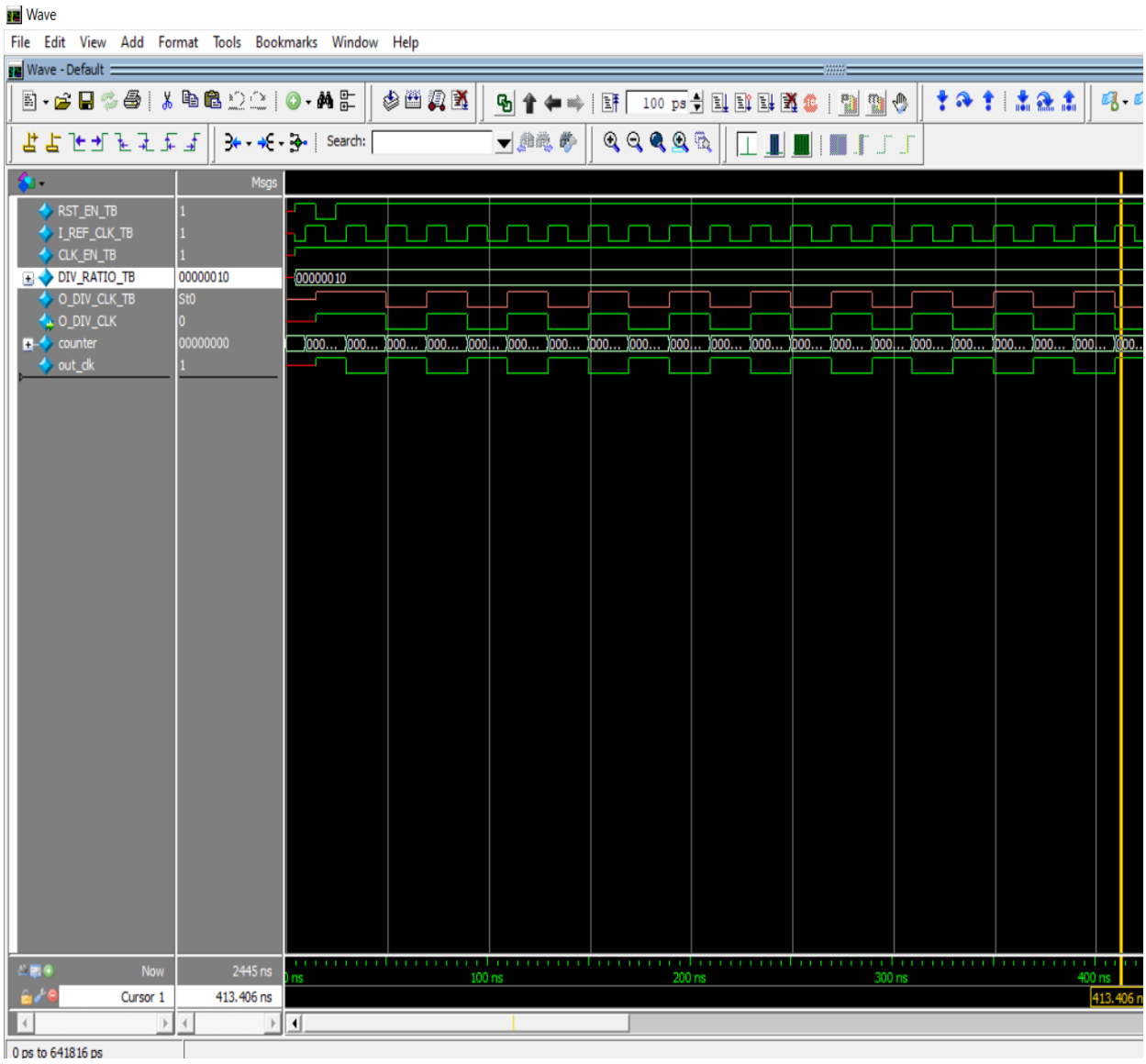
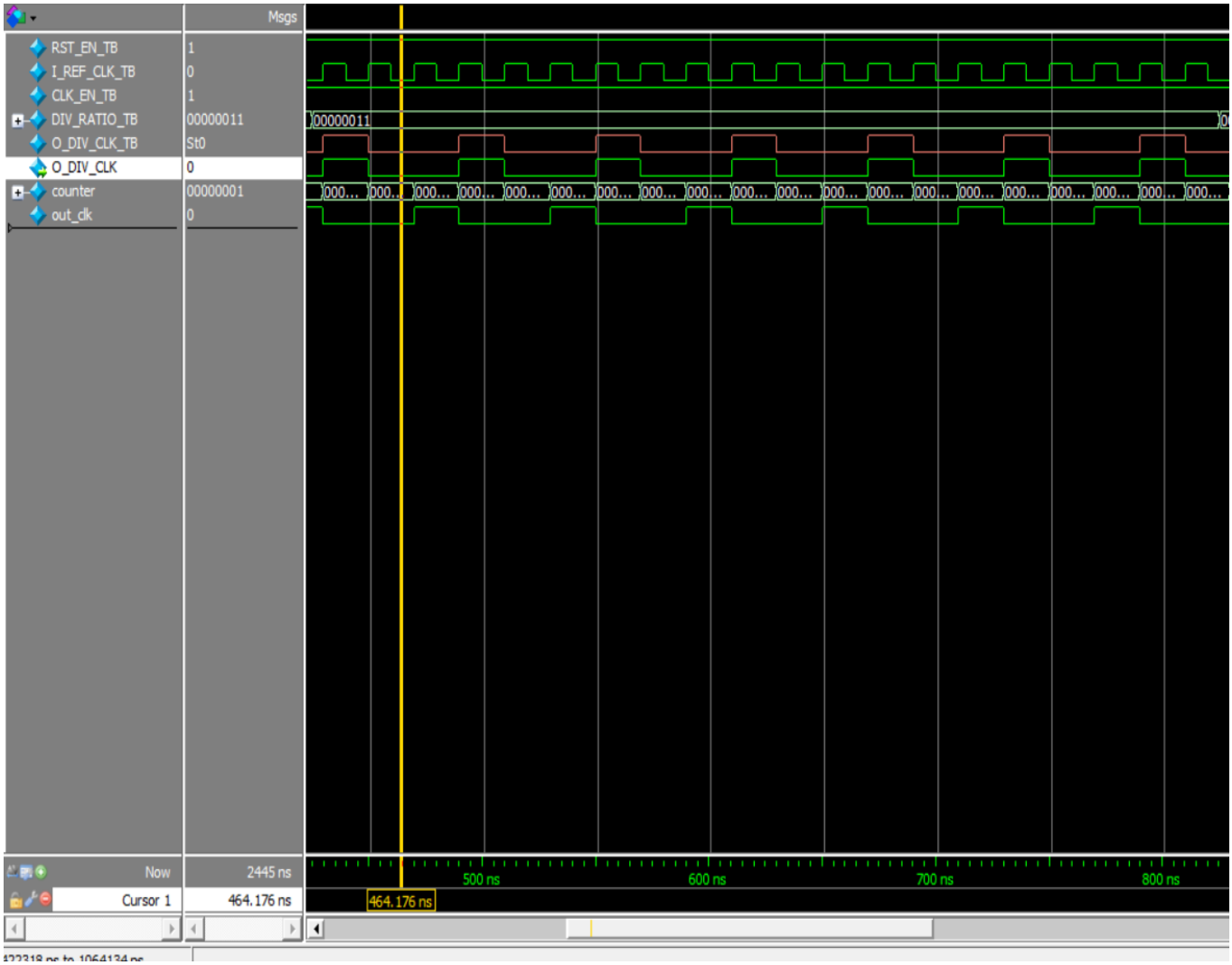
ENG: ALI EL TEMSAH

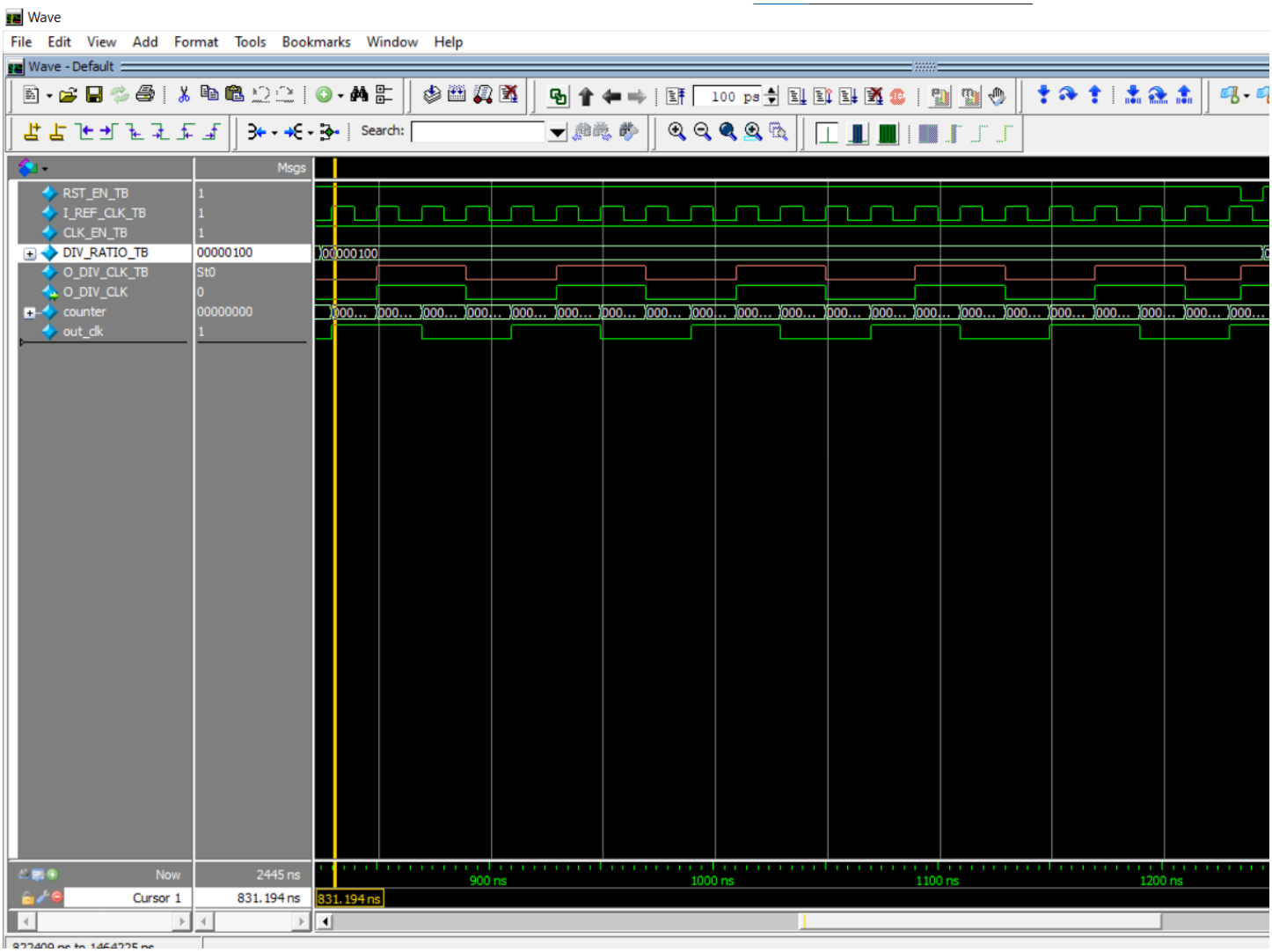
Wave form for Out at Div ratio = 2



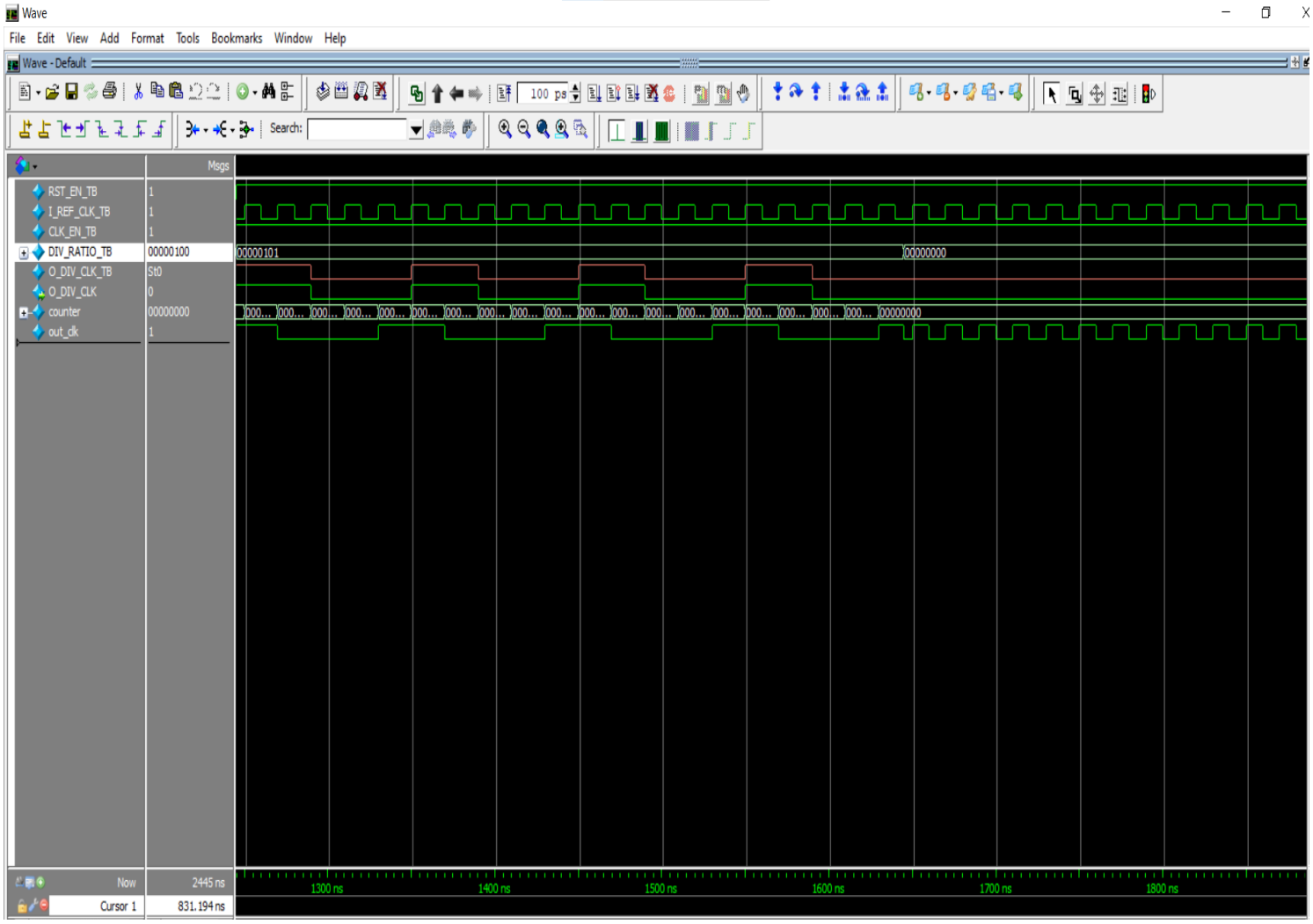
Wave form for Out at Div ratio = 3



Wave form for Out at Div ratio = 4



Wave form for Out at Div ratio = 5 && 0



log window snip shot

```
do run.txt
# ** Warning: (vlib-34) Library already exists at "work".
#
# Model Technology ModelSim ALTERA vlog 10.1b Compiler 2012.04 Apr 27 2012
# -- Compiling module CLK_DIV
# -- Compiling module CLK_DIV_TB
#
# Top level modules:
#       CLK_DIV_TB
# vsim -voptargs=+accs work.CLK_DIV_TB
# Loading work.CLK_DIV_TB
# Loading work.CLK_DIV
# Test Case   test  Divde by 2
# Test Case   Passed
# Test Case   test  Divde by 3
# Test Case   Passed
# Test Case   test  Divde by 4
# Test Case   Passed
# Test Case   test  Divde by 5
# Test Case   Passed
# Test Case   test  Divde by 0
# Test Case   Passed
# Test Case   test  Divde by 1
# Test Case   Passed
# Break in Module CLK_DIV_TB at CLK_DIV_TB.v line 60
# Simulation Breakpoint: Break in Module CLK_DIV_TB at CLK_DIV_TB.v line 60
# MACRO ./run.txt PAUSED at line 10
```