ZIANG TIAN

2004.03 ◇ Wuhan, China

My Website

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EDUCATION

Wuhan University September 2021-June 2025 (Expected)
Undergraduate student in Computer Science

- GPA: 3.94/4 Rank: 3/129 Average course score: 92.7
- TOEFL: 111 (Listening: 30 Reading: 29 Speaking: 24 Writing: 28)
- National Scholarship (top 1.5%) in 2022
- National Scholarship (top 1.5%) in 2023

RESEARCH EXPERIENCE

Reducing encryption-related memory traffic in AES-CTR memory systems April 2024 - November 2024
Collaborator/Advisor: Yuezhi Che (Wuhan University, Postdoc), Haoran Geng (Univeristy of Notre Dame, Ph.D. candidate), Dazhao Cheng (Wuhan University, Professor), Xiaobo Sharon Hu (University of Notre Dame, Professor)

- Identified three performance bottlenecks in existing AES-CTR based memory systems.
- Led the proposal of a new counter-data re-mapping scheme that allows for dynamic and local re-mapping to reduce memory traffic.
- Implemented the scheme in ChampSim simulator to assess overall performance gain over the baseline schemes.
- Submitted for ISCA 25'.

Locality-centric caching optimization for AES-CTR memory systems March 2024 - August 2024
Collaborator/Advisor: Yuezhi Che (Wuhan University, Postdoc), Haoran Geng (Univeristy of Notre Dame, Ph.D. candidate), Dazhao Cheng (Wuhan University, Professor), Xiaobo Sharon Hu (University of Notre Dame, Professor)

- Participated in developing the idea of locality-centric optimization.
- Assisted in acquisition of experimental data for graph-based applications in gem5 and with Intel Pintool.
- Submitted for HPCA 25' and entered rebuttal phase. Resubmitted for ISCA 25'.

Introduction to memory optimization for AI model training October 2023 - December 2023
Cpp, Python [Slides (In Chinese)]

- Read and presented 13 papers from 2016-2021 on AI model training memory optimization.

- Categorized different works according to their optimization methods.
- Read and researched on the source code of Pytorch concerning data dispatching.

PROJECTS

Implementation of the Raft Distributed Systems August 2024 - September 2024
Go [Code]

- Completed labs (a raft implementation without snapshot support) for MIT 6.5840: Distributed Systems, a graduate level course. Code and passed test results are provided.
- Implemented the Raft paper in Golang, in particular leader election and log replication, with full support for persistence and fault-tolerance.
- Gained experience in developing and debugging distributed systems.

A 5-level Pipelined RISC-V Processor May 2023 - July 2023
Verilog, C [Code]

- Implemented a 5-level pipelined CPU on an Artix-7 FPGA board (Nexys A7) in $\sim$ 3000 lines of Verilog in Vivado.
- Resolved data hazard and control hazard with forwarding and stalling.
- Implemented a sudoku game on the CPU (with no OS support).

Functionalities and Optimizations in xv6 OS September 2023 - October 2023
C [Code 1] [Code 2]

- Completed all 10 labs for MIT 6.S081: Operating Systems. Code and passed test results are provided.
- Researched on source codes of the xv6 OS, and implemented a series of fundamental operating system functionalities/optimizations, including copy-on-write, user-level threading, a hash-partitioned block cache for locking contention reduction, an E1000 network driver, etc. Code is available in the branches here.
- Implemented a buddy allocator for the xv6 operating system using a self-devised light-weight bit-map tree. Code is available here.

SKILLS

Computer Languages	Python, Cpp, Go, C, Javascript, Verilog, C#
Tools	Gem5 Simulator, ChampSim Simulator
Others	Latex