Preliminary RISC-V HFI Spec (v1)

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Chapter 1. Purpose

Hardware-assisted fault isolation (HFI) is a hardware extension that supports in-process isolation (sandboxing) of unmodified native binary code and also integrates into existing software based fault isolation (SFI (Wahbe et al., 1993)) based sandboxing systems, systems such as WebAssembly (Haas et al., 2017) and Google's Ubercage (Google Chrome's v8 JIT sandbox (saelo, 2021)), to improve their performance, security, and scalability (Narayan et al., 2023).

HFI aims to provide all the capabilities needed for secure sandboxing, namely data and control flow isolation as well as complete and efficient mediation of privileged instructions (i.e. system calls). This specification describes the functional properties of HFI on RISC-V, a more complete description of the background and motivation for HFI is presented in a paper published at ASPLOS 2023 (Narayan et al., 2023).

Chapter 2. Overview

HFI mode HFI adds a new processor mode (HFI mode). If HFI is enabled, code running on a hart is "sandboxed", i.e, execution is restricted according to: (a) a set of region registers, that grant access to memory (see Section on Regions), (b) a register with the sandbox exit handler, where system calls and sandbox exits are redirected to (see Section on Exit Handler), and (c) a register with sandbox option flags that modify sandbox semantics (see Section on Sandbox Setup). HFI's mode and region registers operate on a per-hart basis; they are not synchronized across harts.

For convenience, we refer to the code using HFI to sandbox other code as the *sandboxing runtime*. With a few exceptions (Section on OS Integration), HFI is enabled when a sandboxing runtime executes an `hfienter` instruction, and disabled when sandboxed code executes an `hfiexit` instruction, which transfers control back to the sandboxing runtime. The runtime is responsible for saving and restoring context appropriately, and can use HFI to multiplex many sandboxes across harts, scheduling them as it sees fit. HFI enables sandboxing through two mechanisms:

Interposition HFI supports interposition on all paths out of the sandbox including when a sandbox exits (through the `hfiexit` instruction), system calls---and by extension, signals. Thus, a runtime can use HFI to mediate all control flow and access to sensitive OS resources.

Regions HFI offers memory and control isolation using a finite set of *regions*---portions of a processes' virtual memory described by *base* (start address for the region) and *bound* (size of the region). By default, an HFI sandbox has no regions defined and thus cannot access memory to either access data or execute code. To grant access, the sandboxing runtime configures regions of memory allowed by, that are stored in internal region registers, and to configured using several dedicated instructions (e.g. `hfisetregionsize`, `hfisetregionpermission`). Regions come in three types:

- *Implicit data regions*: grant read and/or write memory access to a portion of memory, and are applied to every memory access performed by sandboxed code. For example, if sandboxed code executes an instruction---"load address X into register Y"---HFI will ensure that at least one of the implicit regions has a range that includes "X", and then applies the permissions from the first matching region.
- *Implicit code regions:* are similarly used to grant execute permissions, and applied to every instruction fetch a sandboxed program executes.
- *Explicit data regions:* are used to grant read/write access to sandboxed programs, but only through dedicated instructions that perform region-relative memory operations. Specifically, loads and stores to these regions are performed as offsets into the region using new h-prefixed variants the standard RISC-V memory instructions such as `hlw` and `hsw`. The offsets are checked to ensure they remain within the explicit region.

The new instructions introduced by HFI are shown in Figure on HFI Interface, while the new control and status registers as well as internal registers are shown in in Figure on HFI CSRs.

Chapter 3. Sandbox Setup

The sandboxing runtime can query if the processor supports HFI by checking the supported extension string from the device tree or the ACPI RISC-V Hart Capabilities Table as is the common practice (Jones, 2023). Specifically, the string will list "hfi-*version*" if HFI is supported. The HFI version described in this spec is "1".

If HFI is supported, HFI mode is enabled with the `hfienter` instruction, and disabled with the `hfiexit` instruction. The `hfienter` instruction has two variants---the first variant takes a single register operand which specifies the sandbox configuration options as a bit vector called `hfioptions_t`, that has the following fields:

- *lock_regions*: *reg_u1*---Regions configurations are normally specified prior to `hfienter`, using instructions such `hfisetregionsize` (See Section on Regions). If *lock_regions* is set to *false (0)*, region manipulation instructions can also be called while in HFI mode (i.e., the region configuration can be modified in the sandbox). If *true (1)*, these instructions cannot be called while in HFI mode.
- *redirect_system_calls*: *reg_u1*---HFI sandboxes can interpose on system calls made by sandboxed code. If *redirect_system_calls* is set to *false (0)*, system calls are unaffected by HFI. If *true (1)*, HFI will redirect system calls (`ecall`) instructions to the HFI exit handler (which can be set with the `hfisetexithandler` instruction discussed in Section on Exit Handler).
- *redirect_exits*: *reg_u1*---HFI sandboxes can interpose on invocations of `hfiexit` so the application can take control once the sandbox code completes. If *redirect_exits* is set to *false (0)*, `hfiexit` disables HFI and execution simply falls through to the next instruction. If *true (1)*, `hfiexit` disables HFI and redirects control flow to the exit_handler (which can be set with the `hfisetexithandler` instruction discussed in Section on Exit Handler).
- *serialize_enter_exits*: *reg_u1*---HFI sandboxes can add fences sandbox entries and exit (through the `hfienter` and `hfiexit` instructions), a required step for Spectre protections. If *serialize_enter_exits* is *false (0)*, these instructions do not introduce any serialization or fencing. If *true (1)*, these instructions act as a fence for all memory operations that are run prior to these instructions.

The second variant of `hfienter` operates like `hfienter` variant 1 plus a jump instruction; it takes the `hfioptions_t` as the first operand and takes the target of the jump in a register as the second operand.

Behavior The `hfienter` instruction interacts with multiple internal registers. It sets the field `hfiusermodeenabled` in an internal register `hfistatusreg` to 1 on execution, and clears the `hfifaultoccurred` field in another internal register `hfifaultstatusreg` indicating that there has not been a violation of HFI's region rules since the last invocation of `hfienter`. The second variant of `hfienter` additionally sets the PC to the target specified in the second operand after its execution. The `hfiexit` instruction interacts with all three fields from `hfistatusreg`. It sets its `hfiusermodeenabled` field to 0 on execution, write the value of the program counter of the `hfiexit` instruction to its `hfiexitpc` field, and set its `hfiexitreason` field to 1, indicating the sandbox exit was due to and `hfiexit` instruction. `hfienter` and `hfiexit` must always act as fence for other HFI instructions, i.e., they only execute after all in-flight HFI instructions have completed.

Faults The `hfienter` instruction will trap if the CPU is already in HFI mode. The `hfiexit` instruction will trap if the CPU is not in HFI mode.

Design Rationale Most of the options in `hfioptions_t` are present to support different use cases. When executing unmodified native code, the sandboxed code is totally untrusted, thus regions are locked, system calls are redirected, etc. However, when sandboxing code from existing SFI systems

such as WebAssembly, it is more efficient/not necessary for HFI to do some checks, since these systems already handle some safety checks in their compiler/runtime. For example, these systems may not want to redirect system calls. Similarly, the choice of whether or not to serialize `hfiexit` and `hfienter` will depend on the threat model that a particular application is trying to enforce (i.e. if they want greater Spectre safety), we leave it to the user to choose whether they wish to opt into this added overhead. Finally, `hfienter` is offered in two variants as some sandboxing runtimes may want the option to jump directly to executing sandboxed code after sandboxing is enabled via `hfienter`, while other runtimes may want the instruction to fall through to avoid any costs due to extra control flow. The former behavior can be difficult to accomplish with the single operand variant of `hfienter` as it requires the instruction following `hfienter` to be part of the sandbox's code---which may not always be possible. The latter behavior's performance is difficult to achieve with an instruction that includes control flow.

Chapter 4. Configuring the Exit handler

HFI supports interposition via. redirection on all paths out of the sandbox including sandbox exits (via. `hfiexit`) and system calls (and by extension signals). As noted, which instructions (system calls and/or `hfiexit`) are redirected is configured through `hfioptions_t`, that is passed as an operand to `hfienter`.

To handle this redirection, an exit handler is setup with the `hfisetexithandler` instruction. This instruction should be invoked prior to `hfiexit`. `hfisetexithandler` takes one operand, a 64-bit register, that holds the address of the exit handler. The current exit handler can be retrieved via the `hfigetexithandler` instruction.

Behavior The `hfisetexithandler` instruction sets the `hfiexithandlerreg` internal register to the address specified in its operand.

- If `hfiexit` is configured to invoke the exit handler, the `hfiexit` instruction, when executed by sandbox code, will jump to the exit handler *after* execution (during which `hfiexitreason` in `hfistatusreg` is set to 1 indicating the exit was due to the `hfiexit` instruction).
- If system calls are configured to invoke the exit handler, the system call instruction, when executed by sandbox code, will jump to the exit handler *before* execution, set the `hfiexitreason` field to 2 indicating the exit was due to a system call, and disable sandboxing by setting the `hfiusermodeenabled` field to 0.

Faults The `hfisetexithandler` instruction will trap if the CPU is already in HFI mode. If the exit handler is set to a location without code permissions, the behavior of the CPU would be identical to a normal jump to an address without code permissions.

Design Rationale Sandboxed code will invoke `hfiexit` to exit the sandbox. We must ensure that the sandboxed code always returns control to the sandboxing runtime after exits, which means, invocation of `hfiexit` should return control to trusted code. Thus, we have added support for redirecting all invocations of `hfiexit`.

Sandboxed code can also invoke system calls; since HFI's restrictions don't apply to kernel code, system calls could be used to bypass isolation enforced by the hardware (Connor et al., 2020). Thus, trusted code needs the ability to interpose on system calls, so that it can restrict the invocation of unsafe system calls by sandboxed code. Such interposition on system calls could be done using assembly rewriting or using kernel features such as EBPF, however, this is slow and cumbersome. To allow efficient interposition of system calls, HFI provides hardware support to redirect system calls. When enabled, system calls simply act like a jump instruction to the exit handler.

Chapter 5. Regions

Regions offer a limited version of the functionality found in traditional segmented memory systems, that control access using `<base, bound, permission>` tuples to control access to contiguous ranges of memory.

By default, a processor in HFI mode has no access to memory i.e. it cannot read data or run code. To enable sandboxed code to run, a sandbox runtime must explicitly configure regions prior executing `hfienter`. In the next sections, we provide a brief overview of the three types of HFI regions, and then specify how to configure these regions.

5.1. Regions Types

HFI offers three region types implicit code, implicit data, and explicit data. Each type is specialized to particular tasks, with the aim of reducing hardware complexity.

Implicit Data and Implicit Code Regions

Implicit regions are essential for isolating memory accesses and control flow of unmodified native code, as well as other situations where explicit regions (described next) would be impossible to use. HFI discriminates implicit regions into code and data regions, to keep the control and data pipelines simpler and more efficient. Data regions can grant read and write access and only apply to loads and stores, while code regions apply only to instruction fetches, and can only grant execute permissions.

Implicit data region checks apply to every memory access, and grant access on a first-match basis. For example, if sandboxed code executes an "lw rd, rs(offset)" instruction, HFI will check if the address in `rs + offset` is in range in *any* of the implicit regions in parallel. For the first matching implicit region, it will check the permissions to see if reads are allow—if so, it will proceed. If the permission check fails, or if there is no match, HFI will trap. Implicit code regions apply similar checks to code.

Implicit regions perform bounds checks based on *prefix matching*. Concretely, each region specifies a *base_prefix* (the region's base address) and an *lsb_mask*. To check if an address is in bounds, HFI uses the *lsb_mask* to remove the least significant bits of the address, and compares the remaining prefix to *base_prefix*. Implicit regions thus must be power of two sized and aligned---thus, they trade granularity for efficient checking---in particular, checks can be implemented with simple masking operations. Implicit regions checks are not applied to operations on explicit regions, which we discuss next.

Explicit regions Explicit regions provide region relative addressing, i.e., addressing is always relative to the base of the currently *active region* (by default, explicit data region 1). This offers efficient fine grain control over access to memory within a particular sandbox address or shared buffer. HFI provides two different region sizes~(*large*/*small*), with different granularities. Large regions can address up to 256 TiB (2^{48}) and are sized and aligned to multiples of 64K (2^{16}). Small regions, in contrast, can only address up to 4GiB (2^{32}), but are byte granular in size and alignment.

To access memory through explicit regions, a program must use the h-prefixed variants of normal load and store instructions (`hlw`, `hsw`, `hlh`, etc.). These instruction target the active region, but can be changed to use a different region as described in the section on standard profiles. For example, `hlw x1, A(x0)` will succeed if the address being loaded is falls within explicit region 1, and there is a read permission set on that region, otherwise it will fail.

A few notes on size and alignment Unaligned memory operations that are split by the micro-architecture into independent operations will be checked independently by HFI. If one split faults, the

original fused instruction will fault, as will the split instruction that violates HFI bounds. However, the split operation that is within bounds may is allowed to have visible *micro-architectural* side effects within the sandbox.

To safely implement explicit bounds checks, the bounds check must be applied to the operand of an operation (i.e., the address being loaded/stored to) plus the size of the operand, to ensure that longer operations do not exceed bounds checks.

Regions also have minimum sizes. The smallest large explicit region is 64K, there is no minimum size on small explicit regions. The smallest implicit region is 64 bytes. The behavior of regions that do not meet these minimums is undefined.

Design Rationale The large and small region sizes and alignment constraints on explicit regions allow us to implement explicit regions with a single 32-bit comparator. For small regions, HFI checks the least-significant 32-bits is within bounds, and ensures the top bits are zero. For large regions, HFI will drop the first 16-bits, and compare bits 16-48, while checking the top bits are zero. Like Intel x86, RISCV typically support a 48-bit virtual address space, on which this spec is based. This design rationale also applies to Sv39 or Sv57, though the comparator lengths need to be adjusted accordingly.

While allowing regions that support arbitrary address ranges at with any size and alignment is conceptually simpler than specialized large and small regions, our restrictions allow bounds checking with very simple hardware. For base integer loads/stores, HFI's large and small regions constraints can be checked with a single 32-bit comparator, rather than the more costly multiple 64-bit comparators needed to check arbitrary region bounds. For atomic memory instructions that do not rely on relative addressing but use an absolute addresses, two 32-bit comparators are needed.

Explicit regions' added granularity is critical for supporting Wasm heaps, which grow in 64K increments (Haas et al., 2017)---while byte granularity is critical for efficiently sharing individual memory objects and sandboxing legacy code, as existing buffers can be shared in-place changing code or allocators.

5.2. Manipulating Regions

Region state, which is stored in internal registers, can only read or modified HFI instructions. The instructions broadly operate on regions by a region number (`region_number_t`)---a unique number/index assigned to each HFI region on the CPU.

Region number assignments The version of HFI defined in this spec (hfi1), defines three regions: one explicit data region with a `region_number_t` of 1, one implicit data region of `region_number_t` of 2, and one implicit data region of `region_number_t` of 3. Future versions may define multiple regions of each type (Section on Standard Profile), and each region will be assigned a unique `region_number_t`.

We now discuss the instructions that can configure these regions:

Setting Region base and size The following instructions are used to specify the range of memory a region applies to. To configure a specific region's base and size, a sandboxing runtime must first select the target region. This is accomplished by direct instructions that write to a dedicated register indicating current region being configured. Once a region is selected, its base address and mask/bound can be configured using separate pseudo-instructions that target dedicated registers. This approach breaks down the operation to fit standard RISC-V instruction formats, avoiding having multiple destination registers.

`hfiselectregion`(*region_number_t*)

`hfisetregionbase`(*reg_u64 base*)

`hfigetregionbase`() → *reg_u64 base*

`hfisetregionbound`(*reg_u64 mask_or_bound*)

`hfigetregionbound`() → *reg_u64 mask_or_bound*

Behaviour The region to configure is set with `hfiselectregion`, and then its sizes and locations are set using `hfisetregionbase` and `hfisetregionbound`. Regions are typically setup prior to entering the sandbox (with `hfienter`). If this instruction runs in a sandbox, i.e., `hfiusermodeenabled` is 1---which is allowed when `lock_regions` is 0---it must act as a memory fence. All prior memory instructions must complete before executing this instruction and subsequent memory operations should be issued only after the update.

`hfiselectregion` has `region_number_t` as its operand register, and works closely with the other four instructions. While `hfisetregionbase` has the base of the region as its operand, `hfisetregionbound's operand depends on the type of region. If the region is an explicit data region, the operand should contain the bound/size of the region; if the region is an implicit data or code region, the third operand should contain the mask for the region. The value of the base and bound/mask should additionally conform to the per-region size and alignment requirements in the section on region types. However, the instruction does not check whether operands meet this criteria. If the operands don't meet the criteria, the resulting behavior is undefined.

`hfigetregionbound` and `hfigetregionbase` return region size information based on the previously fed `region_number_t`. Similarly, `hfigetregionbound` returns the mask if the region is implicit and the bound if the region is explicit.

Faults These instructions fault if the region number specified does not exist (i.e., it is greater than the total number of regions). For efficiency, these instructions should not check whether region locations or sizes are invalid (e.g., the program has specifies an implicit region base that is not aligned to its size); rather the hardware will continue to operate using the provided base and size, although this behavior is to be considered undefined.

Design Rationale When `hfisetregionsize` is run prior to `hfienter`, it doesn't need to act as a fence as `hfienter` can fulfill this purpose. However, when used inside the sandbox, `hfisetregionsize` must act as a fence, as otherwise inflight memory operations could potentially access memory outside the sandbox when they were issued if a region resized.

Setting Permissions, Enabling/Disabling Regions The following instructions are used to configure permissions on regions, as well as to enable and disable regions.

`hfisetregionpermission`(*permission_set_t*, *permission_t*)

`hfigetregionpermission`(*permission_set_t*) → *permission_t*

Behaviour Region permissions are set using the `hfisetregionpermission` instruction. This instruction sets the permissions of all regions using a single bit vector. The instruction takes `permission_set_t` as the first argument. This is a 32-bit register which must have the value 0; other values are reserved for future use. The second operand to this instruction is a permission bit-vector `permission_t` encoded as follows:

- Bits 0 to 3 are permissions for explicit data region 1. Bit 0 indicates if the region is enabled (i.e., should be enforced by the sandbox). Bit 1 and 2 indicates whether the region has read and write

permissions respectively. Bit 3 indicates if the explicit data region is a large region (i.e., a region with a bound greater than 4GB as explained in the section on region types.

- Bits 4 to 6 are permissions for implicit data region 1. Bit 4 indicates if the region is enabled. Bit 5 and 6 indicates whether the region has read and write permissions respectively.
- Bits 7 to 8 are permissions for implicit code region 1. Bit 7 indicates if the region is enabled. Bit 8 indicates whether the region has execute permissions.

Faults This instruction will fault if the `permission_set_t` is not set to 0, or if `hfiusermodeenabled` and `lock_regions` is set to 1 (when hfi mode is on with region configurations locked). Any unused bits of `permission_t` are ignored; thus setting an unused bit will not fault.

Design Rationale An alternate design for this instruction would be to split up `hfisetregionpermission` to operate per-region (by changing the instruction to take `region_number_t` to operate on as the first parameter). However, this would lead to additional overheads in practice. This is because this instruction is primarily used when switching between active sandboxes. In this case, the permissions of all regions would likely need to be adjusting. If `hfisetregionpermission` operated per region, then three calls to this instruction would be needed to adjust the permissions of the three regions. In contrast, our design allows this to occur in a single instruction. Additionally, the `permission_set_t` parameter further future-proofs this design by allowing us to modify the format of this instruction for future versions of HFI, without breaking backward compatibility.

Clearing Regions To clear region state rapidly e.g. on context switches, HFI offers `hfiresetregions`.

Behaviour This instruction sets the base and bound/mask of all regions to zero (equivalent to calling `hfisetregionsize` with arguments of 0 on all regions), disables all regions and sets their permissions to zero (equivalent to calling `hfisetregionpermission` with a permission vector of 0). It also sets the active explicit data region to 1 (this will matter only in future HFI versions which have multiple explicit data regions).

Faults This instruction faults if `hfiusermodeenabled` and `lock_regions` is set to 1 (when hfi mode is on with region configurations locked).

Design Rationale While this instruction can effectively be achieved using combinations of other instructions, unifying this "reset" operation into a single instruction allows optimizing a number of paths. For example, when an application needs to switch between multiple sandboxes, software has to clear the state of the first sandbox before applying the state of the second sandbox. This allows optimizing the first step sequence. This operation is also useful when the OS kernel is switching between two scheduled processes both of which may use HFI. The OS kernel is responsible for saving and restoring each processes' HFI state, and thus can also use this instruction.

5.3. Implementation Considerations

Implementation Semantics and Spectre To ensure Spectre safety, the following guidance is offered for implementers.

For code regions: To ensure security, prefix-checking should be carried out in parallel with the decode stage. If the check finds a matching region with execute permissions, it succeeds, and decode carries on normally. If the check fails, it prevents the decoded micro-ops from entering the pipeline, and instead translates all instructions into a faulting NOP micro-op. This ensures that instructions that are out-of-bounds are not executed during committed execution, and are also not executed speculatively.

For data regions: Bounds checking, DTLB lookup, and cache index lookups should happen in parallel.

One concern here is that, cache state could be modified as a result of secret (out-of-bounds) data. To prevent this sort of side-channel attack all bounds must checks occur *before* the processor resolves the physical address of a memory access. This is secure because the processor can update cache metadata like the LRU bits (for hits) or fetch new data blocks (for misses) only after resolving the physical address. HFI can therefore strictly prevent any metadata updates if there has been a fault.

Note that out-of-bounds address can affect metadata of the DTLB or i-cache---e.g., LRU bits. However, the invariant we guarantee---no secret (data stored outside the boundaries of the region) ever affects architectural state---is still not violated, since we do not allow the *result* of an out-of-bounds memory operation to propagate into any of these structure.

To summarize, HFI's data pipeline is Spectre safe, since the data cache is not updated prior to bounds checks being completed; HFI's control pipeline is safe as bounds checks finish prior to instruction decode which is before the execution of instructions. This approach also helps to guarantee that any code executed as the result of PHT, BTB, and RSB (speculative) predictions are checked prior to execution.

Chapter 6. New Internal Registers

HFI stores state for the current sandbox in internal registers including: (1) the sandbox status (2) the exit handler (3) region configuration (4) the cause and status of HFI induced faults (traps). These are detailed in Figure on HFI CSRs.

6.1. Sandbox Status Register

Fields The sandbox status, stored in the `hfistatusreg` internal register, is read-only to userspace software, but writable by kernel code. The contents of the `hfistatusreg` register are as follows:

- *hfi_usermode_enabled* (1-bit): is updated automatically during `hfienter` (set to true), `hfiexit` (set to false), and when the exit handler is called (set to false).
- *hfi_exit_reason* (2-bit): indicates the reason for the last sandbox exit. Exit due to `hfiexit` would leave this set to 1. Exit due to a system call with leave this set to 2.
- *hfi_exit_pc* (60-bit): indicates the PC of the instruction causing the last exit. The first 2-bits and the last 2-bits of the PC are dropped and are assumed to be zero. Thus 60-bits of the PC are stored.

Serialization Caveat The `hfistatusreg` register should support updates via register renaming to support the performance expectations of hardware sandboxing. These values are expected to change frequently (once in few thousand instructions), and serializing this register updates with techniques like score-boarding will hinder practical adoption.

6.2. Exit Handler Registers

Fields The address of the sandbox exit handler is stored in the `hfiexithandlerreg` internal register. When a sandboxed hart traps or executes an `hfiexit` instruction, the Program Counter (PC) is set to the value stored in this register. This register is written to using the `hfisetexithandler` instruction and read using the `hfigetexithandler` instruction. The contents of the `hfiexithandlerreg` register are as follows:

- *Exit Handler Address* (60-bit): indicates the address of the exit handler set for current sandbox. The first 2 bits and last 2 bits of this address are dropped and assumed to be zero.

Serialization Caveat The exit handler of the sandbox is stored in the `hfiexithandlerreg` internal register and can be set or read via the `hfisetexithandler` and `hfigetexithandler` instructions. Since the register is not expected to be frequently updated, it's updates may be scoreboarded if needed.

6.3. Region Registers

Fields There are three sets of internal registers dedicated to region configurations required by hfi: bounds registers, permissions registers, and selector registers. Different version of HFI may require different numbers of these registers, as discussed in the section on standard profiles. Bounds registers specify the bounds and sizes of a region. Each implicit region (data or code) has a 64-bit prefix register and a 64-bit mask register, while each explicit region has a 64-bit base register, a 64-bit bound register, and a 1-bit field specifying whether this is a large region or small region. Permissions registers specify whether a region can be read, written, or executed. Each data region has a 1-bit write field and a 1-bit read field, while each code region has a 1-bit execute field. On top of these registers is the selector register, which contains the region number of the region currently being configured. Its only field is a 32-bit `region_number_t`.

Serialization Caveat The region registers cannot be directly named, and must instead be modified or accessed through HFI instructions (e.g. `hfigetregionsize`). Since these registers should updated whenever a sandbox switch occurs, updates to these registers should ideally be supported through register renaming; however, implementations may choose to use the slightly less expensive scheme, as illustrated in Figure on Region Register Example. In particular, implementations can configure the regions outside the sandbox without serializing, and defer fencing to when an `hfienter` instruction executes. This way, updates to these registers do not fence, and the `hfienter` instruction waits for all pending region register updates to complete. When a sandbox is enabled (`hfiusermodeenabled` set to 1), region register updates are not permitted if `lock_regions` option is set to 0. In the case that the region is not locked, however, all updates to the region register within the sandbox must serialize.

6.4. Fault Registers

Fields The result of an HFI fault due to an HFI policy violation is stored in the `hfifaultstatusreg` register. This register stores the precise cause of an HFI induced fault (trap). Since the register is not expected to be frequently updated, it's updates may be scoreboarded if needed. Information in `hfifaultstatusreg` is readable in user space so the runtime can respond appropriately, and read-write in the kernel so that this state can be saved/restored as part of the process context, as multiple processes may be using HFI, and fault delivery is asynchronous. This register has four fields:

- *hfi_fault_occurred* (1-bit): is a bit that indicates that an hfi fault has occurred.
- *hfi_fault_region* (8-bit): indicates which region the fault occured in, if the fault was do to an explicit region trap (out of bounds or insufficient permissions), it will contain the number of the region that caused the fault, i.e., the operand to an h-prefixed instruction. If the fault was caused by an implicit region i.e. insufficient permission to access a matched region,it will contain the number of the region. If the fault was cause because no implicit region matched an operation, it will contain 0.
- *hfi_fault_op* (2-bit): indicates the operation that faulted, this will be a `LOAD_FAULT` or `STORE_FAULT` for a failed load or store, or `FETCH_FAULT` for a failed instruction fetch.
- *hfi_fault_type* (1-bit): indicates the type of fault. If `OUT_OF_BOUNDS`, it indicates that an operation was out of bounds if it was explicit region fault , or that no implicit region matched the operation (in this case `hfi_fault_region` will be equal to zero). If `INSUFFICIENT_PERMISSIONS`, either an explicit region had insufficient permissions for an access, or whatever implicit region matched the operation did not have sufficient permissions.

Design Rationale The `hfienter` and `hfiexit` instructions modify the various bits of the `hfistatusreg` register. The updates to this register must be fast to allow rapid entries and exits to HFI mode; thus this must be supported by register renaming. Region registers are updated frequently as well when switching between different sandboxes. While this would ideally support register renaming for efficient register updates, an alternate scheme that ensures a single serialization (on entry into the sandbox) for a batch of region updates prior to entry, would provide adequate performance. Finally, updates to the region configuration within the sandbox should serialize, as an updates during speculative execution may allow Spectre-style attacks to break out of the sandbox.

Chapter 7. Using HFI

Here we explore how HFI's features are used to create sandboxing runtimes in userspace, and the HFI support needed from the operating systems.

7.1. Sandboxing in Userspace

Suppose we have a sandbox runtime (e.g. part of an application implementing a Wasm FaaS server, or a library sandboxing framework (*The RLBox Sandboxing Toolkit*, 2024)), that is ready to create new sandbox. We assume that the runtime has reserved some memory for the sandbox (i.e., the sandbox memory), has placed the input for the sandboxed code in a memory buffer, and the sandboxed code itself is separated from other code and mapped in an isolated contiguous portion of the address space. Our runtime can now take the following steps:

Setting up regions To start, our runtime sets up access to the code, heap, and input memory so our application has everything it needs once the sandbox starts, it does this using the `hfisetregionsize`, `hfisetregionpermission` instructions to setup and enable regions that grant access to the allocated heap and inputs, and the application code. If no code regions are mapped, HFI will immediately trap after `hfi_enter` is called, as the processor will not be able to fetch instructions.

What type of regions the runtime will use, as as how the sandbox is configured will depend on if it is sandboxing a native or SFI (e.g. Wasm) based application.

Sandboxing Native code When sandboxing native code, the code being sandboxed is entirely untrusted, and thus, it cannot be allowed to modify any of HFI's state, or exit the sandbox in unexpected ways, or perform any other operation that would allow it to violate the sandbox's policy. Thus, the sandbox options flags in `hfioptions_t` that are passed to `hfienter` to start the sandbox will: set the `lock_regions` flag to 1 (true), since sandboxed code cannot be trusted to modify regions; set the `redirect_system_calls` flag to 1, as again this code can't be trusted to perform system calls directly; set the `redirect_exit` flag to 1, ensuring all control flow out of the sandbox is redirect to the trusted runtime. The runtime will use an implicit data region to permit the sandboxed code to use of the sandbox memory; the runtime will then ensure the sandboxed code's stack, heap and inputs are part of this implicit region. An implicit code regions will be used to mark the code of the sandbox.

Sandboxing using SFI runtimes When sandboxing code through SFI runtimes such as a Wasm runtime, sandboxing is handled as a mix of compiler/software-runtime checks as well as hardware checks from HFI. In the scenario, implementer has confidence in the correctness of the SFI's runtime and compiler, and thus their use of HFI is different from sandboxing code, giving it greater flexibility and performance.

For example, on `hfienter` it can set the `lock_regions` flag to 0 (false), allowing the compiler/runtime to modify regions with `hfisetregionsize` and `hfisetregionpermission` without having to exit the sandbox. This can allow regions to be used more flexibly, e.g. it can load and spilling registers, and never need to exit the sandbox. The `redirect_system_calls` flag can also be set to 0 (false), as the Wasm compiler disallows direct access to system call instructions, ensuring that any system calls made will come from the trusted runtime, this can eliminate the overhead of unecessary sandbox exits. What the redirect_exit flag will be set to depends on the SFI implementation, it may set this flag to false and opt to let sandbox exit's fall through to minimize overhead, since it can ensure that it knows that it can control whatever instruction follows an `hfiexit`, or it may opt to set it to true, and setup an exit_handler.

For granting access to memory, the runtime will use still use implicit regions for code, however, an

explicit region(s) will be used for the applications heap(s) and inputs, as the SFI compiler can use h-prefixed instructions for accessing these directly. This allows it to exploit the greater flexibility of explicit regions for sizing and alignment that are necessary to support Wasm and similar systems. Notably, a Wasm runtime in the sandbox may opt to place it's own data into an implicit data region, to ensure Spectre attacks cannot be used to trick the sandbox runtime into leaking its own data.

Saving context A sandboxing runtime must protect its own execution context such as its stack and contents of CPU registers, before it switches to sandbox code. HFI leaves this mechanism entirely up to software---this flexibility is important for efficiency. For example, if our runtime is running untrusted native code---it will have to use springboards and trampolines (Yee et al., 2009)---lightweight assembly routines that (1) clear registers and switch to a separate stack prior to executing the sandboxed code and (2) restore these registers after the sandboxed is executed. However, if it is running Wasm code, it could opt to use zero-cost transitions (Kolosick et al., 2022) that rely on the compiler to ensure that the sandbox code cannot misuse the stack or scratch registers.

Setting up an exit handler If our runtime needs an exit handler either to handle `hfiexit` or redirected system calls, it will need to setup an exit handler with `hfisetexithandler`. This exit handler is implemented as a normal function call in the runtime that takes no arguments. It will query the `hfiexitreason` CSR to find out why it was invoked.

Entering the sandbox Having taken all these steps, our runtime is ready to start the sandbox. Once it calls `hfi_enter`, HFI mode is enabled, and the next instruction that runs will be inside a sandbox.

The exit handler (`hfiexit` and system calls) When the exit handler is called after the sandbox exits, it will transfer control to the exit handler function in the runtime, which will check a control and status register (CSR) to identify the cause of the exit, and respond appropriately.

For example, for sandbox exits, it will need to save context unless the sandbox execution has completed. Similarly for system calls, it will need to save context, but then also execute whatever additional logic is need to check the parameters of the system call for safety and finally invoking the system call (Connor et al., 2020).

7.2. OS (and VMM) integration

HFI is designed to require only minimal changes/support from the OS kernel. HFI requires support from OS kernels in two areas:

Handling HFI faults A fault may occur in HFI mode for to two reasons: (1) normal processor traps such as division by zero. (2) HFI policy violations. In both cases, when the processor traps into the kernel, HFI enforcement is disabled so as not to disrupt kernel execution, and the trap is handled through all the normal OS signal mechanisms (This is automatic as HFI hardware checks are only applied to userspace code). When an instruction can traps due to some HFI policy violation, the normal trap mechanism for the current hart is employed. HFI introduces a new trap code, `hfi_fault` to support this.

When an HFI trap occurs, additional details about the cause are stored in the `hfifaultstatusreg`. A kernel trap handler can immediately read and store this state into the process struct for the current process, so it can be queried by a signal handler. The OS then invokes the standard signal handler registered by the application for memory access violations. The OS must invoke the signal handler with HFI disabled; if the signal handler returns control to the OS, the OS will re-enable HFI prior to resuming the faulting process.

Process scheduling The kernel must save and restore HFI state (stored in internal registers) when switching between processes/VMs etc. This can be performed using the HFI manipulation instructions `hfiresetregions`, `hfisetregionpermission`, `hfisetregionsize`, `hfigetregionsize`, etc. To know whether HFI mode is currently enabled by the user space process, more privileged code can check the state of the `hfiusermodeenabled` status register.

Chapter 8. Instruction Encoding

HFI introduces two sets of new instructions: h-prefixed instructions that mimic native load and store instructions used exclusively in explicit regions, and non-h-prefixed instructions that primarily interact with internal HFI registers. H-prefixed instructions should be encoded using opcodes that fail if not implemented, because the h-prefixed instructions introduce new functionality---relative memory accesses. As a result, binaries that use HFI's explicit region's would not be supported on regular hardware. However, binaries that only use HFI's implicit regions would remain backward compatible on CPUs that don't support HFI (albeit without the isolation enforcement).

8.1. H-prefixed Instructions

In order to provide full support for modern RV64GV processors, multiple extensions need to be supported in addition to the base integer instruction set. Specifically, HFI needs to accommodate memory access instructions in the Atomic extension (A), the Floating Point extensions of different precisions (F, D, Q), and the Vector extension (V).

Base Loads and Stores H-prefixed base loads and stores automatically check against the bounds specified by the explicit region registers before serviced to memory. The effective address (EA) calculation is identical to the native base load and store instructions, except that after the EA is obtained, the base of the region is added on top of the EA to get the final address EA'. The bound check compares EA against the region bound. Specifically, implementations can choose to the place the bound check logic in parallel with the final EA' computation and/or TLB lookup to minimize performance overhead.

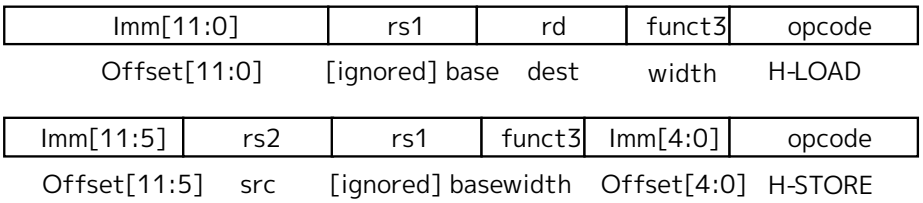

Figure 1. H-prefixed Base Loads and Stores

Table 1. Encodings for h-prefixed base loads and stores, both using custom opcodes reserved in RISCV.

Opcode	Instruction	Funct3	Opcode	Instruction	Funct3
0001011	`hlb`	000	0001011	`hlwu`	110
0001011	`hlh`	001	0101011	`hsb`	000
0001011	`hlw`	010	0101011	`hsh`	001
0001011	`hld`	011	0101011	`hsw`	010
0001011	`hlbu`	100	0101011	`hsd`	011
0001011	`hlhu`	101			

Floating Point Loads and Stores The floating point extensions include the single-precision, double-precision, and quad-precision extensions, all of which are encoded under the same opcode, and differentiated with a 3-bit width field. FP loads and stores behaves the same way as base loads and stores, only its register operands reference the floating point register file rather than the integer one.

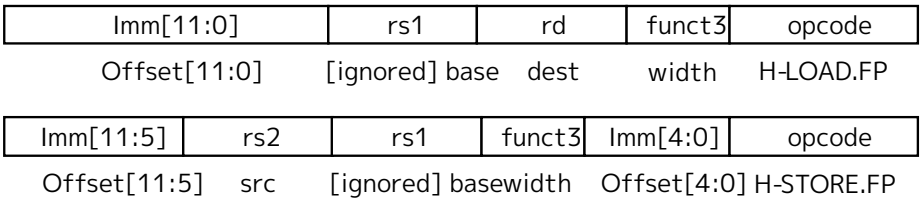

Figure 2. H-prefixed floating point loads and stores.

Table 2. Encodings for h-prefixed vector loads and stores, using custom opcodes.

Opcode	Instruction	Funct3	Opcode	Instruction	Funct3
0011111	`hflw`	010	0111111	`hfsw`	010
0011111	`hfld`	011	0111111	`hfsd`	011
0011111	`hflq`	100	0111111	`hfsq`	100

Vector Memory Operations The vector memory instructions enable accessing multiple memory blocks from multiple memory locations with a single load/store instruction, which complicates bound checks. Unlike Reusing the same opcodes from the FP extension, the vector loads and stores encode the four supported addressing modes in the `mop` field: unit-stride, strided, and two indexed modes (ordered and unordered). For each mode, the `nf` field specifies the number of elements to group together as a segment. To implement HFI versions of these instructions, the same opcodes from the h-hued FP instructions can be reused, with the width field and the mop field inheriting the same encoding of the extension (as in Table on Vector Encodings). H-prefixed versions of these instructions need to bound the multiple memory accesses judiciously. A bounding scheme is detailed as below.

For strided instructions and indexed instructions: Both the strided instructions and indexed instructions are powerful instructions that can address the entire virtual memory space. The strided vector loads and stores access multiple locations in memory at a stride, while the indexed vector loads and stores access irregular memory locations at offsets provided in vector registers, much like the scatter-gather instructions in x86. On top of this, segment versions of these instructions enable accessing anywhere from one to eight elements at each location, called a "segment", potentially accessing bytes to kilobytes of memory based on the hardware capacity of vector registers.

For these instructions, the bound checks can happen individually for each of the effective addresses after the vector memory loads and stores unit computes a chain of these effective addresses in parallel with the TLB lookup. Unlike scalar operations, HFI needs to check the entire segment against region bounds. An intuitive but expensive scheme is to do one 64-bit add and two 32-bit compare: add the segment size to the start address for the end address, and check the start and end addresses respectively against the region bound (how the check is simplifed to only using 32-bit comparators is detailed in original HFI paper). However, implementations can also utilize the relatively small segment size and avoid the expensive full adder.

The segment size is determined by the `nf` field (an integer ranging between 1 and 8) encoded in the instruction, and the element size, whose maximum value depends on the vector length (`vlen`) of specific hardware implementation. `vlen` is put at a maximum value at or smaller than 4096 in most modern RISCV implementations (Perotti et al., 2022), with a theoretical maximum of 2^{16}. The maximum segment size is 4KiB for a `vlen` < = 4096 and 64KiB for the theoretical max. To best capitalize on this property, while bounding the end of the segment, implementations can choose to add a cheaper 16-bit adder and a 48-bit incrementor (if `vlen` < = 4096) or a 32-bit adder and a 32-bit incrementor (for greater `vlen`-s).

For unit-stride instructions: These instructions access multiple memory locations with a stride of 1. Hence, they always access a non-overlapping, contiguous chunk of memory, even when segment

memory operation is enabled (the following segment sits next to the previous one). While the previous individual bound check may well work for unit-stride instructions, implementations may choose to only check the end address of the last segment at a higher cost of using a multiplier.

Figure 3. H-prefixed vector loads and stores.

Table 3. Field encodings for vector loads and stores

mop	Addressing Mode	funct3	Width	opcode	Operation
00	unit stride	000	byte	0011111	h-load
01	index (unordered)	101	half-word	0111111	h-store
10	constant stride	110	word		
11	index (ordered)	111	double-word		

Atomic Memory Operations The atomic extension provides instructions to atomically read, modify, and write back to memory between multiple harts running in the same memory space, including general-purpose load and stores, and fetch-and-op instructions that atomically performs specific computations on memory contents fetched. Similar to the base load and store instructions, h-prefixed atomic memory operations first compute the effective address (EA) in the same way as their native counterparts, then add the base of the explicit region to get the final address EA'. Meanwhile, the EA is checked against the region bound before proceeding with the atomic operation.

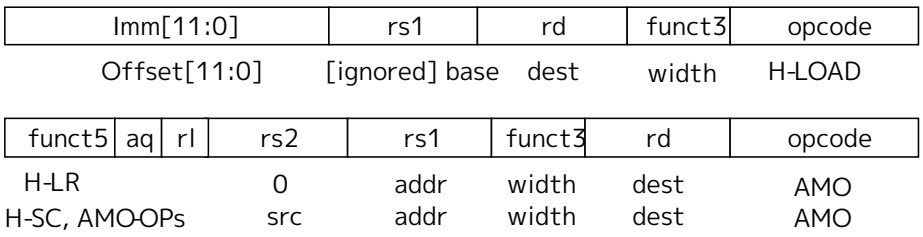

Figure 4. H-prefixed atomic loads, stores and other atomic operations.

Table 4. Encodings for h-prefixed atomic memory instructions, reusing the Atomic opcode.

Opcode	Instruction	Funct5	Opcode	Instruction	Funct5
0101111	hlr	00101	0101111	hamoor	01101
0101111	hsc	00110	0101011	hamomin	01110
0101111	hamoswap	00111	0101011	hamomax	01111
0101111	hamoadd	01001	0101011	hamominu	10001
0101111	hamoxor	01010	0101011	hamomaxu	10010
0101111	hamoand	01011			

8.2. Non-h-prefixed Instructions

The non-h-prefixed HFI instructions are functional instructions interacting with specific internal registers. Corresponding to the new internal registers, these instructions primarily fulfill three tasks: HFI mode transition, exit handler configuration, and region manipulation. All of the non-h-prefixed instructions are encoded in a R-type format under the same custom opcode `HFUNCTION` to achieve maximum flexibility (See R-type format in Figure on R-Type Format). The funct 3 field differentiates the instructions based on the tasks, and the funct 7 field further distinguishes the specific instruction. The specific encoding is shown in Table on Non-h Encodings. The behavior of these instructions has mostly been covered in Sandbox Setup, Exit Handler Config and Regions, and this section mainly details their encoding.

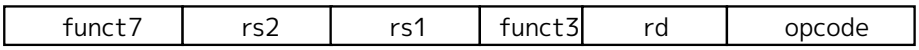

Figure 5. R-type instruction format.

HFI Mode Transition Instructions These include the `hfienter` and `hfiexit` instructions. `hfienter's 4-bit option vector comes from `rs1` and its `rd` field is invalid. The `hfiexit` instruction does not have any source or destination register, and thus these fields are all invalid in the instruction.

Exit Handler Instructions These instructions include `hfisetexithandler` and `hfigetexithandler`. They only take one operand from `rs1` holding the address of the exit handler and configure the handler for sandbox exits and syscalls in the dedicated internal register `hfiexithandlerreg`.

Region Manipulation Instructions These include the region-configure instruction `hfiselectregion`, the region size instructions `hfisetregionbase`, `hfigetregionbase`, `hfisetregionbound`, `hfigetregionbound`, and the region permissions `hfisetregionpermission`, `hfigetregionpermission`, `hfiresetregions`. All of these instructions directly interact with the corresponding internal registers, which are otherwise inaccessible. `hfiselectregion`, `hfisetregionbase`, `hfisetregionbound` and `hfisetregionpermission` all take a single operand from `rs1`, respectively the region number, the base address of the region and the mask (implicit region) or bound (explicit region) for the region. The remaining "get" instructions set the `rd` register based on these internal registers.

Support for More HFI Version In the future standard profile we aim to develop (detailed in the standard profile section), up to 4 explicit data regions are supported. Therefore, an instruction (`hfisetcurrexplicitdataregion` and `hfigetcurrexplicitdataregion`) that sets which explicit region the h-prefixed instructions will use is needed. `hfisetcurrexplicitdataregion` always precedes the h-prefixed instructions and takes the region number from its `rs1`. The instruction pair also double-checks the region number to ensure that it references an explicit region.

Table 5. Encoding for R-type Non-h-prefixed Instructions

funct3	funct7	Instruction	funct3	funct7	Instruction
000	0000000	`hfienter`	010	0000000	`hfiselectregion`
000	0000001	`hfiexit`	010	0000001	`hfisetregionbase`
000	0000010	`hfientertarget`	010	0000010	`hfigetregionbase`
001	0000000	`hfisetexithandler`	010	0000011	`hfisetregionpermission`
001	0000001	`hfigetexithandler`	010	0000100	`hfigetregionpermission`
011	0000000	`hfigetcurrexplicitdataregion`	010	0000101	`hfisetregionbound`

funct3	funct7	Instruction	funct3	funct7	Instruction
011	0000001	`hfisetcurrexplicitdataregion`	010	0000110	`hfigetregionbound`
			010	0000111	`hfiresetregions`

Chapter 9. Pending Design Considerations

Here, we include topics that we believe merit further discussion but which we have not fully resolved for inclusion in the specification.

9.1. Streamlining Control Transfers for Native Binaries

When sandboxing unmodified native binaries, we would ideally like control transfers into and out of the sandbox library to require minimal overhead and complexity. With a few small changes, we could make this simpler than what `hfienter` and `hfiexit` offer today.

At present, control transfers require redirecting control flow through small stubs (trampolines) that need to be mapped by the sandbox runtime into the sandboxed library address space, this adds complexity and overhead.

For example, consider a case where a host application has uses a library sandboxed with HFI; the applications want to invoke a function `foo()` in the library. To call `foo()`, it will need trampoline code---application code that performs a context switch by saving the current registers, switching the stack register to point to memory inside a region, enabling HFI and transferring control to `foo()`. This is mostly straightforward. However, once `foo` finishes executing (`foo` executes a return instruction), execution would attempt to return to the trampoline code---an operation that would fail as the trampoline code is not part of the sandbox code. Thus the host application, must perform an intermediate step---it must call `foo`, while modifying the return address on the stack to point to a stub within the sandbox, which invokes `hfiexit` and then returns to the trampoline. We could eliminate the need for this stub by dedicating a bit in the return address (e.g. it's least significant bit, as this should be unused as instructions are at least 16 bit aligned) on the stack that indicates that if HFI is enabled, this return should simply invoke `hfiexit`. Similar mechanism could also be applied to eliminating the need for trampolines for direct and indirect calls (i.e. callbacks) to host libraries.

9.2. HFI Versions (Profiles)

We aim to support multiple versions (profiles) for HFI to ensure we can support the myriad of RISC-V uses cases from embedded devices to server class CPUs. The two versions we currently aim to support are a minimal profile aka version 0, and a standard profile aka version 1. The key difference between these two is the number of supported regions. Versions may also be used to incorporate additional features in the future. Software can check what version is supported as described in the sandbox setup section.

The minimal profile described in this document supports: 1 implicit code region, 1 implicit data region and 1 explicit data region. The additional standard profile supports: 2 implicit code regions, 4 implicit data regions, and 4 explicit data regions. These regions are numbered as follows: explicit data region 1, implicit data region 1 and implicit code region 1 are regions 1, 2, and 3 in both profiles. In the standard profile: explicit data region 2, 3, and 4 are regions 4, 5, and 6 respectively; implicit data region 2, 3, and 4 are regions 7, 8, and 9 respectively; implicit code region 2 is region 10. Additionally the permissions bit vector operand specified in the `hfisetregionpermission` and `hfigetregionpermission` instructions is also expanded to accommodate region permissions in the same order.

Design Rationale Regions exact some cost in terms of circuit area, and differing trade-offs may make sense for different use cases. Obviously more regions facilitate efficient access to more data and code concurrently, and can simplify runtime implementation.

While the minimal profile is limited in the number of regions, this can still offer meaningful benefits

for certain use cases without significant concurrency or memory sharing. For example, the Google Chrome browser's Ubercage JIT isolation scheme (saelo, 2021) would be able to leverage this minimal profile for its isolation requirements (Groß saelo, 2024).

The standard profile offers an expanded the number of regions, the particular number of regions was inspired by uses cases such as leveraging WebAssembly for efficient isolation of libraries from applications, and efficient isolation of different clients' code in serverless settings (Narayan et al., 2023). The main observation here is that there is greater concurrency and sharing is present than simple use cases, but this can nevertheless be handled efficiently with a handful of regions. For uses cases that need additional regions, this can be achieved by spilling and restoring regions similar to how this is done with general-purpose registers.

Two additional instruction are required to support the standard profile with it's multiple explicit regions.

`hfi_set_curr_explicit_data_region`(*region_number_t*)

`hfi_get_curr_explicit_data_region`() → *region_number_t*

These instructions are used to set which explicit region the h-prefixed instructions will utilize.

9.3. HFI in M-mode or S-mode

We plan to add support for HFI in S-mode. Relatively small changes are necessary, however, we have not yet done a full analysis of how privileged instructions are handled. HFI support in m-mode may similarly be possible, but requires additional analysis for hardware implementation details.