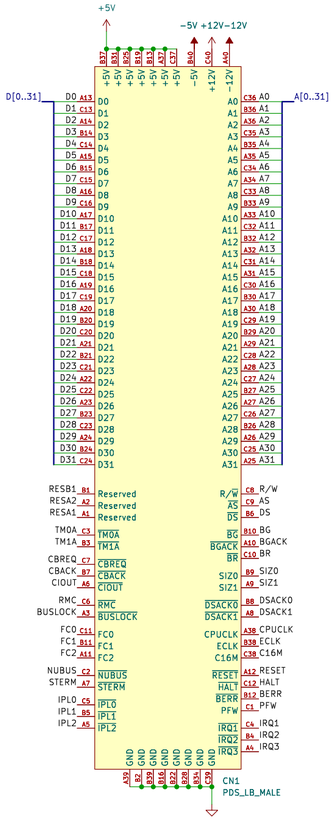
LB PDS

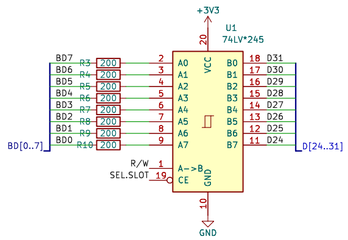


pin 1: T/R aka A->B
High: A->B
low: B->A

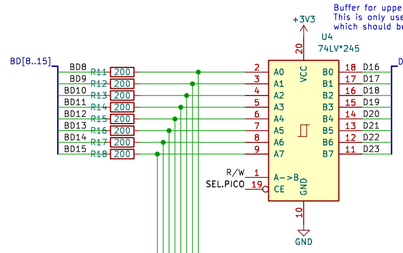
R/W
Write = Low = Host data -> Buffered bus

lower 8 bits of data bus. always used.

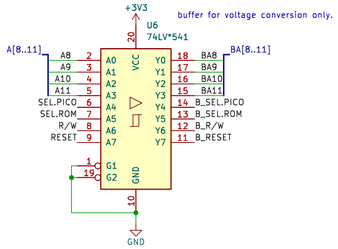
resistor packs allow Pico GPIOs to be left as outputs without the RP2040 and buffers overdriving eachother during state transitions



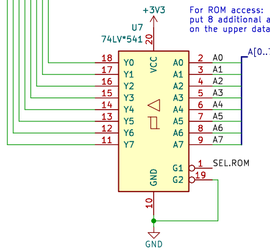
Buffer for upper 8 bits
This is only used on 16 bit accesses which should be only Pico access.



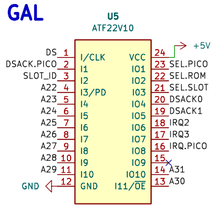
buffer for voltage conversion only.



For ROM access:
put 8 additional address bits on the upper data bits



GAL

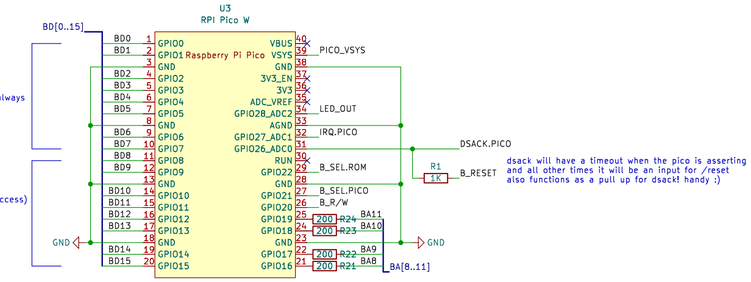


A22–A23 identify card address space (ROM, PICO, Status)
A24–A27 identify slot ID (9, A, B)
A28–A31 identify expansion slot space

slot id selected between A and B
IRQ2 and IRQ3

ignore: SIZ0, SIZ1: require alignment for FIFO access
ignore: FC0–FC2

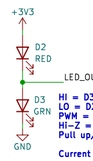
RP PicoW



dsack will have a timeout when the pico is asserting and all other times it will be an input for /reset also functions as a pull up for dsack# handy :)

resistors only in case need to bodge no electrical need for them.

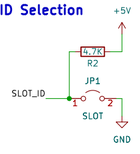
LEDs



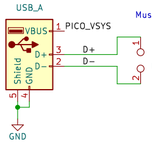
HI = D3 on
LO = D2 on
PWM = both
HI-Z = neither
Pull up/down = dim

Current limited by pico GPIO

Slot ID Selection



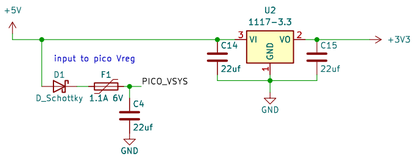
USB Host Port



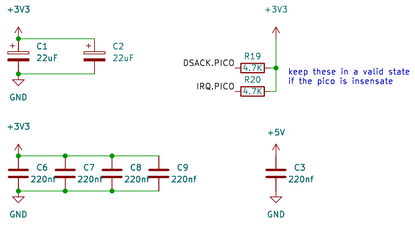
Must jump these pads to the pico.

Power

Pico must not backfeed host when USB powered or backfeed USB micro when host powered



Power, pullups, etc



zigzagjoe/MD

Sheet: /
File: PDSPico.kicad_sch

Title: PDSPico for 68030

Size: C	Date: 2024-02-27	Rev: v0.2
KiCad E.D.A. eeschema 7.0.9		Id: 1/1