

Peer's LCD Pages

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[General info](#)
[8051 example](#)
[PIC example](#)
[Misc. examples](#)
[Manuf./Distrib.](#)
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How to control a HD44780-based Character-LCD

(Industry-Standard-Character-LCD)

General info and code-examples

Visitor # **1039809**

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line

0. Table Of Contents

- 1. General
 - 1.1. Disclaimer
 - 1.2. Usage
 - 1.3. Purpose
- 2. HD44780-based LCD modules
 - 2.1. Pin assignment
 - 2.2. Instruction set
 - 2.3. Visible DDRAM addresses
 - 2.3.1. 1-line displays
 - 2.3.2. 2-line displays
 - 2.3.3. 4-line displays
 - 2.4. Interfacing
 - 2.4.1. 8-bit interface
 - 2.4.2. 4-bit interface
 - 2.5. Character set
 - 2.6. Related pages
- 3. 8051 example
 - 3.1. Basic control software
 - 3.1.1. Requirements / features
 - 3.1.2. Global declarations
 - 3.1.2.1. Register declarations
 - 3.1.2.2. Literal declarations
 - 3.1.2.3. Procedure declarations / library interface
 - 3.1.3. Code
 - 3.1.3.1. LCD initialisation
 - 3.1.3.2. Busy flag
 - 3.1.3.3. Clear display
 - 3.1.3.4. Cursor home
 - 3.1.3.5. Entry mode
 - 3.1.3.6. Display mode
 - 3.1.3.7. Set character generator RAM address
 - 3.1.3.8. Set display data RAM address
 - 3.1.3.9. Get address counter contents
 - 3.1.3.10. Write character
 - 3.2. Advanced control software
 - 3.2.1. Requirements / features
 - 3.2.2. Global declarations
 - 3.2.2.1. Procedure declarations / library interface
 - 3.2.3. Code
 - 3.2.3.1. User defined characters
 - 3.2.3.2. Set cursor position
 - 3.2.3.3. Write character
 - 3.2.3.4. Write string
 - ...
 - 3.3. Availability
 - 3.4. Target hardware
 - 3.4.1. Controller
 - 3.4.2. Interface
 - 3.4.2.1. LCD interface
 - 3.4.2.2. Address decoder example
 - 3.5. Development environment
 - 3.5.1. Software
 - 3.5.2. Hardware
- 4. PIC example
 - 4.1. Basic control software
 - 4.1.1. Requirements / features
 - 4.1.2. Global declarations
 - 4.1.2.1. Register declarations

- 4.1.2.2. Literal declarations
 - 4.1.2.3. Procedure declarations / library interface
 - 4.1.3. Code
 - 4.1.3.1. LCD initialisation
 - 4.1.3.2. Busy flag
 - 4.1.3.3. Clear display
 - 4.1.3.4. Cursor home
 - 4.1.3.5. Entry mode
 - 4.1.3.6. Display mode
 - 4.1.3.7. Set character generator RAM address
 - 4.1.3.8. Set display data RAM address
 - 4.1.3.9. Get address counter contents
 - 4.1.3.10. Write character
 - 4.1.3.11. Write command
 - 4.1.3.12. Delay loops
 - 4.2. Advanced control software
 - 4.2.1. User defined characters
 - ...
 - 4.3. Availability
 - 4.4. Target hardware
 - 4.4.1 Controller
 - 4.4.2 Interface
 - 4.5. Development environment
 - 4.5.1. Software
 - 4.5.2. Hardware
- 5. Miscellaneous examples
 - 5.1. PIC16C54 using only 3 lines
 - 5.2. ATMEL AT90S2313-10PI C-demo
 - 5.3. Variant on PIC16C54 using only 3 lines
 - 5.4. Other information sources
- 6. Manufacturers and Distributors
 - 6.1. Europe
 - 6.2. North America
 - 6.3. South America
 - 6.4. Others

line

1. General

TOC

line

1.1. Disclaimer

THIS DOCUMENT IS PROVIDED TO THE USER "AS IS". Etc.etc.

All information in this document is to the best of my knowledge.

The 8051 PL/M51 software is used in applications using 2*16, 2*20, 4*20 and 2*40 LC-Displays.

The PIC ASM software is used in applications using 2*20, 4*20 and 2*40 LC-Displays.

So there should be no risk, but there's still Murphy.

TOC

line

1.2. Usage

Tell me about your applications.

Send a postcard

TOC

line

1.3. Purpose

Uuuhm..

TOC

line

2. HD44780-based LCD modules

Data from *HITACHI LIQUID CRYSTAL CHARACTER DISPLAY MODULE* and *OPTREX DOT MATRIX LCD MODULE* databooks.

[TOC](#)
line

2.1. Pin assignment

The pin assignment shown in *Table 2.1.* is the industry standard for character LCD-modules with a *maximum* of 80 characters. The pin assignment shown in *Table 2.2.* is the industry standard for character LCD-modules with *more than* 80 characters.

To be sure **always** check the manufacturers datasheet!
To locate pin 1 on a module check the manufacturers datasheet!

Table 2.1., Pin assignment for <= 80 character displays

Pin number	Symbol	Level	I/O	Function
1	Vss	-	-	Power supply (GND)
2	Vcc	-	-	Power supply (+5V)
3	Vee	-	-	Contrast adjust
4	RS	0/1	I	0 = Instruction input 1 = Data input
5	R/W	0/1	I	0 = Write to LCD module 1 = Read from LCD module
6	E	1, 1-->0	I	Enable signal
7	DB0	0/1	I/O	Data bus line 0 (LSB)
8	DB1	0/1	I/O	Data bus line 1
9	DB2	0/1	I/O	Data bus line 2
10	DB3	0/1	I/O	Data bus line 3
11	DB4	0/1	I/O	Data bus line 4
12	DB5	0/1	I/O	Data bus line 5
13	DB6	0/1	I/O	Data bus line 6
14	DB7	0/1	I/O	Data bus line 7 (MSB)

Table 2.2., Pin assignment for > 80 character displays

Pin number	Symbol	Level	I/O	Function
1	DB7	0/1	I/O	Data bus line 7 (MSB)
2	DB6	0/1	I/O	Data bus line 6
3	DB5	0/1	I/O	Data bus line 5
4	DB4	0/1	I/O	Data bus line 4
5	DB3	0/1	I/O	Data bus line 3
6	DB2	0/1	I/O	Data bus line 2
7	DB1	0/1	I/O	Data bus line 1
8	DB0	0/1	I/O	Data bus line 0 (LSB)
9	E1	1, 1->0	I	Enable signal row 0 & 1
10	R/W	0/1	I	0 = Write to LCD module 1 = Read from LCD module
11	RS	0/1	I	0 = Instruction input 1 = Data input
12	Vee	-	-	Contrast adjust
13	Vss	-	-	Power supply (GND)
14	Vcc	-	-	Power supply (+5V)
15	E2	1, 1->0	I	Enable signal row 2 & 3
16	n.c.			

[TOC](#)
line

2.2. Instruction set

Table 2.3. HD44780 instruction set

Instruction	Code										Description	Execution time**
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and returns cursor to the home position (address 0).	1.64mS
Cursor home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position (address 0). Also returns display being shifted to the original position. DDRAM contents remains unchanged.	1.64mS
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction (I/D), specifies to shift the display (S). These operations are performed during data read/write.	40uS
Display On/Off control	0	0	0	0	0	0	1	D	C	B	Sets On/Off of all display (D), cursor On/Off (C) and blink of cursor position character (B).	40uS
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Sets cursor-move or display-shift (S/C), shift direction (R/L). DDRAM contents remains unchanged.	40uS
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display line (N) and character font(F).	40uS
Set CGRAM address	0	0	0	1	CGRAM address						Sets the CGRAM address. CGRAM data is sent and received after this setting.	40uS
Set DDRAM address	0	0	1	DDRAM address							Sets the DDRAM address. DDRAM data is sent and received after this setting.	40uS
Read busy-flag and address counter	0	1	BF	CGRAM / DDRAM address							Reads Busy-flag (BF) indicating internal operation is being performed and reads CGRAM or DDRAM address counter contents (depending on previous instruction).	0uS
Write to CGRAM or DDRAM	1	0	write data								Writes data to CGRAM or DDRAM.	40uS
Read from CGRAM or DDRAM	1	1	read data								Reads data from CGRAM or DDRAM.	40uS

Remarks:

- DDRAM = Display Data RAM.
- CGRAM = Character Generator RAM.
- DDRAM address corresponds to cursor position.
- * = Don't care.
- ** = Based on Fosc = 250KHz.

Table 2.4. Bit names

Bit name	Settings	
I/D	0 = Decrement cursor position	1 = Increment cursor position
S	0 = No display shift	1 = Display shift
D	0 = Display off	1 = Display on
C	0 = Cursor off	1 = Cursor on
B	0 = Cursor blink off	1 = Cursor blink on
S/C	0 = Move cursor	1 = Shift display
R/L	0 = Shift left	1 = Shift right
DL	0 = 4-bit interface	1 = 8-bit interface
N	0 = 1/8 or 1/11 Duty (1 line)	1 = 1/16 Duty (2 lines)
F	0 = 5x7 dots	1 = 5x10 dots
BF	0 = Can accept instruction	1 = Internal operation in progress

TOC
line

2.3. Visible DDRAM addresses

TOC
line

2.3.1. 1-line displays

Shown after reset (with N=0).

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 + Character position (dec.)
 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 + Row0 DDRAM address (hex)

Table 2.5. DDRAM address usage for a 1-line LCD

Display size	Visible	
	Character positions	DDRAM addresses
1*8	00..07	00h..07h
1*16	00..15 [1] [2] [3]	00h..0Fh
1*20	00..19	00h..13h
1*24	00..23	00h..17h
1*32	00..31	00h..1Fh
1*40	00..39	00h..27h

[1] Peter Bozzay:

Found DDRAM addresses 00h..07h + 40h..47h to be functional for a 1*16 display size.

Make/model: not mentioned / SC1601AS*B.

[2] Hendrik Abma:

Found DDRAM addresses 00h..07h + 40h..47h to be functional for a 1*16 display size.

Make/model: Samtron / KP-03.

[3] Luigi Candurro:

Found DDRAM addresses 00h..07h + 40h..47h to be functional for a 1*16 display size.

Make/model: [Crystal Clear Technology](#) / CMC116-01.

TOC

line

2.3.2. 2-line displays

Shown after reset (with N=1).

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	← Character position (dec.)
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	← Row0 DDRAM address (hex)
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	← Row1 DDRAM address (hex)

Table 2.6. DDRAM address usage for a 2-line LCD

Display size	Visible	
	Character positions	DDRAM addresses
2*16	00..15 [1]	00h..0Fh + 40h..4Fh
2*20	00..19	00h..13h + 40h..53h
2*24	00..23	00h..17h + 40h..57h
2*32	00..31	00h..1Fh + 40h..5Fh
2*40	00..39	00h..27h + 40h..67h

[1] Author:

According to their datasheets DDRAM addresses 80h..8Fh + C0h..CFh are used.

Make/model: [Emerging Display Technologies](#) / EW162G0YMY (Local copy available [here](#) as zipped file).

Make/model: [Mitsutech](#) / EW162G0YMY (Local copy available [here](#) as zipped file).

TOC

line

2.3.3. 4-line displays

Shown after reset (with N=1).

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	← Character position (dec.)
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	← Row0 DDRAM address (hex)
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	← Row1 DDRAM address (hex)
14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	← Row2 DDRAM address (hex)
54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	← Row3 DDRAM address (hex)

Table 2.7. DDRAM address usage for a 4-line LCD

Display size	Visible	
	Character positions	DDRAM addresses
4*16	00..15 [1] [2]	00h..0Fh + 40h..4Fh + 14h..23h + 54h..63h
4*20	00..19	00h..13h + 40h..53h + 14h..27h + 54h..67h
4*40	(00..39) on 1 st controller and (00..39) on 2 nd	(00h..27h + 40h..67h) on 1 st controller and (00h..27h + 40h..67h) on 2 nd

[1] Rick Mann:

Found DDRAM addresses 00h..0Fh + 40h..4Fh + 10h..1Fh + 50h..5Fh to be functional for a 4*16 display size.

Make/model: [Optrex](#) / DMC16433.

Author:

This matches with the information mentioned in [Dmcmann_full.pdf](#) paragraph 1.7.6.4. Local copy available [here](#) as zipped file.

[2] Tushar Rane:

Found DDRAM addresses 00h..0Fh + 40h..4Fh + 10h..1Fh + 50h..5Fh to be functional for a 4*16 display size.

Make/model: not mentioned / not mentioned.

TOC

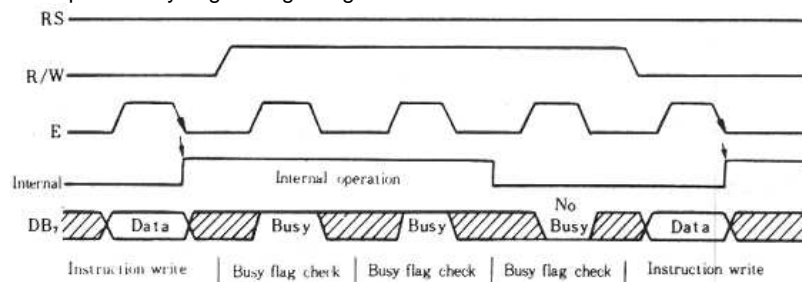
line

2.4. Interfacing

TOC
line

2.4.1. 8-bit interface

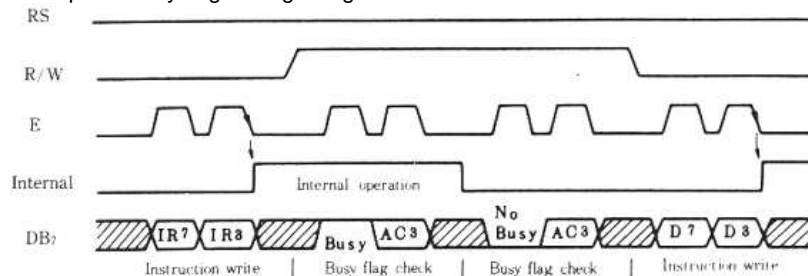
Example of busy flag testing using an 8-bit interface.



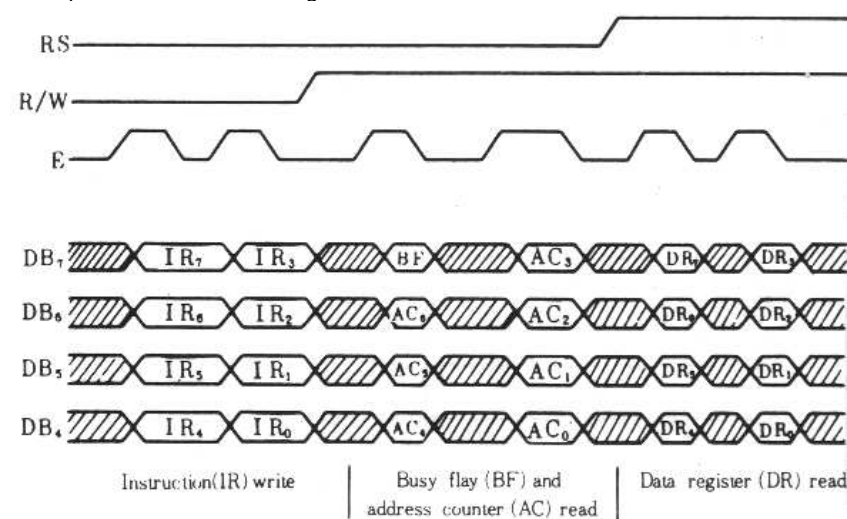
TOC
line

2.4.2. 4-bit interface

Example of busy flag testing using a 4-bit interface.



Example of data transfer using a 4-bit interface.




TOC
line

2.5. Character set

Character set for 5x7 dot font (to be completed..)

Char. code



xxxx0000		0	0	0	0	0	0	1	1	1	1	1	1
xxxx0001	!	1	A	Q	a	q	.	7	7	4	ä	q	
xxxx0010	"	2	B	R	b	r	"	7	7	7	ß	ß	
xxxx0011	#	3	C	S	c	s	7	7	7	£	£	£	
xxxx0100	\$	4	O	T	d	t	.	7	7	7	ü	ü	
xxxx0101	%	5	E	U	e	u	.	7	7	7	ü	ü	
xxxx0110	&	6	F	V	f	v	7	7	7	7	7	7	
xxxx0111	'	7	G	W	g	w	7	7	7	7	7	7	
xxxx1000	(8	H	X	h	x	7	7	7	7	7	7	
xxxx1001)	9	I	Y	i	y	7	7	7	7	7	7	
xxxx1010	*	:	J	Z	j	z	7	7	7	7	7	7	
xxxx1011	+	:	K	[k	[7	7	7	7	7	7	
xxxx1100	,	<	L	¥	l	¥	7	7	7	7	7	7	
xxxx1101	-	=	M]	m]	7	7	7	7	7	7	
xxxx1110	.	>	N	^	n	^	7	7	7	7	7	7	
xxxx1111	/	?	O	_	o	_	7	7	7	7	7	7	

[Shift-Click to download gif.](#)

TOC

line

2.6. Related pages

Private sites:

- [Fil's FAQ-Link-In Corner: LCD Technology FAQ](#)
- [Fil's FAQ-Link-In Corner: HD44780-based LCD](#)
- [LCD Module to PC Interfacing Example](#)
- [HD44780-based LCD Modules](#)

Commercial sites:

- [LCD Intro](#)
- [HANTRONIX, Inc. Home Page](#)
- [Shelly, Inc. - LCD Engineering Application Notes](#)

TOC

line

[General info](#) | [8051 example](#) | [PIC example](#) | [Misc. examples](#) | [Manuf./Distrib.](#) | [Home](#) | [Sign Guestbook](#)
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