Zihua Zhao

Undergraduate in Computer Science

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Education

Shanghai Jiao Tong University   *Shanghai, China*

HONORS BACHELOR OF SCIENCE(B.SC. HONS) IN COMPTER SICENCE   *September 2017-Present*

- Member of ACM Class, which is an elite CS program for top 5% talented students.

Research Experiences

Research Interests

CURRENT RESEARCH INTERESTS AND RESEARCH FIELDS.   *July 2019 - PRESENT*

- Natural Language Processing, Machine Learning

Department of Computer Science and Engineering   *Shanghai Jiao Tong University*

UNDERGRADUATE RESEARCHER   *July 2019 - PRESENT*

- Advised by Prof.Hai Zhao.
- Research interests: Natural Language Processing, Machine Learning.

Capsule Network to replace Attention   *Department of Computer Science and Engineering*

USE CAPSULE NETWORK TO REPLACE ATTENTION.   *October 2019-Present*

- More MRC models adopt multiple attention layers to capture correlation, but a negative consequence is the explosion of parameters. So Capsule Network is used to replace attention layer.
- Work still working on in the lab.

Honors

Zhiyuan Honorary Scholarship   *Shanghai Jiao Tong University*
                                                                                                                    2017 & 2018

The Second Aword for Robomaster   *Shanghai Jiao Tong University*

ELECTRONIC CONTROLLER, MANIPULATOR   *Fall 2018*

- Robomaster is a competition to design and control robots to fight against other teams.
- Robot of our team finally ranked the fifth and got the secind reward for the competition.

Selected Projects

Mx-Compiler   *https://github.com/ZihuaZhao/Compiler*

A COMPILER FOR MX* LANGUAGE   *Spring 2019*

- It is a compiler implemented in Java from scratch, and the source language is Mx*, which is a C-and-Java-like language.
- The compiler is implemented with Sementic Analysis, Dead Code Elimination, Register Allocation methods, etc.

RISC-V   *https://github.com/ZihuaZhao/RISC_V*

A RISC-V CPU ON FPGA   *Fall 2018*

- Designed and implemented a FPGA-supported RISC-V CPU with 5-stage pipeline implemented in Verilog HDL.

Railway Management System   *https://github.com/ZihuaZhao/Railway-Management-System*

RAILWAY TICKET MANAGEMENT SYSTEM   *May 2018*

- Backend Development, including a B-plus tree.
- Group project for Data Structure 2018 (CS147), ACM Class, SJTU.

Text Classification

ENSEMBLED MODELS TO PREDICT WHETHER THE COMMENT IS POSITIVE OR NEGATIVE.

- Seperating the sentences word by word performs the best. XGBoost, NN, CNN ensembled to predict the result.
- The model has exceeded the strong base line.
- Practising project for Maching Learning 2019 taught by Prof. Weinan Zhang, ACM Class, SJTU.

Skills

Skills   Python, Java, C/C++