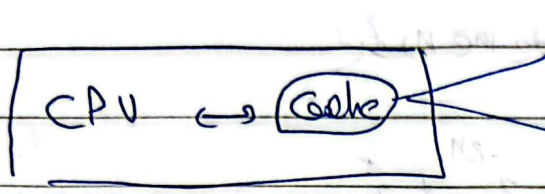
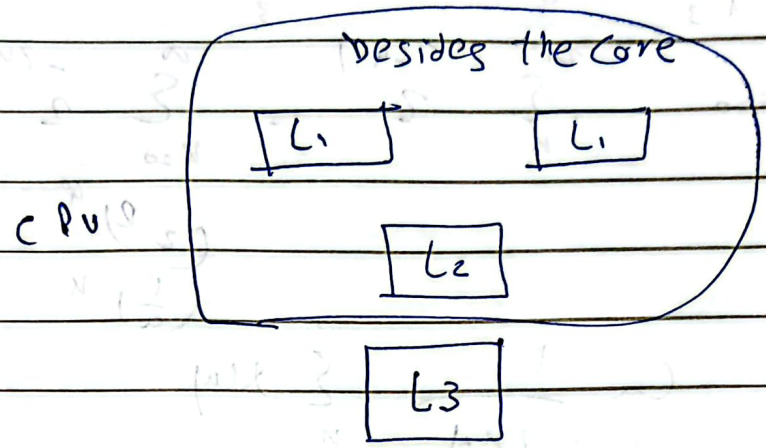
Date: Page:



Cashe has levels

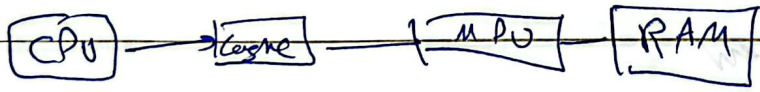


* → cashe Coherence → to make sure that any change in one of the caches reaches the other.

* hit ratio = $\frac{\#hits}{\#total}$

* FPU → floating point unit → used for operations on floating numbers.

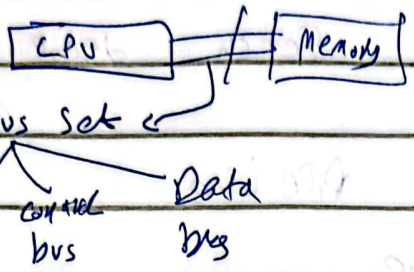
* MPU → memory protection unit → between cashe and ram

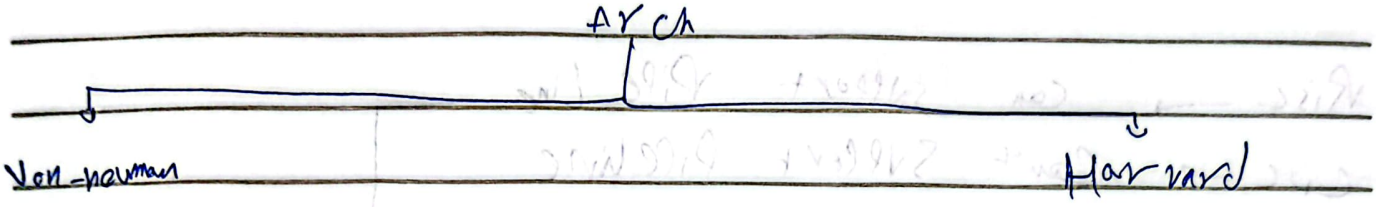


* MMU → (memory managment unit.

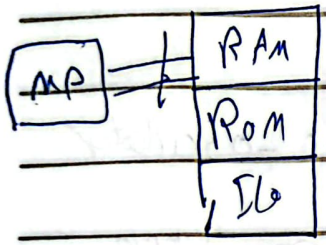
Date: Page:

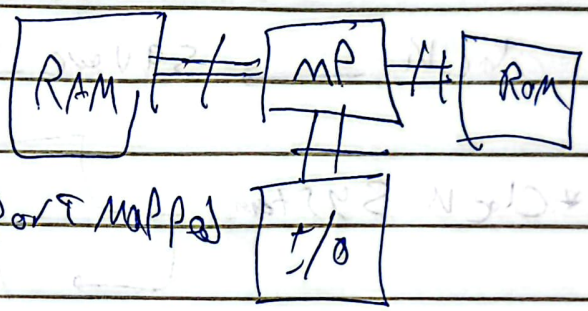
~~I/O techniques~~ :-





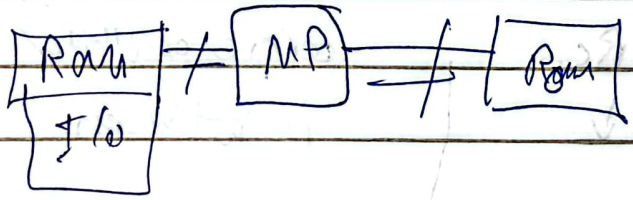
one memory system





I/O → Port Mapped

I/O (Harvard)



I/O → memory mapped

- To talk to ram we can use C programming to convert into Load/store assembly instructions
- To access ROM we use ASS directly

Date: Page:

→ Pipelining — Fetch decode exu
Fetch decode exu
Fetch decode exu

→ Von neuman → Can't support Pipe Line
→ Harvad → support Pipe Line

Risc → Can support Pipe Line
Cisc → Can't Support Pipeline
Finish in 1 clock

clock → square wave

*Clock System → electrical | Rc-oscillator
→ Mechanical | Material → wave
power

	Rc	ceramic oscillator	crystall oscillator
cost	↓	in between	↑
~~accuracy~~ accuricy	↓	~	↑
setting time	↑	~	↓
Noise Immunity			

ROXi

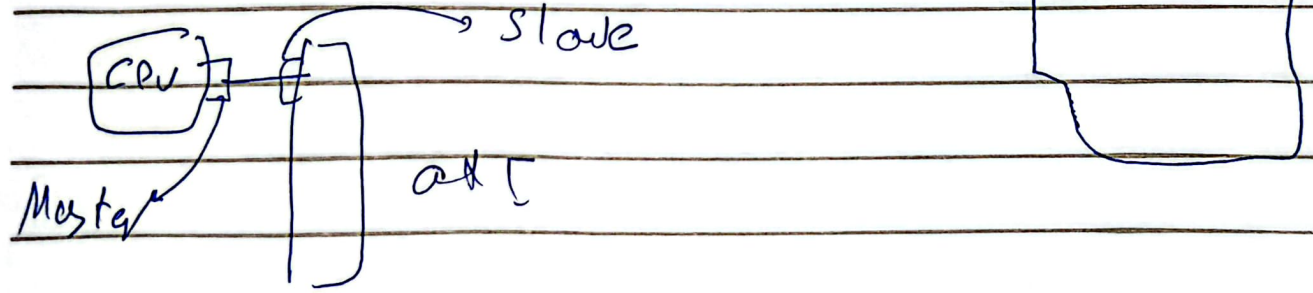
Date: Page:

	RC	ceramic	crystal
temp imm	↓	↑	↑
	↓	↑	↑
Emit	↓	↑	↑
vibrating	↑	↓	↓

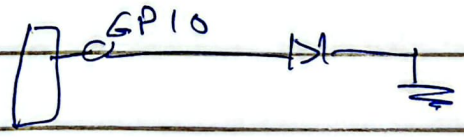
Peripherals → (HW civ + Reg)

* TRM → Tech Ref Manual
→ specs

* specs → TRM
→ memory Map
→ GPIO



Ex SW → Low High

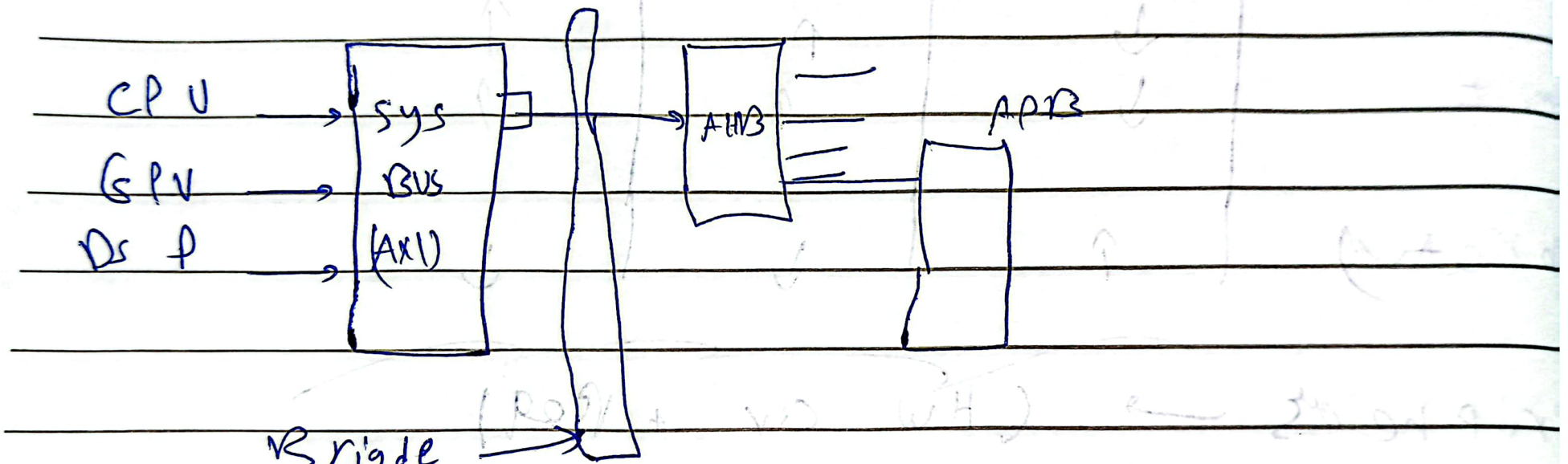


① Pointer → DR → 1 (GPIO)
↓
(Base + offset)

② Pointer → ODR → 1 (High)

Date: Page:

Bus Bridges



AXI → AHB