

```
[<c219ec5f>] security_sk_free+0xf/0x2
[<c2451efb>] __sk_free+0x9b/0x120
[<c25ae7c1>] ? _raw_spin_unlock_irqre
[<c2451ffd>] sk_free+0x1d/0x30
[<c24f1024>] unix_release_sock+0x174/
```

#### Hardware Transactional Memory (2)

**Mohamed Mohamedin** 

**Chapter 5 of TM Book** 





#### **HTM Limitation**

- Best-efforts
  - Transactions are not guaranteed to commit
  - Must provide a software fallback path





# Non-Speculative Fallback

```
if ( xbegin() == XBEGIN STARTED) {
  read lock state
  if (lock taken) xabort();
  work;
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```



# Non-Speculative Fallback

```
if ( xbeqin() == XBEGIN STARTED)
  read lock state
     (lock taken) xabort();
  work;
   xend()
         reading lock ensures that
     transaction will abort if another
           thread acquires lock
```



# Non-Speculative Fallback

```
if ( xbegin() == XBEGIN STARTED)
  read lock state
  if (lock taken) xabort();
  work;
  xend()
  else {
     abort if another thread has
  WO
            acquired lock
```

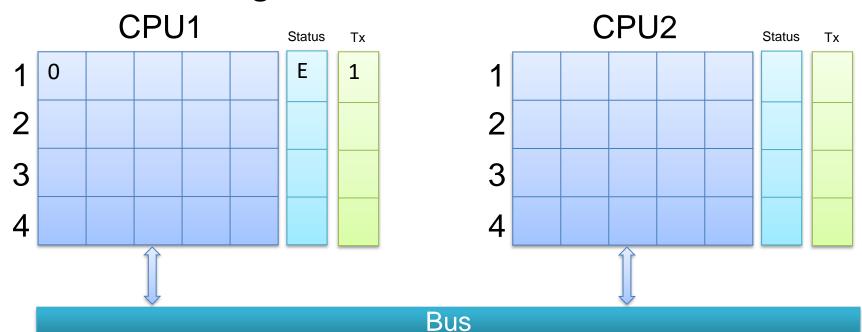


```
on abort, acquire lock & do work
      (aborting concurrent speculative
if
                transactions)
  if (lock taken) xabort();
  work;
   xend()
  else {
  lock->lock();
  work;
  lock->unlock();
```



#### Global Lock Fallback

- Must define a software fallback path
  - Default is global lock



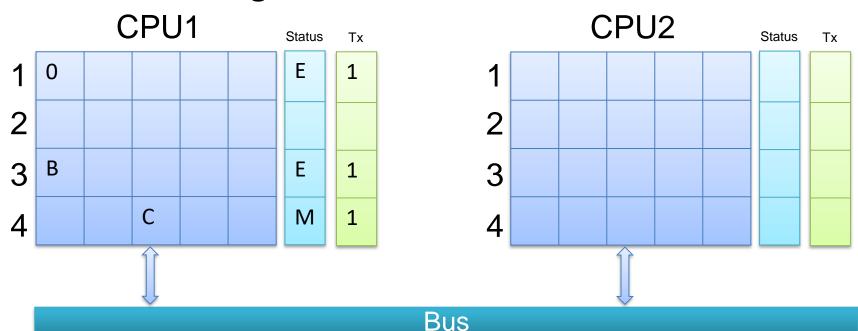
- \_xbegin()
- if (read(lock)) == 1 then \_xabort()





#### Global Lock Fallback

- Must define a software fallback path
  - Default is global lock



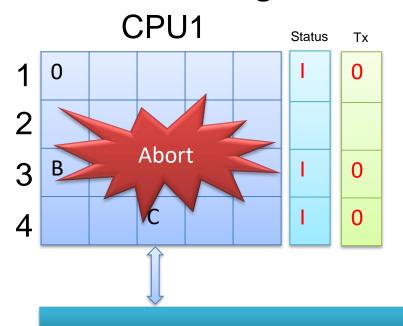
- \_xbegin()
- if (read(lock)) == 1 then \_xabort()
- do some work

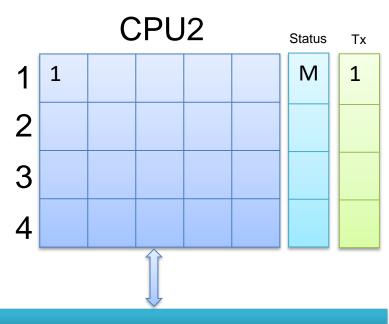




#### Global Lock Fallback

- Must define a software fallback path
  - Default is global lock





#### Bus

- \_xbegin()
- if (read(lock)) == 1 then \_xabort()
- do some work

//non-transactionally CAS(lock, 0,1)





#### Global Clock Fallback

#### Pros

- Very easy to program
- 100% safe

#### Cons

- Unnecessary aborts concurrent HTM transactions
- Limit concurrency
- Lemming effect
  - Cascading the failures in HTM, ending up with all transactions running in the global lock fallback path





### Enhancing the Fallback Path

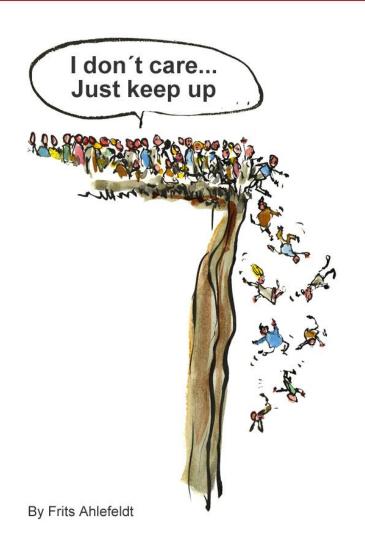
#### Target

- Enhance concurrency
  - Allow non-conflicting HTM transaction to run with the fallback path
- Low overhead on HTM
  - An instrumentation is needed to communicate between HTM and the fallback path
    - E.g., The Global Lock
  - A heavy instrumentation would annul the advantages of HTM
- Allow most transactions to commit in HW
  - No lemming effect





- Once a transaction take the fallback path → All remaining transactions follows
- How?







```
if (xbegin() == XBEGIN STARTED) {
  read lock state
  if (lock taken) xabort();
  work;
                    Lock is in the read-set of the HTM
   xend()
                    transaction, then when it is locked
                    in the fallback path (a write), a
} else {
                    conflict aborts the HTM transacion
  lock->lock()
  work;
  lock->unlock();
```





 Upon immediate retry, all HTM transactions will abort since the lock is already acquired

```
if ( xbegin() == XBEGIN STARTED) {
  read lock state
  if (lock taken) xabort();
  work;
                          Lock is already taken, so all HTM
   xend()
                          retries will abort immediately
} else {
  lock->lock();
  work;
  lock->unlock();
```





Hence, all HTM transaction will take the fallback path

```
if (xbegin() == XBEGIN STARTED) {
  read lock state
  if (lock taken) xabort();
  work;
   xend()
} else {
                        All HTM transaction will fallback to
  lock->lock();
                        the global lock
  work;
  lock->unlock();
```





 This behavior will continue until the next quiescent time

```
if ( xbegin() == XBEGIN STARTED) {
  read lock state
  if (lock taken) xabort();
  work;
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





- Eliminating lemming effect is easy
  - Wait for the lock to be free before retrying

```
while (lock taken) wait();
if ( xbegin() ==
                               STARTED
  read lock stat Wait until lock is free before trying
                    an HTM transaction again
  if (lock taken
                      AGDUL C ( ) ,
  work;
   xend()
 else {
  lock->lock();
  work;
  lock->unlock();
```





Move global lock checking to the end of a transaction

```
if (xbegin() == XBEGIN STARTED) {
  //Do transaction work first
  work;
  //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





Why this is beneficial?

It allows more concurrency

```
if ( xbegin() == XBEGIN STARTED) {
  //Do transaction work first
  work;
  //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





Concurrent transactions will not immediately abort

```
if ( xbegin() == XBEGIN STARTED) {
  //Do transaction work first
  work;
  //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





 New transactions will be allowed to start while the global lock is acquired

```
if (xbegin() == XBEGIN STARTED) {
  //Do transaction work first
  work;
  //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





What about safety?

HTM transactions can access intermediate changes!

```
if (xbegin() == XBEGIN STARTED) {
  //Do transaction work first
  work;
  //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
  work;
  lock->unlock();
```





- What about safety?
  - HTM is sandboxed and exceptions or infinite loops will the transaction

```
if (xbegin() == XBEGIN STARTED) {
  //Do transaction work first
 work;
 //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
 work;
  lock->unlock();
```



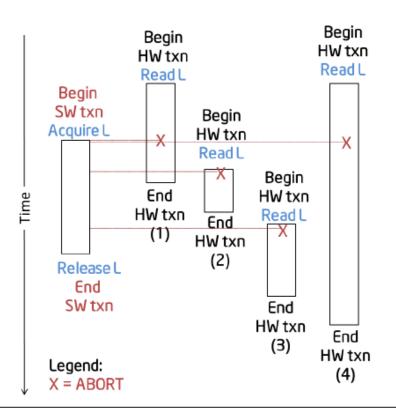


- What about safety?
  - Unfortunately, current HTM implementation is not 100% sandboxed

```
if (xbegin() == XBEGIN STARTED) {
  //Do transaction work first
 work;
 //Check lock just before committing
  if (lock taken) xabort();
  xend()
} else {
  lock->lock();
 work;
  lock->unlock();
```







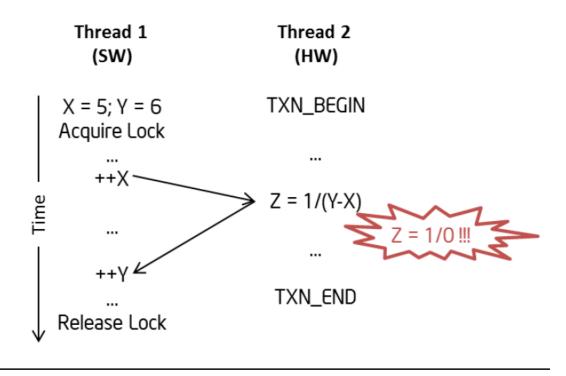
Begin Begin HW txn HW txn Begin SW txn Begin Acquire L HW txn Begin Read L HW txn Read L End HW txn End HW txn (1) (2)Release L End Read L SW txn End Read L HW txn End (3)HW txn COMMIT Legend: (4)COMMIT X = ABORT

**Figure 1.** Obvious SGL Fallback implementation (E-SGL).

Figure 2. Lazy SGL (L-SGL).



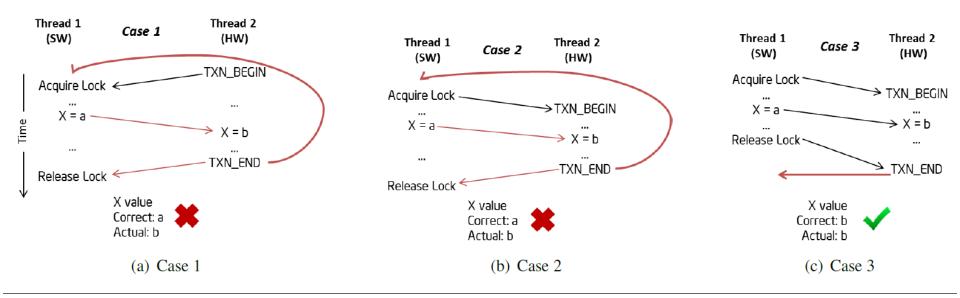




**Figure 3.** Inconsistent reads.







**Figure 4.** Correctness: Cases 1-3. Arrows denote the "happens-before" relation.





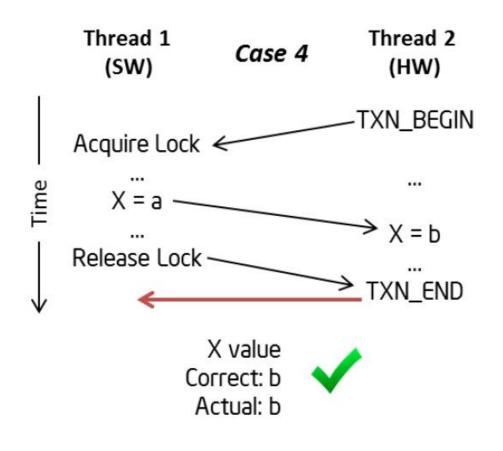


Figure 5. Correctness: Case 4.





Observing inconsistent state

```
void (*method_table[2])() = {method1, method2};

int next_method = 0;

lock L;

void apply_next() {
    acquire(L);
    (*method_table[next_method])();
    if (++next_method > 2)
        next_method = 0;
    release(L);
}
```





#### Indirect branch

```
void (*method_table[2])() = {method1, method2};

int next_method = 0;

lock L;

void apply_next() {
    acquire(L);
    (*method_table[next_method])();
    if (++next_method > 2)
        next_method = 0;
    release(L);
}
```





- Lock scribbling
- Subscribing to the wrong "lock"
- Self modifying code
- Corrupted return address





#### Conclusion

- Lazy Subscription is too risky on current architectures
- HW must be modified first to support complete sandboxing





- When should we retry?
- How many retrials are enough?
- Should we try HTM in the first place?





#### Algorithm 1 TSX in GCC

```
1: int attempts \leftarrow 2
 2: int status \leftarrow XBEGIN
 3: if status \neq ok then
      if attempts = 0 then
         acquire(globalLock)
 5:
    else
 6:
 7:
         attempts—
         goto line 2
 9: if is_locked(globalLock)
10:
      XABORT
11: ▷ ...transactional code
12: if attempts = 0 then
      release(globalLock)
13:
14: else
```

#### Abort code

retry: Transient failure conflict: Contention to data capacity: Exceeded cache explicit: XABORT invoked other: Faults, preemption, ...

Fig. 2. Error codes in TSX.

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XEND

15:



```
Algorithm 1 TSX in GCC
 1: int attempts \leftarrow 2
 2: int status \leftarrow XBEGIN
 3: if status \neq ok then
                                  This code ignores the status code
      if attempts = 0 then
 4:
                                  and just retry without considering
         acquire(globalLock)
                                                                     failure
 5:
                                       the reason of the abort
     else
 6:
                                                                    on to data
 7:
                                                 capacity: Exceeded cache
         attempts—
         goto line 2
                                                explicit: XABORT invoked
 9: if is_locked(globalLock)
                                               other: Faults, preemption, ...
10:
      XABORT
11: ▷ ...transactional code
                                              Fig. 2. Error codes in TSX.
12: if attempts = 0 then
      release(globalLock)
13:
14: else
                                                     *Self-Tuning Intel Transactional
15:
      XEND
                                                    Synchronization Extensions
```





#### **Algorithm 2** Heuristic based approach for TSX.

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                                ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
      if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
           attempts \leftarrow attempts - 1
                                                                                           9:
         else if status = capacity then
10:
           attempts \leftarrow 0
11:
                                                                             ⊳ give up, likely that it always fails
         goto line 2
12:
13: ▷ ...code to run in transaction
14: if attempts = 0 then
      release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
                                                                        > check for concurrent pessimistic thread
         XABORT
19:
      XEND
```

\*Self-Tuning Intel Transactional Synchronization Extensions





```
Algorithm 2 Heuristic based approach for TSX.
```

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                             ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
                                           Avoid lemming effect by waiting for
      if attempts = 0 then
                                                global lock to be free before
         acquire(global-lock)
      else
                                              attempting an HTM transaction
         if status = explicit \lor status =
           attempts \leftarrow attempts - 1
                                                                                         9:
         else if status = capacity then
10:
           attempts \leftarrow 0
                                                                           ⊳ give up, likely that it always fails
11:
        goto line 2
12:
13: ▷ ...code to run in transaction
14: if attempts = 0 then
      release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
                                                                      > check for concurrent pessimistic thread
        XABORT
19:
      XEND
```





```
Algorithm 2 Heuristic based approach for TSX.
```

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                                 k86 instruction
 3: int status \leftarrow XBEGIN
                                                    If the abort is explicit or for "other"
 4: if status \neq ok then
                                                       reasons, consume one attempt
      if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
           attempts \leftarrow attempts - 1
                                                                                          9:
        else if status = capacity then
10:
           attempts \leftarrow 0
                                                                            ⊳ give up, likely that it always fails
11:
        goto line 2
12:
13: ▷ ...code to run in transaction
14: if attempts = 0 then
      release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
                                                                      > check for concurrent pessimistic thread
        XABORT
19:
      XEND
```





```
Algorithm 2 Heuristic based approach for TSX.
```

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                             ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
      if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
           attempts \leftarrow attempts - 1
                                                                                         9:
         else if status = capacity then
10:
           attempts \leftarrow 0
                                                                                            that it always fails
11:
                                                    Capacity aborts consume all
        goto line 2
12:
                                                 attempts as there is no benefit in
13: ▷ ...code to run in transaction
                                               retrying a transaction that doesn't fit
14: if attempts = 0 then
      release(global-lock)
                                                                in HTM
15:
16: else
      if is_locked(global-lock) then
17:
18:
                                                                      > check for concurrent pessimistic thread
        XABORT
19:
      XEND
```





#### **Algorithm 2** Heuristic based approach for TSX.

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
       if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
            attempts \leftarrow attempts - 1
 9:
         else if status = capacity then
10:
            attempts \leftarrow 0
11:
         goto line 2
12:
13: ▷ ...code to run in transaction
14: if attempts = 0 then
       release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
         XABORT
19:
      XEND
```

⊳ x86 instruction

Conflict & Retry aborts do NOT consume any attempts as these are normal expected TM aborts

▷ check for concurrent pessimistic thread





```
Algorithm 2 Heuristic based approach for TSX.
 1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                             ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
      if attempts = 0 then
         acquire(global-lock)
                                       When all attempts are consumed,
      else
                                              acquire the global lock
        if status = explicit \lor sta
           attempts \leftarrow attempts -
                                                                                         9:
        else if status = capacity
10:
           attempts \leftarrow 0
                                                                           ⊳ give up, likely that it always fails
11:
        goto line 2
12:
13: ▷ ...code to run in transaction
14: if attempts = 0 then
      release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
                                                                     > check for concurrent pessimistic thread
        XABORT
19:
      XEND
```





```
Algorithm 2 Heuristic based approach for TSX.
```

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                              ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
      if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
           attempts \leftarrow attempts - 1
                                                                                          9:
         else if status = capacity then
10:
           attempts \leftarrow 0
                                                                            ⊳ give up, likely that it always fails
11:
        goto line 2
12:
13: ▷ ...code to run in transactio
14: if attempts = 0 then
                                  If attempt are zero, then I must have
      release(global-lock)
15:
                                  acquired the lock and need to unlock
16: else
                                                       it
      if is_locked(global-lock) tl
17:
18:
                                                                                br concurrent pessimistic thread
        XABORT
19:
      XEND
```





```
Algorithm 2 Heuristic based approach for TSX.
```

```
1: int attempts \leftarrow 5
   ▷ avoid the lemming effect
 2: while(is_locked(global-lock)) do pause
                                                                                               ⊳ x86 instruction
 3: int status \leftarrow XBEGIN
 4: if status \neq ok then
      if attempts = 0 then
         acquire(global-lock)
      else
         if status = explicit \lor status = other then
           attempts \leftarrow attempts - 1
                                                                                          9:
         else if status = capacity then
10:
           attempts \leftarrow 0
                                                                                     b, likely that it always fails
11:
         goto line 2
12:
                                         Lazy subscription to the lock and
13: ▷ ...code to run in transaction
14: if attempts = 0 then
                                                  _xend if lock is free
      release(global-lock)
15:
16: else
      if is_locked(global-lock) then
17:
18:
        XABORT
                                                                       > check for concurrent pessimistic thread
19:
      XEND
```





#### Algorithm 3 Tuner adaptive configuration.

```
1: int ucbBelief \leftarrow \triangleright last configuration used
 2: int attempts \leftarrow \triangleright last configuration used
 3: if reoptimize() then
       long initCycles \leftarrow obtainRDTSC()
 5: while is_locked(global-lock) do pause
 6: int status ← XBEGIN
 7: if status \neq ok then
       if attempts = 0 then
 8:
          if reoptimize() then tuneAttempts(ucbBelief)
 9:
          acquire(global-lock)
10:
11:
       else
12:
         if status = capacity then
13:
            ▶ set attempts according to ucbBelief
          else if status = explicit \lor status = other then
14:
15:
            attempts \leftarrow attempts - 1
          goto line 5
16:
17: ▷ ...code to run in transaction
18: if attempts = 0 then
19:
       release (global-lock)
20: else
       if is_locked(global-lock) then XABORT
21:
22:
       XEND
23: if reoptimize() then
       long totalCycles \leftarrow obtainRDTSC() - initCycles
24:
       ucbBelief \leftarrow ucb(totalCycles)
25:
       attempts \leftarrow GRAD(totalCycles)
26:
```

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rules of Section 4.2.rules of Section 4.3.





```
Algorithm 3 Tuner adaptive configuration.
 1: int ucbBelief \leftarrow \triangleright last configuration used
 2: int attempts \leftarrow \triangleright last configuration used
 3: if reoptimize() then
      long initCycles \leftarrow obtainRDTSC()
                                                              Number of attempts is adaptive
 5: while is_locked(global-lock) do pause
 6: int status ← XBEGIN
 7: if status \neq ok then
      if attempts = 0 then
 8:
         if reoptimize() then tuneAttempts(ucbBelief)
 9:
         acquire(global-lock)
10:
11:
      else
12:
         if status = capacity then
13:
           ▶ set attempts according to ucbBelief
         else if status = explicit \lor status = other then
14:
15:
           attempts \leftarrow attempts - 1
         goto line 5
16:
17: ▷ ...code to run in transaction
18: if attempts = 0 then
      release (global-lock)
19:
20: else
      if is_locked(global-lock) then XABORT
21:
                                                                                   *Self-Tuning Intel Transactional
22:
      XEND
                                                                                  Synchronization Extensions
23: if reoptimize() then
      long totalCycles \leftarrow obtainRDTSC() - initCycles
24:
                                                                                           ▷ rules of Section 4.2.
      ucbBelief \leftarrow ucb(totalCycles)
25:
```



26:

 $attempts \leftarrow GRAD(totalCycles)$ 



rules of Section 4.3.

#### Algorithm 3 Tuner adaptive configuration.

```
1: int ucbBelief \leftarrow \triangleright last configuration used
 2: int attempts \leftarrow \triangleright last configuration used
 3: if reoptimize() then
       long initCycles \leftarrow obtainRDTSC()
 5: while is_locked(global-lock) do pause
 6: int status ← XBEGIN
 7: if status \neq ok then
       if attempts = 0 then
 8:
          if reoptimize() then tuneAttempts(ucbBelief)
 9:
          acquire(global-lock)
10:
11:
       else
12:
         if status = capacity then
13:
            ▶ set attempts according to ucbBelief
          else if status = explicit \( \times \) status = other the
14:
15:
            attempts \leftarrow attempts - 1
          goto line 5
16:
17: ▷ ...code to run in transaction
18: if attempts = 0 then
       release (global-lock)
19:
20: else
       if is_locked(global-lock) then XABORT
21:
22:
       XEND
23: if reoptimize() then
       long totalCycles \leftarrow obtainRDTSC() - initCycles
24:
       ucbBelief \leftarrow ucb(totalCycles)
25:
       attempts \leftarrow GRAD(totalCycles)
26:
```

Consuming all attempts on capacity aborts is not always the best option

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rules of Section 4.2.rules of Section 4.3.





#### Global Lock Fallback

- Even with all these optimizations
  - Once the global clock is acquired, no concurrency is allowed
  - A long running transaction acquiring the global clock will block the progress of all other transactions
    - Without having any mutual conflicts
- Can we do better?





- Mix HTM with STM
- Allows both HTM and STM to work concurrently (if possible)
  - Some proposals (e.g., PhaseTM) work in phases
     where all transactions run in HTM or STM
- Requires some instrumentation inside HTM path





- One naïve solution is to use per location metadata (Orec based STM)
  - For each read in HTM, check the associated metadata
  - Writes must acquire the associated locks to inform
     STM transactions of that write





- One naïve solution is to use per location metadata (Orec based STM)
  - The resulting algorithm performance is very bad
    - Consumes a lot of the limited HTM resources
      - Extra reads and writes due to metadata manipulation
    - Most HTM transactions abort
      - False aborts due to space limitation (metadata access)
      - False conflict due to global shared metadata access (e.g., global clock)
- What's the solution?





- Minimal instrumentation
- Minimal communication between HTM and STM
- For example, do NOT use Orecs





- Minimal instrumentation
- Minimal communication between HTM and STM
- For example, do NOT use Orecs
  - Best candidate from algorithms we learned
     NOrec





#### NOrec

- A single shared global lock is used
  - Minimal communication between STM and HTM
- Value-based validation
  - No per-location metadata
  - Minimal instrumentation inside HTM





#### NOrec STM Algorithm

```
padded unsigned seglock
                                                  SW_BEGIN
                                                                                                 SW_READ(addr)
                                                    snapshot = seglock
                                                                                                   if (addr in writes)
                                              16
    thread local unsigned snapshot
                                                     if (snapshot & 1)
                                                                                                     return writes . find (addr)
                                              17
                                                                                            30
    thread local ReadSet reads
                                                      goto 16
                                                                                                   val = *addr
                                              18
                                                                                            31
    thread local WriteSet writes
                                                                                            32
                                                                                                   if (snapshot != seqlock)
                                                                                                     SW_VALIDATE
                                                                                            33
                                                  SW COMMIT
                                                                                            34
                                                                                                    goto 31
    SW_VALIDATE
                                                     if (writes.empty())
                                                                                                   reads.append(addr, val)
                                              20
                                                                                            35
      snapshot = seglock
                                                                                                   return val
                                              21
                                                       return
                                                                                            36
      if (snapshot & 1)
                                                    while (!CAS(&seglock, snapshot,
                                              22
                                                        snapshot + 1)
                                                                                                 SW_WRITE(addr, val)
        goto 7
                                                                                            38
                                                                                                   writes.append(addr, val)
      foreach (addr, val) in reads
                                                      SW_VALIDATE
10
                                              23
                                                                                            39
        if (*addr != val)
                                                    foreach (addr, val) in writes
11
                                              24
          SW ABORT
                                                                                                SW ABORT
12
                                              25
                                                      *addr = val
                                                    seglock = seglock + 1
      if (snapshot != seglock)
                                                                                                   reads.reset(), writes.reset()
                                              26
                                                                                            42
13
        goto 7
                                                    reads reset (), writes reset ()
                                                                                                   /* restart transaction */
                                              27
                                                                                            43
14
```

\*Hybrid NOrec: A Case Study in the Effectiveness of Best Effort Hardware Transactional Memory





- Simply, subscribe to NOrec global lock at the beginning
- Increment NOrec global lock at the end to notify STM transaction of the change

```
5 HW_POST_BEGIN
```

- 6 **if** (seqlock & 1)
- 7 while (true) // await abort
- 9 HW\_PRE\_COMMIT
- seqlock = seqlock + 2





- Simply, subscribe to NOrec global lock at the beginning
- Increment NOrec global lock at the end to notify STM transaction of the change

```
5 HW_POST_BEGIN
```

- 6 **if** (seqlock & 1)
- 7 while (true)

All HTM reading seqlock will abort one this line is executed!

- 9 HW\_PRE\_COMM
- seqlock = seqlock + 2





- This improvement, reduces HTM-HTM false conflicts due to writing to seqlock
  - Shorter window of conflicts
    - 1 padded unsigned seqlock
    - 2 padded unsigned counter

```
5 HW_POST_BEGIN
```

- 6 **if** (seqlock & 1)
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- 10 counter = counter + 1





- This improvement, reduces HTM-HTM false conflicts due to writing to seqlock
  - Shorter window of conflicts
    - 1 padded unsigned seqlock
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```
5 HW_POST_BEGIN
6 if (seqlock & 1)
7 while (true) //
```

With using two locations for communication. Only HTM transactions executing this line concurrently will conflict with each other

- 9 HW\_PRE\_COMM
- 10 counter = counter + 1





 This improvement, eliminates HTM-HTM false conflicts due to writing to same counter

```
padded unsigned seqlock
padded unsigned counter[]
thread local unsigned id

HW_POST_BEGIN
f (seqlock & 1)
while (true) // await abort

HW_PRE_COMMIT
counter[id] = counter[id] + 1
```





 This improvement, eliminates HTM-HTM false conflicts due to writing to same counter

```
padded unsigned seqlock
     padded unsigned counter[]
     thread local unsigned id
3
     HW_POST_BEGIN
5
       if (seqlock & 1)
6
                                Now, each thread has its own
           while (true)
                             location to indicate its writes to STM
                               transactions, so no more false
     HW_PRE_COMMI
                             conflicts due to this communication
       counter[id] = counter[id]
10
```





 This improvement, eliminates HTM-HTM false conflicts due to writing to same counter

```
padded unsigned seqlock
    padded unsigned counter[]
    thread local unsigned id
3
    HW_POST_BEGIN
5
       if (seqlock & 1)
6
          while (true)
                            BUT, software tx_commit will have
                            more overhead checking all these
                                     counters
    HW_PRE_COMMI
       counter[id] = counter[id]
10
```



