Ziliang Yin

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EDUCATION

Shenzhen University

September 2022 - June 2025

Mphil, Integrated Circuit Engineering

Average Score: 81.7/100

Core Courses: Matrix Theory and Method, Random Process, Digital Signal Processing, Machine Learning, Digital Integrated Circuit Design, Integrated Circuit Back End Design, VLSI Design Introduction, Design of Analog IC

South China University of Technology

September 2017 - June 2021 Average Score: 84.4/100

BEng, Electrical Engineering and Automation

Core Courses: Circuit Principle, Analog and Digital Electronics, Automatic Control Theories, Power Electronics,

Electromagnetic Fields, Signals and Systems, Electrical Machinery, Electric Power Systems

RESEARCH INTERESTS

Biomedical signal processing;

Algorithm & hardware development

Brain-computer interfaces

Wearable devices

PUBLICATIONS

[J] Z. Yin, and W. Shi, "WPCT: A Lightweight EEG Physiological Artifact Denoising Architecture for Single-Channel BCI Applications", IEEE Transactions on Circuits and Systems I: Regular Papers, 2024, Under Review [C] Z. Yin, W. Shi and K. Liu, "An EEG Signal Processing System Design with Approximate Operations", 2023 IEEE International Conference on Integrated Circuits, Technologies and Applications (IEEE ICTA), Hefei, China, 2023, Published

RESEARCH EXPERIENCE

Algorithm and Hardware Development for Single-channel SSVEP-based BCI

August 2024 - Now

Natural Science Foundation of Guangdong Province, China, (2023A1515010761)

- · Carry out channel selection and stimuli design for an SSVEP-based BCI system (in progress).
- · Design a lightweight neural network, combined with digital signal processing methods, that efficiently extracts brain information (in progress).
- · Propose a high-performance hardware architecture that implements the feature extraction and classification network (in progress).

Algorithm and Hardware Development for the Removal of Physiological Artifacts from Single-Channel EEG October 2023 - August 2024

Natural Science Foundation of Guangdong Province, China, (2023A1515010761)

- · Developed a lightweight algorithm, WPCT, that removes EOG and EMG artifacts, and corrects baseline drift simultaneously from single-channel EEG, which is useful in real-time single-channel BCI signal preprocessing.
- · Proposed an architecture that implements the WPCT algorithm in *digital circuits*. Significantly reduced the hardware scale with a new *area-efficient rotation ordering* for two-sided Jacobi SVD calculation of tall matrices.
- Configured the proposed architecture in four ways: Haar-16, Haar-32, Db2-16, and Db2-32. Their artifact removal performance and hardware performance were analyzed and compared, enabling the selection of *optimal configuration* for specific applications.

Digital System Development for Emotion Recognition Based on Long Short-Term Memory (LSTM)
Network

December 2022 - September 2023

National Natural Science Foundation of China, (61974095)

- · Designed an *EEG signal processing* system with an application to *emotion recognition*, which includes three primary modules: preprocessing, feature extraction, and emotion classification.
- · Used the *energy ratio* of different frequency bands as input feature. Trained an *LSTM network* for dual-label classification of 16 emotions, with an average accuracy of 64.5% on the DEAP dataset.
- · Deployed the system using digital circuits. Minimized redundant logic. Adopted piecewise linear approximation for nonlinear operations to reduce complexity.

PROJECT EXPERIENCE

Research on Low-Power Pattern Recognition AI Edge Chip Design and Hardware Efficiency Optimization December 2022 - Now

Natural Science Foundation of Guangdong Province, China, (2023A1515010761)

· Main Work: Draft research proposal, feasibility report, technical guidelines; Algorithm & hardware co-design of a preprocessing module for single-channel EEG; UPF design for SVM & FFT modules.

Research on Core Technologies for High-Efficiency, Ultra-Low Power Brain-Computer Interface/Neural Signal Detection Chips November 2022 - December 2023

National Natural Science Foundation of China, (61974095)

· Main Work: Design replication; Design of an 1024-point radix-2 FFT; Draft research report; Development and hardware implementation of an LSTM network for emotional recognition using EEG.

TEACHING EXPERIENCE

• Teaching assistant for Introduction to Electronics Engineering	undergraduate course (Fall 2022)
• Teaching assistant for Digital Integrated Circuits	undergraduate course (Spring 2023)

AWARDS

• Academic Scholarship of Shenzhen University (Top 10%)	2022 - 2023
• Kang Dewei Innovation Scholarship (Top 8%)	2018 - 2019
• Outstanding Student Leader (Top 5%)	2019 - 2020
• Outstanding Intern in Power Grid (Top 10%)	2018 - 2019

LEADERSHIP EXPERIENCE

Shenzhen University Student Union	
Member, Practice Department	October 2022 - September 2023
South China University of Technology Student Union	
Secretary, Department of Manpower and Liaison	May 2018 - July 2019
Student Innovation and Entrepreneurship Club of SCUT	
Member, Outreach Practice Department	March 2018 - August 2018

SKILLS

Programming: Matlab, Python, C++, Verilog

Language: English, Chinese

REFERENCE

Associate Prof. Weiwei Shi, IEEE Member

Shenzhen University E-mail: wwshi@szu.edu.cn