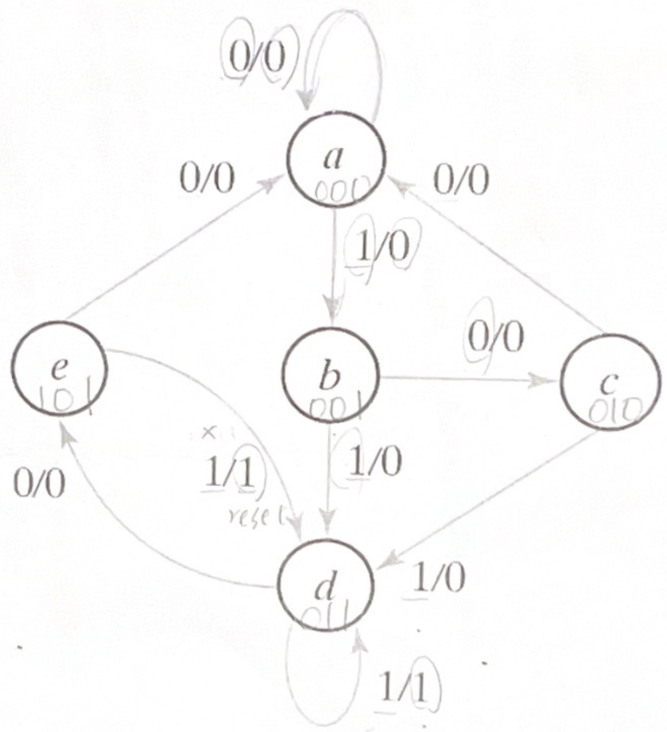
Implement the synchronous circuit with the following state diagram

- Verilog + UWV simulation (50%) or Verilog + testbench simulation (60%)
- FPGA (40%)

Simulation must have at least 10 state transitions



- You must output the state in both simulation and FPGA