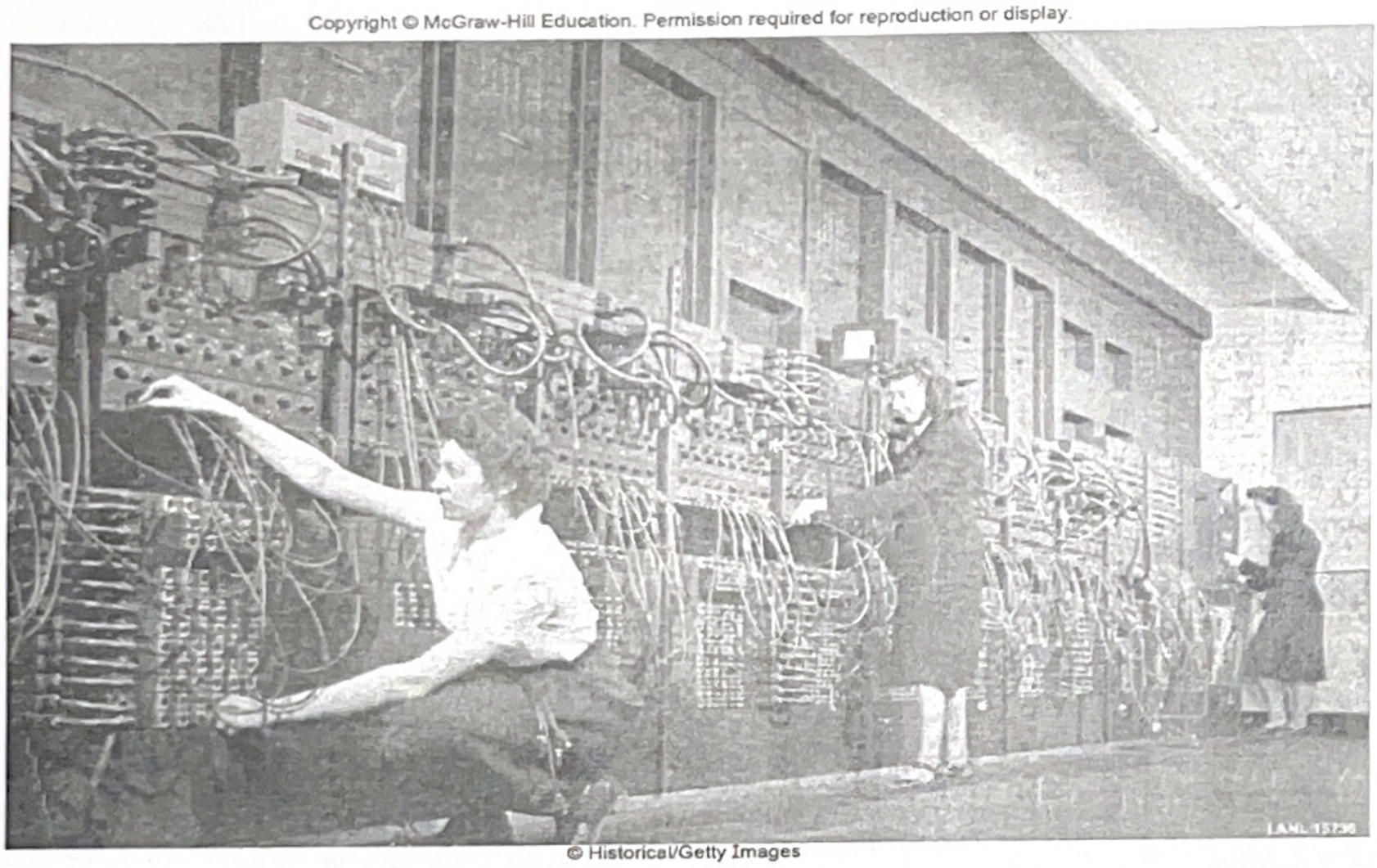
1. 10%

The following figure shows three operators plugging and unplugging cables and switches of ENIAC. What were they doing? patch



2. 10%

A computer today is so powerful to do ten millions multiplications in a second. But it is still an electronic idiot. Why?

3. 10%

A computer must be built on binary system. Is it true or false? Explain your answer.

4. 15+5+5%

The following questions will ask you to write the names of control lines in the following figure where the control lines are indicated with hollow triangles, such as GatePC and LD.MAR.

The instruction cycle of von Neumann model consists of six phases:

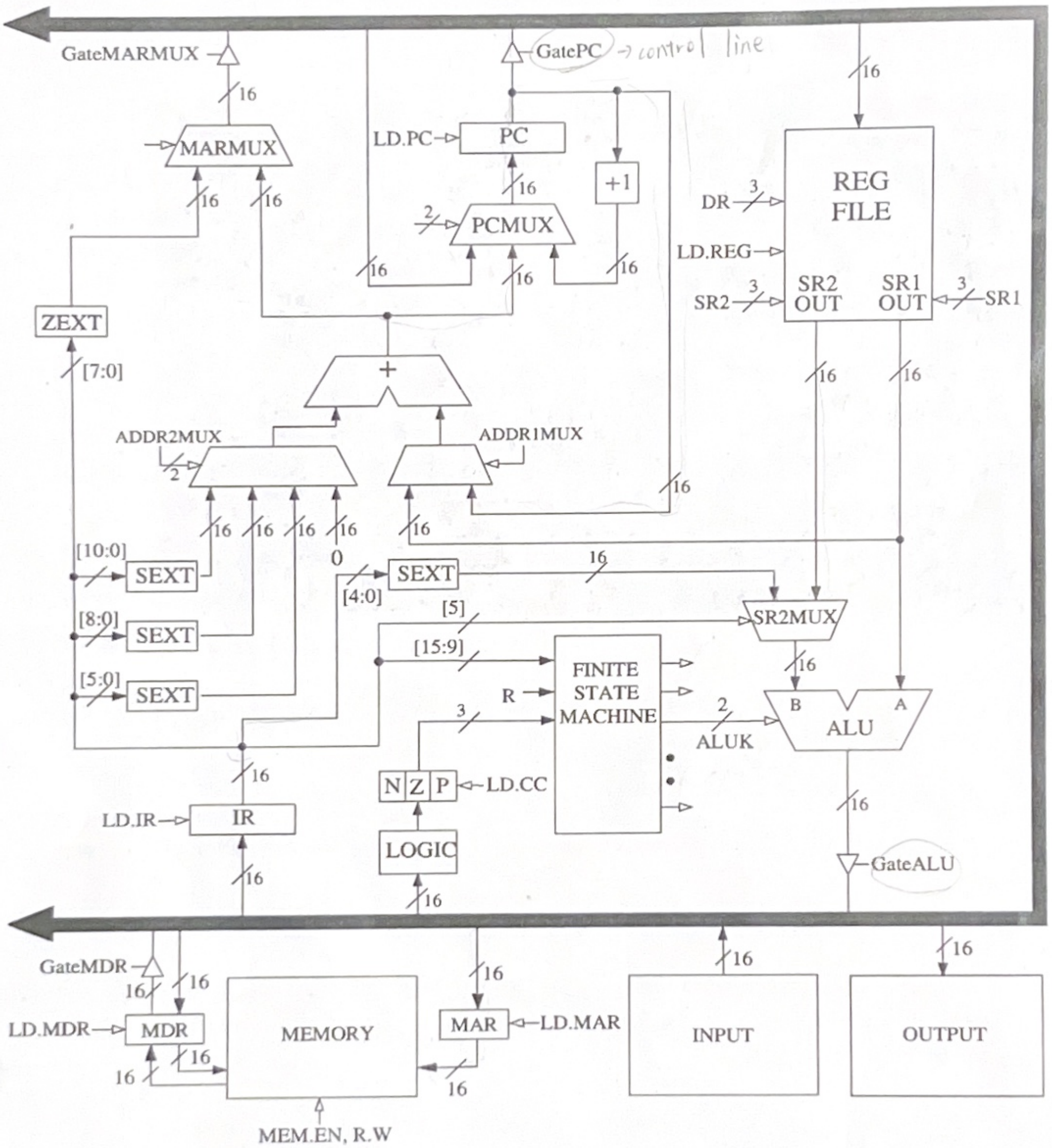
FETCH, DECODE, EVALUATE ADDRESS,
FETCH OPERANDS, EXECUTE, STORE RESULT.

(a) The FETCH is further comprised of three steps. Please show which control lines will be enabled in each step.

(b) The LD instruction is located at x4020. What will be the address of memory be loaded?

0 0 1 0 0 1 0 1 1 0 1 0 1 1 1 0 === LD R2 x1AE

(c) The previous LD instruction needs the third phase to evaluate the effective address. Please show the control lines used in this phase.



5. 5+5+5+5+5%

(a) Assume that there are about 700 students in your class. If every student is to be assigned a unique bit pattern, what is the minimum number of bits required to do this?

(b) Based on the previous question, how many more students can be admitted to the class without requiring additional bits for each student's unique bit pattern?

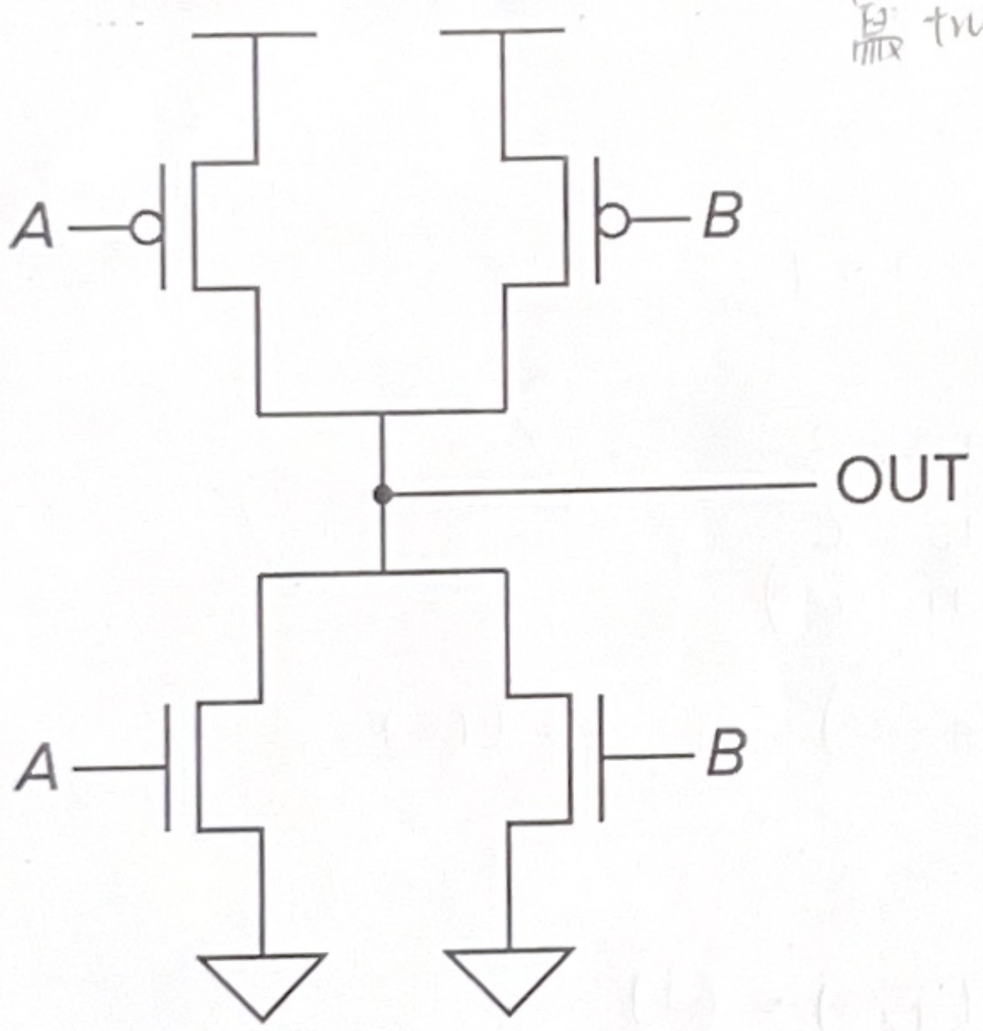
(c) Convert the decimal number -33 to eight-bit 2's complement binary number.

(d) Convert the decimal number 63 to eight-bit 2's complement binary number.

(e) Write the six-bit 2's complement representation of -31.

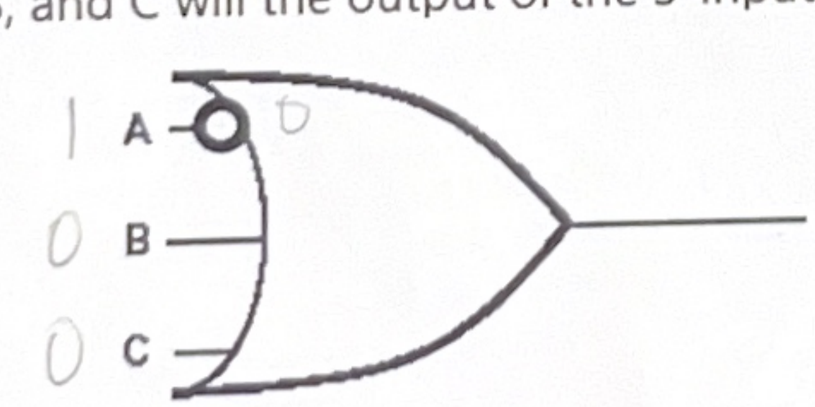
6. 10%

Complete a truth table for the transistor-level circuit in the following figure.



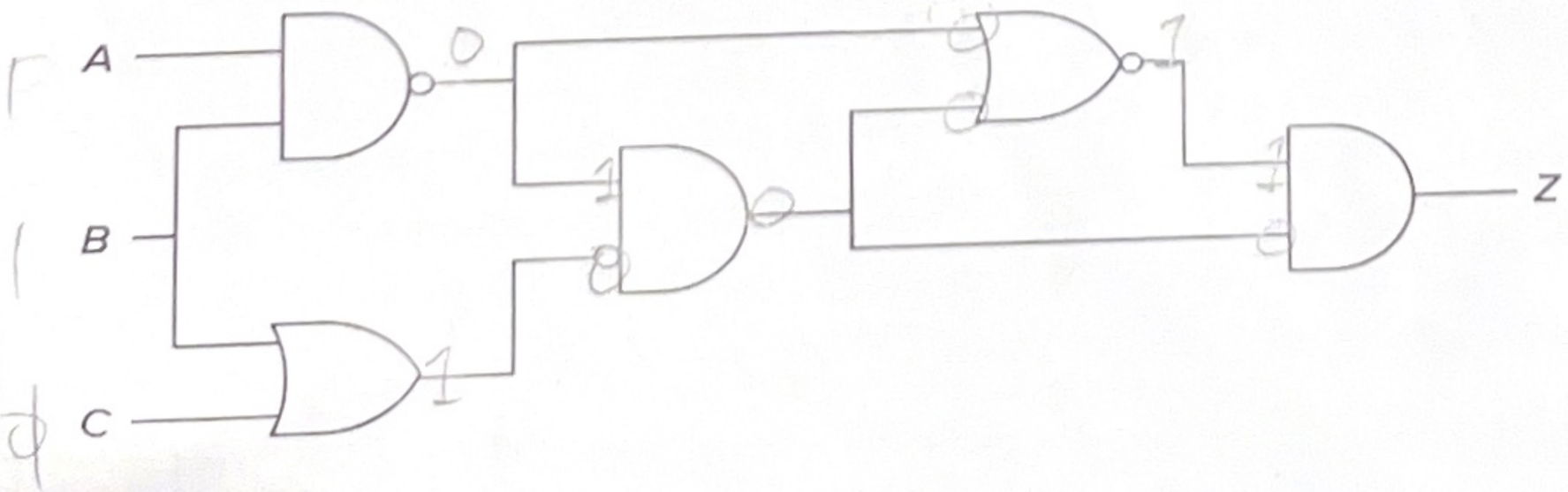
7. 5%

For what values of A, B, and C will the output of the 3-input OR gate be zero?



8. 16%

Construct the output truth table of the following circuit.



A	B	C	Output
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	