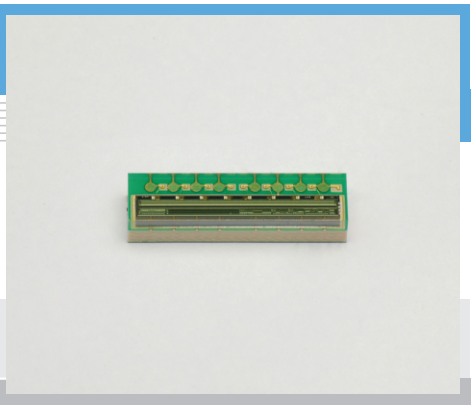
CMOS linear image sensor
S10226

Small plastic package CMOS image sensor



Features

- Compact and high cost-performance
  Surface mount package: 2.4 × 9.1 × 1.6 t mm
- Pixel pitch: 7.8 µm
  Pixel height: 125 µm
- Number of pixels: 1024 ch
- Single 3.3 V power supply operation available
- High sensitivity, low dark current, low noise
- On-chip charge amplifier with excellent input/output characteristics
- Built-in timing generator allows operation with only Start and Clock pulse inputs
- Video data rate: 200 kHz max.
- Spectral response range: 400 to 1000 nm

Note: Consult with the nearest sales office if an evaluation board is needed.

Applications

- Barcode readers
- Displacement meters
- Refractometers
- Interferometers
- Miniature spectrometers

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +6	V
Gain selection terminal voltage	Vg	-0.3 to +6	V
Clock pulse voltage	V(clk)	-0.3 to +6	V
Start pulse voltage	V(st)	-0.3 to +6	V
Operating temperature*1	Topr	-25 to +85	°C
Storage temperature*1	Tstg	-25 to +85	°C

*1: No condensation

■ Dimensions

Parameter	Value	Unit
Number of pixels	1024	-
Pixel pitch	7.8	µm
Pixel height	125	µm
Active area length	7.9872	mm

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■ Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	3.3	5	5.25	V
Gain selection terminal voltage	High gain	Vg	-	0	-	V
	Low gain		Vdd - 0.25	Vdd	Vdd + 0.25	V
Clock pulse voltage	High	V(clk)	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low		-	0	-	V
Start pulse voltage	High	V(st)	Vdd - 0.25	Vdd	Vdd + 0.25	V
	Low		-	0	-	V

■ Electrical characteristics [Ta=25 °C, Vdd=5 V, V(clk)=V(st)=5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(clk)	100	-	800	kHz
Video data rate	VR	-	f(clk)/4	-	kHz

■ Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(clk)=V(st)=5 V]

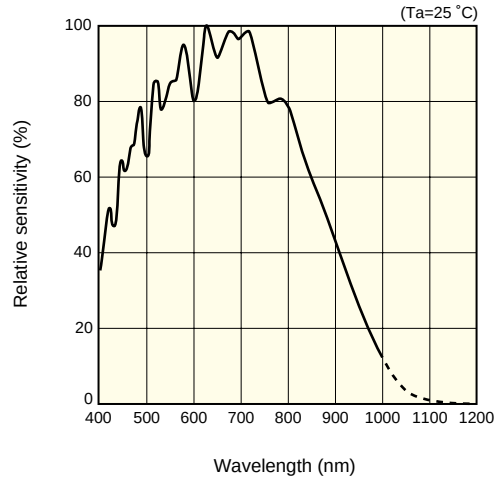
Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ		400 to 1000		nm
Peak sensitivity wavelength		λp	-	700	-	nm
Current consumption		IDD	-	5	-	mA
Dark output voltage*2	High gain	Vd	-	0.6	6	mV
	Low gain		-	0.3	3	
Saturation output voltage		Vsat	-	3.0	-	V
Readout noise	High gain	Nr	-	1.4	2.2	mV rms
	Low gain		-	0.7	1.1	
Offset output voltage		Vo		0.4	-	V
Photo response non-uniformity*3 *4		PRNU	-	-	±8.5	%

*2: Storage time Ts=10 ms

*3: Uniformity is defined under the condition that all pixels in the device are uniformly illuminated by light which is 50 % of the saturation exposure level and using 1022 pixels excluding both ends pixels as follows:
PRNU= ΔX/X × 100 (%)
X: Average output of 1022 pixels excluding the pixels at both ends
ΔX: Difference between X and maximum or minimum output

*4: Measured with a tungsten lamp of 2856 K

■ Spectral response (Typical example)



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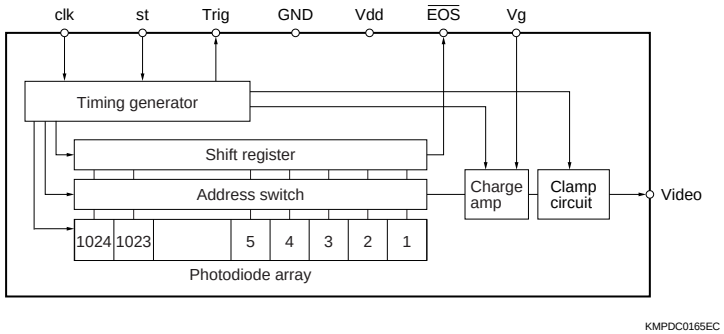
■ Block diagram



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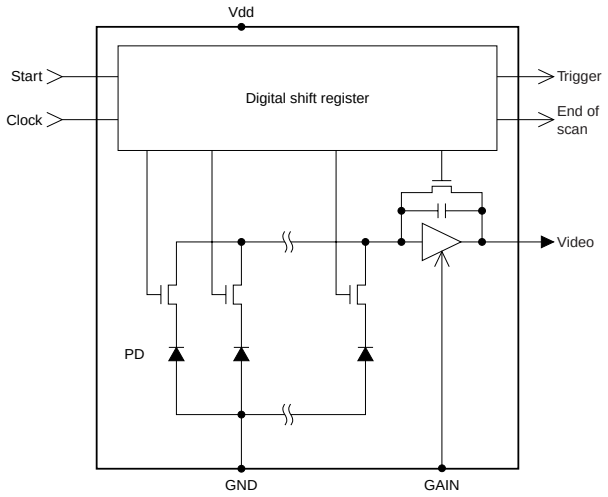
■ Configuration

S10226 consists of a photosensitive area made up of a 1024 pixel photodiode array, address switches for photodiode signal readout, a shift register for controlling the address switches, a charge amplifier for integrating charging current, a timing circuit for generating various timings, and a bias circuit. (See equivalent circuit below.)
Each address switch is comprised of an N-channel MOS transistor using the photodiode cathode as the source, the charge amplifier input end as the drain, and the address pulse input from the shift register as the gate.



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Signal readout method

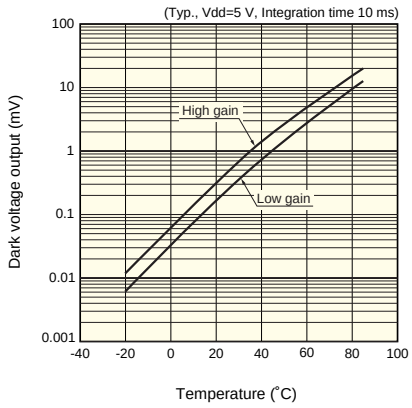
S10226 uses a charge integration method that temporarily accumulates a photoelectrically-converted charge in the junction capacitance of each pixel. While the output in real-time readout is proportional only to the light intensity, the output in charge integration is proportional to the product (amount of exposure) of the light intensity and integration time. So the output from charge integration can be increased by lengthening the integration time, which makes charge integration ideal for low-light-level detection.

Readout by charge integration

In charge integration, a photoelectrically-converted charge is temporarily accumulated in the junction capacitance of each pixel. The integration capacitance of the charge amplifier is discharged by a reset signal from the timing generator circuit immediately before each address switch is turned on. The charge stored in the junction capacitance of each pixel is then input to the charge amplifier by sequentially turning on the address switch connected to each pixel. At this point, each pixel is initialized.
The output voltage*5 of the charge amplifier is then output as a positive-going integrated waveform from the Video terminal through the CDS circuit and the next-stage buffer amplifier circuit. Finally, an EOS (End-Of-Scan) signal is output after the last pixel signal was output.

*5: This is proportional to the amount of exposure. Output response depends on DTC (Discharge Time Constant).

■ Dark voltage output vs. temperature



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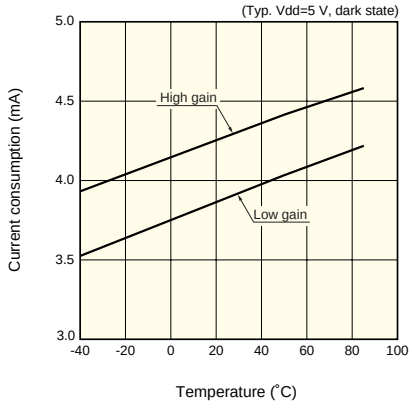
■ Current consumption vs. temperature



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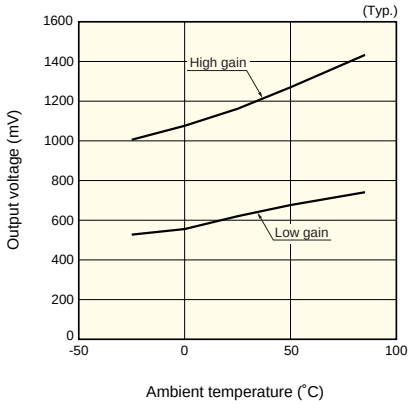
■ Output voltage vs. ambient temperature



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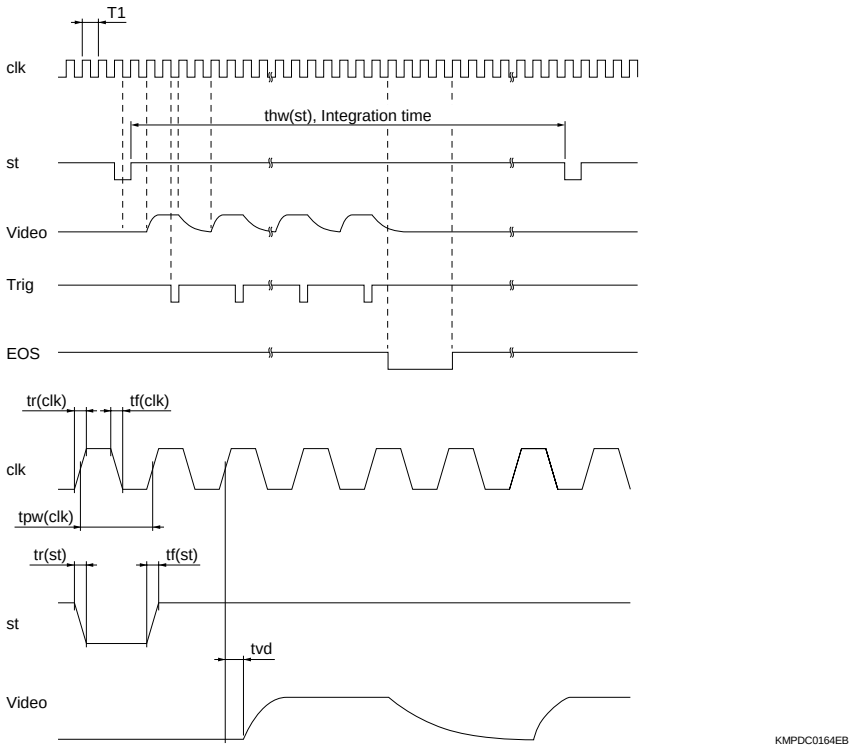
■ Timing chart



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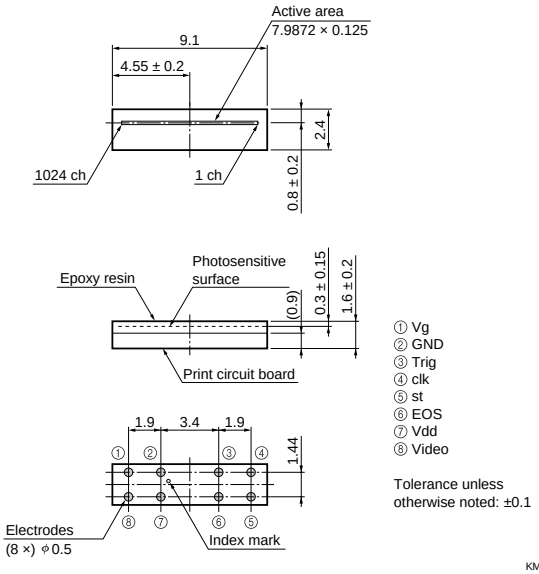
Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse high time	thw(st)	T1 × 4102	-	-	µs
Start pulse rise and fall time	tr(st), tf(st)	0	20	30	ns
Clock pulse width	tpw(clk), T1	1.25	-	10	µs
Clock pulse rise and fall time	tr(clk), tf(clk)	0	20	30	ns
Video delay time	tvd	-	20	-	ns

Note: The clk pulse should be set from high to low just once when the st pulse is low. The internal shift register starts operating at this timing.
The storage time is determined by the start pulse intervals. However, since the charge storage of each pixel is carried out between the signal readout of that pixel and the next signal readout of the same pixel, the start time of charge storage differs depending on each pixel. In addition, the next start pulse cannot be input until signal readout from all pixels is completed.

■ Dimensional outline (unit: mm)



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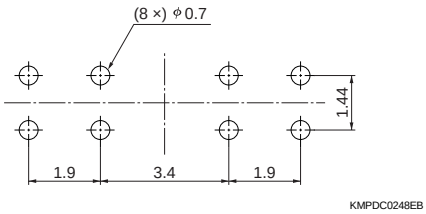
■ Pin connection

Pin No.	Name	Description	Input/output
①	Vg	Gain selection: Low gain → Vdd or open, High gain → GND	Input
②	GND	Ground	Input
③	Trig	Trigger: Timing signal output for A/D converter	Output
④	clk	Clock pulse (Pulse for synchronizing the internally generated pulses that control sensor operation frequency)	Input
⑤	st	Start pulse (Pulse for initializing the internally generated pulses that set the timing to start reading pixel signals)	Input
⑥	EOS	End of scan (Shift register end-of-scan signal pulse generated after reading signals from all pixels)	Output
⑦	Vdd	Power supply voltage	Input
⑧	Video	Video signal output	Output

■ Recommended land pattern



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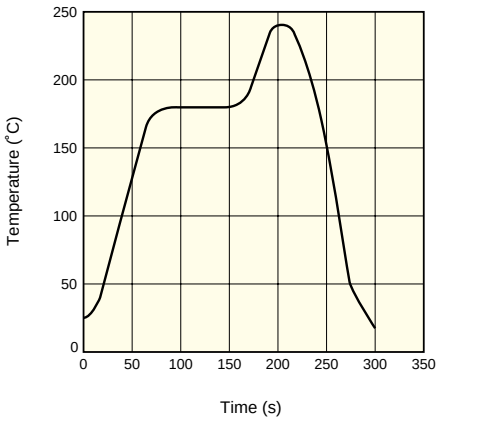
■ Temperature profile of reflow soldering



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■ Precautions for use

(1) Electrostatic countermeasures

· This device has a built-in protection circuit as a safeguard against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges.

· Protect this device from surge voltages which might be caused by peripheral equipment.

(2) Package handling

· The package surface is easily scratched, so handle this device carefully.

· Dust or grime on the light input window might cause non-uniform sensitivity. To remove dust or grime, blow it off with compressed air.

(3) Reflow soldering

· To prevent damaging this device during reflow soldering, perform soldering within 24 hours after opening the moisture-proof packing.

· The extent of damage that might occur during reflow soldering depends on the PC board size and reflow oven conditions. Check the device for any damage before reflow soldering.

(4) Surface protective tape

· Protective tape is affixed to the surface of this product to protect the active area. After assembling the product, remove the tape before use.

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Cat. No. KMPD1097E09
Jun. 2010 DN