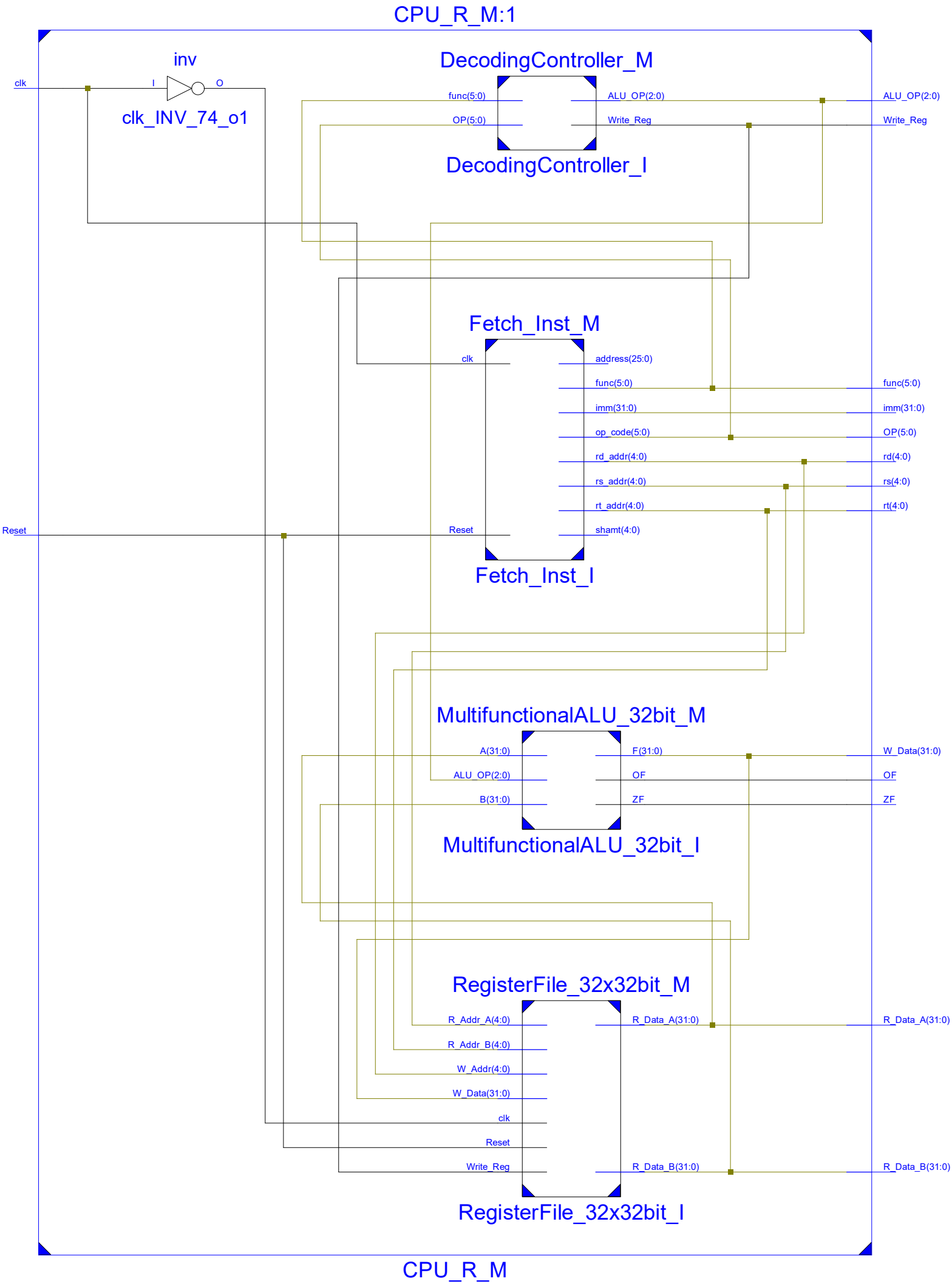
CPU_R_M:1
inv
clk
I
O
clk_INV_74_o1
DecodingController_M
func(5:0)
OP(5:0)
ALU_OP(2:0)
Write_Reg
DecodingController_I
ALU_OP(2:0)
Write_Reg
Fetch_Inst_M
clk
Reset
address(25:0)
func(5:0)
imm(31:0)
op_code(5:0)
rd_addr(4:0)
rs_addr(4:0)
rt_addr(4:0)
shamt(4:0)
Fetch_Inst_I
func(5:0)
imm(31:0)
OP(5:0)
rd(4:0)
rs(4:0)
rt(4:0)
MultifunctionalALU_32bit_M
A(31:0)
ALU_OP(2:0)
B(31:0)
F(31:0)
OF
ZF
MultifunctionalALU_32bit_I
W_Data(31:0)
OF
ZF
RegisterFile_32x32bit_M
R_Addr_A(4:0)
R_Addr_B(4:0)
W_Addr(4:0)
W_Data(31:0)
clk
Reset
Write_Reg
R_Data_A(31:0)
R_Data_B(31:0)
RegisterFile_32x32bit_I
R_Data_A(31:0)
R_Data_B(31:0)
CPU_R_M