This directory should only contain the top level VHDL files!
All other elements/components of the design should be buried in hierarchical levels and therefore stored in libraries created in the */Libraries* directory.

The top level VHDL files are:

- .vhd
  This is the top level of the whole design, the files should only contain instantiated components from libraries of the */Libraries* directory and IO buffers.
- _Tester.vhd_
  This is the VHDL description used to activate inputs and outputs of the .vhd file.
  It is thus a VHDL description of the external world to the .vhd file.
  Multiple of these tester files can be available in order to be able to test different aspects of the top level design. Read the ReadMe file in teh */SimScripts* directory.
- _Testbench.vhd
  This file combines the .vhd and one or more _Tester.vhd files in order to be able to simulate the whole. Please read the ReadMe file in teh */SimScripts* directory.