

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
1A	VREFB1AN0	Ю			DIFFIO_TX_L1n	DIFFOUT_L1n	H23		DETECTION DETECTION		GND
1A		Ю			DIFFIO_RX_L2n	DIFFOUT_L2n	F25	DQ1L			DNU
1A	VREFB1AN0	10			DIFFIO_TX_L1p	DIFFOUT_L1p	H22	DQ1L			GND
1A	VREFB1AN0	10			DIFFIO_RX_L2p	DIFFOUT_L2p	G25	DQ1L			DNU
1A	VREFB1AN0	10			DIFFIO_RX_L3n	DIFFOUT_L3n	G24	DQSn1L			GND
1A	VICEIDIANO	10			DIFFIO_TX_L4n	DIFFOUT_L4n	E22	DQ1L			GND
IA		10			DIFFIO_RX_L3p	DIFFOUT_L3p	H24	DQS1L			GND
IA		10			DIFFIO_TX_L4p	DIFFOUT_L4p	F22				GND
IA IA		10			DIFFIO_TX_L5n	DIFFOUT_L5n	F23	DQ1L	+		GND
IA IA	VREFB1AN0 VREFB1AN0	10			DIFFIO_RX_L6n DIFFIO_TX_L5p	DIFFOUT_L6n DIFFOUT_L5p	J25 G22	DQ1L DQ1L			DNU GND
IA	VREFBIANO VREFBIANO	10			DIFFIO_TX_L5p DIFFIO_RX_L6p	DIFFOUT_L6p	J24	DQ1L DQ1L	+		GND
Α	VREFB1AN0	10			DIFFIO_RX_L6p	DIFFOUT_L7n	K25	DQTL			DNU
IA		IO			DIFFIO TX L8n	DIFFOUT L8n	J23	DQ1L			GND
A	VREFB1AN0	10			DIFFIO_RX_L7p	DIFFOUT_L7p	L25	DQIL			GND
IA.	VREFB1AN0	10			DIFFIO TX L8p	DIFFOUT L8p	K23	DQ1L			VCC
PA .	VREFB2AN0	IO .			DIFFIO TX L9n	DIFFOUT L9n	L22	Daile			GND
2A	VREFB2AN0	10			DIFFIO_RX_L10n	DIFFOUT L10n	M25	DQ1L			DNU
2A	VREFB2AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L9p	M22	DQ1L	1		GND
A	VREFB2AN0	10			DIFFIO_RX_L10p	DIFFOUT_L10p	M24	DQ1L			GND
2A		10			DIFFIO_RX_L11n	DIFFOUT_L11n	N24	DQSn1L			GND
2A		IO			DIFFIO_TX_L12n	DIFFOUT_L12n	N23	DQ1L			VCC
'A		IO			DIFFIO_RX_L11p	DIFFOUT_L11p	P24	DQS1L			VCC
'A	VREFB2AN0	Ю			DIFFIO_TX_L12p	DIFFOUT_L12p	N22				GND
2A	VREFB2AN0	Ю			DIFFIO_TX_L13n	DIFFOUT_L13n	P23	DQ1L			GND
2A	VREFB2AN0	Ю			DIFFIO_RX_L14n	DIFFOUT_L14n	P25	DQ1L			GND
A	VREFB2AN0	Ю			DIFFIO_TX_L13p	DIFFOUT_L13p	R22	DQ1L			GND
Α	VREFB2AN0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	R25	DQ1L			DNU
A	VREFB2AN0	IO			DIFFIO_RX_L15n	DIFFOUT_L15n	T25				DNU
2A	VREFB2AN0	IO			DIFFIO_TX_L16n	DIFFOUT_L16n	T23	DQ1L			VCC
2A	VREFB2AN0	IO			DIFFIO_RX_L15p	DIFFOUT_L15p	T24				GND
2A	VREFB2AN0	10			DIFFIO_TX_L16p	DIFFOUT_L16p	T22	DQ1L			GND
2A	VICEI DEFINO	10			DIFFIO_TX_L17n	DIFFOUT_L17n	U22				GND
2A	VICEI DEFINO	10			DIFFIO_RX_L18n	DIFFOUT_L18n	U25	DQ2L			GND
2A		10			DIFFIO_TX_L17p	DIFFOUT_L17p	V22	DQ2L			GND
2A		10			DIFFIO_RX_L18p	DIFFOUT_L18p	V24	DQ2L			GND
2A	VREFB2AN0	10			DIFFIO_RX_L19n	DIFFOUT_L19n	W25	DQSn2L			DNU
2A	VREFB2AN0	10			DIFFIO_TX_L20n	DIFFOUT_L20n	V23	DQ2L			GND
2A	VREFB2AN0	10			DIFFIO_RX_L19p	DIFFOUT_L19p	Y25	DQS2L			GND
A	VREFB2AN0	10			DIFFIO_TX_L20p	DIFFOUT_L20p	W23				VCC
2A	VREFB2AN0	10			DIFFIO_TX_L21n	DIFFOUT_L21n	Y23	DQ2L			GND
2A	VREFB2AN0	10			DIFFIO_RX_L22n	DIFFOUT_L22n	AA25	DQ2L			DNU
'A	VREFB2AN0 VREFB2AN0	10			DIFFIO_TX_L21p	DIFFOUT_L21p	Y22 Y24	DQ2L			GND VCC
A A	VREFB2AN0 VREFB2AN0	10			DIFFIO_RX_L22p	DIFFOUT_L22p DIFFOUT_L23n	AB25	DQ2L	+		DNU
A		IO			DIFFIO_RX_L23n DIFFIO_TX_L24n	DIFFOUT_L24n	AA22	DON			GND
A A		IO			DIFFIO_TX_L24n DIFFIO_RX_L23p	DIFFOUT_L23p	AA24	DQ2L			GND
A A		IO			DIFFIO_RX_L23p	DIFFOUT_L24p	AB22	DQ2L	+	+	GND
Α.		TDO		TDO	5110_1/_L24p	5 501_LE-TP	AD25	JULL	+	+	0.10
Α		nCSO		DATA4	-		AD23	+	1		
A		TMS		TMS	1		AE25	1			
A		AS DATA3		DATA3	1		AE24	1	1		
A	1	TCK		TCK	1		AC22	1	1		
A	i i	AS_DATA2		DATA2	İ		AB21	1	İ		
A		TDI		TDI			AD23				
A		AS_DATA1		DATA1			AE21				
A		DCLK		DCLK			AE22				
A		AS_DATA0,ASDO		DATA0			AE23				
A	VREFB3AN0	Ю		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AE18	DQ1B			
A	VREFB3AN0	Ю		DATA5	DIFFIO TX B2n	DIFFOUT_B2n	AE20				
A		Ю		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD19	DQ1B			
A	VREFB3AN0	Ю		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AD21	DQ1B			
A		Ю		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AD18	DQSn1B			
A		Ю		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB20	DQ1B			
A	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AC17	DQS1B			
A	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AB19				
A	VREFB3AN0	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AE17	DQ1B			
	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AC19	DQ1B	1	1	1



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AD16	DQ1B			
3A	VREFB3AN0	Ю		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC18	DQ1B			
3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AE16				
3A	VREFB3AN0 VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AB17 AE15	DQ1B			
3A 3A	VREFB3AN0 VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p DIFFIO_TX_B8p	DIFFOUT_B7p DIFFOUT_B8p	AE15 AA17	DQ1B			
3A 3B	VREFB3BN0	10			DIFFIO_TX_B8p DIFFIO_RX_B10n	DIFFOUT_B8p DIFFOUT_B10n	AA17 AA16	DQ1B			
3B	VREFB3BN0	10			DIFFIO_RX_B10II	DIFFOUT_B10II	AC16				
3B	VREFB3BN0	10			DIFFIO_RX_B14n	DIFFOUT B14n	AB15				
3B	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	AD15				
3B	VREFB3BN0	10	CLK0p,FPLL BL FBp		DIFFIO RX B15p	DIFFOUT B15p	AD14				
3B	VREFB3BN0	IO			DIFFIO TX B17n	DIFFOUT_B17n	AB14				
3B	VREFB3BN0	Ю			DIFFIO_RX_B18n	DIFFOUT_B18n	AE13	DQ2B			
3B	VREFB3BN0	Ю			DIFFIO_TX_B17p	DIFFOUT_B17p	AA14	DQ2B			
3B	VREFB3BN0	Ю			DIFFIO_RX_B18p	DIFFOUT_B18p	AE12	DQ2B			
3B	VREFB3BN0	Ю			DIFFIO_RX_B19n	DIFFOUT_B19n	AE11	DQSn2B			
3B	VREFB3BN0	10			DIFFIO_TX_B20n	DIFFOUT_B20n	AD13	DQ2B			
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	AE10	DQS2B			
3B	VREFB3BN0	10	EDIT DI OLIVOLETA EDIT DI CONTO		DIFFIO_TX_B20p	DIFFOUT_B20p	AC14	2002			
3B	VREFB3BN0	0	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB12	DQ2B			
3B	VREFB3BN0 VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_RX_B22n DIFFIO_TX_B21p	DIFFOUT_B22n	AD11 AA12	DQ2B DQ2B	-	-	
3B 3B	VREFB3BN0 VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB		DIFFIO_TX_B21p DIFFIO_RX_B22p	DIFFOUT_B21p	AC12	DQ2B DQ2B			
3B	VREFB3BN0 VREFB3BN0	0	CLK1n	+	DIFFIO_RX_B22p DIFFIO_RX_B23n	DIFFOUT_B22p DIFFOUT_B23n	AC12 AD10	DQZB	+	+	+
3B	VREFB3BN0	10	CERTII		DIFFIO_RX_B23II	DIFFOUT_B24n	AB11	DQ2B			
3B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	AD9	DQZB			
3B	VREFB3BN0	10	CERT		DIFFIO TX B24p	DIFFOUT B24p	AA11	DQ2B			
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AB10	5425			
4A	VREFB4AN0	10			DIFFIO RX B26n	DIFFOUT B26n	AE8	DQ3B			
4A	VREFB4AN0	IO .			DIFFIO TX B25p	DIFFOUT B25p	AA9	DQ3B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B26p	DIFFOUT_B26p	AD8	DQ3B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B27n	DIFFOUT_B27n	AC9	DQSn3B			
4A	VREFB4AN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	AB9	DQ3B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B27p	DIFFOUT_B27p	AC8	DQS3B			
4A	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	AA8				
4A	VREFB4AN0	Ю			DIFFIO_TX_B29n	DIFFOUT_B29n	AC7	DQ3B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B30n	DIFFOUT_B30n	AE6	DQ3B			
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AC6	DQ3B			
4A	VREFB4AN0	IO .			DIFFIO_RX_B30p	DIFFOUT_B30p	AD6	DQ3B			
4A 4A	VREFB4AN0 VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n DIFFIO_TX_B32n	DIFFOUT_B31n DIFFOUT_B32n	AE5 AC4	DQ3B			
4A 4A	VREFB4AN0 VREFB4AN0	10	011/0-		DIFFIO_IX_B32n DIFFIO_RX_B31p	DIFFOUT_B32n DIFFOUT_B31p	AD5	DQ3B		+	
4A 4A	VREFB4AN0 VREFB4AN0	0	CLK2p		DIFFIO_RX_B31p DIFFIO_TX_B32p	DIFFOUT_B31p DIFFOUT_B32p	AD5 AB5	DQ3B			
4A 4A	VREFB4AN0	10			DIFFIO_TX_B33n	DIFFOUT_B33n	AC3	DQ3B			
4A	VREFB4AN0	10			DIFFIO RX B34n	DIFFOUT B34n	AE3	DQ4B			
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	AB4	DQ4B			
4A	VREFB4AN0	10			DIFFIO_RX_B34p	DIFFOUT B34p	AE2	DQ4B	1	1	1
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AD4	DQSn4B			1
4A	VREFB4AN0	Ю			DIFFIO_TX_B36n	DIFFOUT_B36n	AA4	DQ4B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B35p	DIFFOUT_B35p	AD3	DQS4B			
4A	VREFB4AN0	Ю			DIFFIO_TX_B36p	DIFFOUT_B36p	AA3				
4A	VREFB4AN0	Ю			DIFFIO_TX_B37n	DIFFOUT_B37n	W3	DQ4B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B38n	DIFFOUT_B38n	AE1	DQ4B			
4A	VREFB4AN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	V4	DQ4B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B38p	DIFFOUT_B38p	AD1	DQ4B			
4A	VREFB4AN0	10	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	AC2			1	
4A	VREFB4AN0	10	0.15		DIFFIO_TX_B40n	DIFFOUT_B40n	Y3	DQ4B	+		1
4A	VREFB4AN0	10	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	AC1	2012	-	-	
4A	VREFB4AN0	10		+	DIFFIO_TX_B40p	DIFFOUT_B40p	W4	DQ4B	+	+	
4A 4A	VREFB4AN0	10			DIFFIO_RX_B43n	DIFFOUT_B43n	AB2 AB1	+	-	1	_
4A 4A	VREFB4AN0 VREFB4AN0	10		+	DIFFIO_RX_B43p	DIFFOUT_B43p DIFFOUT_B46n	AB1 AA2	+		+	_
4A 4A	VREFB4AN0 VREFB4AN0	10	 		DIFFIO_RX_B46n DIFFIO_RX_B46p	DIFFOUT_B46n DIFFOUT_B46p	Y2	-	+	1	-
4A 4A	VREFB4AN0 VREFB4AN0	10	 	+	DIFFIO_RX_B46p DIFFIO_RX_B47n	DIFFOUT_B46p DIFFOUT_B47n	Y2 Y1	+	+	+	
4A 4A	VREFB4AN0 VREFB4AN0	10	 	+	DIFFIO_RX_B47n DIFFIO_RX_B47p	DIFFOUT_B47n DIFFOUT_B47p	W1	+	+	+	
1 Λ	VREFB5AN0	0	RZQ_1	+	DIFFIO_RX_B47p DIFFIO_TX_R1p	DIFFOUT_B47p DIFFOUT_R1p	U2	1	+		
Url		10	11424_1	INIT DONE	DIFFIO_TX_RTP	DIFFOUT R2p	V2	+		+	-
5A	VREFB5AN0										



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pir Migration Only
A	VREFB5AN0	Ю		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V1				
4	VREFB5AN0	Ю		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T4				
Α	VREFB5AN0	10			DIFFIO_RX_R4p	DIFFOUT_R4p	R2				
4	VREFB5AN0	10		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R3				
Α	VREFB5AN0 VREFB5AN0	10		DEV_OE	DIFFIO_RX_R4n DIFFIO_TX_R5p	DIFFOUT_R4n DIFFOUT_R5p	T2 P3				
A A	VREFB5AN0 VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p DIFFIO_RX_R6p	DIFFOUT_R6p	P3				
A	VREFB5AN0	10		DEV_CLRn	DIFFIO_RX_R6p	DIFFOUT_R5n	N2				
Α	VREFB5AN0	10		DE V_CENTI	DIFFIO_RX_R6n	DIFFOUT_R6n	R1				
Α	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	N4				
Α .	VREFB5AN0	10			DIFFIO RX R8p	DIFFOUT R8p	M1				
١	VREFB5AN0	Ю			DIFFIO_TX_R7n	DIFFOUT_R7n	N3				
4	VREFB5AN0	Ю			DIFFIO_RX_R8n	DIFFOUT_R8n	N1				
3	VREFB5BN0	Ю	CLK6p		DIFFIO_RX_R9p	DIFFOUT_R9p	L2				
3	VREFB5BN0	Ю	CLK6n		DIFFIO_RX_R9n	DIFFOUT_R9n	M2				
3	VREFB5BN0	Ю			DIFFIO_RX_R11p	DIFFOUT_R11p	K2				
3	VREFB5BN0	Ю	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	M4				
3	VREFB5BN0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	K1				
3	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	L3				
3	VREFB5BN0	0			DIFFIO_RX_R13p	DIFFOUT_R13p	H1			-	
3	VREFB5BN0 VREFB5BN0	10			DIFFIO_TX_R14p DIFFIO_RX_R13n	DIFFOUT_R14p	J4 .11	1	+	+	
3	VREFB5BN0 VREFB5BN0	10			DIFFIO_RX_R13n DIFFIO_TX_R14n	DIFFOUT_R13n DIFFOUT_R14n	J1 J3				
3	VREFB5BN0 VREFB5BN0	0			DIFFIO_IX_R14n DIFFIO_RX_R15p	DIFFOUT_R14n DIFFOUT_R15p	H2	+	+	1	1
3	VREFB5BN0	10			DIFFIO_RX_R16p	DIFFOUT_R16p	H4				
3	VREFB5BN0	10			DIFFIO_RX_R15n	DIFFOUT_R15n	G1				
3	VREFB5BN0	10			DIFFIO TX R16n	DIFFOUT_R16n	H3				
<u> </u>	VIXEI BOBITO	GND			Dir Fio_FX_ICION	Bii 1 GG 1_ttiGii	F3				
·	VREFB7AN0	10			DIFFIO RX T1p	DIFFOUT T1p	E1		GND	GND	
	VREFB7AN0	10			DIFFIO RX T1n	DIFFOUT T1n	D1		GND	GND	
١	VREFB7AN0	IO .			DIFFIO_RX_T3p	DIFFOUT_T3p	F2				
1	VREFB7AN0	Ю			DIFFIO_RX_T3n	DIFFOUT_T3n	E2				
Ą	VREFB7AN0	Ю			DIFFIO_TX_T6p	DIFFOUT_T6p	F4		T_RESET#	T_RESET#	
4	VREFB7AN0	Ю			DIFFIO_RX_T7p	DIFFOUT_T7p	E3				
1	VREFB7AN0	Ю			DIFFIO_RX_T7n	DIFFOUT_T7n	D3				
١	VREFB7AN0	10	CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	C1				
4		Ю			DIFFIO_TX_T10p	DIFFOUT_T10p	C7	DQ1T	T_DM_1	T_DM_1	
4		Ю	CLK11n		DIFFIO_RX_T9n	DIFFOUT_T9n	B1				
١	VREFB7AN0	10			DIFFIO_TX_T10n	DIFFOUT_T10n	C6	DQ1T	T_DQ_15	T_DQ_15	
1	VREFB7AN0	Ю			DIFFIO_RX_T11p	DIFFOUT_T11p	C3	DQ1T	T_DQ_13	T_DQ_13	
١	VREFB7AN0	Ю			DIFFIO_TX_T12p	DIFFOUT_T12p	D4	DQ1T	T_DQ_14	T_DQ_14	
١	VREFB7AN0	10			DIFFIO_RX_T11n	DIFFOUT_T11n	C2	DQ1T	T_DQ_12	T_DQ_12	
١	VREFB7AN0	10			DIFFIO_TX_T12n	DIFFOUT_T12n	C4	DQ1T	T_CKE_0	T_CKE_0	
١	VREFB7AN0	10			DIFFIO_RX_T13p	DIFFOUT_T13p	B2	DQS1T	T_DQS_1	T_DQS_1	
١	VREFB7AN0	10			DIFFIO_TX_T14p	DIFFOUT_T14p	D8	DOC 17	T_CKE_1	T_CKE_1	
	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T13n DIFFIO_TX_T14n	DIFFOUT_T13n DIFFOUT_T14n	A2 C8	DQSn1T DQ1T	T_DQS#_1 T_DQ_11	T_DQS#_1 T_DQ_11	
	VREFB7AN0	10					A4	DQ1T			
4	VREFB7AN0 VREFB7AN0	0			DIFFIO_RX_T15p DIFFIO_TX_T16p	DIFFOUT_T15p DIFFOUT_T16p	B5	DQ1T DQ1T	T_DQ_9 T_DQ_10	T_DQ_9 T_DQ_10	1
4	VREFB7AN0	0			DIFFIO_TX_T16p	DIFFOUT_T15n	A3	DQ1T	T_DQ_10	T_DQ_10	
\	VREFB7AN0	10			DIFFIO_RX_T16n	DIFFOUT T16n	B4	שעוו	GND	GND	
\	VREFB7AN0	10	CLK10p		DIFFIO_TX_T16II	DIFFOUT_T17p	B6	+	OIAD	0140	
`	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	E8	DQ2T	T_DM_0	T DM 0	1
	VREFB7AN0	10	CLK10n		DIFFIO_RX_T17n	DIFFOUT_T17n	A5		50		
١	VREFB7AN0	IO			DIFFIO TX T18n	DIFFOUT_T18n	D9	DQ2T	T DQ 7	T DQ 7	İ
	VREFB7AN0	IO			DIFFIO RX T19p	DIFFOUT T19p	B7	DQ2T	T DQ 5	T_DQ_5	
	VREFB7AN0	IO IO			DIFFIO_TX_T20p	DIFFOUT_T20p	E10	DQ2T	T_DQ_6	T_DQ_6	
	VREFB7AN0	Ю			DIFFIO_RX_T19n	DIFFOUT_T19n	A7	DQ2T	T_DQ_4	T_DQ_4	
l.	VREFB7AN0	Ю			DIFFIO_TX_T20n	DIFFOUT_T20n	D10	DQ2T	T_ODT_1	T_ODT_1	
ı	VREFB7AN0	Ю			DIFFIO_RX_T21p	DIFFOUT_T21p	A9	DQS2T	T_DQS_0	T_DQS_0	
1	VREFB7AN0	Ю			DIFFIO_TX_T22p	DIFFOUT_T22p	E11		T_ODT_0	T_ODT_0	
ı	VREFB7AN0	Ю			DIFFIO_RX_T21n	DIFFOUT_T21n	A8	DQSn2T	T_DQS#_0	T_DQS#_0	
ı	VREFB7AN0	Ю			DIFFIO_TX_T22n	DIFFOUT_T22n	D11	DQ2T	T_DQ_3	T_DQ_3	
١	VREFB7AN0	Ю			DIFFIO_RX_T23p	DIFFOUT_T23p	B9	DQ2T	T_DQ_1	T_DQ_1	
١		Ю			DIFFIO_TX_T24p	DIFFOUT_T24p	C11	DQ2T	T_DQ_2	T_DQ_2	
4	VREFB7AN0	10			DIFFIO_RX_T23n	DIFFOUT_T23n	A10	DQ2T	T_DQ_0	T_DQ_0	
4	VREFB7AN0	10	RZQ_2		DIFFIO_TX_T24n	DIFFOUT_T24n	B10				
	VREFB8AN0	10	CLK9p		DIFFIO RX T25p	DIFFOUT_T25p	B12	1	(1 1)	1	



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pir Migration Only
8A	VREFB8AN0	10			DIFFIO_TX_T26p	DIFFOUT_T26p	E13	DQ3T	T_A_0	T_CA_0	
ВА		Ю	CLK9n		DIFFIO_RX_T25n	DIFFOUT_T25n	A12				
BA		10			DIFFIO_TX_T26n	DIFFOUT_T26n	D14	DQ3T	T_A_1	T_CA_1	
8A	VREFB8AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	A14	DQ3T	T_A_4	T_CA_4	
		10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	E15	DQ3T	T_A_2	T_CA_2	
		10			DIFFIO_RX_T27n	DIFFOUT_T27n	A13	DQ3T	T_A_5	T_CA_5	
	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T28n	DIFFOUT_T28n	D15	DQ3T	T_A_3	T_CA_3	
	VREFB8AN0	IO .			DIFFIO_RX_T29p	DIFFOUT_T29p	C13	DQS3T	T_CK	T_CK	
	VREFB8AN0	10			DIFFIO_TX_T30p	DIFFOUT_T30p	E17 C12	DO0 0T	T_A_6	T_CA_6	
	VREFB8AN0 VREFB8AN0	IO			DIFFIO_RX_T29n DIFFIO_TX_T30n	DIFFOUT_T29n	E16	DQSn3T DQ3T	T_CK# T_A_7	T_CK# T_CA_7	
		IO			DIFFIO_TX_T30n DIFFIO_RX_T31p	DIFFOUT_T30n DIFFOUT_T31p	C14	DQ3T	T_BA_1	I_CA_/	
		IO			DIFFIO_TX_T32p	DIFFOUT_T32p	C14	DQ3T	T_BA_0		
BA	VREFB8AN0	IO			DIFFIO RX T31n	DIFFOUT T31n	B14	DQ3T	T BA 2		
8A		10			DIFFIO TX T32n	DIFFOUT T32n	B15	DQJI	GND	GND	
8A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T33p	DIFFOUT T33p	B16		OND	CIND	
8A	VREFB8AN0	10	OEROP, 11 EE_1E_1 BP		DIFFIO_TX_T34p	DIFFOUT_T34p	E18	DQ4T	T_CAS#		
8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T33n	DIFFOUT_T33n	A15	24	1_0/10/		
8A		IO			DIFFIO_TX_T34n	DIFFOUT_T34n	D19	DQ4T	T_RAS#	İ	Ì
8A		IO			DIFFIO_RX_T35p	DIFFOUT_T35p	B17	DQ4T	T_A_8	T_CA_8	1
		IO			DIFFIO_TX_T36p	DIFFOUT_T36p	C19	DQ4T	T_A_10	1 -	
8A		IO			DIFFIO_RX_T35n	DIFFOUT_T35n	A17	DQ4T	T_A_9	T_CA_9	
8A	VREFB8AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	C18	DQ4T	T_A_11		
8A	VREFB8AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	A19	DQS4T	T_CS#_0	T_CS#_0	
8A	VREFB8AN0	Ю			DIFFIO_TX_T38p	DIFFOUT_T38p	C21		T_A_12		
8A		Ю			DIFFIO_RX_T37n	DIFFOUT_T37n	A18	DQSn4T	T_CS#_1	T_CS#_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	B20	DQ4T	T_A_13		
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B19	DQ4T	T_A_14		
		10			DIFFIO_TX_T40p	DIFFOUT_T40p	D21	DQ4T	T_WE#		
	VREFB8AN0	10			DIFFIO_RX_T39n	DIFFOUT_T39n	A20	DQ4T	T_A_15		
9A		MSEL0		MSEL0			A23				
9A		CONF_DONE		CONF_DONE			A22				
9A		MSEL1		MSEL1			A24				
9A		nSTATUS		nSTATUS			B22				
9A		nCE		nCE			A25				
9A		MSEL2		MSEL2			B25				
9A		MSEL3		MSEL3			B24				
9A		nCONFIG		nCONFIG			C23				
9A		MSEL4		MSEL4	-		C24				
		GND GND					C22 A1				
		GND GND					A1 A11			_	
		GND		+			AA1				
		GND			+		AA10			+	
		GND			-		AA15				
		GND			-		AA23				
		GND					AB13				
		GND			1		AB24			1	
		GND					AC10				
		GND			1		AC23			1	GND
		GND					AC25				
		GND			1		AC5				
		GND					AD17				
		GND					AD22				
		GND					AE14				
		GND					AE19				
		GND					AE4				
		GND			ļ		B13			1	
		GND				1	B18				
		GND				1	B23				
		GND				1	B8				
		GND				1	C25				
		GND			_	1	C5	_			
		GND		_	_	1	D12	-		1	
		GND			1		D17			+	
		GND	1]	1	1	D2			I	
		GND					D22				





											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
		GND					E14				
		GND					E23				
		GND					E25				
		GND					E4				
		GND					F24				
		GND					G3				
		GND GND					H25 J22				GND
		GND					K4				GIND
		GND				1	L1				
		GND					L12				
		GND					L14				
		GND					M11				
		GND					M13				
		GND					M15				
		GND					M23				
		GND					P11				
		GND					P13				
		GND					P15				
	1	GND		+	ļ		R12	+		+	1
	 	GND	-	+	 	+	R14	+		+	1
	 	GND GND		+	 		R24 T1	 	+	 	
		GND					U3	+		_	
		GND					W22				
		GND					W24				
		GND					Y4				
		VCC					L11				
		VCC					L13				
		VCC					L15				
		VCC					M12				
		VCC					M14				
		VCC					N11				
		VCC					N12				
		VCC					N13				
		VCC VCC					N14				
		VCC					N15 P12				
		VCC					P12				
		VCC					R11	1			
		VCC					R13				
		VCC					R15				
		DNU					D24				
		DNU					E24				
		DNU					G2				
		DNU					B11				
		VCCPGM					AC21				
	ļ	VCCPGM			ļ		T3	 		_	
	ļ	VCCPGM		 	<u> </u>		D20			_	
	!	VCCBAT		+			B21			 	
	 	VCCIO1A	-	+	 	+	G23	+		+	DNU
	 	VCCIO1A VCCIO2A		+	1		K24 N25	+		 	DNU
	 	VCCIO2A VCCIO2A		+	1		N25 P22	+			DNU
	 	VCCIO2A VCCIO2A		+	 	1	U23	†		†	DNU
	1	VCCIO2A VCCIO2A		+	1	†	V25	+			DNU
	1	VCCIO2A VCCIO3A		1			AB18	1		1	55
	i e	VCCIO3A		1	1		AC20	1		1	
	1	VCCIO3B					AC15				
		VCCIO3B					AD12			<u> </u>	
		VCCIO3B					AE9				
		VCCIO4A					AB3				
		VCCIO4A					AB8				
	ļ	VCCIO4A		 	<u> </u>		AD2			_	
	ļ	VCCIO4A					AD7				
	!	VCCIO4A		+			W2			_	
	ļ	VCCIO5A		+	ļ	1	P2	_		 	
	1	VCCIO5A			1		R4			1	1



Pin Information for the Cyclone® V 5CEFA2 Device Version 1.3 Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	M383	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	Board Connection Requirement for Pin Migration Only
		VCCIO5B					J2				,
		VCCIO5B					M3				
		VCCIO7A					A6				
		VCCIO7A					B3				
		VCCIO7A		İ			C10				
		VCCIO7A					E9				
		VCCIO7A					F1				
		VCCIO8A					A16				
		VCCIO8A		i			A21				
		VCCIO8A					C15				
		VCCIO8A					C20				
		VCCPD1A2A					K22				DNU
	1	VCCPD1A2A VCCPD1A2A		<u> </u>		1	R23	t	1		DNU
	 	VCCPD3A		+	1	1	AB16	1		+	DITO
	+	VCCPD3B4A		- 		1	AB7	†		+	
		VCCPD3B4A VCCPD3B4A					AC13				<u> </u>
		VCCPD5A VCCPD5A				+	P4				
		VCCPD5B					L4				
		VCCPD7A8A					D13		1		
		VCCPD7A8A VCCPD7A8A					D16				-
	VDEEDAANO						D6				OND
1A		VREFB1AN0					L23				GND
2A	VREFB2AN0	VREFB2AN0				ļ	AC24				GND
3A	VREFB3AN0	VREFB3AN0				ļ	AD20				
3B	VREFB3BN0	VREFB3BN0					AC11		ļ		
4A		VREFB4AN0				ļ	AE7				
5A		VREFB5AN0					V3				
5B	VREFB5BN0	VREFB5BN0					K3				
7A	VREFB7AN0	VREFB7AN0					C9				
8A		VREFB8AN0					C17				
		RREF_TL					D25				
		VCCA_FPLL					L24				
		VCCA_FPLL					U24				
		VCCA_FPLL					AB23				
		VCCA_FPLL					D23				
		VCCA_FPLL					U4				
		VCCA_FPLL					G4				
		VCC_AUX					AA13				
		VCC_AUX					AA18				
		VCC AUX					AB6		İ		
		VCC AUX					D18				
		VCC AUX				İ	D5	Ì			
	İ	VCC AUX		İ		İ	E12	İ	İ		

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the

Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
2A	VREFB2AN0				DIFFIO_TX_L9n	DIFFOUT_L9n	C1			DDIKO/DDIKE (E)	
A	VREFB2AN0				DIFFIO_RX_L10n	DIFFOUT_L10n	L1	DQ1L			
Α	VREFB2AN0				DIFFIO_TX_L9p	DIFFOUT_L9p	C2	DQ1L			
Α	VREFB2AN0				DIFFIO_RX_L10p	DIFFOUT_L10p	L2	DQ1L			+
A	VREFB2AN0 VREFB2AN0				DIFFIO_RX_L11n DIFFIO_TX_L12n	DIFFOUT_L11n DIFFOUT_L12n	N1 E2	DQSn1L DQ1L		+	+
A	VREFB2AN0				DIFFIO_IX_L12II	DIFFOUT_L11p	N2	DQS1L			+
A	VREFB2AN0				DIFFIO_TX_L12p	DIFFOUT L12p	D3	DQSTL			+
Α	VREFB2AN0				DIFFIO TX L13n	DIFFOUT L13n	G1	DQ1L			
Α	VREFB2AN0	10			DIFFIO_RX_L14n	DIFFOUT_L14n	U1	DQ1L			
A	VREFB2AN0				DIFFIO_TX_L13p	DIFFOUT_L13p	G2	DQ1L			
A	VREFB2AN0				DIFFIO_RX_L14p	DIFFOUT_L14p	U2	DQ1L			
Α	VREFB2AN0				DIFFIO_RX_L15n	DIFFOUT_L15n	W2				
A	VREFB2AN0				DIFFIO_TX_L16n	DIFFOUT_L16n	AA1	DQ1L			
A.	VREFB2AN0				DIFFIO_RX_L15p	DIFFOUT_L15p	Y3	DOM			
A A	VREFB2AN0			TDO	DIFFIO_TX_L16p	DIFFOUT_L16p	AA2	DQ1L			
A		TDO nCSO		TDO DATA4			V3 AB6				+
A		TMS		TMS			R4				+
A	1	AS DATA3		DATA3	 	<u> </u>	AA5	1	+	1	+
A .	1	TCK		TCK	1		V5	1	1	1	1
3A	1	AS_DATA2		DATA2			T5				
BA		TDI		TDI			P5	<u> </u>			
3A		AS_DATA1		DATA1			W5				
3A		DCLK		DCLK			M5				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0			DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
3A	VREFB3AN0			DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0			DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
3A	VREFB3AN0			DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			_
3A 3A	VREFB3AN0			DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
3A 3A	VREFB3AN0 VREFB3AN0			DATA9 DATA12	DIFFIO_TX_B4n DIFFIO_RX_B3p	DIFFOUT_B4n DIFFOUT_B3p	R5 M7	DQ1B DQS1B		+	
3A	VREFB3AN0			DATA11	DIFFIO_RX_B3p	DIFFOUT_B4p	R6	DQSTB			+
3A	VREFB3AN0			DATA14	DIFFIO RX B5n	DIFFOUT B5n	R7	DQ1B			+
3A	VREFB3AN0			DATA13	DIFFIO TX B6n	DIFFOUT B6n	L7	DQ1B			_
3A	VREFB3AN0			CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B			_
3A	VREFB3AN0			DATA15	DIFFIO TX B6p	DIFFOUT B6p	L8	DQ1B			
3A		10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8				
3A		10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B			
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9				
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B			
3B	VREFB3BN0	10			DIFFIO_TX_B9n	DIFFOUT_B9n	V8				
3B		10			DIFFIO_RX_B10n	DIFFOUT_B10n	N8	DQ2B			
3B	VREFB3BN0	10			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B			
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B10p DIFFIO_RX_B11n	DIFFOUT_B10p DIFFOUT_B11n	M8 N9	DQ2B DQSn2B			-
3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B11h	DIFFOUT_B11h	AA7	DQSn2B DQ2B		+	
RR	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B12h	DIFFOUT_B12h	N10	DQS2B	+	+	+
3B	VREFB3BN0	10		1	DIFFIO_TX_B12p	DIFFOUT_B12p	AB7	DOGOZD	+	1	+
3B	VREFB3BN0	IO		İ	DIFFIO_TX_B13n	DIFFOUT B13n	Y7	DQ2B	1		+
3B	VREFB3BN0	IO			DIFFIO RX B14n	DIFFOUT B14n	U8	DQ2B	1		1
3B	VREFB3BN0	10			DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B			
3B	VREFB3BN0		_		DIFFIO_RX_B14p	DIFFOUT_B14p	V9	DQ2B			
3B		10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	R9				
3B	VREFB3BN0				DIFFIO_TX_B16n	DIFFOUT_B16n	AB8	DQ2B			
3B	VREFB3BN0		CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9	1			
3B	VREFB3BN0				DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B			
3B	VREFB3BN0				DIFFIO_TX_B17n	DIFFOUT_B17n	Y10	<u> </u>		-	
B	VREFB3BN0		<u> </u>	1	DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B	+	+	+
BB	VREFB3BN0			<u> </u>	DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B	+	+	+
BB BB	VREFB3BN0 VREFB3BN0			 	DIFFIO_RX_B18p DIFFIO_RX_B19n	DIFFOUT_B18p DIFFOUT_B19n	Y9 L9	DQ3B	+	+	+
3B	VREFB3BN0 VREFB3BN0			†	DIFFIO_RX_B19n DIFFIO_TX_B20n	DIFFOUT_B19h DIFFOUT_B20h	W11	DQSn3B DQ3B	+		+
3B 3B	VREFB3BN0 VREFB3BN0			1	DIFFIO_IX_B20fi DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B	+	1	+
3B	VREFB3BN0			1	DIFFIO_TX_B20p	DIFFOUT_B20p	Y11	- 4005	+	1	+
3B	VREFB3BN0		FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn	İ	DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B	1		+
3B		IO		İ	DIFFIO_RX_B22n	DIFFOUT_B22n	U10	DQ3B	1	1	1
BB		10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B			1
3B		IO			DIFFIO_RX_B22p	DIFFOUT_B22p	U11	DQ3B			
DD											



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
ιB	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B		DD110/DD112 (2)	El BBILL
B	VREFB3BN0		CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	R10				
B	VREFB3BN0	10			DIFFIO_TX_B24p	DIFFOUT_B24p	P12	DQ3B			
A	VREFB4AN0		RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	AA13				_
IA IA	VREFB4AN0 VREFB4AN0				DIFFIO_RX_B26n DIFFIO_TX_B25p	DIFFOUT_B26n DIFFOUT_B25p	W12 AB13	DQ4B DQ4B		_	
1A	VREFB4AN0				DIFFIO_IX_B25p	DIFFOUT B26p	Y12	DQ4B DQ4B	+	_	+
IA	VREFB4AN0				DIFFIO_RX_B26p	DIFFOUT B27n	U12	DQ4B DQSn4B			
1A	VREFB4AN0	10			DIFFIO TX B28n	DIFFOUT B28n	R12	DQ4B			+
1A	VREFB4AN0				DIFFIO RX B27p	DIFFOUT B27p	T12	DQS4B			_
IA.	VREFB4AN0				DIFFIO_TX_B28p	DIFFOUT_B28p	T13				
IA.	VREFB4AN0	10			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B			
IA.	VREFB4AN0	10			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B			
IA.	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B			
IA IA			OLIVA-		DIFFIO_RX_B30p DIFFIO_RX_B31n	DIFFOUT_B30p	V13	DQ4B		_	
1A 1A	VREFB4AN0 VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n DIFFIO_TX_B32n	DIFFOUT_B31n DIFFOUT_B32n	T14 AB18	DQ4B			+
1A	VREFB4AN0 VREFB4AN0	IO IO	CLK2p		DIFFIO_IX_B32h	DIFFOUT_B32h DIFFOUT_B31p	U13	DQ4B			+
1A	VREFB4AN0	.0	CERZP		DIFFIO_TX_B32p	DIFFOUT_B32p	AA18	DQ4B			+
1A	VREFB4AN0				DIFFIO_TX_B33n	DIFFOUT B33n	AA19	DQTD			+
1A	VREFB4AN0	10			DIFFIO RX B34n	DIFFOUT B34n	Y14	DQ5B	DQ1B		_
IA.	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B		
1A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W14	DQ5B	DQ1B		
4A	VREFB4AN0	10			DIFFIO_RX_B35n	DIFFOUT_B35n	P14	DQSn5B	DQ1B		
4A	VREFB4AN0	10			DIFFIO_TX_B36n	DIFFOUT_B36n	AA20	DQ5B	DQ1B		
1A		10			DIFFIO_RX_B35p	DIFFOUT_B35p	R14	DQS5B	DQ1B		
1A	VREFB4AN0	10			DIFFIO_TX_B36p	DIFFOUT_B36p	Y20				
IA.	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B		
IA.		10			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B		
IA IA		10			DIFFIO_TX_B37p DIFFIO_RX_B38p	DIFFOUT_B37p DIFFOUT_B38p	Y15 V15	DQ5B DQ5B	DQ1B DQ1B		+
IA	VREFB4AN0		CLK3n		DIFFIO_RX_B38p	DIFFOUT B39n	R15	DQSB	DQIB		+
IA	VREFB4AN0		CERSII		DIFFIO_TX_B40n	DIFFOUT B40n	AB20	DQ5B	DQ1B		+
1A	VREFB4AN0		CLK3p		DIFFIO RX B39p	DIFFOUT B39p	T15	DQOD	DQID		+
4A	VREFB4AN0		OLTOP		DIFFIO TX B40p	DIFFOUT B40p	AB21	DQ5B	DQ1B		_
4A	VREFB4AN0				DIFFIO TX B41n	DIFFOUT B41n	AB22				_
4A	VREFB4AN0				DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B		_
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B		
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B		
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B		
4A	VREFB4AN0	10			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B		
1A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B		
1A 1A	VREFB4AN0	10			DIFFIO_TX_B44p	DIFFOUT_B44p	AB17	D.O.O.D.	2012		_
1A 1A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B45n DIFFIO_RX_B46n	DIFFOUT_B45n DIFFOUT_B46n	Y22 V18	DQ6B DQ6B	DQ1B DQ1B		+
1A	VREFB4AN0 VREFB4AN0	io			DIFFIO_RX_B46fi	DIFFOUT_B46n DIFFOUT_B45p	Y21	DQ6B DQ6B	DQ1B DQ1B		+
1A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT B46p	W18	DQ6B	DQ1B DQ1B		+
1A	VREFB4AN0	IO			DIFFIO RX B47n	DIFFOUT B47n	W16	DQOD	DQID		+
1A	VREFB4AN0	10			DIFFIO TX B48n	DIFFOUT B48n	W21	DQ6B	DQ1B		1
1A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT_B47p	W17		1		
IA.	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	W22	DQ6B	DQ1B		
iA .	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R			
5A	VREFB5AN0	10		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20				
5A		10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19		1		\bot
5A		10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	1	+	+
A.	VREFB5ANO			CvP_CONFDONE	DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	+	+	+
M	VREFB5AN0 VREFB5AN0			CVP_CONFDONE	DIFFIO_TX_R3n DIFFIO_RX_R4n	DIFFOUT_R3n DIFFOUT_R4n	T20 T18	DQ1R DQ1R	+	+	+
ΣΔ	VREFB5AN0 VREFB5AN0			DEV_OE	DIFFIO_RX_R4n DIFFIO_TX_R5p	DIFFOUT_R5p	T22	DUTK	1	+	+
iA				DLV_OL	DIFFIO_IX_RSp	DIFFOUT_R5p	R16	DQS1R	1	+	+
iA.	VREFB5AN0			DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT R5n	R22	DQ3TR DQ1R	1	+	+
5A	VREFB5AN0	10			DIFFIO RX R6n	DIFFOUT R6n	R17	DQSn1R	1	1	+
iA	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R			
iA	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R			1
iA	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21				<u> </u>
iΑ	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R			
iB	VREFB5BN0	10	CLK6p		DIFFIO_RX_R9p	DIFFOUT_R9p	L17				
iB	VREFB5BN0	10			DIFFIO_TX_R10p	DIFFOUT_R10p	E20	DQ2R			
iB	VREFB5BN0	10	CLK6n		DIFFIO_RX_R9n	DIFFOUT_R9n	K17		ļ		
5B	VREFB5BN0	10			DIFFIO_TX_R10n	DIFFOUT_R10n	F20	DQ2R			



			Institute Francisco(s)								Note
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3	VREFB5BN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	H20	DQ2R	+	DDR3/DDR2 (2)	LFDDKZ
	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	G18	DQ2R			
	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	H19	DQ2R			
	VREFB5BN0		FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	G17	DQ2R			
	VREFB5BN0				DIFFIO_RX_R13p	DIFFOUT_R13p	K16	DQS2R			
	VREFB5BN0				DIFFIO_TX_R14p	DIFFOUT_R14p	F19				
	VREFB5BN0				DIFFIO_RX_R13n	DIFFOUT_R13n	J16	DQSn2R			
	VREFB5BN0				DIFFIO_TX_R14n	DIFFOUT_R14n	F18	DQ2R			_
	VREFB5BN0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	J17	DQ2R			
	VREFB5BN0				DIFFIO_TX_R16p	DIFFOUT_R16p	J19	DQ2R		+	
	VREFB5BN0 VREFB5BN0	IO IO			DIFFIO_RX_R15n DIFFIO_TX_R16n	DIFFOUT_R15n DIFFOUT_R16n	J18 H18	DQ2R		+	
	VKEFB3BINU	GND			DIFFIO_IX_KIBII	DIFFOUT_R16II	F17	+		+	
	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	H16	+		GND	GND
					DIFFIO_TX_T2p	DIFFOUT_T2p	C21	DQ1T	DQ1T	T DM 2	T DM 2
					DIFFIO RX T1n	DIFFOUT T1n	G16	DQII	DQTT	GND	GND
	VREFB7AN0	10			DIFFIO_TX_T2n	DIFFOUT T2n	C20	DQ1T	DQ1T	T_DQ_23	T_DQ_23
	VREFB7AN0	10			DIFFIO_RX_T3p	DIFFOUT_T3p	D18	DQ1T	DQ1T	T_DQ_21	T_DQ_21
	VREFB7AN0	10			DIFFIO TX T4p	DIFFOUT_T4p	B20	DQ1T	DQ1T	T_DQ_22	T_DQ_22
	VREFB7AN0			1	DIFFIO RX T3n	DIFFOUT_T3n	E17	DQ1T	DQ1T	T_DQ_20	T_DQ_22
				İ	DIFFIO TX T4n	DIFFOUT_T4n	B21	DQ1T	DQ1T	GND	GND
	VREFB7AN0				DIFFIO_RX_T5p	DIFFOUT_T5p	G15	DQS1T	DQS1T	T_DQS_2	T_DQS_2
					DIFFIO_TX_T6p	DIFFOUT_T6p	B22	1	1	T_RESET#	T_RESET#
	VREFB7AN0	10			DIFFIO_RX_T5n	DIFFOUT_T5n	G14	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	A22	DQ1T	DQ1T	T_DQ_19	T_DQ_19
	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	E16	DQ1T	DQ1T	T_DQ_17	T_DQ_17
	VREFB7AN0	10			DIFFIO_TX_T8p	DIFFOUT_T8p	A20	DQ1T	DQ1T	T_DQ_18	T_DQ_18
	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	D17	DQ1T	DQ1T	T_DQ_16	T_DQ_16
	VREFB7AN0				DIFFIO_TX_T8n	DIFFOUT_T8n	A19			GND	GND
	VREFB7AN0		CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	G13				
		IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C19	DQ2T	DQ1T	T_DM_1	T_DM_1
	VREFB7AN0		CLK11n		DIFFIO_RX_T9n	DIFFOUT_T9n	F14				
	VREFB7AN0				DIFFIO_TX_T10n	DIFFOUT_T10n	C18	DQ2T	DQ1T	T_DQ_15	T_DQ_15
	VREFB7AN0				DIFFIO_RX_T11p	DIFFOUT_T11p	C16	DQ2T	DQ1T	T_DQ_13	T_DQ_13
	VREFB7AN0				DIFFIO_TX_T12p	DIFFOUT_T12p	B16	DQ2T	DQ1T	T_DQ_14	T_DQ_14
	VREFB7AN0				DIFFIO_RX_T11n	DIFFOUT_T11n	C15	DQ2T	DQ1T	T_DQ_12	T_DQ_12
	VREFB7AN0				DIFFIO_TX_T12n	DIFFOUT_T12n	B15	DQ2T	DQ1T	T_CKE_0	T_CKE_0
	VREFB7AN0				DIFFIO_RX_T13p	DIFFOUT_T13p	G12	DQS2T	DQ1T	T_DQS_1	T_DQS_1
	VREFB7AN0	10			DIFFIO_TX_T14p	DIFFOUT_T14p	A18	DOC-OT	DQ1T	T_CKE_1	T_CKE_1
	VREFB7AN0 VREFB7AN0				DIFFIO_RX_T13n DIFFIO_TX_T14n	DIFFOUT_T13n DIFFOUT_T14n	H12 A17	DQSn2T DQ2T	DQ1T DQ1T	T_DQS#_1 T_DQ_11	T_DQS#_1 T_DQ_11
	VREFB7AN0	IO IO			DIFFIO_TX_T14II	DIFFOUT_T15p	F15	DQ2T	DQ1T	T_DQ_11	T_DQ_9
	VREFB7AN0 VREFB7AN0	IO IO			DIFFIO_RX_115p	DIFFOUT_T16p	B18	DQ2T	DQ1T	T_DQ_9	T_DQ_10
	VREFB7AN0	IO			DIFFIO_TX_T15n	DIFFOUT_T15n	E14	DQ2T	DQ1T	T_DQ_10	T_DQ_10
	VREFB7AN0	IO .			DIFFIO_TX_T16n	DIFFOUT_T16n	B17	DQZI	DQTT	GND	GND
	VREFB7AN0	IO .	CLK10p		DIFFIO_TX_T16II	DIFFOUT_T17p	H10	+		GIND	GIND
	VREFB7AN0	10	CERTOP		DIFFIO_TX_T18p	DIFFOUT_T18p	A15	DQ3T	- 	T DM 0	T DM 0
	VREFB7AN0	IO	CLK10n		DIFFIO RX T17n	DIFFOUT_T17n	G11	DQUI	- 	T_DIWI_0	T_DIVI_0
	VREFB7AN0	10	CENTON		DIFFIO TX T18n	DIFFOUT T18n	A14	DQ3T	-	T DQ 7	T DQ 7
	VREFB7AN0	10		İ	DIFFIO RX T19p	DIFFOUT_T19p	D13	DQ3T	_	T DQ 5	T DQ 5
	VREFB7AN0	10		İ	DIFFIO_TX_T20p	DIFFOUT_T20p	C14	DQ3T	_	T_DQ_6	T_DQ_6
	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	C13	DQ3T	1	T_DQ_4	T_DQ_4
	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	D14	DQ3T		T_ODT_1	T_ODT_1
		IO			DIFFIO_RX_T21p	DIFFOUT_T21p	H9	DQS3T		T_DQS_0	T_DQS_0
	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	A13	1		T_ODT_0	T_ODT_0
	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	G8	DQSn3T		T_DQS#_0	T_DQS#_0
	VREFB7AN0				DIFFIO_TX_T22n	DIFFOUT_T22n	B13	DQ3T		T_DQ_3	T_DQ_3
	VREFB7AN0				DIFFIO_RX_T23p	DIFFOUT_T23p	E12	DQ3T		T_DQ_1	T_DQ_1
	VREFB7AN0				DIFFIO_TX_T24p	DIFFOUT_T24p	B12	DQ3T		T_DQ_2	T_DQ_2
	VREFB7AN0				DIFFIO_RX_T23n	DIFFOUT_T23n	F12	DQ3T		T_DQ_0	T_DQ_0
			RZQ_2		DIFFIO_TX_T24n	DIFFOUT_T24n	A12				
		10	CLK9p		DIFFIO_RX_T25p	DIFFOUT_T25p	G10				
	VREFB8AN0	10			DIFFIO_TX_T26p	DIFFOUT_T26p	C11	DQ4T		T_A_0	T_CA_0
	VREFB8AN0	10	CLK9n		DIFFIO_RX_T25n	DIFFOUT_T25n	F10				
	VREFB8AN0	10		ļ	DIFFIO_TX_T26n	DIFFOUT_T26n	B11	DQ4T		T_A_1	T_CA_1
	VREFB8AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	D11	DQ4T		T_A_4	T_CA_4
	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	A8	DQ4T		T_A_2	T_CA_2
	VREFB8AN0	10		1	DIFFIO_RX_T27n	DIFFOUT_T27n	E11	DQ4T		T_A_5	T_CA_5
		_									
	VREFB8AN0 VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T28n DIFFIO_RX_T29p	DIFFOUT_T28n DIFFOUT_T29p	A7	DQ4T DQS4T		T_A_3 T_CK	T_CA_3 T_CK



Bank	lyper	Din Name/Eurotian	Ontional Function(s)	Configuration Europian	Dedicated Ty/Dy	Emulated I VDC Output Channel	111404	DOC for Vo	DOS 604 V46	LIMC Din	Tumo nin
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	J8	DQSn4T		T_CK#	T_CK#
8A	VREFB8AN0				DIFFIO_TX_T30n	DIFFOUT_T30n	E7	DQ4T		T_A_7	T_CA_7
8A	VREFB8AN0				DIFFIO_RX_T31p	DIFFOUT_T31p	C10	DQ4T		T_BA_1	
8A	VREFB8AN0				DIFFIO_TX_T32p	DIFFOUT_T32p	C6	DQ4T		T_BA_0	
BA	VREFB8AN0				DIFFIO_RX_T31n	DIFFOUT_T31n	C9	DQ4T		T_BA_2	
BA .	VREFB8AN0		OLIZA EDILI EL ED		DIFFIO_TX_T32n	DIFFOUT_T32n	D7			GND	GND
BA BA	VREFB8ANO		CLK8p,FPLL_TL_FBp		DIFFIO_RX_T33p	DIFFOUT_T33p	K7	DOET		T CAS#	-
BA BA	VREFB8AN0 VREFB8AN0		CLK8n,FPLL_TL_FBn		DIFFIO_TX_T34p DIFFIO_RX_T33n	DIFFOUT_T34p DIFFOUT_T33n	A10 J7	DQ5T		T_CAS#	
BA	VREFB8AN0		CEROII, I FEE_IE_I BII		DIFFIO_TX_T34n	DIFFOUT_T34n	A9	DQ5T		T_RAS#	-
BA .	VREFB8AN0				DIFFIO_RX_T35p	DIFFOUT_T35p	D9	DQ5T		T_A_8	T_CA_8
3A	VREFB8AN0				DIFFIO_TX_T36p	DIFFOUT_T36p	B6	DQ5T		T_A_10	
BA	VREFB8AN0				DIFFIO_RX_T35n	DIFFOUT_T35n	D8	DQ5T		T_A_9	T_CA_9
3A	VREFB8AN0	10			DIFFIO_TX_T36n	DIFFOUT_T36n	B5	DQ5T		T_A_11	
3A	VREFB8AN0				DIFFIO_RX_T37p	DIFFOUT_T37p	H8	DQS5T		T_CS#_0	T_CS#_0
3A	VREFB8AN0				DIFFIO_TX_T38p	DIFFOUT_T38p	C8			T_A_12	
3A	VREFB8AN0				DIFFIO_RX_T37n	DIFFOUT_T37n	G7	DQSn5T		T_CS#_1	T_CS#_1
BA	VREFB8AN0				DIFFIO_TX_T38n	DIFFOUT_T38n	B8	DQ5T		T_A_13	
BA	VREFB8AN0			1	DIFFIO_RX_T39p	DIFFOUT_T39p	H6	DQ5T	1	T_A_14	1
BA	VREFB8AN0			 	DIFFIO_TX_T40p	DIFFOUT_T40p	E6	DQ5T	 	T_WE#	+
A .	VREFB8AN0 VREFB8AN0			+	DIFFIO_RX_T39n DIFFIO_TX_T40n	DIFFOUT_T39n DIFFOUT_T40n	G6	DQ5T	 	T_A_15	GND
BA BA	VKEFB8ANU	MSEL0		MSEL0	DIFFIU_IX_140fi	DIFFO01_140N	F7 L6		 	GND	GIND
9A 9A	 	CONF_DONE		CONF_DONE	1	 	J6	 	 	+	†
9A	 	MSEL1		MSEL1			K6		—	+	1
9A	i	nSTATUS		nSTATUS	1		G5	1	t	1	1
A.		nCE		nCE			H5				
ΙA		MSEL2		MSEL2			A2				
Α		MSEL3		MSEL3			E5				ĺ
A		nCONFIG		nCONFIG			A4				
A		MSEL4		MSEL4			C5				
ΙA		GND					F3				
		GND					A21				
		GND					AB19				
		GND					AB2				
		GND GND					AB1 AA16				
		GND					AA16 AA11				
		GND					AA11				
		GND					AA3				+
		GND					Y13				
		GND					Y8				
		GND					Y5				
		GND					Y2				
		GND					Y1				
		GND					W20				
		GND					W4				
		GND				ļ	W3				-
		GND		1	1	-	V22	1	1	+	+
	 	GND	<u> </u>	1	1	<u> </u>	V17	 	 	+	+
	-	GND GND		+		+	V4 V2		 	+	+
	1	GND		 	1	 	V2 V1	1	t	+	1
	 	GND		1	1	 	U19		 	 	+
	1	GND		1			U14		1		1
	İ	GND		İ			U9	İ	İ	1	İ
		GND					U5				
		GND					U4				
		GND					U3				
		GND					T11				
		GND			ļ		T2		ļ	1	1
	ļ	GND				I	T1			1	1
	 	GND		 		-	R13		 	1	+
		GND		 		-	R3		 	1	+
		GND		-	-		P10 P4		 	+	+
	1	GND GND		 	1	<u> </u>	P4 P2		 	1	+
	 	GND		+	1	+	P2 P1	1	 	+	+
	 	GND		+			N22		 	+	+
	i	GND		1	1		N15	1	t	1	1
		GND	•				N13				





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					N11				
		GND					N7				
		GND					N5				
	+	GND GND					N3 M19				
		GND					M19 M14				-
	+	GND					M12				
		GND					M12 M9				+
		GND					M4				+
	-	GND					M2				
		GND					M1				1
	1	GND					L16				
	1	GND					L13				
		GND					L11				
		GND					L5				
		GND		İ			L3				1
		GND		İ			K14				1
		GND		İ			K12				1
		GND					K10				
		GND					K8				
		GND					K4				
		GND					K2				
		GND					K1				
		GND					J20				ļ <u> </u>
		GND					J15				
		GND					J13				
		GND					J11				
		GND					J5				
		GND					J3				
		GND					H14				
		GND					H4				
		GND					H3				
		GND					H2				
	-	GND			-		H1	-			
		GND GND					G9 G4				-
	-	GND			-		G4 G3	-			
		GND					F21				-
	+	GND			+	-	F16				+
	+	GND			<u> </u>		F11	-			+
	+	GND			<u> </u>		F6	-			+
	+	GND			<u> </u>		F5	-			+
		GND					F2				+
		GND					F1				+
		GND					E13				1
	1	GND					E4				
		GND		1			E3				
	İ	GND			İ		D20	İ	Ì	Ì	1
		GND					D10				1
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C22				
		GND					C17				
		GND					C7				
		GND					C4				ļ <u> </u>
		GND					C3				
		GND					B14				
		GND					B2				
		GND		ļ		ļ	B1				_
		GND			L	1	A11	L			<u> </u>
	_	GND		1			A5				4
	_	VCC		1			L4				4
	_	vcc		1			P15				4
	1	VCC		1	1		P13	1	ļ	ļ	+
	+	VCC		1	 	 	P11	 	ļ	-	
	1	VCC		1	1		P3	1	ļ	ļ	+
	+	VCC		1	 	 	N14	 	ļ	-	
	 	VCC			-		N12	_	-	-	+
 	 	VCC VCC		+	-	-	N4	-	-	-	
		VCC		1	1		M15	1	1	1	1





										Note (1)
Bank Number		Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	VCC					M13				
	VCC					M11				
	VCC					L14				
	VCC					L12				
	VCC					L10				
	VCC					K13				
	VCC					K11				
	VCC					K9				
	VCC					K5				
	VCC					K3				+
	VCC VCC					J14 J12				
	VCC					J12 J10				
	VCC					J4				+
	VCC					H15				+
	VCC					H13				†
	VCC					H11				†
	DNU					B3				1
	DNU					B4				
	DNU					D21				1
	DNU					E10				1
	VCCPGM					Y6				
	VCCPGM					U20				
	VCCPGM					B7				
	VCCBAT					A3				
	VCCIO2A					D4				
	VCCIO2A					Y4				
	VCCIO2A					R1				
	VCCIO2A					J1				
	VCCIO3A					T6				
	VCCIO3A					AA6				
	VCCIO3B					R8				
	VCCIO3B					AB9				
	VCCIO3B					W10				
	VCCIO3B					V7				+
	VCCIO4A					T16				
	VCCIO4A VCCIO4A					AB14 AA21				
	VCCIO4A VCCIO4A					Y18				+
	VCCIO4A VCCIO4A					W15				+
	VCCIO4A VCCIO4A					V12				+
	VCCIO5A					T21				+
	VCCIO5A					R18				†
	VCCIO5B					G19				1
	VCCIO5B					P20				
	VCCIO5B					N17				1
	VCCIO5B					L21				
	VCCIO5B					K18				
	VCCIO5B					H22				
	VCCIO7A					B19				
	VCCIO7A					H17				
	VCCIO7A					E18				
	VCCIO7A					D15				
	VCCIO7A					C12				
	VCCIO7A					A16				
	VCCIO8A		1			B9		1		+
	VCCIO8A		ļ			H7				
	VCCIO8A	 	1	ļ	 	E8		 	ļ	+
	VCCIO8A		-			A6 R2				+
	VCCPD1A2A		+			J2				+
	VCCPD1A2A VCCPD1A2A		+	1	 	J2 E1	-	1	1	+
	VCCPD1A2A VCCPD3A		 			V6				+
	VCCPD3A VCCPD3B4A					W9				+
	VCCPD3B4A VCCPD3B4A		 			V16				+
	VCCPD3B4A VCCPD3B4A		1			V16 V14				
	VCCPD3B4A VCCPD3B4A		1	1		V10		1		
	VCCPD5A		1			P17				
	VCCPD5B		İ	İ		M18	İ	İ		1
		i	t				t	1		+
	VCCPD5B					N19				



Pin Information for the Cyclone® V 5CEFA2 Device Version 1.3 Note (1)

Bank Number			Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCPD7A8A					F13				
		VCCPD7A8A					F9				
		VCCPD7A8A					E9				
2A		VREFB2AN0					W1				
3A	VREFB3AN0	VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0					AB12				
4A	VREFB4AN0	VREFB4AN0					AA14				
5A		VREFB5AN0					V21				
5B	VREFB5BN0	VREFB5BN0					K20				
7A		VREFB7AN0					D16				
8A		VREFB8AN0					B10				
0,1	TILLI BOTTING	NC					AB3				
		NC					V11				
		NC		+			P22				
		NC					P21				
											+
		NC NO					P18	 			
	+	NC .		-	 	 	P16	 	 	 	
		NC		.	ļ	1	N21	ļ	-	1	-
		NC				ļ	N20				
		NC					N18			ļ	ļ
		NC					N16				
		NC					M22				
		NC					M21				
		NC					M20				
		NC					M17				
		NC					M16				
		NC					L22				
		NC .					L20				
		NC					L19				
		NC					L18				
		NC					L15				
		NC		+			K22				
		NC					K21				
		NC .					K19				
		NC .		!			K15				
		NC					J22				
		NC					J21				
		NC				ļ	H21				
		NC				ļ	G22				
		NC					G21				
		NC					G20			1	
		NC					F22				
		NC					E22				
		NC				1	E21				
		NC					D22				
		RREF_TL					A1				
		VCCA_FPLL					M3				
		VCCA_FPLL				İ	T3	Ì		İ	İ
	1	VCCA FPLL		1			T4	1		İ	İ
	1	VCCA_FPLL					F4	İ		1	1
	-	VCCA_FPLL				1	U18	 			
	+					1	E19	†		t	t
	-	VCCA_FPLL		-		+	D6	+	-	-	—
		VCC_AUX						 			
		VCC_AUX			-		D12	+			-
		VCC_AUX		.	ļ	1	D19	ļ		1	-
		VCC_AUX				ļ	W19				
		VCC_AUX					AA12			1	
Notes:		VCC_AUX					AB5	<u> </u>			

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



			Ontional Function(s)	T T			TE484				Note (1)	
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	
2A	VREFB2AN0	10			DIFFIO_TX_L9n	DIFFOUT_L9n	C1			DDI(3)DDI(2 (2)	LIDDICE	
2A	VREFB2AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	G1	DQ1L			1	
2A	VREFB2AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L9p	C2	DQ1L			1	
2A	VREFB2AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	G2	DQ1L				
2A	VREFB2AN0	10			DIFFIO_RX_L11n	DIFFOUT_L11n	E2	DQSn1L				
2A		10			DIFFIO_TX_L12n	DIFFOUT_L12n	L1	DQ1L				
2A	VREFB2AN0	10			DIFFIO_RX_L11p	DIFFOUT_L11p	D3	DQS1L				
2A	VREFB2AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L12p	L2					
2A	VREFB2AN0	10			DIFFIO_TX_L13n	DIFFOUT_L13n	N1	DQ1L				
2A	VREFB2AN0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	U1	DQ1L				
2A	VREFB2AN0	IO			DIFFIO_TX_L13p	DIFFOUT_L13p	N2	DQ1L				
2A	VREFB2AN0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	U2	DQ1L				
2A	VREFB2AN0	10			DIFFIO_RX_L15n	DIFFOUT_L15n	W2					
2A	VREFB2AN0	10			DIFFIO_TX_L16n	DIFFOUT_L16n	AA1	DQ1L				
2A	VREFB2AN0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	Y3					
2A	VREFB2AN0	10			DIFFIO_TX_L16p	DIFFOUT_L16p	AA2	DQ1L				
3A		TDO		TDO			M5					
3A		nCSO		DATA4			R4					
3A		TMS		TMS			P5					
3A		AS_DATA3		DATA3			T4					
3A		TCK		TCK			V5					
3A		AS_DATA2		DATA2	ļ	1	AA5					
3A		TDI		TDI	ļ	1	W5					
3A		AS_DATA1		DATA1	ļ	1	AB3					
3A		DCLK		DCLK		1	V3					
3A		AS_DATA0,ASDO		DATA0			AB4					
3A	VREFB3AN0			DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B				
3A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7					
3A	VREFB3AN0	10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B				
3A	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B				
3A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B				
3A	VREFB3AN0	10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B				
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B				
3A	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9					
3A	VREFB3AN0	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B				
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B				
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B				
3A	VREFB3AN0	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B				
3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6					
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B				
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7					
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B				
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB6					
3B	VREFB3BN0	10			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B				
3B		10			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B				
3B		10			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B				
3B		10			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B				
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B				
3B	VREFB3BN0			ļ	DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B				
3B	VREFB3BN0	10		ļ	DIFFIO_TX_B12p	DIFFOUT_B12p	AB7	L				
3B				ļ	DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B		-		
3B	VREFB3BN0	IO		ļ	DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B		-		
3B	VREFB3BN0	IO		!	DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B	+			
3B	VREFB3BN0	10		ļ	DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B				
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn	ļ	DIFFIO_RX_B15n	DIFFOUT_B15n	M8			-		
3B	VREFB3BN0	IO	1	!	DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B	+			
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp	ļ	DIFFIO_RX_B15p	DIFFOUT_B15p	M9	2002		-		
3B	VREFB3BN0	10		!	DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B	+			
3B	VREFB3BN0	10		1	DIFFIO_TX_B17n	DIFFOUT_B17n	Y10	2002	+		+	
BB	VREFB3BN0	10		1	DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B	+		+	
3B	VREFB3BN0	10		ļ	DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B		-		
3B	VREFB3BN0	10		1	DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B	+	-	+	
3B	VREFB3BN0	IU		1	DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B	+		+	
3B	VREFB3BN0	10		ļ	DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B		-		
38	VREFB3BN0	10		!	DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B	+			
3B	VREFB3BN0	10	EDIT DI OLIGORIA EDIT DI CONTROL	1	DIFFIO_TX_B20p	DIFFOUT_B20p	P12	2002	+	-	+	
3B		10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B				
3B		10		ļ	DIFFIO_RX_B22n	DIFFOUT_B22n	R10	DQ3B		-		
3B	VREFB3BN0		FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB	ļ	DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B			+	
3B	VREFB3BN0		CLK1n		DIFFIO_RX_B22p DIFFIO_RX_B23n	DIFFOUT_B22p	R11	DQ3B				
3B	VREFB3BN0					DIFFOUT B23n	P9					

Pin List F23



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0				DIFFIO_TX_B24n	DIFFOUT_B24n	Y11	DQ3B		551(0/551(2 (2)	
B	VREFB3BN0	-	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	N9				
BB IA	VREFB3BN0 VREFB4AN0	10	RZQ 0		DIFFIO_TX_B24p DIFFIO_TX_B25n	DIFFOUT_B24p DIFFOUT_B25n	AA12 AB13	DQ3B			+
1A	VREFB4AN0 VREFB4AN0		RZQ_0		DIFFIO_IX_B25n DIFFIO_RX_B26n	DIFFOUT_B25n DIFFOUT_B26n	V13	DQ4B			+
1A	VREFB4AN0				DIFFIO TX B25p	DIFFOUT B25p	AB12	DQ4B			+
1A	VREFB4AN0	10			DIFFIO_RX_B26p	DIFFOUT_B26p	U13	DQ4B			
1A	VREFB4AN0				DIFFIO_RX_B27n	DIFFOUT_B27n	T12	DQSn4B			
4A	VREFB4AN0				DIFFIO_TX_B28n	DIFFOUT_B28n	AA14	DQ4B			
1A 1A	VREFB4AN0 VREFB4AN0				DIFFIO_RX_B27p DIFFIO_TX_B28p	DIFFOUT_B27p DIFFOUT_B28p	T13 AA13	DQS4B			+
1A	VREFB4AN0				DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B			+
4A	VREFB4AN0				DIFFIO_RX_B30n	DIFFOUT_B30n	Y14	DQ4B			1
1A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AA15	DQ4B			
4A		10			DIFFIO_RX_B30p	DIFFOUT_B30p	Y15	DQ4B			
4A	VREFB4AN0 VREFB4AN0		CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	V14 AB17	2012			_
4A 4A		lio	CLK2p		DIFFIO_TX_B32n DIFFIO_RX_B31p	DIFFOUT_B32n DIFFOUT_B31p	V15	DQ4B			+
4A	VREFB4AN0	.0	CERZP		DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B			-
4A	VREFB4AN0				DIFFIO_TX_B33n	DIFFOUT_B33n	AB20				
1A		IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B		
4A	VREFB4AN0				DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B		
4A	VREFB4AN0				DIFFIO_RX_B34p	DIFFOUT_B34p	Y17	DQ5B	DQ1B		
4A 4A	VREFB4AN0 VREFB4AN0				DIFFIO_RX_B35n DIFFIO_TX_B36n	DIFFOUT_B35n DIFFOUT_B36n	T14 AA17	DQSn5B DQ5B	DQ1B DQ1B		+
4A	VREFB4AN0				DIFFIO_IX_B35p	DIFFOUT B35p	U15	DQS5B	DQ1B		+
4A	VREFB4AN0	10			DIFFIO_TX_B36p	DIFFOUT B36p	AA18	DQOOD	DQID		-
4A	VREFB4AN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	AA19	DQ5B	DQ1B		1
4A	VREFB4AN0				DIFFIO_RX_B38n	DIFFOUT_B38n	V20	DQ5B	DQ1B		
4A	VREFB4AN0				DIFFIO_TX_B37p	DIFFOUT_B37p	AA20	DQ5B	DQ1B		
4A	VREFB4AN0		011/0		DIFFIO_RX_B38p	DIFFOUT_B38p	W19	DQ5B	DQ1B		_
1A 1A	VREFB4AN0 VREFB4AN0		CLK3n		DIFFIO_RX_B39n DIFFIO_TX_B40n	DIFFOUT_B39n DIFFOUT_B40n	V16 AB22	DQ5B	DQ1B		+
4A	VREFB4AN0		CLK3p		DIFFIO RX B39p	DIFFOUT B39p	W16	DQJB	DQID		+
4A	VREFB4AN0				DIFFIO TX B40p	DIFFOUT B40p	AA22	DQ5B	DQ1B		
4A	VREFB4AN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y22				
4A	VREFB4AN0				DIFFIO_RX_B42n	DIFFOUT_B42n	Y20	DQ6B	DQ1B		
4A	VREFB4AN0				DIFFIO_TX_B41p	DIFFOUT_B41p	W22	DQ6B	DQ1B		
4A 4A	***************************************	10			DIFFIO_RX_B42p DIFFIO_RX_B43n	DIFFOUT_B42p DIFFOUT_B43n	Y19 P14	DQ6B DQSn6B	DQ1B DQSn1B		+
4A 4A		lin			DIFFIO_RX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ3IIIB DQ1B		+
4A	VREFB4AN0	10			DIFFIO RX B43p	DIFFOUT_B43p	R14	DQS6B	DQS1B		
4A	VREFB4AN0	10			DIFFIO_TX_B44p	DIFFOUT_B44p	W21				
4A		10			DIFFIO_TX_B45n	DIFFOUT_B45n	U22	DQ6B	DQ1B		
4A	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	V19	DQ6B	DQ1B		
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B45p DIFFIO_RX_B46p	DIFFOUT_B45p DIFFOUT_B46p	V21 V18	DQ6B DQ6B	DQ1B DQ1B		
+A 1Δ	VREFB4AN0	In			DIFFIO_RX_B46p	DIFFOUT B47n	U16	DQ0B	DQIB		+
4A	VREFB4AN0	IO			DIFFIO_RX_B47II	DIFFOUT B48n	U21	DQ6B	DQ1B		+
IA.	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B47p	U17				
4A	VREFB4AN0	Ю			DIFFIO_TX_B48p	DIFFOUT_B48p	U20	DQ6B	DQ1B		
iΑ	VREFB5AN0	10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R		1	
A	VREFB5AN0 VREFB5AN0	10		INIT_DONE PR REQUEST	DIFFIO_RX_R2p DIFFIO_TX_R1n	DIFFOUT_R2p DIFFOUT_R1n	T18 T20	DQ1R	1	+	+
-A		lio		CRC_ERROR	DIFFIO_IX_R1n DIFFIO_RX_R2n	DIFFOUT_R2n	T17	שעוא		1	+
iΑ	VREFB5AN0			nCEO	DIFFIO_RX_R2II	DIFFOUT_R2D	T22	DQ1R		†	+
iΑ	VREFB5AN0			1	DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R		1	1
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
iΑ	VREFB5AN0				DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R		<u> </u>	
<u>A</u>	VREFB5AN0			DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21	DOC4D	1	-	+
5A	VREFB5AN0 VREFB5AN0			DEV_CLRn	DIFFIO_RX_R6p DIFFIO_TX_R5n	DIFFOUT_R6p DIFFOUT_R5n	R16 P22	DQS1R DQ1R	1	+	+
5A	VREFB5AN0 VREFB5AN0			DLV_CLRII	DIFFIO_IX_R5n DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQ1R DQSn1R	1	+	+
5A	VREFB5AN0				DIFFIO_RX_R6II DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			1
5A	VREFB5AN0				DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			1
		10		1	DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
5A	VREFB5AN0										_
5A	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R			
SA SB	VREFB5AN0 VREFB5BN0	IO IO	CLK6p		DIFFIO_RX_R8n DIFFIO_RX_R9p	DIFFOUT_R9p	N16				
	VREFB5AN0 VREFB5BN0 VREFB5BN0	10	CLK6p CLK6n		DIFFIO_RX_R8n			DQ1R DQ2R			-

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ank lumber		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
В	VREFB5BN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	N19	DQ2R			
В	VREFB5BN0		FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	M22	DQ2R			
3	VREFB5BN0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	M18	DQ2R			
3	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	L22 K17	DQ2R DQS2R	+		+
	VREFB5BN0 VREFB5BN0	10			DIFFIO_RX_R13p DIFFIO_TX_R14p	DIFFOUT_R13p DIFFOUT_R14p	M20	DQS2R			+
	VREFB5BN0	10			DIFFIO_IX_R14p	DIFFOUT_R13n	L17	DQSn2R			+
	VREFB5BN0	IO .			DIFFIO_RX_R13II	DIFFOUT_R14n	M21	DQ3H2R DQ2R			+
	VREFB5BN0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	L19	DQ2R			1
	VREFB5BN0	10			DIFFIO TX R16p	DIFFOUT_R16p	K21	DQ2R			+
	VREFB5BN0	10			DIFFIO RX R15n	DIFFOUT R15n	L18	DQ2R			
	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	K22				
		GND					F17				
	VREFB7AN0	10			DIFFIO_RX_T1p	DIFFOUT_T1p	K20			GND	GND
	VREFB7AN0	10			DIFFIO_TX_T2p	DIFFOUT_T2p	B16	DQ1T	DQ1T	T_DM_2	T_DM_2
	VREFB7AN0				DIFFIO_RX_T1n	DIFFOUT_T1n	K19			GND	GND
	VREFB7AN0				DIFFIO_TX_T2n	DIFFOUT_T2n	C16	DQ1T	DQ1T	T_DQ_23	T_DQ_23
	VREFB7AN0				DIFFIO_RX_T3p	DIFFOUT_T3p	D17	DQ1T	DQ1T	T_DQ_21	T_DQ_21
	VREFB7AN0 VREFB7AN0			+	DIFFIO_TX_T4p	DIFFOUT_T4p	G17 E16	DQ1T	DQ1T DQ1T	T_DQ_22	T_DQ_22
				+	DIFFIO_RX_T3n	DIFFOUT_T3n		DQ1T		T_DQ_20	T_DQ_20
	VREFB7AN0 VREFB7AN0				DIFFIO_TX_T4n DIFFIO_RX_T5p	DIFFOUT_T4n DIFFOUT_T5p	G16 G18	DQ1T DQS1T	DQ1T DQS1T	GND T DQS 2	GND T DQS 2
	VREFB7AN0				DIFFIO_RX_15p DIFFIO_TX_T6p	DIFFOUT_15p DIFFOUT_T6p	J19	בעטוו	ווטטוו	T_RESET#	T_BQS_2 T_RESET#
	VREFB7AN0			1	DIFFIO_RX_T5n	DIFFOUT_T5n	H18	DQSn1T	DQSn1T	T_DQS#_2	T_DQS#_2
	VREFB7AN0				DIFFIO_TX_T6n	DIFFOUT T6n	J18	DQ3ITT	DQ1T	T DQ 19	T_DQ3#_2
	VREFB7AN0				DIFFIO_RX_T7p	DIFFOUT_T7p	E15	DQ1T	DQ1T	T_DQ_17	T_DQ_17
	VREFB7AN0				DIFFIO_TX_T8p	DIFFOUT_T8p	A15	DQ1T	DQ1T	T_DQ_18	T_DQ_18
	VREFB7AN0	10			DIFFIO_RX_T7n	DIFFOUT_T7n	F15	DQ1T	DQ1T	T_DQ_16	T_DQ_16
	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	A14			GND	GND
	TITLE	10	CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	H16				
		10			DIFFIO_TX_T10p	DIFFOUT_T10p	J17	DQ2T	DQ1T	T_DM_1	T_DM_1
	TITLE	10	CLK11n		DIFFIO_RX_T9n	DIFFOUT_T9n	H15				
	VREFB7AN0				DIFFIO_TX_T10n	DIFFOUT_T10n	K16	DQ2T	DQ1T	T_DQ_15	T_DQ_15
		10			DIFFIO_RX_T11p	DIFFOUT_T11p	C15	DQ2T	DQ1T	T_DQ_13	T_DQ_13
	VREFB7AN0	10			DIFFIO_TX_T12p	DIFFOUT_T12p	G15	DQ2T	DQ1T	T_DQ_14	T_DQ_14
	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T11n DIFFIO_TX_T12n	DIFFOUT_T11n DIFFOUT_T12n	B15 F14	DQ2T DQ2T	DQ1T DQ1T	T_DQ_12 T_CKE_0	T_DQ_12 T_CKE_0
	VREFB7AN0	10			DIFFIO_IX_I12n	DIFFOUT_T12h DIFFOUT_T13p	H14	DQS2T	DQ1T	T_DQS_1	T_DQS_1
	VREFB7AN0	10		+	DIFFIO_RX_T13p	DIFFOUT_T14p	B13	DQ321	DQTI	T CKE 1	T_CKE_1
	VREFB7AN0				DIFFIO_RX_T13n	DIFFOUT_T13n	J13	DQSn2T	DQ1T	T DQS# 1	T DQS# 1
	VREFB7AN0				DIFFIO_TX_T14n	DIFFOUT_T14n	A13	DQ2T	DQ1T	T_DQ_11	T_DQ_11
	VREFB7AN0				DIFFIO RX T15p	DIFFOUT_T15p	E14	DQ2T	DQ1T	T DQ 9	T DQ 9
	VREFB7AN0				DIFFIO_TX_T16p	DIFFOUT_T16p	J11	DQ2T	DQ1T	T_DQ_10	T_DQ_10
	VREFB7AN0	10			DIFFIO_RX_T15n	DIFFOUT_T15n	F13	DQ2T	DQ1T	T_DQ_8	T_DQ_8
	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	H10			GND	GND
	VREFB7AN0		CLK10p		DIFFIO_RX_T17p	DIFFOUT_T17p	H13				
	VREFB7AN0				DIFFIO_TX_T18p	DIFFOUT_T18p	G11	DQ3T		T_DM_0	T_DM_0
	VREFB7AN0		CLK10n		DIFFIO_RX_T17n	DIFFOUT_T17n	G13				
	VREFB7AN0			1	DIFFIO_TX_T18n	DIFFOUT_T18n	F12	DQ3T	1	T_DQ_7	T_DQ_7
	VREFB7AN0			1	DIFFIO_RX_T19p	DIFFOUT_T19p	D13	DQ3T	+	T_DQ_5	T_DQ_5
	VREFB7AN0				DIFFIO_TX_T20p	DIFFOUT_T20p	B12	DQ3T	+	T_DQ_6	T_DQ_6
	VREFB7AN0 VREFB7AN0	10		+	DIFFIO_RX_T19n DIFFIO_TX_T20n	DIFFOUT_T19n DIFFOUT_T20n	C13 A12	DQ3T DQ3T	-	T_DQ_4 T_ODT_1	T_DQ_4 T_ODT_1
	VREFB7AN0 VREFB7AN0	10			DIFFIO_IX_120n DIFFIO_RX_T21p	DIFFOUT_T21p	H11	DQ31	+	T_DQS_0	T_DQS_0
	VREFB7AN0	IO IO			DIFFIO_RX_121p DIFFIO_TX_T22p	DIFFOUT_T22p	L8	DQ001	+	T_ODT_0	T_ODT_0
	VREFB7AN0	10		1	DIFFIO_TX_T22p	DIFFOUT_T21n	G12	DQSn3T	+	T_DQS#_0	T_DQS#_0
	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	K9	DQ3T	1	T_DQ_3	T_DQ_3
	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	D12	DQ3T		T_DQ_1	T_DQ_1
	VREFB7AN0	IO		<u> </u>	DIFFIO_TX_T24p	DIFFOUT_T24p	C11	DQ3T		T_DQ_2	T_DQ_2
	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	E12	DQ3T		T_DQ_0	T_DQ_0
	VREFB7AN0	10	RZQ_2		DIFFIO_TX_T24n	DIFFOUT_T24n	B11				
	VREFB8AN0	10	CLK9p		DIFFIO_RX_T25p	DIFFOUT_T25p	G10	1			
	VREFB8AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	L7	DQ4T		T_A_0	T_CA_0
		10	CLK9n		DIFFIO_RX_T25n	DIFFOUT_T25n	F10	DO 17			
		10		1	DIFFIO_TX_T26n	DIFFOUT_T26n	K7	DQ4T	+	T_A_1	T_CA_1
	VREFB8ANO	10	EDIT TI CIKOLTA EDIT TI CIKOLTA EDIT TI SO		DIFFIO_RX_T27p	DIFFOUT_T27p	J7	DQ4T	+	T_A_4	T_CA_4
		10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p DIFFIO_RX_T27n	DIFFOUT_T28p DIFFOUT_T27n	H8 J8	DQ4T DQ4T	+	T_A_2 T_A_5	T_CA_2 T_CA_5
	VREFB8AN0 VREFB8AN0		FPLL TL CLKOUT1,FPLL TL CLKOUTn	+	DIFFIO_RX_12/n DIFFIO_TX_T28n	DIFFOUT_T28n	J8 G8	DQ4T	+	T_A_5	T_CA_5
	VREFB8AN0 VREFB8AN0		FEE_IE_GEROUTI,FFEE_IE_GEROUTI		DIFFIO_IX_I28n DIFFIO_RX_T29p	DIFFOUT_T29p	J9	DQ41 DQS4T	+	T_CK	T_CK
	VREFB8AN0		 	+	DIFFIO_RX_129p	DIFFOUT_T30p	A10	DQ041	-	T A 6	T CA 6

Pin List F23



			louteral Foundation(s)	T 1							Note (1	
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	
8A	VREFB8AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	H9	DQSn4T		T_CK#	T_CK#	
BA	VREFB8AN0				DIFFIO_TX_T30n	DIFFOUT_T30n	A9	DQ4T		T_A_7	T_CA_7	
iA.	VREFB8AN0				DIFFIO_RX_T31p	DIFFOUT_T31p	B10	DQ4T		T_BA_1		
iA.	VREFB8AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	A5	DQ4T		T_BA_0		
BA	VREFB8AN0	10			DIFFIO_RX_T31n	DIFFOUT_T31n	C9	DQ4T		T_BA_2		
BA		10			DIFFIO_TX_T32n	DIFFOUT_T32n	B5			GND	GND	
RA	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T33p	DIFFOUT_T33p	E10					
IA.	VREFB8AN0	IO.	021109,1122_12_139		DIFFIO_TX_T34p	DIFFOUT_T34p	B6	DQ5T		T_CAS#		
iA.	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T33n	DIFFOUT_T33n	F9	5401		1_0/10//		
RA.	VREFB8AN0	10	OERON, IT EE_TE_I BIT		DIFFIO_TX_T34n	DIFFOUT_T34n	B7	DQ5T		T_RAS#		
RA	VREFB8AN0	10			DIFFIO RX T35p	DIFFOUT T35p	A8	DQ5T		T A 8	T CA 8	
DA	VREFB8AN0	10			DIFFIO_TX_T36p	DIFFOUT_T36p	C6	DQ5T		T_A_10	I_CA_6	
A	VREFB8AN0	10			DIFFIO_TX_T35p	DIFFOUT_T35n	A7	DQ5T		T_A_10	T CA 9	
DA .	VREFB8AN0	10			DIFFIO_RX_135II	DIFFOUT T36n	D6	DQ5T		T A 11	I_CA_9	
iA .												
BA	VREFB8AN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	E9	DQS5T		T_CS#_0	T_CS#_0	
iA .		IO			DIFFIO_TX_T38p	DIFFOUT_T38p	D7			T_A_12		
A		10			DIFFIO_RX_T37n	DIFFOUT_T37n	D9	DQSn5T		T_CS#_1	T_CS#_1	
A	VREFB8AN0				DIFFIO_TX_T38n	DIFFOUT_T38n	C8	DQ5T		T_A_13		
A	VREFB8AN0				DIFFIO_RX_T39p	DIFFOUT_T39p	G6	DQ5T	1	T_A_14		
A	VREFB8AN0				DIFFIO_TX_T40p	DIFFOUT_T40p	F7	DQ5T		T_WE#		
ıΑ	VREFB8AN0				DIFFIO_RX_T39n	DIFFOUT_T39n	H6	DQ5T		T_A_15		
iΑ	VREFB8AN0				DIFFIO_TX_T40n	DIFFOUT_T40n	E7			GND	GND	
9A		MSEL0		MSEL0			L6					
IA.		CONF_DONE		CONF_DONE			K6					
IA		MSEL1		MSEL1			J6					
A		nSTATUS		nSTATUS			H5					
)A		nCE		nCE			G5					
A		MSEL2		MSEL2			A2					
Α		MSEL3		MSEL3			E5					
A .		nCONFIG		nCONFIG			A4					
Α		MSEL4		MSEL4			F3					
A		GND					C5					
		GND					P2					
		GND					AB19					
		GND					AB14					
		GND					AB9					
		GND					AB2					
		GND					AB1					
		GND					AA11					
		GND					AA6					
		GND					AA4					
		GND					AA3					
		GND					Y18					
		GND					Y5					
		GND					Y2					
	İ	GND			İ		Y1					
	1	GND		1	İ		W4				1	
	1	GND		1	†	†	W3	1	1	1	1	
	l	GND		<u> </u>	<u> </u>	†	V22	1	1	1	†	
	t	GND	 	†	t	+	V22 V17	+	+	+	+	
	1	GND		†	t	+	V17			1	+	
	1			 	—	+		+	+	+	+	
	 	GND		 			V7	-	+	-	+	
	 	GND		 	 	+	V4	+	+	+	+	
	1	GND	ļ	!	-	+	V2	+	4	+	+	
	ļ	GND	ļ			+	V1	-			-	
	ļ	GND		ļ	Ļ	1	U9				 	
		GND					U5					
		GND					U4					
		GND					U3		1			
		GND					T21					
		GND				I -	T16					
		GND					T2					
	l e	GND		İ	1		T1					
	1	GND		1	1		R13					
	t	GND	 	†	t	+	R3	+	+	+	+	
	1	GND	1	 	t	+	P10	+	+	+	1	
	1			+	 	+		+	+	+	+	
	1	GND		 	 	+	P4	1	+	+	+	
	1	GND	ļ	!	-	+	P1	+	4	+	+	
	ļ	GND	ļ			+	N22	-				
	ļ	GND		ļ	Ļ	1	N17				 	
		GND	T. Control of the Con	1	1	1	N15	1	1		1	





							Note (1)				
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					N13				
		GND					N11				
		GND					N7				
		GND					N5				
		GND					N3				
		GND					M14				
	-	GND			-		M12	-			
		GND GND					M10 M4				+
											+
		GND GND					M2 M1				+
	+	GND			+		L21				+
	+	GND			+		L15				+
	+	GND			<u> </u>		L13	-			+
	+	GND			<u> </u>		L13	-			+
		GND		+			L5				+
		GND		+			L3				+
	1	GND					K14				1
		GND					K12				+
	1	GND		1			K10		†		+
	1	GND			1		K8	1	İ	İ	+
	1	GND					K4				1
	İ	GND		1	İ		K2	İ	Ì	İ	1
	1	GND					K1		1		1
		GND					J20				1
		GND					J15				1
		GND					J5				1
		GND					J3				
		GND					H22				
		GND					H12				
		GND					H7				
		GND					H4				
		GND					H3				
		GND					H2				
		GND					H1				
		GND					G19				
		GND					G9				
		GND					G4				
		GND					G3				
		GND					F16				
		GND					F6				
		GND					F5				
		GND					F2				
	-	GND			-		F1	-			
		GND GND					E13 E4				+
		GND					E3				+
	 	GND		+	 		D20	 	-	+	+
	+	GND		+	 		D20 D10	 	+	1	+
	†	GND		+	 		D10	 	<u> </u>	<u> </u>	+
	+	GND		+	 		D5 D2	 	+	1	+
	†	GND		+	 		D2 D1	 	<u> </u>	<u> </u>	+
	1	GND		+			C17				+
	 	GND		1	 		C17	 		1	+
	†	GND		+	 	<u> </u>	C3	 			+
	1	GND		1	†		B14	†	1	1	†
	1	GND			1		B9	1	İ	İ	1
	1	GND		1			B2		†		+
	1	GND			1		B1	1	İ	İ	1
	1	GND					A21				1
		GND					A11		1		1
	1	VCC					N4				1
		VCC					P15		1		1
		VCC					P13				1
		VCC					P11		1		1
		VCC					P3				1
		VCC					N14				1
	1	VCC					N12		1		1
		VCC					N10				1
		VCC					M15				
		VCC					M13				





											Note	
ank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	
		VCC					M11					
		VCC					L16					
		VCC					L14				_	
		VCC VCC					L12 L10				+	
		VCC					L10				+	
		VCC					K15				+	
		VCC					K13				+	
		VCC					K11				1	
		VCC					K5					
		VCC					K3					
		VCC					J16					
		vcc					J14				_	
		VCC VCC					J12 J10					
		VCC					J4				+	
		DNU					B3			+	+	
		DNU					B4				+	
		DNU					E17				1	
		DNU					L9					
		VCCPGM					V8					
		VCCPGM			ļ		R19		ļ	ļ		
		VCCPGM					F8					
		VCCBAT			 		A3			+	+	
		VCCIO2A VCCIO2A		-	-		D4 Y4		-	 	+	
		VCCIO2A VCCIO2A					R1			+	+	
		VCCIO2A VCCIO2A					J1			+	+	
		VCCIO3A					T6				+	
		VCCIO3A					Y8				1	
		VCCIO3B					T11				+	
		VCCIO3B					Y13				1	
		VCCIO3B					W10					
		VCCIO3B					R8					
		VCCIO4A					U19					
		VCCIO4A					AA21					
		VCCIO4A					AA16					
		VCCIO4A VCCIO4A					W20 W15					
		VCCIO4A VCCIO4A					W15 U14			+	+	
		VCCIO5A					P20				+	
		VCCIO5A VCCIO5A					R18				+	
		VCCIO5B					M19				1	
		VCCIO5B					K18				+	
		VCCIO7A					A16				1	
		VCCIO7A					H17					
		VCCIO7A					G14					
		VCCIO7A					F21			ļ		
		VCCIO7A					F11					
	ļ	VCCIO7A			-		E18		ļ	+	+	
	 	VCCIO7A VCCIO7A	<u> </u>	1	 	 	D15		1	+	+	
	-	VCCIO7A VCCIO7A		 	+		C22 C12			+	+	
	 	VCCIO7A VCCIO7A		1	 	<u> </u>	B19		1	†	+	
		VCCIO7A VCCIO8A		<u> </u>			A6			+	+	
	1	VCCIOSA VCCIOSA		İ	1		G7			1	1	
		VCCIO8A		İ	1		E8			1	1	
		VCCIO8A					C7				1	
		VCCPD1A2A					E1					
		VCCPD1A2A					R2			ļ		
		VCCPD1A2A					J2			1		
		VCCPD3A					W6					
		VCCPD3B4A			1		W17			1	+	
	 	VCCPD3B4A		<u> </u>	 		W14			+	+	
		VCCPD3B4A VCCPD3B4A		1	_	-	W12		-	 	+	
	-	VCCPD3B4A VCCPD5A		 	+		W11 P21			+	+	
	-	VCCPD5B		 	+		N18			+	+	
		VOOR DOD		+		ļ	INTO		 		+	
		IVCCPD5B					IM17					
		VCCPD5B VCCPD7A8A					M17 D16				+	



Pin Information for the Cyclone® V 5CEFA2 Device Version 1.3 Note (1)

Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number					Channel					Assignment for DDR3/DDR2 (2)	Assignment for LPDDR2
		VCCPD7A8A					D14				
		VCCPD7A8A					D8				
		VCCPD7A8A					C10				
2A	VREFB2AN0	VREFB2AN0					W1				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0					R20				
5B	VREFB5BN0	VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					Y6				
		NC					V11				
		NC					J22				
		NC					J21				
<u> </u>		NC				+	H21	ļ	ļ	ļ	ļ
		NC NC			1	 	H20	ļ	ļ	ļ	
 		NC NC		-		+	G22	 	 	 	-
		NC NO			1	 	G21	ļ	ļ	1	1
		NC NC					G20				
		NC NC					F22				
		NC NO					F20				
		NC NC					F19				
		NC NC					F18				
		NC NC					E22 E21				
		NC NC					E20				
-		NC NC					E19				
		NC					D22				
		NC					D21				
		NC NC					D19				
		NC					C21				
		NC					C20				
		NC NC					C19				
		NC NC					C18				
		NC NC					B22				
		NC NC					B21				
		NC					B20				
		NC					B18				
		NC					B17		1		1
		NC					A22				
		NC					A20				
		NC					A19				
		NC					A18				
		NC					A17				
		RREF_TL					A1				
		VCCA_FPLL					M3				
		VCCA_FPLL					T3				
		VCCA_FPLL					T5				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					H19				
		VCC_AUX					E6				
		VCC_AUX					D11				
		VCC_AUX					D18				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX				1	W7				

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CEFA2 Device Version 1.3

Version Number	Date	Changes Made
1.0	9/20/2012	Initial release.
1.1	10/5/2012	Removed nPERST* pins because Cyclone V E devices do not support PCIe interface.
1.2	1/3/2013	Removed F256 and U324 pin lists.
1.3	6/12/2013	 - Added M383 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added note to the "HMC Pin Assignment for DDR3/DDR2" column.
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