Unspecified Transition Faults: A Transition Fault Model for At-Speed Fault Simulation and Test Generation

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***Abstract*—A transition fault model is described, which is easy to simulate under test sequences that are applied at-speed, and provides a target for the generation of at-speed test sequences. At-speed test application allows a circuit to be tested under its normal-operation conditions. However, fault simulation and test generation for standard transition faults become significantly more complex due to the need to handle faulty signal transitions that span multiple clock cycles. As a result, each transition fault needs to be considered multiple times, with multiple sizes of the extra delay on the faulty line. The proposed fault model alleviates this shortcoming by introducing unspecified values into the faulty circuit when fault effects may occur, thus allowing faults of all possible sizes to be encompassed in a single fault. Fault detection potentially occurs when an unspecified value reaches a primary output. "Pessimistic," "optimistic," and "random" versions of the fault model and corresponding fault coverages are defined. If a single fault coverage is to be computed, the pessimistic one provides the lowest fault coverage. By using the optimistic or random version, it is possible to obtain a range of possible fault coverages that is analogous to the range of sizes of transition faults. For certain applications, it is also possible to include more than one version of every fault in a single set of target faults and to compute a single fault coverage. Experimental results of fault simulation and test generation are presented to demonstrate the behavior of the model and to compare it with other fault models.**

***Index Terms*—Delay faults, fault simulation, synchronous sequential circuits, test generation, transition faults.**

I. Introduction

APPLICATION of tests for delay faults in synchronous sequential circuits can be done in one of several ways. Scan can be used to apply two-pattern tests that start and end with scan operations [1]–[3]. Tests can also be applied using only the functional mode of operation of the circuit. In this case, it is possible to use slow clock cycles for initialization and fault propagation and fast clock cycles for capturing fault effects [4]–[6]. Alternatively, a test sequence can be applied at-speed [7]–[10] using only fast clock cycles. At-speed test application has the advantage that the circuit is tested under its normal-operation conditions. It has been shown that certain defects will only be detected if tests are applied at-speed. In addition, as demonstrated in [11], test application that deviates from normal operation can cause faulty behavior that would not show up during normal operation, resulting in overtesting.

Transition faults are used for their simplicity in modeling spot defects that affect delays at inputs or outputs of gates. Under scan-based tests, the transition faults are associated with an extra delay that is large enough to cause the delay of any path through the fault site to exceed the clock period. Beyond this assumption, the specific delay size is not important. When at-speed tests are used, a faulty line must be considered under multiple consecutive fast clock cycles. In this case, it becomes necessary to explicitly consider the fault sizes measured in numbers of clock cycles in order to determine the value of a faulty line in consecutive fast clock cycles [9]. Thus, it is necessary to consider each transition fault site multiple times, associating with it a delay of size one, two, ... cycles. This increases the complexity of fault simulation and test generation.

In this paper, we propose a new delay fault model similar to the transition fault model for use with at-speed tests. The model allows the simulation of a given transition fault site, with a given delayed signal transition, only once to determine whether the transition fault on the site is detected by a given test sequence, and it also allows test generation similar to the generation of n-detection test sequences for stuck-at faults. The model has the following main features.

1) The fault-simulation process for the proposed model is similar in complexity to fault simulation of stuck-at faults. Each transition fault site is considered twice: once for a slow-to-rise fault and once for a slow-to-fall fault.
2) The conditions for fault activation are simple to compute. When a fault is activated, the value assigned to the fault site in the faulty circuit is unspecified. Whereas fault effects represented as 0/1 or 1/0 may cancel each other, injecting an additional unspecified value can only increase the number of unspecified values in the circuit. Thus, a conservative approach to fault activation will result in a conservative estimate of fault coverage, and a single fault-coverage number is sufficient for the evaluation of a given test set or as a guide for test generation.

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In Section II, we introduce the proposed transition fault model. In Section III, we present the results of fault simulation of test sequences generated for stuck-at faults. The results demonstrate that the model behaves as intended in terms of fault coverage and numbers of detections of target faults. In Section IV, we discuss test generation for the proposed fault model.

We assume that at most one transition fault (slow-to-rise or slow-to-fall) will occur on each line. The model can be extended to deal with the case where both faults may be present on a line simultaneously by introducing unspecified values for both types of transitions when they occur.

II. Delay Fault Model

In this section, we describe the proposed delay fault model. The model is similar to the transition fault model, but it is particularly suitable for at-speed fault simulation and test generation. We refer to the faults of the new fault model as unspecified transition faults. We define three versions of the proposed fault model: one that can be viewed as pessimistic, one that can be viewed as optimistic, and one that can be viewed as a random combination of the first two. When it is important to distinguish between the three versions of a fault, we refer to the faults as pessimistic unspecified transition faults, optimistic unspecified transition faults, and random unspecified transition faults, respectively.

Similar to standard transition faults, we associate an unspecified transition fault with every line g and signal transition $v \rightarrow v'$, for $v \in \{0, 1\}$. The fault associated with g and $v \rightarrow v'$ is denoted by $g : v \rightarrow v'$. Similar to the standard transition fault, the unspecified transition fault $g : v \rightarrow v'$ is activated at time unit $u + 1$ if $g = v$ at time unit u and $g = v'$ at time unit $u + 1$. However, when the fault is activated, we set the value of g in the faulty circuit to the unspecified value x instead of setting g to the value v. The unspecified value on g can then be propagated to the next time units until it eventually disappears. For every time unit where an unspecified value is propagated to a primary output, we say that the fault is detected once. The detection is viewed as a potential detection to accommodate the following effects.

1) The duration of the fault is unknown, and different durations may result in different values. As a result, a fault of a certain duration may be detected, whereas a fault of a different duration may not be detected by a given test sequence [9].
2) Unmodeled delay effects may be pattern-dependent, and they may cause the effects of a transition fault not to appear at observable outputs under certain conditions that a test may create [12]–[16].

For an unspecified transition fault, the higher the number of potential detections, the more likely it is that a delay defect on the fault site (or a standard transition fault on the same line) will actually be detected. Therefore, the fault simulation and test generation procedures should consider the numbers of times the faults are detected.

We illustrate the model and the fault-simulation process for it by using the circuit shown in Fig. 1. The input sequence

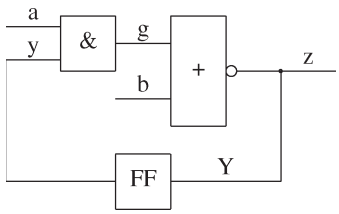

Fig. 1. Example circuit.

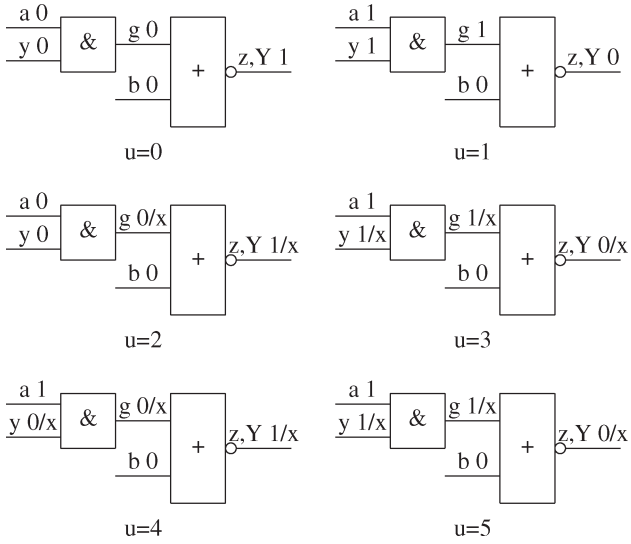

Fig. 2. Example circuit with a fault.

under consideration is 00 10 00 10 10 10. The circuit is assumed to be initialized to state 0 before the application of the input sequence. The fault under consideration is $g : 1 \rightarrow 0$. The values throughout the fault-free and faulty circuits are shown in Fig. 2. Y and z are combined in Fig. 2 since they assume the same values at all the time units under the fault $g : 1 \rightarrow 0$. Values are shown in Fig. 2 in the form of fault-free/faulty values. The following points should be noted.

1) Since $g = 1$ at time unit 1 and $g = 0$ at time unit 2, the fault is activated at time unit 2. This results in the value $g = 0/x$ at time unit 2.
2) The fault effect is propagated to the output z at time unit 2. Thus, the fault is detected for the first time.
3) At time unit 3, the fault effect continues to propagate. The value $1/x$ on g is a result of the value $1/x$ on y at time unit 3. The fault is detected for the second time.
4) If the fault effect had disappeared by time unit 3 and the fault-free values had been obtained at time units 3 and 4, the fault would have been injected again at time unit 4 (this would have been based on $g = 1$ at time unit 3 and $g = 0$ at time unit 4). The unspecified value on g at time unit 4 accommodates this case.
5) In this example, for every time unit u, where the fault is potentially detected since an x is propagated to the output, there is a transition on the output in the fault-free circuit. The transition occurs between time units $u - 1$ and u. In general, an x value can also be propagated to an output at time unit u when the fault-free value of the output is the same at time units $u - 1$ and u.

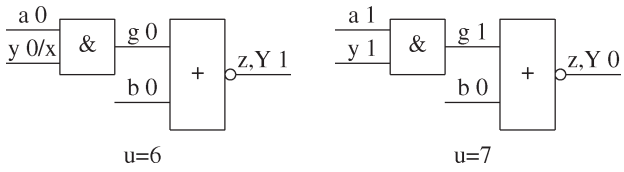

Fig. 3. Pessimistic fault activation.

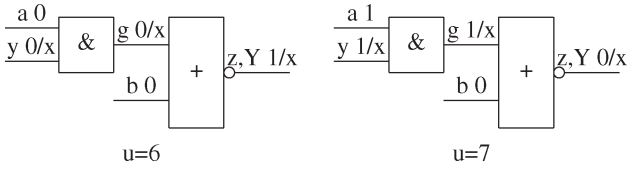

Fig. 4. Optimistic fault activation.

A pessimistic unspecified transition fault requires specified values in two consecutive time units to determine that a fault is activated. An optimistic unspecified transition fault may be activated even if the value in the first of two consecutive time units is unspecified. To demonstrate the difference between the pessimistic and optimistic fault-activation conditions, we add two input vectors (00 and 10) to the sequence of Fig. 2. Under the pessimistic view, fault simulation continues as shown in Fig. 3. In this case, the values $g = 1/x$ at time unit 5 and $g = 0$ at time unit 6 do not cause the fault to be activated again at time unit 6. This is a result of the fact that under a pessimistic view, $g = x$ in the faulty circuit at time unit 5 will not support the fault activation at time unit 6.

Under the optimistic view, fault simulation continues as shown in Fig. 4. In this case, the values $g = 1/x$ at time unit 5 and $g = 0$ at time unit 6 cause the fault to be activated again at time unit 6. This is a result of the fact that under an optimistic view, $g = x$ in the faulty circuit at time unit 5 will support the fault activation at time unit 6. This is independent of the fault-free value and is based only on the fact that the unspecified value in the faulty circuit may be zero or one.

Considering the pessimistic and optimistic fault activations, the following point is important. Unspecified values have the property that injecting a new unspecified value cannot mask an unspecified value injected earlier. A new unspecified value can only increase the likelihood that an unspecified value will be propagated to an output. Under the optimistic view, we introduce more unspecified values into the faulty circuit than under the pessimistic view. Therefore, the optimistic view will have higher numbers of potential fault detections than the pessimistic one.

It should also be noted that the use of unspecified values to mark fault activation and propagation has the following shortcoming. The simulation of unspecified values using three-value logic has an inherent loss of accuracy that may result in an output being unspecified even though more accurate simulation would indicate that the output can only be zero or one. However, this effect is small, and it is tolerated in most of the fault-simulation and test-generation procedures for synchronous sequential circuits that use three-value logic.

Next, we show another example that will demonstrate the relationship between the two versions of an unspecified transition fault and the sizes of the standard transition faults. We consider the circuit of Fig. 1 under the test sequence 00 10 00 00 00 00. The fault under consideration is the same as in Fig. 2 ($g : 1 \rightarrow 0$). The values throughout the circuit for the fault-free case and for the pessimistic unspecified transition fault are shown in Fig. 5. The values for the fault-free case and for the optimistic unspecified transition fault are shown in Fig. 6. Considering the faulty circuit, in this case, the computed value of g, $g = 0$, at time units $u = 3, 4,$ and 5 is changed to x due to the possibility of activating the fault when the x value in the previous time unit is actually one (the computed value of a faulty line at time unit u is the value computed based on the present state and the primary input vector at time unit u before the fault is injected at time unit u).

Fig. 5 is analogous to the case where a standard transition fault of a single clock cycle is present in the circuit. The effects of such a fault disappear after one clock cycle, similar to the situation in Fig. 5. Fig. 6 is analogous to the case where a standard transition fault of a large number of clock cycles

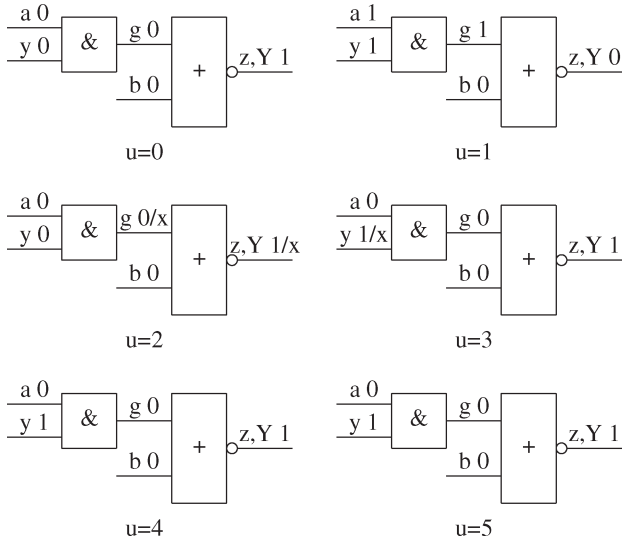

Fig. 5. Example circuit under the pessimistic view.

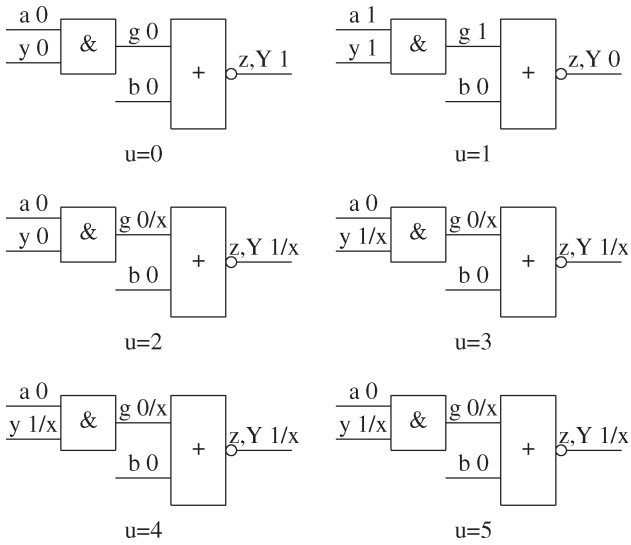

Fig. 6. Example circuit under the optimistic view.

is present in the circuit. The effects of such a fault stay in the circuit as long as the computed value of the faulty line g is zero, similar to the situation in Fig. 6. It is important to note that due to the fact that adding unspecified values only increases the fault coverage and the numbers of detections of the unspecified transition faults, a pessimistic unspecified transition fault is suitable on its own to model the effects of the standard transition faults of all sizes. However, the use of optimistic transition faults will provide additional information in the form of a higher fault coverage and higher numbers of detections that are likely to be closer to the numbers for the standard transition faults of higher sizes.

Next, we summarize the fault-activation conditions for a fault $g : v \rightarrow v'$ at a time unit $u > 0$. The random activation conditions are explained in more detail in the following.

Let S be the state of the faulty circuit at time unit u, and let A be the primary input vector. Then, compute the values throughout the circuit under S and A.

Pessimistic Fault Activation: If the value of line g at time unit $u-1$ is v and the computed value of line g at time unit u is v', assign an unspecified value to line g and find the implications of this value.

Optimistic Fault Activation: If the value of line g at time unit $u-1$ is v, or if g is unspecified at time unit $u-1$, and the computed value of line g at time unit u is v', assign an unspecified value to line g and find the implications of this value.

Random Fault Activation:

1) If the value of line g at time unit $u-1$ is v and the computed value of line g at time unit u is v', assign an unspecified value to line g and find the implications of this value.
2) If g is unspecified at time unit $u-1$ and the computed value of line g at time unit u is v', with a probability p, assign an unspecified value to line g and find the implications of this value.

The difference between the pessimistic and optimistic fault-activation conditions for a fault $g : v \rightarrow v'$ is seen when the fault site g assumes the value x at time unit $u-1$ and the value v' at time unit u. In this case, the pessimistic view leaves $g = v'$ at time unit u, whereas the optimistic view sets $g = x$ at time unit u. Under the same situation, the random fault-activation condition decides randomly whether to leave $g = v'$ at time unit u or set $g = x$ at time unit u. This is analogous to deciding on the length of a transition fault randomly during the fault-simulation process. For illustration, we consider the example circuit with the test sequence shown in Fig. 6. The values at time unit $u = 0$, 1, and 2 are the same under all three models. Under the random view, we may decide to set $g = x$ at time unit $u = 3$ but leave $g = 0$ at time unit 4. This would also cause g to remain zero at time unit 5.

In addition to providing a metric with values between the pessimistic and optimistic ones, the physical justification for the random unspecified transition fault model is that the actual delays in a circuit are pattern-dependent and that they may cause the effects of a transition fault to be different at different time units of a test sequence [12]–[16]. Without performing an accurate analysis of delays, the random transition fault model introduces pattern dependence into the unspecified transition fault model.

TABLE I
CIRCUIT PARAMETERS

circuit	flts	len
s208	416	105
s298	596	117
s344	688	57
s382	764	416
s386	772	121
s400	800	611
s420	840	108
s510	258	1020
s526	1052	1006
s641	1280	101
s820	1640	491
s953	267	1906
s1196	2392	238
s1423	2846	1024
s5378	10590	646
s35932	71864	150
b03	768	130
b04	2284	168
b09	678	269
b10	870	190
b11	1830	675

The probability p included in the random fault-activation conditions will determine how close the fault coverage will be to the pessimistic or optimistic ones. With $p = 0$, we obtain the pessimistic view, whereas with $p = 1$, we obtain the optimistic view. We use $p = 1/2$ in our experiments.

III. FAULT SIMULATION

We implemented a fault-simulation procedure for the unspecified transition fault model. The procedure simulates pessimistic, optimistic, and random unspecified transition faults. It simulates a fault until the fault is detected n times for a constant n. For comparison, we also perform an n-detection fault simulation of stuck-at faults. In this process, a stuck-at fault is considered detected at a time unit u if there exists an output with different specified fault-free and faulty values at time unit u. A fault is dropped from consideration after it is detected at n different time units. Experiments reported in [17] indicate that counting detections of a fault as different if they occur in different time units is as effective as using more complex definitions that require stricter conditions. For further comparison, we also simulated transition faults with an extra delay of c clock cycles, for $c = 1, 2, \ldots, 10$.

The test sequences that we simulated are compacted deterministic test sequences generated for stuck-at faults. In every case, the circuit is started from the all-zero state. This is done to eliminate the unspecified values that occur due to the initial state of the circuit. It is possible to accommodate an unspecified initial state by starting the simulation of unspecified transition faults only after the fault-free and faulty circuit states are specified and by ignoring fault activations and fault detections that occur earlier.

The results obtained using $n = 5$ are shown in Tables I–IV. In Table I, under column flts, we show the number of faults (the number of uncollapsed single stuck-at faults, which is equal to

TABLE II
RESULTS OF SIMULATION (FAULT COVERAGES)

	f.c.							
circuit	s.a.	p-xtr	r-xtr	o-xtr	1-tr	2-tr	5-tr	10-tr
s208	70.19	51.68	54.57	61.54	51.68	54.09	56.73	60.34
s298	89.60	69.97	79.53	89.09	69.97	76.68	85.74	88.42
s344	97.38	85.47	91.42	96.51	85.47	92.44	94.91	95.78
s382	96.60	74.08	81.41	96.73	73.43	79.58	82.33	85.47
s386	90.16	67.49	78.11	88.99	67.49	79.53	86.27	88.08
s400	95.38	72.38	79.00	94.75	72.38	77.25	80.38	83.38
s420	46.79	27.98	29.40	32.50	27.86	28.93	30.24	31.79
s510	100.00	85.39	94.71	100.00	85.39	94.41	98.73	99.61
s526	86.88	59.13	71.58	86.41	59.03	71.29	74.62	77.66
s641	88.12	75.16	78.75	82.11	75.16	79.69	81.80	82.11
s820	96.34	74.51	87.01	96.34	74.33	84.94	94.70	96.10
s953	99.37	88.20	94.81	99.37	88.20	95.38	98.32	99.27
s1196	99.87	81.56	88.84	99.83	81.44	90.68	97.07	98.75
s1423	96.94	83.24	89.60	96.94	81.66	87.42	91.78	93.92
s5378	80.34	71.72	73.73	77.37	71.67	73.98	75.31	76.17
s35932	89.78	86.50	88.32	89.77	86.50	88.01	89.37	89.49
b03	74.22	54.17	60.16	63.67	54.17	60.94	62.89	63.28
b04	88.66	72.42	78.94	87.13	71.94	77.01	84.02	86.21
b09	84.81	63.72	67.99	83.33	64.31	68.44	72.71	79.65
b10	93.33	70.57	79.66	93.56	70.00	78.28	88.16	91.61
b11	92.40	75.68	84.21	91.91	75.57	79.73	88.31	90.16

TABLE III
RESULTS OF SIMULATION (AVERAGE NUMBERS OF DETECTIONS)

	ave			
circuit	s.a.	p-xtr	r-xtr	o-xtr
s208	2.32	1.47	1.67	2.09
s298	4.20	3.05	3.57	4.19
s344	4.69	3.99	4.28	4.64
s382	4.66	3.18	3.69	4.70
s386	3.89	2.73	3.22	3.88
s400	4.67	3.18	3.66	4.64
s420	1.76	0.91	1.00	1.24
s510	4.95	4.17	4.61	4.96
s526	4.29	2.71	3.43	4.27
s641	4.07	3.32	3.55	3.80
s820	4.44	3.43	3.98	4.54
s953	4.56	3.72	4.15	4.57
s1196	3.82	2.54	2.96	3.81
s1423	4.34	4.05	4.37	4.76
s5378	3.81	3.37	3.49	3.69
s35932	4.48	4.29	4.39	4.48
b03	3.42	2.38	2.71	2.99
b04	4.13	2.66	3.28	4.13
b09	3.92	2.92	3.10	3.90
b10	4.38	3.21	3.64	4.41
b11	4.57	3.71	4.13	4.56

the number of transition faults). Under column len, we show the length of the test sequence simulated.

In Table II, we show the fault coverages obtained (the fault coverage is the number of faults detected at least once as a percentage of the total number of faults). The fault coverage of single stuck-at faults is shown under column s.a. The pessimistic, random, and optimistic unspecified transition fault coverages are shown under columns $p-$ xtr, $r-$ xtr, and $o-$ xtr, respectively. The fault coverage of standard transition faults of size c clock cycles is shown under column $c-$ tr, for $c = 1$, 2, 5, and 10.

In Table III, under column ave, we show the average number of times that a fault is detected by the test sequence, considering stuck-at faults and pessimistic, random, and optimistic unspecified transition faults.

In Table IV, under column $d = d_0$, for $d_0 = 0, 1, \ldots, 5$, we show the number of faults detected d_0 times. We show the results for stuck-at faults in row s.a., for pessimistic unspecified transition faults in row $p-$ xtr, and for optimistic unspecified transition faults in row $o-$ xtr. We omit the results for random unspecified transition faults since they are bounded by the pessimistic and optimistic numbers.

In Tables I–IV, it can be seen that the coverage of the unspecified transition faults of any type is lower than the coverage of stuck-at faults and that the numbers of detections of the unspecified transition faults are also lower. The pessimistic unspecified transition fault coverage is close to that obtained for the standard transition faults with an extra delay of a single clock cycle. The optimistic unspecified transition fault coverage is higher than the pessimistic one and closer to the stuck-at fault coverage. As expected, the random unspecified transition fault coverage is in-between the pessimistic and optimistic ones.

Overall, these results indicate that the unspecified transition fault model behaves as expected and is similar to other delay fault models. Using the fault coverages of the pessimistic and optimistic unspecified transition faults, it is possible to obtain a range of fault coverages that provides an indication of the fault coverages that would be obtained for the transition faults of c clock cycles, for $c = 1, 2, \ldots, 10, \ldots$.

For the purpose of test generation, it is also interesting to see the correlation between the number of detections of an unspecified transition fault $g : v \rightarrow v'$ and the number of detections of the related stuck-at fault g stuck-at v. We say that the faults are related since the detection of both faults occurs when the fault changes the value of g from v' to a faulty value (a similar relationship exists between the standard transition faults and the stuck-at faults [18]). For example, we would like to know whether a high (low) number of detections for g stuck-at v implies a high (low) number of detections for $g : v \rightarrow v'$. If the correlation between the numbers of detections is high, then test generation for unspecified transition faults

TABLE IV
RESULTS OF SIMULATION (NUMBERS OF DETECTIONS)

circuit	model	d=0	d=1	d=2	d=3	d=4	d=5
s208	s.a.	124	72	33	36	35	116
	p-xtr	201	74	41	14	17	69
	o-xtr	160	62	35	18	21	120
s298	s.a.	62	10	30	3	29	462
	p-xtr	179	32	26	21	22	316
	o-xtr	65	10	27	1	32	461
s344	s.a.	18	7	12	19	19	613
	p-xtr	100	18	17	16	39	498
	o-xtr	24	9	10	19	21	605
s382	s.a.	26	11	16	12	11	688
	p-xtr	198	61	30	18	34	423
	o-xtr	25	9	11	10	12	697
s386	s.a.	76	55	48	39	34	520
	p-xtr	251	69	56	16	22	358
	o-xtr	85	51	49	31	28	528
s400	s.a.	37	7	11	4	13	728
	p-xtr	221	39	41	23	23	453
	o-xtr	42	7	9	5	11	726
s420	s.a.	447	71	32	41	26	223
	p-xtr	605	83	19	8	6	119
	o-xtr	567	63	16	5	13	176
s510	s.a.	0	3	2	11	9	995
	p-xtr	149	5	1	29	17	819
	o-xtr	0	3	0	10	9	998
s526	s.a.	138	4	1	9	16	884
	p-xtr	430	11	51	19	20	521
	o-xtr	143	3	1	9	15	881
s641	s.a.	152	63	37	30	10	988
	p-xtr	318	71	46	55	27	763
	o-xtr	229	62	26	27	7	929
s820	s.a.	60	67	61	60	52	1340
	p-xtr	418	55	50	47	27	1043
	o-xtr	60	57	40	42	28	1413
s953	s.a.	12	72	92	78	55	1597
	p-xtr	225	159	125	120	71	1206
	o-xtr	12	73	90	77	50	1604
s1196	s.a.	3	275	368	202	196	1348
	p-xtr	441	466	409	225	137	714
	o-xtr	4	276	370	207	206	1329
s1423	s.a.	87	182	137	78	140	2222
	p-xtr	477	34	31	39	9	2256
	o-xtr	87	34	18	28	7	2672
s5378	s.a.	2082	291	206	164	101	7746
	p-xtr	2995	286	208	215	105	6781
	o-xtr	2396	239	161	189	81	7524
s35932	s.a.	7344	18	43	108	43	64308
	p-xtr	9704	379	183	198	146	61254
	o-xtr	7350	14	47	109	23	64321
b03	s.a.	198	9	35	31	21	474
	p-xtr	352	10	42	24	42	298
	o-xtr	279	6	31	12	9	431
b04	s.a.	259	76	68	69	49	1763
	p-xtr	630	191	279	230	126	828
	o-xtr	294	50	45	65	49	1781
b09	s.a.	103	34	20	9	2	510
	p-xtr	246	36	5	5	10	376
	o-xtr	113	26	22	2	10	505
b10	s.a.	58	25	43	10	0	734
	p-xtr	256	37	35	8	4	530
	o-xtr	56	22	43	8	0	741
b11	s.a.	139	7	13	5	7	1659
	p-xtr	445	8	24	5	13	1335
	o-xtr	148	4	13	2	8	1655

TABLE V
NUMBERS OF DETECTIONS FOR s298

n_{sa}	n_{p-xtr} 0	1	2	3	4	5
0	62	0	0	0	0	0
1	2	8	0	0	0	0
2	17	2	7	0	1	3
3	2	0	0	1	0	0
4	11	6	1	9	1	1
5	85	16	18	11	20	312

can be replaced with n-detection test generation for stuck-at faults.

In Table V, we show detailed information about the numbers of detections for s298. Similar results were obtained for other benchmark circuits. We consider only the pessimistic unspecified transition faults since they are harder to detect than the optimistic or random ones. For every pair (g, v), let $n_{p-\mathrm{xtr}}(g, v)$ be the number of times the pessimistic unspecified transition fault $g : v \rightarrow v'$ is detected, and let $n_{\mathrm{sa}}(g, v)$ be the number of times the stuck-at fault g stuck-at v is detected. The pair (g, v) contributes one to the entry in row $n_{\mathrm{sa}}(g, v)$ and column $n_{p-\mathrm{xtr}}(g, v)$ of Table V. Thus, the entry in row i and column j of Table V provides the number of pairs (g, v) such that $n_{\mathrm{sa}}(g, v) = i$ and $n_{p-\mathrm{xtr}}(g, v) = j$. We continue to use $n = 5$ during fault simulation; therefore, $n_{\mathrm{sa}}(g, v) \leq 5$ and $n_{p-\mathrm{xtr}}(g, v) \leq 5$ for every (g, v).

From Table V, it can be seen that there are cases where $n_{\mathrm{sa}}(g, v) < n$ and $n_{p-\mathrm{xtr}}(g, v) < n$. For example, there are 62 cases where both the stuck-at fault and the corresponding unspecified transition fault are not detected. In these cases, n-detection test generation for stuck-at faults may also help increase the numbers of detections of unspecified transition faults. However, there are also cases where $n_{\mathrm{sa}}(g, v) = n$ and $n_{p-\mathrm{xtr}}(g, v) < n$. For example, there are 85 cases where the stuck-at fault is detected five times, whereas the corresponding unspecified transition fault is not detected. In these cases, it may be necessary to increase the numbers of detections of stuck-at faults that are already detected n times in order to potentially increase the numbers of detections of the related pessimistic unspecified transition faults. We investigate a variation of an n-detection test-generation procedure for stuck-at faults as a way of increasing the numbers of detections of unspecified transition faults in the next section.

IV. TEST GENERATION

In this section, we describe a test-generation procedure for unspecified transition faults. The procedure attempts to increase the numbers of detections of unspecified transition faults, which are detected fewer than n times by a given test sequence, for a constant n.

Based on the discussion of the previous section, we start from a test sequence T for stuck-at faults. We increase the numbers of detections of stuck-at faults by adding test subsequences to T in order to indirectly increase the numbers of detections of unspecified transition faults. We concentrate on the pessimistic unspecified transition faults since their numbers of detections are lower than those of the optimistic or random unspecified

transition faults. However, if a pessimistic unspecified transition fault cannot be detected, an optimistic or random version of the same fault can be considered instead. Test generation proceeds as follows.

For $d = 0, 1, \ldots, n-1$, we consider every pessimistic unspecified transition fault $g : v \rightarrow v'$ such that $n_{\rm sa}(g, v) > 0$ and $n_{p-{\rm xtr}}(g, v) = d$. The reason for requiring $n_{\rm sa}(g, v) > 0$ is that we will use a subsequence that detects the stuck-at fault g stuck-at v in order to generate a subsequence that potentially detects the related pessimistic unspecified transition fault $g : v \rightarrow v'$.

For every value of d, we consider all the faults with $n_{\rm sa}(g, v) > 0$ and $n_{p-{\rm xtr}}(g, v) = d$. For $d > 0$, we then consider all the faults with $n_{\rm sa}(g, v) > 0$ and $n_{p-{\rm xtr}}(g, v) = d$ again. This is done in case a fault with $n_{p-{\rm xtr}}(g, v) = d - 1$ is accidentally detected, and a test subsequence for it may be generated if it is targeted again directly.

When we consider $g : v \rightarrow v'$, we obtain a new test subsequence $\hat{T}$ that detects g stuck-at v and concatenate it to T. The new test subsequence $\hat{T}$ for g stuck-at v is obtained from T as follows.

We first simulate T under the fault g stuck-at v to find the final state P reached by the fault-free circuit and the final state P' reached by the faulty circuit. Our goal is to generate $\hat{T}$ such that it detects g stuck-at v starting from state P/P'. This is sufficient to ensure that $T\hat{T}$ will detect g stuck-at v an additional time.

To find $\hat{T}$, we simulate g stuck-at v under the test sequence T starting from state P/P'. If g stuck-at v is not detected by T, we do not consider it further. Otherwise, we find the smallest time unit u_e where g stuck-at v is detected by T. Denoting the subsequence of T that starts at time unit u_s and ends at time unit u_e by $T[u_s, u_e]$, we find in this step a subsequence $T[0, u_e]$ that detects g stuck-at v starting from state P/P'.

We then consider decreasing values of $u_s, u_s = u_e, u_{e-1}, \ldots, 0$. We simulate the subsequence $T[u_s, u_e]$ of T that starts at time unit u_s and ends at time unit u_e starting from state P/P'. We stop with the highest value of u_s such that $T[u_s, u_e]$ detects g stuck-at v. Since $T[u_s, u_e]$ detects g stuck-at v starting from state P/P', concatenating $T[u_s, u_e]$ to T is guaranteed to increase the number of detections of g stuck-at v. To ensure that different test subsequences are obtained when g stuck-at v is considered multiple times, even if the final state P/P' is the same, we add the following two steps.

Considering the time units of $T[u_s, u_e]$ in a random order, we attempt to omit each test vector from $T[u_s, u_e]$. When time unit u is considered, we omit the vector $T[u]$ at time unit u of $T[u_s, u_e]$. If g stuck-at v continues to be detected, we accept the omission. Otherwise, we restore $T[u]$ into $T[u_s, u_e]$.

After the vector omission step is complete, we randomly decide whether to try and change every bit b of $T[u_s, u_e]$. When bit b is considered, if the decision is to try and change it, we complement the bit and simulate g stuck-at v. If the fault is not detected, we complement the bit again to restore its initial value.

For illustration, we consider the test sequence of s27 shown in Table VI under column initial. We consider a stuck-at fault f that is detected once by T, whereas the related unspecified transition fault is not detected by T. We find the final states reached under T in the fault-free circuit and in the presence of f. By simulating T starting from these states, we find that f is detected by T at time unit $u_e = 8$. Considering $u_s = 8, 7, \ldots$, we find that $T[8, 8] = 0000$ does not detect f, $T[7, 8] = 0000\ 0000$ does not detect f, and so on until $T[4, 8] = 0100\ 1011\ 1001\ 0000\ 0000$ detects f. We set $\hat{T} = T[4, 8]$.

TABLE VI
TEST SEQUENCE FOR s27

u	$T[u]$ initial	$T[u]$ extended
0	0111	0111
1	1001	1001
2	0111	0111
3	1001	1001
4	0100	0100
5	1011	1011
6	1001	1001
7	0000	0000
8	0000	0000
9	1011	1011
10		1110
11		1111
12		0011
13		1000

We randomly order the time units of $\hat{T}$ as $\langle 3, 2, 0, 4, 1 \rangle$. We find that the vector 1001 at time unit 2 of $\hat{T}$ can be omitted, but the remaining vectors cannot be omitted. The resulting test subsequence is $\hat{T} = 0100\ 1011\ 0000\ 0000$.

We randomly decide to try and complement bits 0 and 2 at time unit 0 of $\hat{T}$, bits 1 and 2 at time unit 1 of $\hat{T}$, bits 1, 2, and 3 at time unit 2 of $\hat{T}$, and bits 0 and 1 at time unit 3 of $\hat{T}$. We find that bits 0 and 2 at time unit 0 of $\hat{T}$, bit 1 at time unit 1 of $\hat{T}$, bits 2 and 3 at time unit 2 of $\hat{T}$, and bit 0 at time unit 3 of $\hat{T}$ can be complemented. The resulting test subsequence is $\hat{T} = 1110\ 1111\ 0011\ 1000$. After concatenating $\hat{T}$ to T, we obtain the test sequence shown in Table VI under column extended.

The second time the same fault f is considered, the test subsequence $T[4, 8] = 0100\ 1011\ 1001\ 0000\ 0000$ is found again. This time, the order of omission is set to $\langle 3, 4, 0, 2, 1 \rangle$. Again, only the vector at time unit 2 is omitted to obtain $\hat{T} = 0100\ 1011\ 0000\ 0000$. We randomly decide to try and complement bits 0 and 1 at time unit 0, bit 1 at time unit 1, bits 0, 1, and 3 at time unit 2, and bit 0 at time unit 3. All the bits are complemented without losing the detection of the fault. The resulting test subsequence is $\hat{T} = 1000\ 1111\ 1101\ 1000$. This test subsequence is different from the one extracted before for the same fault.

After concatenating a test subsequence $\hat{T}$ for the fault g stuck-at v to T, we simulate the pessimistic unspecified transition fault $g : v \rightarrow v'$. If the number of detections of $g : v \rightarrow v'$ does not increase, we remove $\hat{T}$ from T in order not to increase the length of T unnecessarily.

The results of test generation for the circuits of Table I are reported in Tables VII–X. We explain the table entries and then discuss the results.

In Table VII, we show the test length before test generation (column init) and after test generation (column tg).

In Table VIII, we show the fault coverages of stuck-at faults (column s.a.), pessimistic unspecified transition

TABLE VII
TEST LENGTHS AFTER TEST GENERATION

	len	
circuit	init	tg
s208	105	485
s298	117	364
s344	57	182
s382	516	2028
s386	121	506
s400	611	2177
s420	108	443
s510	258	343
s526	1006	3119
s641	101	446
s820	491	1546
s953	267	1066
s1196	238	1130
s1423	1024	3044
s5378	646	2172
s35932	150	1150
b03	130	404
b04	168	696
b09	269	672
b10	190	453
b11	675	907
average	345	1111

TABLE VIII
FAULT COVERAGES AFTER TEST GENERATION

	s.a.		p-xtr		o-xtr	
circuit	init	tg	init	tg	init	tg
s208	70.19	70.19	51.68	54.09	61.54	62.74
s298	89.60	89.77	69.97	71.81	89.09	89.26
s344	97.38	97.38	85.47	89.53	96.51	96.95
s382	96.60	96.99	74.08	76.18	96.73	96.99
s386	90.16	90.16	67.49	74.74	88.99	89.77
s400	95.38	95.50	72.38	74.50	94.75	95.12
s420	46.79	46.79	27.98	28.33	32.50	32.74
s510	100.00	100.00	85.39	86.08	100.00	100.00
s526	86.88	86.88	59.13	61.69	86.41	86.41
s641	88.12	88.12	75.16	80.31	82.11	82.34
s820	96.34	96.34	74.51	80.67	96.34	96.34
s953	99.37	99.37	88.20	93.60	99.37	99.37
s1196	99.87	99.87	81.56	97.20	99.83	99.87
s1423	96.94	97.36	83.24	85.73	96.94	97.19
s5378	80.34	80.34	71.72	73.09	77.37	77.39
s35932	89.78	89.78	86.50	87.20	89.77	89.78
b03	74.22	74.22	54.17	55.34	63.67	63.67
b04	88.66	88.66	72.42	79.03	87.13	87.17
b09	84.81	84.96	63.72	67.40	83.33	83.63
b10	93.33	93.33	70.57	76.21	93.56	93.56
b11	92.40	92.46	75.68	76.83	91.91	91.97
average	88.44	88.50	71.00	74.74	86.09	86.30

faults (column $p-$ xtr), and optimistic unspecified transition faults (column $o-$ xtr). The fault coverage before test generation is shown under column init, and the fault coverage after test generation is shown under column tg.

Increases in the stuck-at fault coverage due to test generation are possible in Table VIII since the initial test sequences used were generated assuming an unknown initial state while we are assuming that the circuit is initialized to the all-zero state before the test sequence is applied.

In Table IX, we show the average numbers of detections of stuck-at faults (column s.a.), pessimistic unspecified transition faults (column $p-$ xtr), and optimistic unspecified transition faults (column $o-$ xtr).

TABLE IX
AVERAGE NUMBERS OF DETECTIONS AFTER TEST GENERATION

	s.a.		p-xtr		o-xtr	
circuit	init	tg	init	tg	init	tg
s208	2.32	3.46	1.47	2.66	2.09	3.11
s298	4.20	4.45	3.05	3.54	4.19	4.43
s344	4.69	4.87	3.99	4.43	4.64	4.85
s382	4.66	4.82	3.18	3.76	4.70	4.85
s386	3.89	4.49	2.73	3.61	3.88	4.47
s400	4.67	4.78	3.18	3.69	4.64	4.76
s420	1.76	2.31	0.91	1.38	1.24	1.62
s510	4.95	4.99	4.17	4.29	4.96	5.00
s526	4.29	4.34	2.71	3.06	4.27	4.32
s641	4.07	4.39	3.32	3.97	3.80	4.10
s820	4.44	4.75	3.43	3.98	4.54	4.79
s953	4.56	4.96	3.72	4.64	4.57	4.96
s1196	3.82	4.93	2.54	4.67	3.81	4.93
s1423	4.34	4.79	4.05	4.25	4.76	4.86
s5378	3.81	3.96	3.37	3.59	3.69	3.84
s35932	4.48	4.49	4.29	4.36	4.48	4.49
b03	3.42	3.67	2.38	2.75	2.99	3.16
b04	4.13	4.41	2.66	3.87	4.13	4.36
b09	3.92	4.18	2.92	3.34	3.90	4.18
b10	4.38	4.65	3.21	3.76	4.41	4.67
b11	4.57	4.62	3.71	3.82	4.56	4.60
average	4.07	4.40	3.09	3.69	4.01	4.30

In Table X, we show the numbers of unspecified transition faults detected d_0 times, for $d_0 = 0, 1, \ldots, 5$. The first row for every circuit shows the numbers of detections before test generation, and the second row shows the numbers of detections after test generation. Under column $p-$ xtr, we show the numbers of detections of the pessimistic unspecified transition faults, and under column $o-$ xtr, we show the numbers of detections of the optimistic unspecified transition faults.

From the tables, test generation increases the percentage of the detected pessimistic unspecified transition faults. This corresponds to a reduction in the number of faults with $d = 0$ detections after test generation. Test generation also increases the average number of detections of the pessimistic transition faults. The number of faults with $d \geq 5$ detections increases significantly. In some cases, the number of faults detected is at least five times more than doubles. For example, in s208, 69 faults are detected at least five times before test generation, and 218 faults are detected at least five times after test generation. The average number of detections includes the effect of test generation on all the values of d. The same applies to the optimistic unspecified transition faults. Relatively few pessimistic unspecified transition faults remain, which are detected between one and four times. Even fewer such optimistic unspecified transition faults remain.

Faults that remain uncovered $(d = 0)$ are expected to be undetectable, whereas faults with five detections may actually have much higher numbers of detections, and the corresponding standard transition faults (and delay defects) are expected to be detected. The small numbers of faults that remain with one to four detections can be targeted directly.

The increase in test length is consistent with the requirement to detect each fault five times $(n = 5)$.

V. CONCLUDING REMARKS

We defined a transition fault model for use with at-speed test sequences. The model is referred to as the unspecified

TABLE X
NUMBERS OF DETECTIONS AFTER TEST GENERATION

		p-xtr						o-xtr					
circuit		d=0	d=1	d=2	d=3	d=4	d=5	d=0	d=1	d=2	d=3	d=4	d=5
s208	init	201	74	41	14	17	69	160	62	35	18	21	120
	tg	191	3	1	2	1	218	155	2	0	0	5	254
s298	init	179	32	26	21	22	316	65	10	27	1	32	461
	tg	168	5	1	2	4	416	64	1	5	1	1	524
s344	init	100	18	17	16	39	498	24	9	10	19	21	605
	tg	72	6	0	2	4	604	21	0	0	0	0	667
s382	init	198	61	30	18	34	423	25	9	11	10	12	697
	tg	182	7	1	2	4	568	23	0	0	0	1	740
s386	init	251	69	56	16	22	358	85	51	49	31	28	528
	tg	195	13	5	12	4	543	79	1	1	3	2	686
s400	init	221	39	41	23	23	453	42	7	9	5	11	726
	tg	204	0	2	7	4	583	39	0	0	0	0	761
s420	init	605	83	19	8	6	119	567	63	16	5	13	176
	tg	602	0	1	7	10	220	565	1	4	0	1	269
s510	init	149	5	1	29	17	819	0	3	0	10	9	998
	tg	142	2	1	0	0	875	0	0	0	0	0	1020
s526	init	430	11	51	19	20	521	143	3	1	9	15	881
	tg	403	3	2	1	2	641	143	0	0	0	0	909
s641	init	318	71	46	55	27	763	229	62	26	27	7	929
	tg	252	5	6	5	8	1004	226	2	3	1	2	1046
s820	init	418	55	50	47	27	1043	60	57	40	42	28	1413
	tg	317	14	7	4	7	1291	60	4	6	4	2	1564
s953	init	225	159	125	120	71	1206	12	73	90	77	50	1604
	tg	122	5	9	9	13	1748	12	1	0	4	2	1887
s1196	init	441	466	409	225	137	714	4	276	370	207	206	1329
	tg	67	36	61	36	50	2142	3	13	19	9	19	2329
s1423	init	477	34	31	39	9	2256	87	34	18	28	7	2672
	tg	406	14	9	5	6	2406	80	0	1	0	2	2763
s5378	init	2995	286	208	215	105	6781	2396	239	161	189	81	7524
	tg	2850	99	51	53	48	7489	2394	60	17	27	2	8090
s35932	init	9704	379	183	198	146	61254	7350	14	47	109	23	64321
	tg	9201	4	5	6	7	62641	7344	0	0	0	0	64520
b03	init	352	10	42	24	42	298	279	6	31	12	9	431
	tg	343	0	1	2	9	413	279	1	3	1	0	484
b04	init	630	191	279	230	126	828	294	50	45	65	49	1781
	tg	479	20	15	26	14	1730	293	0	1	0	5	1985
b09	init	246	36	5	5	10	376	113	26	22	2	10	505
	tg	221	1	0	6	2	448	111	0	0	1	1	565
b10	init	256	37	35	8	4	530	56	22	43	8	0	741
	tg	207	8	4	1	0	650	56	0	1	0	1	812
b11	init	445	8	24	5	13	1335	148	4	13	2	8	1655
	tg	424	5	1	6	5	1389	147	0	0	0	1	1682
average	init	897	101	82	64	44	3855	578	51	51	42	30	4290
	tg	819	12	9	9	10	4191	576	4	3	2	2	4455

transition fault model since it introduces unspecified values into the faulty circuit when fault effects may occur. Fault detection potentially occurs when an unspecified value reaches a primary output. Due to the uncertainty that the unspecified value will be different from the fault-free value, an added requirement of this model may be that a fault would be detected multiple times.

We defined pessimistic and optimistic unspecified transition faults that can be used to obtain ranges of fault coverages and numbers of detections for unspecified transition faults. Such ranges fit with the ranges of possible sizes of the standard transition faults. We also defined random unspecified transition faults that combine the pessimistic and optimistic fault-activation conditions randomly.

Experimental results demonstrated that the model behaves as expected in terms of fault coverage and numbers of detections of target faults. Moreover, an unspecified transition fault may have a significantly smaller number of detections than the related stuck-at fault. Thus, the model provides a target for the generation of at-speed test sequences, which is more effective than n-detection test generation for stuck-at faults.

A variation of an n-detection test-generation procedure for stuck-at faults was used for the generation of test sequences under this model.

We expect the unspecified transition faults to be used as follows. While the pessimistic unspecified transition faults are sufficient for obtaining a fault coverage metric for a test sequence applied at-speed, a consideration of optimistic or random unspecified transition faults adds more information about the potential detection of delay defects (or standard transition faults). Thus, test generation can start by targeting the pessimistic unspecified transition faults that are harder to

detect. If a pessimistic unspecified transition fault is not detected, the corresponding optimistic or random version of the fault can be targeted. It is also possible to include pessimistic and optimistic, or pessimistic and random, or all three versions of each fault in a single set of target faults. We found this approach to be useful for applications such as observation-point insertion (not described here), where it is important to capture all the possible behaviors of transition faults.

REFERENCES

[1] S. Dasgupta, R. G. Walther, T. W. Williams, and E. B. Eichelberger, "An enhancement to LSSD and some applications of LSSD in reliability, availability and serviceability," in *Proc. 11th Fault-Toler. Comput. Symp.*, 1981, pp. 880–885.

[2] J. Savir and S. Patil, "Scan-based transition test," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 12, no. 8, pp. 1232–1241, Aug. 1993.

[3] J. Savir and S. Patil, "Broad-side delay test," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 13, no. 8, pp. 1057–1064, Aug. 1994.

[4] S. Devadas, "Delay test generation for synchronous sequential circuits," in *Proc. Int. Test Conf.*, Aug. 1989, pp. 144–152.

[5] T. J. Chakraborty, V. D. Agrawal, and M. L. Bushnell, "Delay fault models and test generation for random logic sequential circuits," in *Proc. Des. Autom. Conf.*, Jun. 1992, pp. 165–172.

[6] I. Pomeranz and S. M. Reddy, "SPADES-ACE: A simulator for path delay faults in sequential circuits with extensions to arbitrary clocking schemes," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 13, no. 2, pp. 251–263, Feb. 1994.

[7] I. Pomeranz and S. M. Reddy, "At-speed delay testing of synchronous sequential circuits," in *Proc. 29th Des. Autom. Conf.*, Jun. 1992, pp. 177–181.

[8] S. Bose, P. Agrawal, and V. D. Agrawal, "Path delay fault simulation of sequential circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 1, no. 4, pp. 453–461, Dec. 1993.

[9] K.-T. Cheng, "Transition fault testing for sequential circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 12, no. 12, pp. 1971–1983, Dec. 1993.

[10] W.-C. Lai, A. Krstic, and K.-T. Cheng, "On testing the path delay faults of a microprocessor using its instruction set," in *Proc. VLSI Test Symp.*, Apr. 2000, pp. 15–20.

[11] J. Rearick and R. Rodgers, "Calibrating clock stretch during AC scan testing," in *Proc. Int. Test Conf.*, Nov. 2005, pp. 266–273.

[12] P. Franco and E. J. McCluskey, "Three-pattern tests for delay faults," in *Proc. 12th VLSI Test Symp.*, Apr. 1994, pp. 452–456.

[13] A. Pierzynska and S. Pilarski, "Quality considerations in delay fault testing," in *Proc. EURO-DAC*, Sep. 1995, pp. 196–201.

[14] A. Pierzynska and S. Pilarski, "Non-robust versus robust," in *Proc. Int. Test Conf.*, Oct. 1995, pp. 123–131.

[15] L.-C. Wang, J.-J. Liou, and K.-T. Cheng, "Critical path selection for delay fault testing based upon a statistical timing model," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 11, pp. 1550–1565, Nov. 2004.

[16] B. Seshadri, I. Pomeranz, S. M. Reddy, and S. Kundu, "Path-oriented transition fault test generation considering operating conditions," in *Proc. Eur. Test Symp.*, May 2005, pp. 54–59.

[17] I. Pomeranz and S. M. Reddy, "On n-detection test sequences for synchronous sequential circuits," in *Proc. 15th VLSI Test Symp.*, Apr. 1997, pp. 336–342.

[18] J. Waicukauski, E. Lindbloom, B. Rosen, and V. Iyengar, "Transition fault simulation," *IEEE Des. Test Comput.*, vol. 4, no. 2, pp. 32–38, Apr. 1987.

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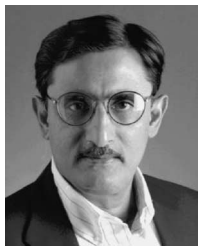

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