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Good Controllability and Observability Do Not Guarantee Good Testability

JACOB SAVIR

***Abstract*—In this paper we show that good controllability and observability do not guarantee good testability. In fact, one can easily find examples of faults that are difficult or impossible to detect, although both the controllability and observability figures are good.**

***Index Terms*—Controllability, deterministic testing, observability, random testing, testability.**

INTRODUCTION

The problem of analyzing the testability of a digital circuit has long been recognized to be an important one. With the levels of integration existing today, the cost of testing and diagnosis have become so large, that they are a significant part of the cost of the product. In order to reduce this cost it is crucial to have highly testable circuits. Since test generation and fault simulation consume a lot of computer time in present day densities, it is worthwhile to be able to predict whether or not the testing task is going to be easy.

A few testability measures and programs that implement them have been reported to date [1]–[5]. The limitations of these measures are:

1) The controllability, observability, and testability measures are not an accurate measure to the "ease of testing."
2) They fail to report testability problems in the presence of reconverging fanout.
3) The testability measures are defined such that "good controllability and observability figures usually imply good testability," which is not true in many cases.
4) Because the measures are not a true reflection of the ease of testing, they may guide the test designer to introduce hardware real estate (to enhance testability) in the wrong place.

In this paper we elaborate on these issues. The paper should not be regarded as a "new testability measure," but rather as an attempt to point out the limitations of the existing methods, and the kind of emphasis necessary from the future ones to come.

The discussion is restricted to combinational circuits and stuck-at-faults.

I. DEFINITIONS AND PROPERTIES

Let C be a combinational circuit with n inputs, $x_1, x_2, \cdots, x_n$, and m outputs, $F_1, F_2, \cdots, F_m$. Let $\vec{x} = (x_1, x_2, \cdots, x_n)$. Let $g(\vec{x})$ be a line in the circuit. We denote by $g/0$ ($g/1$) the fault g stuck-at-zero (g stuck-at-one).

The controllability of a line in the circuit is a measure of how easy it is to set the line to a given value. Similarly, the observability of a line is a measure of how easy it is to observe its value. We define the controllability and observability of a fault in the following way.

Definition 1: The *controllability of a fault* g/i, $i \in \{0, 1\}$ is the fraction of input vectors that will set the value of that line to $\bar{i}$. In other words, the controllability of a fault g/i is the probability that an input picked at random will set the value of line g to $\bar{i}$.

Definition 2: The *observability of a fault* g/i, $i \in \{0, 1\}$, is the fraction of input vectors that will propagate the effect of this fault to a primary output. In other words, the observability of a fault is the probability that an input picked at random will propagate the effect of this fault to a primary output.

The input vectors that detect the fault $g/0$ can be obtained by solving the Boolean equation

$$g(\vec{x}) \sum_{j=1}^{m} \frac{\partial F_j}{\partial g} = 1, \tag{1}$$

and the input vectors that detect the fault $g/1$ can be obtained by solving the equation

$$\bar{g}(\vec{x}) \sum_{j=1}^{m} \frac{\partial F_j}{\partial g} = 1 \tag{2}$$

where the summation symbol means the Boolean sum (OR operation). Thus, according to definitions 1 and 2, the controllability of the fault $g/0$, $c(g/0)$, is the fraction of input combinations that yield $g(\vec{x}) = 1$, and the controllability of the fault $g/1$, $c(g/1)$, is the fraction of input vectors that yield $\bar{g}(\vec{x}) = 1$. Similarly, the observability o of either fault ($g/0$, or $g/1$) is the fraction of the input vectors that yield

$$\sum_{j=1}^{m} \frac{\partial F_j}{\partial g} = 1. \tag{3}$$

It is worth while to note that the notion of the *syndrome* [6] of a function F, denoted by $S(F)$, is exactly the fraction of the input vectors that yield $F = 1$. Thus, we can take advantage of syndrome relations to compute controllability and observability figures. In particular, the following relations hold:

$$c(g/0) = S(g(\vec{x})), \tag{4}$$

$$c(g/1) = S(\bar{g}(\vec{x})), \tag{5}$$

and

$$o(g/0) = o(g/1) = S\left(\sum_{j=1}^{m} \frac{\partial F_j}{\partial g}\right). \tag{6}$$

Definition 3: The testability of a fault g/i, $i \in \{0, 1\}$ is the fraction of the input vectors that detect the fault.

In other words, the testability of a fault is the probability that an input picked at random will detect the fault.

According to Definition 3 and the notion of the syndrome, we can relate the testabilities $t(g/0)$ and $t(g/1)$ of the faults $g/0$ and $g/1$ to the following syndrome relations:

$$t(g/0) = S\left(g(\vec{x}) \sum_{j=1}^{m} \frac{\partial F_j}{\partial g}\right), \tag{7}$$

$$t(g/1) = S\left(\bar{g}(\vec{x}) \sum_{j=1}^{m} \frac{\partial F_j}{\partial g}\right). \tag{8}$$

The definitions listed above, and the properties of the syndrome, further imply the following relations between controllability, observability, and testability of a fault:

Property 1:

$$0 \le c(g/i), o(g/i) \le 1, \text{ for } i \in \{0, 1\} \tag{9}$$

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Property 2:

$$c(g/0) = 1 - c(g/1) \tag{10}$$

Property 3:

$$o(g/0) = o(g/1) \tag{11}$$

Property 4:

$$t(g/i) \leq Min[c(g/i), o(g/i)], i \in \{0, 1\} \tag{12}$$

Property 5: If $g(\vec{x})$ and $\sum_{j=1}^{m} \frac{\partial F_j}{\partial g}$ are independent (namely, both depend on different inputs), then

$$t(g/i) = c(g/i)o(g/i), i \in \{0, 1\}. \tag{13}$$

Note, that if a circuit is a tree, then Property 5 holds. However, we can even come up with a stronger statement. Let cone(g) be the collection of lines feeding (directly, or indirectly) the line g. Then Property 5 holds for line g if either

i) Every path originating in line $l \in$ cone(g) passes through line g, or

ii) Every path originating in line $l \in$ cone(g), and not passing through g, reaches the outputs $F_j, j = i_1, i_2, \cdots, i_k$, where $g \notin cone$ (F_j) for all $j = i_1, i_2, \cdots, i_k$.

The important point to observe here is that the tests that detect a given fault lie in the *intersection* of the set of input vectors that control the fault, and the collection of vectors that observe the fault. Thus, it is possible to have large controllability and observability sets, and small testability sets. So, no conclusion, based solely on controllability and observability, can be drawn, in general, regarding the testability of the circuit. Moreover, some testability measures proposed in the past define the testability as either the geometric mean of the controllability and the observability [1], [2], the square root of sum of squares of the controllability and the observability figures, or as a product of the two [5]. These definitions may lead to false conclusions. In fact, using an arbitrary function of the product of observability and controllability as a measure of testability may lead to a result which is either vastly greater or smaller than the actual testability.

II. Examples

Example 1: Consider the circuit of Fig. 1, with the fault $g/1$. We have

$$g = x_2$$

and

$$F = x_1 g + \bar{x}_2.$$

Thus, the controllability, observability, and testability are given by

$$c(g/1) = S(\bar{g}) = S(\bar{x}_2) = 1/2,$$

$$o(g/1) = S\left(\frac{\partial F}{\partial g}\right) = S(x_1 x_2) = 1/4,$$

and

$$t(g/1) = S\left(\bar{g}\frac{\partial F}{\partial g}\right) = S(\bar{x}_2 x_1 x_2) = 0.$$

In this example, for the specified fault, we have 50 percent controllability, 25 percent observability figure, and 0 testability figure. Notice that the product of the controllability and observability is much larger than the testability figure. The reconverging fanout, in this example, yields disjoint controllability and observability sets which explains the 0 testability figure. Obviously, the circuit of Fig. 1 is redundant.

Example 2: Consider the circuit of Fig. 2, with fault $g/0$. We have

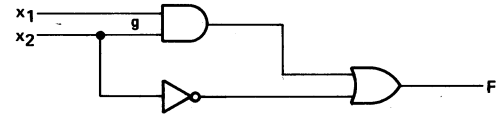

Fig. 1. The circuit of Example 1.

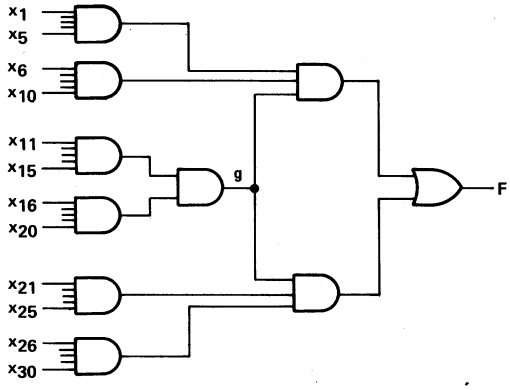

Fig. 2. The circuit of Example 2.

$$g = \prod_{j=11}^{20} x_j,$$

$$F = g\left(\prod_{j=1}^{10} x_j + \prod_{j=21}^{30} x_j\right)$$

where Πx_j means Boolean multiplication (AND operation).

$$\frac{\partial F}{\partial g} = \prod_{j=1}^{10} x_j + \prod_{j=21}^{30} x_j.$$

Thus,

$$c(g/0) = S(g) = 2^{-10},$$

and

$$o(g/0) = S\left(\frac{\partial F}{\partial g}\right) = 2^{-10} + 2^{-10} - 2^{-20} \cong 2^{-9}.$$

Since the line g meets the condition of Property 5, we have

$$t(g/0) = c(g/0)o(g/0) \cong 2^{-19}.$$

One could argue that neither the controllability nor the observability figures are too bad (application of, say, 10 000 random inputs are either very likely to control the fault, or observe the fault), but the testability figure is very low (it requires an application of about one million random inputs to have a good chance of detecting the fault).

Example 3: Consider the circuit of Fig. 3, with fault $g/1$. We have

$$g = \overline{x_2 x_3},$$

$$c(g/1) = S(x_2 x_3) = 1/4,$$

$$\frac{\partial F_1}{\partial g} = 0$$

$$F_2 = \bar{g} + x_3 x_4,$$

$$\frac{\partial F_2}{\partial g} = \overline{x_3 x_4},$$

$$F_3 = \bar{g} + x_4 x_5,$$

$$\frac{\partial F_3}{\partial g} = \overline{x_4 x_5},$$

$$o(g/1) = S(\overline{x_3 x_4} + \overline{x_4 x_5}) = S(\bar{x}_3 + \bar{x}_4 + \bar{x}_5) = 7/8,$$

$$t(g/1) = S[x_2 x_3(\bar{x}_3 + \bar{x}_4 + \bar{x}_5)] = S[x_2 x_3(\bar{x}_4 + \bar{x}_5)] = 3/16.$$

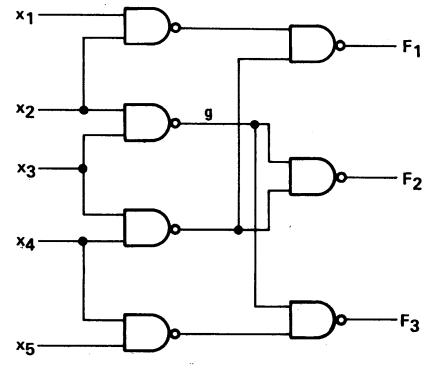

Fig. 3. The circuit of Example 3.

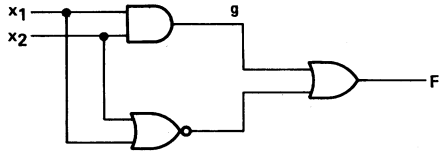

Fig. 4. The circuit of Example 4.

Note, that in this case

$$t(g/1) < c(g/1)o(g/1),$$

namely, the testability figure is worse than the product of the controllability and observability figures.

Example 4: Consider the circuit of Fig. 4, with fault $g/0$. We have

$$g = x_1x_2,$$

$$F = g + \bar{x}_1\bar{x}_2,$$

$$c(g/0) = S(g) = 1/4,$$

$$o(g/0) = S\left(\frac{\partial F}{\partial g}\right) = S(x_1 + x_2) = 3/4,$$

$$t(g/0) = S\left(g\frac{\partial F}{\partial g}\right) S[x_1x_2(x_1 + x_2)] = 1/4.$$

This is an example for which the testability is larger than the product of the controllability and observability.

III. Summary and Conclusions

In this paper we have shown that, in general, no conclusion can be drawn regarding the testability of the circuit, based strictly on the examination of the controllability and observability figures. The reason for that is that the testability is governed by the overlap between the input vectors that control the fault, and those that observe the fault. Thus, it is possible to have large controllability and observability sets, and, still, poor testability sets. We have shown that the testability of a fault is at best the smaller between the controllability and observability figures. We have shown examples where the controllability and observability figures were reasonably good, while the testability figure was poor, or even 0.

This paper should by no means be regarded as a tool for computing testability figures. The problem of computing the testability is in general NP-complete. The thrust of this paper is to show that the widely used notions of controllability and observability may be insufficient in analyzing testability issues. In particular this is critical when very high fault coverages are required. In this case, it is important to detect every detectable fault. It is necessary, therefore to have a testability estimation engine which besides being simple and efficient, has to be able to identify correctly testing bottle necks.

It is important to note that the definitions of controllability, observability, and testability apply both to random testing and deterministic testing. Because of its probabilistic interpretation, it is evident that it applies to random testing (and therefore to any method based on random application of patterns, like, for example, self-test with random patterns). It also applies to deterministic testing, since it addresses the size of the class of input patterns that either control, observe, or detect the fault. The larger the class of test vectors, the easier it will be for any deterministic test generator to locate one.

A subsequent paper will report on efforts to come up with testability prediction tools which trade off complexity with accuracy, and have the potential of meeting the challenges listed above.

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Comments on "Optimal Design of Distributed Information Systems"

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***Abstract*—Deficiencies in the formulation of the model for optimal design of the distributed network are pointed out. These concern the existence of communication links and routing variables for updates. Several feasible solutions, with a lower cost than the one given in the above paper for the example discussed, are presented. These establish the inadequacy of the procedure adopted to arrive at the optimal design.**

The paper[1] represents an effort to develop a comprehensive model for distributed information systems. Towards this end, distribution of processing power, allocation of programs and databases, assignment of communication line capacities, etc., have been taken into account. An algorithm to obtain the optimal solution of the model has been proposed. The paper applies the techniques developed to the real-life example of the distributed system of a large bank.

The model, however, has certain major deficiencies which result in an incorrect and nonoptimal result. Some of them are as explained below.

1) The routing variables for user to program and program to database have not been linked to the existence of corresponding com-

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