Controllability/Observability Analysis of Digital Circuits

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Abstract—**The testability of a digital circuit is directly related to the difficulty of controlling and observing the logical values of internal nodes from circuit inputs and outputs, respectively. This paper presents a method for analyzing digital circuits in terms of six functions which characterize combinational and sequential controllability and observability.**

I. Introduction

As LSI circuits become larger, the need for designing them with testability in mind becomes more acute. To accomplish this objective, it is necessary to quantify the testability of a circuit in some manner. This quantitative measure of testability can then be used to aid in partitioning circuits to make systems more testable.

Such testability measures as gate count, number of test vectors needed to achieve a given fault coverage and controllability/observability (C/O) matrices for linear-sequential machines have been considered and compared for consistency by Dejka [1]. Unfortunately, all of these measures have problems: gate count is too crude; test sequence length is too difficult to determine in general; and most practical circuits are not linear-sequential machines.

Stephenson and Grason [2] developed testability measures normalized between zero and one for register-transfer-level digital circuits and compared their predictions with actual test-generation effort required for digital circuits of various sizes. There appeared to be good correlation between testability values and actual test-generation effort. Breuer [3] worked on characterizing the costs associated with setting lines internal to a digital circuit to specified logical values and driving these values to primary outputs. These measures are not normalized and their values tend to increase as the testability of the circuit decreases. They were developed specifically for the purpose of improving the efficiency of automated test-sequence generation by providing estimates of the difficulty of justification and propagation operations in a D-algorithm-type approach.

Other approaches to the testability problem include design for testability using LSSD [4], analysis and system reorganization to enhance testability using COMET [5], and diagnosability theory for digital systems [6].

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II. Preliminaries

This paper will develop six functions to characterize the C/O properties of the internal nodes of a digital circuit. The intent is to provide a quantitative measure of the difficulty of controlling and observing the logical values of internal nodes from consideration of circuit topology alone without analyzing particular sequences of input and state vectors. Ideally, the measures should be easy to compute and accurately characterize the C/O properties of interest.

The digital circuits under consideration are composed of combinational and sequential standard cells or modules contained in a standard cell library. This library includes basic elements such as AND gates, OR gates, inverters, buffers, flip-flops, as well as more complex logical functions created by combining basic elements. Depending upon the level of integration utilized, standard cells may be packaged independently (SSI or MSI) or connected on a single IC by a layout program (LSI). The functions selected for implementation as standard cells depend upon both the technology (functions easy to realize in MOS, I^2L, etc.) and the type of design work underway (frequently used functions). While the analysis presented in this paper assumes the existence of a standard cell library, it places no restrictions upon its contents.

The C/O functions to be described are divided into two sets—combinational and sequential. Combinational 0 and 1 controllabilities of an internal node N, $CC^0(N)$ and $CC^1(N)$, are related to the minimum number of combinational node assignments in the circuit required to justify a 0 or 1, respectively, on node N. A "combinational node" is defined as either a primary input node or an output node of a combinational standard cell. The combinational observability of N, $CO(N)$, is related to both the number of combinational standard cells between node N and a primary output terminal and the minimum number of combinational node assignments required to propagate the logical value on node N to a primary output of the circuit.

Sequential 0 and 1 controllabilities of a node N, $SC^0(N)$ and $SC^1(N)$, estimate the minimum number of sequential nodes that must be set to specified logical values in order to justify a 0 or 1, respectively, on node N. A "sequential node" is an output node of a sequential standard cell. These sequential controllabilities provide a

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measure of the number of time frames required to control nodes that are deeply embedded in a digital network from the primary inputs. If it is possible to exploit parallelism inherent in the circuit to simultaneously control groups of sequential nodes, the acutal number of time frames needed to set a node of the circuit to a specified logical value may be less than the estimate provided by the sequential controllability measures. In this sense, the sequential controllabilities estimate an upper bound. Analogously, the sequential observability of node N, $SO(N)$, is related to both the number of sequential standard cells between node N and a primary circuit output and the number of sequential standard cells that must be controlled in order to propagate the logical value of N to an output.

III. Motivation

A. Combinational Testability Measures

The combinational 0 and 1 controllabilities and combinational observabilities mentioned in the preceding section can be viewed as cost functions measuring the difficulty in a spatial sense of accomplishing the complete set of node justifications required to control or observe a specified node in the circuit. This approach is philosophically related to that of Breuer [3] in its utilization of the cost function concept but supplants Breuer's method by providing a more accurate and consistent relationship of cell depths and functions to controllability and observability costs and by dichotomizing these costs into spatial and temporal components (combinational and sequential testability measures, respectively).

Quantitatively, the magnitude of the combinational e controllability, $e \in \{0,1\}$, of node A in a given logic circuit can be positively correlated with the percentage of nodes in the circuit that must be set to specified logical values in order to justify a logical value e on node A. As an example, consider a set of two-input AND gates interconnected as a binary tree with output node OUT. For a tree depth of k, there will be 2^k primary inputs, 2^k-1 AND gates, and $2^{k+1}-1$ nodes in the circuit. In order to set node OUT to a logical 1, every node in the circuit must be set to a logical 1, and $CC^1(\text{OUT})=2^{k+1}-1$, an exponential function of tree depth. However, only one primary input and only $k+1$ nodes total must be set to logical 0 in order to force OUT to 0. Therefore, $CC^0(\text{OUT})=1+k$, a linear function of tree depth. This result agrees with the intuitively reasonable observation that it is substantially easier to set the output of a tree of AND gates to a logical 0 than to set it to a logical 1.

1) Relationship to Signal Probabilities: Additional corroboration for the reasonableness of the approach presented in this paper comes from the work of Parker and McCluskey on signal probabilities [7]. If the justification of an internal node A in a circuit to a logical value 1, for example, is very difficult to accomplish, then $CC^1(A)$ will be computed to be a large positive integer. The analysis of Parker and McCluskey generates the result that the probability of node A being a logical 1 will be near 0 for equal input signal probabilities. On the other hand, an easy node justification will have a smaller combinational controllability number and a larger signal probability (nearer 1) associated with it. In the case of the AND gate binary tree example, for equally likely logical values on all of the circuit input lines, $P(\text{OUT}=1)=(1/2)^{2^k}$ and $P(\text{OUT}=0)=1-(1/2)^{2^k}$, where $CC^1(\text{OUT})=2^{k+1}-1$ and $CC^0(\text{OUT})=1+k$, as derived earlier.

Although the correlation discussed in the preceding paragraph between signal probabilities and the controllability measures defined in this paper does exist, there is a basic difference in objective between the two approaches. The C/O numbers computed by the algorithm presented here are an inherent property of the topology of the circuit under consideration. As discussed by Keiner [8] inherent testability is a deterministic property of the circuit design that excludes test stimulus/response considerations. When the environment within which the circuit operates is taken into consideration, probabilistic measures such as those discussed by Parker and McCluskey become more meaningful.

2) Minimum Cost Approach: In general, there are a number of alternative mechanisms for accomplishing a specified node justification in a circuit. Each distinct alternative will have a cost associated with it. The costs actually utilized in the analysis presented in this paper to characterize node controllabilities and observabilities are the minima over the sets of alternatives of the costs associated with each alternative. This approach is motivated by the observation that the cost of controlling a node in a digital circuit will depend only upon the method actually chosen to accomplish the control. Since the best alternative is the easiest to accomplish, it will have the minimum cost. Costs of alternatives not chosen are not relevant.

The minimum cost approach proposed in this paper contrasts with the testability analysis technique discussed by Stephenson and Grason [2]. Their objective in the formulation of controllability transfer factors (CTF's), for example, for logical components is to characterize the uniformity of a module's input–output mapping. These factors are normalized between 0 and 1 with values near 0 corresponding to less uniform I/O maps and CTF's near 1 being produced by more uniform maps. Their reasoning is that the greater the deviation from uniformity of a logical component's input–output mapping the more difficult it will be to obtain particular output values and, hence, the less controllable the component will be. This is basically an averaging approach, and it tends to obscure the relative difficulties of accomplishing distinct logical justifications on a component's output nodes.

As a specific example of the contrast between CTF's and combinational controllability measures, consider 2- and 3-input AND gates. The CTF's of 2- and 3-input AND gates are 1/2 and 1/4, respectively, indicating that a

3-input AND gate is less controllable than a 2-input AND gate. The combinational 0 and 1 controllabilities for these same two gates, when their inputs are primary inputs of the circuit, are 2 and 3 for the 2-input AND gate and 2 and 4 for the 3-input AND gate. Notice that these combinational controllability measures preserve the information that the loss of controllability in adding one input to a 2-input AND gate is caused by the increased difficulty of setting the output node to a logical 1. The 0 controllability of the output node is not affected.

3) Treatment of Reconvergent Fanout: For circuits with reconvergent fanout, the combinational controllability and observability numbers defined in this paper measure the minimum number of combinational node assignments in the equivalent tree circuit required to accomplish the necessary logical justifications. This approach to the definition of testability measures accomplishes two objectives:

1) reduces the complexity of testability analysis from an exponential to a linear function of circuit size, making computer program implementation feasible for large circuits, and
2) produces an exact analysis for circuits without reconvergent fanout and provides a useful approximate analysis in the general case which is a consistent extension of the procedure for circuits with no reconvergent fanout.

The combinational testability measures as defined can be used to flag potentially uncontrollable nodes. If node A is 0 or 1 uncontrollable because either it or one of its predecessors is not properly connected to the primary inputs of the circuit, its combinational 0 or 1 controllability will be computed to be ∞. However, if node A is, for example, 1 uncontrollable because of reconvergent fanout, its combinational 1 controllability will not be computed to be infinite. Proving that node A is 1 uncontrollable requires the exploration of all possible control mechanisms for node A, an exponentially complex process in general. Since this approach is not feasible for very large circuits, it is worthwhile to investigate the information obtainable about circuit testability with a linear computational effort.

Using a linear complexity algorithm, it can be determined that $CC^1(A)$ is an integer larger than the total number of combinational nodes in a subcircuit containing node A and its predecessor fanout point. The interpretation of this result is that distinct nodes in the equivalent tree circuit corresponding to the same node in the actual circuit must be assigned to different logical values in order to set node A to a logical 1. This inconsistent multiple assignment condition leads to node uncontrollability. It is also possible for a multiple assignment to be logically consistent. The reduction in computational complexity of the testability analysis approach presented in this paper over exhaustive search is related to the fact that the logical consistency of multiple node assignments is not completely resolved in circuits possessing reconvergent fanout. However, since nodes with large combinational controllability numbers may in fact be uncontrollable, they can be identified by this analysis and examined more closely by design engineers. Similar comments apply to the interpretation of the observability measures.

B. Sequential Testability Measures

The sequential 0 and 1 controllabilities and sequential observabilities defined in Section II are cost functions measuring the difficulty in a temporal sense of accomplishing the node justifications required to control or observe a specified node in the circuit. Since a combinational circuit possesses no sequential standard cells, all of its sequential controllability and observability numbers are zero. The interpretation of this result is that any possible node justification in a combinational circuit can be accomplished within one time frame.

For the case of general sequential circuits, the sequential controllability numbers estimate the number of sequential modules that must be set to specified logical values in order to accomplish the necessary node justifications. If the sequential cells in a circuit are interconnected serially, the logical justification of each successive sequential node will take one additional time frame, and the sequential controllability numbers will measure the number of time frames required to accomplish the desired operations. If it is possible to exploit circuit parallelism to simultaneously control groups of sequential nodes, then the actual number of time frames required to accomplish certain node justifications may be less than the estimate provided by the sequential controllability numbers. However, these sequential testability measures can always be interpreted as temporal cost functions.

The combinational controllability and observability numbers for a sequential circuit can still be viewed as spatial cost functions, but now that cost may be spread over a number of time frames instead of concentrated in one time frame as in the case of combinational circuits.

IV. Quantitative Testability Analysis

A. Primary Inputs and Outputs

If I is a primary input node of a digital circuit, then the controllabilities of node I are defined as follows:

$$CC^0(I) \triangleq 1 \tag{1}$$

$$CC^1(I) \triangleq 1 \tag{2}$$

$$SC^0(I) \triangleq 0 \tag{3}$$

and

$$SC^1(I) \triangleq 0. \tag{4}$$

Equations (1) and (2) follow from the consideration that a primary input is a combinational node that requires

exactly one node assignment to set to either 0 or 1. Since it is not necessary to control any sequential nodes in the justification of a primary input, $SC^0(I)$ and $SC^1(I)$ are defined to be 0.

A primary output node U of a digital circuit can be observed without the necessity of either controlling or observing any other nodes in the circuit. Therefore, $CO(U)$ and $SO(U)$ can be consistently defined to be 0.

$$CO(U) \triangleq 0 \tag{5}$$

and

$$SO(U) \triangleq 0. \tag{6}$$

B. Standard Cells

In analyzing the controllability of standard cells, we are interested in determining the difficulty of setting cell output nodes to specified logical values in terms of the corresponding quantities for cell input nodes. The observability of standard cell input nodes depends upon both the cell output node observabilities and the controllabilities of the input nodes and output nodes.

To compute the controllability of a standard cell output node, all possible input assignments that accomplish the desired output node justification are examined, and a number equal to the sum of the controllabilities associated with each of the input assignments considered is computed. The minimum of these numbers, incremented by the cell depth, is defined to be the output node controllability.

In this paper, all cell depths will be defined to be either 0 or 1. The "combinational depth" of a combinational standard cell is defined to be 1, and its "sequential depth" is defined to be 0. The combinational depth of a sequential standard cell is defined to be 0, and its sequential depth is defined to be 1. Note that it is possible to define cell depths to be greater than 1. In fact, for multiple-output standard cells, the depths of different outputs may be defined to be different. However, for the definitions utilized in this paper, the node controllabilities and observabilities have relatively straightforward interpretations.

For a node N in a tree-like interconnection of standard cells, $CC^e(N)$ $[SC^e(N)]$, $e \in \{0,1\}$, is equal to the minimum number of combinational (sequential) node assignments required to set node N to a logical value e. This result is obvious for primary input nodes and can be proven by mathematical induction for the other nodes in the circuit. The combinational and sequential controllability numbers computed for more general circuits have a similar interpretation with respect to the equivalent tree circuit. Finally, combinational and sequential observabilities have an analogous interpretation.

In order to determine the observabilities of a standard cell input node, all of the cell input assignments that sensitize one or more cell outputs to changes in the specified input are considered. The observability of the input node is defined as the observability of the easiest to observe sensitized output plus the sum of the controllabilities of the minimum cost sensitizing input assignment plus the cell depth.

As an example, consider the C1130, a 3-input NOR combinational standard cell. The C1130 cell with output Y and inputs X_1, X_2, and X_3 realizes the logical function $Y=(X_1+X_2+X_3)'$. In order to assign Y to 1, it is necessary to set all three input nodes to 0. Hence,

$$CC^1(Y)=CC^0(X_1)+CC^0(X_2)+CC^0(X_3)+1 \tag{7}$$

and

$$SC^1(Y)=SC^0(X_1)+SC^0(X_2)+SC^0(X_3). \tag{8}$$

Notice that the combinational depth of the C1130 is equal to 1 and its sequential depth equals 0. The output Y can be set to 0 in three distinct ways: $X_1=1$, $X_2=d$, $X_3=d$; $X_1=d$, $X_2=1$, $X_3=d$; and $X_1=d$, $X_2=d$, $X_3=1$; where "d" represents "do not care." Therefore,

$$CC^0(Y)=\min\left[CC^1(X_1),CC^1(X_2),CC^1(X_3)\right]+1 \tag{9}$$

and

$$SC^0(Y)=\min\left[SC^1(X_1),SC^1(X_2),SC^1(X_3)\right]. \tag{10}$$

Observing input X_i requires the observation of output Y while the other two inputs are maintained at logical 0. Thus the observability equations for cell C1130 can be written

$$CO(X_i)=CO(Y)+CC^0(X_j)+CC^0(X_k)+1 \tag{11}$$

and

$$SO(X_i)=SO(Y)+SC^0(X_j)+SC^0(X_k) \tag{12}$$

where i, j, k are distinct elements of the set $\{1, 2, 3\}$.

The C1130 combinational controllability equations presented in (7) and (9) can be written in matrix form as follows:

$$\begin{bmatrix} CC^0(Y) \\ CC^1(Y) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ & & & \min & & & \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ & & & \min & & & \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} CC^0(X_1) \\ CC^1(X_1) \\ CC^0(X_2) \\ CC^1(X_2) \\ CC^0(X_3) \\ CC^1(X_3) \\ 1 \end{bmatrix}. \tag{13}$$

The output controllability vector on the left is computed by multiplying the input controllability vector by the combinational controllability matrix. Whenever a "min" is encountered, the scalar product of the next row of the matrix with the input vector is formed, and the minimum of that result and the previously computed result becomes

the entry for the current component of the controllability output vector. Multiple minima are handled in an analogous fashion. If no "min" word is encountered, the next output vector component is computed.

Notice that the matrix utilized in (13) consists of entirely 0's, 1's, and "min's." It can be compactly represented in a cell library entry by writing each binary line as an octal number and each "min" line as an *M*. The resulting library entry line for the C1130 combinational controllability (*CC*) matrix has the form:

$$41 \quad M \quad 11 \quad M \quad 3 \quad 125. \tag{14}$$

Analogous analyses can be performed for the combinational observability (*CO*), sequential controllability (*SC*), and sequential observability (*SO*) properties of cell C1130, resulting in a complete controllability/observability library entry of the form:

```
Name   C113 0
CC     41    M    11   M   3   125
CO     1025      1105   1121
SC     40    M    10   M   2   124
SO     1024      1104   1120
End.                                  (15)
```

Each combinational and sequential cell of interest can be analyzed in the manner indicated above, and entries of the form presented for the C1130 can be made in the library.

For a second example, consider the C1490, a resettable negative-edge-triggered *D*-flip-flop sequential standard cell. In order to set the output Q of a C1490 to 1, it is necessary to set the D input to 1, hold the reset line R at 0, and generate a falling edge on the clock line, C. Therefore, the 1 controllability equations for Q can be written:

$$CC^1(Q) = CC^1(D) + CC^1(C) + CC^0(C) + CC^0(R) \tag{16}$$

and

$$SC^1(Q) = SC^1(D) + SC^1(C) + SC^0(C) + SC^0(R) + 1. \tag{17}$$

Notice that the difficulty of generating a falling edge on the clock line is represented in (16) by $CC^1(C) + CC^0(C)$, since it is necessary first to set the clock line to 1, then force it to 0.

There are two distinct mechanisms for setting Q to 0. Either the reset line can be used while maintaining the clock line at a logical 0, or a 0 value can be clocked into the flip-flop from the *D*-input line. Consequently, the 0-controllability equations for Q can be written:

$$CC^0(Q) = \min \left[CC^1(R) + CC^0(C) \right.$$
$$\left. CC^0(D) + CC^1(C) + CC^0(C) + CC^0(R) \right] \tag{18}$$

and

$$SC^0(Q) = \min \left[SC^1(R) + SC^0(C) \right.$$
$$\left. SC^0(D) + SC^1(C) + SC^0(C) + SC^0(R) \right] + 1. \tag{19}$$

The *D*-input line value can be observed at the Q output of the flip-flop by generating a falling edge on the clock line while holding the reset line low.

$$CO(D) = CO(Q) + CC^1(C) + CC^0(C) + CC^0(R) \tag{20}$$

and

$$SO(D) = SO(Q) + SC^1(C) + SC^0(C) + SC^0(R) + 1. \tag{21}$$

The reset line R can be observed at Q by setting the flip-flop to a logical 1 and then using the reset line to force it to a logical 0.

$$CO(R) = CO(Q) + CC^1(Q) + CC^0(C) + CC^1(R) \tag{22}$$

and

$$SO(R) = SO(Q) + SC^1(Q) + SC^0(C) + SC^1(R) + 1. \tag{23}$$

Finally, the clock line can be indirectly observed at the flip-flop output by either setting the flip-flop to 1 and clocking in a 0 or resetting the flip-flop to 0 and clocking in a 1.

$$CO(C) = \min \left[CO(Q) + CC^0(R) + CC^1(C) \right.$$
$$+ CC^0(C) + CC^0(D) + CC^1(Q)$$
$$CO(Q) + CC^0(R) + CC^1(C)$$
$$\left. + CC^0(C) + CC^1(D) + CC^0(Q) \right] \tag{24}$$

and

$$SO(C) = 1 + \min \left[SO(Q) + SC^0(R) + SC^1(C) \right.$$
$$+ SC^0(C) + SC^0(D) + SC^1(Q)$$
$$SO(Q) + SC^0(R) + SC^1(C)$$
$$\left. + SC^0(C) + SC^1(D) + SC^0(Q) \right]. \tag{25}$$

C. Controllability / Observability Calculation Algorithm for a Circuit

Calculate circuit node controllabilities.

Initializations: For all primary input nodes I, set

$$CC^0(I) = CC^1(I) = 1$$

$$SC^0(I) = SC^1(I) = 0.$$

For all other nodes N, set

$$CC^0(N) = CC^1(N) = \infty$$

$$SC^0(N) = SC^1(N) = \infty.$$

Working from primary inputs to circuit outputs, use standard cell controllability equations to map cell input node controllabilities into cell output node controllabilities.

Iterate on the above step until the controllability numbers stabilize (to handle feedback loops external to standard cells, etc.).

Since this is an integer algorithm, and the controllability numbers are monotonically nonincreasing from iteration to iteration, we are always guaranteed that the algorithm converges. Practically, only two or three iterations are usually necessary for the controllability numbers to stabilize.

Calculate circuit node observabilities.

Initializations: For all primary output nodes U, set

$$CO(U)=0$$
$$SO(U)=0.$$

For all other nodes N, set

$$CO(N)=SO(N)=\infty.$$

Working from primary outputs to circuit inputs, use standard cell observability equations together with the previously computed node controllabilities to map cell output node observabilities into cell input node observabilities. Note that the observability of a fanout point is defined to be equal to the minimum of the observabilities of the nodes to which it fans out.

Iterate on the above step until the observability numbers stabilize.

If, after application of the above algorithm to a given digital circuit, there remains a node N with an infinite e-controllability number, $e\in\{0,1\}$, then that node is e-uncontrollable. $CC^e(N)=\infty$ or $SC^e(N)=\infty$ is a sufficient but not necessary condition for the e uncontrollability of N. Similarly, $CO(N)=\infty$ or $SO(N)=\infty$ is a sufficient but not necessary condition for the unobservability of node N. As was discussed in the section on motivation, this type of untestability results from the existence in the circuit of nodes which are not properly connected to either primary inputs or outputs.

Program Implementation

In order to help evaluate the computational practicality of this testability analysis approach, working versions of the algorithms presented in the preceding section were implemented on a DEC-10 computer system. The algorithms as programmed were stable, and run times on the order of 0.75 min for 30 cell circuits and 3.5 min for 200 cell circuits were typical. When compared with multihour execution times for test-sequence-generation programs, these run times on the order of several minutes to accomplish the testability analysis of complex sequential circuits appear quite attractive.

V. Example-7-Stage-Feedback Shift Register

As an example of the analysis discussed in the preceding sections, consider the 7-stage-feedback shift-register circuit in Fig. 1. Application of the combinational controllability calculation algorithm to the circuit in Fig. 1 yields the combinational controllability profiles in Fig. 2. These

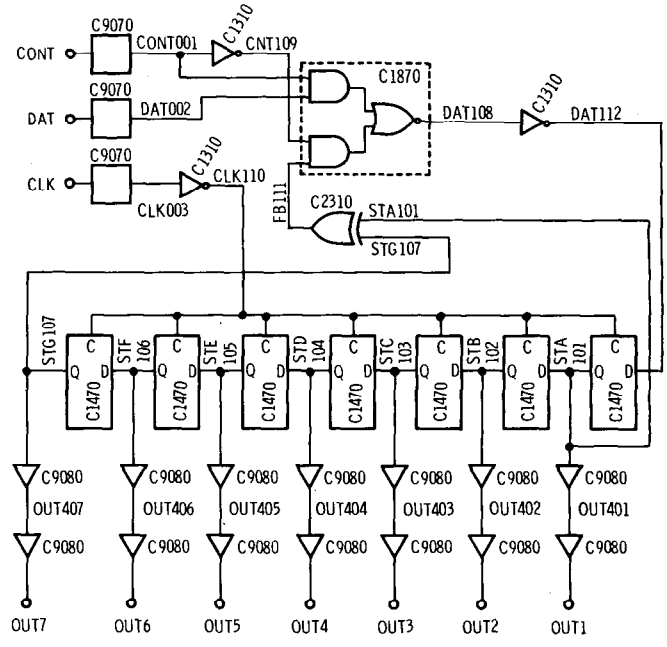

Fig. 1. 7-stage-feedback shift-register circuit.

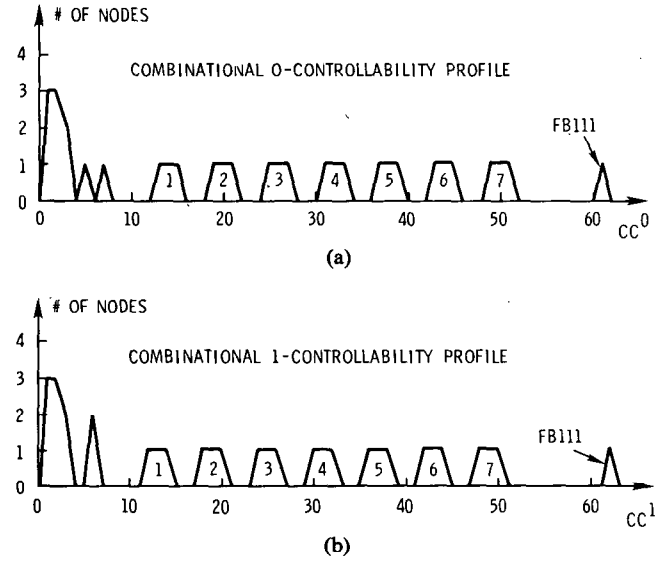

Fig. 2. Combinational controllability profiles of the 7-stage-feedback shift-register circuit. (a) Combinational 0-controllability profile. (b) Combinational 1-controllability profile.

profiles summarize circuit controllability information by plotting 0 or 1 controllability on the x axis versus the number of nodes possessing that controllability on the y axis. The result is a controllability density plot which can be used to characterize the overall controllability of the circuit, pinpoint the least controllable nodes, and suggest circuit modifications to enhance controllability.

For the 7-stage-feedback shift-register circuit, nodes near the primary inputs are highly controllable and appear between $CC=0$ and $CC=10$ on the controllability profiles. Each flip-flop in the shift register has a group of nodes associated with it that appear as a bump in the

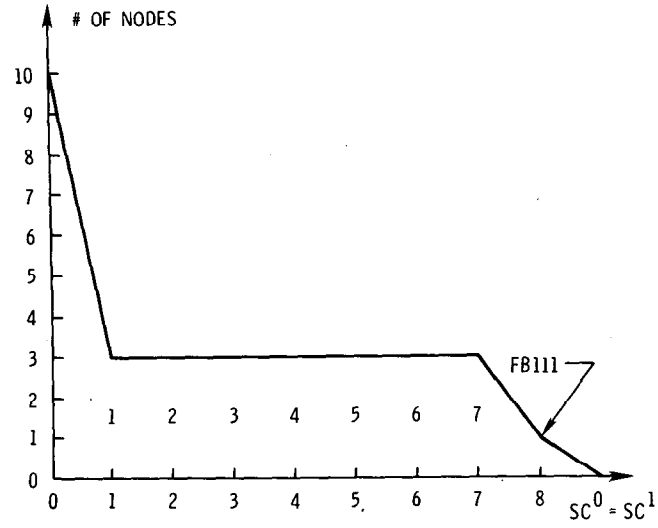

Fig. 3. Sequential controllability profiles of the 7-stage-feedback shift-register circuit.

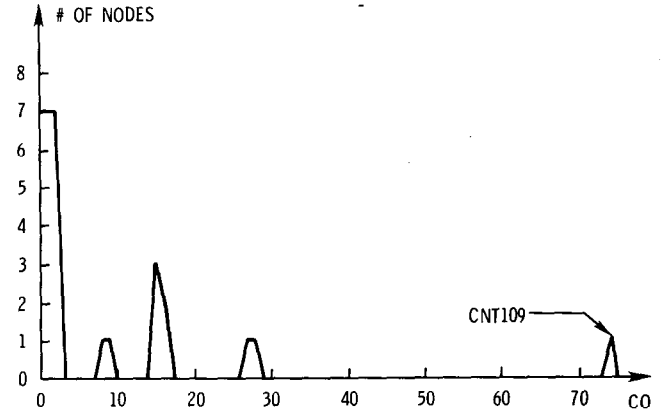

Fig. 4. Combinational observability profile for the 7-stage-feedback shift-register circuit.

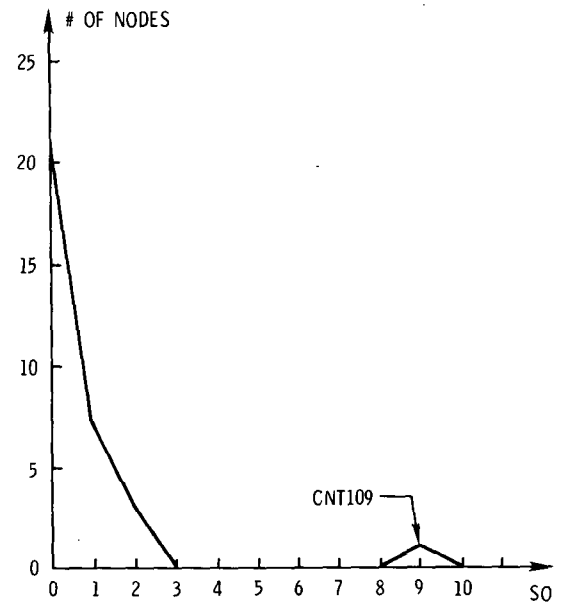

Fig. 5. Sequential observability profile for the 7-stage-feedback shift-register circuit.

profiles. Bumps one through seven correspond to flip-flops STA101 through STG107 in the profiles. The least controllable node in the circuit is FB111, the output of the feedback exclusive OR gate. This result is obvious from the observation that the inputs to the exclusive OR are the least controllable flip-flop output and one other flip-flop output.

The sequential 0 and 1 controllability profiles for the 7-stage-feedback shift-register circuit in Fig. 1 are identical and are presented in Fig. 3. These profiles are identical in this case because the input multiplexing circuitry allows any of the flip-flops in the circuit to be set to logical 0 or logical 1 with equal temporal facility. (The same number of sequential nodes must be controlled in either case.)

All of the combinational nodes near primary inputs have 0-sequential controllability and account for the peak in the sequential controllability profiles at $SC=0$. The nodes associated with flip-flops one through seven form a plateau in the sequential controllability profile between $SC=1$ and $SC=7$. Again, FB111 appears furthest to the right on the profile (at $SC=8$) indicating that it is the least-controllable node in the circuit from a sequential controllability point-of-view, as well as from a combinational controllability evaluation.

The combinational observability profile for the 7-stage-feedback shift-register circuit is presented in Fig. 4. The large peak near the origin represents outputs of flip-flops and their associated buffers. Each flip-flop output fed through two buffers is a primary output of the circuit. The other peaks in the profile correspond to nodes closer to primary inputs of the circuit. CNT109 is substantially less observable than any other node in the circuit, as indicated by the peak at $CO=74$. While this fact is not immediately obvious from the schematic, it can be understood by observing that CNT109 is one input of the AND gate whose other input is FB111, the least-controllable node in the circuit. If one additional output pad was available to enhance the observability of the circuit, a logical location for it would be at CNT109.

Finally, the sequential observability profile for the 7-stage-feedback shift-register circuit is presented in Fig. 5. Since most nodes in the circuit have a very small sequential depth from the primary outputs, a large peak near $SO=0$ appears in the profile. CNT109 is again flagged as the least observable node by the peak at $SO=9$.

VI. Evaluation of the Controllability/Observability Measures

Relationships between the controllability/observability measures presented in this paper and related approaches [2], [3], [7] have been discussed in the motivation section. In this section, correlations between the testability measures and inherent testability properties of a digital circuit will be presented.

It is apparent from Fig. 1 that the 7-stage-feedback shift-register circuit analyzed in the previous section is testable in the sense proposed in [4]. By setting primary input CONT to 1, the shift register can be initialized to any state through the primary circuit input DAT. Call this circuit C_1. If the input multiplexing section of C_1 is replaced by an OR gate with inputs FB111 and DAT and output DAT112, the only state to which the shift register can be initialized is 1111111, an obvious decrease in intrinsic controllability. Call this less-controllable circuit C_2.

If the maximum combinational controllability number CC_{max} is used as a figure of merit for the controllability of the circuit, it can be seen that CC_{max} exhibits the desired behavior for the two circuits defined above. Specifically,

$$CC_{max}(C_1)=62 \tag{26}$$

and

$$CC_{max}(C_2)=106. \tag{27}$$

As circuit controllability decreases, CC_{max} increases in the manner indicated in (26) and (27).

A circuit C_3 can be derived from C_1 by adding a sufficient number of primary inputs and multiplexers to control each flip-flop independently. This structure is inherently more controllable than C_1, and

$$CC_{max}(C_3)=19 \tag{28}$$

better than three times smaller than $CC_{max}(C_1)$. The enhanced controllability of C_3 over C_1 leads to improved observability properties for circuit C_3 as well since logical values can be propagated to primary outputs more easily. These intrinsic observability characteristics of circuits C_1 and C_3 are reflected by their maximum combinational observability numbers:

$$CO_{max}(C_1)=74 \tag{29}$$

and

$$CO_{max}(C_3)=33. \tag{30}$$

The more observable circuit C_3 has a CO_{max} better than two times smaller than $CO_{max}(C_1)$. By making the least-observable node in C_3 a primary output, the resulting configuration becomes even more observable and its CO_{max} is further reduced to 22. Sequential testability measures exhibit similar behavior.

While maximum controllability and observability numbers were used in this analysis to correlate with inherent circuit testability properties, other aspects of the controllability/observability profiles can provide additional information. Means, moments, and cumulative distributions can be derived from the node testability numbers to highlight various properties of the profiles; and measures of multimodality may be used to identify sections of the circuit that may be difficult to test. However, the key result to emphasize in this section is that the controllability and observability measures computed by the algorithms presented in this paper correlate well with intrinsic controllability and observability properties of the circuits analyzed.

VII. Use of the Controllability/Observability Measures

The testability measures presented in this paper can be utilized in two distinct modes: 1) to guide redesign for the purpose of enhancing circuit testability, and 2) to guide vector-generation algorithms as part of the test-sequence-generation process. While being used as a feedback tool for the design engineer, these measures identify potentially uncontrollable or unobservable nodes and order all of the nodes in the circuit according to the six parameters discussed. As the designer rearranges circuit topology and possibly adds test points, he can observe the effect of these actions on the testability profiles and factor this information into the design process.

As an aid for automated test-sequence-generation programs, these measures can be used to order the alternatives in decisions that must be made during the vector-generation process. For example, an ATG program will be more likely to quickly succeed in propagating an internal logical value to a primary output of the circuit if it has access to node observability information than if it must make random choices at each decision point. This intelligent guidance of the vector-generation process has the potential of substantially improving the performance of automated test sequence generation.

VIII. Conclusions

Six measures have been presented which characterize the controllability and observability of a digital circuit: combinational 0 and 1 controllability, sequential 0 and 1 controllability, combinational observability, and sequential observability. The dichotomization of these measures into spatial and temporal components has been discussed as well as their relationship to other testability measures proposed in the past. While motivating the treatment of circuits with reconvergent fanout, the relative complexities of this testability analysis and an exact treatment were compared, and the areas within which information was sacrificed to reduce the complexity of the problem were identified.

Section IV of the paper described required initializations, treatment of standard cells and development of a standard cell library, algorithms for the calculation of circuit node controllabilities and observabilities, and implementation of the algorithms in a working computer program. The controllability and observability of a 7-stage-feedback shift register was thoroughly analyzed and profiles were presented that allow visualization of these properties at a glance. This example was then extended for the purpose of correlating the testability measures derived with intrinsic controllability and observability properties of the circuits analyzed. Finally, use of the

controllability/observability measures to guide design for testability and automated test-sequence-generation was discussed.

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Frequency Domain Analysis for Operational Amplifier Macromodels

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***Abstract*—Under large signal conditions, active circuits containing operational amplifiers as elements can exhibit discontinuous response in the frequency domain. A computational procedure is described in this paper for the prediction of large signal frequency response characteristics of active circuits based upon an operational amplifier macromodel containing nonlinear circuit components to represent slew-rate limiting. The interconnection circuitry, exclusive of the operational amplifiers, is mathematically represented in the hybrid matrix form and a minimal set of nonlinear equations for the active circuit is given. A Newton–Raphson iteration, based on a describing function representation for the nonlinear circuit components, is used to numerically solve the circuit equations. Two active circuit configurations that have been observed to exhibit discontinuous large signal frequency response characteristics are described. Data obtained by application of the algorithm to these two circuits is given. Correlation between experimental data and computational results has been excellent.**

Nomenclature

$H_{ab}(j\omega)$	Hybrid matrix describing interconnection circuit response at terminals a resulting from excitation at terminals b.
$\{V_{IN}(j\omega)\}$	Vector of voltages at operational amplifier input terminals.
$\{I_{IN}(j\omega)\}$	Vector of currents flowing into operational amplifier input terminals.
$\{V_O(j\omega)\}$	Vector of voltages at operational amplifier output terminals.
$\{I_O(j\omega)\}$	Vector of currents flowing into operational amplifier output terminals.
$V_E(j\omega)$	External excitation voltage applied to the active circuit.
$\{V_T(j\omega)\}$	Vector of active circuit output voltages.
$G^{(i)}(\lvert V_{IN}^{(i)}\rvert)$	Admittance describing function for macromodel i slew-rate nonlinearity.
G_{IN}	Diagonal matrix of operational amplifier input admittances.
R_O	Diagonal matrix of operational amplifier output resistances.
$F^{(i)}(j\omega)$	Complex impedance function defined for amplifier macromodel i.

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I. Introduction

THE INTEGRATED circuit operational amplifier is a fundamental component in the realization of a wide class of active circuits. Due to the internal complexity of

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