Digital IC Comprehensive Experiment Report

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Experiment Name: 16-bit High-Speed Adder Design

Experiment Objective

Familiarize with digital integrated circuit design and simulation methods to implement functional circuits.

Experiment Content

- First, complete the circuit design and simulation of a **16-bit Ripple Carry Adder (RCA)** as a reference circuit and measure the **maximum delay time** as the speed benchmark for this experiment.
- Design a **16-bit high-speed adder** and achieve a speed improvement of more than **2x** through optimization of **adder structure, circuit design, and device sizing**.

Experiment Steps

1. Construct the 16-bit Ripple Carry Adder (RCA) circuit

- Simulate and measure the **maximum delay**.

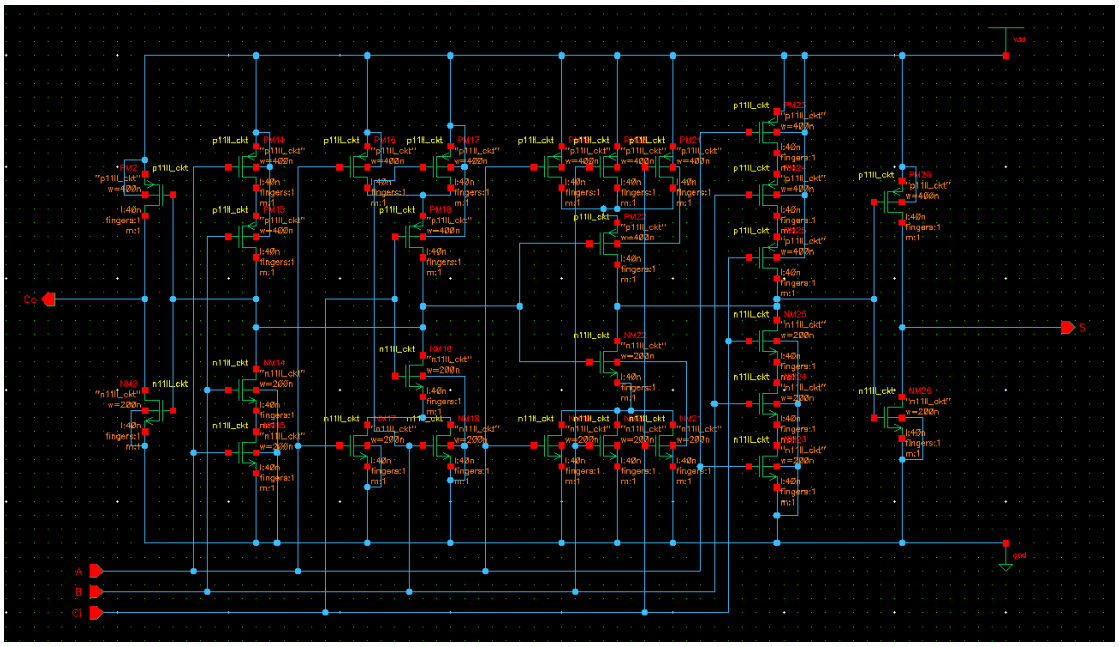
2. Design a 16-bit High-Speed Adder (Carry Select Adder)

- Modify the MOS transistor sizes in the full adder so that **all MOS transistors have W/L = 200n/40n**.
- Connect the modified full adders in series to form a **4-bit RCA**.
- Construct a **MUX**, where **all PMOS have W/L = 200n/40n** and **all NMOS have W/L = 120n/40n**, used for selection.
- Use **two 4-bit RCAs** and **five MUXes** (for selecting **S0, S1, S2, S3, and Co**) to form a **4-bit Carry Select Adder**, with the **Ci of the two 4-bit RCAs connected to VDD and GND, respectively**.
- Use **three 4-bit Carry Select Adders and one 4-bit RCA** to construct a **16-bit Carry Select Adder**.
- Measure the **maximum delay**.
- **Draw the layout**.

- **Perform post-layout simulation** to verify correct functionality.

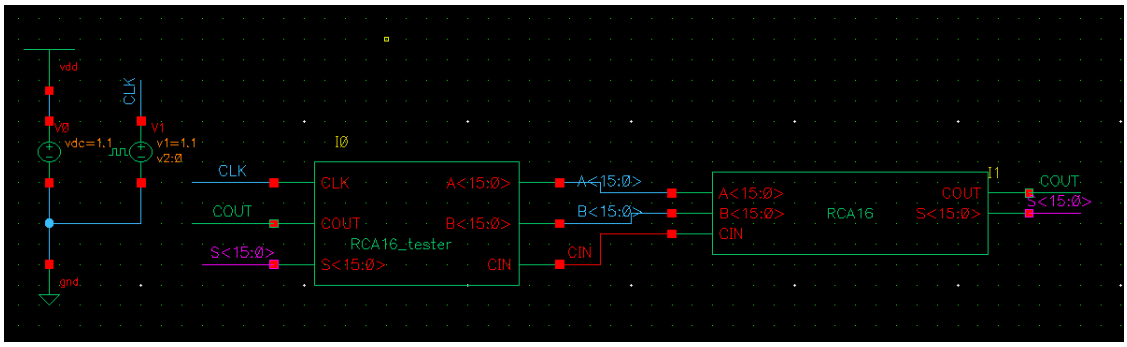
Experiment Results & Analysis

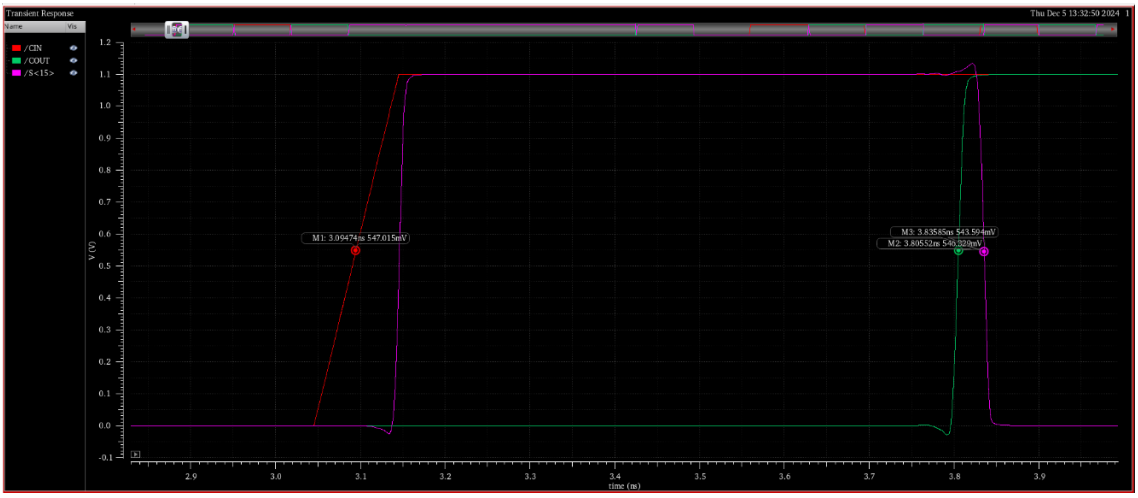
1. Full Adder



- **All PMOS:** W/L = **400n/40n**
- **All NMOS:** W/L = **200n/40n**

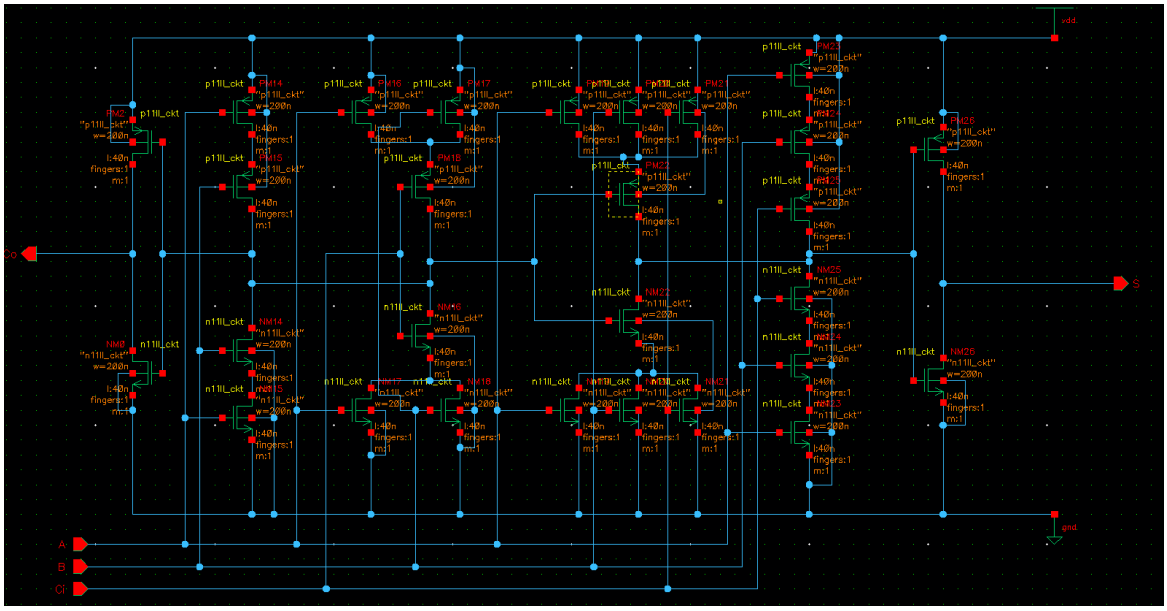
2. RCA Test Circuit & Maximum Delay Measurement



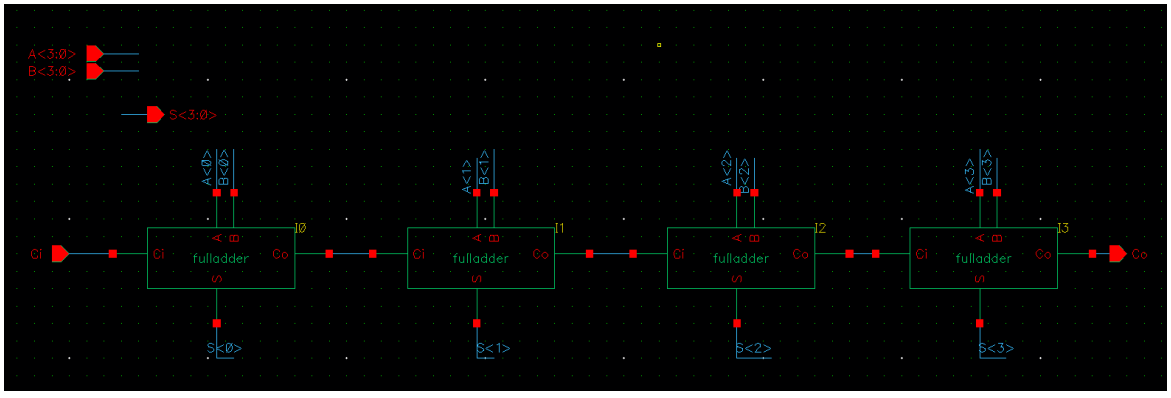


- Measured Maximum Delay:
  - 3.83585 ns - 3.09474 ns = 0.7411 ns = 741.1 ps

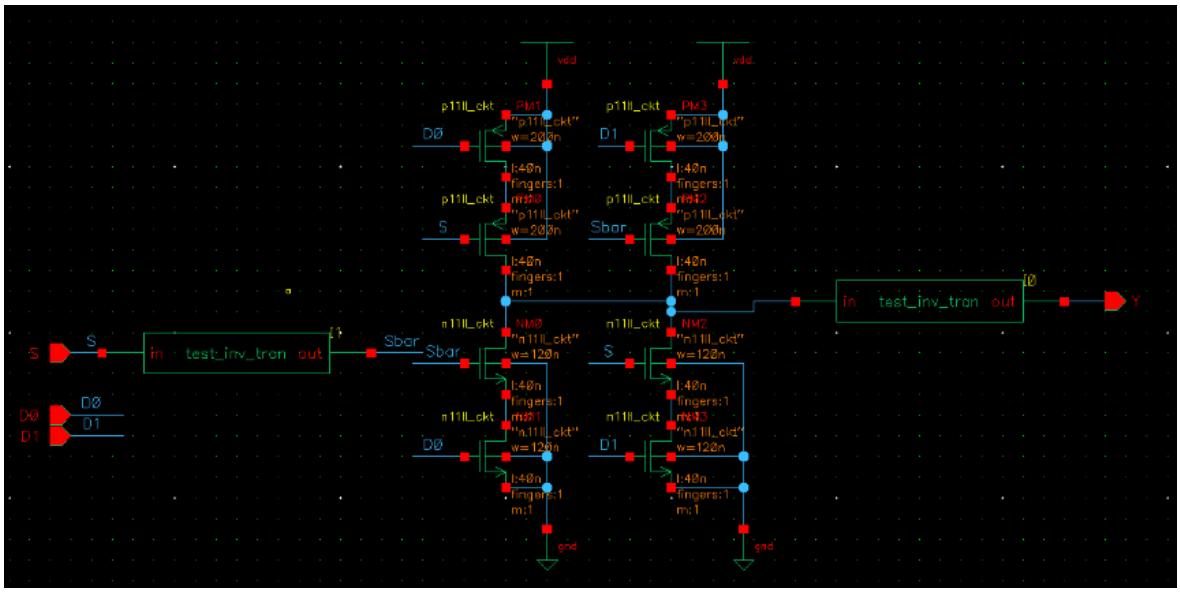
3. Modified Full Adder (Circuit connections remain unchanged)



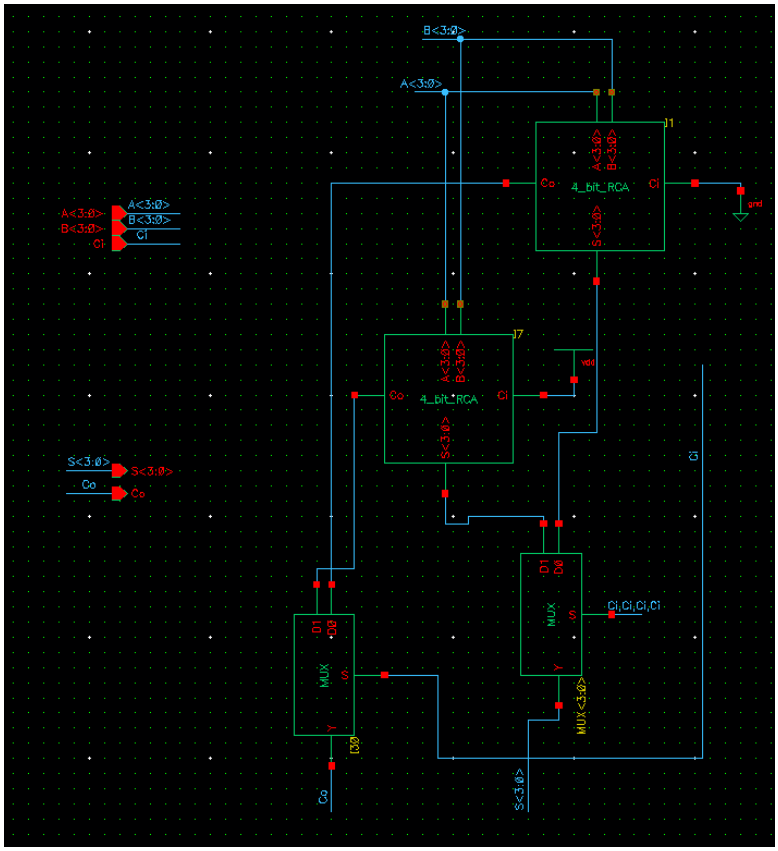
- Constructed **4-bit RCA circuit**



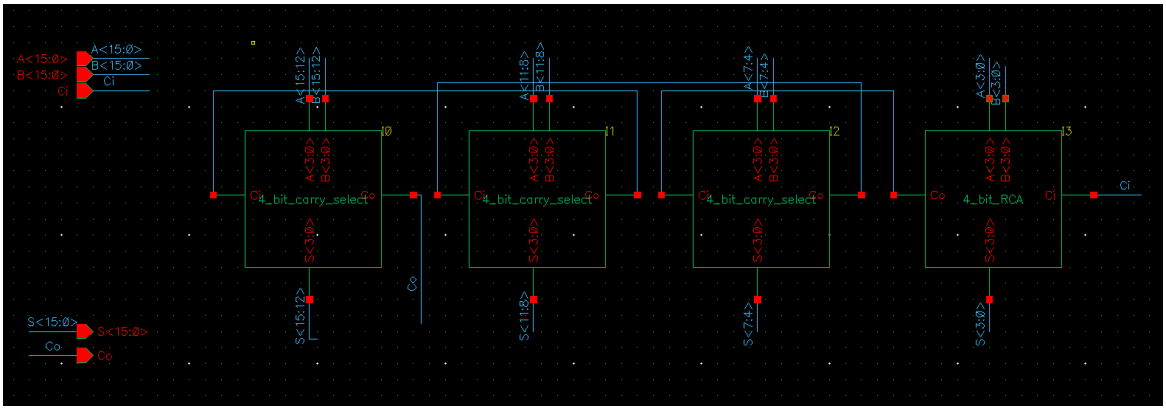
- Designed **MUX circuit**



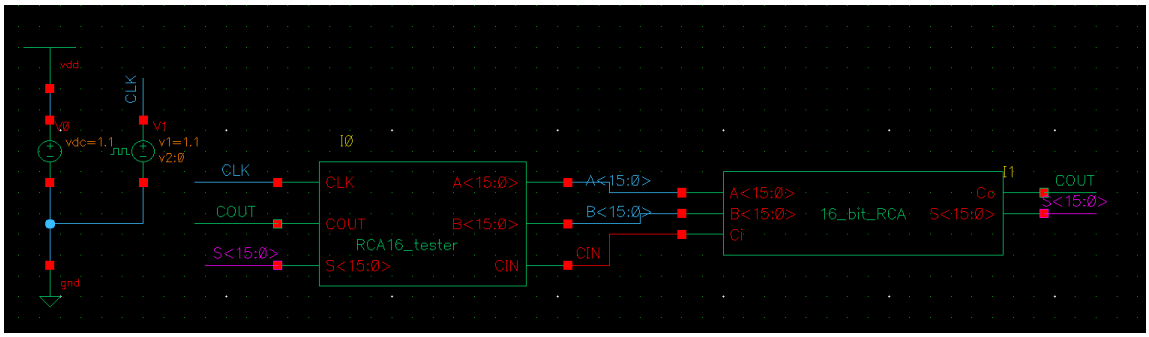
- Built **4-bit Carry Select Adder using 4-bit RCA and MUX**



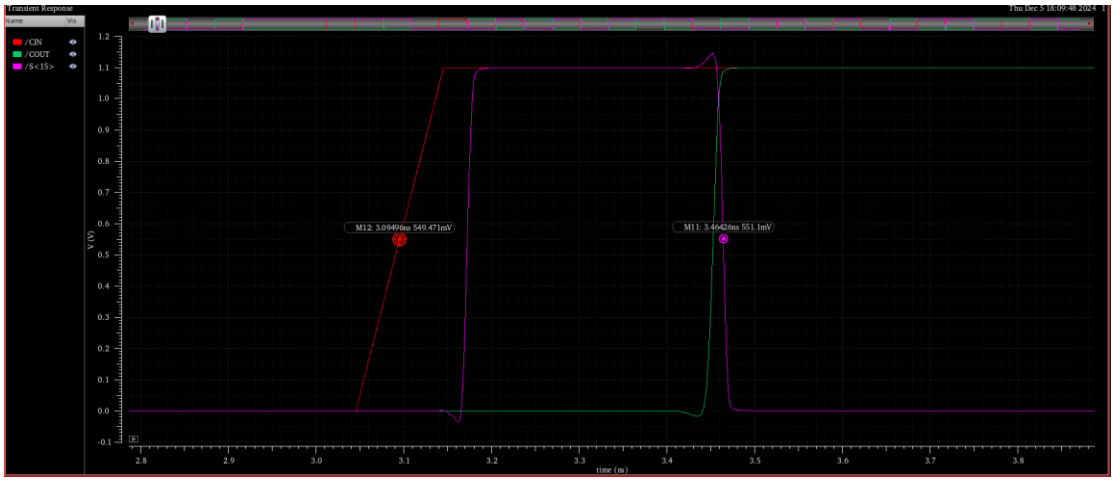
- Connected **one 4-bit RCA and three 4-bit Carry Select Adders** to form a **16-bit Carry Select Adder**



4. Optimized Circuit & Pre-layout Simulation Results



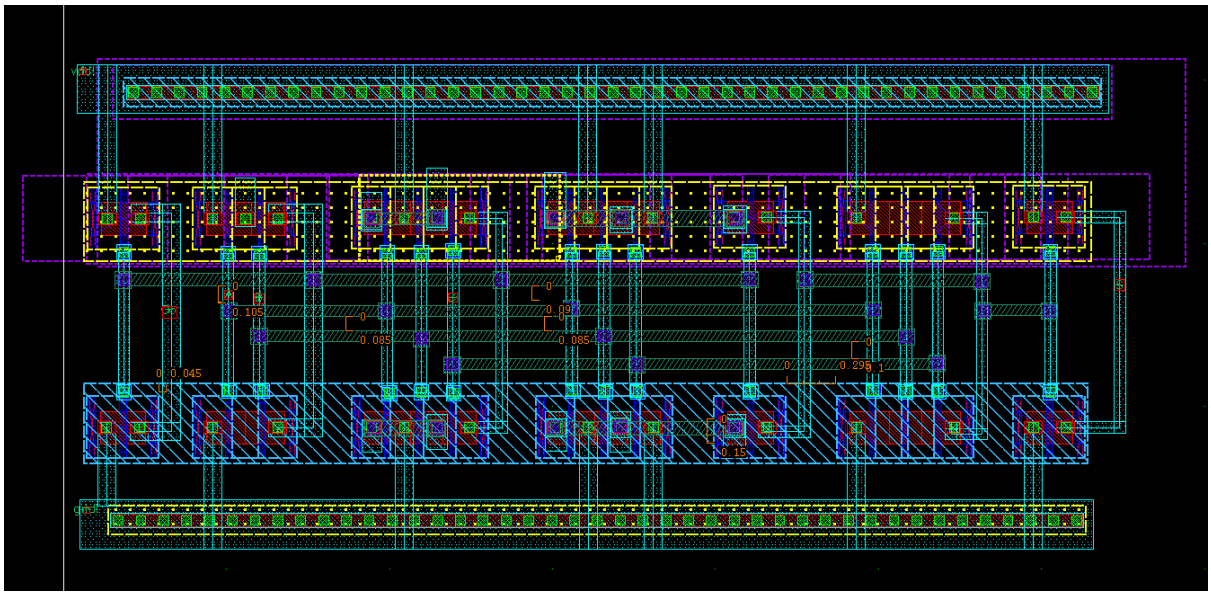
- Optimized Pre-layout Delay Measurement:



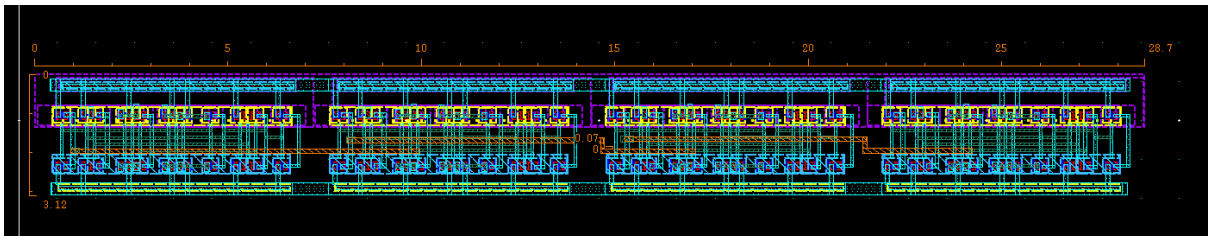
  - 3.4642 ns - 3.09496 ns = 0.3692 ns = 369.2 ps
  - This meets the design goal: 369.2 ps < (741.1 ps / 2) = 370.55 ps

5. Layout Design

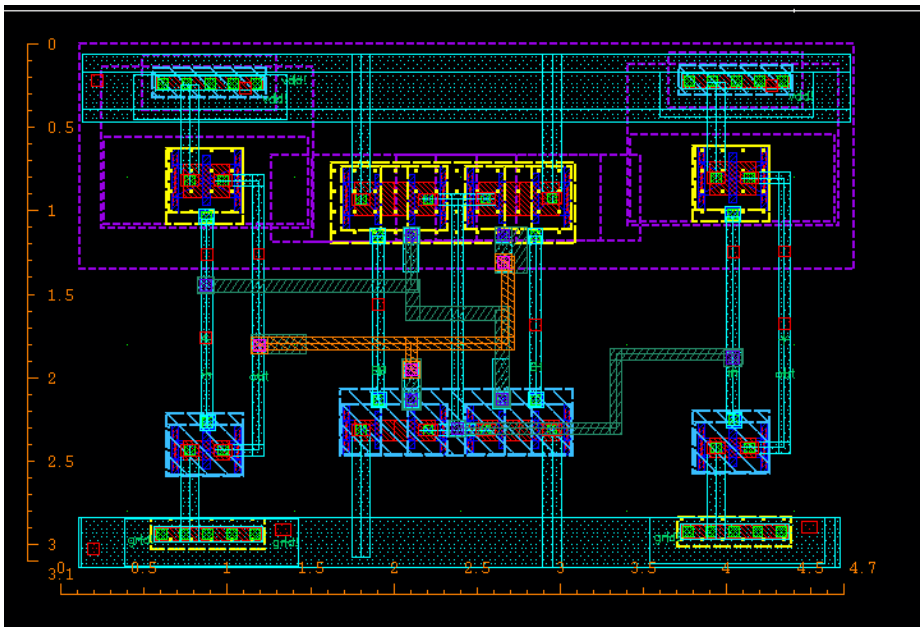
- Full Adder Layout



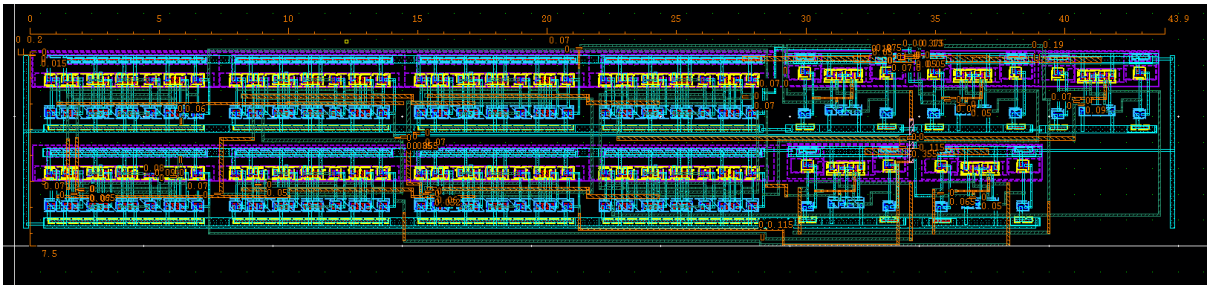
- 4-bit RCA Layout



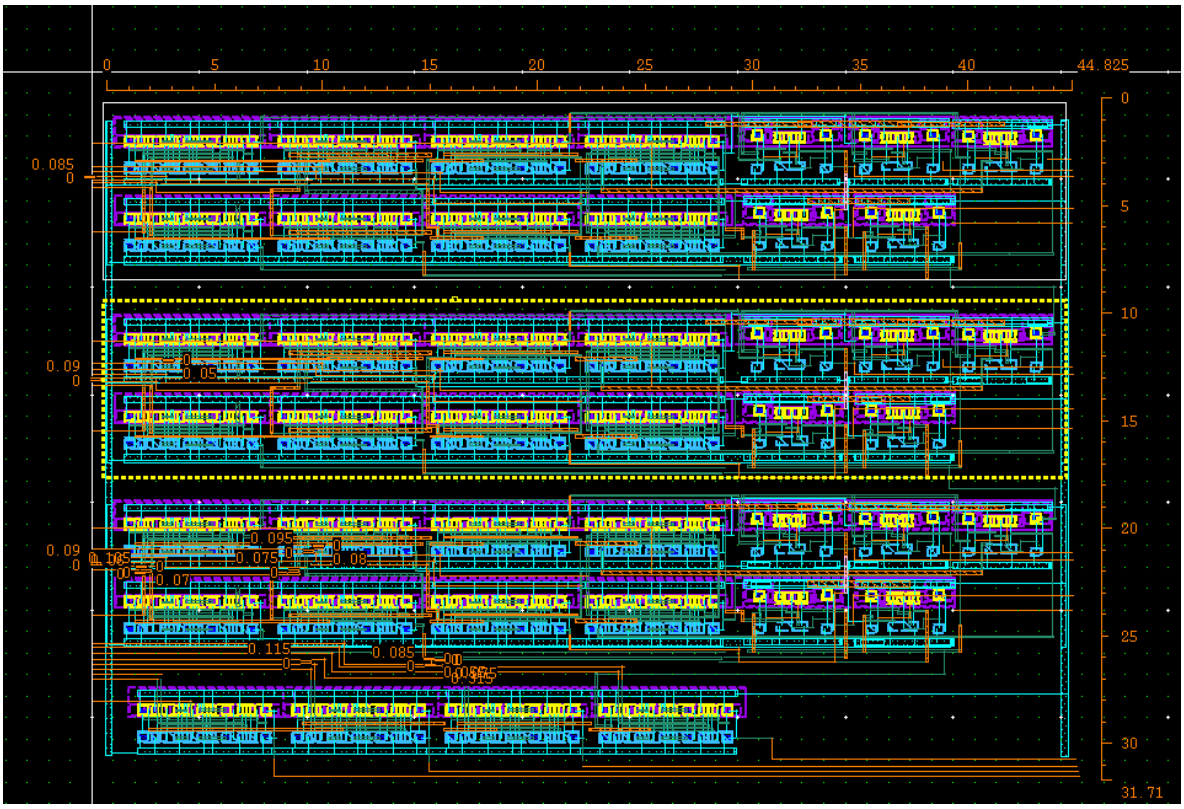
- MUX Layout



- 4-bit Carry Select Adder Layout



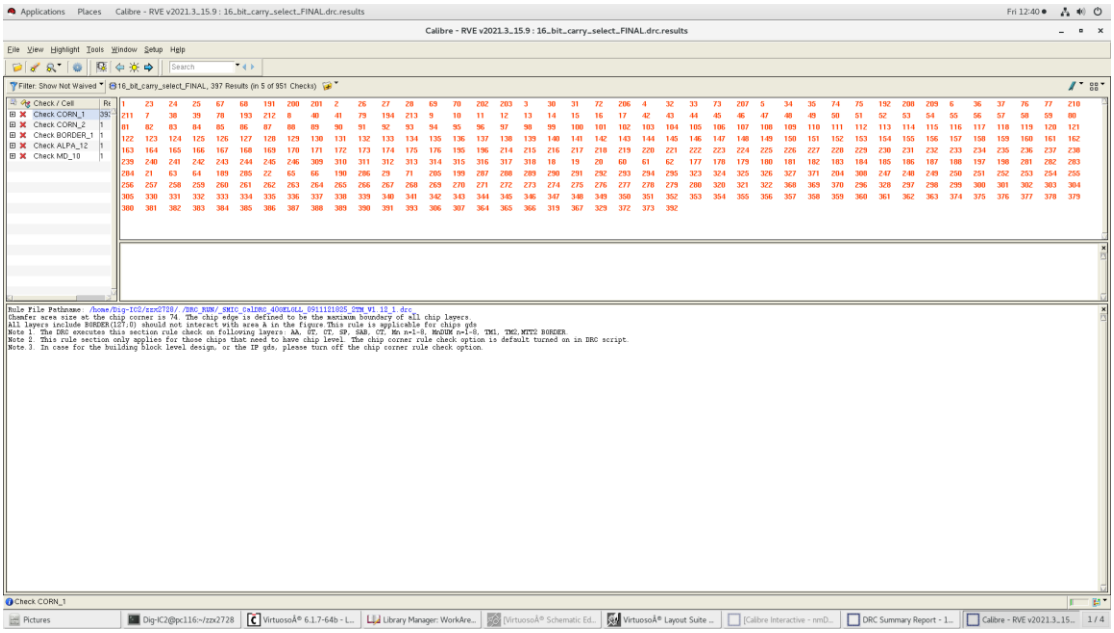
- 16-bit Carry Select Adder Layout



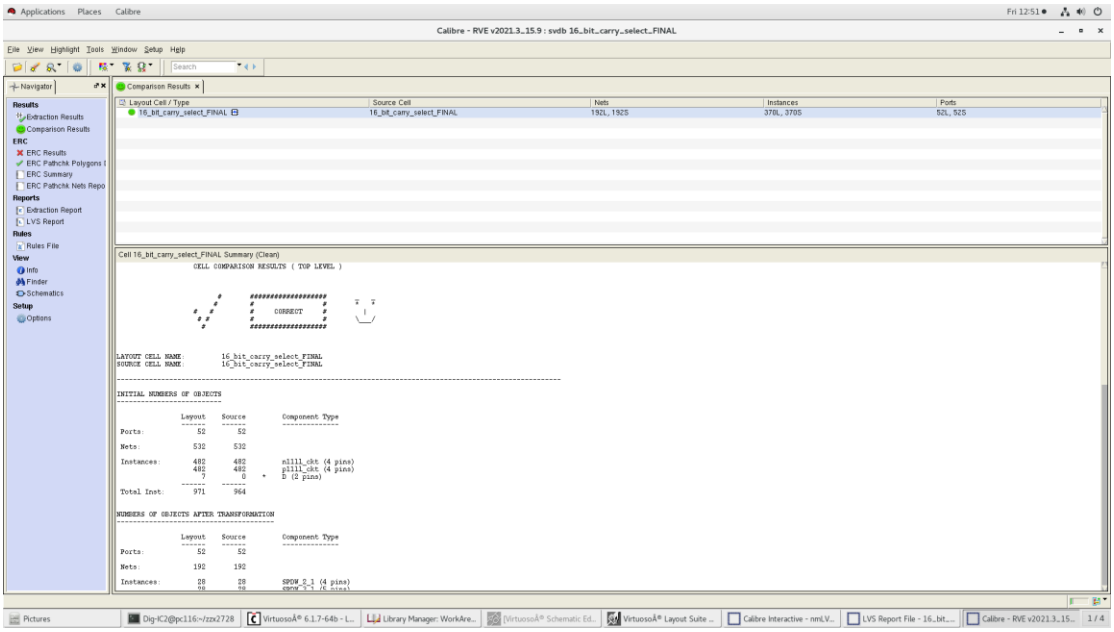
- Input connections from the left, output connections from the right
- Overall layout aspect ratio: 44.825 µm / 31.71 µm, meeting the requirements

6. Design Rule Check (DRC) & Layout vs. Schematic (LVS) Results

- DRC Passed

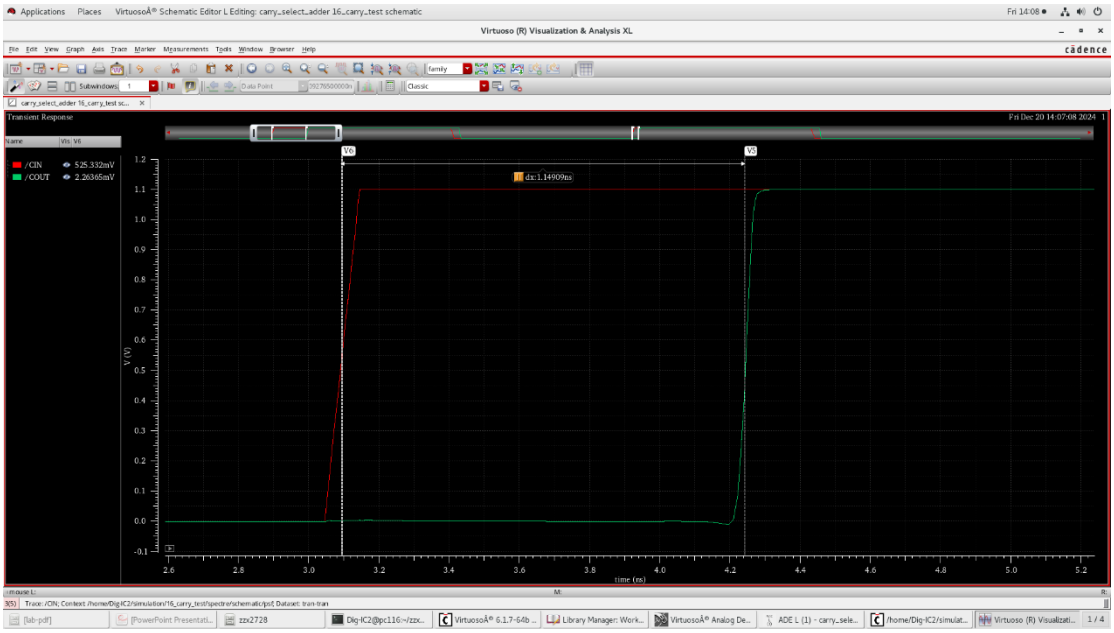


- LVS Passed



7. Post-layout Simulation & Final Validation

- Delay Analysis Post-layout:




```
    tran: time = 814.4 ps    (4.07 %), step = 400 ps          (2 %)
    tran: time = 1.614 ns    (8.07 %), step = 400 ps          (2 %)
    tran: time = 2.722 ns    (13.6 %), step = 307.8 ps      (1.54 %)
[3.04501 ns] A     0 + B     0 + CIN 0 = sum1      0 |      0 sum2 = S     0 + CO      0
 ---------  error_count =     0
    tran: time = 3.503 ns    (17.5 %), step = 3.597 ps       (18 m%)
    tran: time = 4.554 ns    (22.8 %), step = 63.81 ps      (319 m%)
    tran: time = 5.696 ns    (28.5 %), step = 369 ps        (1.84 %)
    tran: time = 6.791 ns      (34 %), step = 400 ps          (2 %)
    tran: time = 7.591 ns      (38 %), step = 400 ps          (2 %)
    tran: time = 8.711 ns    (43.6 %), step = 319.4 ps       (1.6 %)
[9.04501 ns] A     0 + B 65535 + CIN 1 = sum1  65536 |  65536 sum2 = S     0 + CO  65536
 ---------  error_count =     0
    tran: time = 9.502 ns    (47.5 %), step = 6.53 ps      (32.7 m%)
    tran: time = 10.55 ns    (52.7 %), step = 159.6 ps      (798 m%)
    tran: time = 11.73 ns    (58.7 %), step = 265.6 ps      (1.33 %)
    tran: time = 12.77 ns    (63.8 %), step = 388.2 ps      (1.94 %)
    tran: time = 13.57 ns    (67.8 %), step = 400 ps          (2 %)
    tran: time = 14.7 ns     (73.5 %), step = 330.3 ps      (1.65 %)
[15.045 ns] A 10482 + B 17931 + CIN 0 = sum1  28413 |  28413 sum2 = S 28413 + CO      0
 ---------  error_count =     0
    tran: time = 15.51 ns    (77.5 %), step = 10.28 ps     (51.4 m%)
    tran: time = 16.56 ns    (82.8 %), step = 235.3 ps      (1.18 %)
    tran: time = 17.69 ns    (88.5 %), step = 400 ps          (2 %)
    tran: time = 18.79 ns      (94 %), step = 400 ps          (2 %)
    tran: time = 19.59 ns      (98 %), step = 400 ps          (2 %)
Number of accepted tran steps =             633

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.

Initial condition solution time: CPU = 763.769 ms, elapsed = 763.787 ms.
Intrinsic tran analysis time:    CPU = 23 s, elapsed = 23.0613 s.
Total time required for tran analysis `tran': CPU = 23.9862 s, elapsed = 24.0476 s.
Time accumulated: CPU = 25.632 s, elapsed = 25.8819 s.
```

- **The design functions correctly, and the error count is zero.**

Conclusion

The **16-bit Carry Select Adder** achieved over **2x speed improvement** compared to the **Ripple Carry Adder**, successfully meeting the experimental goals. The design was verified through **circuit simulation, layout verification (DRC, LVS), and post-layout validation**, confirming that the high-speed adder performs correctly.