Digital Circuit Design Homework Report

Inverter, NAND, and NOR Gates Design and Simulation

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Contents

1 Introduction

This homework provides a comprehensive introduction to digital CMOS circuit design, combining layout design, circuit extraction, and functional verification. Throughout the assignment, three fundamental CMOS designs—inverter, NOR, and NAND—are implemented at the layout level. The layout design is completed using the Magic VLSI layout tool, while NGSpice is employed for circuit simulation, allowing for accurate validation of each design. This hands-on approach ensures a deeper understanding of both physical design principles and the electrical behavior of CMOS circuits.

2 Design

2.1 Inverter Design

In designing the inverter layout, general CMOS design rules were followed to ensure proper functionality and manufacturability. Key considerations included:

- Placing the n-diffusion (**ndiff**) region in the p-type substrate for the nMOS transistor and the p-diffusion (**pdiff**) region in the n-well for the pMOS transistor.
- Using contacts (**ncontact** for ndiff and **pcontact** for pdiff) to connect diffusion regions to the metal1 layer, enabling electrical connectivity.
- Connecting the gates of both transistors using polysilicon (**poly**) to form the input, adhering to standard inverter design practices.
- Ensuring appropriate spacing and alignment according to general design rules to prevent layout errors and facilitate fabrication.

2.2 NAND Design

For the NAND gate layout, similar general design principles were applied:

- Arranging ndiff and pdiff regions for nMOS and pMOS transistors according to the NAND gate configuration.
- Utilizing contacts to link diffusion regions with metal layers, ensuring reliable connections.
- Connecting the poly gates to form inputs A and B, maintaining proper spacing for signal integrity.
- Following standard design rules for layer placement and spacing to ensure the circuit operates correctly.

2.3 NOR Design

In the NOR gate layout design, the focus was on general design guidelines:

- Positioning ndiff and pdiff regions appropriately for the nMOS and pMOS transistors as per the NOR gate structure.

- Employing contacts to connect diffusion areas with metal layers.
- Connecting poly gates to inputs A and B, ensuring they are correctly spaced and aligned.
- Adhering to general design rules for spacing and layer placement to avoid fabrication issues and ensure functionality.

2.4 Important

In our design, the pMOS transistors are sized at 8 / 2 8/2 lambda (width/length), while the nMOS transistors are sized at 4 / 2 4/2 lambda. This deliberate sizing addresses the difference in carrier mobility between electrons and holes. Since pMOS transistors (which use holes as charge carriers) have lower mobility compared to nMOS transistors (which use electrons), they are inherently slower. By increasing the width of the pMOS transistors, we allow more current to flow, effectively compensating for their slower speed. This ensures that both pMOS and nMOS transistors switch at comparable speeds, synchronizing their operation. As a result, the rise and fall times of the output signals are balanced, enhancing the overall performance and reliability of the CMOS circuits.

3 Layout Design

3.1 Inverter Design

The layout design spans a total of 100 lambda, with component spacing carefully defined to ensure optimal performance and reliability:

- **Metal1 to Poly spacing:** 1 lambda
- **Poly spacing:** 2 lambda
- **Metal1 spacing:** 4 lambda
- **Ground (GND) layer spacing:** 8 lambda
- **Supply (VDD) layer spacing:** 8 lambda

The GND and VDD layers are assigned a spacing of 8 lambda to improve voltage stability, thereby safeguarding against potential overvoltage conditions.

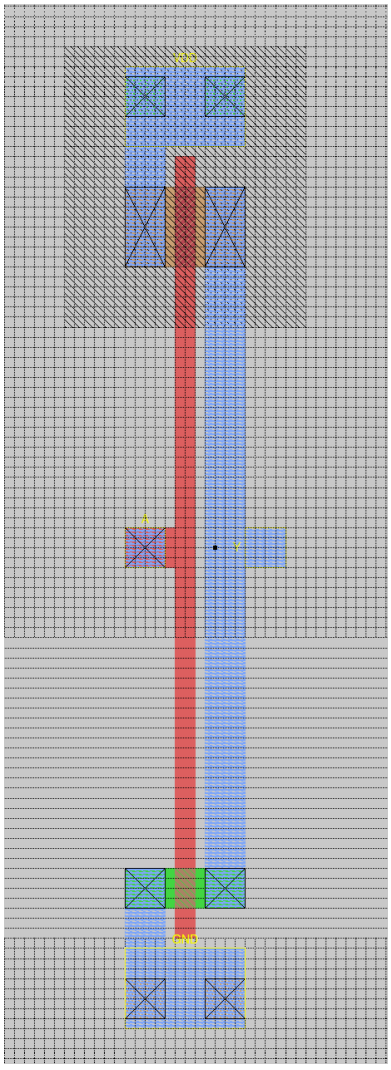

Figure 1: Inverter Layout Design

3.2 NAND Design

The layout design for the NAND gate spans a total of 100 lambda, with precise component spacing to ensure optimal performance and reliability:

- **Metal1 to Poly spacing:** 1 lambda
- **Poly spacing:** 2 lambda
- **Metal1 spacing:** 4 lambda
- **Ground (GND) layer spacing:** 8 lambda
- **Supply (VDD) layer spacing:** 8 lambda
- **Poly to Poly spacing:** 4 lambda

As in the inverter design, the GND and VDD layers are spaced at 8 lambda to enhance voltage stability, offering protection against potential overvoltage conditions and ensuring accurate voltage values throughout the circuit.

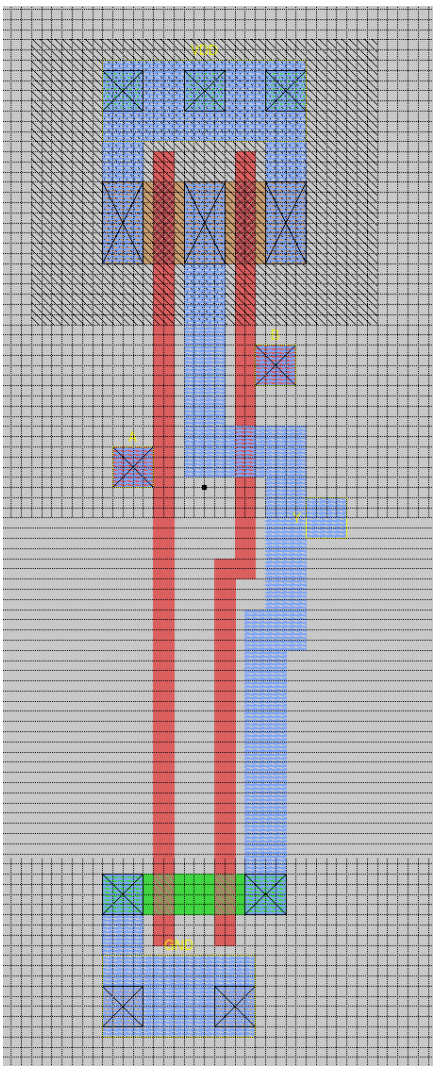

Figure 2: NAND Layout Design

3.3 NOR Design

The layout design for the NOR gate spans a total of 100 lambda, with carefully defined component spacing to maintain optimal performance and circuit reliability:

- **Metal1 to Poly spacing:** 1 lambda
- **Poly spacing:** 2 lambda
- **Metal1 spacing:** 4 lambda
- **Ground (GND) layer spacing:** 8 lambda
- **Supply (VDD) layer spacing:** 8 lambda
- **Poly to Poly spacing:** 4 lambda

The GND and VDD layers are set with an 8 lambda spacing to ensure stable voltage levels, providing protection against potential overvoltage conditions and promoting accurate voltage values across the circuit.

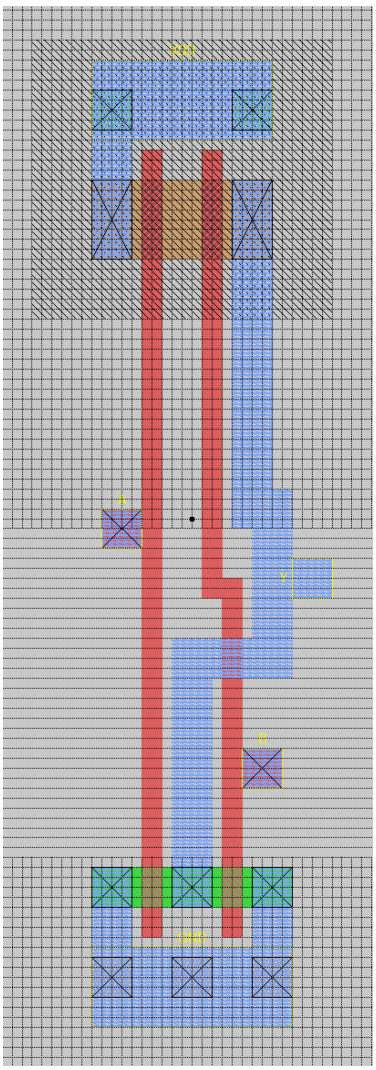

Figure 3: NOR Layout Design

4 Simulation

4.1 Inverter Simulation

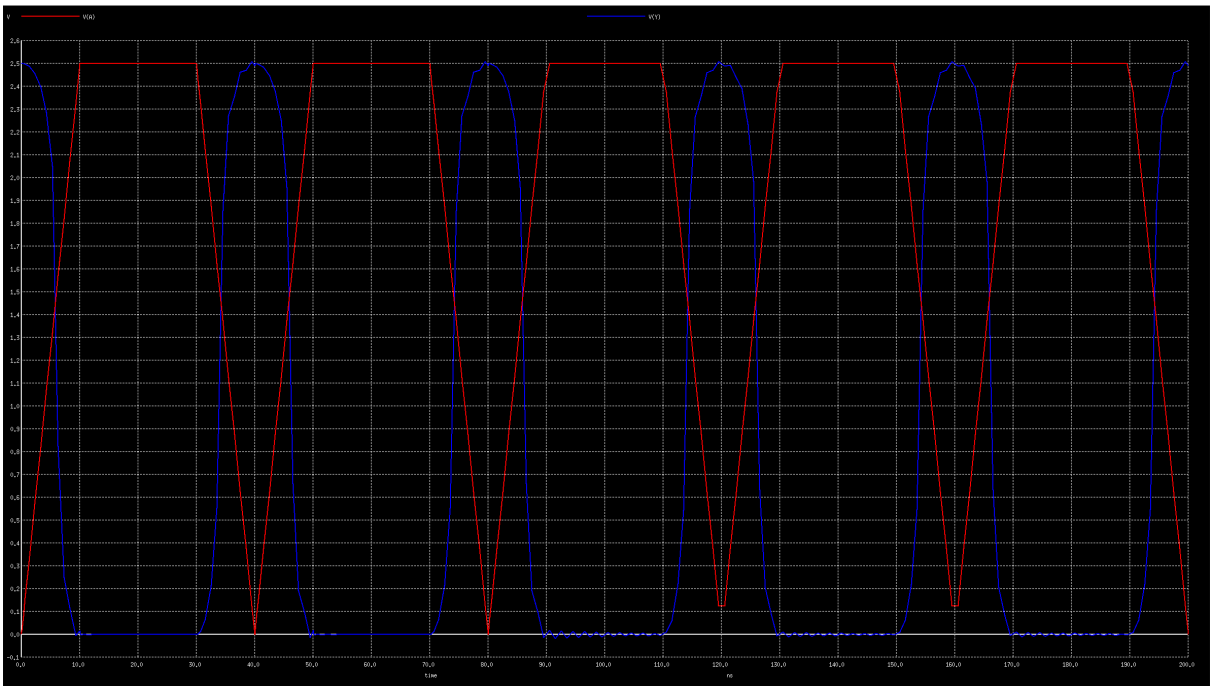

Figure 4: Inverter Simulation

The Inverter simulation waveform above shows the voltage behavior at the input and output nodes over time in an inverter circuit. The blue waveform $V(X)$ represents the input voltage, oscillating between high and low levels. The orange waveform $V(Y)$ indicates the output voltage, which is the inverted signal of the input, maintaining a high level when the input is low and dropping to a low level when the input is high. This behavior is consistent with the functionality of an inverter gate, providing a logical NOT operation. The calculated parameters $dx = 1.03704\,\text{ns}$ and $dy = 0.00106383\,\text{V}$ represent the time and voltage differences, respectively, used to determine the slope of the waveform at specific points, which indicates the switching speed of the inverter.

Input (V(X))	**Output (V(Y))**
0	1
1	0

Table 1: Inverter Gate Truth Table

The truth table above provides a summary of the expected output values for each input state in an inverter gate. Here, "0" represents a low voltage (logic 0), and "1" represents a high voltage (logic 1). The table confirms that the inverter output is the opposite of the input, as reflected in the simulated waveforms.

4.2 NAND Simulation

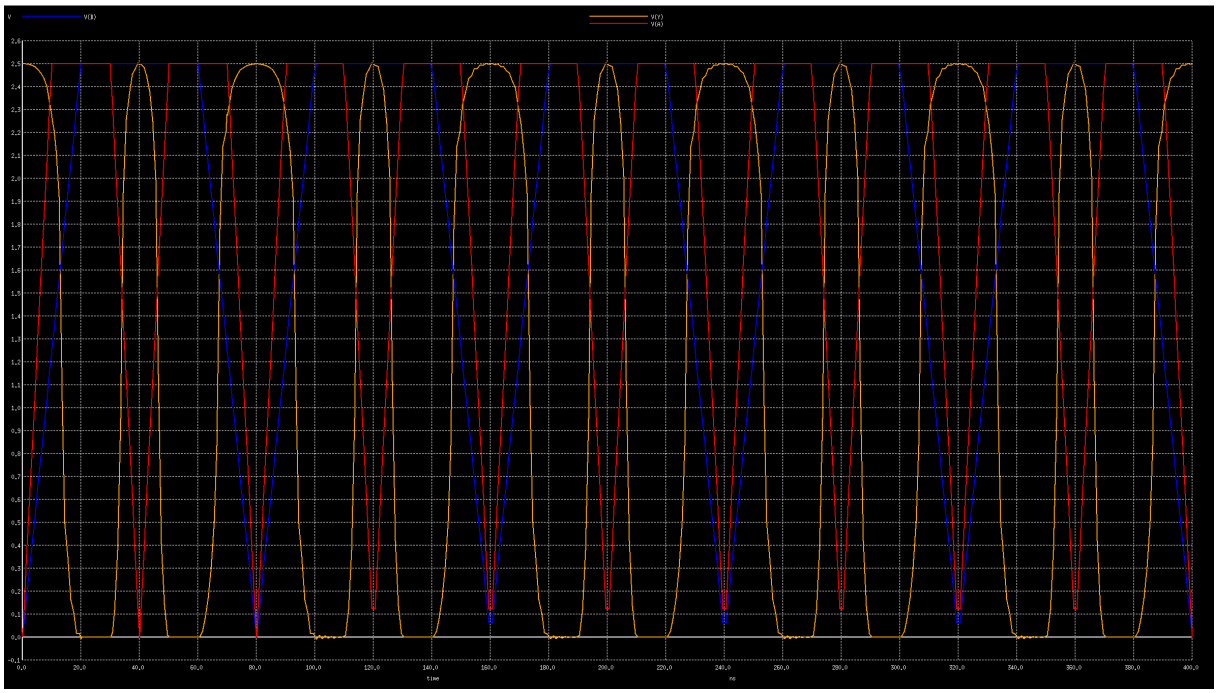

Figure 5: NAND Simulation

The NAND simulation waveform above shows the voltage variations at different nodes over time in a NAND gate circuit. The blue waveform $V(X)$ represents the voltage at one of the input nodes, while the red waveform $V(Y)$ shows the voltage at the second input. Both signals alternate between high and low levels, allowing observation of all input combinations. The orange waveform $V(Z)$ indicates the output voltage of the NAND gate, which remains high unless both inputs are high, in which case it drops to a low level, consistent with NAND gate behavior. The calculated parameters $dx = 1.41791\,\text{ns}$ and $dy = -0.000735294\,\text{V}$ represent the time and voltage differences, respectively, used to find the slope of the waveform at specific points, indicating the switching speed of the gate.

Input A (V(X))	**Input B (V(Y))**	**Output (V(Z))**
0	0	1
0	1	1
1	0	1
1	1	0

Table 2: NAND Gate Truth Table

The truth table above provides a summary of the expected output values for each input combination in a NAND gate. Here, "0" represents a low voltage (logic 0), and "1" represents a high voltage (logic 1). The table confirms that the NAND gate output is only low when both inputs are high, as reflected in the simulated waveforms.

4.3 NOR Simulation

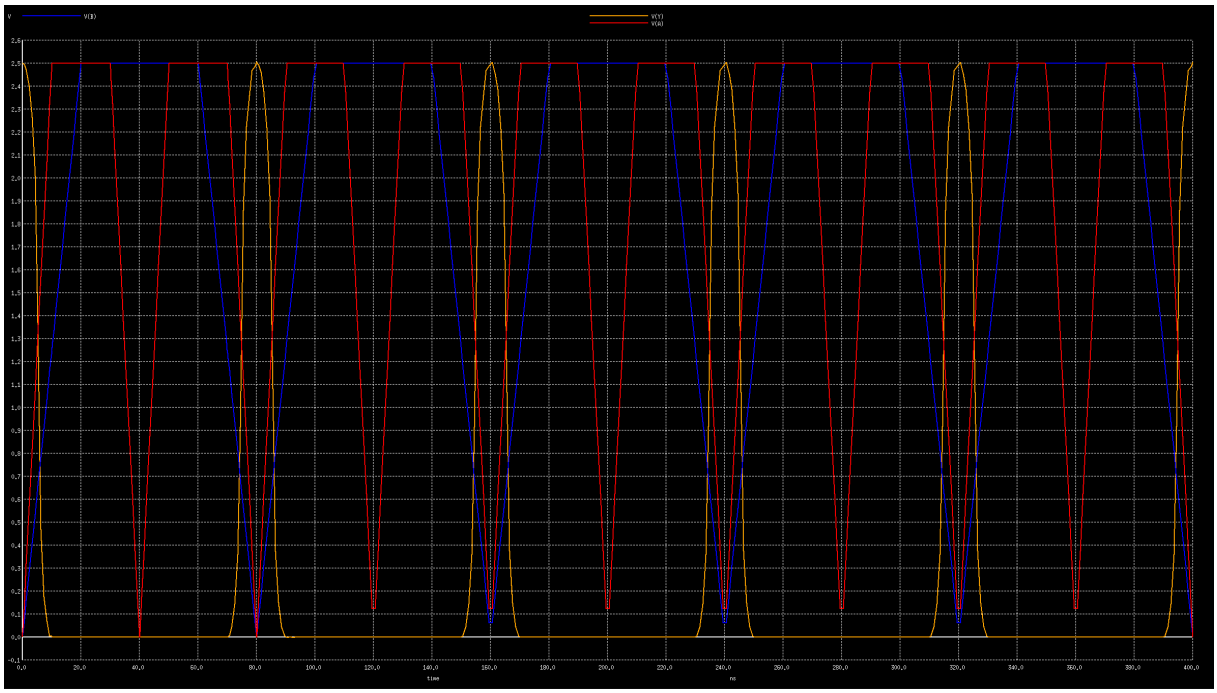

Figure 6: NOR Simulation

The NOR simulation waveform above illustrates the voltage changes at various nodes over time in a NOR gate circuit. The blue waveform $V(X)$ represents the voltage at one of the input nodes, while the red waveform $V(Y)$ indicates the voltage at the second input. Both inputs oscillate between high and low states, allowing all possible input combinations to be observed. The orange waveform $V(Z)$ displays the output voltage of the NOR gate, which remains low unless both inputs are low, in which case it rises to a high level, consistent with NOR gate functionality. Calculated parameters $dx = 3.73134\,\text{ns}$ and $dy = 0.000425532\,\text{V}$ denote the time and voltage differences, respectively, used to determine the waveform slope at certain points, reflecting the switching speed of the NOR gate.

Input A (V(X))	**Input B (V(Y))**	**Output (V(Z))**
0	0	1
0	1	0
1	0	0
1	1	0

Table 3: NOR Gate Truth Table

The truth table above summarizes the expected output values for each input combination in a NOR gate. Here, "0" represents a low voltage (logic 0), and "1" represents a high voltage (logic 1). This table confirms that the NOR gate output is only high when both inputs are low, as demonstrated by the simulated waveforms.