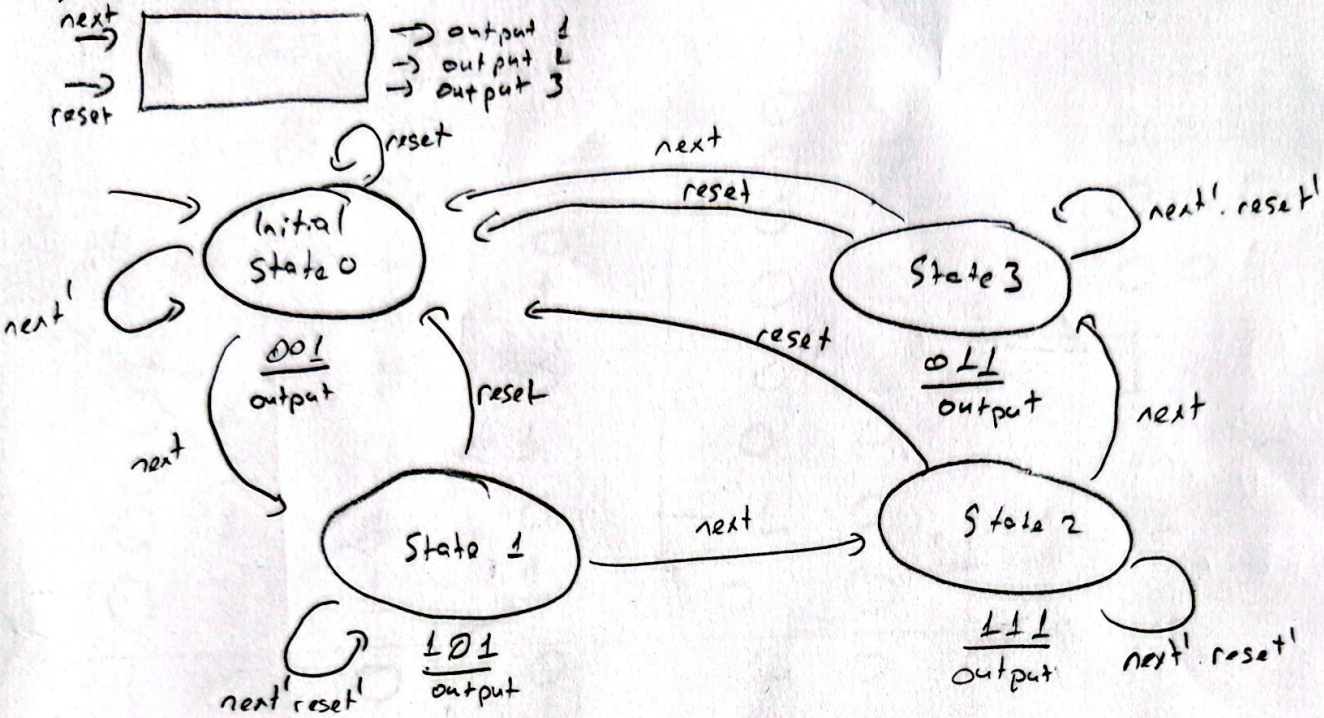
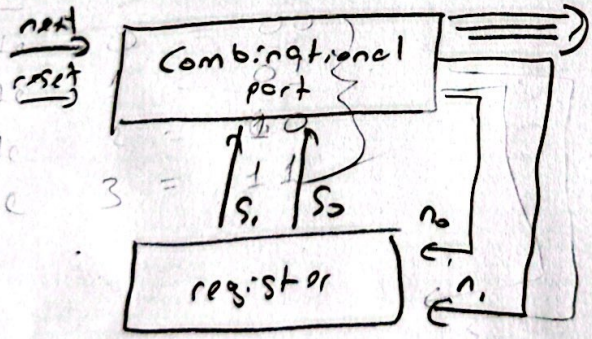
3bit Sequence Displayer

1) Draw FSM



2) Create architecture

we need a 2bit register because we have 4states.



3) Encode the states

State 0 = 00
State 1 = 01
State 2 = 10
State 3 = 11

4) Create a state table

Truth Table

S_1	S_0	next	reset	n_1	n_0	$q_1 (q_2) q_3$ 3 bit output
0	0	0	0	0	0	0 0 1
0	0	0	1	0	0	0 0 1
0	0	1	0	0	1	0 0 1
0	0	1	1	0	0	0 0 1
0	1	0	0	0	1	1 0 1
0	1	0	1	0	0	1 0 1
0	1	1	0	1	0	1 0 1
0	1	1	1	0	0	1 0 1
1	0	0	0	1	0	1 1 1
1	0	0	1	0	0	1 1 1
1	0	1	0	1	1	1 1 1
1	0	1	1	0	0	1 1 1
1	1	0	0	1	1	0 1 1
1	1	0	1	0	0	0 1 1
1	1	1	0	0	0	0 1 1
1	1	1	1	0	0	0 1 1
1	1					

$Q_1 = S_0 S_1' + S_1 S_0' = Q_1 = \underline{S_1 \oplus S_0}$ $\quad Q_2 = S_1 \quad Q_3 = 1$

Kmap for n_1

$S_1 S_0$ \ next reset	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

$n_1 = S_1 \cdot next' reset' + S_1 \cdot S_0' next \cdot reset' + S_0 \cdot S_1' \cdot next \cdot reset'$

$n_1 = S_1 \cdot next \cdot reset' + next \cdot reset' (S_1 \oplus S_0)$

Kmap for n_0

$S_1 S_0$ \ next reset	00	01	11	10
00				1
01	1			
11	1			1
10	1			1

$n_0 = S_0 \cdot next' reset' + S_1' \cdot S_0' \cdot next \cdot reset' + S_1 \cdot S_0' \cdot next \cdot reset'$

$n_0 = S_0 \cdot next' \cdot reset' + next \cdot reset' (S_1' \cdot S_0' + S_1 \cdot S_0')$

$n_0 = S_0 \cdot next' \cdot reset' + next \cdot reset' (S_0' (S_1 + S_1'))$

$n_0 = S_0 \cdot next' \cdot reset' + next \cdot reset' (S_0' \cdot 1)$

$n_0 = S_0 \cdot next' \cdot reset' + next \cdot reset' (S_0')$