Computer Archetecture Midterm

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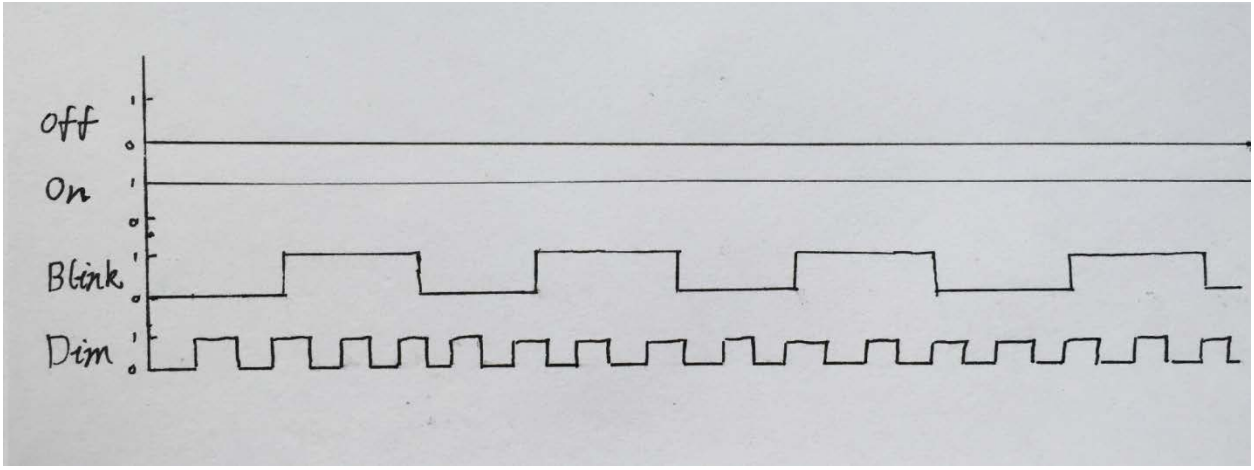
Specification Document

- Inputs and Outputs

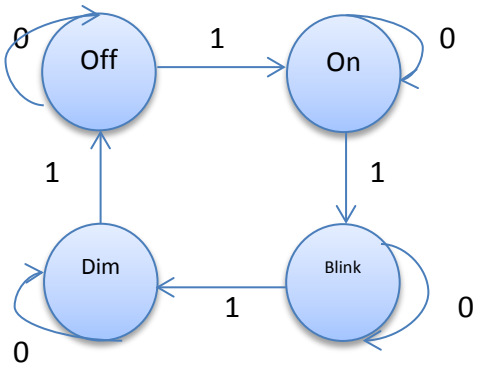
  There is one input and one output for the bike light. The single input is a button that is used to change between different operational modes. The output is a LED which performs different behaviors based on the input to the system.

- Operational Modes

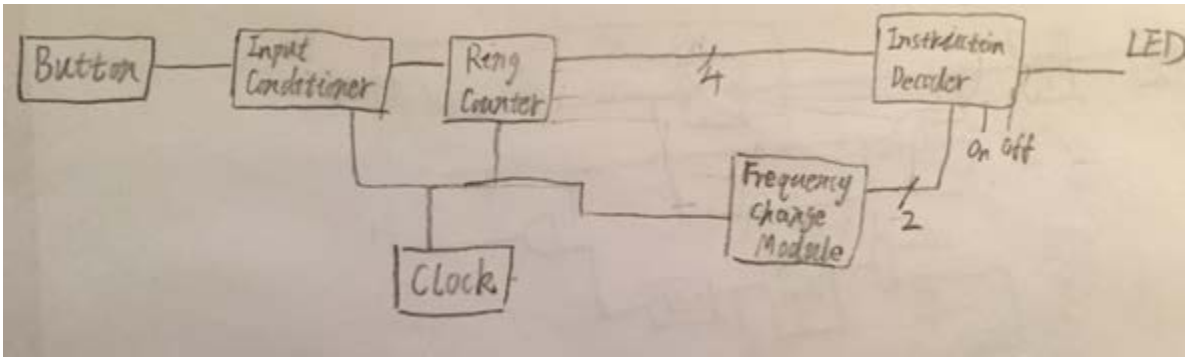


  As shown as above, the system output is in the cycle of four modes:
  - Off: the LED is turned off.
  - On: the LED is turned on at normal brightness.
  - Blink: the LED is blinking between on and off at 1.8Hz.
  - Dim: the LED is turned on at a light brightness.

- FSM

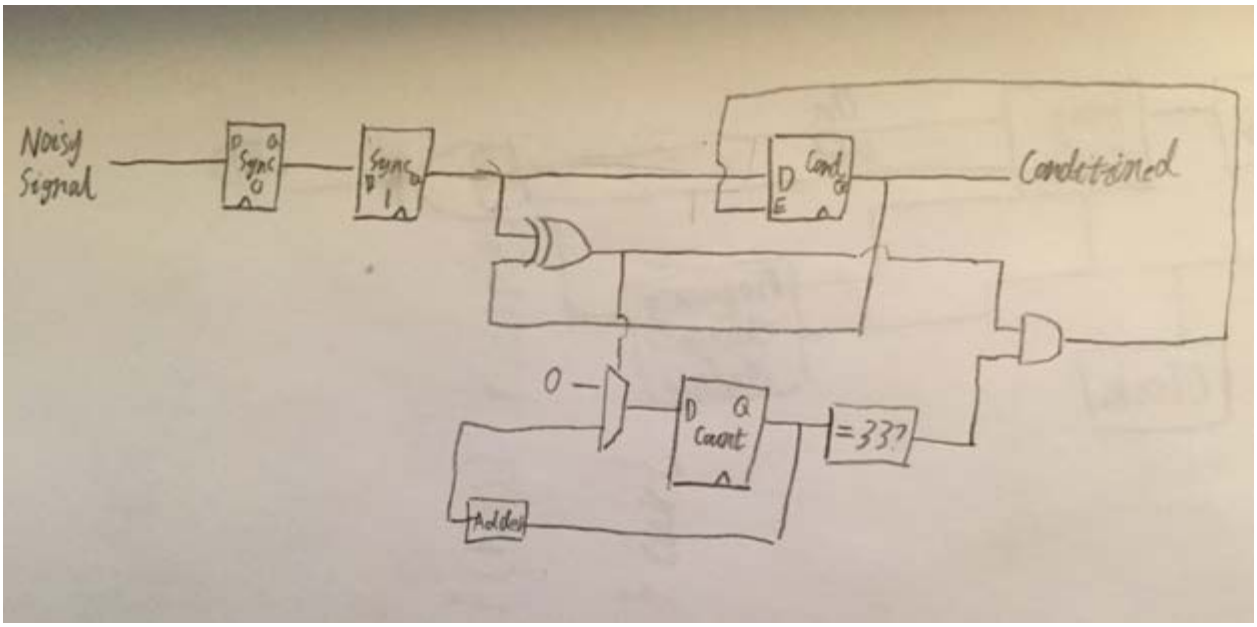


Block Diagram



Schematic

Input Conditioner



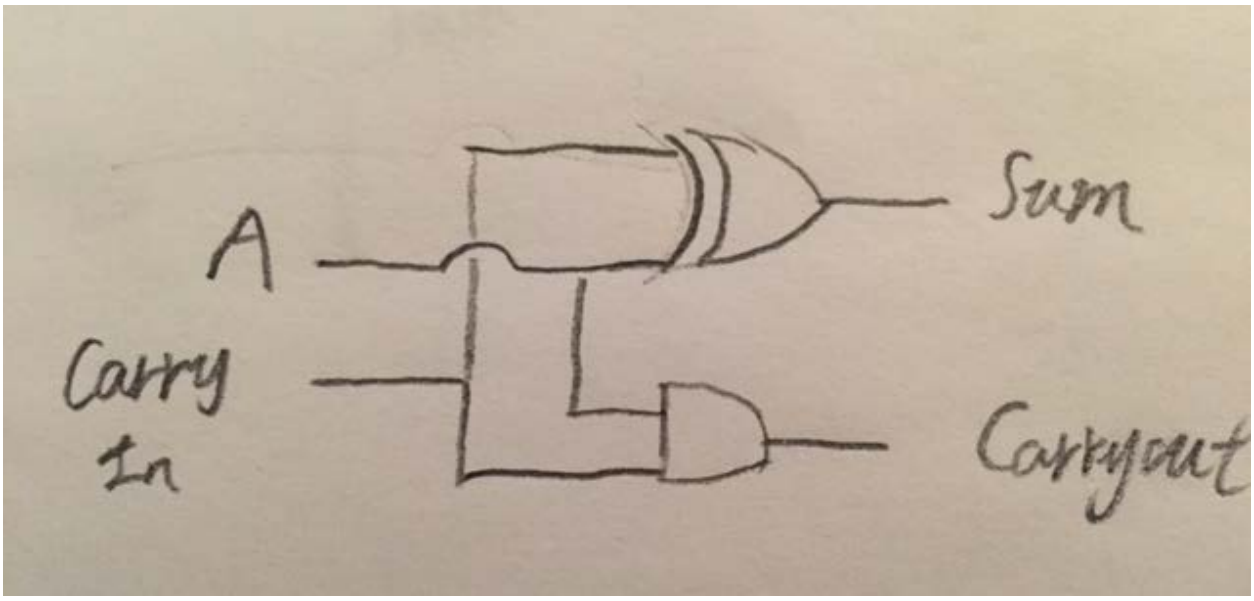
- Specification
  The input conditioner buffers the noisy signal (button press) in 33 clock cycles and outputs a smooth signal.
- Inputs
  - 1 bit noisy signal
  - clock
- Output

- 1 bit stable signal

- Cost

Name	Number	Cost
D Flip Flop	4	4*13=52
6 Bit Adder	1	36
2-1 Mux	1	7
2-1 And	1	3
Check 33	1	6
2-1 XOR	1	3
Total		117

One Bit Full Adder

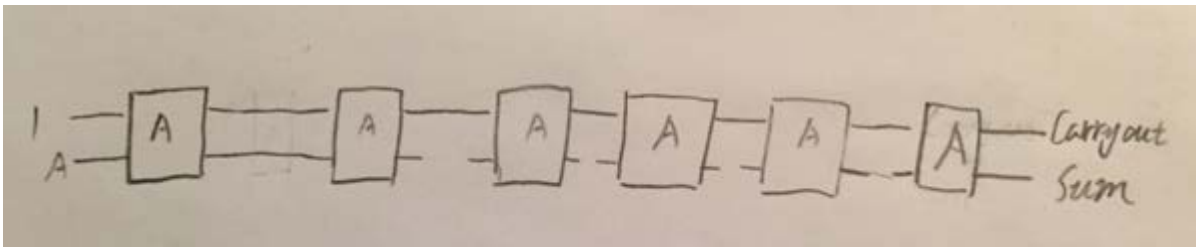


- Specification
  This one bit adder takes a one bit number and a carry-in, computes their sum and outputs the sum as well as sets the carry-out flag.
- Input
  - An one bit number
  - An one bit carry-in
- Output
  - Sum
  - Carryout
- Cost

Name	Number	Cost
2-1 AND	1	3

2-1 XOR	1	3
Total		6

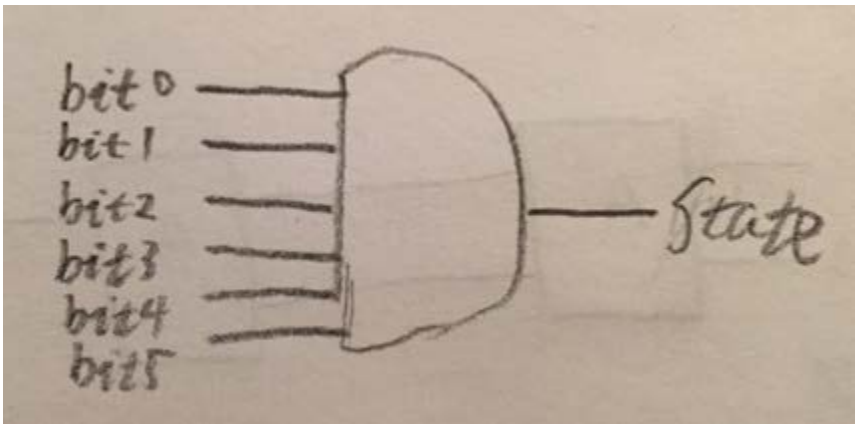
Six-Bit Full Adder



- Specification
  The 6-bit adder in the input conditioner takes in a five bit number, adds one to it and outputs the sum and carryout. It is started by adding one to the LSB.
- Input
  - o “1”
  - o A 6-bit number
- Output
  - oSum
  - oCarry-out
- Cost

Name	Number	Cost
One-bit Adder	5	6*6
Total		36

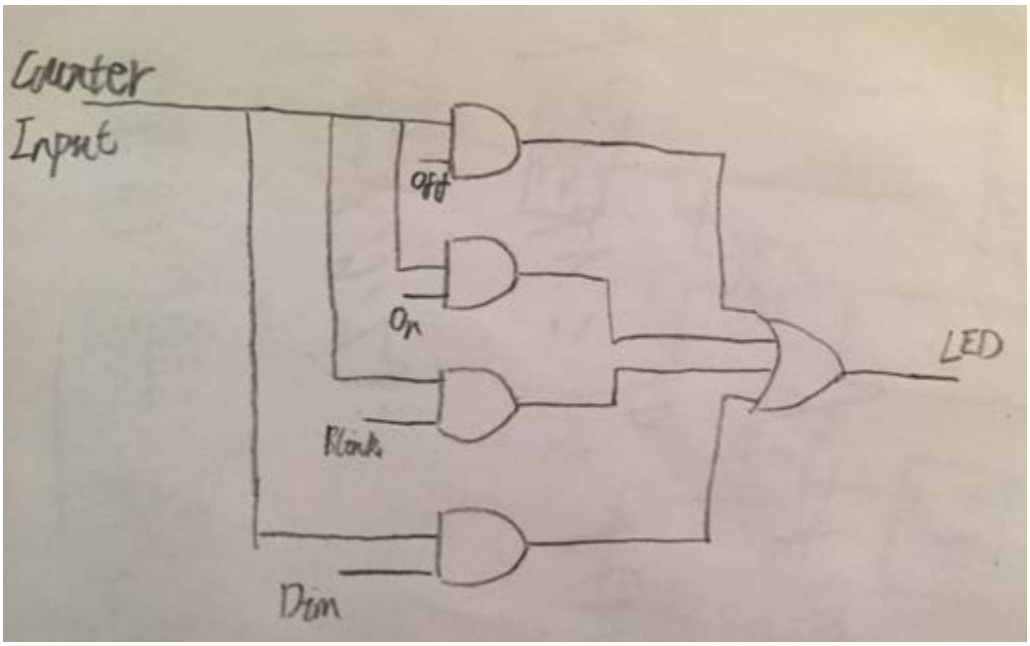
Check 33



- Specification
  Checks whether the input is 33 by comparing each bit.
- Input
  - A 6-bit number
- Output
  - State (whether is 33)
- Cost

Name	Number	Cost
6-1 AND	1	7
Total		7

Instruction Decoder



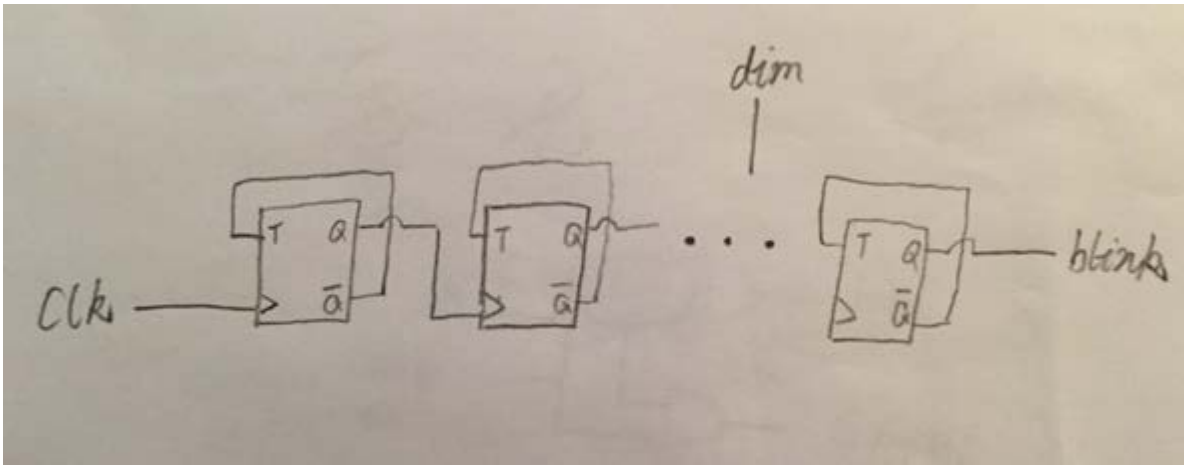
- Specification
  The decoder takes the 4-bit one-hot output from the 4-stage ring counter and selects the corresponding state of LED.
- Input
  - Four-Stage Ring Counter output
- Output

- LED Instruction

- Cost

Name	Number	Cost
2-1 AND	4	12
4-1 OR	1	5
Total		17

Frequency Change Module



- Specification
  This module uses 12 D Flip Flops to reset the frequency of the clock. Each single DFF reduce the frequency by half. Since the clock is 2^15Hz and the desired frequency for blink to be 8Hz and frequency for dim to be 128Hz, we need (2^15/8=2^12) 12 DFFs for blink and (2^15/128 = 2^8) 8 DFFs for dim.
- Input
  - Clock Signal: 2^15 Hz
- Output
  - Blink Signal: 8Hz
  - Dim Signal: 128Hz
- Cost

Name	Number	Cost
DFF	12	156
Total		156

Total Cost

Name	Number	Cost
Input Conditioner	1	117
Instruction Decoder	1	17
Frequency Changer	1	156
Four-Stage Ring Counter	1	83
Clock	1	2
Total		373