Ziyi (Jason) Lan's Homework2

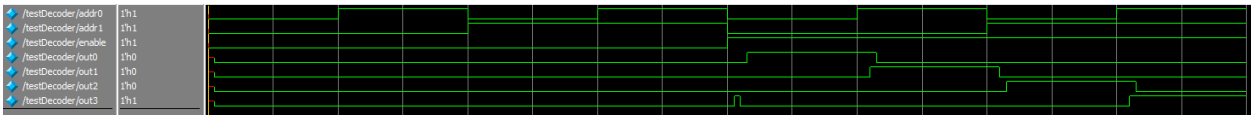
2015/09/25

Decoder

```
# vsim
# Start time: 14:26:03 on Sep 25,2015
# Loading work.testDecoder
# Loading work.structuralDecoder
# En A0 A1| O0 O1 O2 O3 | Expected Output
# 0  0  0 |  0  0  0  0 | All false
# 0  1  0 |  0  0  0  0 | All false
# 0  0  1 |  0  0  0  0 | All false
# 0  1  1 |  0  0  0  0 | All false
# 1  0  0 |  1  0  0  0 | O0 Only
# 1  1  0 |  0  1  0  0 | O1 Only
# 1  0  1 |  0  0  1  0 | O2 Only
# 1  1  1 |  0  0  0  1 | O3 Only
# 0 ns
# 8400 ns
```

```
# vsim
# Start time: 14:28:23 on Sep 25,2015
# Loading work.testDecoder
# Loading work.behavioralDecoder
# En A0 A1| O0 O1 O2 O3 | Expected Output
# 0  0  0 |  0  0  0  0 | All false
# 0  1  0 |  0  0  0  0 | All false
# 0  0  1 |  0  0  0  0 | All false
# 0  1  1 |  0  0  0  0 | All false
# 1  0  0 |  1  0  0  0 | O0 Only
# 1  1  0 |  0  1  0  0 | O1 Only
# 1  0  1 |  0  0  1  0 | O2 Only
# 1  1  1 |  0  0  0  1 | O3 Only
# 0 ns
# 8400 ns
```

Above are the truth tables for a 2-bit decoder with enable (2+1 inputs, 4 outputs), the left one is test bench for my version of the device and the right on is the test bench for the general functionality of the device.



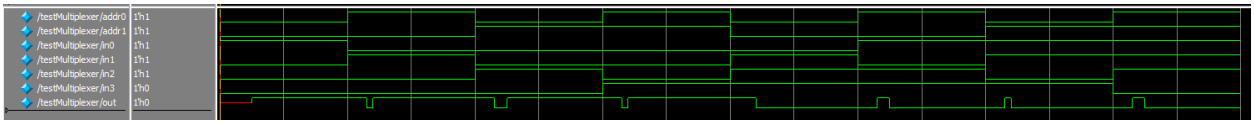
This is the wave form for 8000 ns, we can clearly see the effect of 50 units delay on each of the gate. Also there is one little noise on the out3 wave; its occurred time implicates that it's due to the shift of state of addr0, addr1 and enable.

Multiplexer

```
# vsim
# Start time: 14:29:27 on Sep 25,2015
# Loading work.testMultiplexer
# Loading work.structuralMultiplexer
#
#
# Truth Table for Multiplexer
# A0 A1| I0 I1 I2 I3 | Output  | Expected Output
# 0  0 |  1  0  0  0 | 1       |  1
# 1  0 |  0  1  0  0 | 1       |  1
# 0  1 |  0  0  1  0 | 1       |  1
# 1  1 |  0  0  0  1 | 1       |  1
# 0  0 |  0  1  1  1 | 0       |  0
# 1  0 |  1  0  1  1 | 0       |  0
# 0  1 |  1  1  0  1 | 0       |  0
# 1  1 |  1  1  1  0 | 0       |  0
# 0 ns
# 8400 ns
```

```
# vsim
# Start time: 14:31:20 on Sep 25,2015
# Loading work.testMultiplexer
# Loading work.behavioralMultiplexer
#
#
# Truth Table for Multiplexer
# A0 A1| I0 I1 I2 I3 | Output  | Expected Output
# 0  0 |  1  0  0  0 | 1       |  1
# 1  0 |  0  1  0  0 | 1       |  1
# 0  1 |  0  0  1  0 | 1       |  1
# 1  1 |  0  0  0  1 | 1       |  1
# 0  0 |  0  1  1  1 | 0       |  0
# 1  0 |  1  0  1  1 | 0       |  0
# 0  1 |  1  1  0  1 | 0       |  0
# 1  1 |  1  1  1  0 | 0       |  0
# 0 ns
# 8400 ns
```

These are the truth tables for a 4:1 (four input Multiplexor), the left one is test bench for my version of the device and the right on is the test bench for the general functionality of the device.

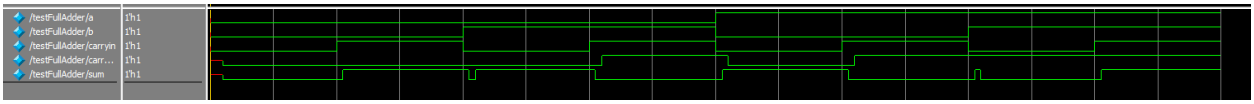


As we can see from the wave from above, there is delay before the "out" line is gets any signal, that's due to the delays on the gates in the circuit. Also the noise arisen from input rising/dropping on the "out" line is apparent.

One-bit adder

```
# vsim
# Start time: 14:32:53 on Sep 25,2015
# Loading work.testFullAdder
# Loading work.structuralFullAdder
# a  b| Cin Cout | Sum | Expected Output
# 0  0 | 0     0 |   0 |  0
# 0  0 | 1     0 |   1 |  1
# 0  1 | 0     0 |   1 |  1
# 0  1 | 1     1 |   0 |  0
# 1  0 | 0     0 |   1 |  1
# 1  0 | 1     1 |   0 |  0
# 1  1 | 0     1 |   0 |  0
# 1  1 | 1     1 |   1 |  1
# 0 ns
# 8400 ns
```

```
# vsim
# Start time: 14:34:26 on Sep 25,2015
# Loading work.testFullAdder
# Loading work.behavioralFullAdder
# a  b| Cin Cout | Sum | Expected Output
# 0  0 | 0     0 |   0 |  0
# 0  0 | 1     0 |   1 |  1
# 0  1 | 0     0 |   1 |  1
# 0  1 | 1     1 |   0 |  0
# 1  0 | 0     0 |   1 |  1
# 1  0 | 1     1 |   0 |  0
# 1  1 | 0     1 |   0 |  0
# 1  1 | 1     1 |   1 |  1
# 0 ns
# 8400 ns
```



These are truth tables and waveform for a one-bit Full Adder. Similar to the previous two cases, we can observe the noise and time delay from the output on the waveform.