CS 2200 Homework 3

Fall 2018

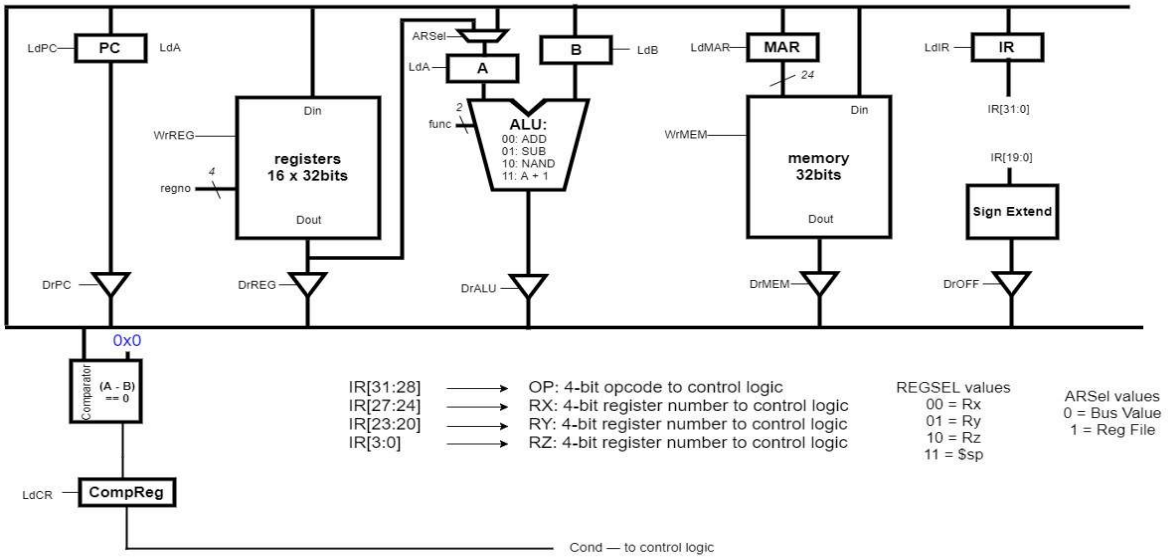
Rules:

- Print a copy of the assignment and hand-write your answers. No electronic submissions are allowed.
- Print as one double-sided sheet. There will be a 30 point penalty if you don't.
- You may discuss concepts with your classmates but not the answers.
- Due Date: September 19th – 6:00 PM in recitation. Bring your BuzzCard.

Name:_____ GT Username:_____ Section: ____

*The modified datapath below is **ONLY** used for question 1.*

LC-2300 Datapath



The above is the datapath of the **LC-2300**, a modified version of LC-2200. **Notice the extra MUX in front of the ALU "A" register.**

1. Write out the microstates for a more efficient **LW** and **SW** using the modifications on the LC-2300 datapath. For each microstate, give the control signals used (see the example). Signals irrelevant to the state can be omitted and will be assumed to be zero. **You will lose points for an inefficient answer!**

ADD (example)	**LW**	**SW**
ADD0: DrREG, LdA, RegSel=01 **ADD1:** DrREG, LdB, RegSel=10 **ADD2:** DrALU, WrReg, func=00, RegSel=00		

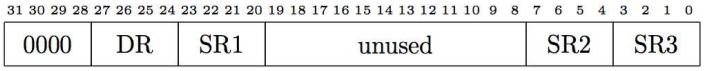
2. Briefly describe what the FETCH, DECODE, & EXECUTE phases of the FSM are used for.

   During the DECODE phase, how exactly does the processor transition from the end of the fetch macrostate to the appropriate ISA instruction? (Hint: Talk about the signals and sequencer ROM in the context of Project 1)

3. We are introducing a new instruction to **LC-2200** called ADD3 :

   ADD3 DR, SR1, SR2, SR3

   The instruction takes the source registers SR1, SR2, and SR3 and adds all three, resulting in an effective operation of DR = SR1 + SR2 + SR3. The bit layout of the instruction is as follows:



   A. In order to connect the appropriate register field in the Instruction Register (IR) to the register file, the RegSel MUX must be used. Because our ADD3 instruction contains additional register fields beyond those included in other LC-2200 instructions, the RegSel MUX must be modified. **Complete the table of inputs for the modified RegSel MUX below:**

RegSelHi	RegSelLo	Register Name	Bit Range
0	**0**	**DR**	**IR[27:24]**
0	**1**		
1	**0**		
1	**1**		

   B. **List all of the microstates needed to implement ADD3**. We have provided the first state for you. For each microstate, specify both the datapath actions as well as the control signals. You will lose points for an inefficient answer. **Note: You must specify RegSel values (for example RegSel=00)**.