08/21	Course Rules, Introduction	Chapter 1	
08/23	Processor – Design of the ISA	Chapter 2	
08/28	Processor – Calling Conventions, Datapath	Chapter 2, 3	
08/30	Processor – Microcode Control, Datapath	Chapter 3	P1 (datapath) release
09/04	Processor – Decode Step for Branch	Chapter 3	
09/06	Processor – 3 ROM Microcode Control	Chapter 3	
09/11	Interrupts	Chapter 4	
09/13	Interrupts and Performance	Chapter 4, 5	P1 due P2 (interrupts) release
09/18	Pipelining – Basic Datapath modifications	Chapter 5	
09/20	Pipelining – Hazards	Chapter 5	
09/25	Pipelining – Register Forwarding Design	Chapter 5	P2 due P3 (pipeline) release
09/27	Pipelining – Final Design	Chapter 5	
10/02	Pipelining	Chapter 5	
10/04	Test 1…		
10/09	Spring Recess		
10/11	Processor Scheduling	Chapter 6	
10/16	Processor Scheduling	Chapter 6	
10/18	Memory Management – Historic Algorithms	Chapter 7	P3 due P4 (memory) release
10/23	Memory Management – Paging	Chapter 8	
10/25	Caching	Chapter 9	
10/30	Caching	Chapter 9	
11/01	Multi-threading	Chapter 12	P4 due P5 (Process Schedule) release
11/06	Multi-threading	Chapter 12	
11/08	Networking	Chapter 13	
11/13	Networking	Chapter 13	P5 due P6 (Networking) release
11/15	Test 2		
11/20	Networking	Chapter 13	
11/22	Thanksgiving Holiday		
11/27	IO and Disks	Chapter 10	

11/29	File Systems	Chapter 11	P6 due
12/04	Final Instructional Day		