CS 2200 Homework 8

Fall 2018

Instructions:

- Please print a copy of the assignment and hand write your answers. No electronic submissions are allowed. **Please print as one double-sided page. Do NOT staple multiple sheets together. There will be a 70 point penalty if you do not.**
- This is an individual assignment. You may discuss concepts but not the answers.
- Due Date: **10/31/18 – 6:00 PM** in recitation. Bring your BuzzCard. Show up on time.

Name:_____ **GT Username:**_____ **Section:**_____

1. Average Access Time

Say we have two setups for hierarchical memory with the following miss rates and hit times:

Memory 1

Hardware	Miss Rate	Hit Time
L1 Cache	0.15	5ns
L2 Cache	0.20	10ns
Main Memory	0	85ns

Memory 2

Hardware	Miss Rate	Hit Time
L1 Cache	0.05	8ns
L2 Cache	0.10	20ns
Main Memory	0	115ns

Compute the AAT (average access time) for each setup, and show your answer below. Which setup would you choose and why?

2. Address Splitting

You are designing a cache for a 32-bit processor. Memory is organized into 4-byte words, but it is byte addressable. You have been told to make a 4-way set associative cache with 128 words (512 bytes) per block. The cache size is 128k words (512kB), excluding tag, status bits, etc.

a. Suppose the box represents the bits of a memory address. **Draw the dividing lines for tag, index, and offset (not all may applicable).** Indicate how many bits are allocated to each portion.

b. Split the following address into Tag/Index/Offset: **0xBEADFEEB**

TAG: _____

INDEX: _____

OFFSET: _____

3. Consider the following three caches, which each accept 16-bit byte-addressable memory addresses:

A. Cache size 1kB, block size 128 bytes, direct mapped
B. Cache size 2kB, block size 128 bytes, 2-way set associative
C. Cache size 4kB, block size 128 bytes, fully associative

Complete the following table showing the performance of the three caches with the same set of accesses. **For each access in the sequence, write an 'X' in each column where it's respective cache encounters a miss. Leave the space blank for a hit.** The first one has been filled in for you.

Assume the following:

- All accesses are read accesses.
- The replacement policy is LRU (least recently used), where appropriate.
- The caches are initially empty.

	Cache A	Cache B	Cache C
0x80B0	**X**		
0x80C4			
0x674C			
0x8668			
0xC754			
0x6724			
0x8644			
0x7E44			
0xC716			
0x80B5			