CS 2200 Fall 2013 Test 2

Prism ID:_____

Name:_____ GTID#: 9_____

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	15				
3	10				
4	14				
5	10				
6	10				
7	20				
8	20				
Total	100				

- **You may ask for clarification but you are ultimately responsible for the answer you write on the paper.**
- **Illegible answers are wrong answers.**
- **Please do not discuss this test by any means (until 5 pm today)**
- **Please look through the entire test before starting. WE MEAN IT!!!**

Illegible answers are wrong answers.
Good luck!

1. (1 point, 0 min) (circle one; you get a point regardless of correct/incorrect answer)
"They have the attention span of slightly moronic woodland creatures."
(a) Said President Obama about Republicans
(b) Said Linux creator Linus Torvalds about code developers
(c) Said German Chancellor Angela Merkel about the NSA
(d) Said the President of Georgia Tech about UGA students

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Pipelining

2. (15 points, 10 min)

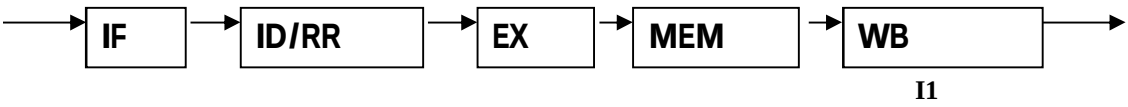
(a) (2 points)Structural hazard in a pipeline occurs due to (circle the correct choice)

(i) Branch instructions in the program
(ii) Load instructions in the program
(iii) Data dependencies in the program
(iv) Hardware limitations in the datapath

(b) Consider the following three consecutive instructions in a program in flight in a pipelined processor with **register forwarding**:

I1: R1 ⟵ R2 + R3
I2: R1 ⟵ R3 + R4
I3: R5 ⟵ R1 + R7

The state of the pipeline is:



(i) (2 points) At what stage of the pipeline are **I2** and **I3?**

(ii) (3 points) Why are **I2 and I3** where you have shown them to be?

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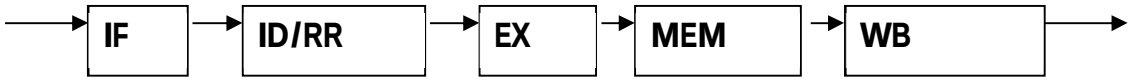
(c) Consider the following instructions in flight in a pipelined processor **with register forwarding**:

I1: R0 ← R2 + R3
I2: R3 ← R0 + R1
I3: R7 ← R3 + R9
I4: R8 ← R0 + R7
I5: R7 ← R6 + R8

The partial state of the pipeline is:



I1

(i) (2 points) At what stages of the pipeline are the other instructions?

(ii) (6 points) Recall that associated with each element of the register file are a busy bit (B) and a read pending signal (RP) as shown below. **Fill in the state of the B and RP bits** in the register file given the state of the pipeline as you have it in your answer for part (i).

		B	RP
R0			
R1			
R2			
R3			
R4			
R5			
R6			
R7			
R8			
R9			

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3. (10 points, 7 min)

(a) Given the following sequence of instructions:

```
      BEQ      L1
      ADD
      LW
      ...
L1    NAND
      SW
```

The processor uses **branch prediction** assuming the **sequential path to be the probable one.**

In the actual execution of the above code snippet, **the prediction turns out to false.**

(i) (8 points) Fill in the "waterfall diagram" below showing the progress of the above instructions through the pipeline stages.

Cycle number	IF	ID/RR	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					

(ii) (2 points)What is the observed CPI for the instructions that actually get executed (BEQ, NAND, SW)?

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Process Scheduling

4. (14 points, 5 min)

(a) (2 points) (**Select one correct choice**)
One of the following is **NOT** part of the state of a running program

1. General Purpose Registers that are visible to the instruction set
2. Program counter and the register that represents the stack pointer
3. Layout of the program in memory
4. Priority information
5. Internal registers in the datapath of the processor

(b) (4 points)
What is the difference between a “scheduler” and a “dispatcher”?

(c) (2 points) (**Select one correct choice**)
A preemptive scheduling algorithm requires

1. A trap instruction
2. An external interrupt
3. The currently running process to terminate
4. The currently running process to make an I/O request

(c) (2 points) (**Select one correct choice**)
Upon context switch, the scheduler saves the volatile state of the current process in

1. The system stack
2. The PCB for that process
3. The user stack
4. The heap space of the process

(d) (2 points) (**Select one correct choice**)
I want to know how good the system is for executing my gaming application. The metric that will help me determine this best is:

1. Throughput
2. Average waiting time
3. Average turnaround time
4. CPU Utilization
5. Response time

(e) (2 points) (**Select one correct choice**)
One of the following attributes is common to SJF and priority schedulers:

1. They are both fair
2. Both of them could lead to “starvation”
3. They both favor short running processes
4. They both lead to the best average waiting time for processes
5. They both suffer from convoy effect

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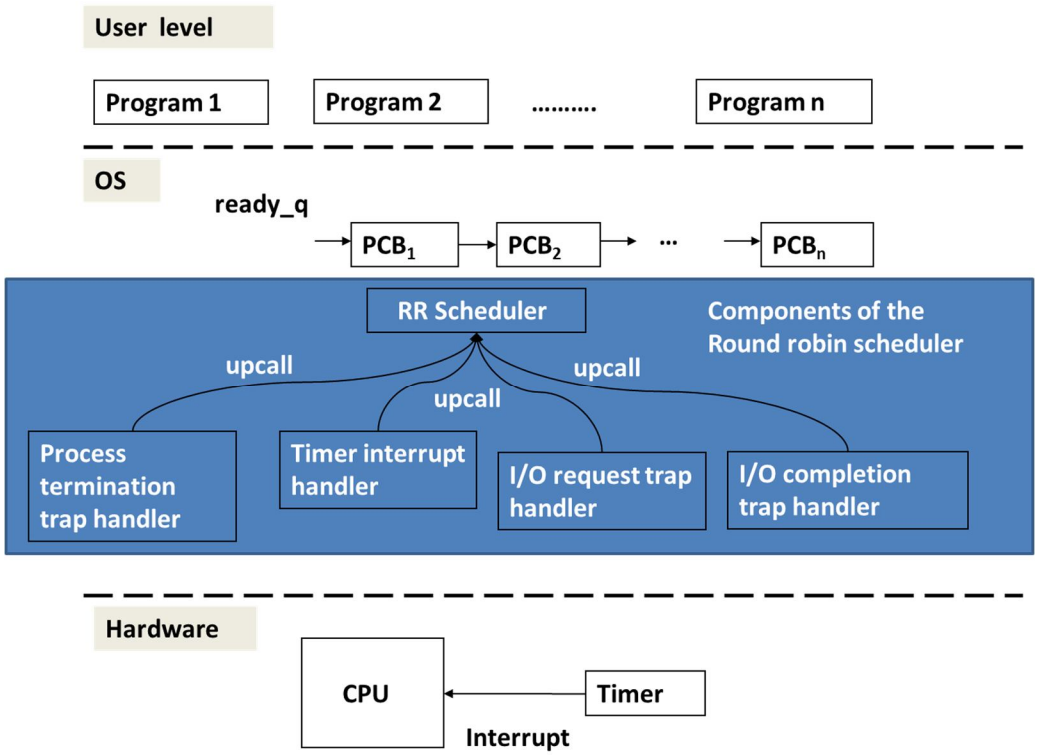
5. (10 points, 5 min)
Given the picture of the RR scheduler:



Fill in functionally the work to be done in each of the components of the RR scheduling framework (your work on the next page).

The level of detail expected for the "work to be done" is ("get head of the ready_q"; "dispatch selected PCB on the processor"; "upcall to RR Scheduler"; "save context of running process in PCB"; etc.).

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RR Scheduler:

Timer interrupt handler:

I/O request trap:

I/O completion interrupt handler:

Process termination trap handler:

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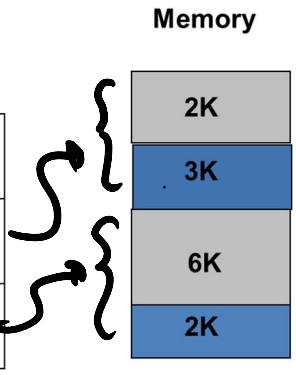
Memory Management and Virtual Memory (Note: K = 1024)

6. (10 points, 5 min)

(a) Consider the following allocation table with fixed-size partition memory allocation.

Allocation table

Occupied bit	Partition Size	Process
1	5K	P2 (need 2K)
1	8K	P1 (need 6K)



(i) (2 points) How much is the internal fragmentation?

(ii) (2 points) How much is the external fragmentation?

(b) (3 points)
Virtual address is 32 bits; pagesize 4 Kbytes; How many entries are there in the page table?

(c) (3 points)
For the same memory system as in (b), the physical address is 24 bits. How many physical page frames does the memory system have?

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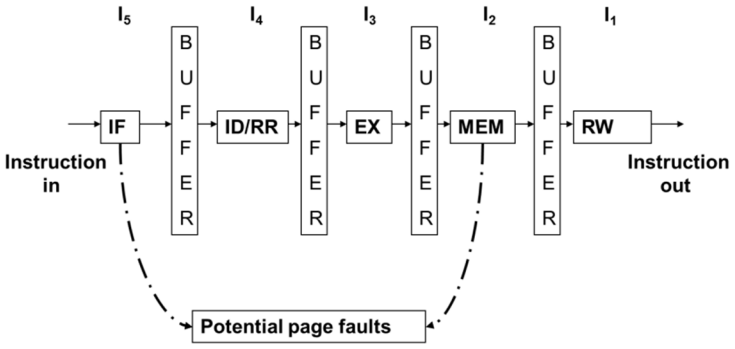
Demand paging, Working set, page replacement

7. (20 points, 15 min)

(a) Consider a 5-stage piplelined processor, which uses demand-paged virtual memory management. **Instruction I2 incurs a page fault.**



(i) (2 points) What will happen to the instructions in flight in the processor?

(ii) (2 points) At which instruction will the program be resumed?

(iii) (2 points) What additional information is needed to be carried along in the buffers between the stages for demand paging to work in a pipelined processor?

(b) (2 points)
In page-based virtual memory system, what information is in the PCB that identifies to the OS the memory space occupied by the process?

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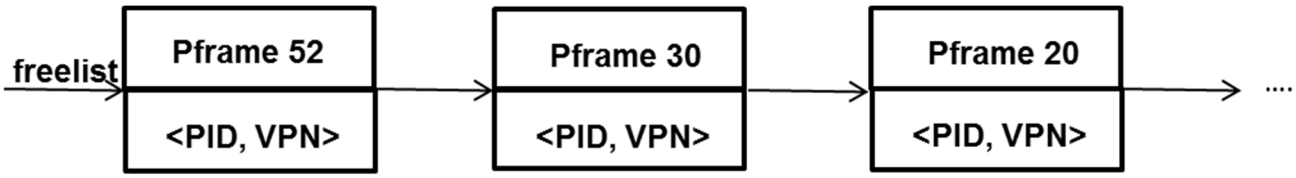
(c) (3 points)
The freelist (as shown below) is a data structure of the memory manager that contains the pool of page frames that are available for allocation to satisfy page faults.



Each entry in the freelist, shows the page frame number that is available for allocation as well as the reverse mapping, i.e., the process-ID and the VPN of that process that was hosted in this page frame. What is the purpose of this reverse mapping for a page frame that is in the freelist?

(d) (3 points)
Why is it infeasible to implement a true LRU algorithm for page replacement in the operating system?

(e) (2 points)
What is the difference between a simple FIFO page replacement algorithm and the “second chance” page replacement scheme(aka “clock” algorithm)?

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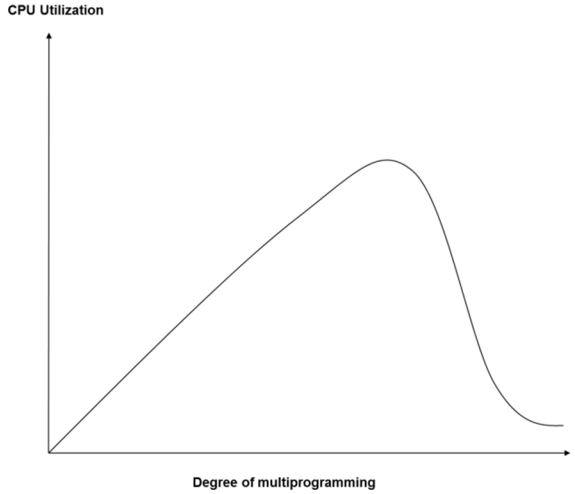
(f)



(i) (2 points) In the picture above, why does the CPU utilization increase as we increase the degree of multiprogramming?

(ii) (2 points) Why does CPU utilization start decreasing beyond a certain point?

TLB and Processor Cache (Note: K = 1024)

8. (20 points, 10 min)

(a) (4 points)

A TLB is a small table implemented in hardware to speed up memory access in a virtual memory system. Explain the principle behind the concept of a TLB.

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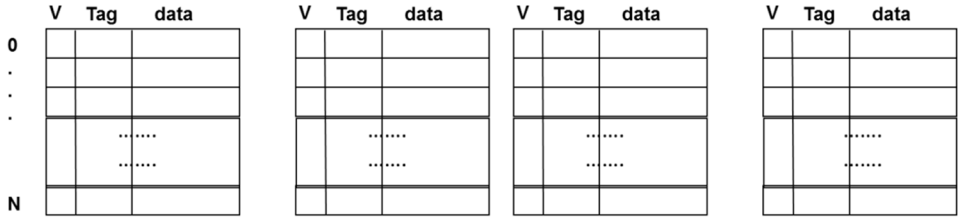
(b) (4 points)
What is motivation for implementing the cache closest to the CPU as a "virtually indexed and physically tagged" cache?

(c) (2 points)
Why are the caches not implemented using the virtual address for both index and tag?

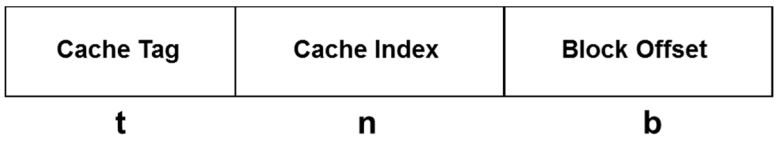
(d)
Consider a 4-way set associative cache with the following parameters:



- Cache size (i.e, the amount of actual data it can hold) of **128 Kbytes**
- **32-bit byte-addressable** memory
- Each memory word contains **4 bytes**
- cache block size is **16 bytes**.
- **write-through** policy.
- **one valid bit** per block.

(i) (4 points) How big is **N** in the above picture (show your work)?

(ii) (6 points) The 32-bit memory address is split into block offset, tag, and index as shown below:



What are the values of **t**, **n**, and **b** (show your work)?