EECE8010

Embedded Systems Hardware Design

Milestone #6 – Test Plan Document

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Contents

1 Introduction

1.1 Objective

Provide a detailed testing plan for all components and on-board peripherals for the Embedded systems hardware design PCB.

1.2 Scope

This document covers all interface signal level checking for the STM32 Nucleo-64 board and connected peripherals on the PCB. All power level and oscillator waveform test plans are also covered.

Only simple software that performs basic functions of the peripherals are tested. Testing of advanced software functions for the MCU are not covered in this document. The STM32 Nucleo-64 board internal testing is not covered in this document.

1.3 Audience

The intended audience is embedded systems development students and instructors; however, this document can easily be understood by any engineer or tester in the embedded systems development field.

1.4 System Block Diagram

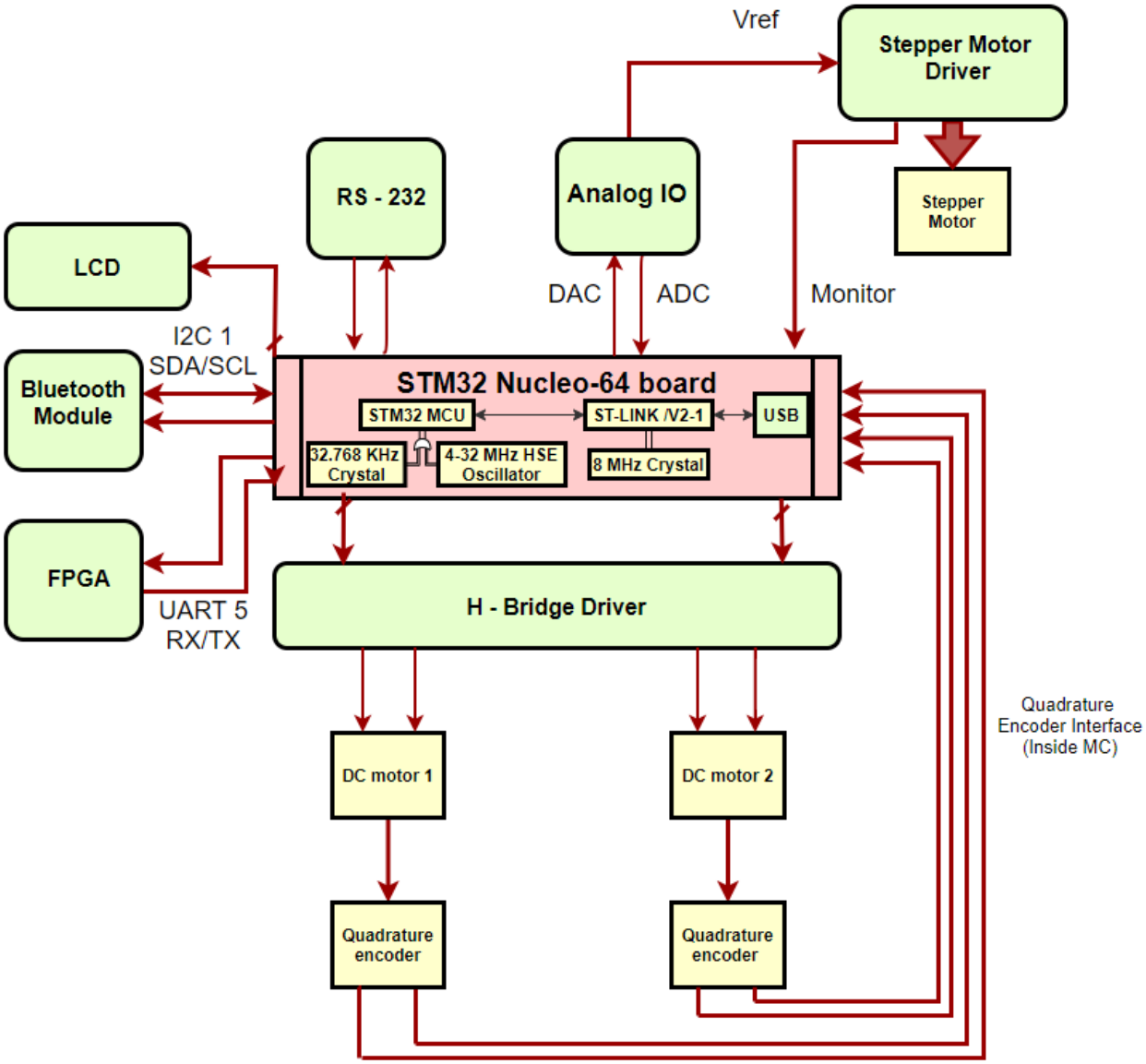

Figure 1
System block diagram

2 VISUAL INSPECTION

2.1 Individual Component Inspection

Print out the bill of materials for the project. Using this as a checklist, check each component for the following:

i. Good solder connection
ii. Proper orientation
iii. Correct values

2.2 Solder Check

Check all solder joints for short/open circuits. Record any deficiencies below:

2.3 Jumper Check

There are two jumpers for the command selector P2 that must always be on the same rows. A connectivity check should be performed to determine proper functionality as shown in table 1.

Table 1
Jumper connections

Jumper position	Expected connections	Connections satisfied (Y/N)
Rows 1 and 2	PC11 connected to URX232 PC10 connected to UTX232	
Rows 2 and 3	PC11 connected to UTXBT PC10 connected to URXBT	
Rows 3 and 4	URX232 connected to URXBT UTX232 connected to UTXBT	

3 POWER SUPPLIES AND REGULATORS

3.1 Current Monitoring

Connect a DC power supply with current-limiting feature to power up the Nucleo-64 board before and after plugging it to the PCB and record the readings. Observe the current and make sure it does not go beyond specifications. If current consumption required is greater than 300 mA, an external power source must be connected to E5V or VIN following the instruction in table 2.

Table 2
Current limitations

Input power name	Connectors pins	Voltage range	Max current	Limitations
VIN	CN6 pin 6 CH7 pin 24	7 V to 12 V	800 mA	800 mA when Vin=7 V 450 mA when 7 V<Vin <= 9 V 250 mA when 9 V<Vin <=12 V
E5V	CH7 pin 6	4.75 V to 5.25 V	500 mA	-

3.2 Voltage Verification

Measure the regulated voltage from the Nucleo-64 board. Ensure that it is within the specified accepted tolerance range. Record the measurements in table 3.

Table 3
Voltage verification

Voltage at Nucleo-64 board	Location	Expected	Measured
3.3 V	CH7 pin 16	3.3 V	
5 V	CH7 pin 18	5 V	
GND	CH7 pins 8, 19, 20 and 22 CH10 pins 9 and 20	0 V	

3.3 Power Pin Verification

Measure voltage levels at all power terminals as shown in table 4.

Table 4
Power pin verification

Location		Expected Voltage	Measured voltage
U3	Pin 11	3.3 V	
	Pin 12	GND	
	Pin 15	GND	
	Pin 22	GND	
U4	Pin 14	3.3 V	
	Pin 2	GND	
	Pin 13	GND	
U1	Pin 15	GND	
	Pin 16	3.3 V	
P5	Pin 2	5 V	
	Pin 15	5 V	
	Pin 1	GND	
P11	Pin 4	GND	
U2	Pin 20	5 V	
P5	Pin 4	GND	
	Pin 5	GND	
	Pin 6	GND	
	Pin 7	GND	
	Pin 14	GND	
	Pin 15	GND	
	Pin 16	GND	
	Pin 17	GND	
P6	Pin 2	3.3 V	
	Pin 4	GND	
P1	Pin 2	3.3 V	
	Pin 4	GND	
P4	Pin 1	GND	
P8	Pin 1	GND	
J1	Pin 5	GND	

4 RESET AND CLOCK CIRCUIT

4.1 Functionality Check

The reset signal is output to the NSRT pin on the STM32 Nucleo- 64 board. An external reset can be triggered by pushing the B2 RESET button on the board. An internal reset can be triggered from many sources through software this is shown in more detail in figure 3.

4.2 Waveform Check

Analyze the reset waveforms. They should match the specs of the device being reset. NSRT Input low level voltage 0.3VDD + 0.07V(MAX), NSRT Input low level voltage 0.445VDD + 0.398(MIN).

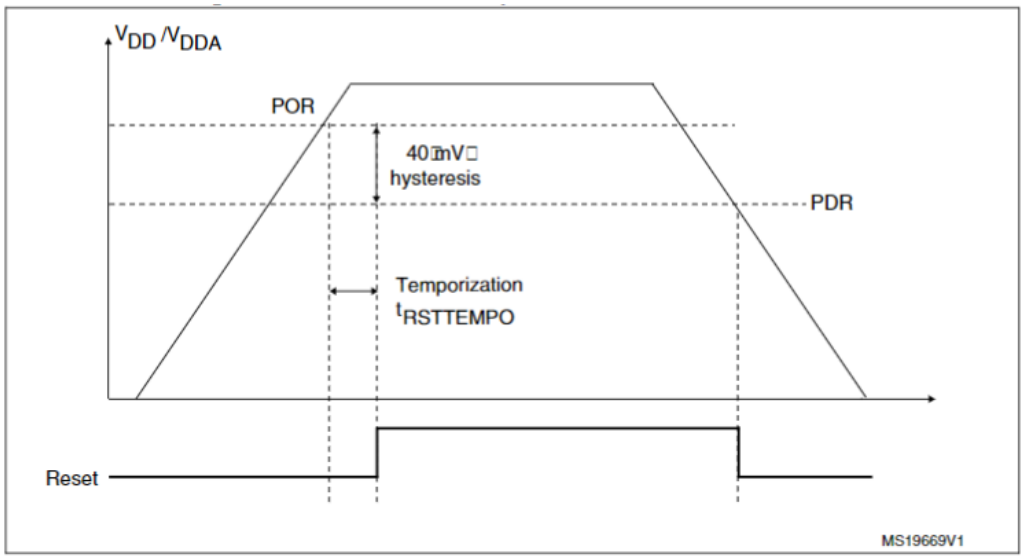

Figure 2
Power on reset/power down reset waveform

4.3 Rise/Fall time Check

The rise and fall times for the reset signal is 125 ns.

The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

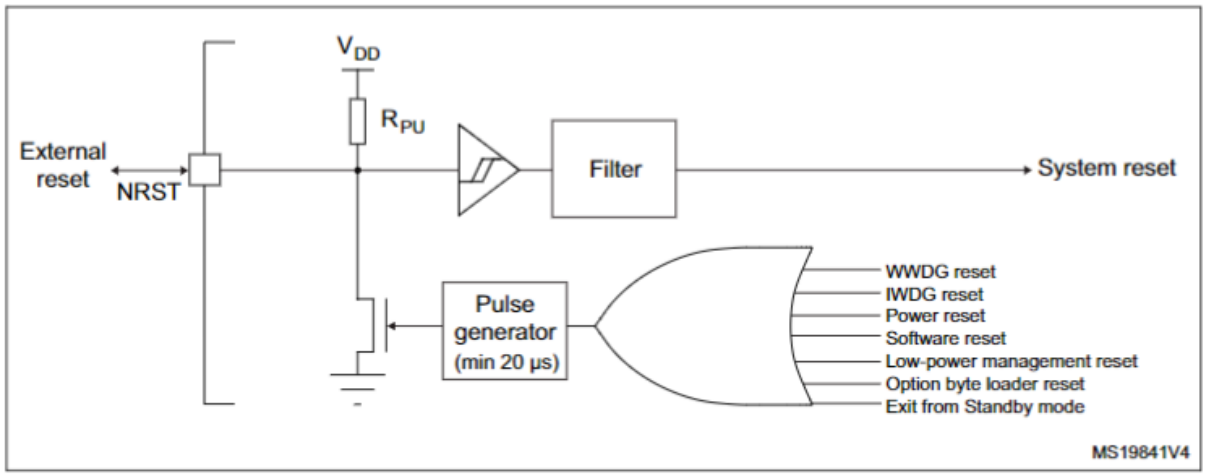

Figure 3
Simplified diagram of reset circuit

4.4 Oscillator Frequency Check

Use an oscilloscope to measure the oscillator frequency and ensure that it is within accepted range. Test oscillators after reset and initialize MCU to default configurations. Record the results in table 5.

For the MCU, there are two oscillators that need to be verified, the HSE oscillator that has a range of frequencies from 4 – 32 MHz (8 MHz by default) and the X2 crystal which has a frequency of 32.768 KHz.

The HSE oscillator pins are *OSC_IN* PF0 pin, *OSC_OUT* PF1 pin.

The X2 Crystal pins are *OSC32_IN* PC14 pin, *OSC32_OUT* PC15 pin.

For the ST-LINK V2-1 there is an X1 Crystal that has a frequency of 8 MHz.

Table 5
Oscillator frequency check

MCU Oscillators	Expected Frequency	Measured Frequency
HSE	8 MHz	
X2 Crystal	32.768 KHz	
ST-LINK V2-1 Oscillators		
X1 Crystal	8 MHz	

5 MICROCONTROLLER TESTING

5.1 Interface Timing Checks

Measure the rising and falling time of the outputs and compare them with expected values shown in table 6.

Table 6
Switching time for outputs

Speed mode	Rising time	Falling time
Low	125 ns	125 ns
Medium	25 ns	25 ns
High	8 ns	8 ns

5.2 Interface Signal Level Checks

Measure the minimum and maximum voltages for the analog input as shown in table 7. Measure the voltage of all I/O pins. Record the signal level for outputs at logic ‘1’ and logic ‘0’ and ensure that it is within specified range as shown in table 8. Record the signal level for inputs and ensure that readings do not exceed the specified limits for V_{IL} and V_{IH} as shown in table 9.

Table 7
Analog I/O port voltages

Analog I/O					
Pin name	**Function**	**Expected minimum voltage**	**Measured minimum voltage**	**Expected maximum voltage**	**Measured maximum voltage**
PC1	ADC INPUT	GND		VDD	
PC0	ADC INPUT	GND		VDD	
PC2	ADC INPUT	GND		VDD	
PA4	DAC_STEP_VREF	GND		VDD	

Table 8
Output signal levels

Outputs					
Pin name	**Function**	**Expected Voltage at logic '1'**	**Measured Voltage at logic '1'**	**Expected Voltage at logic '0'**	**Measured Voltage at logic '0'**
PC10	UART4_TX	2.4 V>Vout>VDD		< 0.4 V	
PC12	UART5_TX	2.4 V>Vout>VDD		< 0.4 V	
PA15	BT APP. MODE	2.4 V>Vout>VDD		< 0.4 V	
PB7	LCD_D7	2.4 V>Vout>VDD		< 0.4 V	
PC3	STEP_RST	2.4 V>Vout>VDD		< 0.4 V	
PA0	DC_MOTOR1_DIR1	2.4 V>Vout>VDD		< 0.4 V	
PA1	DC_MOTOR1_DIR2	2.4 V>Vout>VDD		< 0.4 V	
PB0	UART TX/RX INDICAT.	2.4 V>Vout>VDD		< 0.4 V	
PB8	I2C1_SCL	2.4 V>Vout>VDD		< 0.4 V	
PB9	I2C1_SDA	2.4 V>Vout>VDD		< 0.4 V	
PA5	FEEDB. TO FPGA	2.4 V>Vout>VDD		< 0.4 V	
PB6	LCD_D6	2.4 V>Vout>VDD		< 0.4 V	
PA9	PWM_DC_MOTOR2	2.4 V>Vout>VDD		< 0.4 V	
PA8	PWM_DC_MOTOR1	2.4 V>Vout>VDD		< 0.4 V	
PB10	DC_MOTOR2_DIR1	2.4 V>Vout>VDD		< 0.4 V	
PB4	LCD_D4	2.4 V>Vout>VDD		< 0.4 V	
PB5	LCD_D5	2.4 V>Vout>VDD		< 0.4 V	
PA10	LCD_BKLT	2.4 V>Vout>VDD		< 0.4 V	
PC8	STEP. POWER SAVE	2.4 V>Vout>VDD		< 0.4 V	
PC5	STEP. DIRECTION	2.4 V>Vout>VDD		< 0.4 V	
PB12	LCD_ENABLE	2.4 V>Vout>VDD		< 0.4 V	
PB11	DC_MOTOR2_DIR2	2.4 V>Vout>VDD		< 0.4 V	
PB2	BLUETOOTH	2.4 V>Vout>VDD		< 0.4 V	
PB1	BLUETOOTH	2.4 V>Vout>VDD		< 0.4 V	
PB15	LCD_RW	2.4 V>Vout>VDD		< 0.4 V	
PB14	STEP SIGNAL	2.4 V>Vout>VDD		< 0.4 V	
PB13	LCD_RS	2.4 V>Vout>VDD		< 0.4 V	
PC4	STEP. OUTPUT ENAB.	2.4 V>Vout>VDD		< 0.4 V	

Table 9
Input signal levels

Inputs					
Pin name	**Function**	**Expected Voltage at logic '1'**	**Measured Voltage at logic '1'**	**Expected Voltage at logic '0'**	**Measured Voltage at logic '0'**
PC11	UART4_RX	> 0.5 VDD + 0.2 V		< 0.475 VDD - 0.2 V	
PD2	UART5_RX	> 0.5 VDD + 0.2 V		< 0.475 VDD - 0.2 V	
PC9	STEP. MONITOR	> 0.5 VDD + 0.2 V		< 0.475 VDD - 0.2 V	
PA6	DC_M1_ENCOD_A	> 0.445 VDD + 0.398 V		< 0.3 VDD + 0.07 V	
PA7	DC_M1_ENCOD_B	> 0.445 VDD + 0.398 V		< 0.3 VDD + 0.07 V	
PA12	DC_M2_ENCOD_B	> 0.5 VDD + 0.2 V		< 0.475 VDD - 0.2 V	
PA11	DC_M2_ENCOD_A	> 0.5 VDD + 0.2 V		< 0.475 VDD - 0.2 V	

5.3 RAM / Memory Testing

This test has already been done by STM.

5.4 BDM Testing

This test has already been done by STM.

6 SOFTWARE LOADING & PERIPHERAL TESTING

6.1 Software Loading

Load a test program to the MCU to check the functionality of each interface at a time.

6.2 RS-232 Interface

Test the logic level conversion for MAX3232 Tx and Rx using a square wave signal at the Tx pin and an oscilloscope at the Rx pin on both directions. Ensure that the slew rate and output voltage levels are within range as shown in table 10.

Table 10
RS-232 interface test

Parameter	Expected value	Measured value
Slew rate	4 – 30 V/µs	
Output Voltage Low	< 0.4 V	
Output Voltage High	> VCC – 0.6 V	

6.3 H-Bridge Driver

Perform a test on the tristate buffer (pins 1 and 11 for motor 1 and motor 2 respectively) for different frequencies. Test the functionality of the direction control pins.

6.4 DC Motor and Feedback

Test the voltage levels at the motor terminals and compare it with VMOTOR. Using an oscilloscope, observe the encoder signals for both motors and record the results in table 11.

Table 11
DC motor interface check

Interface	I/O port	Pass/fail
DC motor	OUT1	
	OUT2	
	OUT3	
	OUT4	
	M1_ENCODER_A	
	M1_ENCODER_B	
	M2_ENCODER_A	
	M2_ENCODER_B	

6.5 LCD

Check the logic level on each pin by referring to section 5.2. Record the results in table 12.

Table 12
LCD interface check

Interface	I/O port	Pass/fail
LCD	LCD_RS	
	LCD_RW	
	LCD_ENABLE	
	LCD_D4	
	LCD_D5	
	LCD_D6	
	LCD_D7	
	LCD_BKLT	

Test each character on the screen for both lines along with the brightness.

6.6 DAC

The test software implements a simple DAC command to convert user inserted voltages to the corresponding analog voltage from 0 to 3.3V. Test that the correct voltage is being output to pin PA4.

The DAC can be configured to display a wider range of voltages using the AVDD pin. To verify that the correct values are being displayed use the formula below, where N = 12 for 12-bit resolution.

$$Analog\ Value = \frac{Reference\ voltage}{2^N - 1} \times Digital\ value\ , N = resolution\ bits$$

6.7 ADC

The test software implements a simple ADC command that reads voltages over the range 0<Analog Value<3.3 then converts the value to 0<Digital Value<4096 (12-bit resolution), using the circuit displayed in figure 4 verify that the conversion is being performed as expected for the Analog Value range. ADC pins are PC0, PC1, and PC2 for channels 1, 2, and 3 respectively.

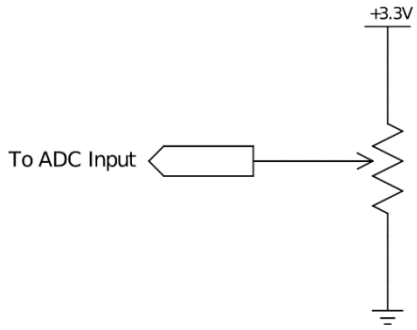

Figure 4
Simple circuit configuration to test ADC

The AVDD and AGND pins can be used to adjust the range of the ADC, to test that the ADC is performing correctly use the formula below.

$$Digital\ Value = \frac{Voltage\ drop\ \times (2^N - 1)}{Reference\ voltage}\ , N = resolution\ bits$$

6.8 Stepper Motor Driver

Test the pins listed in table 13 for their expected values. Test the CHOP frequency only when the stepper motor is operating.

Table 13
Stepper motor driver interface check

Interface	I/O port	Expected value	Pass/fail
Stepper motor	MD1	3.3 V	
	MD2	3.3 V	
	ATT1	0 V	
	ATT2	0 V	
	CHOP	45.45 KHz	
	VCC	3.3 V	
	GND	0 V	
	PGND	0 V	
	PGND	0 V	

6.9 Stepper Motor

While the stepper motor is operating verify that the output ports for the stepper motor match the frequency of the STEP signal. Check the interface pins and record the results in table 14.

Table 14
Stepper motor interface check

Interface	I/O port	Pass/fail
Stepper motor	OUT1A	
	OUT1B	
	OUT2A	
	OUT2B	

6.10 Bluetooth

6.10.1 Interface Signal Level Checks

Measure the interfaces of the Bluetooth module and record the results in table 15.

Note that VDD is 1.9 – 3.6 V

Table 15
Bluetooth interface check

Pin #	Pin name	Expected Voltage level at logic '1'	Measured Voltage level at logic '1'	Expected Voltage level at logic '0'	Measured Voltage level at logic '0'
1	NC	N/A	N/A	N/A	N/A
2	GND	0		0	
3	P1_2	0.8VDD - VDD		0 - 0.2VDD	
4	P1_3	0.7VDD - VDD		0 - 0.3VDD	
5	P1_7(NC)	N/A	N/A	N/A	N/A
6	P1_6	0.7VDD - VDD		0 - 0.3VDD	
7	UART_RX	0.7VDD - VDD		0 - 0.3VDD	
8	UART_TX	0.8VDD - VDD		0 - 0.2VDD	
9	P3_6(NC)	N/A	N/A	N/A	N/A
10	RST_N	0 - 0.3VDD		0.7VDD - VDD	
11	PO_0	0		0	
12	P0_2	0 - 0.2VDD		0.8VDD - VDD	
13	GND	0		0	
14	VBAT	VDD		N/A	N/A
15	P2_7	0 - 0.2VDD		0.8VDD - VDD	
16	P2_0	0.7VDD - VDD		0 - 0.3VDD	

6.10.2 Functionality Check

Connect to the Bluetooth module via the RS-232 interface to a host CPU after the test software has been loaded onto the MCU. Using a serial capture program (e.g. Realterm) establish a connection to the Bluetooth module. To test that a connection has been established enter the following commands in the terminal:

- $$$ to enter command mode
- + <text> If a connection is established the entered text should be echoed back to the terminal.
-]W, <hex8 32bytes data> If the I2C is setup correctly an AOK should be returned to the terminal.

The default UART settings for the Bluetooth is shown in table 16.

Table 16
Bluetooth default UART settings

UART setting	Default value
Baud rate	115200
Data bits	8
Parity	None
Stop bits	1
Flow control	Disabled

6.11 FPGA

Check the logic level on pins used between MCU and FPGA by referring to section 5.2. Record the results in table 17.

Table 17
FPGA test

Interface	I/O port	Pass/fail
FPGA	UART5_TX	
	UART5_RX	
	FEEDBACK	

6.12 Module Testing

Test each module at a time and record the results in table 18.

Table 18
Module testing

Module	Pass/fail
DC Motor	
Stepper Motor	
LCD	
Bluetooth	
FPGA	
Analog I/O	

7 SYSTEM LEVEL TESTING

7.1 System Level Software

Use a test program to check the whole system working together at the same time.

7.2 Performance Testing

Push the system to its boundaries to test the system's performance as follows:

- Test DC motors and stepper motor at different speeds including maximum speed.
- Check the performance of the LCD and its brightness.
- Send commands from the FPGA and Bluetooth at the same time and ensure that system operates normally.
- Inject different analog values at the same time and ensure that all inputs are processed correctly.

8 Appendix

8.1 Important Datasheets and manuals

stm32f303xE datasheet

Nucleo-64 board user manual

STM32F303xE reference manual

DC motor driver datasheet

Stepper motor driver datasheet

Stepper motor datasheet

RS-232 datasheet

LCD datasheet

RN4871 Bluetooth module user guide

RN4871 Bluetooth module datasheet