

## Department of Electrical & Computer Engineering North South University

Project Title: A 12-bit Custom RISC-V Control Unit

Course: CSE 332 - Computer Organization & Architecture

Section – 06

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## **Submitted by:**

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## **Control Unit for 12-bit ISA:**

Operation	Opcode	RT/RD	Write Enable	ALU Source	Sub	Load Enable	Store Enable	Jump Control	Beq Control	RAM to Reg
add	000	1	1	0	0	0	0	0	0	0
sub	001	1	1	0	1	0	0	0	0	0
addi	010	0	1	1	0	0	0	0	0	0
lw	011	0	1	1	0	1	0	0	0	1
SW	100	0	0	1	0	0	1	0	0	0
and	101	1	1	0	0	0	0	0	0	0
beq	110	0	0	0	1	0	0	0	1	0
jmp	111	0	0	0	0	0	0	1	0	0