

Project 4 Cache Coherence --- project in Adv Computer Architecture

Cache Coherence means:

* Read what is written.

A read of X on P_1 , return most recently written value of X by P_1 if no other processing element written to X .

* Coherent writes seen by all processors (eventually).

For example, if P_1 writes to X and after sufficient time, P_2 reads X , P_2 gets the value P_1 wrote.

* Write Causality: writes to the same location are serialized, and all PE's see the same order of writes.

Goal of Project:

Creating a simulator that maintains coherent caches for a 4, 8, and 16 core CMP.

Implementing the MSI, MESI, MOSSI, MOESI, and MOESIF protocols for a bus-based broadcast system.

Some Important Functions:

send_getM(); // Gets(block) - get clean copy of block

send_getS(); // GetM(block) - get a copy with intent to modify.

send_DATA_on_bus(); // Data sent on the bus.

send_DATA_to_proc(); // Data sent from a cache to proc.

set_shared_line(); // Set the bus shared line.

get_shared_line(); // Find out if the shared line is active.

State Diagrams of Processor Transactions, Bus Transactions:

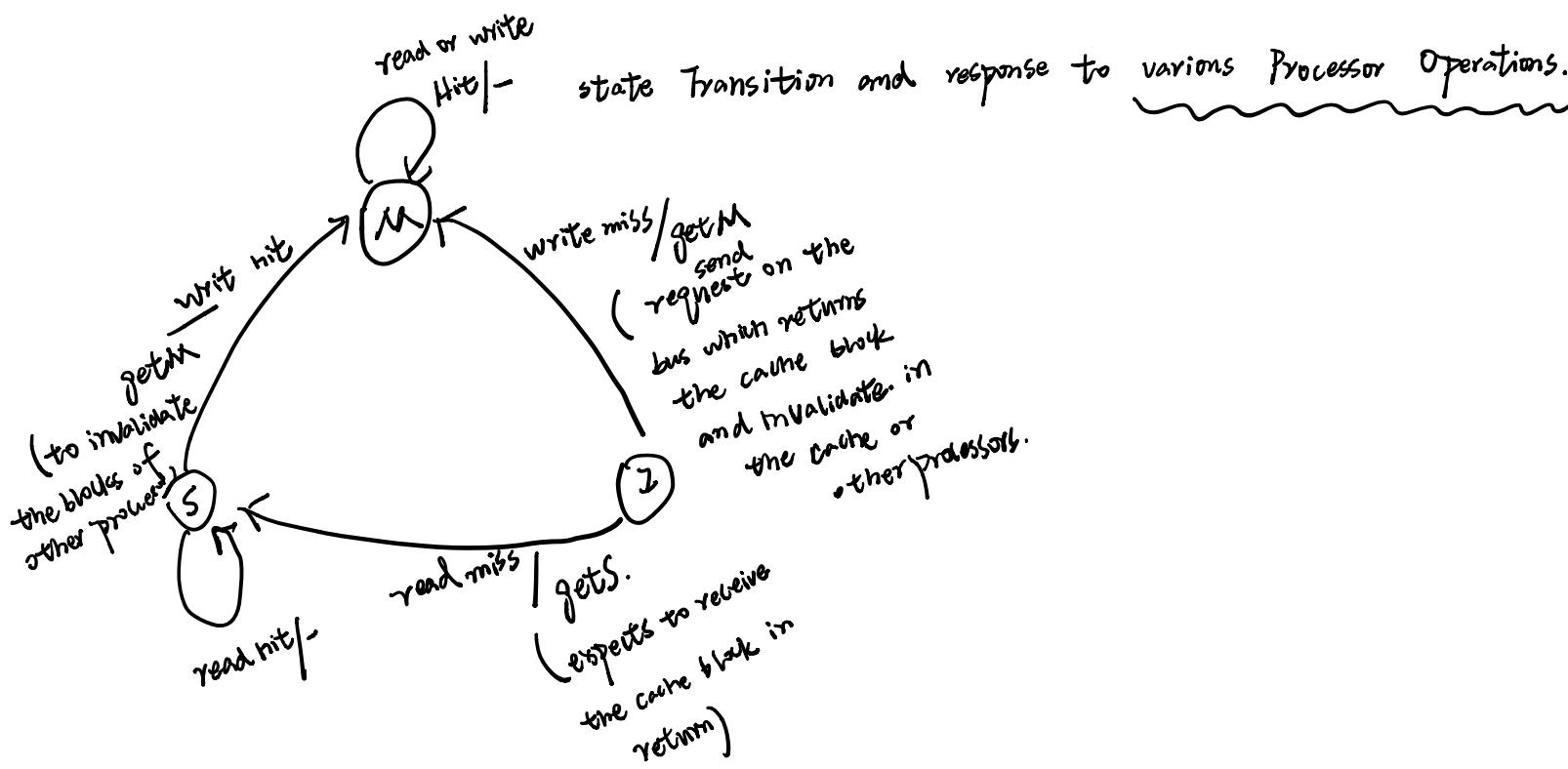
MSI:

Modified (M): The block has been modified in the cache.

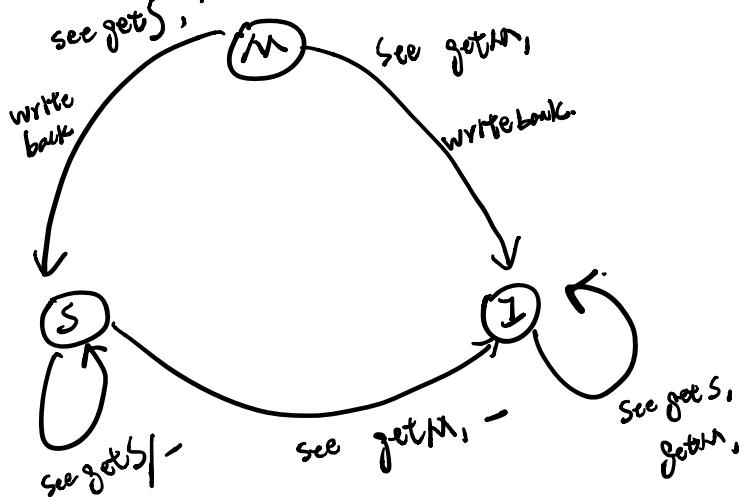
Shared (S): The block is unmodified and exists in read-only state in at least one cache.

Invalid (I): The block does not exist in current cache or has been

Invalid (I): The block is either not present in the current cache or has been invalidated by a bus request.



state Transition and response to various Bus Operations.



MESI

Modified (M): Cache line is present only in the current cache, and is dirty.

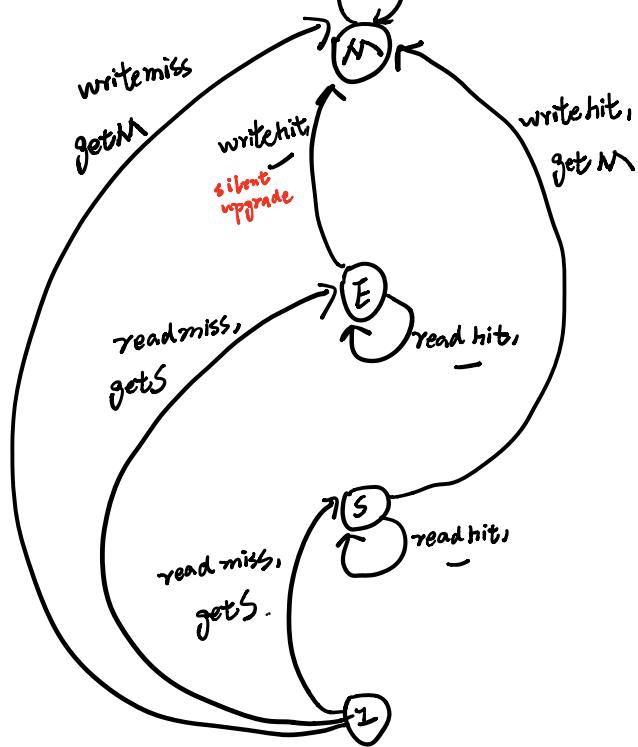
Exclusive (E): Cache line is present only in the current cache, but is clean.

Shared (S): this cache line may be stored in other caches of the machines and is clean.

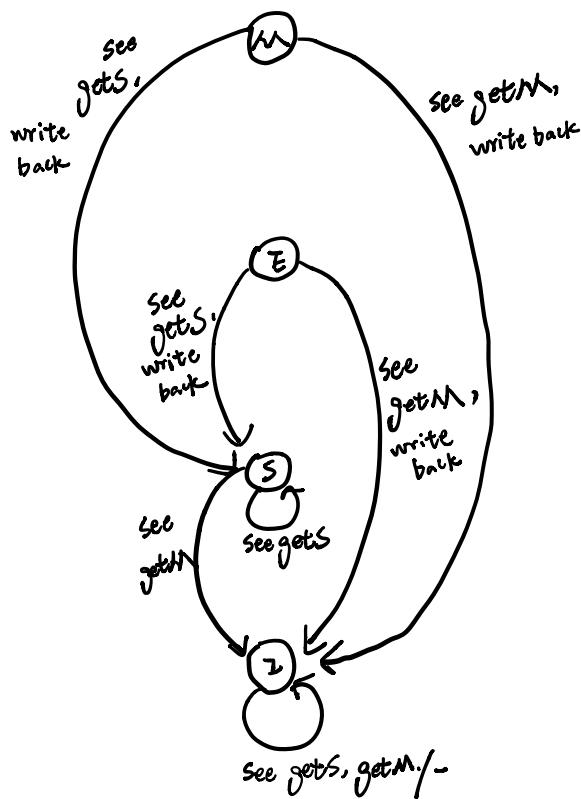
Invalid (I): this cache line is invalid.

state Transition and response to various Processor Operations.

read/write hit, -



State Transitions and response to various Bus Operations.



MDSI

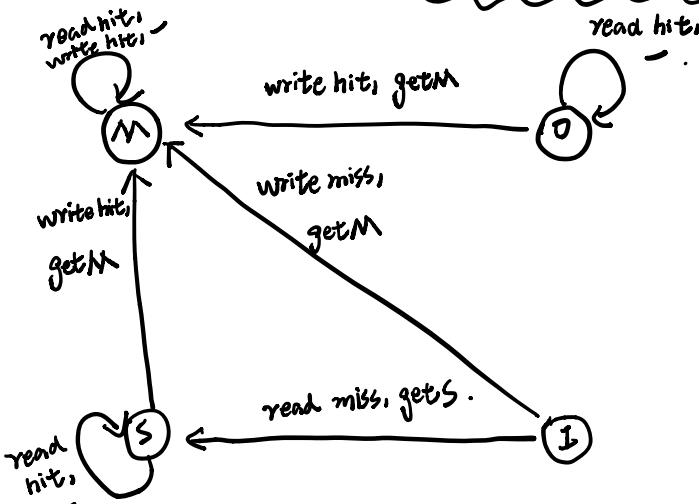
Modified (M) - Only one cache has a valid copy of the block and the value is likely to be different from the one in main memory.

Dirty (D) - Multiple caches may hold the most recent and correct value of a block and the value in main memory may or may not be correct.

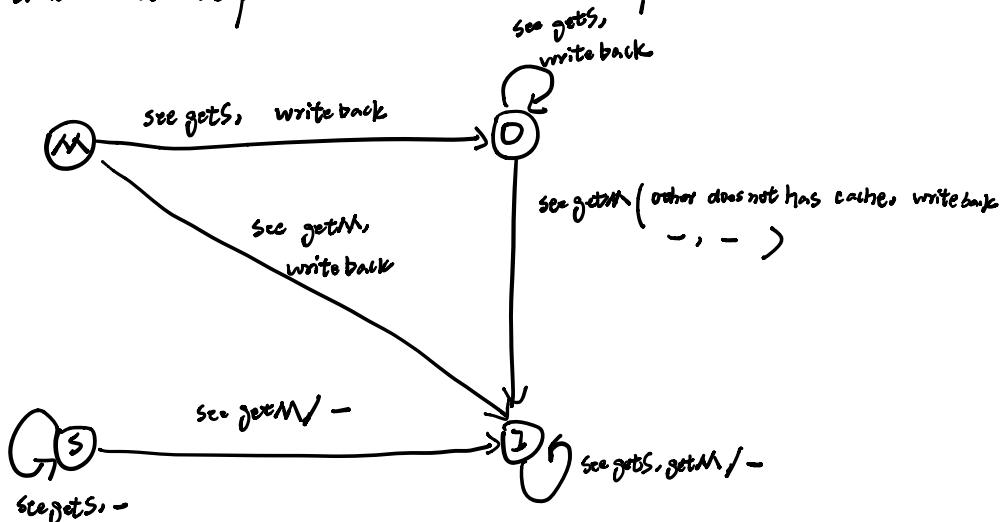
Shared (S) - Cache block is valid, could be shared by multiple caches, and may or may not have the same value as the main memory.

Invalid (I) - Cache block is invalid.

state Transition and response to various Processor Operations.



State Transitions and response to various Bus Operations.



MOESI

Modified (M) - This cache has the only valid copy of the cache line, and has made changes to that copy.

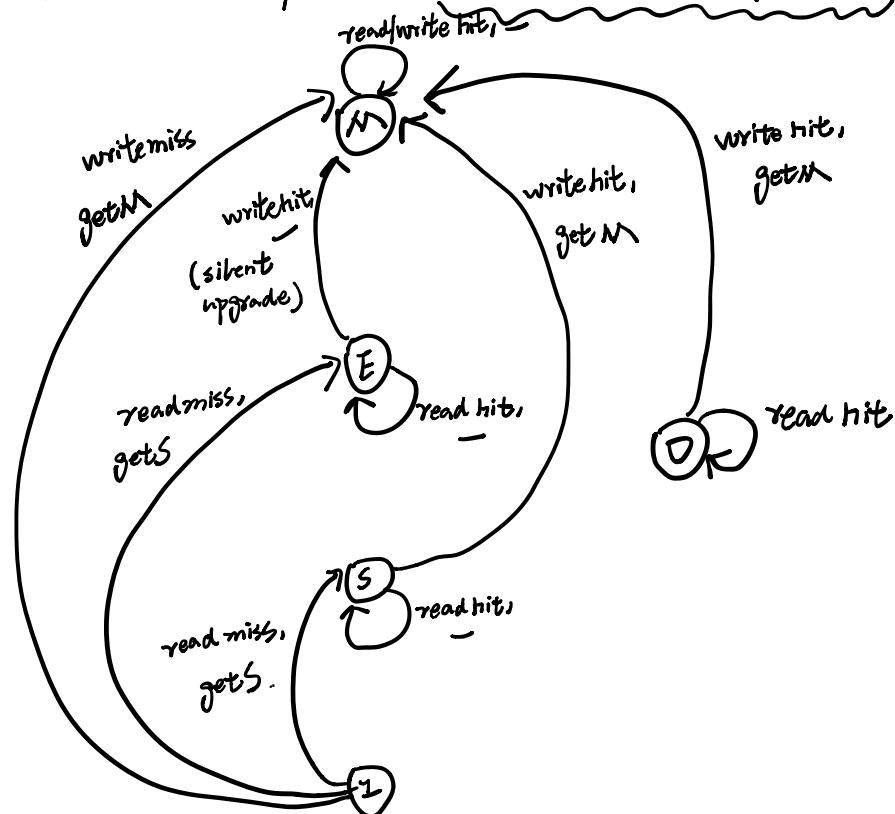
Owned (O) - This cache is one of several with a valid copy of the cache line, but has the exclusive right to make changes to it.

Exclusive (E) - This cache has the only copy of the line, but the line is clean.

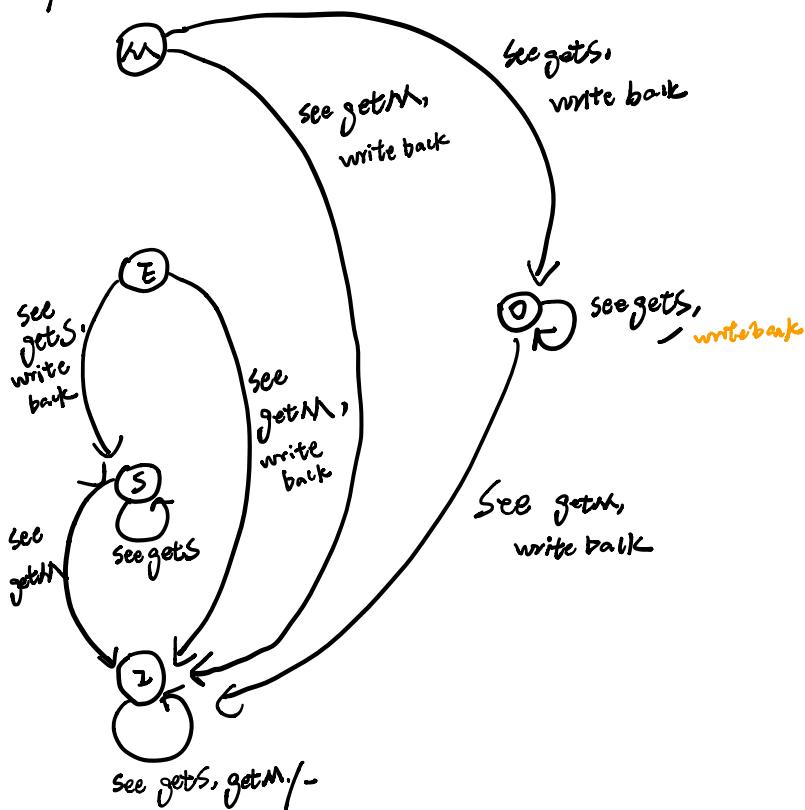
Shared (S) - This line is one of several copies in the system. This cache does not have permission to modify the copy.

Invalid (I) - This block is not valid.

state Transition and response to various Processor Operations.



State Transitions and response to various Bus Operations.



MOESIF

Modified (M)

Owned (D)

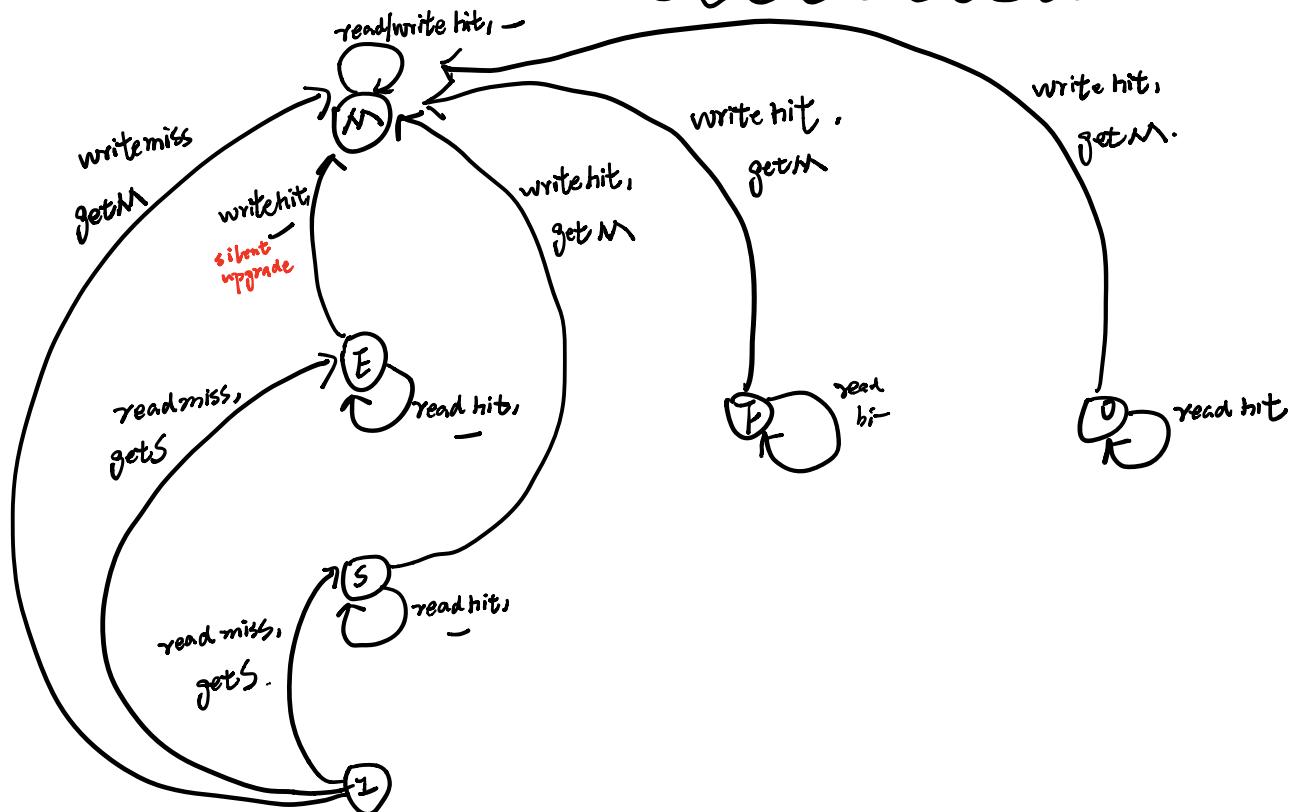
Exclusive (E)

Shared (S)

Invalid (I)

Forward (F) : cache line in the F state is clean and maybe discarded at any time without notice.

state Transition and response to various Processor Operations.



State Transitions and response to various Bus Operations.

